Technical Approach Document:

Team Name : *Red Electrical Devils by CE+T*	**Registration Code :** *545_9151f5_56568*

General overview and innovations

The use of GaN technology enables a power density of ~145 W/in.³ for the 2 kVA inverter designed for this project. The dimensions are 2.5 x 1.615 x 3.41 in. with a **volume of 13.77 inches³.**

GaN transistors have many very interesting electrical characteristics (low R_{ds_on}, low Q_{gate} and C_{ds}, ultra low Q_{rr}); these create technological advantages over current MOSFET and IGBT devices (small size and low production costs). Unfortunately, they also have serious drawbacks due to their very fast switching characteristics: they are challenging to drive and require sensitive electromagnetic noise management. Another pitfall is the high voltage drop due to the reverse current when the GaN is turned off. **The solution selected to overcome these difficulties is to control all the GaN transistors using soft switching for the entire operation range**.

In order to combine a continuous current at the 450 V input stage with an alternating 240 V output voltage, we have chosen a **five legs topology** because it minimizes energy transfer within the inverter**.** Two half bridges (HB) generate the neutral voltage, two further half bridges generate the line voltage and the last is used as an active filter.

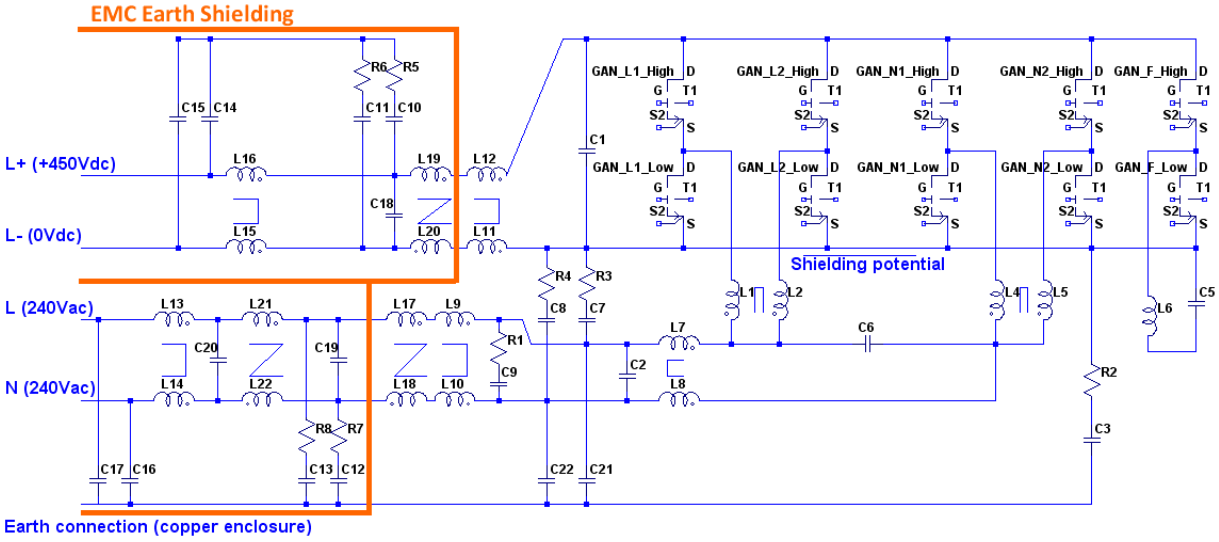

Figure 1: inductors L1 to L6 are rated between 10 µH and 50 µH. Due to the active filter (C5/L6), input capacitor C1 is reduced to less than 15 µF and C5 is rated at less than 150 µF. Common mode inductors (L7 to L16) are rated between 200 µH and 1 mH. The total rating of Y capacitors is more than 500 nF while keeping the leakage current below the allowed value (initially 5 mA) because the output sine wave is symmetric between L+ and L-, i.e. $(V_L + V_N)/2 \sim= (V_{L+} + V_{L-})/2 \sim= V_{Earth}$ with split phase grounding configuration and cancels the leakage current. The EMC differential inductors (L17 to L22) are rated between 10 µH and 20 µH and the X capacitors (C2, C6, C18 to C20) range from 1 µF to 5 µF.

The high density and the high efficiency of this inverter come from optimized control of the five legs. For any type of load, this control achieves soft switching operation of all GaN devices while minimizing reverse currents during the dead times. The algorithm ensures that the module is naturally protected against overcurrents. During the debug phase, we encountered problems due to the high processing load demanded by the control algorithms. We have finally upgraded the processor, using a 40 % faster pin to pin compatible model.

The objectives of the control are achieved with the help of the following principles: digital control based on a fast microcontroller combined with a CPLD; fast measurement of input/output currents and voltages; efficient feedback on the switching events of the HBs; a learning algorithm for the active filter; optimization of the switching frequency between 35 and 240 kHz depending on the output current; a variable phase shift between the HBs (0° or 90°) and a dead time modulation of the five HBs (50 ns to 3 µs). The switching losses are almost canceled and the frequency increase helps to optimize the size of the passive components.

The robustness of the **GaN control** is critical. Indeed, GaNs switch extremely fast so that they generate high dv/dt across the control isolation (far beyond the allowed values for most of the drivers on the market). Furthermore, the gate voltage threshold is very low. We have designed very compact, low cost and extremely robust driver circuitry that can drive GaN transistors well within their specifications.

Selecting the right **GaN package** is also very important. An SMD model with 2 source accesses: one for the power, one for the command, is the best choice for this design. It allows safe control of the transistor. Moreover, a small package reduces the parasitic inductances and consequently the functional overvoltage. The PCB layout and the positioning of the decoupling capacitors are crucial to operating the GaN properly.

The methodology applied comprises: precise dimensioning with analytical calculations and finite element modeling; the use of SPICE simulations for power and control; 3D mechanical modeling; and the use of thermal simulations. This allowed us to create an inverter meeting all the requirements **in only 1 run.**

120 Hz input current/voltage ripple requirement

To meet the ripple requirement on DC input, we have designed a **parallel active filter** that can compensate the ripple more efficiently than using a large capacitor at the input. The adopted solution is also more reliable than the use of a boost based topology for which the working voltages could rise up to the limit V_{max} of the GaN transistors.

The active filter works with higher voltage variations (~200 V_{pk-pk}) and stores the corresponding energy in ceramic capacitors whose capacitance rises as the voltage decreases, leading to three benefits: (1) size reduction of the input tank capacitor (less than 15 µF), (2) size reduction of the **filter capacitor to less than 150 µF**, (3) inverter robustness due to the use of the GaNs below 450 V_{dc}. The software also contributes; the algorithm maintains V_{in} constant while allowing a larger ripple across the active filter. Moreover, a learning algorithm still reduces the input ripple (by a factor of 3) through correction of the modeling errors due to the presence of dead times.

Miniaturization of components for DC-AC conversion

MLC Capacitors for the energy storage lead to a more compact and efficient module.

The **magnetic components** are mainly composed of **ferrite** whose magnetic losses are very low at high frequencies. The use of Litz wires minimizes the losses due to skin and proximity effects. For further miniaturization, the wires are wound directly onto the ferrite, without a coil former. Their cooling is provided by the air flow of the fan and by use of an **aluminum oxide foil placed in the middle of the ferrite** to create the requested air gap plus a thermal drain. The size of the filter capacitors and inductors is optimized by increasing the allowed ripple current.

Concerning the output current, an open loop Hall sensor combined with an electromagnetic shield lead to a very **compact measurement device**, offering galvanic

decoupling and reducing the sensitivity to common mode and parasitic inductance noise. The time response is very short to protect the inverter from short-circuit or high load impacts.

It is important to note that all the other current measurements ($I_{inductor}$, …) are made without current sensors by state observers; this reduces the overall inverter size.

Thanks to a specific **GaN control modulation** which reduces the current within the filter inductors L7-L8, their core size is reduced **without reaching saturation level.**

A sandwich structure for all the PCBs and the heatsink is a real challenge. The use of micro-spring contacts, a custom heatsink made by EDM (Electrical Discharge Machining), an ultra-thin PCB (0.012 inch thick), silicone foam to spread the GaN contact pressure on the heatsink... All these techniques greatly helped to reduce the size of the inverter.

The module comprises mainly two parts. The first includes the control, the auxiliary supply, the five legs and their corresponding drivers together with the heatsink. The second part includes the passive filters.

A **soft switching LLC resonant** topology is used for the isolated **auxiliary supply** 12V/5V/3.3V (~10W). This reduces the volume to less than 0.128 $in.^3$ (0.8 x 0.8 x 0.2 in.), which enables the integration with the control part on a unique PCB.

Thermal management

Based on the estimated and simulated losses, forced air cooling is the only viable solution that sufficiently reduces the thermal resistance with the ambient air. An efficient axial fan (~1.57 x 1.57 x 0.6 in.) is placed in the middle of the front plate.

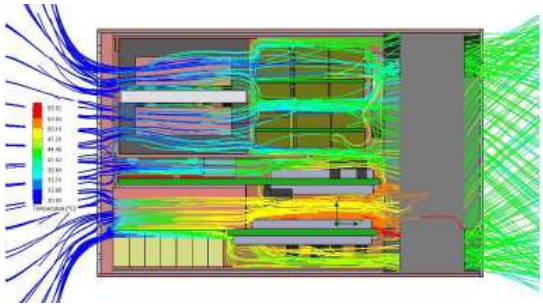

Figure 2: all components are optimally positioned around the fan.
- Hottest components are placed in the direct air flow.
- Exchange surface areas are maximized.
- Pressure losses are minimized.
- Air speed near the side is optimized.
- Fresh air entry is near the GaN heatsink to minimize the thermal resistance, maximizing the inverter efficiency.

The external shield and the heatsink are both made of copper, while the storage capacitors are ceramic MLCC. Both materials were chosen to enhance heat flux and exchange surface area. The capacitor assembly made for the active filter is an energy storage device but is also an extension of the heatsink. The air flow between each MLCC row (gap $\pm$ 0.04 in.) enhances the cooling effect. The volume occupied for the energy storage acts as a second heatsink, due to the assembly geometry and the capacitor type (MLCC).

Several types of **heatsink** were thermally simulated and compared with the 3D model (multiple blades, honeycomb, fins interlaced or not, copper foam...).

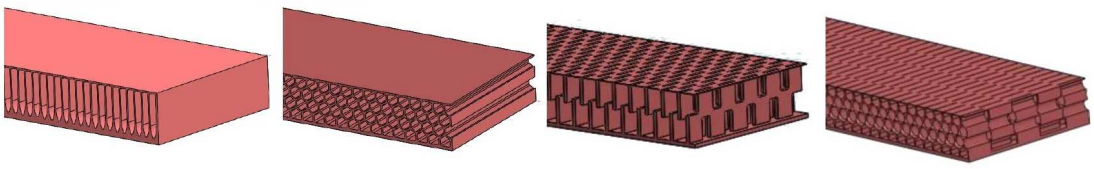

Figure 3: the copper honeycomb heatsink has been selected (Rth_total = 1.3 °C/W; L2.79 x W0.83 x H0.26 in.) because it minimizes GaN temperature and has holes large enough to avoid any clogging by dust. The two-dimensional structure distributes the temperature and reduces the hot spots.

Several inductors are thermally fastened to the shield. In order to meet the external enclosure 60 °C temperature limit, a Gap-Pad provides a thermally conductive interface between the shield and the external module copper enclosure. With this method, the thermal resistance of the interface helps to extract the heat of the hottest inner components and prevent this heat being dissipated by the external enclosure locally.

Choosing the right **thermal interfaces** is then very critical in reducing hot spots on the outer inverter surface. Figure 4 shows the thermal stack. The GaN junction temperature does not exceed 60 °C with an ambient temperature of 30 °C at 2 kW load.

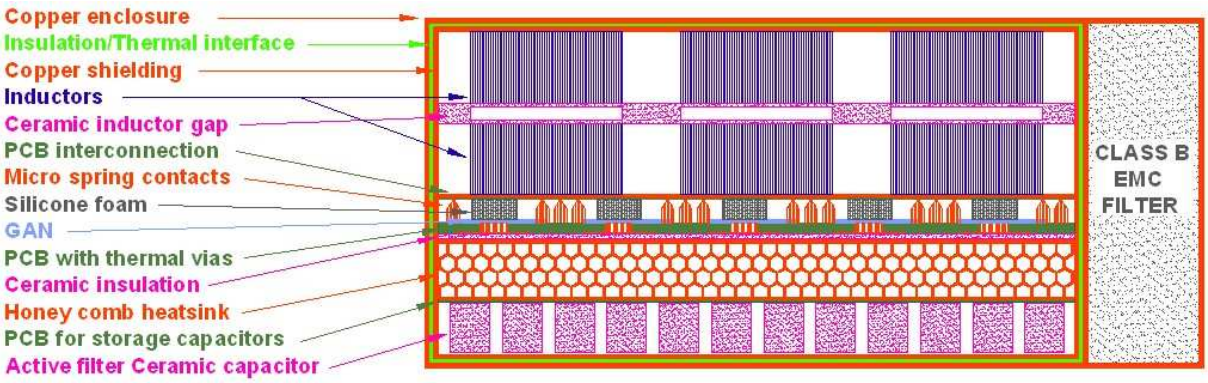

Figure 4: detailed structure of the thermal interfaces. For one GaN transistor (~2 W loss), the thermal impedances are as follows: (1) GaN junction – thermal pad: 0.5 °C/W. (2) Innovative PCB design maximizing heat transfer from the GaN transistor to the heatsink: 1.1 °C/W. (3) thermal compound with aluminum oxide dust: 0.3 °C/W. (4) ceramic insulation foil with aluminum nitride: 0.02 °C/W. (5) thermally conductive glue with silver dust: 0.15 °C/W. (6) honeycomb-shaped heatsink – forced air: 13 °C/W (relative to 1 GaN).

Electromagnetic Compliance (EMC)

In order to be compliant with FCC part 15 class B, the choice of topology and the type of modulation has been based on the noise source models. Each filter has been simulated with the established noise model to optimize the inductor design and the PCB routing. Key factors for meeting class B can be summarized as follows: soft switching operation of the main switches and auxiliary supply independently of the load; variable frequency and a specific spread spectrum modulation; a first internal shield electrically connected to (L-); a second shield (enclosure) and a last filter stage shielding; an AC_{out} filter referenced to (L-); the use of several small filters instead of a large one; the suppression of all the resonant poles at frequencies higher than 50 kHz; the use of ceramic capacitors to minimize the parasitic inductances and the size; the minimization of coupling between filters; the minimization of capacitive coupling in the inductor design.

Conclusions

GaN transistors operated in ZVS (Zero Voltage Switching) mode, combined with a specific parallel active filtering topology and with the use of MLC capacitors as storage components are the key factors that have contributed to reaching such a high power density. The shape of the heatsink, the geometric arrangement of the ceramic capacitors and the thermal interfaces optimization contribute to a low temperature while in full load operation. The optimized software running on a fast microcontroller associated with a dedicated logic circuit (CPLD) warrants the ZVS behavior for the entire operation range and reduces the electromagnetic noise. Double shielding and an optimized set of filters allow the inverter to meet EMC compliance requirements.

Biographical Appendix Document :

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Olivier BOMBOIR is VP of Product management and New Business within CE+T Power. He has over 25 years experiences in AC backup power supply equipments using modular DC to AC inverter, modular UPS and Static by pass switches.
He joined CE+T Power R&D lab design team in 1990 as a project engineer for electronic static by pass switch where he first introduce embedded processor into electronic power supply products. In 1995 he joined the sales support team to develop the global accounts as a Customer Sales Support for system design and implementation, customer training and servicing worldwide until 1997. Since joining the sales management team in 1997 he is coordinating the sales and marketing strategy for all CE+T group worldwide until 2013 where he took over the Product Management & New Business innovation team. He is member of the board of CE+T Power. Olivier holds a Master degree in electrical engineering from Liege University (Belgium) and was graduated in 1989.

Paul Bleus is R&D director at CE+T since 1997 with the mission to set up innovation in the field of power electronics conversion, supporting the deposit of more than 10 patents about efficiency improvement in energy converters on the last 15 years.
His experience started in Belgium as a researcher at the University of Liege, followed by a PE designer experience at Alstom for 2 years, a 9 years' project leader experience at ABB focusing on electronic control design, to finally work at CE+T Benelux, China & India for 18 years.
From 2008 to 2014, he was concurrently a power electronics teacher for 1st master of 5 years graduate engineers at the University of Liege.

François Milstein received his Physics Master degree in 2004 from the Faculty of Applied Sciences at the University of Liège in Belgium. His master thesis was focused on dielectric permittivity measurement at low temperature for superconductivity applications. He began to work in CE+T in 2004 as a R&D engineer and became responsible for inverters embedded software maintenance and development. François Milstein designed and implemented the control strategy of various electrical power convertors. He developed the software for the first generation of EPC mode CE+T inverter in 2006 and the first generation of CE+T modular three phase UPS in 2010. He also worked at Broadband Power Solutions SA where he was in charge of the embedded software of DC/DC converters used in Remote Line Powering. He contributed, in JEMA SA, to the development of a high precision current DC supply for proton therapy application. His realizations also include the software for a three phase Static By Pass and for a synchronization module for large modular inverters systems. Today, François Milstein works on the software development of the new CE+T ECI modular inverter and of the GOOGLE & IEEE Little Box Challenge.

Thierry Joannès received his Electromechanical Master degree in 1999 from the Faculty of Applied Sciences at the University of Liège in Belgium. His master thesis was focused on Control and Driving of PM Synchronous Motor. After two years as a research engineer at the University of Liège, he began to work at CE+T in 2001 as a research engineer and became rapidly development project manager in power supply conversion. Thierry Joannès is inventor of many mechanical assemblies and electrical converter topologies that help CE+T to keep his leadership in 48Vdc input inverter. He successfully led the first forced air cooled CE+T inverter in 2001, the first generation of EPC mode CE+T inverter in 2006 and the first generation of CE+T modular three phases UPS in 2010. Between 2005 and 2012, he also worked at Broadband Power Solutions S.A. where he mainly developed a rectifier and DC/DC converters. He recently developed the first CE+T modular three phase Static By Pass for AGIL UPS system. Today, Thierry Joannès is concentrated on the complete hardware conception of two exciting projects: the new CE+T ECI modular inverter and the GOOGLE & IEEE Little Box Challenge.

Pierre Stassain received his M.S. in Electrical engineering from the Faculty of Applied Sciences at the University of Liège in Belgium in 1993. He designed and realized a resonant forward DC/DC converter for his master thesis. He worked 4 years on patented sensor development for instrumented drill bits in collaboration with Security Diamond Board Stratabit. He joined the Research & Development Department of CE+T S.A. in 1998 as a project manager for new generation of static switches, DC/AC and remote line power conversion modules.
Pierre was also involved in patented power supply system and method development. He is co-inventor of 3 patents. His activities of interests mainly include design and control of static switch, small to medium power inverters, development of remote power feeding devices according to RFTC technology, safety requirements for IEC and UL60950 certifications, synchronization processes applied to inverter large systems.

Christophe Geuzaine received his PhD degree in 2001 from the Faculty of Applied Sciences at the University of Liège in Belgium. After post-doctoral positions at the California Institute of Technology and with the Belgian National Science Foundation, he became an assistant professor of Mathematics at Case Western Reserve University in 2005. In 2007 he came back to the University of Liège, where he is now a full professor in the department of Electrical Engineering and Computer Science. He is the founder and head of the Applied and Computational Electromagnetics group at the University of Liège, as well as the director of its electromagnetics compatibility laboratory.
Prof. Geuzaine's research encompasses modeling, analysis, algorithm development, and simulation for problems arising in various areas of engineering and science, with current applications in computational electromagnetics and biomedical problems. He has authored more than 100 papers in the fields of computational electromagnetics, applied mathematics and scientific computing. He is the co-creator of the popular open source mesh generator Gmsh and the multi-physics finite element solver GetDP.

Carl Emmerechts received his Master of Mechanical Engineering in 1989 at the Catholic University of Louvain in Belgium. He has been working for 25 years at Sirris, the Belgian Research Center of the technological Industry as a consultant and project leader in new product development. His skills are focused on mechanical design (CAD, thermal and structural FE modeling, CFD analysis) and manufacturing process (thermoplastic injection molding, Metal Injection molding, Magnesium thixomolding, thermoplastic composites,…)
He has been developing the activity of thermal management at Sirris since 2002 and is responsible for more than 10 years in thermal design of product and systems ("Thermal Management in Product Development" IWT project 2002-2004). He led successfully many analysis and advices in product design and thermal management for various companies in Flanders and Wallonia in the field of electronics, lighting, medical devices …

Fabrice Frebel received his M.S. and Ph.D. degrees in electronic engineering from the Faculty of Applied Sciences at the University of Liège in Belgium, in 1995 and 2003, respectively. His career began in Difra Instrumentation S.A. with the creation of a complete digital image processing system. In 1997, he joined CE+T S.A. in Liège. He was responsible for the development of fully digitally controlled inverters working in parallel and the creation of new power converters topologies.
In 2003, he joined the Euresys S.A. company specialized in machine vision software tools and frame grabbers where he started to work as Vice President of Engineering in 2007. He founded eFFiciency research in 2003 in order to provide Research & Innovation services for the design of electronic circuits when electromagnetic aspects matter. Since 2012, he has been working full time in eFFiciency research. He has been collaborating with the Applied and Computational Electromagnetics group at the University of Liège in order to develop a high frequency transformer and inductor simulation tool. He is inventor of six patents. His main activities of interest are power converter topologies, radio frequency communications, circuit and electromagnetic components simulations.

Philippe Laurent received his PhD degree from the Faculty of Applied Sciences at the University of Liege in Belgium. Then, he joined the Techspace Aero Company (SAFRAN Group), which is a low-pressure compressor expert, as a Materials and Process Engineer. Since 2010, he is working at the Microsys lab of the University of Liege, department of Electrical Engineering and Computer Science. The Microsys lab performs innovative research in microsystems Micro-assembly and Packaging, and Energy Harvesting.
Philippe Laurent's research encompasses mechanics, electricity and electronics, heat transfer and material science. His research activity is related to problems arising in various areas of engineering and science, with a strong interest for Power Management and Energy Harvesting dedicated for autonomous and wireless sensors.