Technical approach, updated oct 2015

Team name: Schneider Electric team	**Registration code:** 545-14tq1R-57137

Introduction and overall technical approach:

We have been successful in creating the working prototype of the “Little Box” meeting the project requirements. The prototype has been tested and validated and meets all the specifications put forward in Technical specification sheet. We federated a multi-disciplined team of electrical, mechanical, thermal and firmware engineers to solve the challenge. We applied the latest semiconductor (wide band-gap components) and magnetic technologies as well as new technologies and techniques to achieve unique high power density requirements. To meet input ripple current requirements we deployed a novel active filtering technique. The first result was a volume of 24.3 in^3 for the 2kW inverter. Based on our thermal margins and new components, we’ve been able to further shrink the volume (increase power density) by the time we present our final prototype to 20 in^3.

Specific actions undertaken to meet the high power density goal and other specifications are:

Novel topology for 120Hz ripple filtering,
Use of compact electrolytic capacitor,
Use of wide band-gap devices to achieve high efficiency and low volume,
Optimized thermal management.

120 Hz input current/voltage ripple requirement:

The input ripple voltage and current reduction technique and topology are our most important innovation and breakthrough. After having analyzed passive filtering and active filtering in patents and publications, we came up with a totally new active ripple filtering architecture.

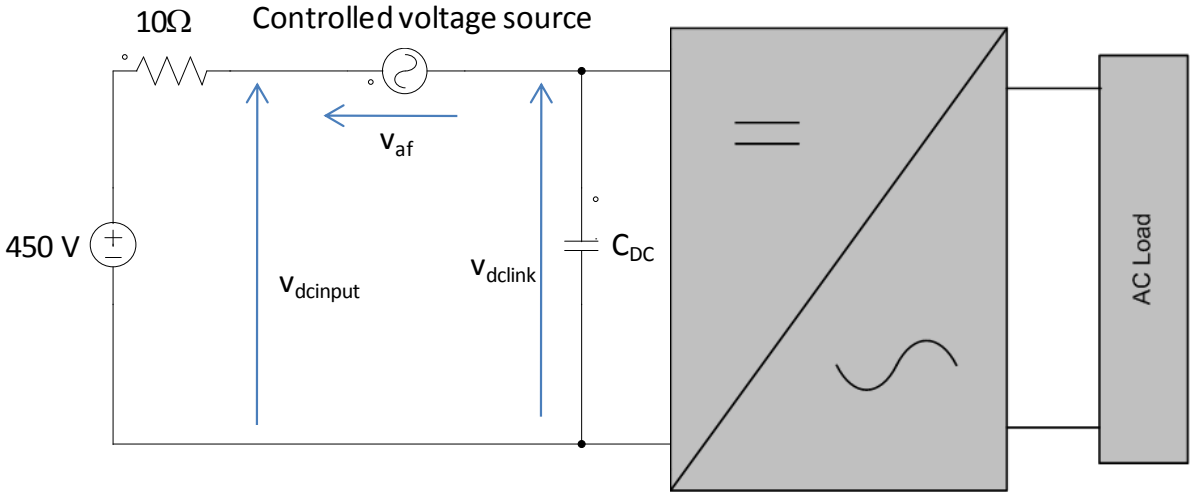
<u>120Hz ripple filtering architecture:</u>

Our active ripple filtering architecture [1] is composed of a capacitor (C_{DC}) and a controlled AC voltage source (v_{af}), as shown in Fig. 1.

To minimize the volume, we used low-value capacitor C_{DC} across the inverter DC link. The purpose of this capacitor is to carry the low frequency (120Hz) and high frequency current ripple generated by inverter switching. The voltage across the DC link is v_{dclink}= V_{dclink_av} +v_{ripple}, where V_{dclink_av} is the average value and v_{ripple} is the ripple content, mainly of 120Hz.

A controlled voltage source is connected between the DC input (after 10Ω resistor) and the inverter DC link. The voltage source is controlled in such a way that it generates a AC voltage across its output with the amplitude same as the amplitude of the ripple voltage in the DC link capacitor C_{DC}, and a phase shift of 180 degree with respect to the

DC link ripple voltage, i.e., $v_{af} = - v_{ripple}$. As a result, the ripple in the input voltage tends to be close to zero, so does the ripple in the input current.



$v_{dclink} = V_{dclink\_av} + v_{ripple}$

$v_{af} = - v_{ripple}$

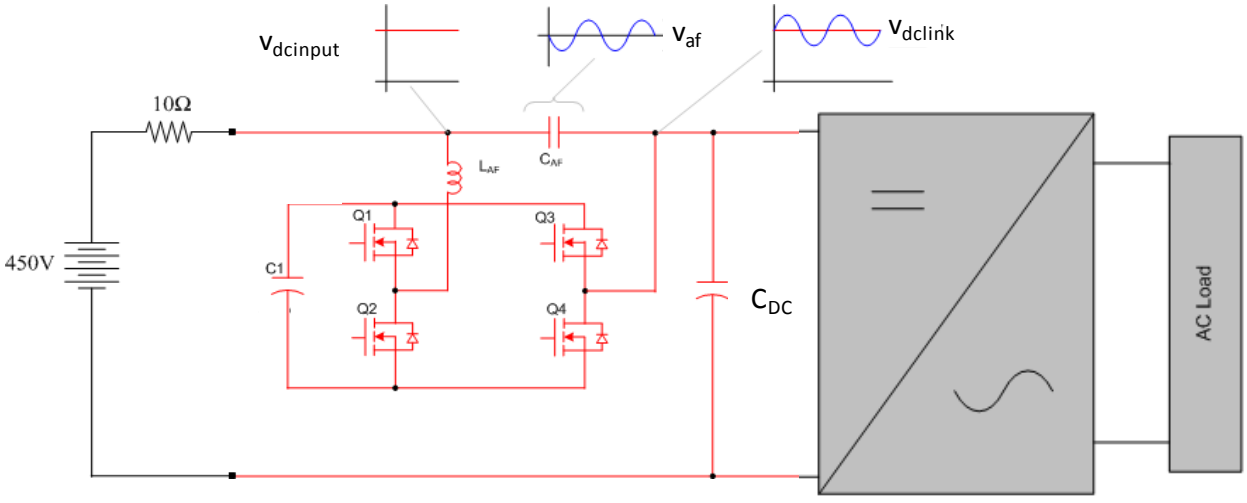
$v_{dcinput} = v_{dclink} + v_{af} = V_{dclink\_av} + v_{ripple} - v_{ripple} = V_{dclink\_av}$

Fig.1: Basic structure of 120Hz ripple filtering

<u>Implementation of the active ripple filtering:</u>

To optimize the size of the DC link capacitor (C_{DC}), we worked with several vendors and finally chose the latest electrolytic capacitor technology that offers the highest power density while handling safely both the low frequency (120Hz) ripple current and the high frequency ripple current generated by inverter switching.

A full-bridge low voltage inverter is used to implement the controlled voltage source. This inverter operates in high frequency PWM mode with a LC filter (L_{AF}, C_{AF}).



C_{DC} : DC link capacitor (*implemented: 400 µF, 450V*).

$Q_1 – Q_4$: Low voltage MOSFETs (*implemented: Vds=40V, Rds_on<3 mΩ)*

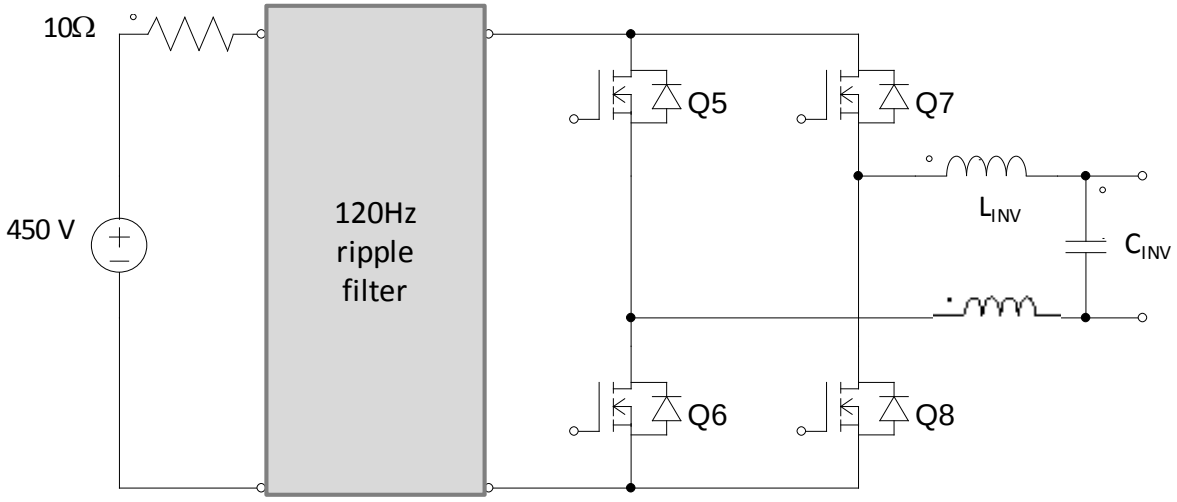
L_{AF} : few tens of µH. C_{AF}= few µF.
C1: active filter bus capacitor (*implemented: 3000 µF, 25V*).

Fig. 2: Active ripple filter topology

Low-voltage, low-Rds_on MOSFETs are used to achieve very low switching losses and low conduction losses, which allows to mount these devices directly on PCB without any heat sink. Due to low voltage and high-frequency operation, the size of the LC filter (L_{AF}, C_{AF}) is very small.
Overall, the active filter enables very low ripple voltage and in turn low ripple current at the DC input, much less than the levels specified by the requirements. Compared to known passive and active solutions, the volume allocated to DC ripple filtering is drastically reduced, while the losses are very low.
We also patented an alternate ripple filtering architecture[2] with similar performance.

Miniaturization of components for DC/AC

The selected inverter topology deploys full bridge operating at PWM mode. The inverter shown in fig. 3 consists of two half bridge legs and an LC output filter.
In order to minimize common mode voltage and meet ground current requirement while maximizing efficiency, the operation of the inverter bridge is such that both legs are at high frequency.



Q_5 – Q_8: SiC MOSFETs, switching at 45 kHz.
L_{INV}: hundred of µH, C_{INV}= few µF.

Fig. 3: Basic schematics of the DC/AC inverter

Wide band-gap semiconductors are selected in order to reach high efficiency. Different GaN and SiC components with various package forms such as QFN, TO220 and TO247 were tested and the final choice was to use SiC MOSFETs with TO247 package, which proved to be best in terms of component ruggedness, thermal management, gate driving and EM interference.

Thermal management:

To handle total losses in high power density design, we set our target for efficiency at 97%. With about 60W of power losses, forced-air cooling turned out to be the most effective way to reach high power density while keeping the enclosure surface below 60°C. Low internal temperature in turn also helps minimize conduction losses of magnetic components and power semiconductors. Fan mounting, heat sink design, and airflow have been studied extensively in order to effectively cool the power semiconductors and other parts with small size fan and heat sink. Fig. 4 gives a view of initial internal implementation, air flow management and simulated temperature profile. The measured temperature profile matches the simulation results.

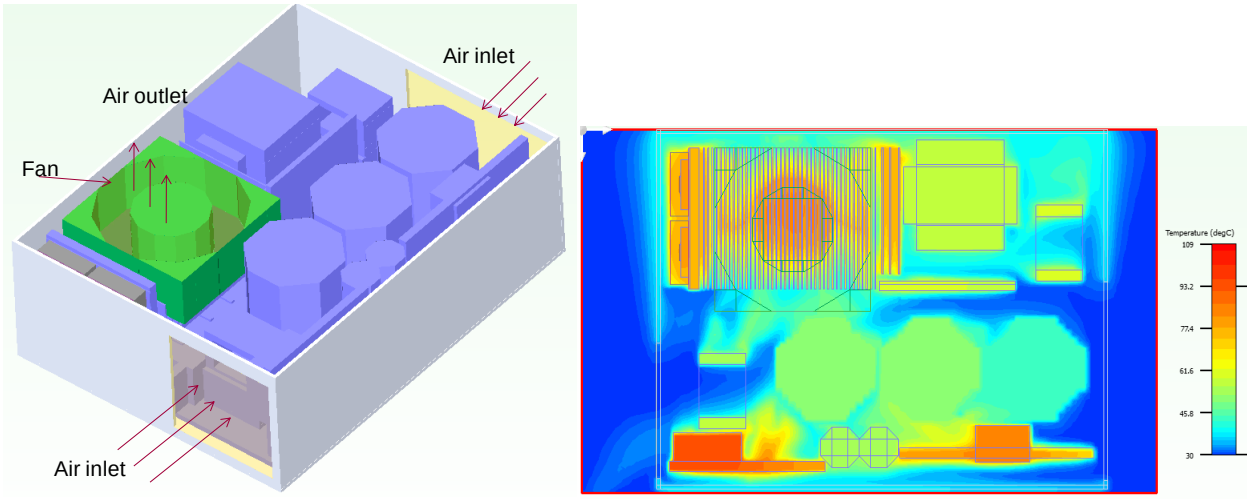


Fig. 4: (a) Cooling implementation (b) simulated temperature profile

Electromagnetic Compliance (EMC):

The following measures have been taken to keep EMC within the limits determined by governing CISPR and FCC standards:

- operate Inverter switches at quite low frequency (45kHz)
- separated DC input from AC output,
- implemented DC side and AC side EMI/RFI filter,
- minimized sheet metal openings and added shielding with ferrite sheets and Mu-metal sheets.

Patents applications:

[1] Series Active Ripple Filter. U.S. Patent Application serial number: 14/704591. Filing date : 5 May 2015

[2] Active filtering system. Filing number: FR 1552997. First Filing: 8 April 2015

Biographical information appendix:

Miao-xin Wang received the Engineer degree in automatics and power electronics from ENSEEIHT, Toulouse, France, in 1989, and the Ph.D. degree in electrical engineering from INPT, France, in 1992.
He joined Schneider Electric in 1993, before moving to UPS development and RD management within MGE UPS System from 2000 to 2007 and Eaton Electrical from 2007 to 2011. Since 2011, he has been leading Advanced Electronics and Power Electronics team within Schneider Electric, Corporate Technology Innovation Department, France. He is the author and coauthor of several papers and patents on harmonic filtering, low-harmonic converter topology, and UPS topology.

Rajesh Ghosh received the Ph. D degree in Electrical Engineering from The Indian Institute of Science Bangalore in 2007. He joined APC by Schneider Electric, Bangalore in 2007 as an Electrical Engineer. Currently he is a staff Electrical Engineer in the IT business of Schneider Electric. His interests include high-frequency power conversion and digital control.
Prior to joining APC he worked with CESC Ltd. Calcutta, India and GE Global Research center Bangalore, India. He has published many journal and conference papers in IEEE and holds many US patents.

Srikanth Mudiyula received the Master's degree in Electrical engineering with specialization in Power Electronics from NIT Trichy. He has joined Schneider Electric in 2012 as an Electrical Engineer. His interests include power electronics converters design and digital control. He has developed many digital control algorithm including droop method of paralleling several inverters, LLC resonant converter control and UPS control.

Dr. Radoslava Mitova received her diploma in Electrical Engineering from Technical University of Sofia in 2001. She received her Ph.D degree in Power electronics from the National Polytechnic Institute of Grenoble, France in 2005. She also worked for PRIMES lab (Tarbes) on high voltage multilevel power converter architectures with medium voltage transformer for railway traction. She joined Schneider Electric in 2007 as power electronic engineer. She works on SiC and GaN based power devices semiconductors application in industrial inverter.

David Reilly is a member of the technical staff and group expert for the APC division of Schneider Electric, and has over 35 years experience designing magnetics and power electronics. Dave has been awarded seven US patents related to power conversion: including patents that reduce the size and increase the efficiency of DC-DC converters currently used in Schneider UPS's; and a highly efficient quasi-sine DC-AC inverter

topology also used in Schneider UPS's. He has developed corporate CAD tools to aid in the design of power converters and magnetic devices. Dave attended Northeastern University, Boston, USA.

Milind Dighrasker has been working with Schneider Electric India from the year 2007. Currently, he is working in Schneider Electric, India Design Center as Sr. Engineering Manager. Previously, he worked with OSRAM India from 2004 to 2007 as Design engineer in the area of lighting electronics. He has got Master degree in Power & Control from Indian Institute of Technology Kanpur India in the year of 2004. His areas of interest are Power conversion techniques & Magnetic Design. He owns several patents in the area of power conversion and energy storage domain.

Sajeesh Sulaiman received his B-tech in Electrical and Electronics engineering from Cochin University of Science And Technology (CUSAT) in the 2008. In 2008 he joined Emerson Network Power, Mumbai as R&D engineer and was responsible for UPS development. Since 2010, he has been part of Schneider electric, handling product EMI/EMC and Safety certifications. In his current role, he is responsible for 'Design for EMC' of electronic hardware development. He is also an active member of IEEE Society of EMC Engineers India.

Alain Dentella has been with Schneider group since 1984. He is Electronic Designer, in protections relays for medium voltage from 1984 to 2010, and in electronics and power electronics innovation projects since 2010.

Damir Klikic received his Master's degree n Electrical Engineering from the University of Zagreb, Croatia in 1985. He has been with American Power Conversion from 1991 and with Schneider Electric from 2007 where he has been involved with power converters, UPS systems, control and modeling. In his current role he's leading applied research and study of emerging technologies , applications and markets . His current interests include research of static converter architectures, applications of new semiconductor and battery technologies. He is author and co-author of more than 10 patents and scientific papers.

Michael Hartmann received the B.S. (Hons.) and M.Sc. degrees (Hons.) in electrical engineering from the University of Technology Vienna, Vienna, Austria, in 2005 and 2006, respectively. In summer 2011, he received the Ph.D. degree from the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology, Zurich, Switzerland, where his research was focused on active three-phase PFC rectifier systems with ultrahigh switching frequencies and three-phase PFC rectifiers for aircraft applications.

He is currently with Schneider Electric, Drive Technology, and Systems in Vienna, where he is involved in the research on high efficiency three-phase converter systems for low and medium voltage drives. His research interests further include three-phase power conversion, electromagnetic interference and switched-mode power amplifiers using multicell topologies.
Dr. Hartmann received the IEEE PELS Prize Paper Award in 2012.

Additional members:
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