RW-WLAN HE TOP User Manual

User Manual
RW-WLAN-HE-TOP-HW-UM
Version 0.01
2018-12-31

RivieraWaves
http://www.rivierawaves.com/

Revision History

Version	Date	Revision Description	Author
0.01	2018-10-09	Initial release	JV

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1 Overview

1.1 Document Overview

The document describes the software and hardware interfaces of the RW-WLAN-HE TOP Reference Platform.

2 Hardware Implementation

2.1 Overview

The following figure represents the block diagram of the RW-WLAN-HE Top Level including the RISCV CPU subsystem.

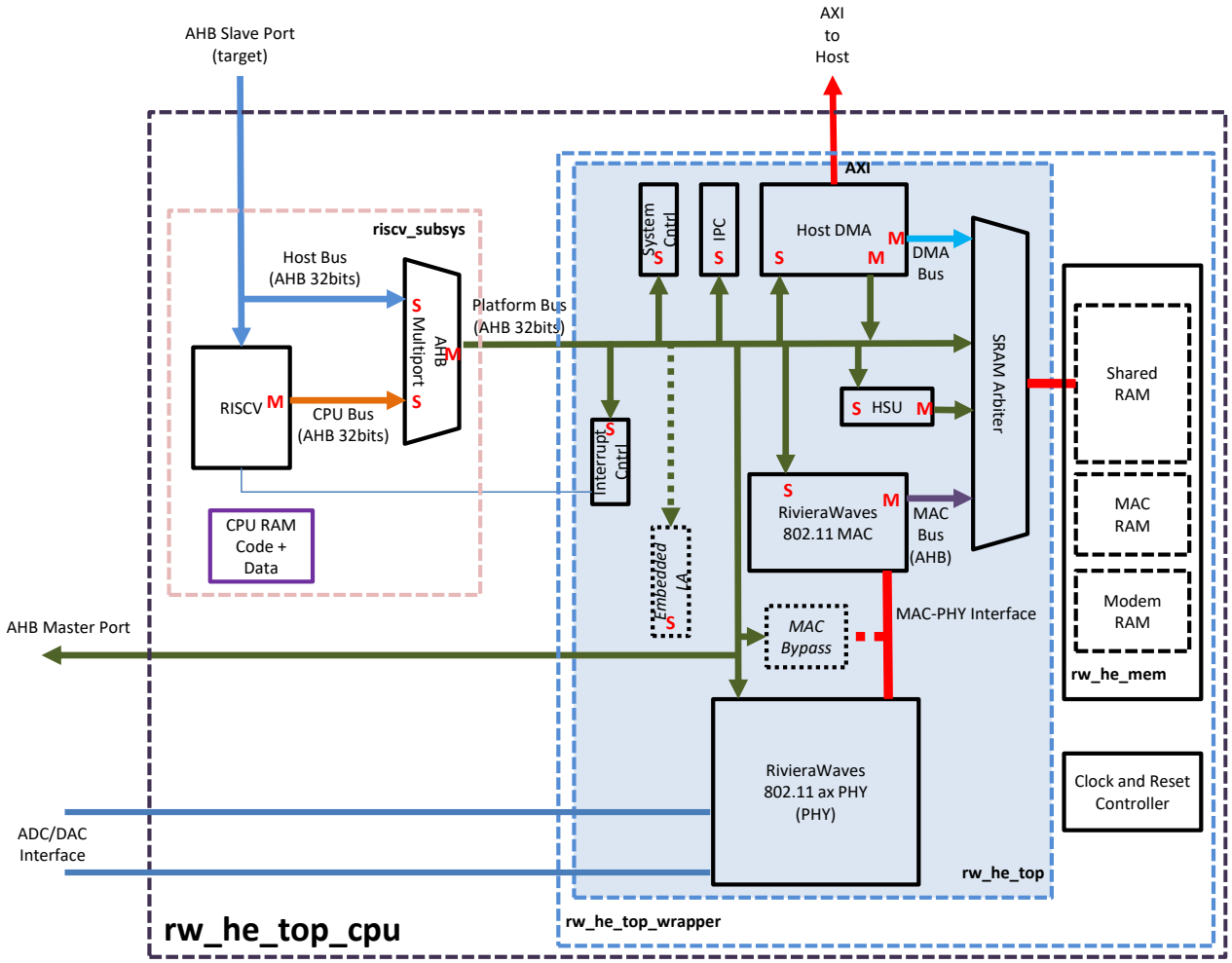

Figure 2-1 – RW-WLAN-nX FPGA V7 Platform block diagram

2.2 Block Description

2.2.1 rw_nx_top_cpu.

This is the top level of the complete RW WLAN HE IP including the RISCV CPU subsystem and the rw_nx_top_wrapper.

2.2.2 rw_nx_top_wrapper.

As the clock generation and the memory need to be implemented specifically to the targeted library, they are instantiated outside of the rw_nx_top. The purpose of rw_nx_top_wrapper is to integrate the RW 802.11ax IP, the clock/reset generation and the Memories instantiation together.

2.2.3 RISCV_subsys

2.2.3.1 Description

This block integrates the RISCV as well as the AHB Slave interface (coming from the host interface) and provides a single AHB master interface which is connected to the RW 802.11ax IP.

The AHB Salve interface goes to the RISCV Code and Data RAM port (which enables the download of the firmware from the Host) and it also goes to an AHB multiport arbiter to provide host access to the RW 802.11ax IP.

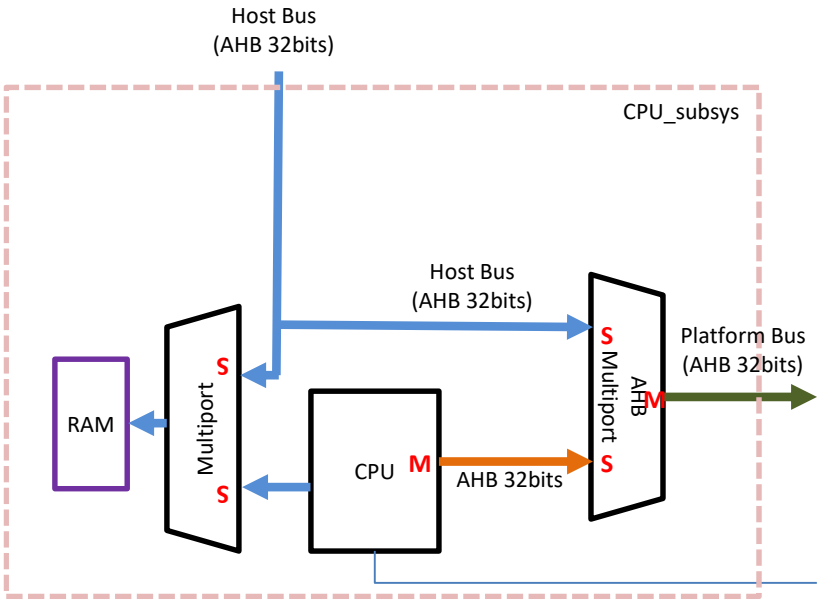

Figure 2-2 – riscv_subsys block diagram

3 Software interface

Some registers or fields in registers have been defined for debug purposes alone and will be read/set only through the alternate debug interface to the platform, not by SW.

3.1 Memory map

The table below shows the memory location of devices seen by the masters (TL4 processor and Host bridge) accessing to the peripheral bus.

Module	Address start	Address end
TL4 Data RAM	0x00000000	0x001FFFFF
TL4 Instruction RAM	0x00200000	0x002FFFFF
RW-WLAN NX IP	0x60000000	0x6FFFFFFF
FPGA Registers	0x60C10000	0x60C1FFFF
Frame Buffer Ch0	0x60C20000	0x60C2FFFF
Frame Buffer Ch1	0x60C30000	0x60C3FFFF

Table 3.1 - Memory map

Some registers or fields in registers have been defined for debug purposes alone and will be read/set only through the alternate debug interface to the platform, not by SW.

3.2 Memory map

The table below shows the memory location of devices seen by the masters (WLAN CPU and Host bridge) accessing to the peripheral bus.

Module	Address start	Address end
RISCV RAM	0x00000000	0x001FFFFF
RW-WLAN NX Ref Platform	0x60000000	0x6FFFFFFF
Shared RAM	0x60000000	0x607FFFFF
IPC	0x60800000	0x608FFFFF
System Controller	0x60900000	0x6090FFFF
Interrupt Controller	0x60910000	0x6091FFFF
Packet Traffic Arbiter (Optional)	0x60920000	0x6092FFFF
Hardware Security Unit	0x60930000	0x6093FFFF
Clock & Reset Manager	0x60940000	0x6094FFFF
Platform DMA	0x60A00000	0x60AFFFFF
MAC	0x60B00000	0x60BFFFFF
PHY	0x60C00000	0x60CFFFFF
Embedded LA Config (Optional)	*0x60E00000*	*0x60EFFFFF*
Embedded LA MEM (Optional)	*0x61100000*	*0x61FFFFFF*

Table 2 - Memory map for WLAN CPU and Host Bridge

The platform DMA can also access some of the AHB peripheral using the following memory map.

Module	Address start	Address end
Shared RAM (256KB)	0x00000000	0x007FFFFF
PHY	0x00C00000	0x00CFFFFF
Embedded LA MEM (Optional)	*0x01000000*	*0x01FFFFFF*

Table 3 - Memory map for Platform DMA

3.3 Interrupt map

The below shows the interrupt vector assignments to the corresponding interrupt sources.

Interrupt controller Vector number	Description
95-80	RESERVED
PHY HW	
79-72	RESERVED
71	Radio-Controller
70	Modem
Inter Processor Communication	
69-64	RESERVED
63-60	IPC 3-0
MAC Hardware	
59-56	RESERVED
55	Protocol Trigger
54	General
53	TX Trigger
52	RX Trigger
51	TX/RX Misc
50	TX/RX Timer
LA	
49	Embedded Logic Analyzer (if present)
HSU	
48	Hardware Security Unit
SYSCNTL	
47	Tick Timer Interrupt
DMA	
46-41	RESERVED
40	DMA Error detected
39-24	LLI 15-0 (Specific fragment of link list item has been processed)
23-20	Channel 3-0 EOT (Last fragment of the corresponding channel link list has been processed)
12-19	RESERVED
PHY	
11	Radio-Controller
10	Modem
0-9	RESERVED

Table 4 - Interrupt sources map

All sources are level sensitive and active high.

Interrupt vectors 0, 1, 2 and 3 are internal processor interrupts and are not controllable by the interrupt controller.

3.4 Inter-Processor Communication (IPC) registers

The following table summarizes the registers displayed by the IPC device. The host dedicated registers are only accessible by the host and can't be accessed by the embedded processor. In the same manner, the embedded dedicated registers are only accessible by the embedded processor and can't be accessed by the host.

3.4.1 Register Map

Address	Register Name
0x0	APP2EMB_TRIGGER
0x4	EMB2APP_RAWSTATUS
0x8	EMB2APP_ACK
0xC	EMB2APP_UNMASK_SET
0x10	EMB2APP_UNMASK_CLEAR
0x1C	EMB2APP_STATUS
0x40	APP_SIGNATURE
0x100	EMB2APP_TRIGGER
0x104	APP2EMB_RAWSTATUS
0x108	APP2EMB_ACK
0x10C	APP2EMB_UNMASK_SET
0x110	APP2EMB_UNMASK_CLEAR
0x114	APP2EMB_LINE_SEL_LOW
0x118	APP2EMB_LINE_SEL_HIGH
0x11C	APP2EMB_STATUS
0x140	EMB_SIGNATURE

Table 3.5 - Register Map

3.4.2 Register List

3.4.2.1 Register APP2EMB_TRIGGER

The IPC enables the host processor to assert up to thirty interrupt sources towards the reference platform processor.

Address	Access		APP2EMB_TRIGGER																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+0'H	RW	S	APP2EMB_TRIGGER[31]	APP2EMB_TRIGGER[30]	APP2EMB_TRIGGER[29]	APP2EMB_TRIGGER[28]	APP2EMB_TRIGGER[27]	APP2EMB_TRIGGER[26]	APP2EMB_TRIGGER[25]	APP2EMB_TRIGGER[24]	APP2EMB_TRIGGER[23]	APP2EMB_TRIGGER[22]	APP2EMB_TRIGGER[21]	APP2EMB_TRIGGER[20]	APP2EMB_TRIGGER[19]	APP2EMB_TRIGGER[18]	APP2EMB_TRIGGER[17]	APP2EMB_TRIGGER[16]	APP2EMB_TRIGGER[15]	APP2EMB_TRIGGER[14]	APP2EMB_TRIGGER[13]	APP2EMB_TRIGGER[12]	APP2EMB_TRIGGER[11]	APP2EMB_TRIGGER[10]	APP2EMB_TRIGGER[9]	APP2EMB_TRIGGER[8]	APP2EMB_TRIGGER[7]	APP2EMB_TRIGGER[6]	APP2EMB_TRIGGER[5]	APP2EMB_TRIGGER[4]	APP2EMB_TRIGGER[3]	APP2EMB_TRIGGER[2]	APP2EMB_TRIGGER[1]	APP2EMB_TRIGGER[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
SW Access			S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S

Table 3.6 - Register APP2EMB_TRIGGER

Name	Type	Size	Description

APP2EMB_TRIGGER[31:0]	U	32	Written bit to 1'b1 asserts the corresponding application to embedded IPC interrupt source.

Table 3.7 - Register APP2EMB_TRIGGER fields description

3.4.2.2 Register EMB2APP_RAWSTATUS

The register reports the active interrupt sources triggered by the reference platform processor. This register is not affected by the mask applied on the interrupt sources. The reference platform can assert up to eight interrupt sources towards the host processor.

Address	Access		EMB2APP_RAWSTATUS																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+4'H	W	R	EMB2APP_RAWSTATUS[31]	EMB2APP_RAWSTATUS[30]	EMB2APP_RAWSTATUS[29]	EMB2APP_RAWSTATUS[28]	EMB2APP_RAWSTATUS[27]	EMB2APP_RAWSTATUS[26]	EMB2APP_RAWSTATUS[25]	EMB2APP_RAWSTATUS[24]	EMB2APP_RAWSTATUS[23]	EMB2APP_RAWSTATUS[22]	EMB2APP_RAWSTATUS[21]	EMB2APP_RAWSTATUS[20]	EMB2APP_RAWSTATUS[19]	EMB2APP_RAWSTATUS[18]	EMB2APP_RAWSTATUS[17]	EMB2APP_RAWSTATUS[16]	EMB2APP_RAWSTATUS[15]	EMB2APP_RAWSTATUS[14]	EMB2APP_RAWSTATUS[13]	EMB2APP_RAWSTATUS[12]	EMB2APP_RAWSTATUS[11]	EMB2APP_RAWSTATUS[10]	EMB2APP_RAWSTATUS[9]	EMB2APP_RAWSTATUS[8]	EMB2APP_RAWSTATUS[7]	EMB2APP_RAWSTATUS[6]	EMB2APP_RAWSTATUS[5]	EMB2APP_RAWSTATUS[4]	EMB2APP_RAWSTATUS[3]	EMB2APP_RAWSTATUS[2]	EMB2APP_RAWSTATUS[1]	EMB2APP_RAWSTATUS[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
SW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 3.8 - Register EMB2APP_RAWSTATUS

Name	Type	Size	Description
EMB2APP_RAWSTATUS[31:0]	U	32	A bit set to 1'b1 indicates that the corresponding interrupt source is pending.

Table 3.9 - Register EMB2APP_RAWSTATUS fields description

3.4.2.3 Register EMB2APP_ACK

The register enables the host processor to acknowledge the interrupt sources asserted by the reference platform processor.

Address	Access		EMB2APP_ACK																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+8'H	R	C	EMB2APP_ACK[31]	EMB2APP_ACK[30]	EMB2APP_ACK[29]	EMB2APP_ACK[28]	EMB2APP_ACK[27]	EMB2APP_ACK[26]	EMB2APP_ACK[25]	EMB2APP_ACK[24]	EMB2APP_ACK[23]	EMB2APP_ACK[22]	EMB2APP_ACK[21]	EMB2APP_ACK[20]	EMB2APP_ACK[19]	EMB2APP_ACK[18]	EMB2APP_ACK[17]	EMB2APP_ACK[16]	EMB2APP_ACK[15]	EMB2APP_ACK[14]	EMB2APP_ACK[13]	EMB2APP_ACK[12]	EMB2APP_ACK[11]	EMB2APP_ACK[10]	EMB2APP_ACK[9]	EMB2APP_ACK[8]	EMB2APP_ACK[7]	EMB2APP_ACK[6]	EMB2APP_ACK[5]	EMB2APP_ACK[4]	EMB2APP_ACK[3]	EMB2APP_ACK[2]	EMB2APP_ACK[1]	EMB2APP_ACK[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
SW Access			C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C

Table 3.10 - Register EMB2APP_ACK

Name	Type	Size	Description

EMB2APP_ACK[31:0]	U	32	A written bit set to 1'b1 acknowledges the corresponding interrupt pending source.

Table 3.11 - Register EMB2APP_ACK fields description

3.4.2.4 Register EMB2APP_UNMASK_SET

The register enables the host processor to un-mask interrupt sources from the reference platform.

Address	Access		EMB2APP_UNMASK_SET																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+C'H	R	S	EMB2APP_UNMASK_SET[31]	EMB2APP_UNMASK_SET[30]	EMB2APP_UNMASK_SET[29]	EMB2APP_UNMASK_SET[28]	EMB2APP_UNMASK_SET[27]	EMB2APP_UNMASK_SET[26]	EMB2APP_UNMASK_SET[25]	EMB2APP_UNMASK_SET[24]	EMB2APP_UNMASK_SET[23]	EMB2APP_UNMASK_SET[22]	EMB2APP_UNMASK_SET[21]	EMB2APP_UNMASK_SET[20]	EMB2APP_UNMASK_SET[19]	EMB2APP_UNMASK_SET[18]	EMB2APP_UNMASK_SET[17]	EMB2APP_UNMASK_SET[16]	EMB2APP_UNMASK_SET[15]	EMB2APP_UNMASK_SET[14]	EMB2APP_UNMASK_SET[13]	EMB2APP_UNMASK_SET[12]	EMB2APP_UNMASK_SET[11]	EMB2APP_UNMASK_SET[10]	EMB2APP_UNMASK_SET[9]	EMB2APP_UNMASK_SET[8]	EMB2APP_UNMASK_SET[7]	EMB2APP_UNMASK_SET[6]	EMB2APP_UNMASK_SET[5]	EMB2APP_UNMASK_SET[4]	EMB2APP_UNMASK_SET[3]	EMB2APP_UNMASK_SET[2]	EMB2APP_UNMASK_SET[1]	EMB2APP_UNMASK_SET[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
SW Access			S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S

Table 3.12 - Register EMB2APP_UNMASK_SET

Name	Type	Size	Description
EMB2APP_UNMASK_SET[31:0]	U	32	A written bit set to 1'b1 un-masks the corresponding interrupt source.

Table 3.13 - Register EMB2APP_UNMASK_SET fields description

3.4.2.5 Register EMB2APP_UNMASK_CLEAR

The register enables the host processor to mask interrupt sources from the reference platform.

Address	Access		EMB2APP_UNMASK_CLEAR																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+10'H	RW	C	EMB2APP_UNMASK_CLEAR[31]	EMB2APP_UNMASK_CLEAR[30]	EMB2APP_UNMASK_CLEAR[29]	EMB2APP_UNMASK_CLEAR[28]	EMB2APP_UNMASK_CLEAR[27]	EMB2APP_UNMASK_CLEAR[26]	EMB2APP_UNMASK_CLEAR[25]	EMB2APP_UNMASK_CLEAR[24]	EMB2APP_UNMASK_CLEAR[23]	EMB2APP_UNMASK_CLEAR[22]	EMB2APP_UNMASK_CLEAR[21]	EMB2APP_UNMASK_CLEAR[20]	EMB2APP_UNMASK_CLEAR[19]	EMB2APP_UNMASK_CLEAR[18]	EMB2APP_UNMASK_CLEAR[17]	EMB2APP_UNMASK_CLEAR[16]	EMB2APP_UNMASK_CLEAR[15]	EMB2APP_UNMASK_CLEAR[14]	EMB2APP_UNMASK_CLEAR[13]	EMB2APP_UNMASK_CLEAR[12]	EMB2APP_UNMASK_CLEAR[11]	EMB2APP_UNMASK_CLEAR[10]	EMB2APP_UNMASK_CLEAR[9]	EMB2APP_UNMASK_CLEAR[8]	EMB2APP_UNMASK_CLEAR[7]	EMB2APP_UNMASK_CLEAR[6]	EMB2APP_UNMASK_CLEAR[5]	EMB2APP_UNMASK_CLEAR[4]	EMB2APP_UNMASK_CLEAR[3]	EMB2APP_UNMASK_CLEAR[2]	EMB2APP_UNMASK_CLEAR[1]	EMB2APP_UNMASK_CLEAR[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
SW Access			C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C

Table 3.14 - Register EMB2APP_UNMASK_CLEAR

Name	Type	Size	Description

EMB2APP_UNMASK_CLEAR[31:0]	U	32	A written bit set to 1'b1 masks the corresponding interrupt source.

Table 3.15 - Register EMB2APP_UNMASK_CLEAR fields description

3.4.2.6 Register EMB2APP_STATUS

The register reports the active and un-masked interrupt sources triggered by the reference platform processor. The reference platform can assert up to eight interrupt sources towards the host processor.

Address	Access		EMB2APP_STATUS																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+1C'H	W	R	EMB2APP_STATUS[31]	EMB2APP_STATUS[30]	EMB2APP_STATUS[29]	EMB2APP_STATUS[28]	EMB2APP_STATUS[27]	EMB2APP_STATUS[26]	EMB2APP_STATUS[25]	EMB2APP_STATUS[24]	EMB2APP_STATUS[23]	EMB2APP_STATUS[22]	EMB2APP_STATUS[21]	EMB2APP_STATUS[20]	EMB2APP_STATUS[19]	EMB2APP_STATUS[18]	EMB2APP_STATUS[17]	EMB2APP_STATUS[16]	EMB2APP_STATUS[15]	EMB2APP_STATUS[14]	EMB2APP_STATUS[13]	EMB2APP_STATUS[12]	EMB2APP_STATUS[11]	EMB2APP_STATUS[10]	EMB2APP_STATUS[9]	EMB2APP_STATUS[8]	EMB2APP_STATUS[7]	EMB2APP_STATUS[6]	EMB2APP_STATUS[5]	EMB2APP_STATUS[4]	EMB2APP_STATUS[3]	EMB2APP_STATUS[2]	EMB2APP_STATUS[1]	EMB2APP_STATUS[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
SW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 3.16 - Register EMB2APP_STATUS

Name	Type	Size	Description
EMB2APP_STATUS[31:0]	U	32	A bit set to 1'b1 indicates that the corresponding un-masked interrupt source is pending.

Table 3.17 - Register EMB2APP_STATUS fields description

3.4.2.7 Register APP_SIGNATURE

The register reports the IPC signature

Address	Access		APP_SIGNATURE																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+40'H	W	R	SIGNATURE[31]	SIGNATURE[30]	SIGNATURE[29]	SIGNATURE[28]	SIGNATURE[27]	SIGNATURE[26]	SIGNATURE[25]	SIGNATURE[24]	SIGNATURE[23]	SIGNATURE[22]	SIGNATURE[21]	SIGNATURE[20]	SIGNATURE[19]	SIGNATURE[18]	SIGNATURE[17]	SIGNATURE[16]	SIGNATURE[15]	SIGNATURE[14]	SIGNATURE[13]	SIGNATURE[12]	SIGNATURE[11]	SIGNATURE[10]	SIGNATURE[9]	SIGNATURE[8]	SIGNATURE[7]	SIGNATURE[6]	SIGNATURE[5]	SIGNATURE[4]	SIGNATURE[3]	SIGNATURE[2]	SIGNATURE[1]	SIGNATURE[0]
Reset Value			0	1	0	0	1	0	0	1	0	1	0	1	0	0	0	0	0	1	0	0	0	0	1	1	0	0	1	1	0	0	1	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
SW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 3.18 - Register APP_SIGNATURE

Name	Type	Size	Description
SIGNATURE[31:0]	U	32	Signature

Table 3.19 - Register APP_SIGNATURE fields description

3.4.2.8 Register EMB2APP_TRIGGER

The IPC enables the host processor to assert up to thirty interrupt sources towards the reference platform processor.

Address	Access		EMB2APP_TRIGGER																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+0'H	RW	S	EMB2APP_TRIGGER[31]	EMB2APP_TRIGGER[30]	EMB2APP_TRIGGER[29]	EMB2APP_TRIGGER[28]	EMB2APP_TRIGGER[27]	EMB2APP_TRIGGER[26]	EMB2APP_TRIGGER[25]	EMB2APP_TRIGGER[24]	EMB2APP_TRIGGER[23]	EMB2APP_TRIGGER[22]	EMB2APP_TRIGGER[21]	EMB2APP_TRIGGER[20]	EMB2APP_TRIGGER[19]	EMB2APP_TRIGGER[18]	EMB2APP_TRIGGER[17]	EMB2APP_TRIGGER[16]	EMB2APP_TRIGGER[15]	EMB2APP_TRIGGER[14]	EMB2APP_TRIGGER[13]	EMB2APP_TRIGGER[12]	EMB2APP_TRIGGER[11]	EMB2APP_TRIGGER[10]	EMB2APP_TRIGGER[9]	EMB2APP_TRIGGER[8]	EMB2APP_TRIGGER[7]	EMB2APP_TRIGGER[6]	EMB2APP_TRIGGER[5]	EMB2APP_TRIGGER[4]	EMB2APP_TRIGGER[3]	EMB2APP_TRIGGER[2]	EMB2APP_TRIGGER[1]	EMB2APP_TRIGGER[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
SW Access			S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S

Table 3.20 - Register EMB2APP_TRIGGER

Name	Type	Size	Description
EMB2APP_TRIGGER[31:0]	U	32	Written bit to 1'b1 asserts the corresponding embedded to application IPC interrupt source.

Table 3.21 - Register EMB2APP_TRIGGER fields description

3.4.2.9 Register APP2EMB_RAWSTATUS

The register reports what are the active interrupt sources triggered by the host processor. This register is not affected by the mask applied to interrupt sources. The host processor can assert up to 32 interrupt sources towards the reference platform processor.

Address	Access		APP2EMB_RAWSTATUS																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+4'H	W	R	APP2EMB_RAWSTATUS[31]	APP2EMB_RAWSTATUS[30]	APP2EMB_RAWSTATUS[29]	APP2EMB_RAWSTATUS[28]	APP2EMB_RAWSTATUS[27]	APP2EMB_RAWSTATUS[26]	APP2EMB_RAWSTATUS[25]	APP2EMB_RAWSTATUS[24]	APP2EMB_RAWSTATUS[23]	APP2EMB_RAWSTATUS[22]	APP2EMB_RAWSTATUS[21]	APP2EMB_RAWSTATUS[20]	APP2EMB_RAWSTATUS[19]	APP2EMB_RAWSTATUS[18]	APP2EMB_RAWSTATUS[17]	APP2EMB_RAWSTATUS[16]	APP2EMB_RAWSTATUS[15]	APP2EMB_RAWSTATUS[14]	APP2EMB_RAWSTATUS[13]	APP2EMB_RAWSTATUS[12]	APP2EMB_RAWSTATUS[11]	APP2EMB_RAWSTATUS[10]	APP2EMB_RAWSTATUS[9]	APP2EMB_RAWSTATUS[8]	APP2EMB_RAWSTATUS[7]	APP2EMB_RAWSTATUS[6]	APP2EMB_RAWSTATUS[5]	APP2EMB_RAWSTATUS[4]	APP2EMB_RAWSTATUS[3]	APP2EMB_RAWSTATUS[2]	APP2EMB_RAWSTATUS[1]	APP2EMB_RAWSTATUS[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
SW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 3.22 - Register APP2EMB_RAWSTATUS

Name	Type	Size	Description
APP2EMB_RAWSTATUS[31:0]	U	32	A bit set to 1'b1 indicates that the corresponding interrupt source is pending.

Table 3.23 - Register APP2EMB_RAWSTATUS fields description

3.4.2.10 Register APP2EMB_ACK

The register enables the reference platform processor to acknowledge the interrupt sources asserted by the host processor.

Address	Access		APP2EMB_ACK																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+8'H	RW	C	APP2EMB_ACK[31]	APP2EMB_ACK[30]	APP2EMB_ACK[29]	APP2EMB_ACK[28]	APP2EMB_ACK[27]	APP2EMB_ACK[26]	APP2EMB_ACK[25]	APP2EMB_ACK[24]	APP2EMB_ACK[23]	APP2EMB_ACK[22]	APP2EMB_ACK[21]	APP2EMB_ACK[20]	APP2EMB_ACK[19]	APP2EMB_ACK[18]	APP2EMB_ACK[17]	APP2EMB_ACK[16]	APP2EMB_ACK[15]	APP2EMB_ACK[14]	APP2EMB_ACK[13]	APP2EMB_ACK[12]	APP2EMB_ACK[11]	APP2EMB_ACK[10]	APP2EMB_ACK[9]	APP2EMB_ACK[8]	APP2EMB_ACK[7]	APP2EMB_ACK[6]	APP2EMB_ACK[5]	APP2EMB_ACK[4]	APP2EMB_ACK[3]	APP2EMB_ACK[2]	APP2EMB_ACK[1]	APP2EMB_ACK[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
SW Access			C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C

Table 3.24 - Register APP2EMB_ACK

Name	Type	Size	Description
APP2EMB_ACK[31:0]	U	32	A written bit set to 1'b1 acknowledges the corresponding interrupt pending source.

Table 3.25 - Register APP2EMB_ACK fields description

3.4.2.11 Register APP2EMB_UNMASK_SET

The register enables the reference platform processor to un-mask interrupt sources from the host processor.

Address	Access		APP2EMB_UNMASK_SET																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+C'H	RW	S	APP2EMB_UNMASK_SET[31]	APP2EMB_UNMASK_SET[30]	APP2EMB_UNMASK_SET[29]	APP2EMB_UNMASK_SET[28]	APP2EMB_UNMASK_SET[27]	APP2EMB_UNMASK_SET[26]	APP2EMB_UNMASK_SET[25]	APP2EMB_UNMASK_SET[24]	APP2EMB_UNMASK_SET[23]	APP2EMB_UNMASK_SET[22]	APP2EMB_UNMASK_SET[21]	APP2EMB_UNMASK_SET[20]	APP2EMB_UNMASK_SET[19]	APP2EMB_UNMASK_SET[18]	APP2EMB_UNMASK_SET[17]	APP2EMB_UNMASK_SET[16]	APP2EMB_UNMASK_SET[15]	APP2EMB_UNMASK_SET[14]	APP2EMB_UNMASK_SET[13]	APP2EMB_UNMASK_SET[12]	APP2EMB_UNMASK_SET[11]	APP2EMB_UNMASK_SET[10]	APP2EMB_UNMASK_SET[9]	APP2EMB_UNMASK_SET[8]	APP2EMB_UNMASK_SET[7]	APP2EMB_UNMASK_SET[6]	APP2EMB_UNMASK_SET[5]	APP2EMB_UNMASK_SET[4]	APP2EMB_UNMASK_SET[3]	APP2EMB_UNMASK_SET[2]	APP2EMB_UNMASK_SET[1]	APP2EMB_UNMASK_SET[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
SW Access			S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S

Table 3.26 - Register APP2EMB_UNMASK_SET

Name	Type	Size	Description
APP2EMB_UNMASK_SET[31:0]	U	32	A written bit set to 1'b1 un-masks the corresponding interrupt source.

Table 3.27 - Register APP2EMB_UNMASK_SET fields description

3.4.2.12 Register APP2EMB_UNMASK_CLEAR

The register enables the host processor to mask interrupt sources from the reference platform.

Address	Access		APP2EMB_UNMASK_CLEAR																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+10'H	RW	C	APP2EMB_UNMASK_CLEAR[31]	APP2EMB_UNMASK_CLEAR[30]	APP2EMB_UNMASK_CLEAR[29]	APP2EMB_UNMASK_CLEAR[28]	APP2EMB_UNMASK_CLEAR[27]	APP2EMB_UNMASK_CLEAR[26]	APP2EMB_UNMASK_CLEAR[25]	APP2EMB_UNMASK_CLEAR[24]	APP2EMB_UNMASK_CLEAR[23]	APP2EMB_UNMASK_CLEAR[22]	APP2EMB_UNMASK_CLEAR[21]	APP2EMB_UNMASK_CLEAR[20]	APP2EMB_UNMASK_CLEAR[19]	APP2EMB_UNMASK_CLEAR[18]	APP2EMB_UNMASK_CLEAR[17]	APP2EMB_UNMASK_CLEAR[16]	APP2EMB_UNMASK_CLEAR[15]	APP2EMB_UNMASK_CLEAR[14]	APP2EMB_UNMASK_CLEAR[13]	APP2EMB_UNMASK_CLEAR[12]	APP2EMB_UNMASK_CLEAR[11]	APP2EMB_UNMASK_CLEAR[10]	APP2EMB_UNMASK_CLEAR[9]	APP2EMB_UNMASK_CLEAR[8]	APP2EMB_UNMASK_CLEAR[7]	APP2EMB_UNMASK_CLEAR[6]	APP2EMB_UNMASK_CLEAR[5]	APP2EMB_UNMASK_CLEAR[4]	APP2EMB_UNMASK_CLEAR[3]	APP2EMB_UNMASK_CLEAR[2]	APP2EMB_UNMASK_CLEAR[1]	APP2EMB_UNMASK_CLEAR[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
SW Access			C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C

Table 3.28 - Register APP2EMB_UNMASK_CLEAR

Name	Type	Size	Description
APP2EMB_UNMASK_CLEAR[31:0]	U	32	A written bit set to 1'b1 masks the corresponding interrupt source.

Table 3.29 - Register APP2EMB_UNMASK_CLEAR fields description

3.4.2.13 Register APP2EMB_LINE_SEL_LOW

The register enables the reference platform processor to assign the lower sixteen interrupt sources to the four IPC interrupt lines ipc_irq[3:0].

Address	Access		APP2EMB_LINE_SEL_LOW																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+14'H	R	RW	APP2EMB15_SEL[1]	APP2EMB15_SEL[0]	APP2EMB14_SEL[1]	APP2EMB14_SEL[0]	APP2EMB13_SEL[1]	APP2EMB13_SEL[0]	APP2EMB12_SEL[1]	APP2EMB12_SEL[0]	APP2EMB11_SEL[1]	APP2EMB11_SEL[0]	APP2EMB10_SEL[1]	APP2EMB10_SEL[0]	APP2EMB9_SEL[1]	APP2EMB9_SEL[0]	APP2EMB8_SEL[1]	APP2EMB8_SEL[0]	APP2EMB7_SEL[1]	APP2EMB7_SEL[0]	APP2EMB6_SEL[1]	APP2EMB6_SEL[0]	APP2EMB5_SEL[1]	APP2EMB5_SEL[0]	APP2EMB4_SEL[1]	APP2EMB4_SEL[0]	APP2EMB3_SEL[1]	APP2EMB3_SEL[0]	APP2EMB2_SEL[1]	APP2EMB2_SEL[0]	APP2EMB1_SEL[1]	APP2EMB1_SEL[0]	APP2EMB0_SEL[1]	APP2EMB0_SEL[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
SW Access			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 3.30 - Register APP2EMB_LINE_SEL_LOW

Name	Type	Size	Description
APP2EMB15_SEL[1:0]	U	2	app2emb source #15 is assigned to ipc_irq[app2emb_15_sel].
APP2EMB14_SEL[1:0]	U	2	app2emb source #14 is assigned to ipc_irq[app2emb_14_sel].
APP2EMB13_SEL[1:0]	U	2	app2emb source #13 is assigned to ipc_irq[app2emb_13_sel].
APP2EMB12_SEL[1:0]	U	2	app2emb source #12 is assigned to ipc_irq[app2emb_12_sel].

APP2EMB11_SEL[1:0]	U	2	app2emb source #11 is assigned to ipc_irq[app2emb_11_sel].
APP2EMB10_SEL[1:0]	U	2	app2emb source #10 is assigned to ipc_irq[app2emb_10_sel].
APP2EMB9_SEL[1:0]	U	2	app2emb source #9 is assigned to ipc_irq[app2emb_9_sel].
APP2EMB8_SEL[1:0]	U	2	app2emb source #8 is assigned to ipc_irq[app2emb_8_sel].
APP2EMB7_SEL[1:0]	U	2	app2emb source #7 is assigned to ipc_irq[app2emb_7_sel].
APP2EMB6_SEL[1:0]	U	2	app2emb source #6 is assigned to ipc_irq[app2emb_6_sel].
APP2EMB5_SEL[1:0]	U	2	app2emb source #5 is assigned to ipc_irq[app2emb_5_sel].
APP2EMB4_SEL[1:0]	U	2	app2emb source #4 is assigned to ipc_irq[app2emb_4_sel].
APP2EMB3_SEL[1:0]	U	2	app2emb source #3 is assigned to ipc_irq[app2emb_3_sel].
APP2EMB2_SEL[1:0]	U	2	app2emb source #2 is assigned to ipc_irq[app2emb_2_sel].
APP2EMB1_SEL[1:0]	U	2	app2emb source #1 is assigned to ipc_irq[app2emb_1_sel].
APP2EMB0_SEL[1:0]	U	2	app2emb source #0 is assigned to ipc_irq[app2emb_0_sel].

Table 3.31 - Register APP2EMB_LINE_SEL_LOW fields description

3.4.2.14 Register APP2EMB_LINE_SEL_HIGH

The register enables the reference platform processor to assign the upper sixteen interrupt sources to the four IPC interrupt lines ipc_irq[3:0].

Address	Access		APP2EMB_LINE_SEL_HIGH																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+18'H	R	RW	APP2EMB31_SEL[1]	APP2EMB31_SEL[0]	APP2EMB30_SEL[1]	APP2EMB30_SEL[0]	APP2EMB29_SEL[1]	APP2EMB29_SEL[0]	APP2EMB28_SEL[1]	APP2EMB28_SEL[0]	APP2EMB27_SEL[1]	APP2EMB27_SEL[0]	APP2EMB26_SEL[1]	APP2EMB26_SEL[0]	APP2EMB25_SEL[1]	APP2EMB25_SEL[0]	APP2EMB24_SEL[1]	APP2EMB24_SEL[0]	APP2EMB23_SEL[1]	APP2EMB23_SEL[0]	APP2EMB22_SEL[1]	APP2EMB22_SEL[0]	APP2EMB21_SEL[1]	APP2EMB21_SEL[0]	APP2EMB20_SEL[1]	APP2EMB20_SEL[0]	APP2EMB19_SEL[1]	APP2EMB19_SEL[0]	APP2EMB18_SEL[1]	APP2EMB18_SEL[0]	APP2EMB17_SEL[1]	APP2EMB17_SEL[0]	APP2EMB16_SEL[1]	APP2EMB16_SEL[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
SW Access			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 3.32 - Register APP2EMB_LINE_SEL_HIGH

Name	Type	Size	Description
APP2EMB31_SEL[1:0]	U	2	app2emb source #31 is assigned to ipc_irq[app2emb_31_sel].
APP2EMB30_SEL[1:0]	U	2	app2emb source #30 is assigned to ipc_irq[app2emb_30_sel].
APP2EMB29_SEL[1:0]	U	2	app2emb source #29 is assigned to ipc_irq[app2emb_29_sel].
APP2EMB28_SEL[1:0]	U	2	app2emb source #28 is assigned to ipc_irq[app2emb_28_sel].
APP2EMB27_SEL[1:0]	U	2	app2emb source #27 is assigned to ipc_irq[app2emb_27_sel].
APP2EMB26_SEL[1:0]	U	2	app2emb source #26 is assigned to ipc_irq[app2emb_26_sel].
APP2EMB25_SEL[1:0]	U	2	app2emb source #25 is assigned to ipc_irq[app2emb_25_sel].
APP2EMB24_SEL[1:0]	U	2	app2emb source #24 is assigned to ipc_irq[app2emb_24_sel].
APP2EMB23_SEL[1:0]	U	2	app2emb source #23 is assigned to ipc_irq[app2emb_23_sel].
APP2EMB22_SEL[1:0]	U	2	app2emb source #22 is assigned to ipc_irq[app2emb_22_sel].
APP2EMB21_SEL[1:0]	U	2	app2emb source #21 is assigned to ipc_irq[app2emb_21_sel].
APP2EMB20_SEL[1:0]	U	2	app2emb source #20 is assigned to ipc_irq[app2emb_20_sel].
APP2EMB19_SEL[1:0]	U	2	app2emb source #19 is assigned to ipc_irq[app2emb_19_sel].
APP2EMB18_SEL[1:0]	U	2	app2emb source #18 is assigned to ipc_irq[app2emb_18_sel].
APP2EMB17_SEL[1:0]	U	2	app2emb source #17 is assigned to ipc_irq[app2emb_17_sel].
APP2EMB16_SEL[1:0]	U	2	app2emb source #16 is assigned to ipc_irq[app2emb_16_sel].

Table 3.33 - Register APP2EMB_LINE_SEL_HIGH fields description

3.4.2.15 Register APP2EMB_STATUS

The register reports what are the active and un-masked interrupt sources triggered by the host processor. The host processor can assert up to 31 interrupt sources towards the reference platform processor.

Address	Access		APP2EMB_STATUS																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+1C'H	W	R	APP2EMB_STATUS[31]	APP2EMB_STATUS[30]	APP2EMB_STATUS[29]	APP2EMB_STATUS[28]	APP2EMB_STATUS[27]	APP2EMB_STATUS[26]	APP2EMB_STATUS[25]	APP2EMB_STATUS[24]	APP2EMB_STATUS[23]	APP2EMB_STATUS[22]	APP2EMB_STATUS[21]	APP2EMB_STATUS[20]	APP2EMB_STATUS[19]	APP2EMB_STATUS[18]	APP2EMB_STATUS[17]	APP2EMB_STATUS[16]	APP2EMB_STATUS[15]	APP2EMB_STATUS[14]	APP2EMB_STATUS[13]	APP2EMB_STATUS[12]	APP2EMB_STATUS[11]	APP2EMB_STATUS[10]	APP2EMB_STATUS[9]	APP2EMB_STATUS[8]	APP2EMB_STATUS[7]	APP2EMB_STATUS[6]	APP2EMB_STATUS[5]	APP2EMB_STATUS[4]	APP2EMB_STATUS[3]	APP2EMB_STATUS[2]	APP2EMB_STATUS[1]	APP2EMB_STATUS[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
SW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 3.34 - Register APP2EMB_STATUS

Name	Type	Size	Description
APP2EMB_STATUS[31:0]	U	32	A bit set to 1'b1 indicates that the corresponding interrupt source is pending.

Table 3.35 - Register APP2EMB_STATUS fields description

3.4.2.16 Register EMB_SIGNATURE

The register reports the IPC signature

Address	Access		EMB_SIGNATURE																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+40'H	W	R	SIGNATURE[31]	SIGNATURE[30]	SIGNATURE[29]	SIGNATURE[28]	SIGNATURE[27]	SIGNATURE[26]	SIGNATURE[25]	SIGNATURE[24]	SIGNATURE[23]	SIGNATURE[22]	SIGNATURE[21]	SIGNATURE[20]	SIGNATURE[19]	SIGNATURE[18]	SIGNATURE[17]	SIGNATURE[16]	SIGNATURE[15]	SIGNATURE[14]	SIGNATURE[13]	SIGNATURE[12]	SIGNATURE[11]	SIGNATURE[10]	SIGNATURE[9]	SIGNATURE[8]	SIGNATURE[7]	SIGNATURE[6]	SIGNATURE[5]	SIGNATURE[4]	SIGNATURE[3]	SIGNATURE[2]	SIGNATURE[1]	SIGNATURE[0]
Reset Value			0	1	0	0	1	0	0	1	0	1	0	1	0	0	0	0	0	1	0	0	0	0	1	1	0	0	1	1	0	0	1	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
SW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 3.36 - Register EMB_SIGNATURE

Name	Type	Size	Description
SIGNATURE[31:0]	U	32	Signature

Table 3.37 - Register EMB_SIGNATURE fields description

3.5 System Controller registers

3.5.1 Register Map

Address	Register Name

0x0	SIGNATURE
0x4	DATE
0x8	TIME
0xC	SVNREV_MAC
0x10	SVNREV_FPGAA
0x40	TIMER
0x44	TICK_TIMER_CNT
0x48	TICK_TIMER_DURATION
0x4C	TICK_TIMER_IRQ_SET
0x50	TICK_TIMER_IRQ_CLEAR
0x54	TICK_TIMER_IRQ_CONTROL
0x68	DIAG_CONF
0x6C	DIAG_STAT
0x70	DIAG_TRIGGER
0x74	PHYDIAG_CONF
0x78	RIUDIAG_CONF
0x80	GPIO_OEN
0x84	GPIO_OUT
0x88	GPIO_IN
0xE0	MISC_CNTL

Table 3.38 - Register Map

3.5.2 Register List

3.5.2.1 Register SIGNATURE

This register contains the signature

Address	Access		SIGNATURE																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+0'H	W	R	fpga_signature[31]	fpga_signature[30]	fpga_signature[29]	fpga_signature[28]	fpga_signature[27]	fpga_signature[26]	fpga_signature[25]	fpga_signature[24]	fpga_signature[23]	fpga_signature[22]	fpga_signature[21]	fpga_signature[20]	fpga_signature[19]	fpga_signature[18]	fpga_signature[17]	fpga_signature[16]	fpga_signature[15]	fpga_signature[14]	fpga_signature[13]	fpga_signature[12]	fpga_signature[11]	fpga_signature[10]	fpga_signature[9]	fpga_signature[8]	fpga_signature[7]	fpga_signature[6]	fpga_signature[5]	fpga_signature[4]	fpga_signature[3]	fpga_signature[2]	fpga_signature[1]	fpga_signature[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
SW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 3.39 - Register SIGNATURE

Name	Type	Size	Description
fpga_signature[31:0]	U	32	Return the FPGA signature

Table 3.40 - Register SIGNATURE fields description

3.5.2.2 Register DATE

This register contains the creation date

Address	Access		DATE																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

+4'H	W	R	fpga_date[31]	fpga_date[30]	fpga_date[29]	fpga_date[28]	fpga_date[27]	fpga_date[26]	fpga_date[25]	fpga_date[24]	fpga_date[23]	fpga_date[22]	fpga_date[21]	fpga_date[20]	fpga_date[19]	fpga_date[18]	fpga_date[17]	fpga_date[16]	fpga_date[15]	fpga_date[14]	fpga_date[13]	fpga_date[12]	fpga_date[11]	fpga_date[10]	fpga_date[9]	fpga_date[8]	fpga_date[7]	fpga_date[6]	fpga_date[5]	fpga_date[4]	fpga_date[3]	fpga_date[2]	fpga_date[1]	fpga_date[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
SW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 3.41 - Register DATE

Name	Type	Size	Description
fpga_date[31:0]	U	32	Return the creation date

Table 3.42 - Register DATE fields description

3.5.2.3 Register TIME

This register contains the creation time

Address	Access		TIME																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+8'H	W	R	fpga_time[31]	fpga_time[30]	fpga_time[29]	fpga_time[28]	fpga_time[27]	fpga_time[26]	fpga_time[25]	fpga_time[24]	fpga_time[23]	fpga_time[22]	fpga_time[21]	fpga_time[20]	fpga_time[19]	fpga_time[18]	fpga_time[17]	fpga_time[16]	fpga_time[15]	fpga_time[14]	fpga_time[13]	fpga_time[12]	fpga_time[11]	fpga_time[10]	fpga_time[9]	fpga_time[8]	fpga_time[7]	fpga_time[6]	fpga_time[5]	fpga_time[4]	fpga_time[3]	fpga_time[2]	fpga_time[1]	fpga_time[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
SW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 3.43 - Register TIME

Name	Type	Size	Description
fpga_time[31:0]	U	32	Return the creation date

Table 3.44 - Register TIME fields description

3.5.2.4 Register SVNREV_MAC

This register contains the MAC SVN revision

Address	Access		SVNREV_MAC																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+C'H	W	R	svnrev_mac[31]	svnrev_mac[30]	svnrev_mac[29]	svnrev_mac[28]	svnrev_mac[27]	svnrev_mac[26]	svnrev_mac[25]	svnrev_mac[24]	svnrev_mac[23]	svnrev_mac[22]	svnrev_mac[21]	svnrev_mac[20]	svnrev_mac[19]	svnrev_mac[18]	svnrev_mac[17]	svnrev_mac[16]	svnrev_mac[15]	svnrev_mac[14]	svnrev_mac[13]	svnrev_mac[12]	svnrev_mac[11]	svnrev_mac[10]	svnrev_mac[9]	svnrev_mac[8]	svnrev_mac[7]	svnrev_mac[6]	svnrev_mac[5]	svnrev_mac[4]	svnrev_mac[3]	svnrev_mac[2]	svnrev_mac[1]	svnrev_mac[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

HW Access	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
SW Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 3.45 - Register SVNREV_MAC

Name	Type	Size	Description
svnrev_mac[31:0]	U	32	Return the MAC SVN Revision

Table 3.46 - Register SVNREV_MAC fields description

3.5.2.5 Register SVNREV_FPGAA

This register contains the FPGAA SVN revision

Address	Access		SVNREV_FPGAA																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+10'H	W	R	svnrev_fpgaa[31]	svnrev_fpgaa[30]	svnrev_fpgaa[29]	svnrev_fpgaa[28]	svnrev_fpgaa[27]	svnrev_fpgaa[26]	svnrev_fpgaa[25]	svnrev_fpgaa[24]	svnrev_fpgaa[23]	svnrev_fpgaa[22]	svnrev_fpgaa[21]	svnrev_fpgaa[20]	svnrev_fpgaa[19]	svnrev_fpgaa[18]	svnrev_fpgaa[17]	svnrev_fpgaa[16]	svnrev_fpgaa[15]	svnrev_fpgaa[14]	svnrev_fpgaa[13]	svnrev_fpgaa[12]	svnrev_fpgaa[11]	svnrev_fpgaa[10]	svnrev_fpgaa[9]	svnrev_fpgaa[8]	svnrev_fpgaa[7]	svnrev_fpgaa[6]	svnrev_fpgaa[5]	svnrev_fpgaa[4]	svnrev_fpgaa[3]	svnrev_fpgaa[2]	svnrev_fpgaa[1]	svnrev_fpgaa[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
SW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 3.47 - Register SVNREV_FPGAA

Name	Type	Size	Description
svnrev_fpgaa[31:0]	U	32	Return the FPGAA SVN Revision

Table 3.48 - Register SVNREV_FPGAA fields description

3.5.2.6 Register TIMER

This register is a free running timer based on Platform Clock

Address	Access		TIMER																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+40'H	R	RW	timer_value[31]	timer_value[30]	timer_value[29]	timer_value[28]	timer_value[27]	timer_value[26]	timer_value[25]	timer_value[24]	timer_value[23]	timer_value[22]	timer_value[21]	timer_value[20]	timer_value[19]	timer_value[18]	timer_value[17]	timer_value[16]	timer_value[15]	timer_value[14]	timer_value[13]	timer_value[12]	timer_value[11]	timer_value[10]	timer_value[9]	timer_value[8]	timer_value[7]	timer_value[6]	timer_value[5]	timer_value[4]	timer_value[3]	timer_value[2]	timer_value[1]	timer_value[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
SW Access			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 3.49 - Register TIMER

Name	Type	Size	Description
timer_value[31:0]	U	32	Return the current value of the free running timer

Table 3.50 - Register TIMER fields description

3.5.2.7 Register TICK_TIMER_CNT

This register is a tick timer based on Platform Clock

Address	Access		TICK_TIMER_CNT																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+44'H	R	RW	tick_timer_cnt[31]	tick_timer_cnt[30]	tick_timer_cnt[29]	tick_timer_cnt[28]	tick_timer_cnt[27]	tick_timer_cnt[26]	tick_timer_cnt[25]	tick_timer_cnt[24]	tick_timer_cnt[23]	tick_timer_cnt[22]	tick_timer_cnt[21]	tick_timer_cnt[20]	tick_timer_cnt[19]	tick_timer_cnt[18]	tick_timer_cnt[17]	tick_timer_cnt[16]	tick_timer_cnt[15]	tick_timer_cnt[14]	tick_timer_cnt[13]	tick_timer_cnt[12]	tick_timer_cnt[11]	tick_timer_cnt[10]	tick_timer_cnt[9]	tick_timer_cnt[8]	tick_timer_cnt[7]	tick_timer_cnt[6]	tick_timer_cnt[5]	tick_timer_cnt[4]	tick_timer_cnt[3]	tick_timer_cnt[2]	tick_timer_cnt[1]	tick_timer_cnt[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
SW Access			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 3.51 - Register TICK_TIMER_CNT

Name	Type	Size	Description
tick_timer_cnt[31:0]	U	32	Return the current value of the tick timer

Table 3.52 - Register TICK_TIMER_CNT fields description

3.5.2.8 Register TICK_TIMER_DURATION

This register programs the tick period

Address	Access		TICK_TIMER_DURATION																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+48'H	R	RW	tick_timer_duration[31]	tick_timer_duration[30]	tick_timer_duration[29]	tick_timer_duration[28]	tick_timer_duration[27]	tick_timer_duration[26]	tick_timer_duration[25]	tick_timer_duration[24]	tick_timer_duration[23]	tick_timer_duration[22]	tick_timer_duration[21]	tick_timer_duration[20]	tick_timer_duration[19]	tick_timer_duration[18]	tick_timer_duration[17]	tick_timer_duration[16]	tick_timer_duration[15]	tick_timer_duration[14]	tick_timer_duration[13]	tick_timer_duration[12]	tick_timer_duration[11]	tick_timer_duration[10]	tick_timer_duration[9]	tick_timer_duration[8]	tick_timer_duration[7]	tick_timer_duration[6]	tick_timer_duration[5]	tick_timer_duration[4]	tick_timer_duration[3]	tick_timer_duration[2]	tick_timer_duration[1]	tick_timer_duration[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
SW Access			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 3.53 - Register TICK_TIMER_DURATION

Name	Type	Size	Description
tick_timer_duration[31:0]	U	32	Period of tick interrupt

Table 3.54 - Register TICK_TIMER_DURATION fields description

3.5.2.9 Register TICK_TIMER_IRQ_SET

This register returns the status of tick interrupt and allow the software generation of the tick_timer interrupt

Address	Access		TICK_TIMER_IRQ_SET																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+4C'H	R	S																																tick_timer_irq_set
Reset Value																																		0
Type																																		U
HW Access																																		R
SW Access																																		S

Table 3.55 - Register TICK_TIMER_IRQ_SET

Name	Type	Size	Description
tick_timer_irq_set	U	1	Writing 1 in this field set the tick timer interrupt, Reading in this field returns the tick timer interrupt status

Table 3.56 - Register TICK_TIMER_IRQ_SET fields description

3.5.2.10 Register TICK_TIMER_IRQ_CLEAR

This register clears the tick timer interrupt

Address	Access		TICK_TIMER_IRQ_CLEAR																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+50'H	R	C																																tick_timer_irq_clear
Reset Value																																		0
Type																																		U
HW Access																																		R
SW Access																																		C

Table 3.57 - Register TICK_TIMER_IRQ_CLEAR

Name	Type	Size	Description

tick_timer_irq_clear	U	1	Writing 1 in this field clear the tick timer interrupt

Table 3.58 - Register TICK_TIMER_IRQ_CLEAR fields description

3.5.2.11 Register TICK_TIMER_IRQ_CONTROL

This register clear the tick timer interrupt

Address	Access		TICK_TIMER_IRQ_CONTROL																											
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+54'H	R	RW																															tick_timer_en	tick_timer_irq_en
Reset Value																																	0	0
Type																																	U	U
HW Access																																	R	R
SW Access																																	RW	RW

Table 3.59 - Register TICK_TIMER_IRQ_CONTROL

Name	Type	Size	Description
tick_timer_en	U	1	Enable the tick timer
tick_timer_irq_en	U	1	Enable the tick timer interrupt generation

Table 3.60 - Register TICK_TIMER_IRQ_CONTROL fields description

3.5.2.12 Register DIAG_CONF

This register controls the diagnostic port selection

Address	Access		DIAG_CONF																											
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+68'H	R	RW	diag_sel_en											diag_sel2[4]	diag_sel2[3]	diag_sel2[2]	diag_sel2[1]	diag_sel2[0]	diag_mux			diag_sel1[4]	diag_sel1[3]	diag_sel1[2]	diag_sel1[1]	diag_sel1[0]				diag_sel0[4]	diag_sel0[3]	diag_sel0[2]	diag_sel0[1]	diag_sel0[0]
Reset Value			0											1	0	0	0	0	0			0	1	1	0	0				1	0	0	1	0
Type			U											U	U	U	U	U	U			U	U	U	U	U				U	U	U	U	U
HW Access			R											R	R	R	R	R	R			R	R	R	R	R				R	R	R	R	R
SW Access			RW											RW	RW	RW	RW	RW	RW			RW	RW	RW	RW	RW				RW	RW	RW	RW	RW

Table 3.61 - Register DIAG_CONF

Name	Type	Size	Description
diag_sel_en	U	1	Enable the diag port selection
diag_sel2[4:0]	U	5	Select the diagnostic bank routed to diag Port2
diag_mux	U	1	Mux fpgaB diag and diag_mac_sw

diag_sel1[4:0]	U	5	Select the diagnostic bank routed to diag Port1
diag_sel0[4:0]	U	5	Select the diagnostic bank routed to diag Port0

Table 3.62 - Register DIAG_CONF fields description

3.5.2.13 Register DIAG_STAT

This register controls the diagnostic port selection

Address	Access		DIAG_STAT																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+6C'H	W	R	diag_value[31]	diag_value[30]	diag_value[29]	diag_value[28]	diag_value[27]	diag_value[26]	diag_value[25]	diag_value[24]	diag_value[23]	diag_value[22]	diag_value[21]	diag_value[20]	diag_value[19]	diag_value[18]	diag_value[17]	diag_value[16]	diag_value[15]	diag_value[14]	diag_value[13]	diag_value[12]	diag_value[11]	diag_value[10]	diag_value[9]	diag_value[8]	diag_value[7]	diag_value[6]	diag_value[5]	diag_value[4]	diag_value[3]	diag_value[2]	diag_value[1]	diag_value[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
SW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 3.63 - Register DIAG_STAT

Name	Type	Size	Description
diag_value[31:0]	U	32	Return the current value of diag port 1

Table 3.64 - Register DIAG_STAT fields description

3.5.2.14 Register DIAG_TRIGGER

This register generates a Diag trigger for logic analyser

Address	Access		DIAG_TRIGGER																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+70'H	R	RW																																diag_trigger
Reset Value																																		0
Type																																		U
HW Access																																		R
SW Access																																		RW

Table 3.65 - Register DIAG_TRIGGER

Name	Type	Size	Description
diag_trigger	U	1	Writing 1 trigs the embedded LA

Table 3.66 - Register DIAG_TRIGGER fields description

3.5.2.15 Register PHYDIAG_CONF

This register generates a Diag trigger for logic analyser

Address	Access		PHYDIAG_CONF																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+74'H	R	RW	phydiag_conf_msb1[7]	phydiag_conf_msb1[6]	phydiag_conf_msb1[5]	phydiag_conf_msb1[4]	phydiag_conf_msb1[3]	phydiag_conf_msb1[2]	phydiag_conf_msb1[1]	phydiag_conf_msb1[0]	phydiag_conf_lsb1[7]	phydiag_conf_lsb1[6]	phydiag_conf_lsb1[5]	phydiag_conf_lsb1[4]	phydiag_conf_lsb1[3]	phydiag_conf_lsb1[2]	phydiag_conf_lsb1[1]	phydiag_conf_lsb1[0]	phydiag_conf_msb0[7]	phydiag_conf_msb0[6]	phydiag_conf_msb0[5]	phydiag_conf_msb0[4]	phydiag_conf_msb0[3]	phydiag_conf_msb0[2]	phydiag_conf_msb0[1]	phydiag_conf_msb0[0]	phydiag_conf_lsb0[7]	phydiag_conf_lsb0[6]	phydiag_conf_lsb0[5]	phydiag_conf_lsb0[4]	phydiag_conf_lsb0[3]	phydiag_conf_lsb0[2]	phydiag_conf_lsb0[1]	phydiag_conf_lsb0[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
SW Access			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 3.67 - Register PHYDIAG_CONF

Name	Type	Size	Description
phydiag_conf_msb1[7:0]	U	8	Configure the PHYDIAG MSB1
phydiag_conf_lsb1[7:0]	U	8	Configure the PHYDIAG LSB1
phydiag_conf_msb0[7:0]	U	8	Configure the PHYDIAG MSB0
phydiag_conf_lsb0[7:0]	U	8	Configure the PHYDIAG LSB0

Table 3.68 - Register PHYDIAG_CONF fields description

3.5.2.16 Register RIUDIAG_CONF

This register generates a Diag trigger for logic analyser

Address	Access		RIUDIAG_CONF																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+78'H	R	RW	riudiag_conf_msb1[7]	riudiag_conf_msb1[6]	riudiag_conf_msb1[5]	riudiag_conf_msb1[4]	riudiag_conf_msb1[3]	riudiag_conf_msb1[2]	riudiag_conf_msb1[1]	riudiag_conf_msb1[0]	riudiag_conf_lsb1[7]	riudiag_conf_lsb1[6]	riudiag_conf_lsb1[5]	riudiag_conf_lsb1[4]	riudiag_conf_lsb1[3]	riudiag_conf_lsb1[2]	riudiag_conf_lsb1[1]	riudiag_conf_lsb1[0]	riudiag_conf_msb0[7]	riudiag_conf_msb0[6]	riudiag_conf_msb0[5]	riudiag_conf_msb0[4]	riudiag_conf_msb0[3]	riudiag_conf_msb0[2]	riudiag_conf_msb0[1]	riudiag_conf_msb0[0]	riudiag_conf_lsb0[7]	riudiag_conf_lsb0[6]	riudiag_conf_lsb0[5]	riudiag_conf_lsb0[4]	riudiag_conf_lsb0[3]	riudiag_conf_lsb0[2]	riudiag_conf_lsb0[1]	riudiag_conf_lsb0[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
SW Access			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 3.69 - Register RIUDIAG_CONF

Name	Type	Size	Description
riudiag_conf_msb1[7:0]	U	8	Configure the RIUDIAG MSB1
riudiag_conf_lsb1[7:0]	U	8	Configure the RIUDIAG LSB1
riudiag_conf_msb0[7:0]	U	8	Configure the RIUDIAG MSB0
riudiag_conf_lsb0[7:0]	U	8	Configure the RIUDIAG LSB0

Table 3.70 - Register RIUDIAG_CONF fields description

3.5.2.17 Register GPIO_OEN

This register control the direction of GPIO pins

Address	Access		GPIO_OEN																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+80'H	R	RW	gpio_oen[31]	gpio_oen[30]	gpio_oen[29]	gpio_oen[28]	gpio_oen[27]	gpio_oen[26]	gpio_oen[25]	gpio_oen[24]	gpio_oen[23]	gpio_oen[22]	gpio_oen[21]	gpio_oen[20]	gpio_oen[19]	gpio_oen[18]	gpio_oen[17]	gpio_oen[16]	gpio_oen[15]	gpio_oen[14]	gpio_oen[13]	gpio_oen[12]	gpio_oen[11]	gpio_oen[10]	gpio_oen[9]	gpio_oen[8]	gpio_oen[7]	gpio_oen[6]	gpio_oen[5]	gpio_oen[4]	gpio_oen[3]	gpio_oen[2]	gpio_oen[1]	gpio_oen[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
SW Access			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 3.71 - Register GPIO_OEN

Name	Type	Size	Description
gpio_oen[31:0]	U	32	Control the GPIO out enable

Table 3.72 - Register GPIO_OEN fields description

3.5.2.18 Register GPIO_OUT

This register control the GPIO output value

Address	Access		GPIO_OUT																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+84'H	R	RW	gpio_out[31]	gpio_out[30]	gpio_out[29]	gpio_out[28]	gpio_out[27]	gpio_out[26]	gpio_out[25]	gpio_out[24]	gpio_out[23]	gpio_out[22]	gpio_out[21]	gpio_out[20]	gpio_out[19]	gpio_out[18]	gpio_out[17]	gpio_out[16]	gpio_out[15]	gpio_out[14]	gpio_out[13]	gpio_out[12]	gpio_out[11]	gpio_out[10]	gpio_out[9]	gpio_out[8]	gpio_out[7]	gpio_out[6]	gpio_out[5]	gpio_out[4]	gpio_out[3]	gpio_out[2]	gpio_out[1]	gpio_out[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
SW Access			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 3.73 - Register GPIO_OUT

Name	Type	Size	Description
gpio_out[31:0]	U	32	Control the GPIO out value

Table 3.74 - Register GPIO_OUT fields description

3.5.2.19 Register GPIO_IN

This register returns the GPIO In value

Address	Access	GPIO_IN

	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+88'H	W	R	gpio_in[31]	gpio_in[30]	gpio_in[29]	gpio_in[28]	gpio_in[27]	gpio_in[26]	gpio_in[25]	gpio_in[24]	gpio_in[23]	gpio_in[22]	gpio_in[21]	gpio_in[20]	gpio_in[19]	gpio_in[18]	gpio_in[17]	gpio_in[16]	gpio_in[15]	gpio_in[14]	gpio_in[13]	gpio_in[12]	gpio_in[11]	gpio_in[10]	gpio_in[9]	gpio_in[8]	gpio_in[7]	gpio_in[6]	gpio_in[5]	gpio_in[4]	gpio_in[3]	gpio_in[2]	gpio_in[1]	gpio_in[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
SW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 3.75 - Register GPIO_IN

Name	Type	Size	Description
gpio_in[31:0]	U	32	Return the GPIO Input value

Table 3.76 - Register GPIO_IN fields description

3.5.2.20 Register MISC_CNTL

This register controls the clock and reset

Address	Access		MISC_CNTL																															
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+E0'H	R	RW	nmb_io_busy											sec_mac_pi_tx_clk_gating_en	sec_mac_crypt_clk_gating_en	sec_mac_core_tx_clk_gating_en	sec_mpif_clk_gating_en	mac_pi_clk_gating_en	mac_pi_tx_clk_gating_en	mac_pi_rx_clk_gating_en	mac_core_clk_gating_en	mac_crypt_clk_gating_en	mac_core_tx_clk_gating_en	mac_core_rx_clk_gating_en	mac_wt_clk_gating_en	mpif_clk_gating_en				bootrom_enable			fpgab_reset_req	soft_reset_req
Reset Value			0											0	0	0	0	0	0	0	0	0	0	0	0	0				0			0	0
Type			U											U	U	U	U	U	U	U	U	U	U	U	U	U				U			U	U
HW Access			W											R	R	R	R	R	R	R	R	R	R	R	R	R				R			R	R
SW Access			R											RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW				RW			RW	RW

Table 3.77 - Register MISC_CNTL

Name	Type	Size	Description
nmb_io_busy	U	1	Indicate the NMB_IO state
sec_mac_pi_tx_clk_gating_en	U	1	Enable the clock gating on Secondary MAC PI Tx Clock
sec_mac_crypt_clk_gating_en	U	1	Enable the clock gating on Secondary MAC Crypt Clock
sec_mac_core_tx_clk_gating_en	U	1	Enable the clock gating on Secondary MAC Core Tx Clock
sec_mpif_clk_gating_en	U	1	Enable the clock gating on Secondary MPIF Clock
mac_pi_clk_gating_en	U	1	Enable the clock gating on MAC PI Clock
mac_pi_tx_clk_gating_en	U	1	Enable the clock gating on MAC PI TX Clock
mac_pi_rx_clk_gating_en	U	1	Enable the clock gating on MAC PI RX Clock
mac_core_clk_gating_en	U	1	Enable the clock gating on MAC Core Clock
mac_crypt_clk_gating_en	U	1	Enable the clock gating on MAC Crypt Clock

mac_core_tx_clk_gating_en	U	1	Enable the clock gating on MAC Core Tx Clock
mac_core_rx_clk_gating_en	U	1	Enable the clock gating on MAC Core Rx Clock
mac_wt_clk_gating_en	U	1	Enable the clock gating on MAC WT Clock
mpif_clk_gating_en	U	1	Enable the clock gating on MPIF Clock
bootrom_enable	U	1	Boot the CPU
fpgab_reset_req	U	1	Request FPGA reset
soft_reset_req	U	1	Request a Software reset

Table 3.78 - Register MISC_CNTL fields description

The following table summarizes the registers displayed by the system controller device.

Address	Name
0x00	signature
0x04	build date
0x08	build time
0x40	current_cycle
0x44	tick_timer_cnt
0x48	tick_timer_duration
0x4C	tick_timer_irq_set
0x50	tick_timer_irq_clear
0x54	tick_timer_irq_control
0x68	diagport_conf
0x70	diagport_trigger
0x74	phydiag_conf
0x78	riudiag_cong
0x80	gpio_output_enable
0x84	gpio_output
0x88	gpio_input
0xe0	control0

Table 79 - System controller register summary

3.5.2.21 Signature register

This register indicates the signature of the system.

Field Name	rw	Bit	Reset	Description
signature	ro	31-0	32'h0	Signature of the system.

Table 80 – Signature register

3.5.2.22 Build Date register

This register indicates the date of the system build. The format is 0xYYYYMMDD

Field Name	rw	Bit	Reset	Description
Build Date	ro	31-0	32'h0	Date of the system build.

Table 81 – Build Date register

3.5.2.23 Build Time register

This register indicates the time of the system build. The format is 0x00HHMMSS

Field Name	rw	Bit	Reset	Description
Build Time	ro	31-0	32'h0	Time of the system build.

Table 82 – Build Time register

3.5.2.24 Current cycle register

This register implements a free running 32 bits counter. It is incremented every platform clock period and wraps to zero. It can be written at anytime by the software.

Field Name	rw	Bit	Reset	Description
current_cycle	rwu	31-0	32'h0	counter value

Table 83 - current_cycle register

3.5.2.25 Tick Timer registers

The system controller implements a programmable tick timer allowing the generation of tick interrupts required by RTOS. This timer is a 32bits counter. It is loaded with TICK_TIMER_DURATION and is decremented every platform clock period. When it reaches zero, the tick interrupt is generated (when enabled) and it restarts from TICK_TIMER_DURATION.

Field Name	rw	Bit	Reset	Description
tick_timer_cnt	rwu	31-0	32'h0	Return the current value of the tick timer

Table 84 – tick_timer_cnt register

Field Name	rw	Bit	Reset	Description
tick_timer_duration	rw	31-0	32'h0	Period of tick interrupt

Table 85 – tick_timer_duration register

Field Name	rw	Bit	Reset	Description
tick_timer_irq_set	rw	0	1'h0	Writing 1 in this field set the tick timer interrupt, Reading in this field returns the tick timer interrupt status

Table 86 – tick_timer_irq_set register

Field Name	rw	Bit	Reset	Description
tick_timer_irq_clear	w	0	1'h0	Writing 1 in this field set the tick timer interrupt,

Table 87 – tick_timer_irq_clear register

Field Name	rw	Bit	Reset	Description
tick_timer_irq_en	rw	0	1'h0	Enable the tick timer interrupt generation
tick_timer_en	rw	1	1'h0	Enable the tick timer

Table 88 – tick_timer_irq_control register

3.5.2.26 Diagnostic configuration register

This register configures the diagnostic port. On the DiniV6 prototype, this register routes the selected banks towards the mictor connector present on the sodimma connector. On the CevaV7 prototype, this register routes the selected banks 0, 1 and 2 towards the embedded Logic Analyzer, and the selected banks 1 and 2 towards the J10 and J9 mictor connectors.

Field Name	rw	Bit	Reset	Description

diag_sel_en	rw	31	1'b0	DiniV6 prototype only: Software controlled diagnostic port. When this bit is set, the diagnostic bank defined by the field *diag_sel0* is routed towards the mictor connector. If this bit is clear, the diagnostic bank defined by the position of the SODIMM A dip switches #2 range[4:0] is routed towards the mictor connector.
diag_sel2	rw	21:16	16'b0	CevaV7 prototype only: Select diagnostic bank 2, routed towards the embedded LA upper 32bits and the mictor connector J9
diag_mux	rw	15	16'b0	Diniv6 prototype only: select the diagnostic port connected to the embedded LA lower 32 bits. 0: select MAC SW diagnostic port 1: select PHY diagnostic port
diag_sel1	rw	12:8	16'b0	CevaV7 prototype only: Select diagnostic bank 1, routed towards the embedded LA middle 32bits and the mictor connector J10
diag_sel0	rw	4:0	16'b0	Select diagnostic bank 0. On the CevaV7 prototype, this bank is routed towards the embedded LA lower 32 bits. On the DiniV6 prototype, it is used as defined by diag_sel_en.

Table 89 - diagport_conf register

3.5.2.27 Diagnostic trigger register

This register enables the software to generate an event observable from the diag ports.

Field Name	rw	Bit	Reset	Description
diag_trigger	rw	0	1'b0	Diagnostic trigger level

Table 90 - diag_trigger register

3.5.2.28 GPIO Output enable register

This register controls the tri-state drivers of the GPIO ports.

Field Name	rw	Bit	Reset	Description
gpio_oen	rw	31-0	32'b0	0=input 1=output

Table 91 - gpio_oen register

3.5.2.29 GPIO Output register

This register controls the state of the GPIO output ports.

Field Name	rw	Bit	Reset	Description
gpio_out	rw	31-0	32'b0	In read access, the register displays the state of the GPIO Output ports. In write access, the register defines the value to be driven if the corresponding ports are configured as outputs.

Table 92 - gpio_out register

3.5.2.30 GPIO Input register

This register controls the state of the GPIO input ports.

Field Name	Rw	Bit	Reset	Description
gpio_in	r	31-0	32'b0	In read access, the register displays the state of the GPIO Input ports.

Table 93 - gpio_in register

3.5.2.31 Clock and reset control register

This register controls the clocks, resets and miscellaneous features.

Field Name	rw	Bit	Reset	Description
reg_mac_pi_clk_gating_en	rw	16	1'b0	When set enable the clock gating on mac_pi_clk clock
reg_mac_pi_tx_clk_gating_en	rw	15	1'b0	When set enable the clock gating on mac_pi_tx_clk clock
reg_mac_pi_rx_clk_gating_en	rw	14	1'b0	When set enable the clock gating on mac_pi_rx_clk clock
reg_mac_core_clk_gating_en	rw	13	1'b0	When set enable the clock gating on mac_core_clk clock
reg_mac_crypt_clk_gating_en	rw	12	1'b0	When set enable the clock gating on mac_crypt_clk clock
reg_mac_core_tx_clk_gating_en	rw	11	1'b0	When set enable the clock gating on mac_core_tx_clk clock
reg_mac_core_rx_clk_gating_en	rw	10	1'b0	When set enable the clock gating on mac_core_rx_clk clock
reg_mac_wt_clk_gating_en	rw	9	1'b0	When set enable the clock gating on mac_wt_clk clock
reg_mpif_clk_gating_en	rw	8	1'b0	When set enable the clock gating on mpif_clk clock
bootrom_en	rw	4	1'b0	This bit defines the content of the address 32'hFFFF0000 seen by the processor. When set to 0: The bootrom displays the opcode 0x000000f2: bra.s 0xFFFF000. This features makes the processor to continuously loop in boot rom while the processor instruction memory is not yet initialized by the host. When set to 1: The bootrom displays the opcode 0x00000071: trap #0. Once the firmware load in the instruction ram by the host, the host releases the processor for normal operations.
fpga_b_reset_req	rw	1	1'b1	This bit enables the software to reset the FPGA B. This bit shall be written back to 0 in order to de-assert the FPGA B reset.
fpga_a_reset_req	rwu	0	1'b0	This bit enables the software to reset the FPGA A and B. This bit is automatically cleared once the reset sequence performed by the hardware.

Table 94 - clk_rst_misc register

3.6 Interrupt Controller registers

3.6.1 Register Map

Address	Register Name
0x0	IRQ_STATUS0
0x4	IRQ_STATUS1
0x8	IRQ_RAW_STATUS0
0xC	IRQ_RAW_STATUS1
0x10	IRQ_UNMASK_SET0
0x14	IRQ_UNMASK_SET1
0x18	IRQ_UNMASK_CLEAR0
0x1C	IRQ_UNMASK_CLEAR1
0x20	IRQ_POLARITY0
0x24	IRQ_POLARITY1
0x40	IRQ_INDEX

Table 3.95 - Register Map

3.6.2 Register List

3.6.2.1 Register IRQ_STATUS0

This register provides the interrupt current status

Address	Access		IRQ_STATUS0																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+0'H	W	R	IRQ_STATUS0[31]	IRQ_STATUS0[30]	IRQ_STATUS0[29]	IRQ_STATUS0[28]	IRQ_STATUS0[27]	IRQ_STATUS0[26]	IRQ_STATUS0[25]	IRQ_STATUS0[24]	IRQ_STATUS0[23]	IRQ_STATUS0[22]	IRQ_STATUS0[21]	IRQ_STATUS0[20]	IRQ_STATUS0[19]	IRQ_STATUS0[18]	IRQ_STATUS0[17]	IRQ_STATUS0[16]	IRQ_STATUS0[15]	IRQ_STATUS0[14]	IRQ_STATUS0[13]	IRQ_STATUS0[12]	IRQ_STATUS0[11]	IRQ_STATUS0[10]	IRQ_STATUS0[9]	IRQ_STATUS0[8]	IRQ_STATUS0[7]	IRQ_STATUS0[6]	IRQ_STATUS0[5]	IRQ_STATUS0[4]	IRQ_STATUS0[3]	IRQ_STATUS0[2]	IRQ_STATUS0[1]	IRQ_STATUS0[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
SW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 3.96 - Register IRQ_STATUS0

Name	Type	Size	Description
IRQ_STATUS0[31:0]	U	32	Return the current status of interrupt. Reading 1 in a bit indicate that the interrupt associated to this bit is pending

Table 3.97 - Register IRQ_STATUS0 fields description

3.6.2.2 Register IRQ_STATUS1

This register provides the interrupt current status

Address	Access		IRQ_STATUS1																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+4'H	W	R	IRQ_STATUS1[31]	IRQ_STATUS1[30]	IRQ_STATUS1[29]	IRQ_STATUS1[28]	IRQ_STATUS1[27]	IRQ_STATUS1[26]	IRQ_STATUS1[25]	IRQ_STATUS1[24]	IRQ_STATUS1[23]	IRQ_STATUS1[22]	IRQ_STATUS1[21]	IRQ_STATUS1[20]	IRQ_STATUS1[19]	IRQ_STATUS1[18]	IRQ_STATUS1[17]	IRQ_STATUS1[16]	IRQ_STATUS1[15]	IRQ_STATUS1[14]	IRQ_STATUS1[13]	IRQ_STATUS1[12]	IRQ_STATUS1[11]	IRQ_STATUS1[10]	IRQ_STATUS1[9]	IRQ_STATUS1[8]	IRQ_STATUS1[7]	IRQ_STATUS1[6]	IRQ_STATUS1[5]	IRQ_STATUS1[4]	IRQ_STATUS1[3]	IRQ_STATUS1[2]	IRQ_STATUS1[1]	IRQ_STATUS1[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
SW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 3.98 - Register IRQ_STATUS1

Name	Type	Size	Description
IRQ_STATUS1[31:0]	U	32	Return the current status of interrupt. Reading 1 in a bit indicate that the interrupt associated to this bit is pending

Table 3.99 - Register IRQ_STATUS1 fields description

3.6.2.3 Register IRQ_RAW_STATUS0

This register provides the interrupt current status before mask

Address	Access		IRQ_RAW_STATUS0																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+8'H	W	R	IRQ_RAW_STATUS0[31]	IRQ_RAW_STATUS0[30]	IRQ_RAW_STATUS0[29]	IRQ_RAW_STATUS0[28]	IRQ_RAW_STATUS0[27]	IRQ_RAW_STATUS0[26]	IRQ_RAW_STATUS0[25]	IRQ_RAW_STATUS0[24]	IRQ_RAW_STATUS0[23]	IRQ_RAW_STATUS0[22]	IRQ_RAW_STATUS0[21]	IRQ_RAW_STATUS0[20]	IRQ_RAW_STATUS0[19]	IRQ_RAW_STATUS0[18]	IRQ_RAW_STATUS0[17]	IRQ_RAW_STATUS0[16]	IRQ_RAW_STATUS0[15]	IRQ_RAW_STATUS0[14]	IRQ_RAW_STATUS0[13]	IRQ_RAW_STATUS0[12]	IRQ_RAW_STATUS0[11]	IRQ_RAW_STATUS0[10]	IRQ_RAW_STATUS0[9]	IRQ_RAW_STATUS0[8]	IRQ_RAW_STATUS0[7]	IRQ_RAW_STATUS0[6]	IRQ_RAW_STATUS0[5]	IRQ_RAW_STATUS0[4]	IRQ_RAW_STATUS0[3]	IRQ_RAW_STATUS0[2]	IRQ_RAW_STATUS0[1]	IRQ_RAW_STATUS0[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
SW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 3.100 - Register IRQ_RAW_STATUS0

Name	Type	Size	Description
IRQ_RAW_STATUS0[31:0]	U	32	Return the current status of interrupt before applying the mask. Reading 1 in a bit indicate that the interrupt associated to this bit is pending

Table 3.101 - Register IRQ_RAW_STATUS0 fields description

3.6.2.4 Register IRQ_RAW_STATUS1

This register provides the interrupt current status before mask

Address	Access		IRQ_RAW_STATUS1																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+C'H	W	R	IRQ_RAW_STATUS1[31]	IRQ_RAW_STATUS1[30]	IRQ_RAW_STATUS1[29]	IRQ_RAW_STATUS1[28]	IRQ_RAW_STATUS1[27]	IRQ_RAW_STATUS1[26]	IRQ_RAW_STATUS1[25]	IRQ_RAW_STATUS1[24]	IRQ_RAW_STATUS1[23]	IRQ_RAW_STATUS1[22]	IRQ_RAW_STATUS1[21]	IRQ_RAW_STATUS1[20]	IRQ_RAW_STATUS1[19]	IRQ_RAW_STATUS1[18]	IRQ_RAW_STATUS1[17]	IRQ_RAW_STATUS1[16]	IRQ_RAW_STATUS1[15]	IRQ_RAW_STATUS1[14]	IRQ_RAW_STATUS1[13]	IRQ_RAW_STATUS1[12]	IRQ_RAW_STATUS1[11]	IRQ_RAW_STATUS1[10]	IRQ_RAW_STATUS1[9]	IRQ_RAW_STATUS1[8]	IRQ_RAW_STATUS1[7]	IRQ_RAW_STATUS1[6]	IRQ_RAW_STATUS1[5]	IRQ_RAW_STATUS1[4]	IRQ_RAW_STATUS1[3]	IRQ_RAW_STATUS1[2]	IRQ_RAW_STATUS1[1]	IRQ_RAW_STATUS1[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
SW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 3.102 - Register IRQ_RAW_STATUS1

Name	Type	Size	Description
IRQ_RAW_STATUS1[31:0]	U	32	Return the current status of interrupt before applying the mask. Reading 1 in a bit indicate that the interrupt associated to this bit is pending

Table 3.103 - Register IRQ_RAW_STATUS1 fields description

3.6.2.5 Register IRQ_UNMASK_SET0

This register sets the interrupt mask

Address	Access		IRQ_UNMASK_SET0																											
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+10'H	RW	S	IRQ_UNMASK_SET0[31]	IRQ_UNMASK_SET0[30]	IRQ_UNMASK_SET0[29]	IRQ_UNMASK_SET0[28]	IRQ_UNMASK_SET0[27]	IRQ_UNMASK_SET0[26]	IRQ_UNMASK_SET0[25]	IRQ_UNMASK_SET0[24]	IRQ_UNMASK_SET0[23]	IRQ_UNMASK_SET0[22]	IRQ_UNMASK_SET0[21]	IRQ_UNMASK_SET0[20]	IRQ_UNMASK_SET0[19]	IRQ_UNMASK_SET0[18]	IRQ_UNMASK_SET0[17]	IRQ_UNMASK_SET0[16]	IRQ_UNMASK_SET0[15]	IRQ_UNMASK_SET0[14]	IRQ_UNMASK_SET0[13]	IRQ_UNMASK_SET0[12]	IRQ_UNMASK_SET0[11]	IRQ_UNMASK_SET0[10]	IRQ_UNMASK_SET0[9]	IRQ_UNMASK_SET0[8]	IRQ_UNMASK_SET0[7]	IRQ_UNMASK_SET0[6]	IRQ_UNMASK_SET0[5]	IRQ_UNMASK_SET0[4]	IRQ_UNMASK_SET0[3]	IRQ_UNMASK_SET0[2]	IRQ_UNMASK_SET0[1]	IRQ_UNMASK_SET0[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
SW Access			S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S

Table 3.104 - Register IRQ_UNMASK_SET0

Name	Type	Size	Description
IRQ_UNMASK_SET0[31:0]	U	32	Writing 1 in a field unmasks the interrupt

Table 3.105 - Register IRQ_UNMASK_SET0 fields description

3.6.2.6 Register IRQ_UNMASK_SET1

This register sets the interrupt mask

Address	Access		IRQ_UNMASK_SET1																											
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+14'H	RW	S	IRQ_UNMASK_SET1[31]	IRQ_UNMASK_SET1[30]	IRQ_UNMASK_SET1[29]	IRQ_UNMASK_SET1[28]	IRQ_UNMASK_SET1[27]	IRQ_UNMASK_SET1[26]	IRQ_UNMASK_SET1[25]	IRQ_UNMASK_SET1[24]	IRQ_UNMASK_SET1[23]	IRQ_UNMASK_SET1[22]	IRQ_UNMASK_SET1[21]	IRQ_UNMASK_SET1[20]	IRQ_UNMASK_SET1[19]	IRQ_UNMASK_SET1[18]	IRQ_UNMASK_SET1[17]	IRQ_UNMASK_SET1[16]	IRQ_UNMASK_SET1[15]	IRQ_UNMASK_SET1[14]	IRQ_UNMASK_SET1[13]	IRQ_UNMASK_SET1[12]	IRQ_UNMASK_SET1[11]	IRQ_UNMASK_SET1[10]	IRQ_UNMASK_SET1[9]	IRQ_UNMASK_SET1[8]	IRQ_UNMASK_SET1[7]	IRQ_UNMASK_SET1[6]	IRQ_UNMASK_SET1[5]	IRQ_UNMASK_SET1[4]	IRQ_UNMASK_SET1[3]	IRQ_UNMASK_SET1[2]	IRQ_UNMASK_SET1[1]	IRQ_UNMASK_SET1[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
SW Access			S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S

Table 3.106 - Register IRQ_UNMASK_SET1

Name	Type	Size	Description
IRQ_UNMASK_SET1[31:0]	U	32	Writing 1 in a field unmasks the interrupt

Table 3.107 - Register IRQ_UNMASK_SET1 fields description

3.6.2.7 Register IRQ_UNMASK_CLEAR0

This register clears the interrupt mask

Address	Access		IRQ_UNMASK_CLEAR0																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+18'H	RW	C	IRQ_UNMASK_CLEAR0[31]	IRQ_UNMASK_CLEAR0[30]	IRQ_UNMASK_CLEAR0[29]	IRQ_UNMASK_CLEAR0[28]	IRQ_UNMASK_CLEAR0[27]	IRQ_UNMASK_CLEAR0[26]	IRQ_UNMASK_CLEAR0[25]	IRQ_UNMASK_CLEAR0[24]	IRQ_UNMASK_CLEAR0[23]	IRQ_UNMASK_CLEAR0[22]	IRQ_UNMASK_CLEAR0[21]	IRQ_UNMASK_CLEAR0[20]	IRQ_UNMASK_CLEAR0[19]	IRQ_UNMASK_CLEAR0[18]	IRQ_UNMASK_CLEAR0[17]	IRQ_UNMASK_CLEAR0[16]	IRQ_UNMASK_CLEAR0[15]	IRQ_UNMASK_CLEAR0[14]	IRQ_UNMASK_CLEAR0[13]	IRQ_UNMASK_CLEAR0[12]	IRQ_UNMASK_CLEAR0[11]	IRQ_UNMASK_CLEAR0[10]	IRQ_UNMASK_CLEAR0[9]	IRQ_UNMASK_CLEAR0[8]	IRQ_UNMASK_CLEAR0[7]	IRQ_UNMASK_CLEAR0[6]	IRQ_UNMASK_CLEAR0[5]	IRQ_UNMASK_CLEAR0[4]	IRQ_UNMASK_CLEAR0[3]	IRQ_UNMASK_CLEAR0[2]	IRQ_UNMASK_CLEAR0[1]	IRQ_UNMASK_CLEAR0[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
SW Access			C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C

Table 3.108 - Register IRQ_UNMASK_CLEAR0

Name	Type	Size	Description
IRQ_UNMASK_CLEAR0[31:0]	U	32	Writing 1 in a field masks the interrupt

Table 3.109 - Register IRQ_UNMASK_CLEAR0 fields description

3.6.2.8 Register IRQ_UNMASK_CLEAR1

This register clears the interrupt mask

Address	Access		IRQ_UNMASK_CLEAR1																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+1C'H	RW	C	IRQ_UNMASK_CLEAR1[31]	IRQ_UNMASK_CLEAR1[30]	IRQ_UNMASK_CLEAR1[29]	IRQ_UNMASK_CLEAR1[28]	IRQ_UNMASK_CLEAR1[27]	IRQ_UNMASK_CLEAR1[26]	IRQ_UNMASK_CLEAR1[25]	IRQ_UNMASK_CLEAR1[24]	IRQ_UNMASK_CLEAR1[23]	IRQ_UNMASK_CLEAR1[22]	IRQ_UNMASK_CLEAR1[21]	IRQ_UNMASK_CLEAR1[20]	IRQ_UNMASK_CLEAR1[19]	IRQ_UNMASK_CLEAR1[18]	IRQ_UNMASK_CLEAR1[17]	IRQ_UNMASK_CLEAR1[16]	IRQ_UNMASK_CLEAR1[15]	IRQ_UNMASK_CLEAR1[14]	IRQ_UNMASK_CLEAR1[13]	IRQ_UNMASK_CLEAR1[12]	IRQ_UNMASK_CLEAR1[11]	IRQ_UNMASK_CLEAR1[10]	IRQ_UNMASK_CLEAR1[9]	IRQ_UNMASK_CLEAR1[8]	IRQ_UNMASK_CLEAR1[7]	IRQ_UNMASK_CLEAR1[6]	IRQ_UNMASK_CLEAR1[5]	IRQ_UNMASK_CLEAR1[4]	IRQ_UNMASK_CLEAR1[3]	IRQ_UNMASK_CLEAR1[2]	IRQ_UNMASK_CLEAR1[1]	IRQ_UNMASK_CLEAR1[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
SW Access			C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C

Table 3.110 - Register IRQ_UNMASK_CLEAR1

Name	Type	Size	Description
IRQ_UNMASK_CLEAR1[31:0]	U	32	Writing 1 in a field masks the interrupt

Table 3.111 - Register IRQ_UNMASK_CLEAR1 fields description

3.6.2.9 Register IRQ_POLARITY0

This register controls the polarity of interrupt input

Address	Access		IRQ_POLARITY0																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

+20'H	R	RW	IRQ_POLARITY0[31]	IRQ_POLARITY0[30]	IRQ_POLARITY0[29]	IRQ_POLARITY0[28]	IRQ_POLARITY0[27]	IRQ_POLARITY0[26]	IRQ_POLARITY0[25]	IRQ_POLARITY0[24]	IRQ_POLARITY0[23]	IRQ_POLARITY0[22]	IRQ_POLARITY0[21]	IRQ_POLARITY0[20]	IRQ_POLARITY0[19]	IRQ_POLARITY0[18]	IRQ_POLARITY0[17]	IRQ_POLARITY0[16]	IRQ_POLARITY0[15]	IRQ_POLARITY0[14]	IRQ_POLARITY0[13]	IRQ_POLARITY0[12]	IRQ_POLARITY0[11]	IRQ_POLARITY0[10]	IRQ_POLARITY0[9]	IRQ_POLARITY0[8]	IRQ_POLARITY0[7]	IRQ_POLARITY0[6]	IRQ_POLARITY0[5]	IRQ_POLARITY0[4]	IRQ_POLARITY0[3]	IRQ_POLARITY0[2]	IRQ_POLARITY0[1]	IRQ_POLARITY0[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
SW Access			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 3.112 - Register IRQ_POLARITY0

Name	Type	Size	Description
IRQ_POLARITY0[31:0]	U	32	Interrupt polarity. 0: active high interrupt. 1 : active low interrupt

Table 3.113 - Register IRQ_POLARITY0 fields description

3.6.2.10 Register IRQ_POLARITY1

This register controls the polarity of interrupt input

Address	Access		IRQ_POLARITY1																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+24'H	R	RW	IRQ_POLARITY1[31]	IRQ_POLARITY1[30]	IRQ_POLARITY1[29]	IRQ_POLARITY1[28]	IRQ_POLARITY1[27]	IRQ_POLARITY1[26]	IRQ_POLARITY1[25]	IRQ_POLARITY1[24]	IRQ_POLARITY1[23]	IRQ_POLARITY1[22]	IRQ_POLARITY1[21]	IRQ_POLARITY1[20]	IRQ_POLARITY1[19]	IRQ_POLARITY1[18]	IRQ_POLARITY1[17]	IRQ_POLARITY1[16]	IRQ_POLARITY1[15]	IRQ_POLARITY1[14]	IRQ_POLARITY1[13]	IRQ_POLARITY1[12]	IRQ_POLARITY1[11]	IRQ_POLARITY1[10]	IRQ_POLARITY1[9]	IRQ_POLARITY1[8]	IRQ_POLARITY1[7]	IRQ_POLARITY1[6]	IRQ_POLARITY1[5]	IRQ_POLARITY1[4]	IRQ_POLARITY1[3]	IRQ_POLARITY1[2]	IRQ_POLARITY1[1]	IRQ_POLARITY1[0]
Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
HW Access			R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
SW Access			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 3.114 - Register IRQ_POLARITY1

Name	Type	Size	Description
IRQ_POLARITY1[31:0]	U	32	Interrupt polarity. 0: active high interrupt. 1 : active low interrupt

Table 3.115 - Register IRQ_POLARITY1 fields description

3.6.2.11 Register IRQ_INDEX

This register provides the lowest pending interrupt index

Address	Access		IRQ_INDEX																													
	HW	SW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+40'H	W	R																											IRQ_INDEX[5]	IRQ_INDEX[4]	IRQ_INDEX[3]	IRQ_INDEX[2]	IRQ_INDEX[1]	IRQ_INDEX[0]

Reset Value																											0	0	0	0	0	0
Type																											U	U	U	U	U	U
HW Access																											W	W	W	W	W	W
SW Access																											R	R	R	R	R	R

Table 3.116 - Register IRQ_INDEX

Name	Type	Size	Description
IRQ_INDEX[5:0]	U	6	Returns the index of the lowest pending interrupt

Table 3.117 - Register IRQ_INDEX fields description

3.7 Packet Traffic Arbiter (PTA) registers

Refer to [2].

3.8 Hardware Security Unit (HSU) registers

Refer to [5]

3.9 Platform DMA registers

Refer to [1]

3.10 MAC registers

Refer to [4]

3.11 Embedded LA registers

Refer to [3]

4 Hardware Interface

This chapter describes the port map of rw_nx_platform module.

Name	Type	Size	Description
Clocks / Resets Inputs			
system resets			
sys_rst_n	input	1	System Reset active Low
Clocks			
ref0_root_clk	input	1	Reference clock for PHY (240/480 Mhz)
ref1_root_clk	input	1	Reference clock for MAC (80 Mhz)
plf_root_clk	input	1	Platform clock
mac_lp_root_clk	input	1	Low-Power clock
ref40_clk	output	1	40 MHz Reference Clock output
ref40_rst_n	output	1	40 MHz Reference Reset output (Active Low)
plf_clk	output	1	Platform Clock output
plf_rst_n	output	1	Platform Reset output (Active Low)
plf_por_n	output	1	Platform Power On Reset output (Active Low)
Clock enables			
platform_wake_up	output	1	Wake Up platform
AHB Slave interface			
target_hready	output	1	Processor hready
target_hready_in	input	1	Processor hready_in
target_haddr	input	32	Processor haddr
target_htrans	input	2	Processor htrans
target_hwrite	input	1	Processor hwrite
target_hmastlock	input	1	Processor hmastlock
target_hburst	input	3	Processor hburst
target_hprot	input	4	Processor hprot
target_hsize	input	3	Processor hsize
target_hrdata	output	32	Processor hrdata
target_hwdata	input	32	Processor hwdata
target_hresp	output	2	Processor hresp
host_irq	output	1	Interrupt from host
GPIO interface			
gpio_out	output	32	GPIO output
gpio_in	input	32	GPIO input
gpio_oen	output	32	GPIO output enable
AHB to Coexistence interface			
coexif_hready_in	output	1	Coexistence Interface hready_in
coexif_hsel	output	1	Coexistence Interface hsel
coexif_haddr	output	9	Coexistence Interface haddr
coexif_htrans	output	2	Coexistence Interface htrans
coexif_hwrite	output	1	Coexistence Interface hwrite
coexif_hrdata	input	32	Coexistence Interface hrdata
coexif_hwdata	output	32	Coexistence Interface hwdata
coexif_hresp	input	2	Coexistence Interface hresp
coexif_hready	input	1	Coexistence Interface hready
Bluetooth Coexistence Interface			
coex_bt_tx	input	1	BT Transmission On-going
coex_bt_rx	input	1	BT ReceptionOn-going
coex_bt_event	input	1	BT EventOn-going
coex_bt_tx_abort	output	1	BT Transmission Abort Request
coex_bt_rx_abort	output	1	BT ReceptionAbort Request

coex_bt_pti	input	4	BT Packet Traffic Information
coex_bt_channel	input	7	BT Channel (0-78)
coex_bt_bw	input	1	BT Bandwidth (0:1MHz, 1:2MHz)
RC Coexistence interface			
rc_tx_abort	output	1	Radio Controller Transmission Abort Request
rc_rx_abort	output	1	Radio Controller ReceptionAbort Request
AXI Interface			
upstream interface			
dma0_awid	output	4	DMA Upstream awid
dma0_awaddr	output	32	DMA Upstream awaddr
dma0_awlen	output	8	DMA Upstream awlen
dma0_awsize	output	3	DMA Upstream awsize
dma0_awburst	output	2	DMA Upstream awburst
dma0_awuser	output	12	DMA Upstream awuser
dma0_awvalid	output	1	DMA Upstream awvalid
dma0_awready	input	1	DMA Upstream awready
dma0_wid	output	4	DMA Upstream wid
dma0_wdata	output	64	DMA Upstream wdata
dma0_wstrb	output	8	DMA Upstream wstrb
dma0_wlast	output	1	DMA Upstream wlast
dma0_wvalid	output	1	DMA Upstream wvalid
dma0_wready	input	1	DMA Upstream wready
dma0_bid	input	4	DMA Upstream bid
dma0_bresp	input	2	DMA Upstream bresp
dma0_bvalid	input	1	DMA Upstream bvalid
dma0_bready	output	1	DMA Upstream bready
downstream interface			
dma1_arid	output	4	DMA Downstream arid
dma1_araddr	output	32	DMA Downstream araddr
dma1_arlen	output	8	DMA Downstream arlen
dma1_arsize	output	3	DMA Downstream arsize
dma1_arburst	output	2	DMA Downstream arburst
dma1_arvalid	output	1	DMA Downstream arvalid
dma1_arready	input	1	DMA Downstream arready
dma1_rid	input	4	DMA Downstream rid
dma1_rdata	input	64	DMA Downstream rdata
dma1_rresp	input	2	DMA Downstream rresp
dma1_rlast	input	1	DMA Downstream rlast
dma1_rvalid	input	1	DMA Downstream rvalid
dma1_rready	output	1	DMA Downstream rready
ADC Interface			
adc0_on	output	1	ADC0 Power/Clock enable
adc0_i	input	12	ADC0 Data I
adc0_q	input	12	ADC0 Data Q
adc1_on	output	1	ADC1 Power/Clock enable
adc1_i	input	12	ADC1 Data I
adc1_q	input	12	ADC1 Data Q
DAC Interface			
dac0_on	output	1	DAC0 Power/Clock enable
dac0_en	output	1	DAC0 Data valid
dac0_i	output	12	DAC0 Data I
dac0_q	output	12	DAC0 Data Q
dac1_on	output	1	DAC1 Power/Clock enable
dac1_en	output	1	DAC1 Data valid
dac1_i	output	12	DAC1 Data I

dac1_q	output	12	DAC1 Data Q
RF interface			
Reset output			
rf_resetn	output	1	Active Low Reset for Radio
RF AGC Control			
rf_agcfreeze	output	1	AGC freeze
RF Test mode			
rf_tmode	output	1	Radio Test Mode
Fast write bus			
rf_gpio	output	8	GPIO Data
SPI Interface			
rf_spi_in	input	1	SPI Interface In
rf_spi_ss_n	output	1	SPI Interface Slave Select
rf_spi_clk	output	1	SPI Interface Clock
rf_spi_out	output	1	SPI Interface Out
Tx/Rx switch			
rf_trsw0	output	1	Radio Tx On 0
rf_trsw1	output	1	Radio Tx On 1
External PA			
rf_extpaon_ch0_5G9	output	1	Radio External PA Channel 0 5Ghz
rf_extpaon_ch0_2G4	output	1	Radio External PA Channel 0 2.4Ghz
rf_extpaon_ch1_5G9	output	1	Radio External PA Channel 1 5Ghz
rf_extpaon_ch1_2G4	output	1	Radio External PA Channel 1 2.4Ghz
AHB to FPGA			
fpga_hready_in	output	1	FPGA hready_in
fpga_hsel	output	1	FPGA hsel
fpga_haddr	output	20	FPGA haddr
fpga_htrans	output	2	FPGA htrans
fpga_hwrite	output	1	FPGA hwrite
fpga_hrdata	input	32	FPGA hrdata
fpga_hwdata	output	32	FPGA hwdata
fpga_hresp	input	2	FPGA hresp
fpga_hready	input	1	FPGA hready
Diagnostic Ports			
ext_diagport	input	32	Diagnostic port
reg_bootrom_enable	output	1	CPU Boot enable
rw_nx_ss_diag	output	5	Diagnostic port to be used with IQ for source synchrone capture
rw_nx_diag0	output	32	Diagnostic port
rw_nx_diag1	output	32	Diagnostic port
rw_nx_diag2	output	32	Diagnostic port
mac_internal_error	output	1	MAC internal Error
mac_debug_ksr	input	1	Debug Key Storage RAM.
macbypass_trigger	output	2	MAC Bypass Trigger Port
reg_diag_trigger	output	1	SW Trigger Port
JTAG			
jtag_rtck	output	1	JTAG RTCK
jtag_tdo	output	1	JTAG TDO
jtag_tdi	input	1	JTAG TDI
jtag_tms	input	1	JTAG TMS
jtag_tck	input	1	JTAG TCK

Table 4.1 - rw_he_top_cpu module port map

References

[1]	**Title**	RW-WLAN nX PLATFORM DMA Functional Specification
	Reference	RW-DMA-FS.pdf

[2]	**Title**	RW Packet Traffic Arbiter Design Specification
	Reference	RW-PTA-DS.pdf

[3]	**Title**	RW-WLAN-nX Embedded Logic Analyzer User Manual
	Reference	RW-WLAN-nX-EMB-LA-UM.pdf

[4]	**Title**	RW-WLAN-HE MAC HW User Manual
	Reference	RW-WLAN-HE-MAC-HW-UM.pdf

[5]	**Title**	RW-WLAN-nX HSU Design Document
	Reference	RW-WLAN-HSU-DS.pdf