AN18.6

SMSC Ethernet Physical Layer Layout Guidelines

1 Introduction

SMSC Ethernet products are highly-integrated devices designed for 10 or 100 Mbps Ethernet systems. They are based on IEEE 10BASE-T and 100BASE-TX standards. The IEEE 802.3-2005 standard for 100BASE-TX defines networking over two pairs of Category 5 unshielded twisted pair cable or Type 1 shielded twisted pair cable.

This application note is intended to assist customers in designing a PCB using SMSC's Ethernet products to interface with an Ethernet network. This document provides recommendations regarding the PCB layout. This is a critical component in maintaining signal integrity, and reducing EMI.

1.1 Audience

This application note is written for a reader that is familiar with Ethernet hardware design.

1.2 Overview

The following recommendations for the printed circuit board layout with SMSC parts are not the only way to layout SMSC Ethernet QFP/QFN parts. Every board designer will have a preference. Complexity, board space, number and types of devices will dictate routing and placement strategies. For example, the PCB described in this application note has components on both sides of the board. A four layer board could be realized with components on one side only. The datasheets and reference schematics for SMSC Ethernet products should be used as a reference for this layout design guideline.

2 General Design Guidelines

The Evaluation Board (EVB) schematics and gerber files are available on the SMSC web site. These can be used as a reference for component placement and routing.

Good engineering practices should be followed with respect to unused inputs by terminating them with pull-up or pull-down resistors, unless the datasheet, design guide or reference schematic indicates otherwise. Do not attach pull-up or pull-down resistors to any pins identified as reserved (unless explicitly stated in the datasheet). These devices may have special test modes that could be entered inadvertently.

2.1 Industrial Temperature

When designing with the industrial temperature version of the PHY, care needs to be given to the temperature range of the supporting components. If the end application requires industrial temperature support, then the system designer needs to select all pertinent components to be functional in the industrial temperature range.

2.2 Power and Ground Planes

The sections below describe typical 2 and 4 layer board stackups for Ethernet Physical Layer designs. The goal of the 4 layer designs is to keep the signal routing on outer layers, isolated by the power and ground planes. These power and ground planes also serve the purpose of reference planes for the signal traces. The signal traces should run over continuous reference planes when possible. When 2 layer board designs are required, it remains necessary that the signal traces run over continuous reference planes when possible.

2.2.1 4 Layer Stackup

- Top (Layer 1) – Signal with ground plane except where noted.
- Layer 2 – Continuous ground plane. No signals should be routed on this layer.
- Layer 3 – Power planes with ground planes except where noted. Signals may be routed on this layer if needed, especially for buried MII/RMII bus and MII/RMII CLK signals.
- Bottom (Layer 4) – Signal with ground plane except where noted.
- Decouple ground floods and ground layer as practical. When signal traces are re-referenced to power island planes, decoupling capacitors (0.01uF ceramic) are required between the ground plane and power plane.
- Signal traces routed on bottom layer over power islands that are on Layer 3 layer should have decoupling capacitors (0.01uF ceramic) near the trace to enable short (direct) return current paths.
- When signal traces are re-referenced to power island planes, decoupling capacitors (0.01uF ceramic) are required between the ground plane and power plane as shown below in Figure 2.1

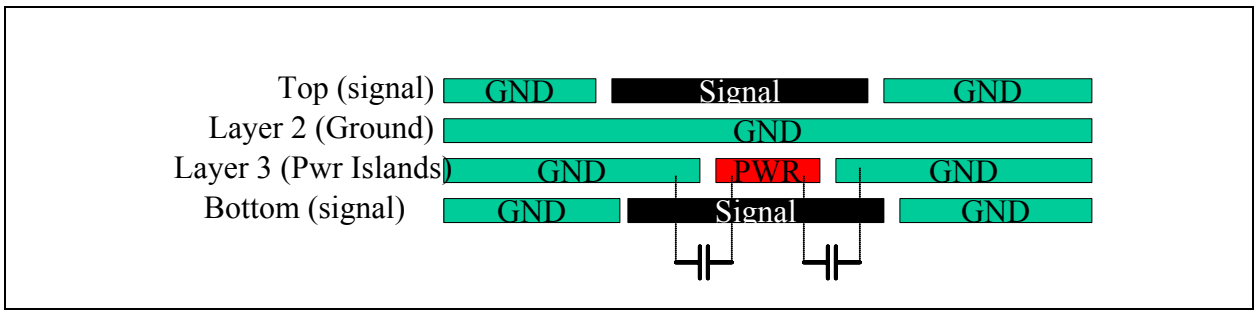

Figure 2.1 4 Layer Stackup Power and Ground Decoupling

2.2.2 2 Layer Stackup

- Top (Layer 1) Signal with ground plane except where noted.
- Bottom (Layer 2) Ground plane and power islands. A limited number of slow speed signals may be routed on the bottom layer.
- Signal traces should be surrounded by ground or ground trace along at least one edge. If ground trace is used, it should be connected to ground plane on this layer and decoupled to ground plane on top layer.

- Decouple ground planes as practical, as shown below in Figure 2.2. This will allow short (direct) return current paths when signal traces are re-referenced to different power island planes.

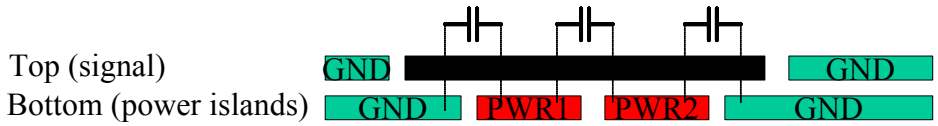

Figure 2.2 2 Layer Stackup Power and Ground Decoupling

2.3 Component Placement

Component placement can affect signal quality, emissions, and component operating temperature. Careful component placement can decrease potential EMI problems and simplify the task of routing traces.

- If the magnetic is a discrete component, then the distance between the magnetic and the RJ-45 needs to have the highest consideration and be kept to under 25mm (approx. 1 inch) of separation. Refer to Figure 2.3.

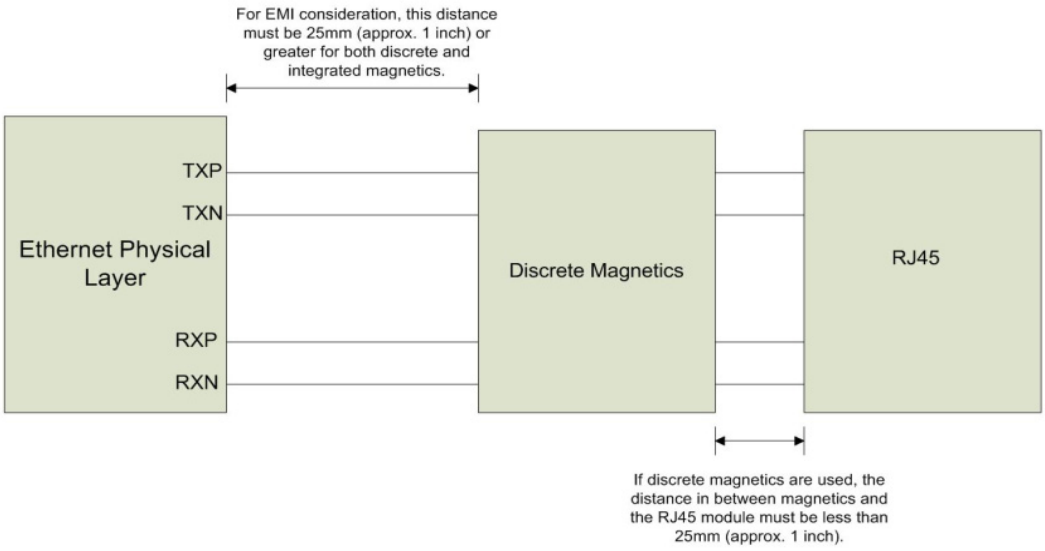

Figure 2.3 Discrete Magnetic and RJ-45 Placement

- The distance between the PHY and the magnetics needs to be 25mm (approx. 1 inch) or greater. Among PHY vendors, the 25mm (approx. 1 inch) rule is considered good design practice for EMI considerations. The intention is to isolate the PHY from the magnetics.
- The crystal oscillator and its resistors and capacitors must be placed within 12mm (approx. 500mils) of the PHY.
- The power supply decoupling capacitors need to be placed within 7mm (approx. 280mils) of the power supply.

- Keep the PHY device and the differential transmit pairs at least 25mm (approx. 1 inch) from the edge of the PCB, up to the magnetics. If the magnetics are integrated into the RJ45, the differential pairs should be routed to the back of the integrated magnetics RJ45 connector, away from the board edge.
- The 49.9 ohm pull-up resistors on the differential lines, TXP/TXN and RXP/RXN, must be placed within 10mm (approx. 400mils) of the PHY device. This ensures the transmit path is identical between the TX and RX.
- The signals associated with each port (TX or RX) should be independently matched in length to within 6mm (approx. 240 mils).
- The strapping resistors need to be located within 20mm (approx. 800mils) of the Ethernet PHY to ensure the voltage into the pin at boot-up is at the correct Vih or Vil level.

2.4 Design Techniques for EMI Suppression

The following techniques may improve EMI margin.

- Common mode capacitors may be added to the TX+/- and RX+/- signals of the Ethernet PHY device for high frequency attenuation, as shown below in Figure 2.4. One end of each capacitor should be connected to the system ground plane, and placed within 10mm (approx. 400mils) of the magnetics. Typical capacitance values should be between 10pF and 22pF. Values higher than 22pF may negatively impact the TX and RX signalling.

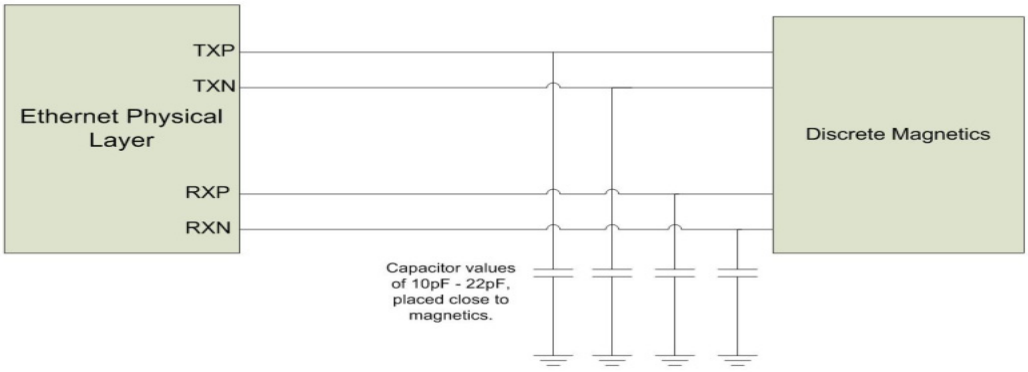

Figure 2.4 Common Mode Capacitors

- Common mode chokes may be added to the design at the point where DC power enters the PCB as shown below in Figure 2.5. This attenuates emissions that would otherwise be radiated from the system power cord. Common mode chokes will have some impedance at a given frequency. Choose the number of chokes and/or type of ferrite material to provide adequate attenuation at the frequencies in the system that may generate unwanted emissions.

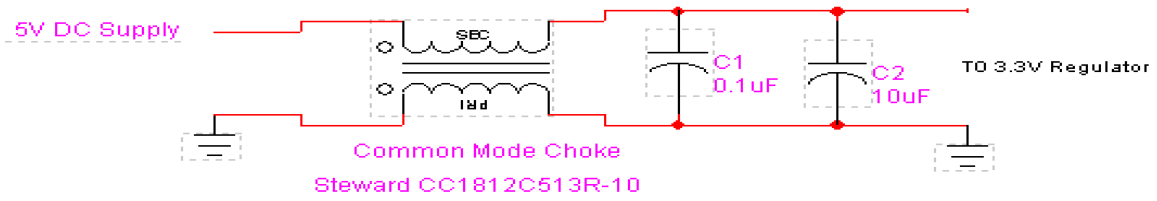

Figure 2.5 Common Mode Choke on PCB DC Input

- Common mode chokes may be added to the TX and RX differential pairs as shown below in Figure 2.6. The common mode chokes should be placed within 10mm (approx 400mils) of the integrated RJ45 module, and on the magnetics side of the common mode EMI suppression capacitors.Typical common mode impedance of the common mode choke selected should be 2Kohm @ 100MHz or higher.

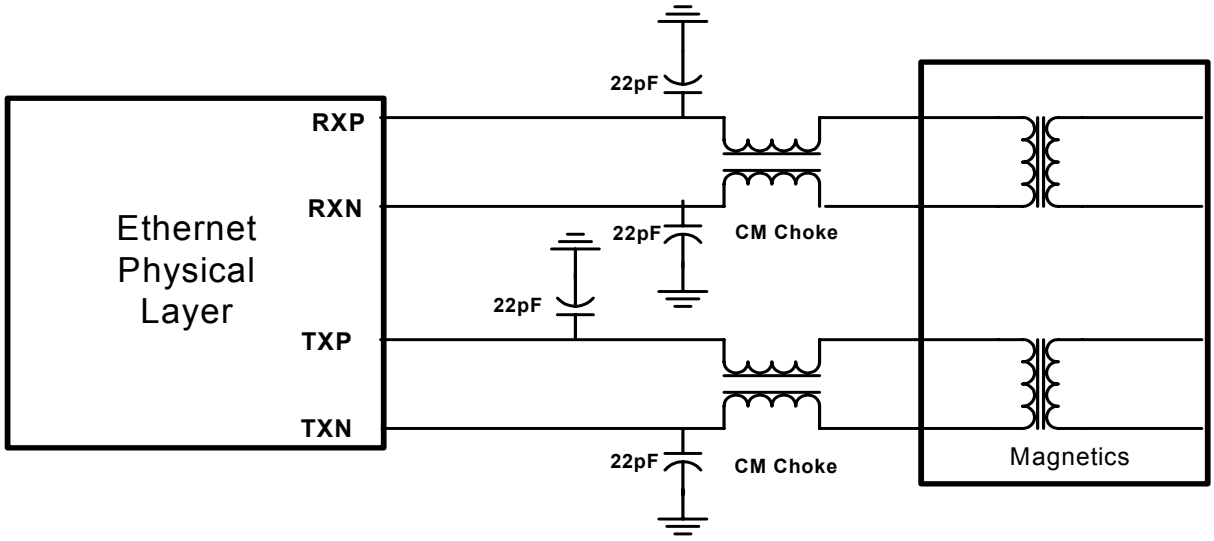

Figure 2.6 Common Mode Chokes on TX and RX pairs

- In general, no ground plane should extend under the TX and RX differential pairs, under the magnetics, or under the RJ45 jack. In the case where common mode capacitors are used for EMI suppression, a ground plane may be located under the TX and RX signals, however the plane must not extend beyond the capacitors. When designing 4 layer boards, the ground plane should exist on layer 4, assuming the differential pair is routed on layer 1. On 2 layer boards, the ground plane can be located on layer 2, the adjacent layer to the TX and RX signal pairs. Under no circumstances should a ground plane exist under the magnetics, the RJ45 connector, or in between the magnetics and RJ45 connector.

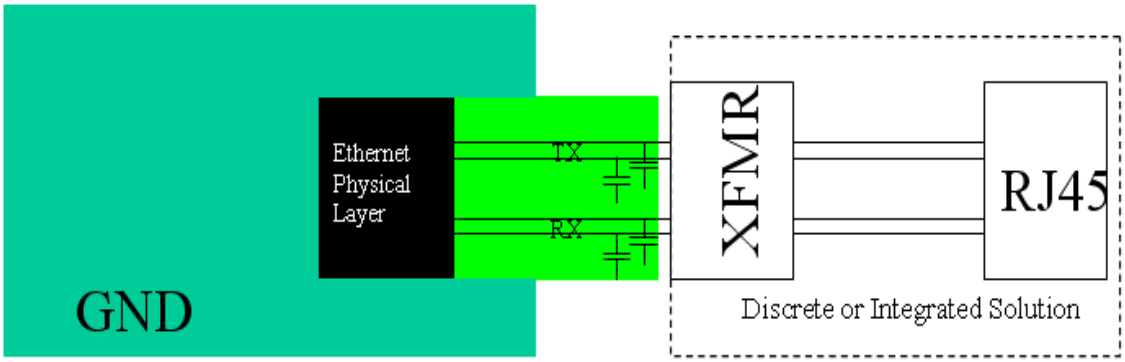

Figure 2.7

- Generally, MII/RMII interface signals can be directly routed to the MAC, however series termination resistors may be included on RXCLK, TXCLK, and all other RX MII or RMII interface signals for additional EMI suppression. Figure 2.8 below shows these termination resistors. MII/RMII series terminations should be located within 10mm (approx. 400mils) of the Ethernet physical layer device, and routed adjacent to an uninterrupted reference plane. 100 ohm series termination resistors have been found to be good values for improving EMI.

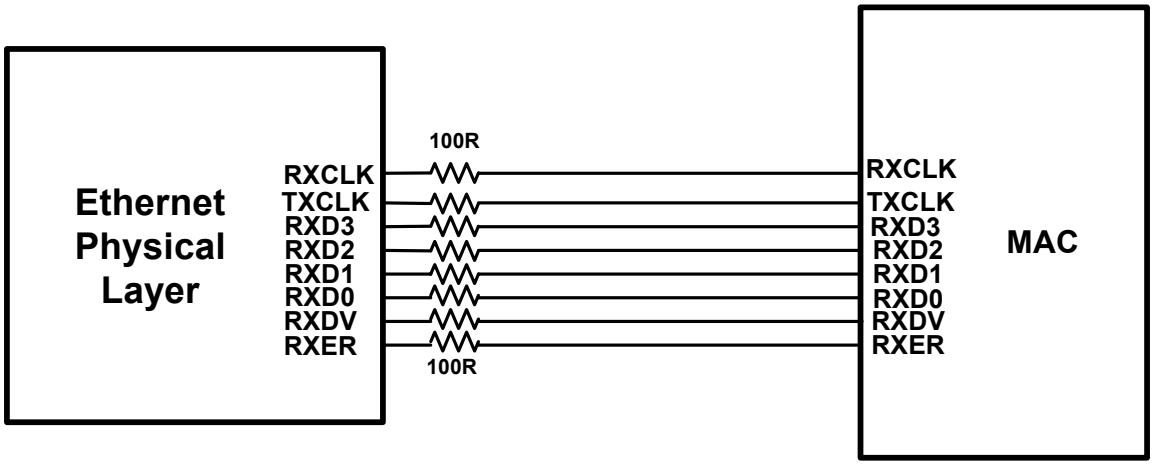

Figure 2.8

3 Review of Critical Circuits

This chapter provides guidelines for the sensitive circuits associated with the system application of SMSC Ethernet products.

3.1 Controlled Impedance for Differential Signals

The 802.3-2005 specifications requires the TX and RX lines to run in differential mode. The TXP and TXN are a differential pair and need to be designed to a 100 ohm differential impedance. The RXP

and RXN traces are also a differential pair and need to be designed to a 100 ohm differential impedance target.

The Board Designer must maintain 100 ohm differential impedance in the layout for all the differential pairs. For different dielectric thickness, copper weight or board stack-up, trace widths and spacings will need to be recalculated.

Differential pair nets must maintain symmetry. TXP and TXN must be equal length and symmetric with regards to shape, length, and via count. RXP and RXN must also be equal length and symmetric. For example, if TXP goes through a via at 8mm, then TXN should also go through a via at 8mm.

Figure 3.1 shows TX/RX traces with approximately equal trace length and symmetry. It is important to maintain width and spacing that provides differential and common mode impedances compliant with the 802.3 specification. Avoid using 90 degree turns to minimize impedance discontinuities.

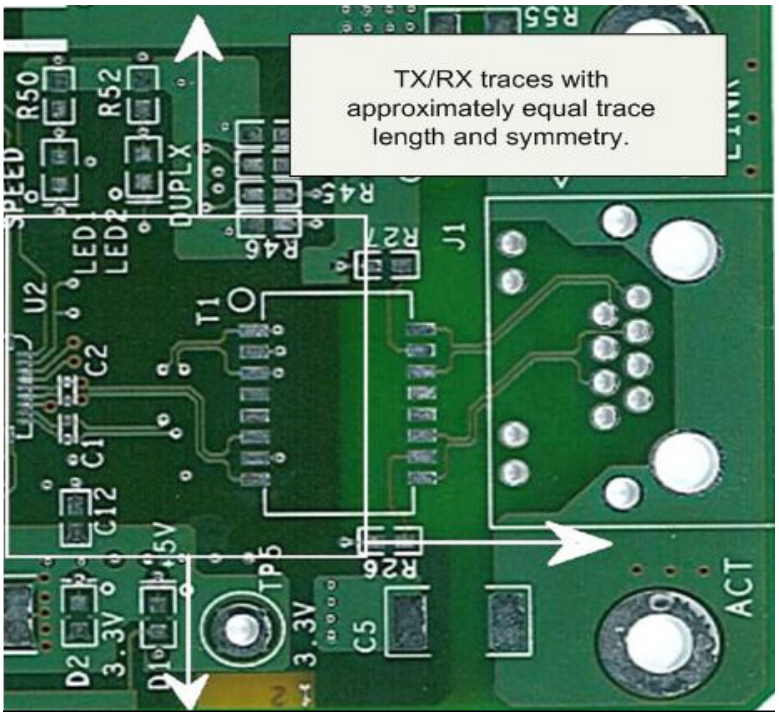

Figure 3.1 Example of Routing TX/RX to RJ-45

- Isolation of TX/RX Traces

  The TX/RX traces must be isolated from nearby circuitry and signals. Maintain a distance of parts to lines that are greater than or equal to 5 times the distance of the spacing between the traces. Do not route differential pairs under parts. Do not cross TX/RX lines with other PCB traces unless the traces are on the opposite side of the ground plane from TX/RX.

- Crystal Oscillator

  The crystal oscillator is sensitive to stray capacitances and noise from other signals. It can also disturb other signals and cause EMI noise. The load capacitors, crystal and parallel resistors should be placed within 7mm (approx. 280mils) of each other. The ground connection for the load capacitors should be short and out of the way from return currents of power lines. Figure 3.2 shows a schematic of the crystal oscillator circuit.

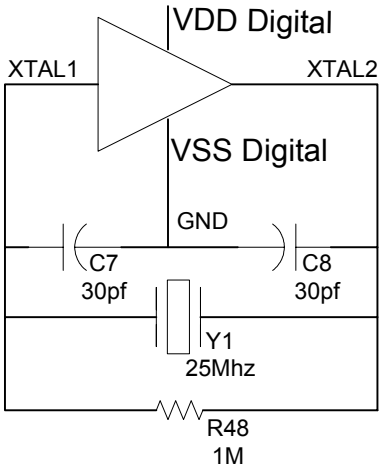

Figure 3.2 Crystal Oscillator Schematic

Figure 3.3 illustrates a suggested PCB layout of the crystal circuit. All components are far removed from TX/RX lines.

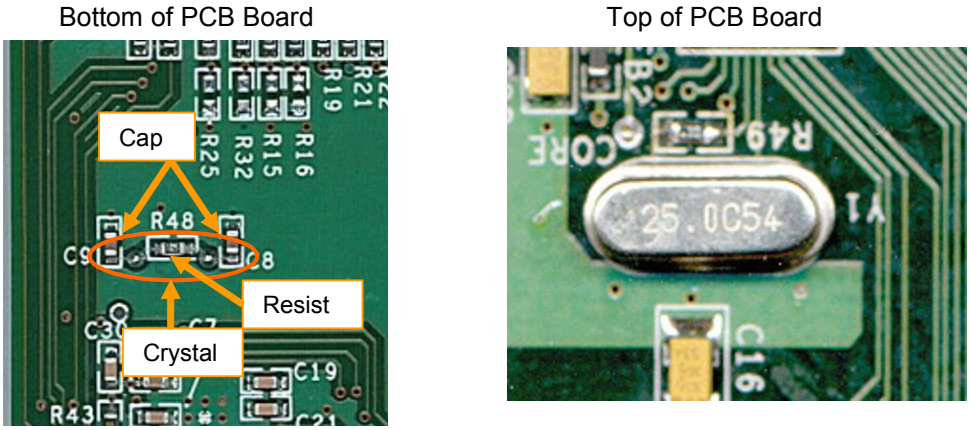

Figure 3.3 Crystal Oscillator PCB Layout

3.2 Bias Resistor pin

The EXRES/RBIAS resistor sets an internal current source reference. Thus, the EXRES/RBIAS pin is a high impedance node and so any noise induced on the EXRES/RBIAS traces will directly impact internal current references and negatively degrade eye-diagram quality. The EXRES/RBIAS resistor must have 1% tolerance or better, and should be placed within 7mm (approx. 280mils) of the EXRES/RBIAS pin. The ground return should be short and direct to VSS. Resistor traces should be very short and isolated from nearby traces if possible.

3.3 Power Supply Bypass Capacitors

Bypass capacitors should be placed within 7mm (approx. 280mils) of the power pins of the PHY and connected with short traces. SMSC Ethernet product evaluation boards have bypassing directly under the part, with return current paths tied to the bottom ground plane.

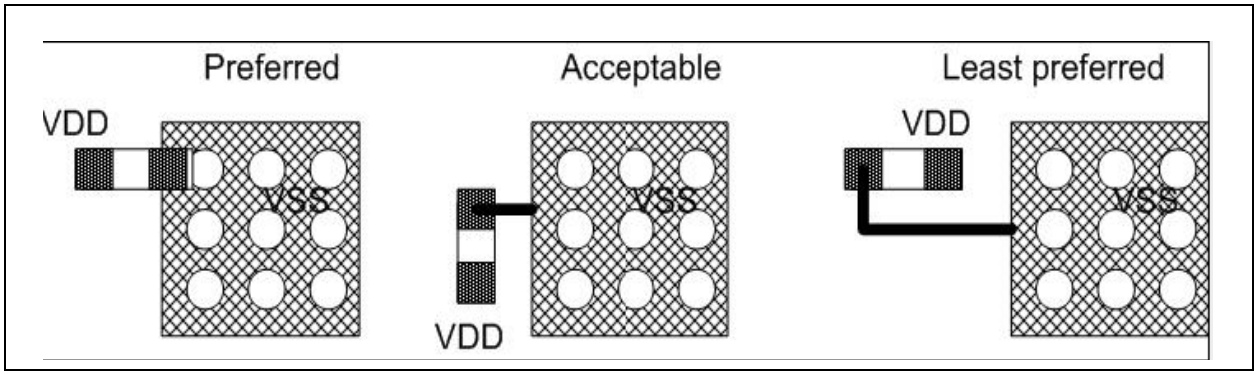

Figure 3.4 Placement of Bypass Capacitors

3.4 VIAS in Ground Flag for QFN Package

A via grid array pattern is suggested, and has been found to result in excellent signal integrity performance.

3.5 Magnetics Module

The magnetics module has a critical effect on overall IEEE and emissions conformance. The device should meet the performance required for a design with reasonable margin to allow for manufacturing variation. Occasionally, components that meet basic specifications may cause the system to fail IEEE testing because of interactions with other components or the Printed Circuit Board (PCB) itself. Carefully qualifying new magnetics modules can go a long way toward preventing this type of problem.

SMSC provides two levels of Magnetics qualification, Suggested magnetics and Qualified magnetics.

Suggested magnetics have not been tested in order to verify proper operation with the specified SMSC device. This category of magnetic has been evaluated by the contents of the vendor supplied data sheet and legacy performance only. However, the designer can assume with some degree of confidence, that with proper PCB design techniques, the combinations of SMSC devices and magnetics presented as suggested magnetics will perform to high standards.

Qualified magnetics have been tested in order to verify proper operation with the specific SMSC device listed with it. The designer can assume with a high degree of confidence, that with proper PCB design techniques, the combinations of SMSC devices and qualified magnetics will perform to the highest standards.

For more information on magnetics, please refer to the Application Note 8-13 “Suggested Magnetics”.