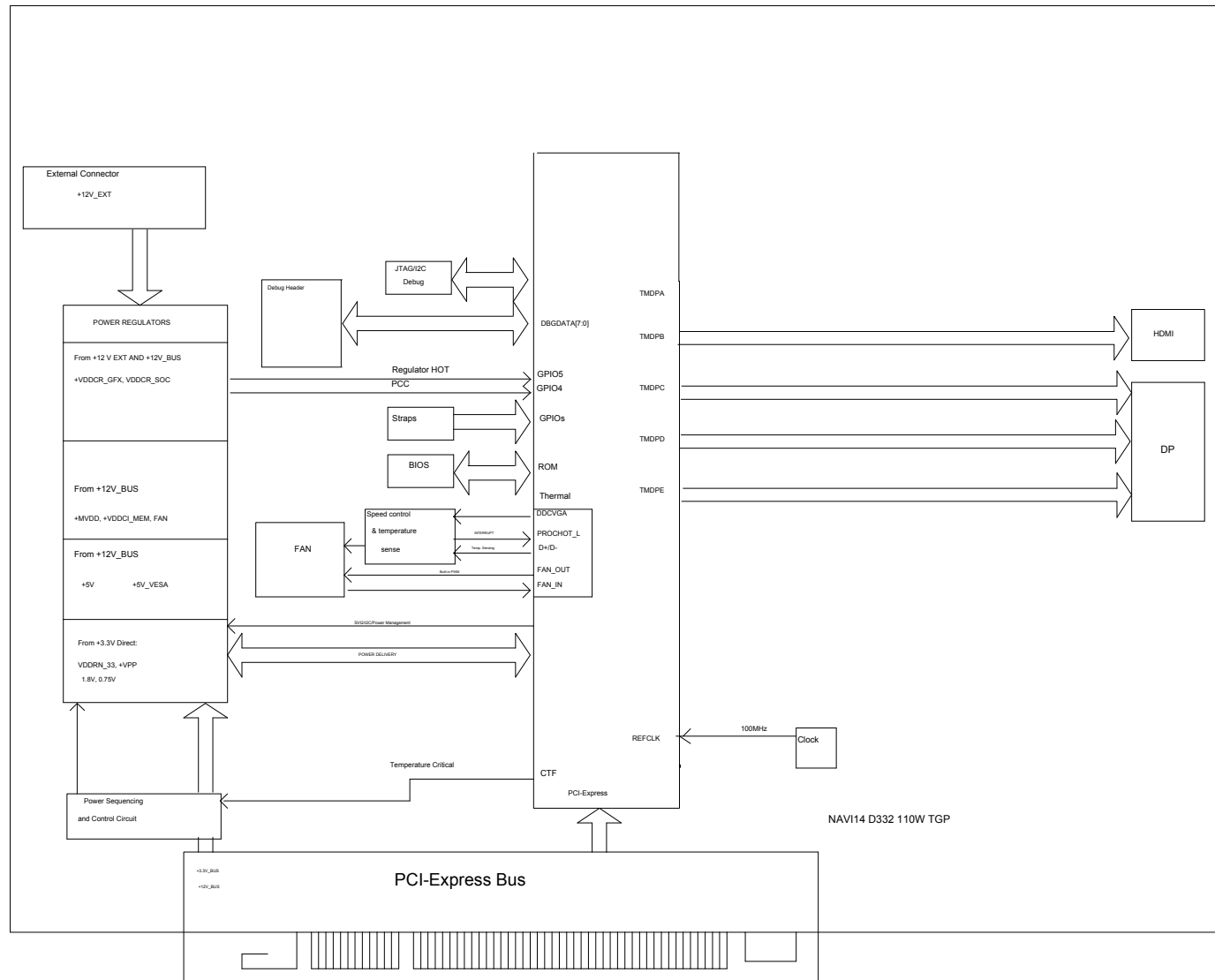


NAVI14 GDDR6 4PCS,8L 3xDPs +1xHDMI

105-D332xx-00B RevB Desktop board(110W TGP)

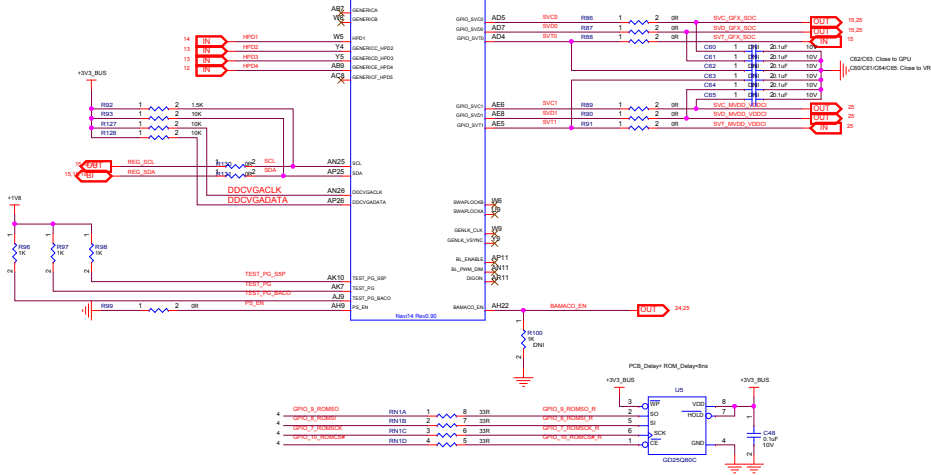
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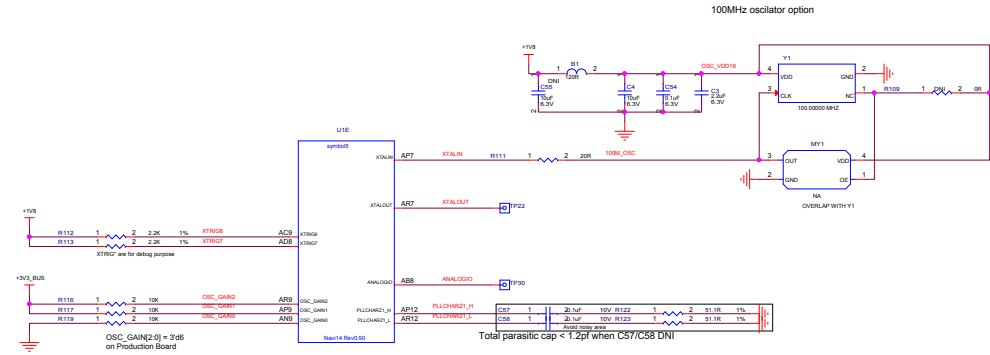


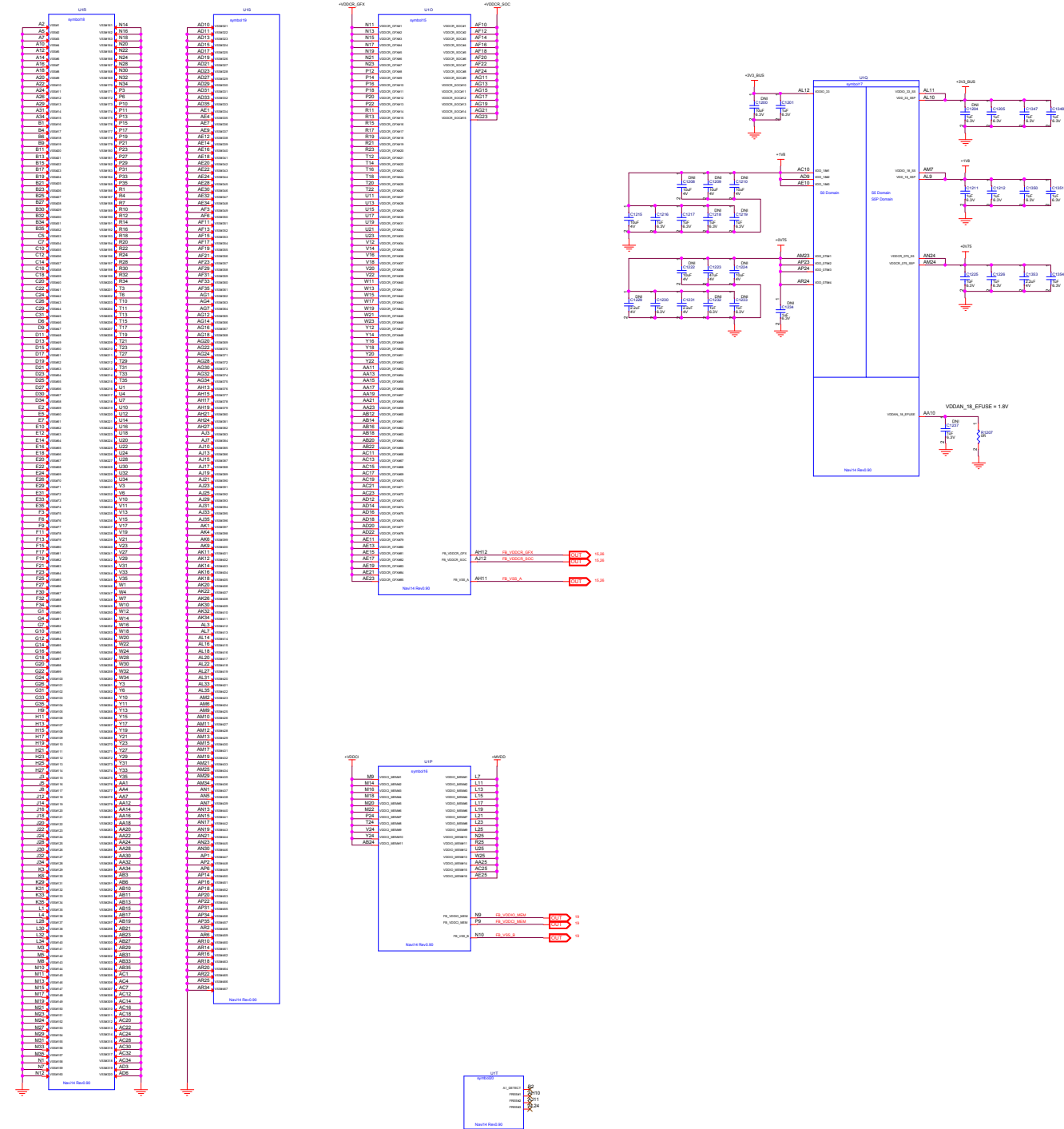
Note: Internal PULLUP at GPIO pad is ~40k strength in 14nm design spec

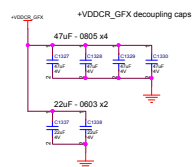
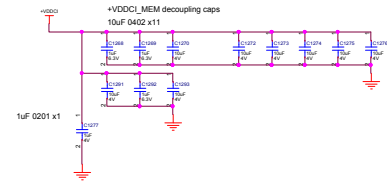
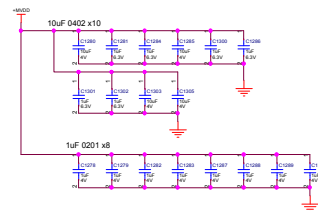
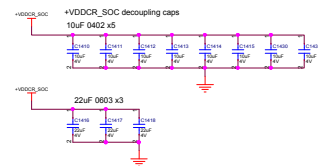
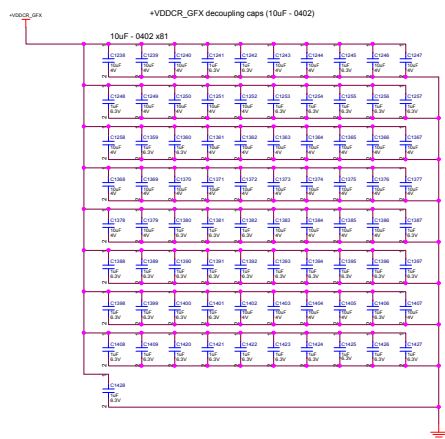
GPIO	FUNCTION	DC BUS	DEVICE
0x0	VDDOR_GFX/SDC	SCL/SDA	U501NR3S217
0x2	MVSD/VSOC	SCL/SDA	U701NCR1802
0x3	PC/Opresense	SCL/SDA	U4801CS8601
0x48	GS Temperature	DDCVGACK/DCVGAQDATA	U4000TMP102A
0x4C	EXT SENSOR	DDCVGACK/DCVGAQDATA	U4001LM96183

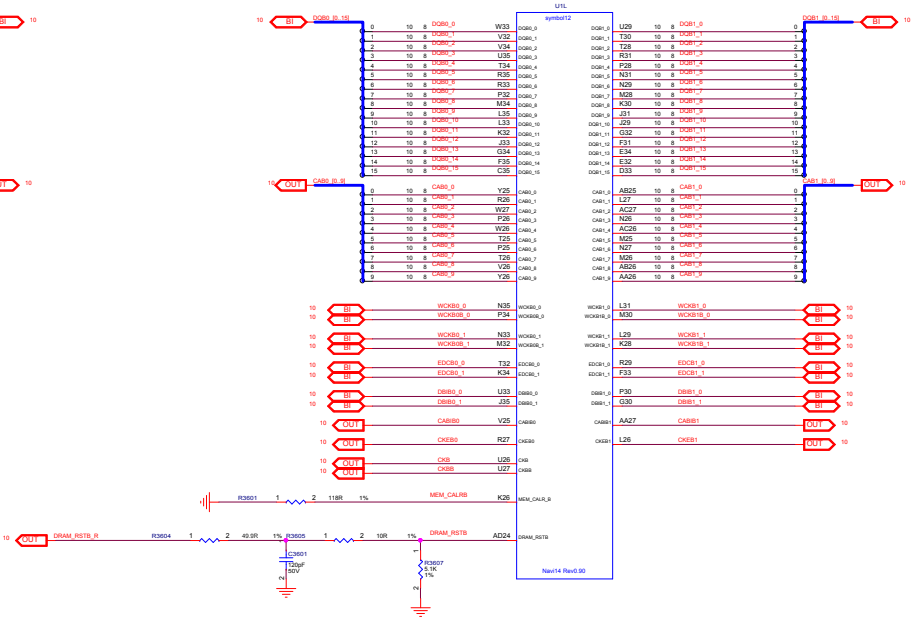
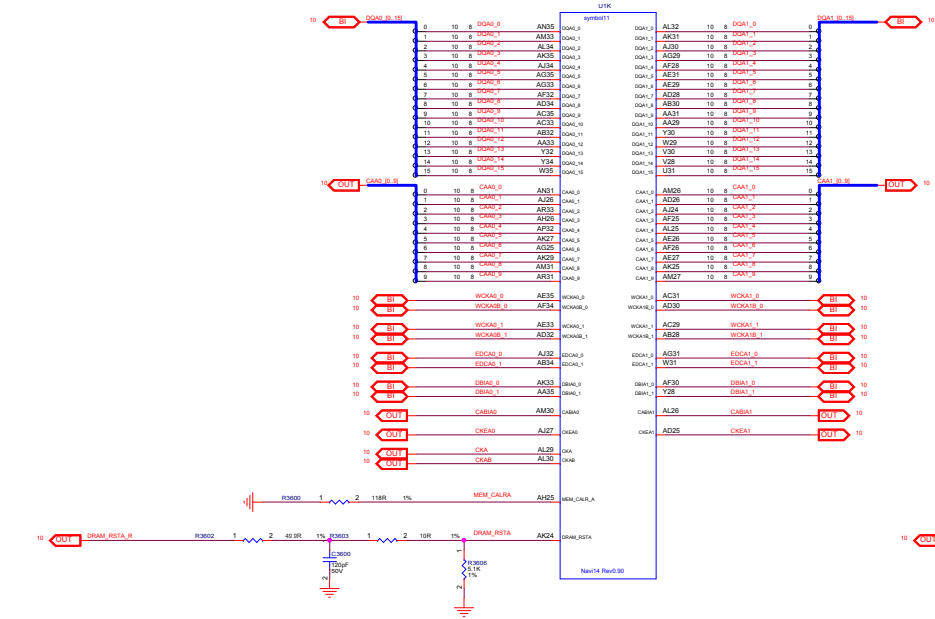


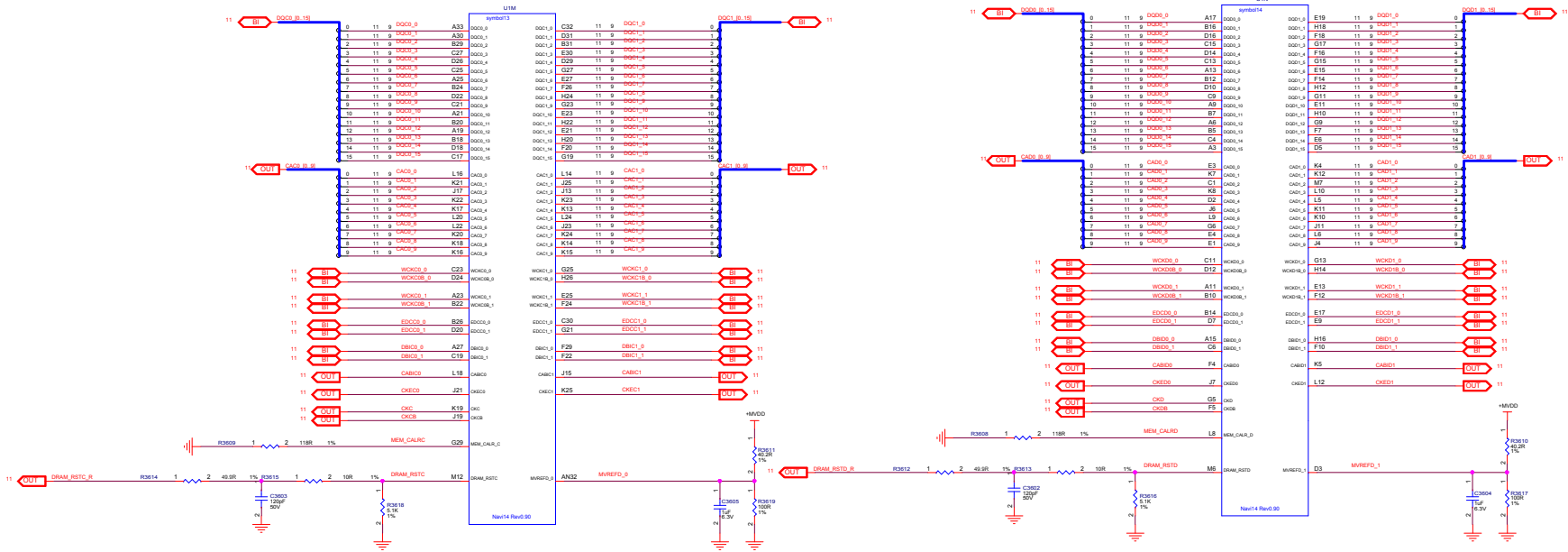
User	Internal Default Value	Definition
BIF	0	STRAP_BIF_GENA_DIS_A 0: PICH GEN4 supported 1: PICH GEN4 not supported
	0	PINSTRAP_BIF_CLK_PM_EN 0: CLKREQ power management capability is disabled 1: CLKREQ power management capability is enabled
	0	PINSTRAP_BIF_LC_TX_SWING 0: Full swing mode 1: Reduced swing mode(half swing)
	0	PINSTRAP_BIF_VGA_DIS 0: VGA controller capacity enabled 1: The device won't be recognized as the system's VGA controller
DCE	0	PINSTRAP_AUD_PORT_CONN[2:0] Number of audio-capable display outputs 0: All endpoints connected 1: 8 endpoints connected 2: 5 endpoints connected 3: 4 endpoints connected Default(PINSTRAP_AUD_PORT_CONN[2:0]) = 000
	0	PINSTRAP_AUD[1:0] 1: Audio for DisplayPort only 2: Audio for DisplayPort and HDMI if dongle is detected 3: Audio for both DisplayPort and HDMI Default(PINSTRAP_AUD[1:0]) = 11
	0	PINSTRAP_FIG[1:0] - No definition on NV
	0	PINSTRAP_MVDD_FB_DIVIDER_CONFIG 0: Divider does not exist 1: Divider exists
Platform	0	PINSTRAP_BFI_MEM_AP_SIZE[2:0] Or PINSTRAP_ROM_CONFIG[2:0] 100: 512KBIT (BT) M20P05A 101: 1MBIT (BT) M20P10A 102: 32MBIT (BT) M20P10A 103: 48MBIT (BT) M20P10A 104: 32MBIT (BT) M20P10A 105: 512KBIT (CHANGES) PM20LV12 106: 1MBIT (CHANGES) PM20LV10 Default(PINSTRAP_BFI_MEM_AP_SIZE[2:0] Or PINSTRAP_ROM_CONFIG[2:0]) = 101
	0	PINSTRAP_SMBUS_ADDR 0: 0x41h 1: 0x40h
	1	PINSTRAP_BIOS_ROM_EN 0: Disable the external BIOS ROM device 1: Enable the external BIOS ROM device
	0	GPIO_0

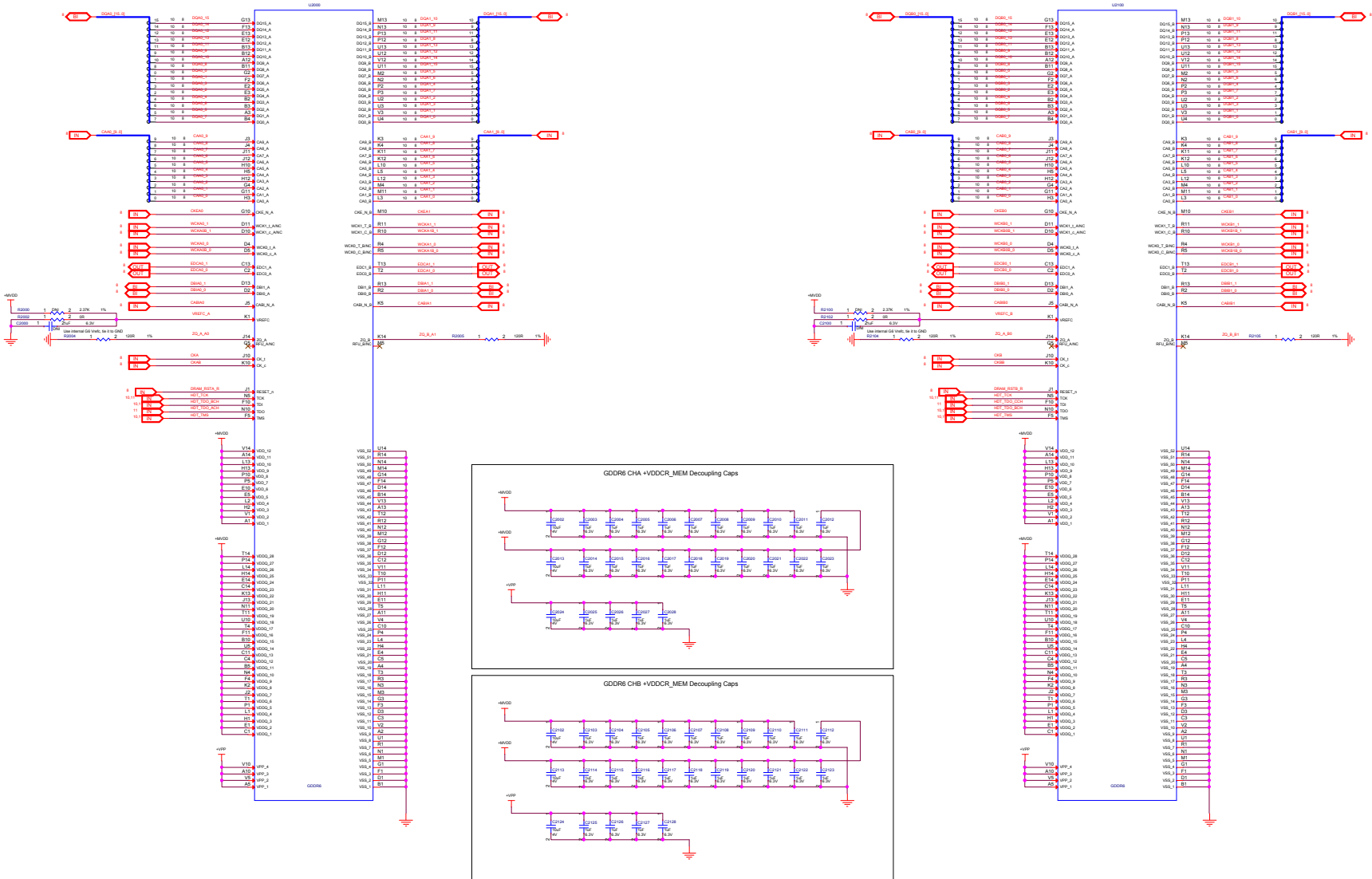


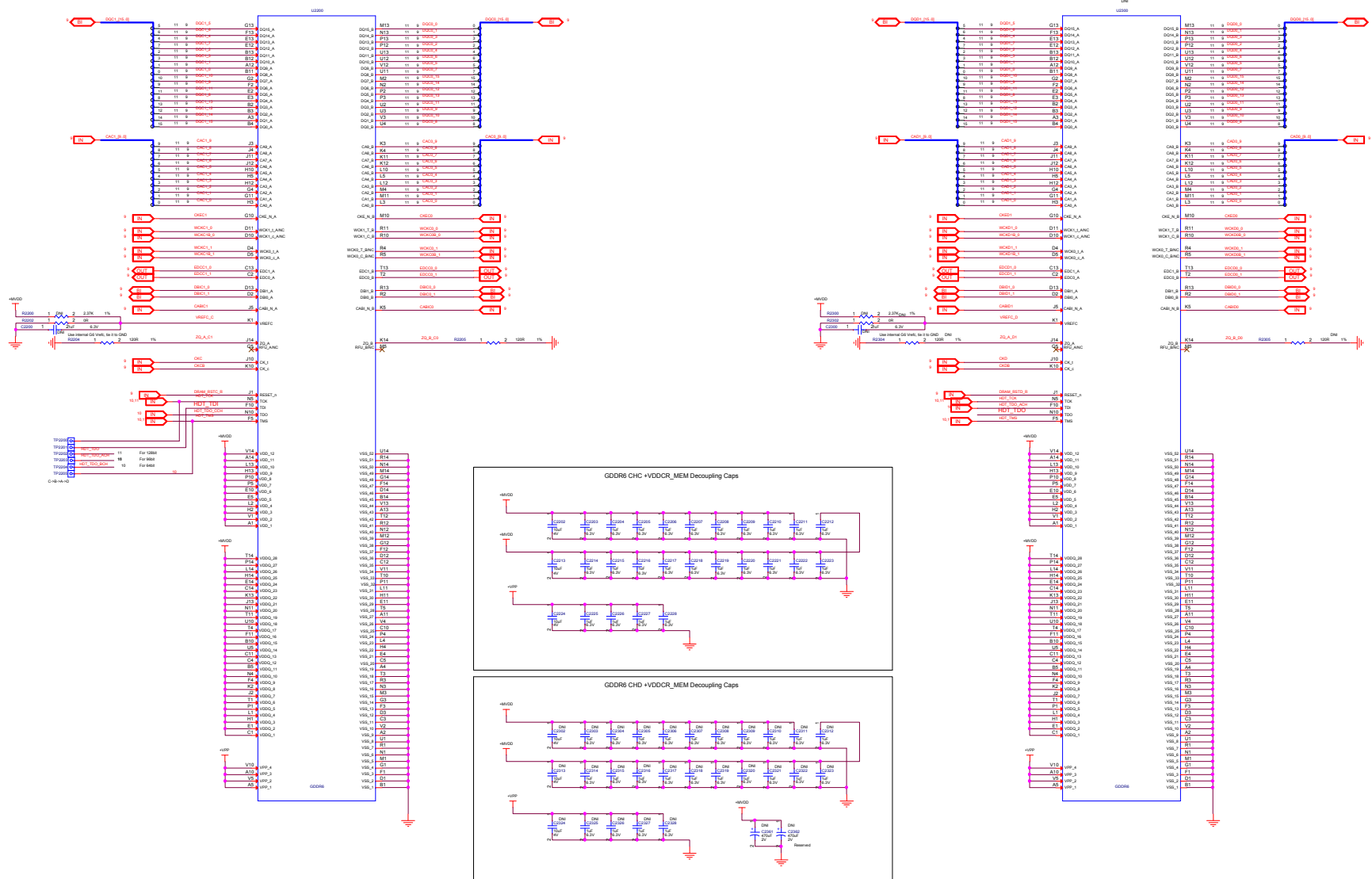




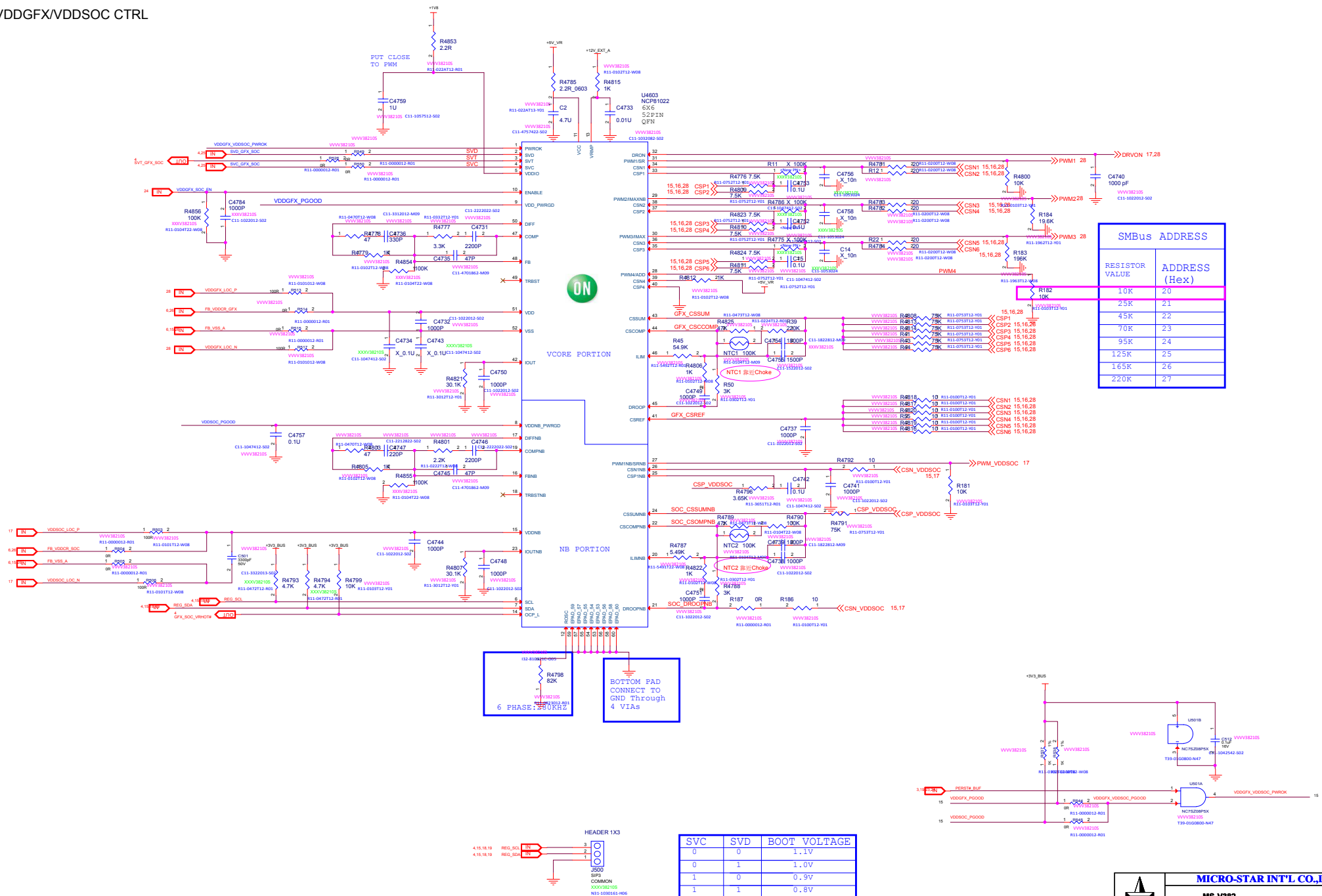


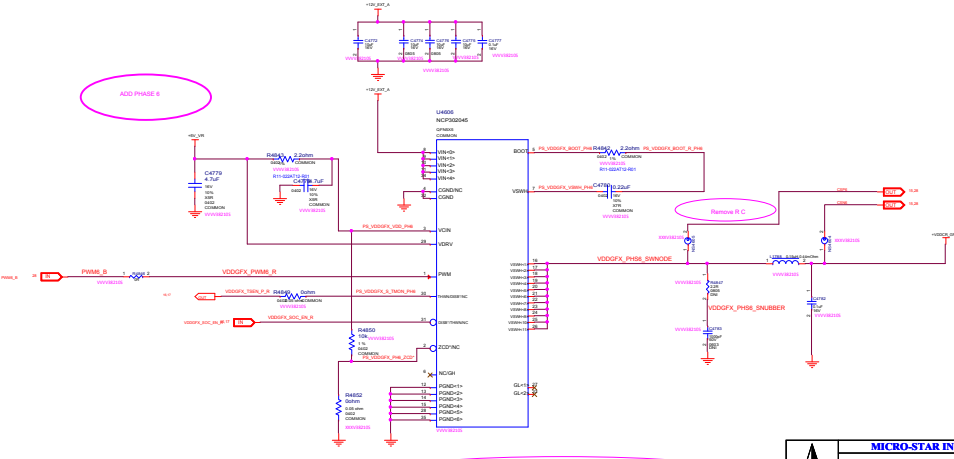
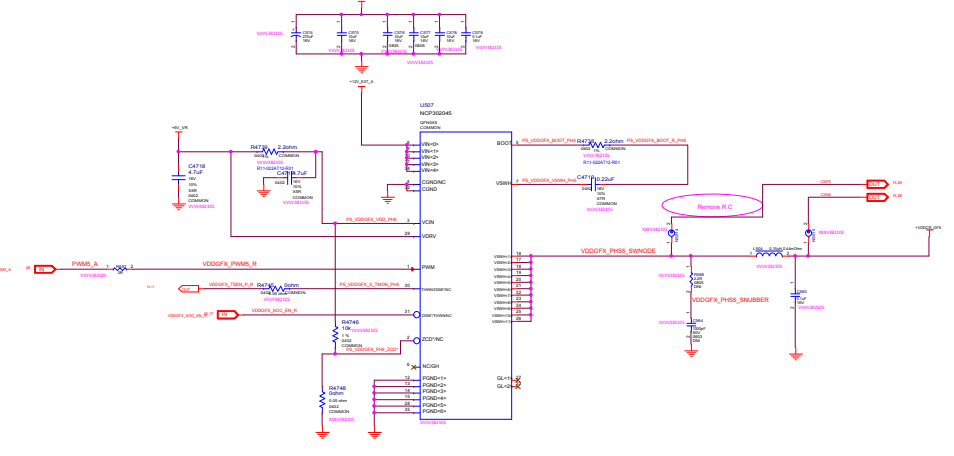
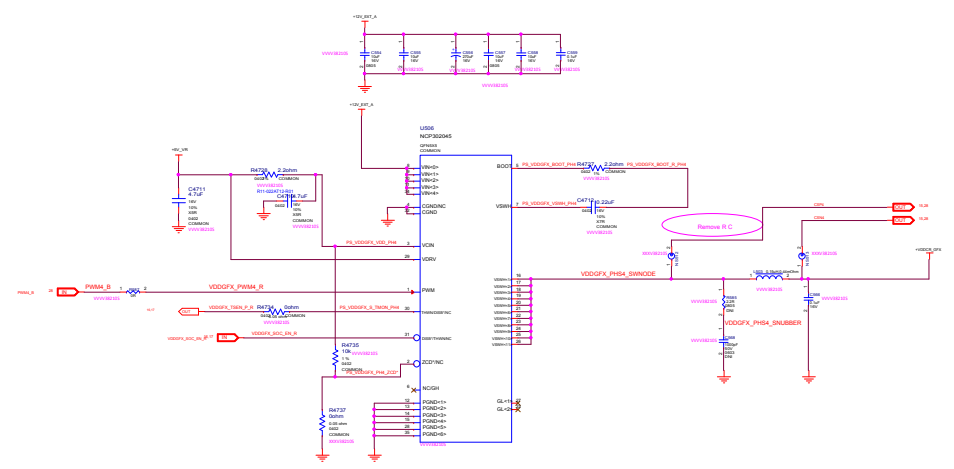
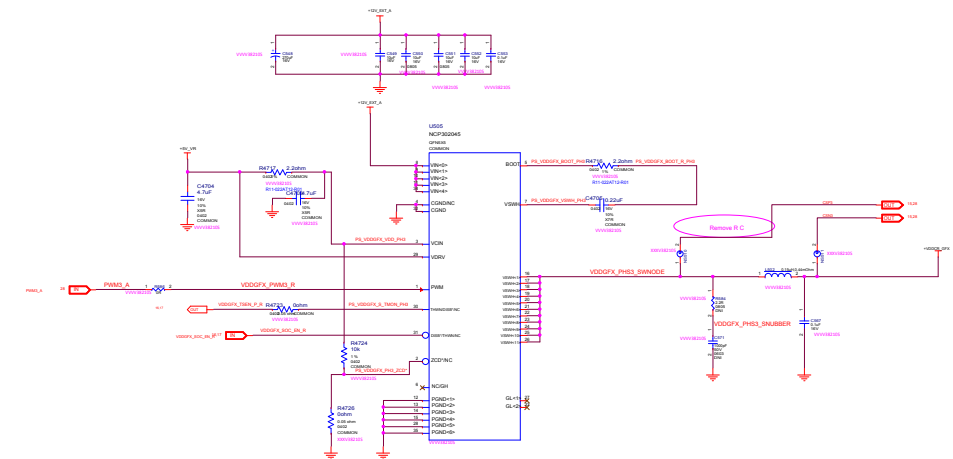
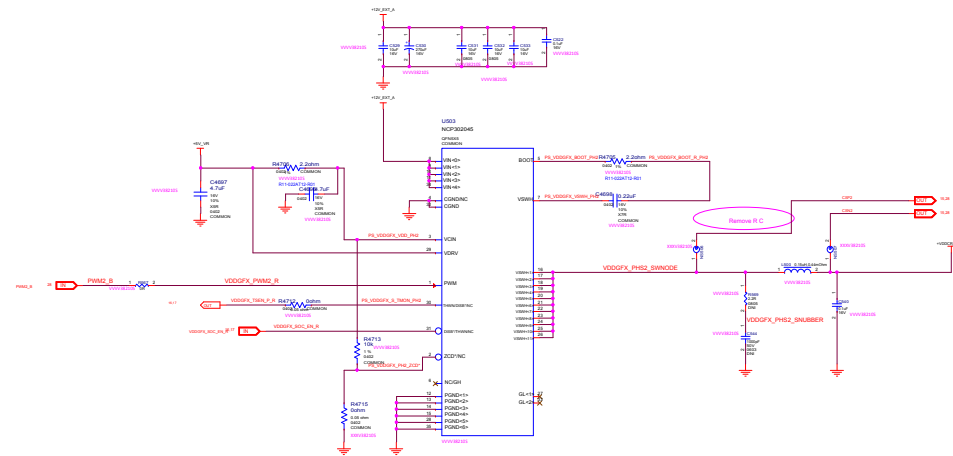
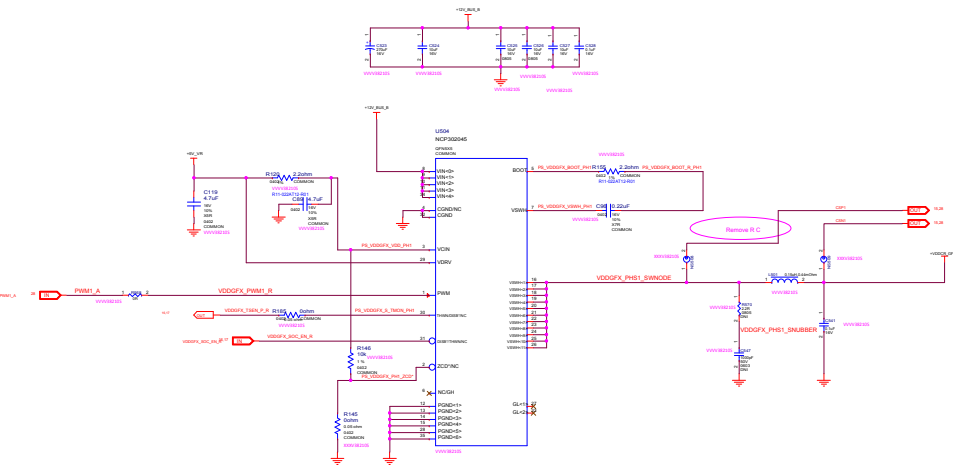


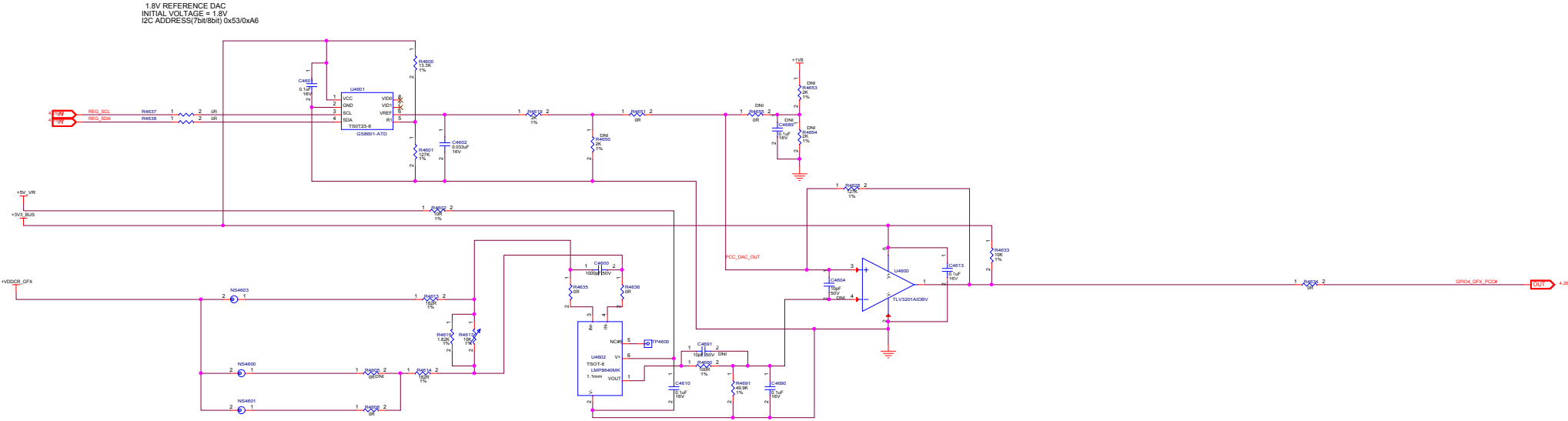


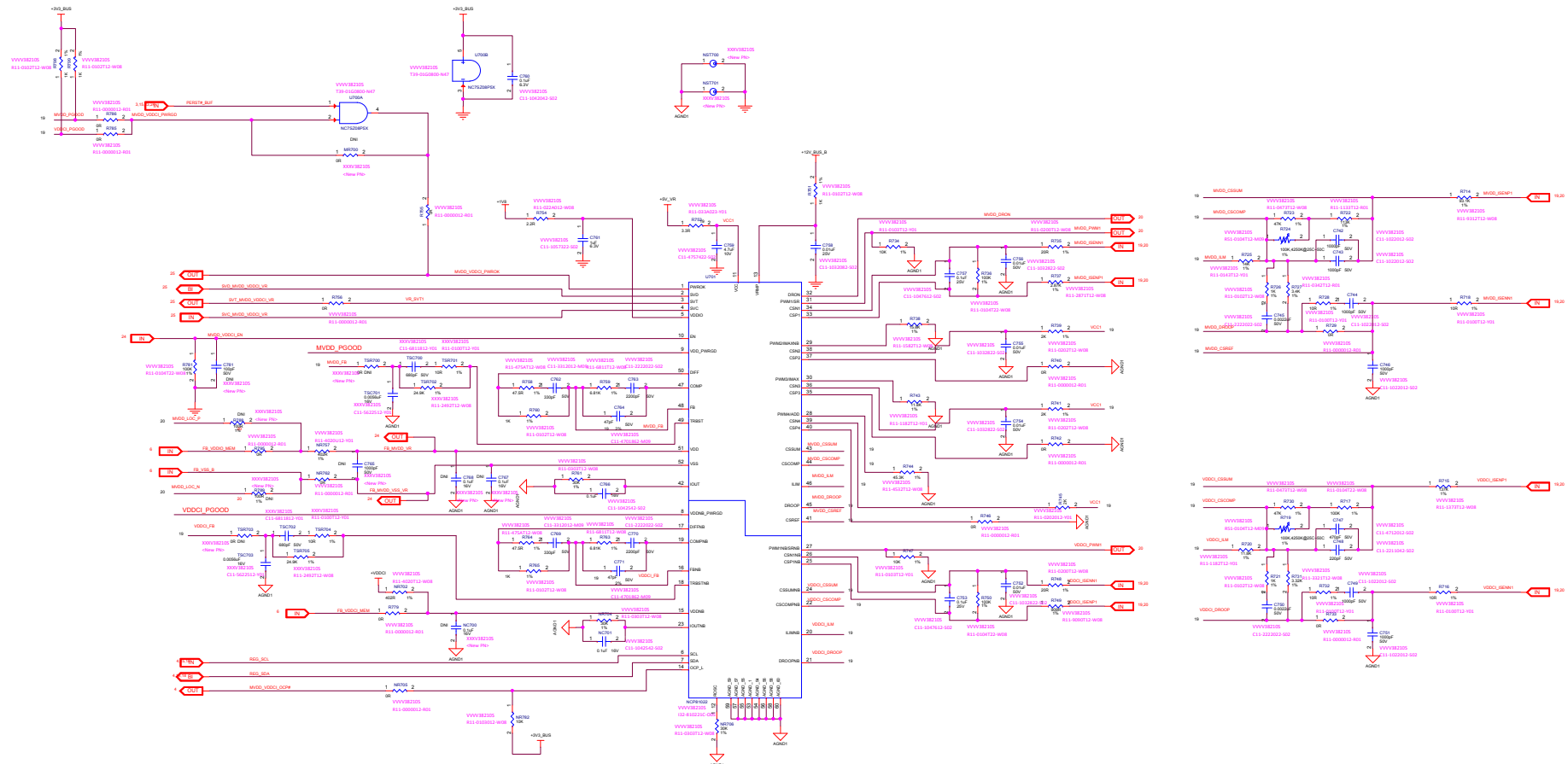


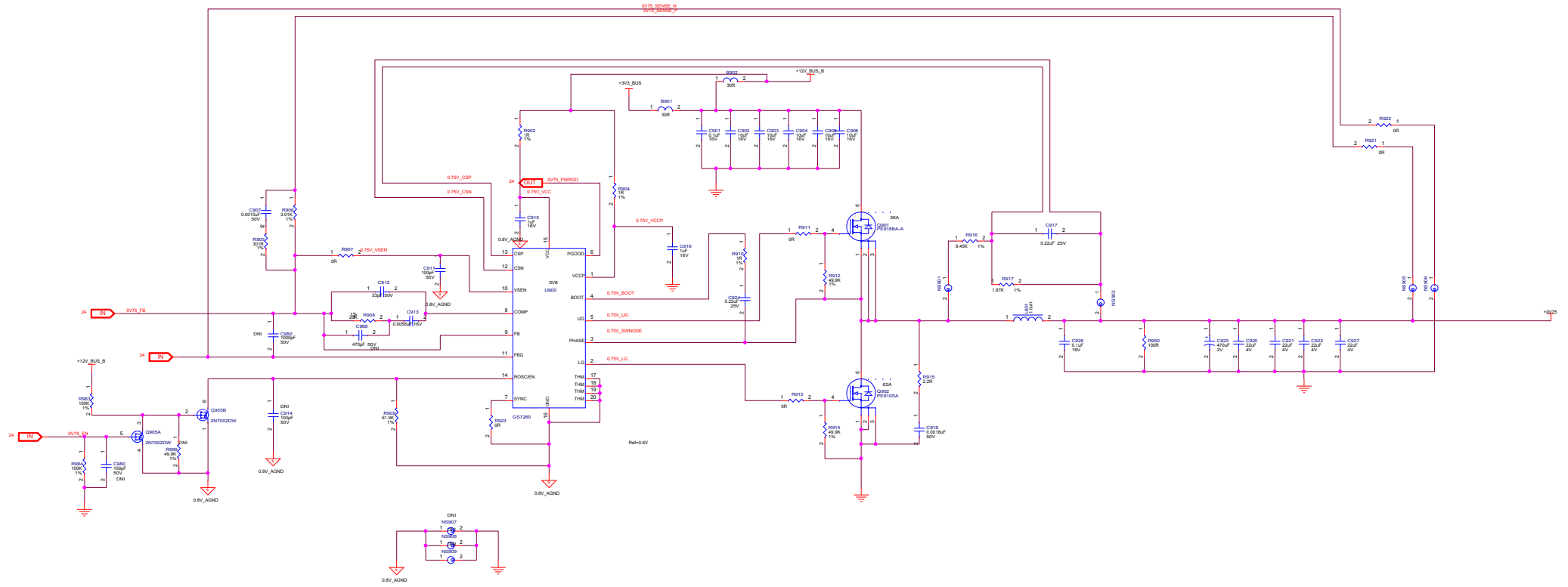
REG - VDDGFX/VDDSOC CTRL



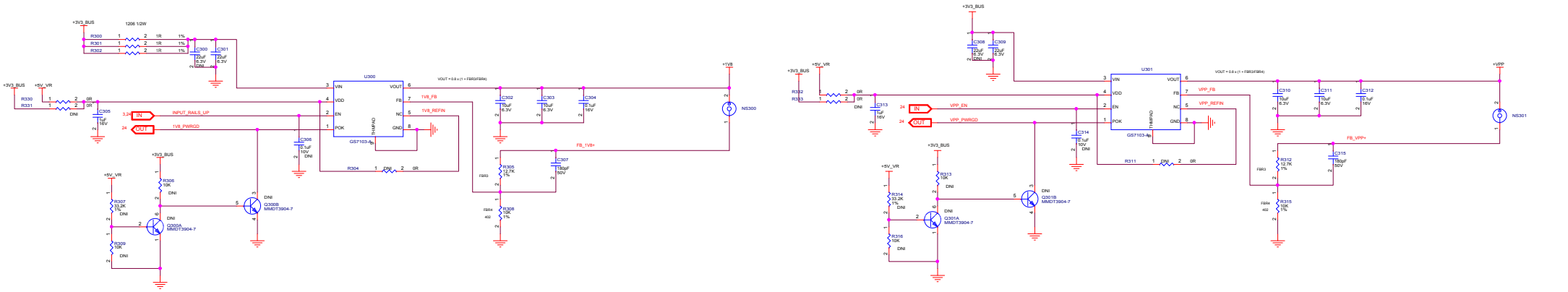


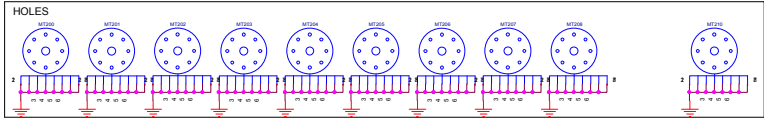
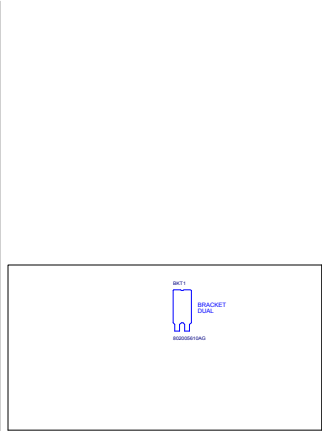
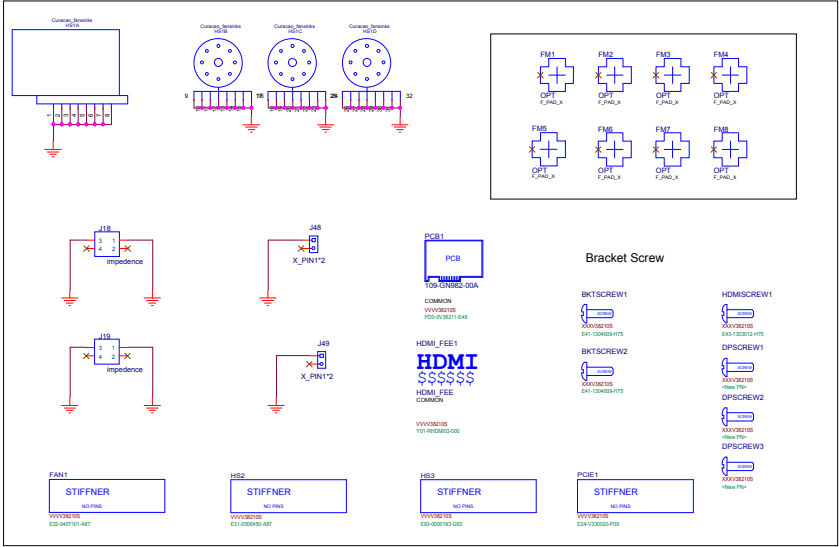
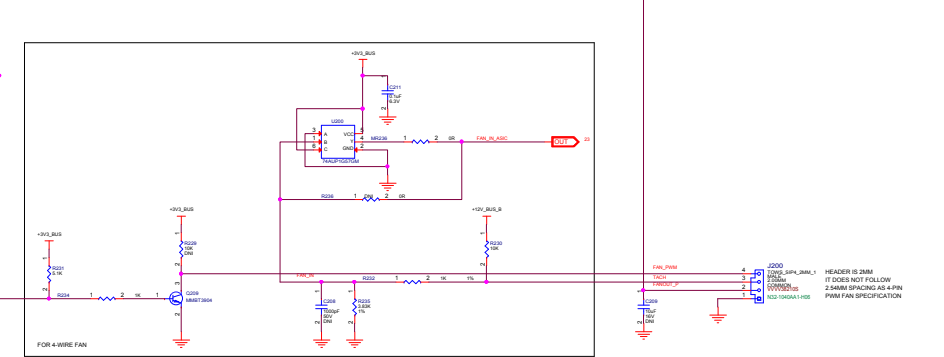
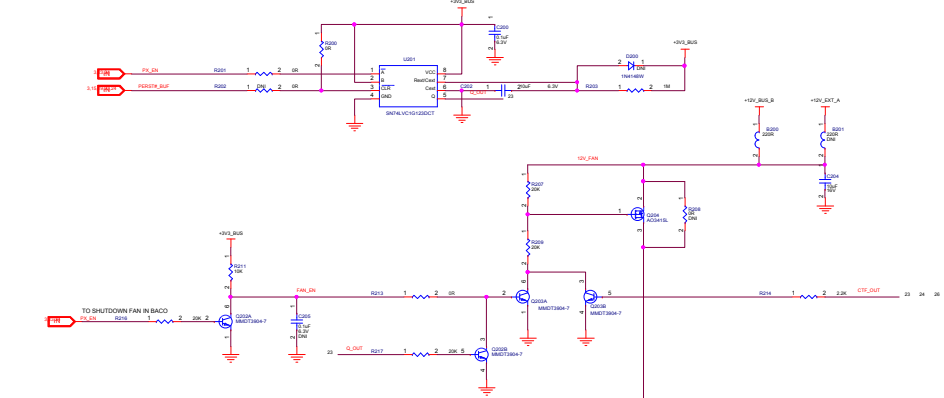
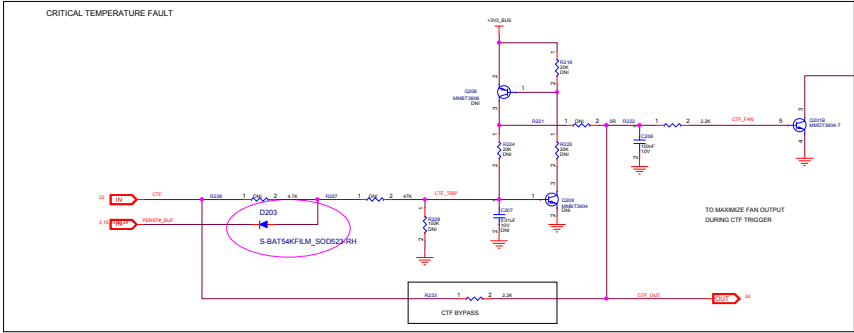
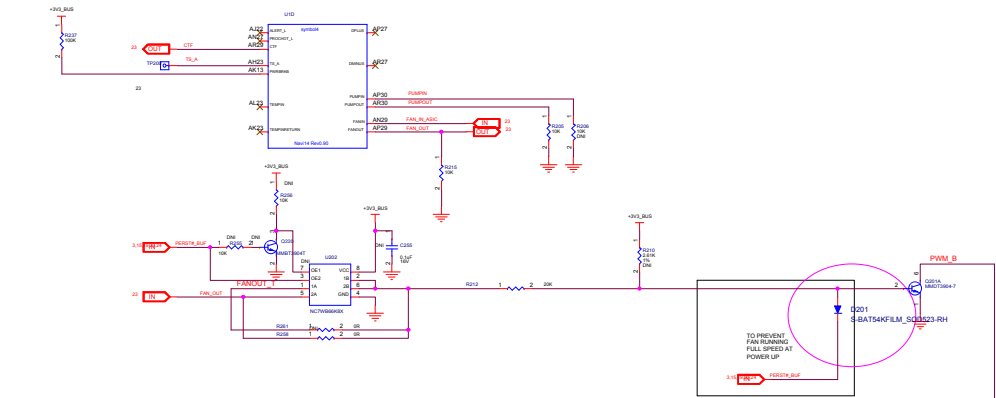


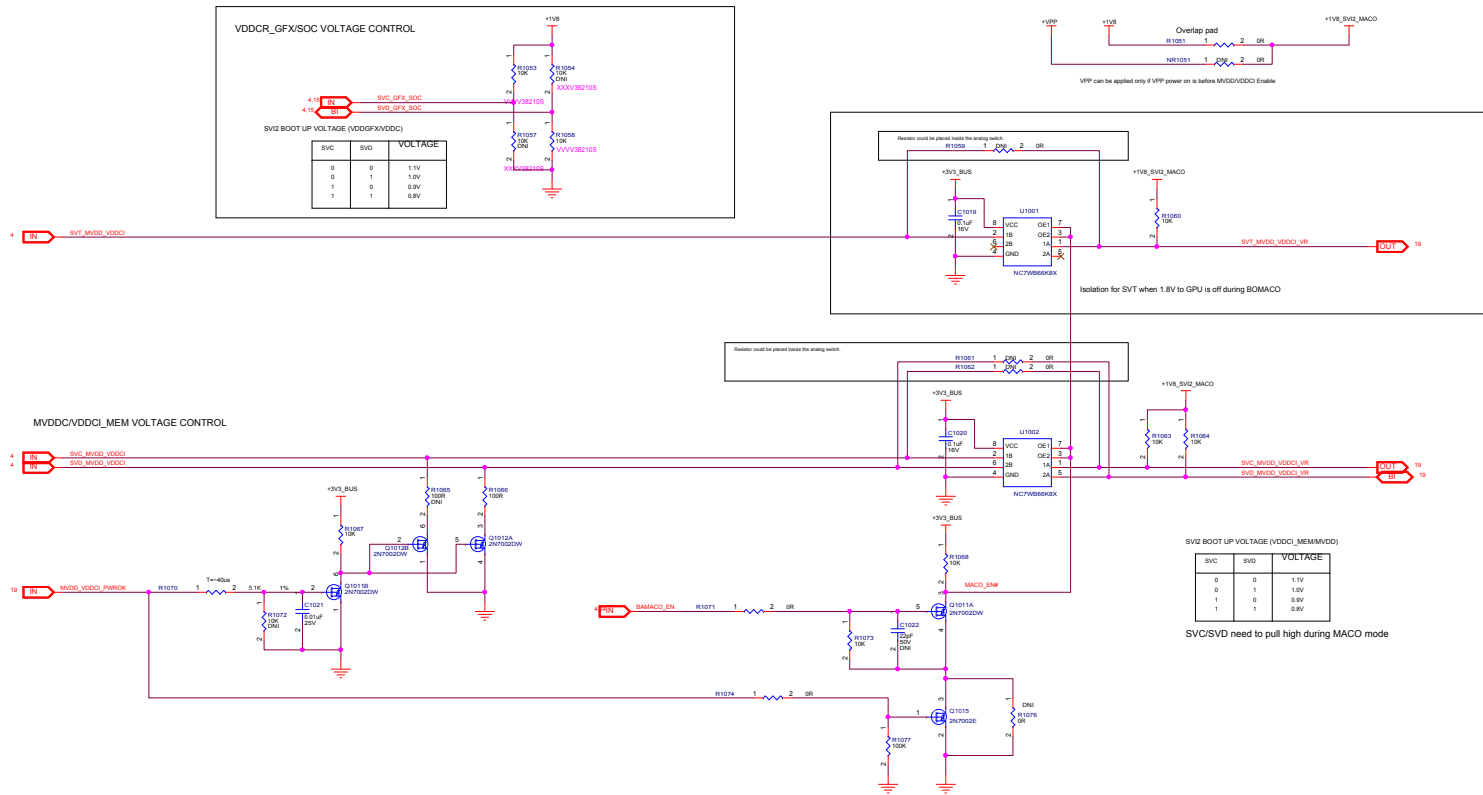




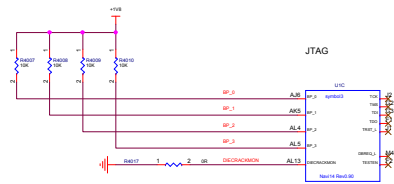
LDO - 1V8/VPP/5V







29) DEBUG CIRCUIT



REVISION HISTORY

1.00	00A	08/09/2018	Initial schematic
1.00	00B	12/28/2018	change all 4172010501G parts to 4172010500G
		04/16/2019	ADD D1152 D1162 D1162 D1162 ADD R1152 AND CHANGE R1152 LOCAL SENSE POINT ADD R1162 R1162 R1162 R1162 and reassign gfa phase1-3 input source ADD R4653 R4654 R4655 C4655 Change T01: 0.53uV520118000G R749: 800R318000000G NR104: 30K3180300200G R743: 18K3180180200G C747:470pF/4170047100G C748:220pF/4
			170522100G

2019/11/18 .V382 1 0 - V382 1 1 ChangeyddGEXVddSSOCPWMIR33217 .\ONZUR81022Z

ADD P.28

