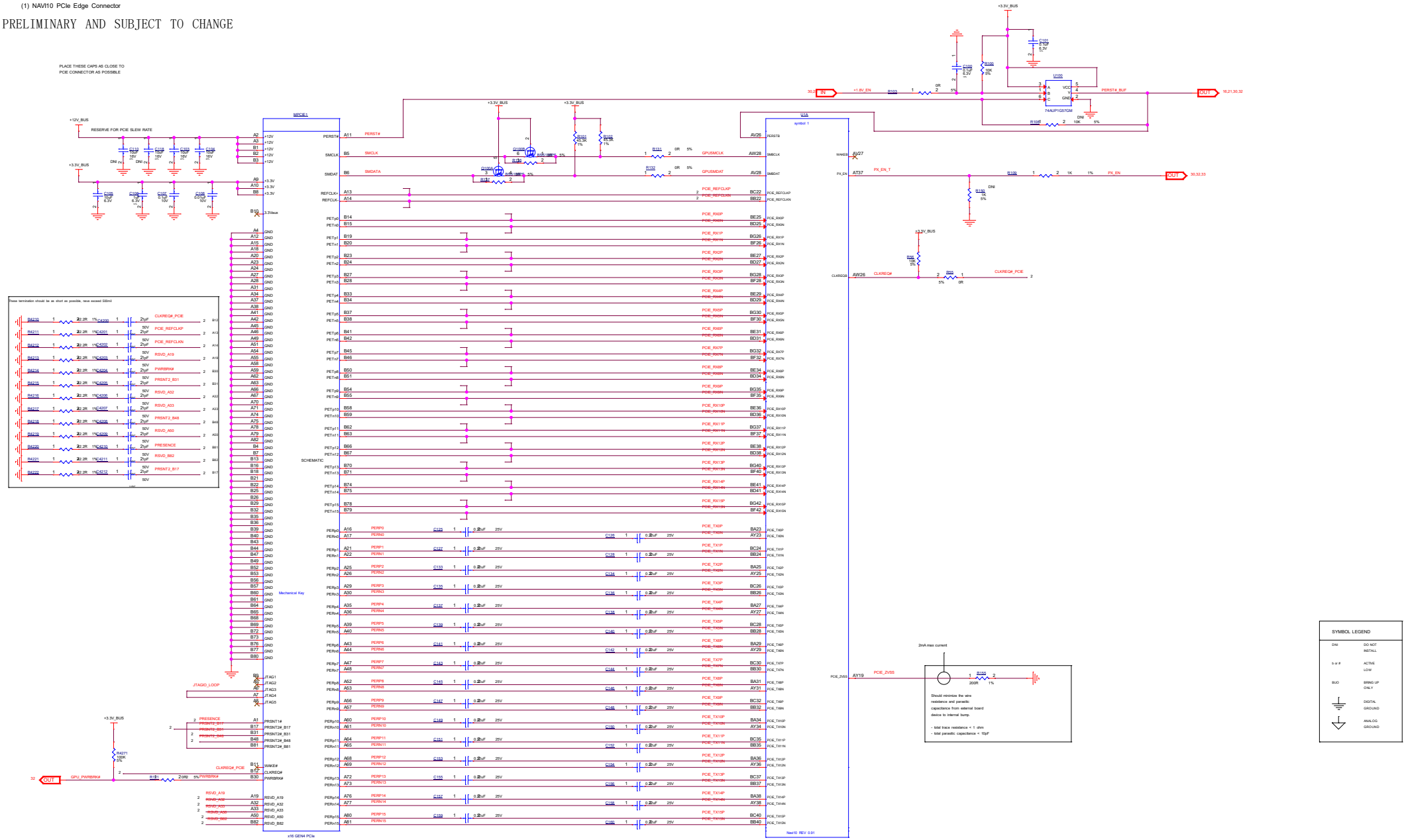
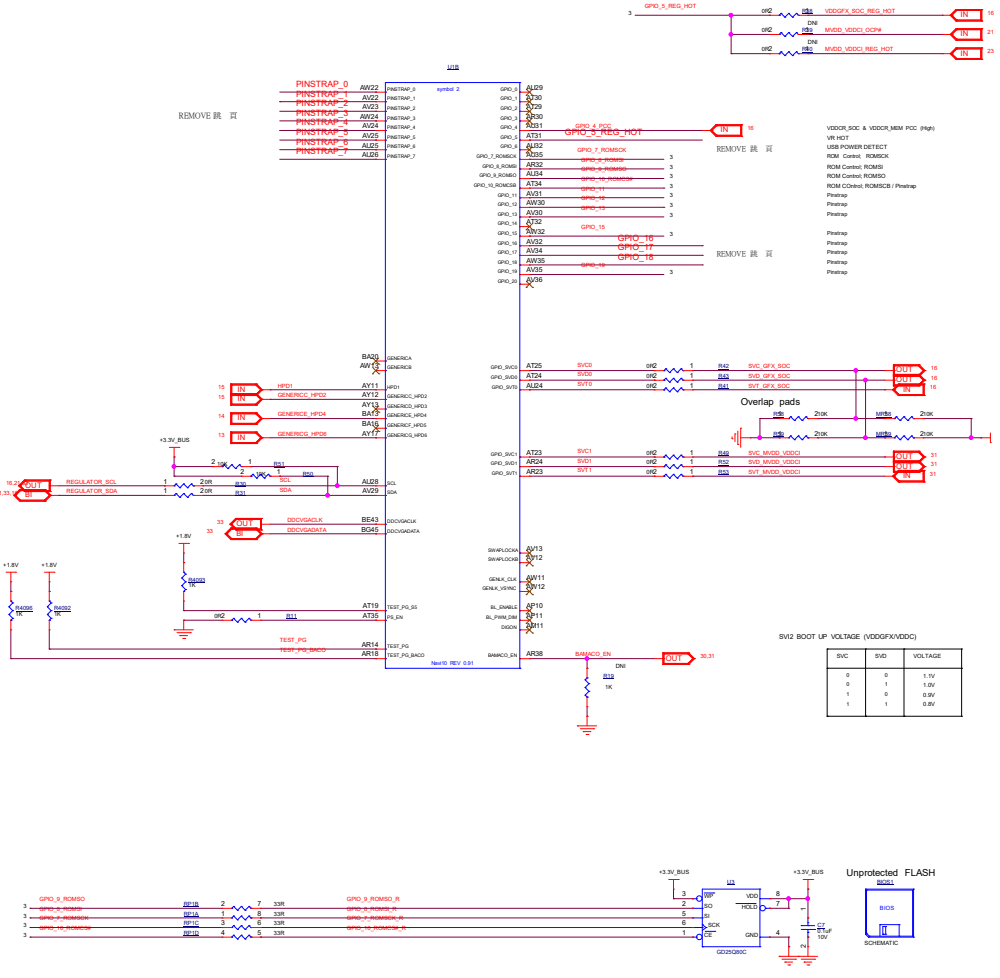
(1) NAVI10 PCIe Edge Connector

PRELIMINARY AND SUBJECT TO CHANGE

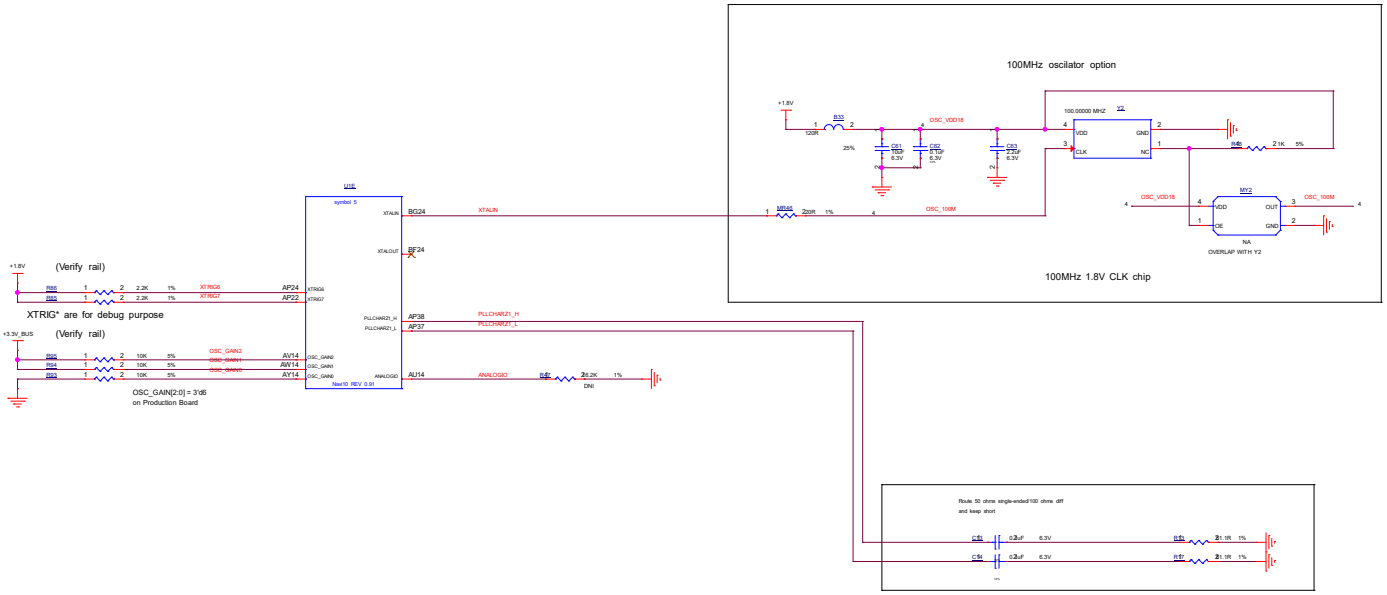




Note: Internal PU/PD at GPIO pad is ~40k
strength in 14nm design spec

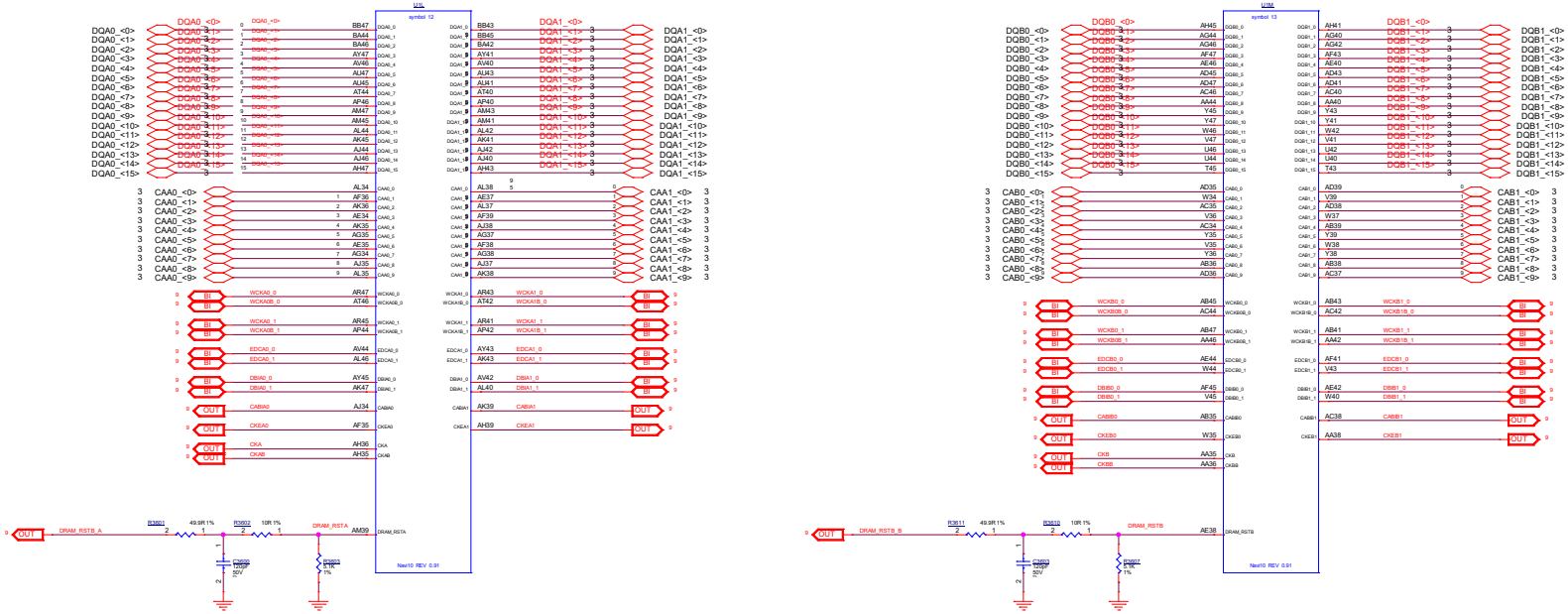
User	Internal Default Value	Definition
BIF	0	STRAP_BIF_GEN4_DIS_A 0: PCIe GEN 4 supported 1: PCIe GEN 4 not supported
	0	PINSTRAP_BIF_CLK_PM_EN 0: CLKREQ# power management capability is disabled 1: CLKREQ# power management capability is enabled
	0	PINSTRAP_BIF_LC_TX_SWING
	0	PINSTRAP_BIF_VGA_DIS 0: VGA controller capacity enabled 1: The device won't be recognised as the system's VGA controller
DCE	0 0 0	PINSTRAP_AUD_PORT_CONN[2:0] Number of audio-capable display outputs 0: All endpoints connected 1: 6 endpoints connected 2: 5 endpoints connected 3: 4 endpoints connected 4: 3 endpoints connected 5: 2 endpoints connected 6: 1 endpoint connected 7: 0 endpoints connected
	0 0	PINSTRAP_AUD[1:0] 1: Audio for DisplayPort only 2: Audio for DisplayPort and HDMI if dongle is detected 3: Audio for DisplayPort and native HDMI
Platform	0 0 0	
SMU	1 0 1	
		PINSTRAP_SMBUS_ADDR 0: 0x61h 1: 0x62h
	1	PINSTRAP_BIOS_ROM_EN 0: Disable the external BIOS ROM device 1: Enable the external BIOS ROM device

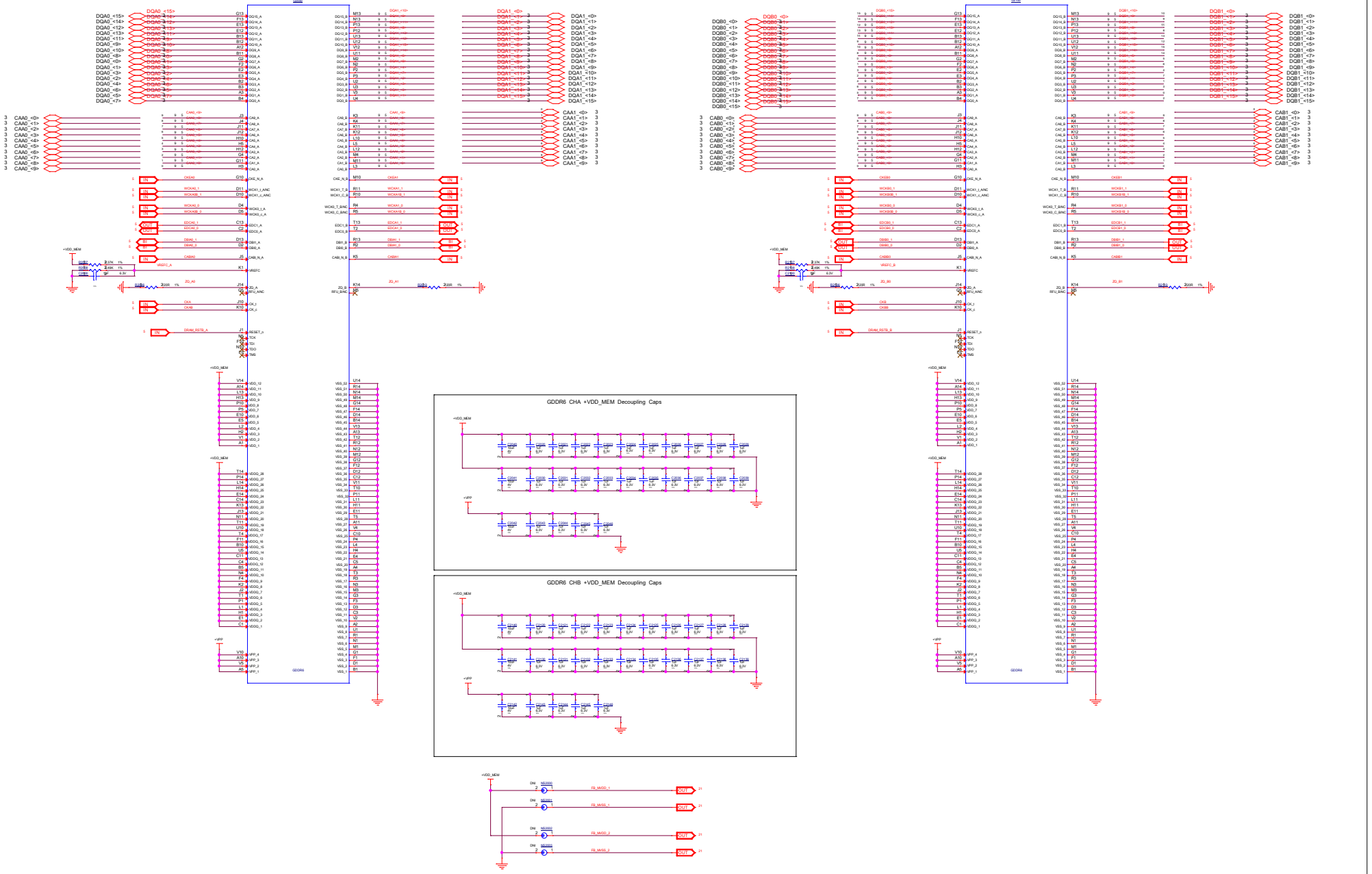
PRELIMINARY AND SUBJECT TO CHANGE



NAVI 10 MEM INTERFACE CH A/B

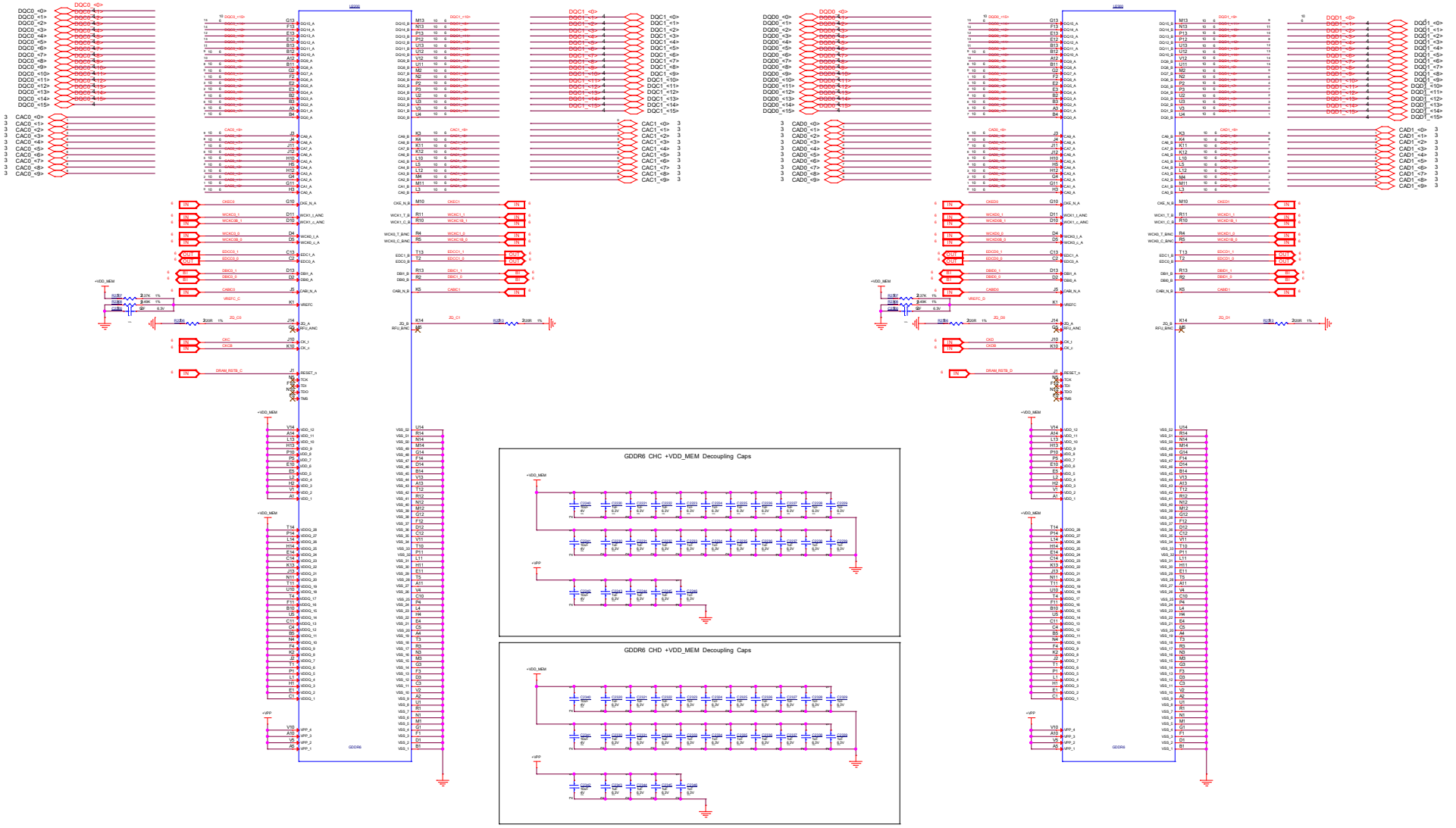
PRELIMINARY AND SUBJECT TO CHANGE




GDDR6 CHA +VDD_MEM Decoupling Caps
GDDR6 CHB +VDD_MEM Decoupling Caps

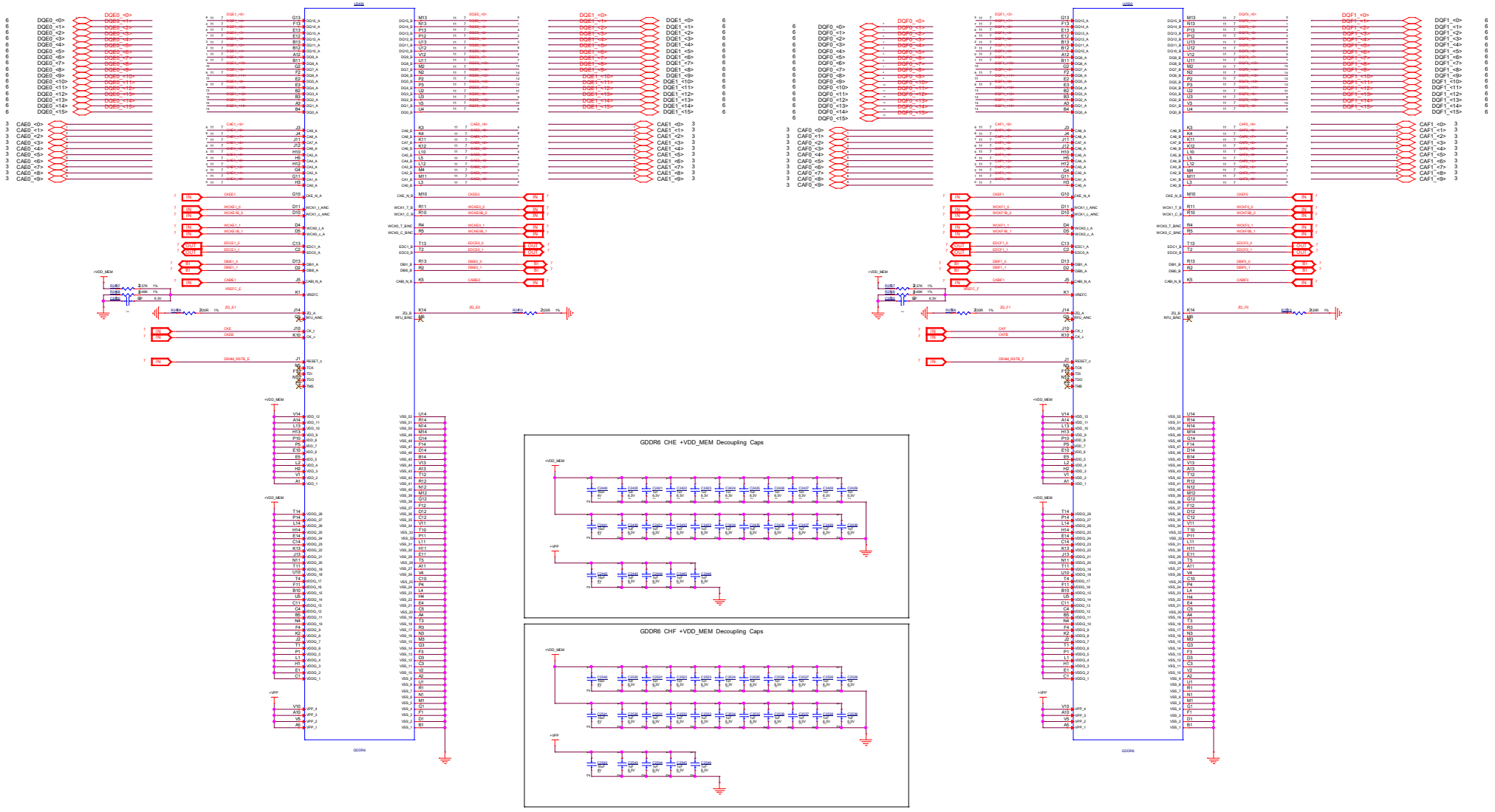
GDDR6x16 CHCD Memory

PRELIMINARY AND SUBJECT TO CHANGE



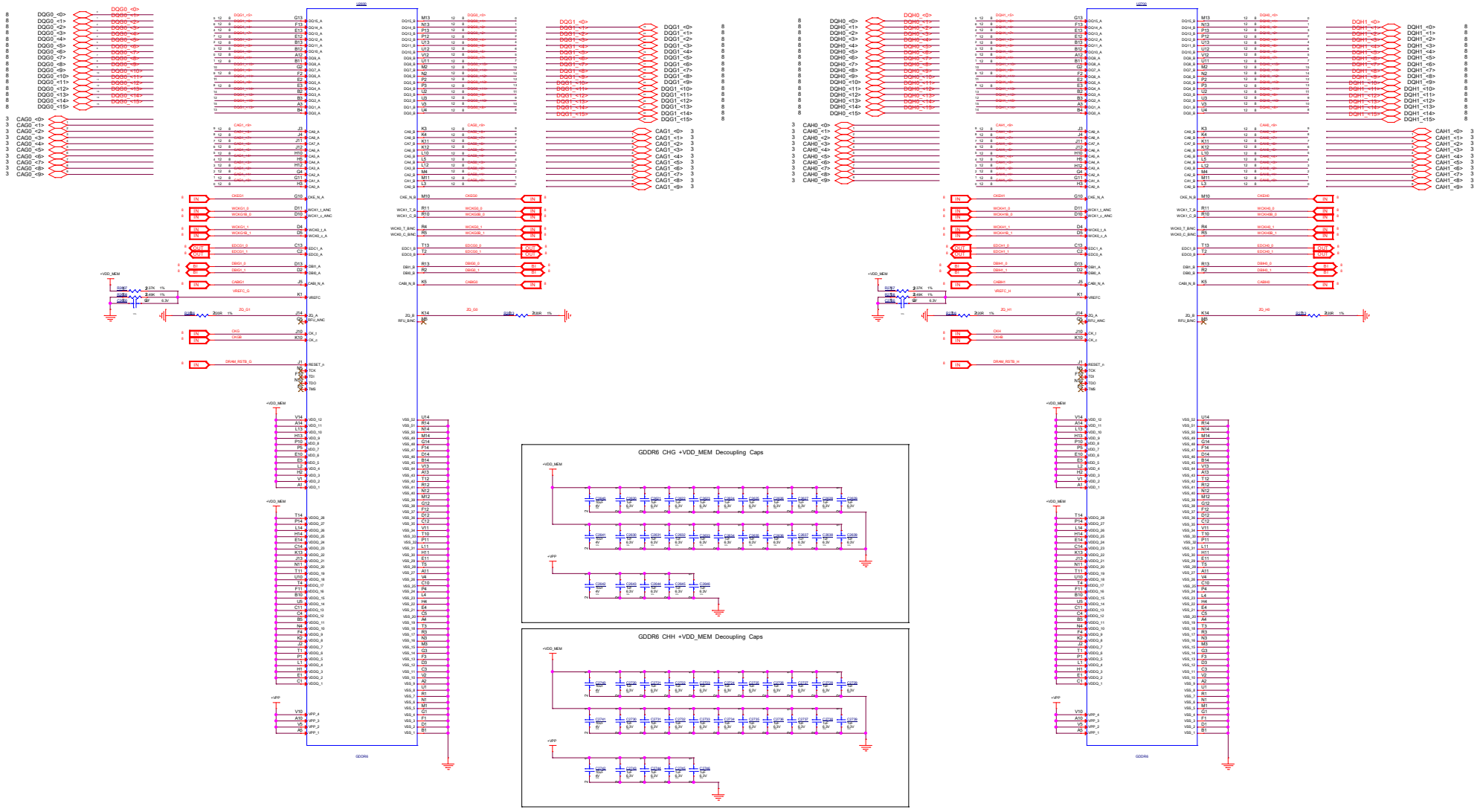
GDDR6x16 CHEF Memory

PRELIMINARY AND SUBJECT TO CHANGE



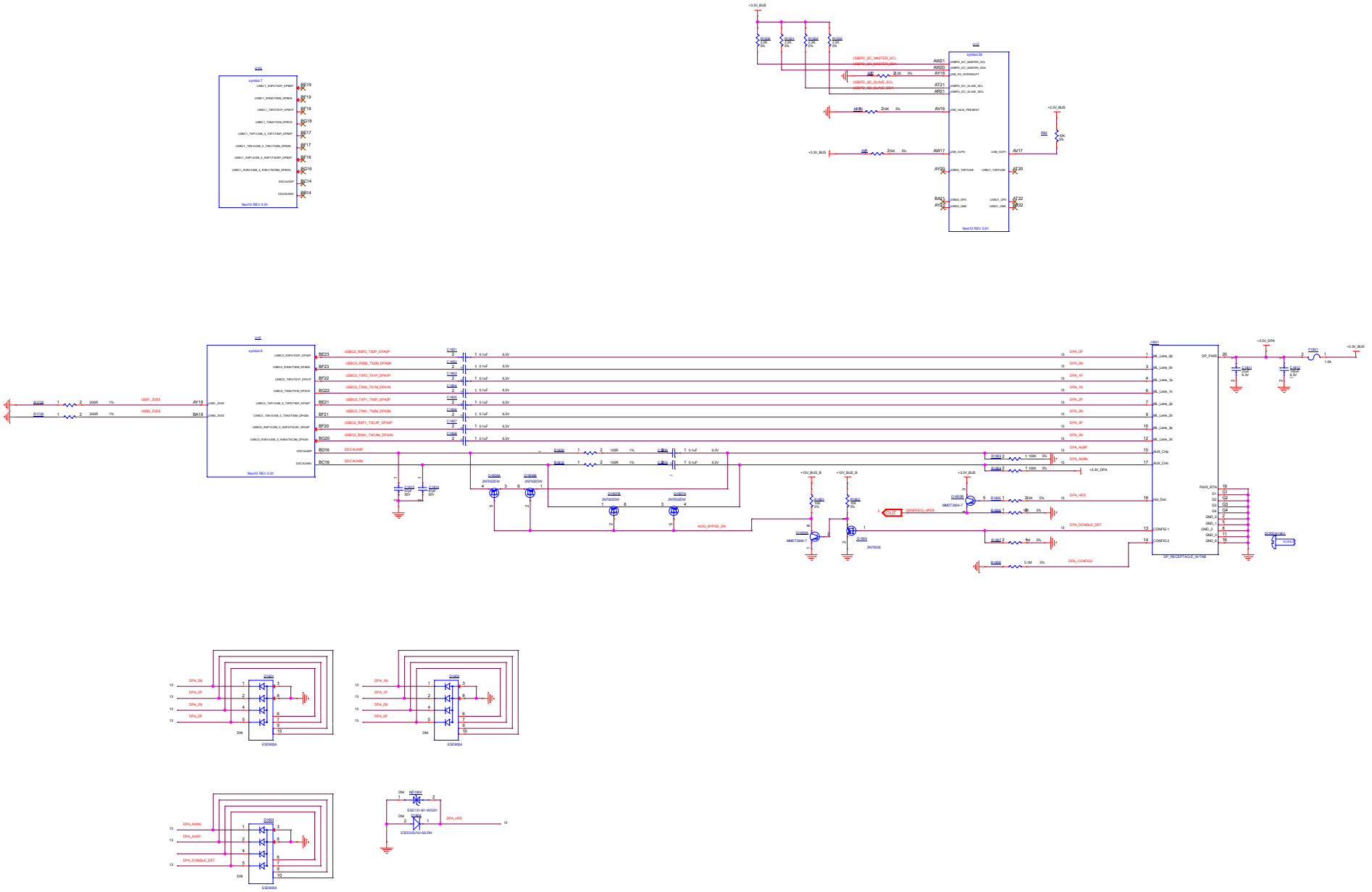
GDDR6x16 CHGH Memory

PRELIMINARY AND SUBJECT TO CHANGE

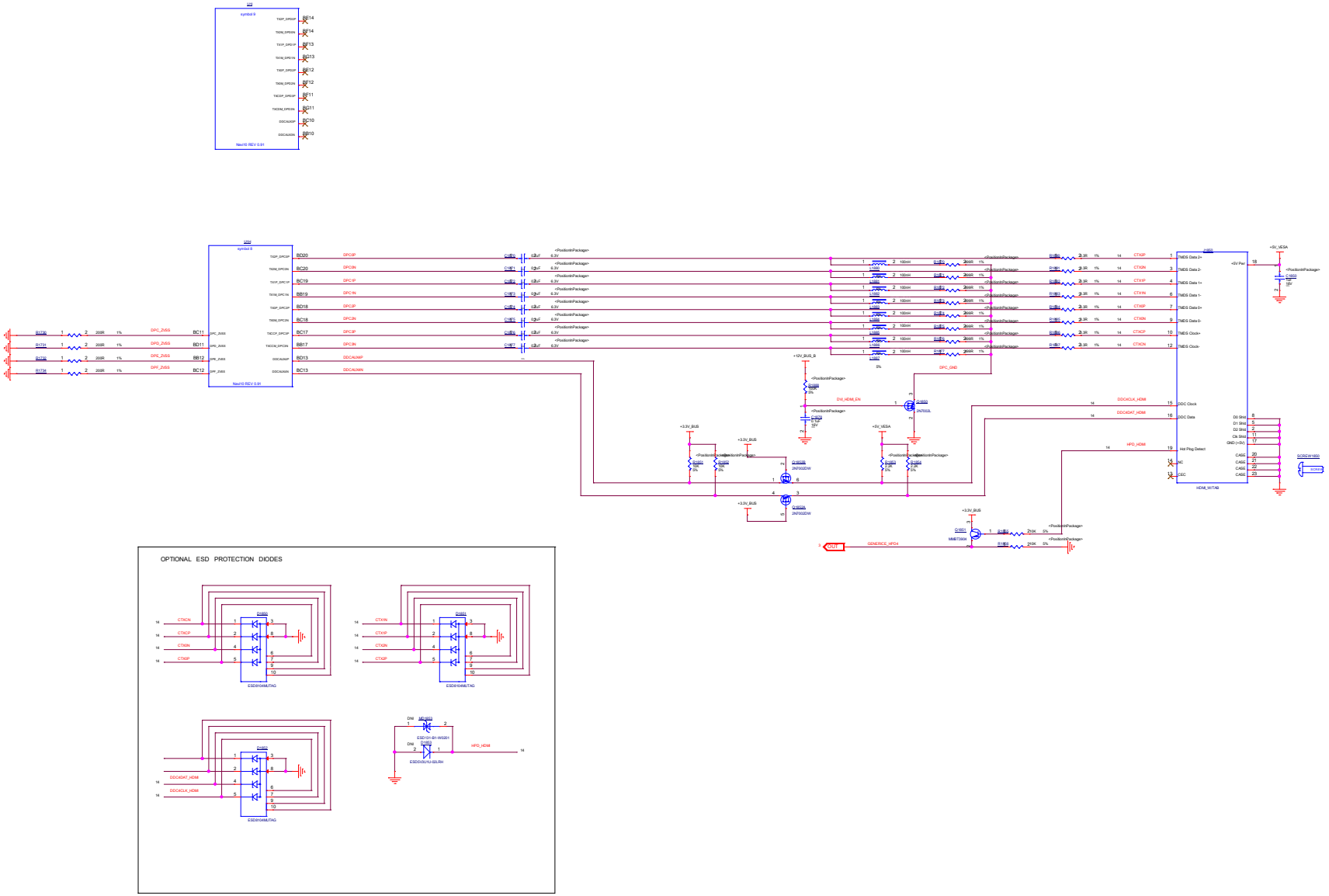


NAVI10 TMDP A/B

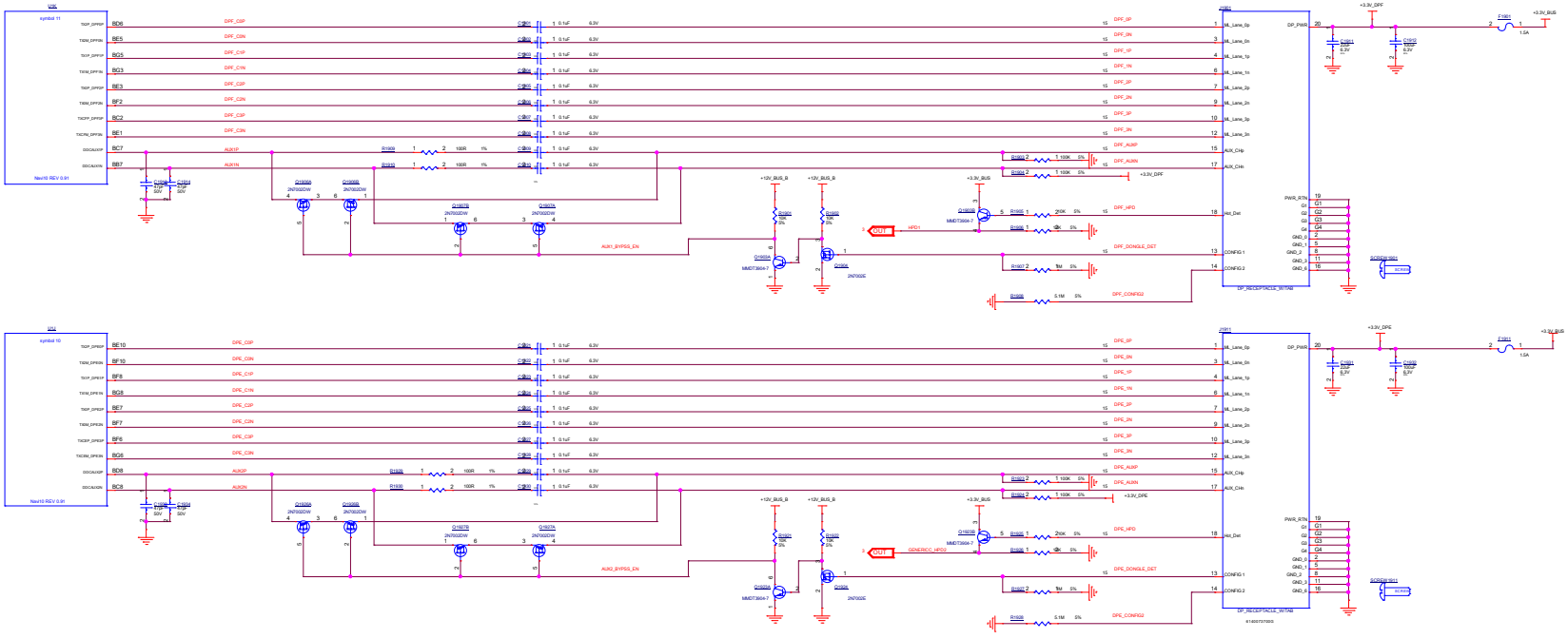
PRELIMINARY AND SUBJECT TO CHANGE

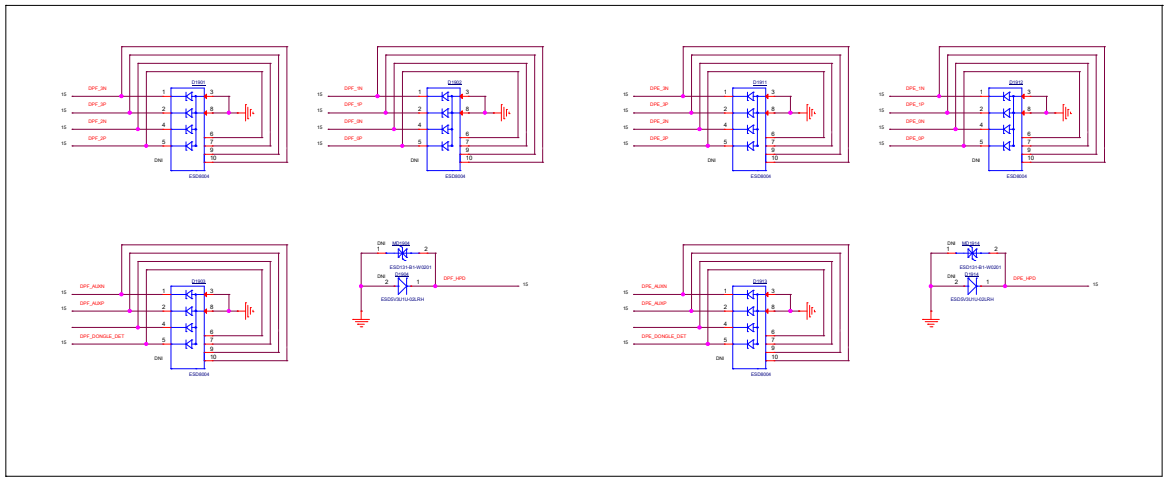


NAVI10 TMDP C/D

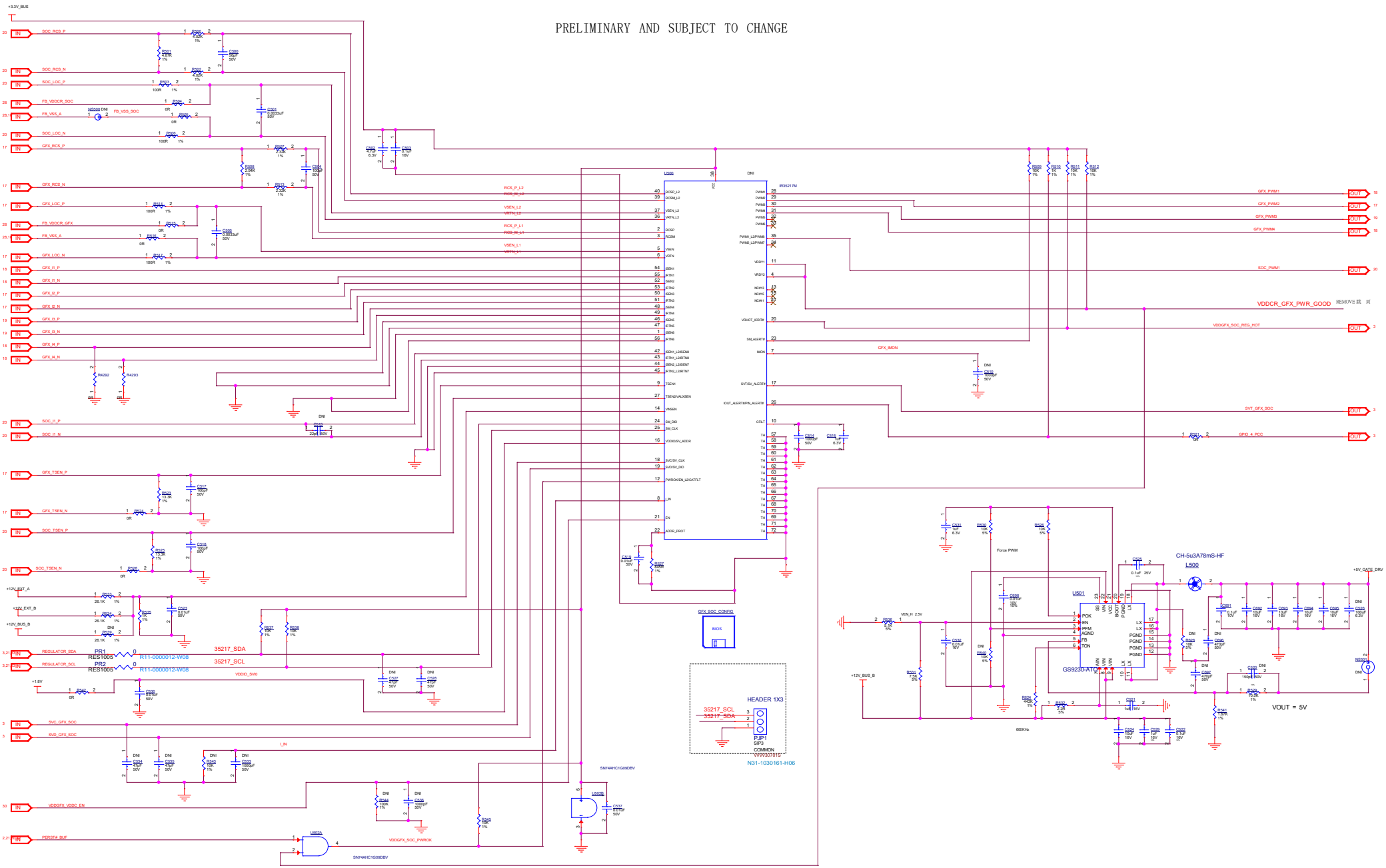


(9) NAVI10 TMDP E/F

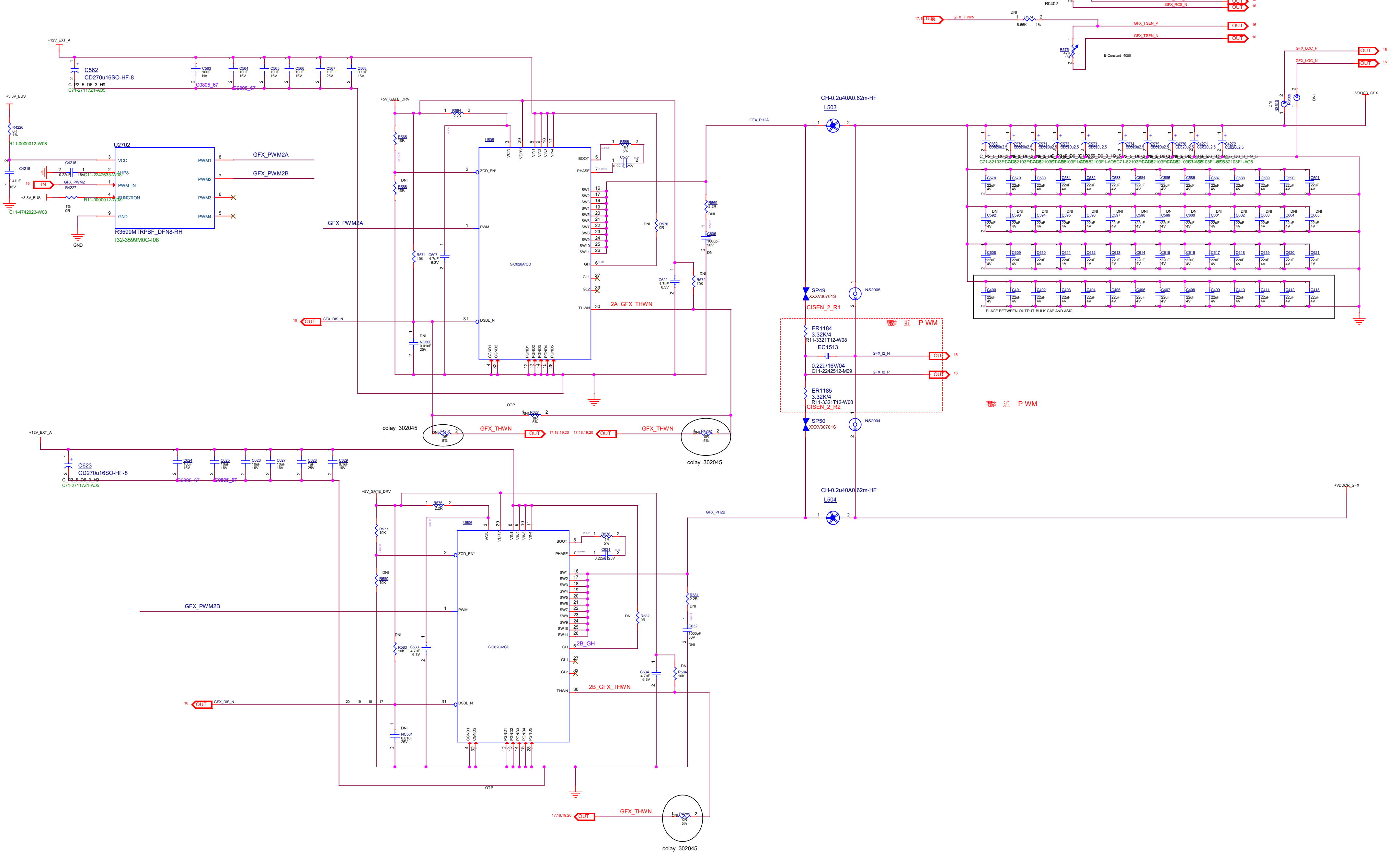




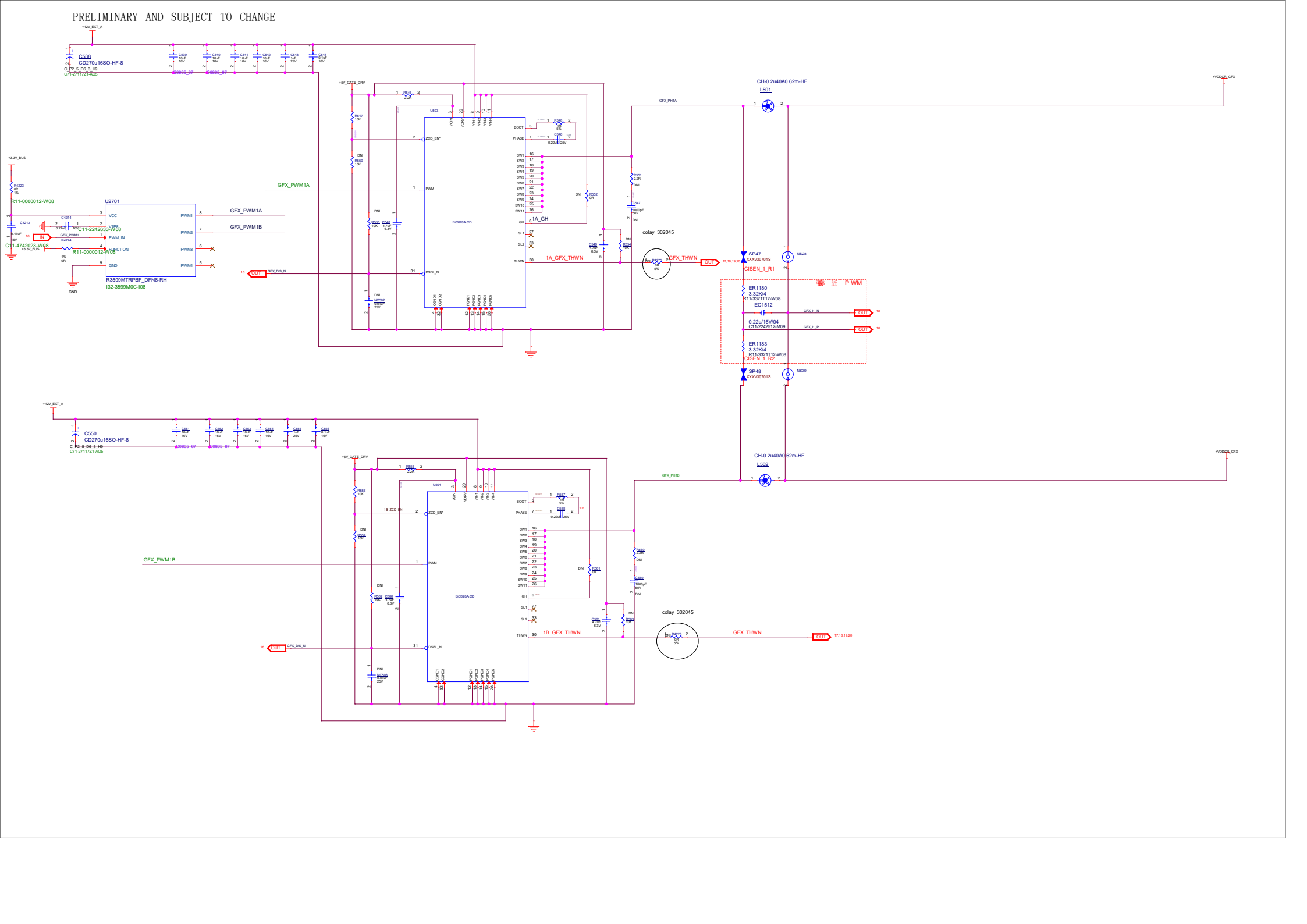
PRELIMINARY AND SUBJECT TO CHANGE



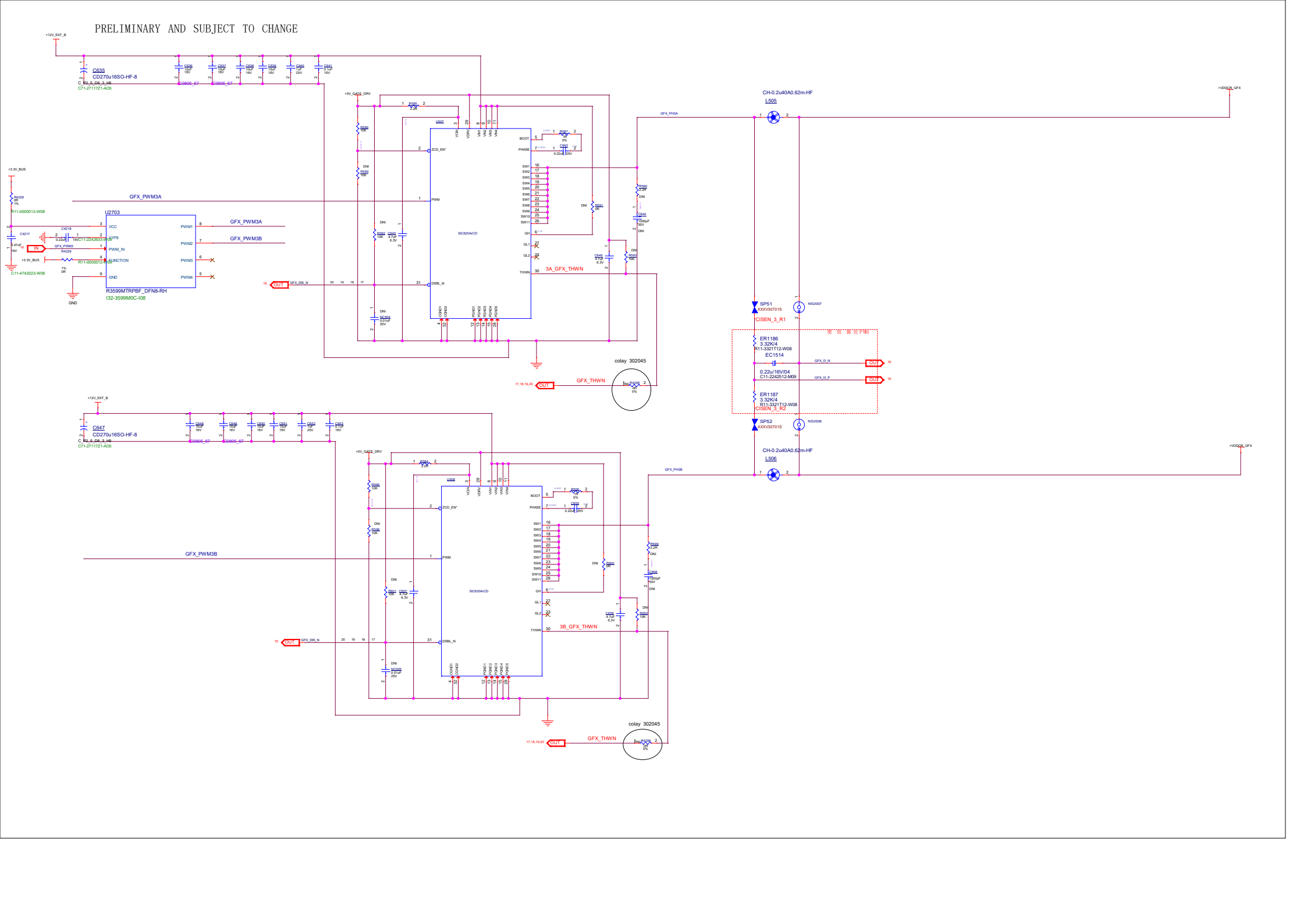
PRELIMINARY AND SUBJECT TO CHANGE

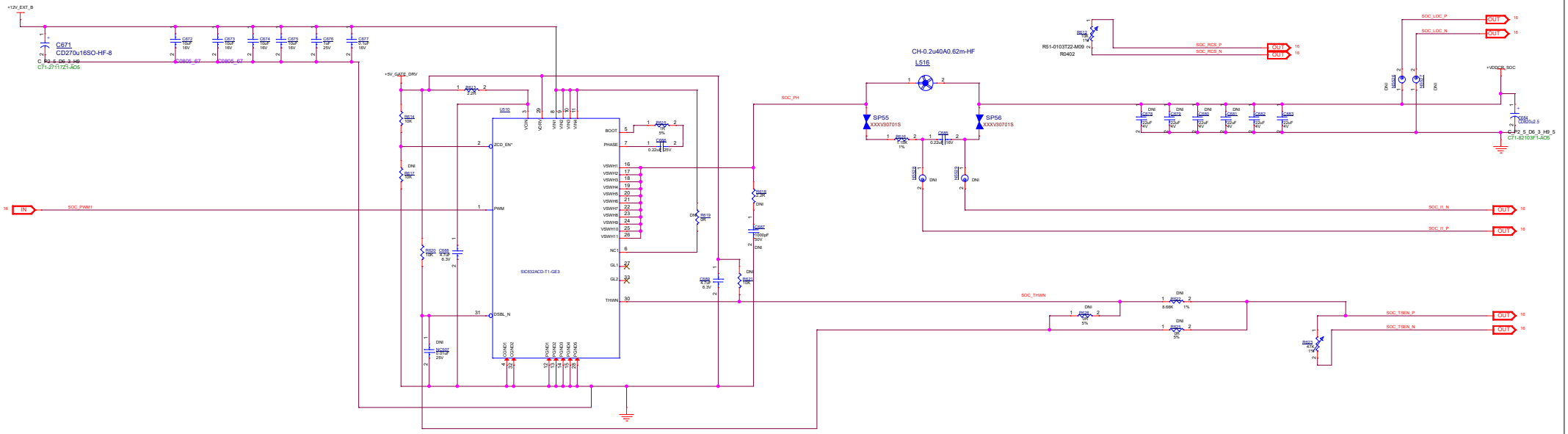


PRELIMINARY AND SUBJECT TO CHANGE

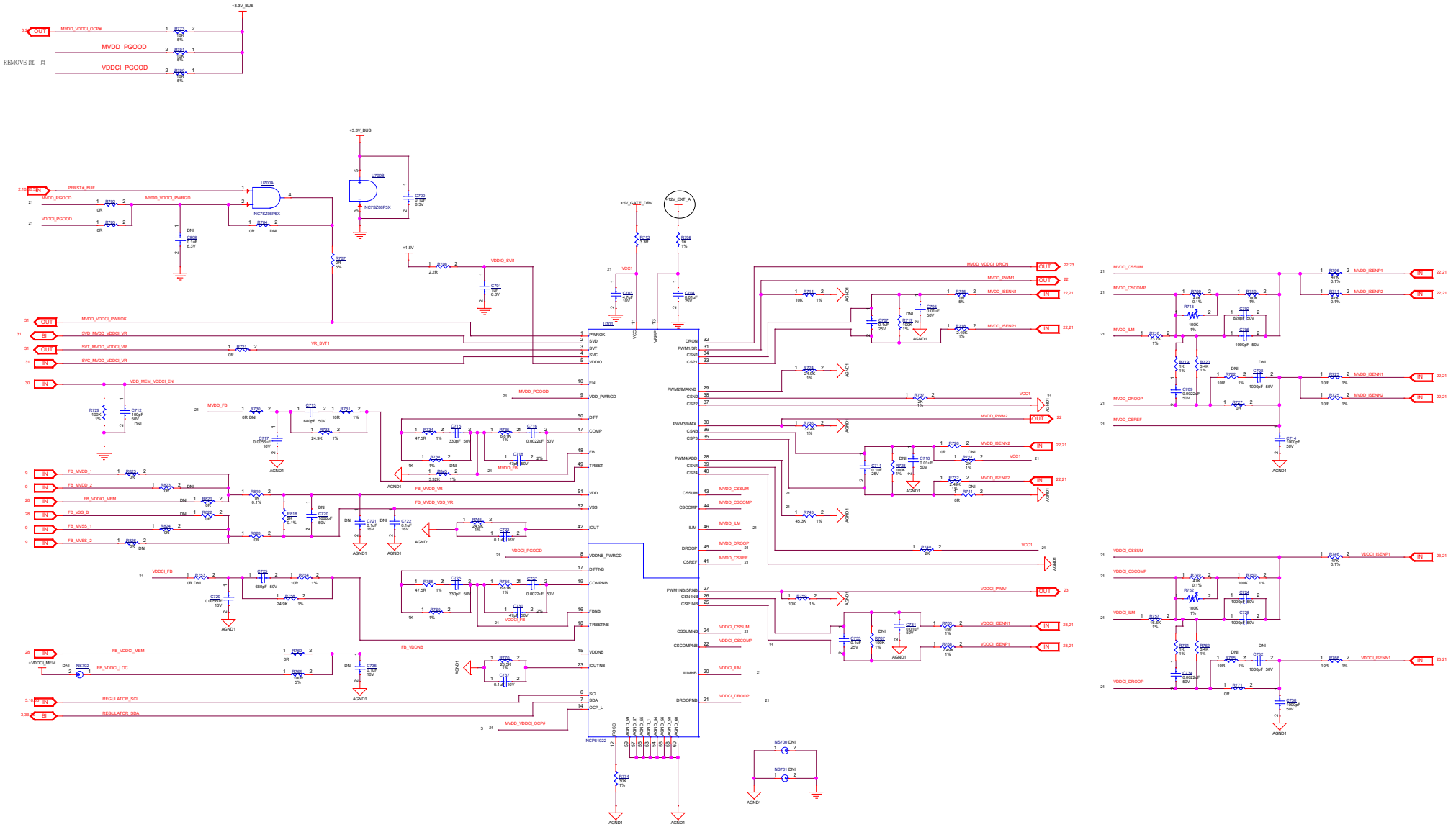


PRELIMINARY AND SUBJECT TO CHANGE

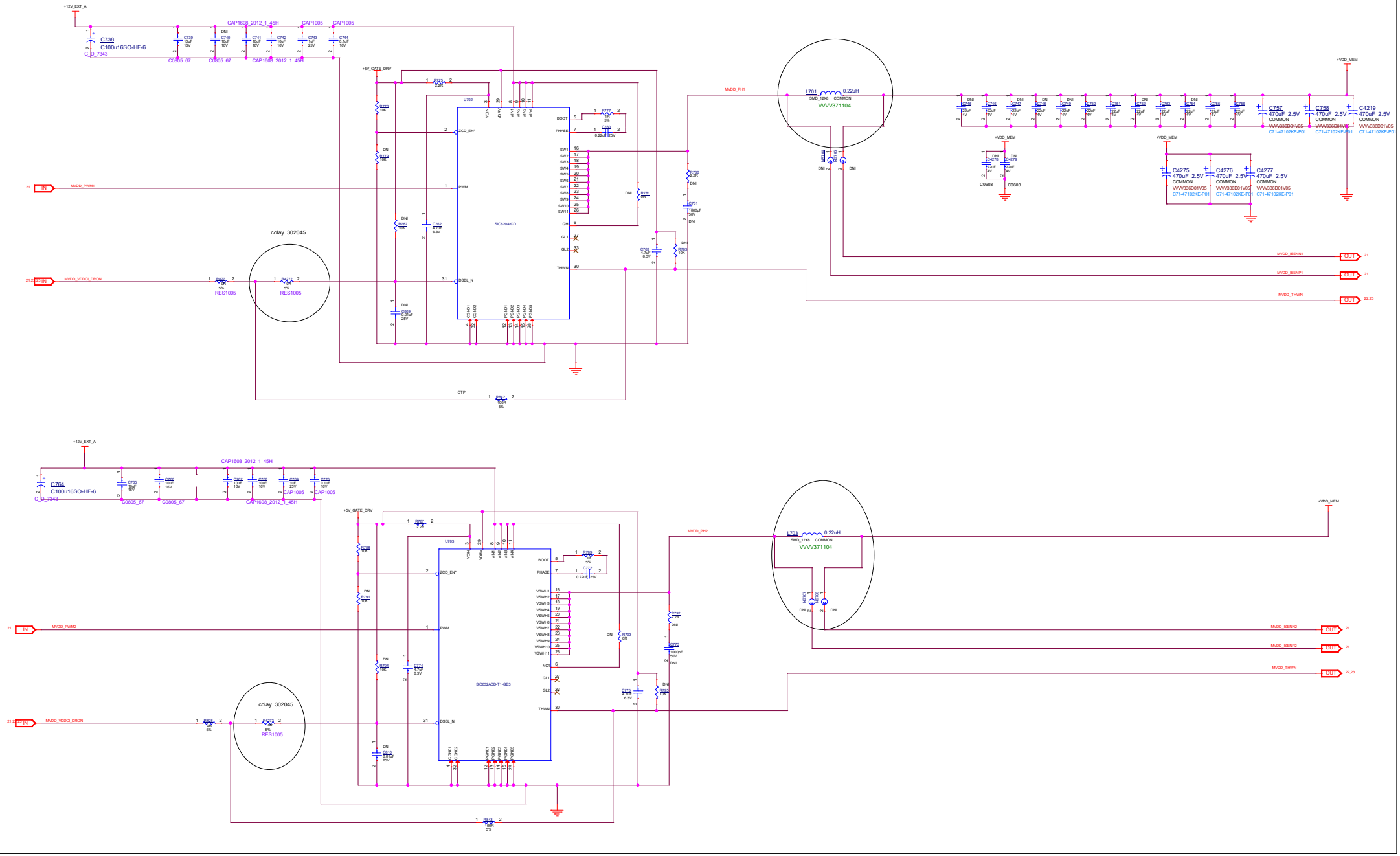



+12V_EXT_B
C671
CD270u16SO-HF-8
C_P2_5_D6_3_H9
C71-2711Z1-AO5
C672 150uF 16V
C673 150uF 16V
C674 150uF 16V
C675 150uF 16V
C676 1uF 25V
C677 0.1uF 16V
C0805_67
+5V_GATE_DRV
R613 2.2R
R614 10K
DNI R617 10K
ZCD_EN*
PWM
DSBL_N
R620 10R
C656 4.7uF 6.3V
DNI NC/50V 0.47uF 25V
U510
SIC632ACD-T1-GE3
VCIN
VDRV
VIN1
VIN2
VIN3
VIN4
BOOT
PHASE
VSWH1
VSWH2
VSWH3
VSWH4
VSWH5
VSWH6
VSWH7
VSWH8
VSWH9
VSWH10
VSWH11
NC1
GL1
GL2
THWN
PGND1
PGND2
PGND3
PGND4
PGND5
SGND1
SGND2
R610 5%
C658 0.22nF 25V
R615 5%
C657 1500pF 750V
DNI R619 0R
C660 4.7uF 6.3V
DNI R621 10K
SOC_PWM1
IN
SOC_PH
CH-0.2u40A0.62m-HF
L516
SP55
XXXV30701S
SP56
XXXV30701S
R616 1K 1%
C659 0.22nF 25V
DNI D510
DNI D511
R618 2.2R
DNI
R51-0103722-M09
R0402
R616 10K
SOC_RCS_P
SOC_RCS_N
OUT
DNI C678 22uF 16V
DNI C679 22uF 16V
DNI C680 22uF 16V
DNI C681 22uF 16V
C682 22uF 16V
C683 22uF 16V
DNI C684
DNI C685
SOC_LOC_P
SOC_LOC_N
+VDDCR_SOC
C684 1000u2.5
C_P2_5_D6_3_H9_5
C71-8210F1-AO5
SOC_I1_N
SOC_I1_P
SOC_THWN
DNI R635 5%
DNI R0402 8.66K 1%
DNI R636 5%
SOC_TSEN_P
SOC_TSEN_N
R637 47K 1%

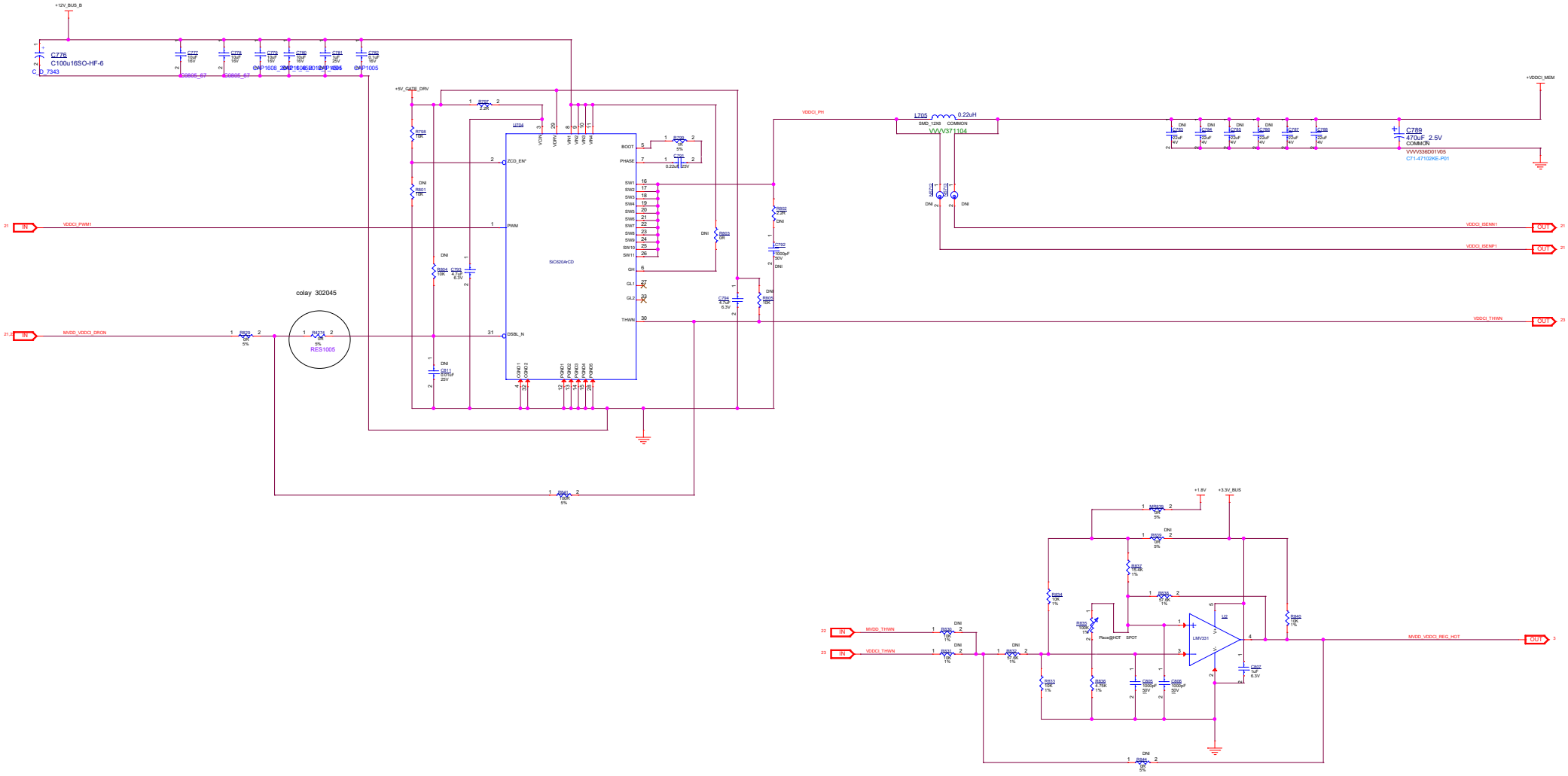
PRELIMINARY AND SUBJECT TO CHANGE



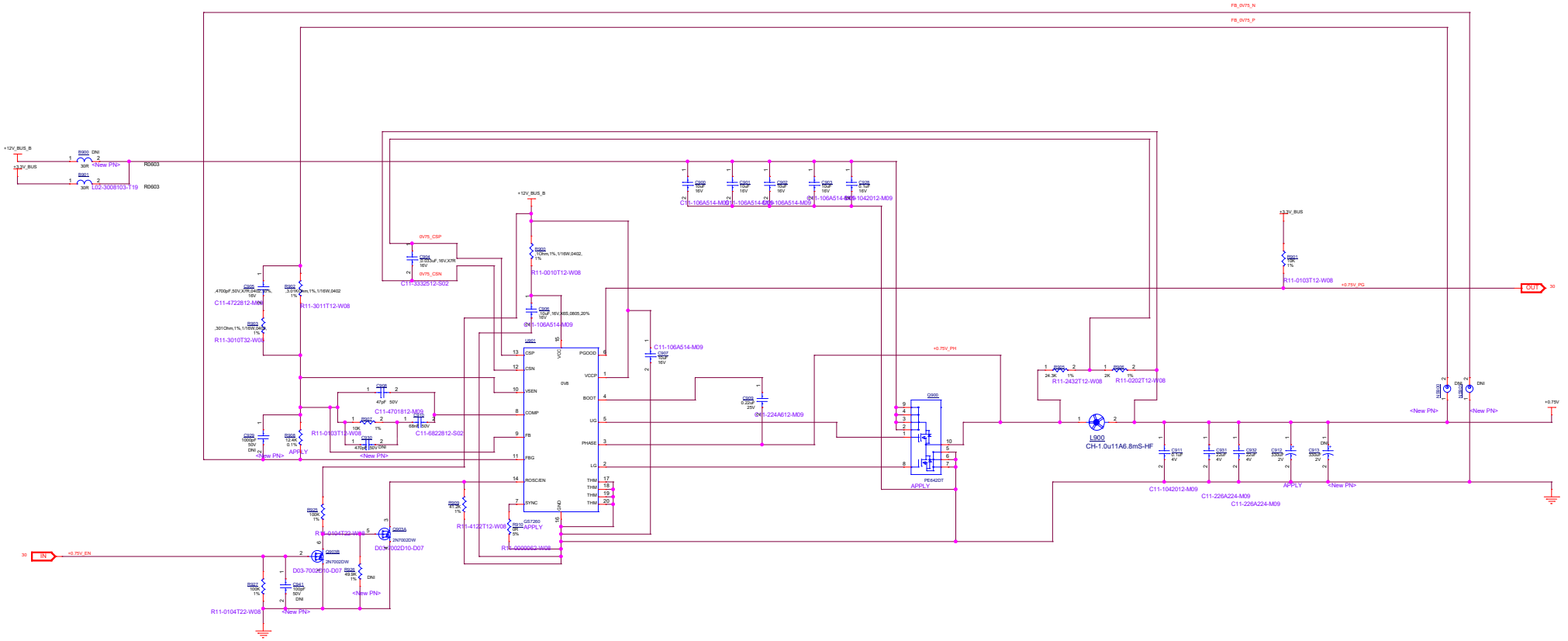
PRELIMINARY AND SUBJECT TO CHANGE

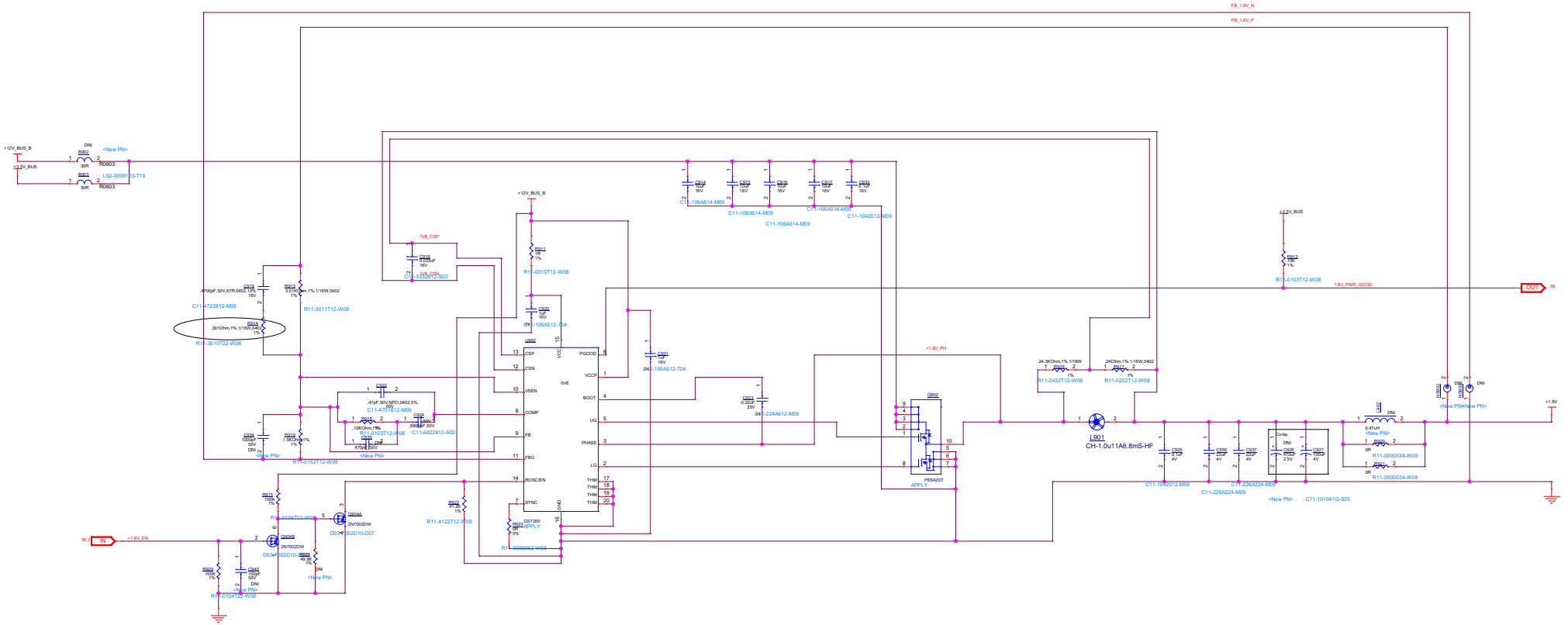


PRELIMINARY AND SUBJECT TO CHANGE



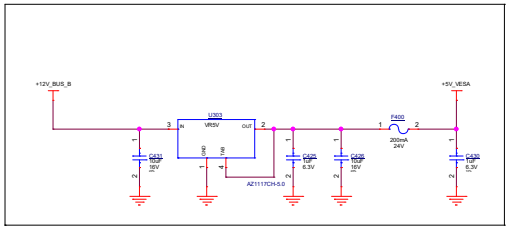
PRELIMINARY AND SUBJECT TO CHANGE

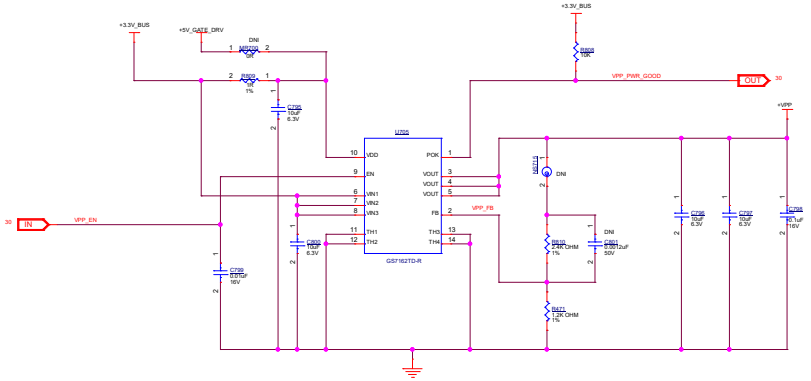



+12V_BUS_B
+12V_BUS
L02-3008103-T19
R11-3011T12-W08
R11-3010T32-W08
R11-0010T12-W08
R11-0103T12-W08
R11-2432T12-W08
R11-0202T12-W08
R11-0152T12-W08
R11-0103T32-W08
R11-0104T22-W08
R11-4122T12-W08
R11-0000034-W08
R11-0000063-W08
C11-4722812-M09
C11-106A514-M09
C11-1042612-M09
C11-105A512-T04
C11-224A612-M09
C11-4702T12-M09
C11-6822812-S02
C11-3332Y12-S02
C11-1042012-M09
C11-226A224-M09
C71-101041G-S03
L901
CH-1.0u11A6.8mS-HF
Q902
PE64203T
APPLY
U902
GS7260
APPLY
FB_1.8V_N
FB_1.8V_P
1.8V_PWR_GOOD
OUT
IN
+1.8V_EN
+1.8V_PH
+1.8V
VB_CSP
VB_CSN
VB
CSP
CSN
VDEN
COMP
FB
FBG
RDSCIEN
SYNC
VCC
PGOOD
VCCP
BOOT
UG
PHASE
LG
THM
GND
<New PN>
DNI

REGULATOR FOR +5V RAILS

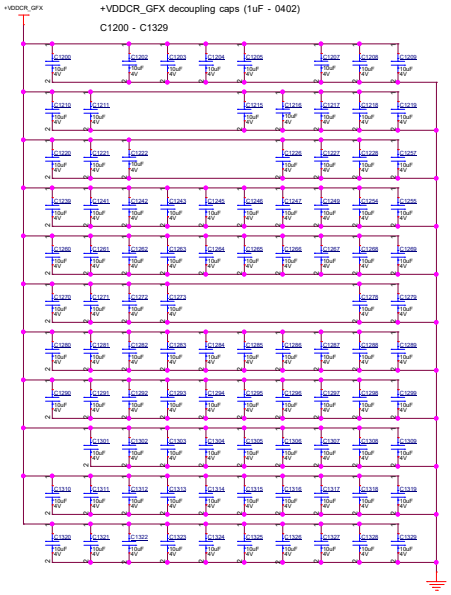
IOUT = 50mA





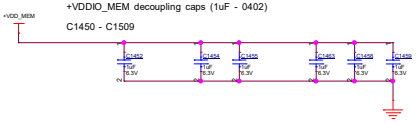
+VDDCR_GFX decoupling caps (1uF - 0402)

C1200 - C1329



+VDDIO_MEM decoupling caps (1uF - 0402)

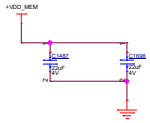
C1450 - C1509



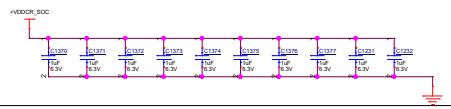
+VDDIO_MEM decoupling caps (22uF)

C1510 - C1539

0805



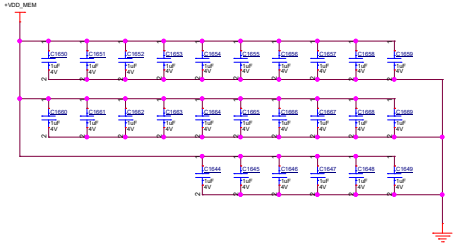
+VDDCR_SOC decoupling caps (1uF - 0402)



+VDDIO_MEM decoupling caps (1uF)

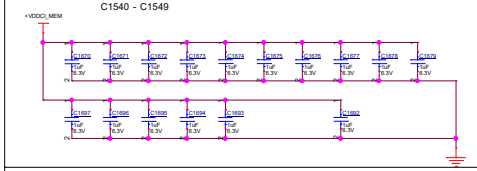
C1650 - C1669

0201



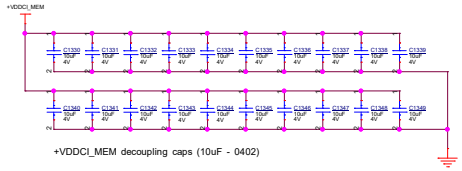
+VDDCI_MEM decoupling caps (1uF - 0402)

C1540 - C1549

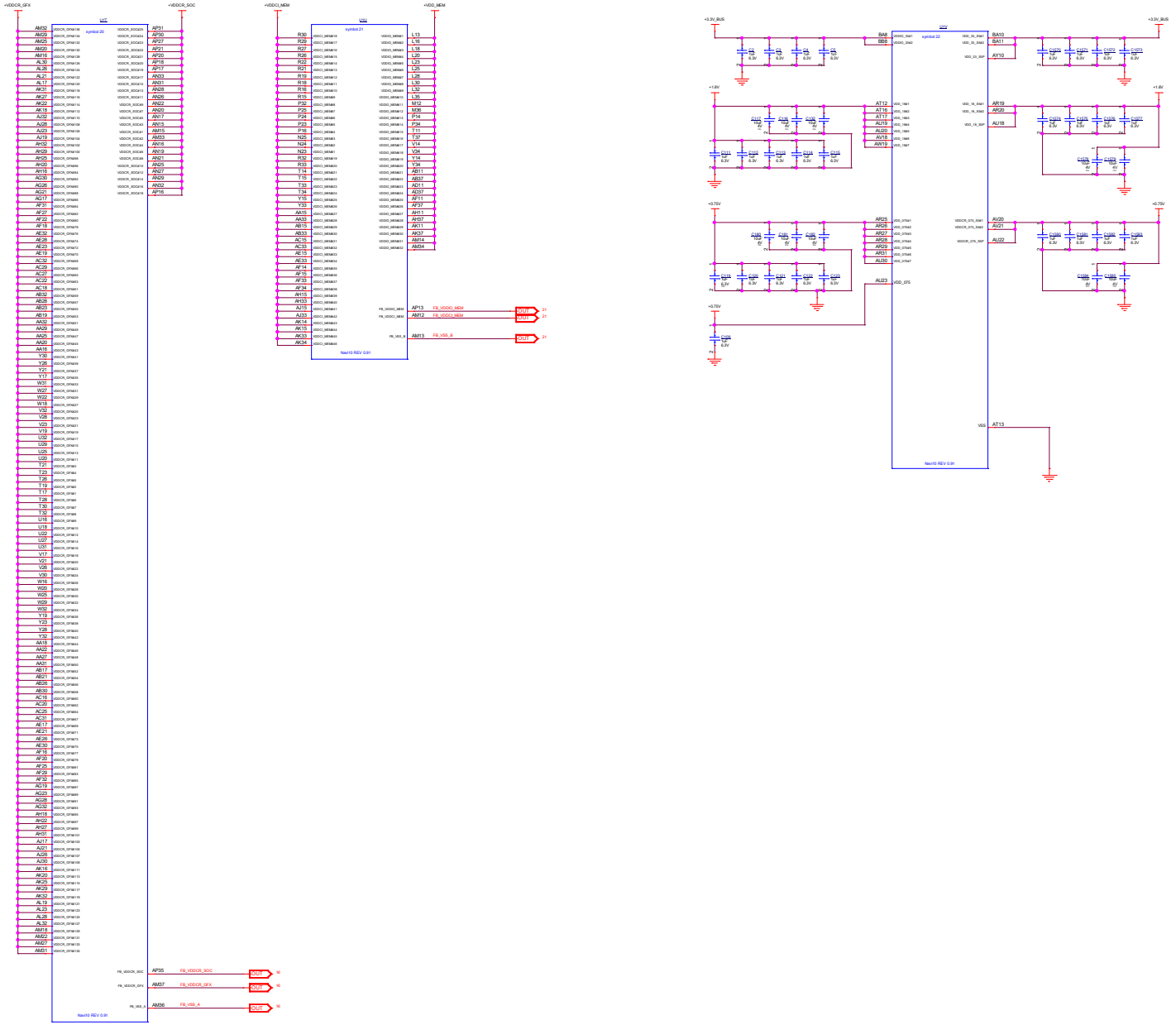


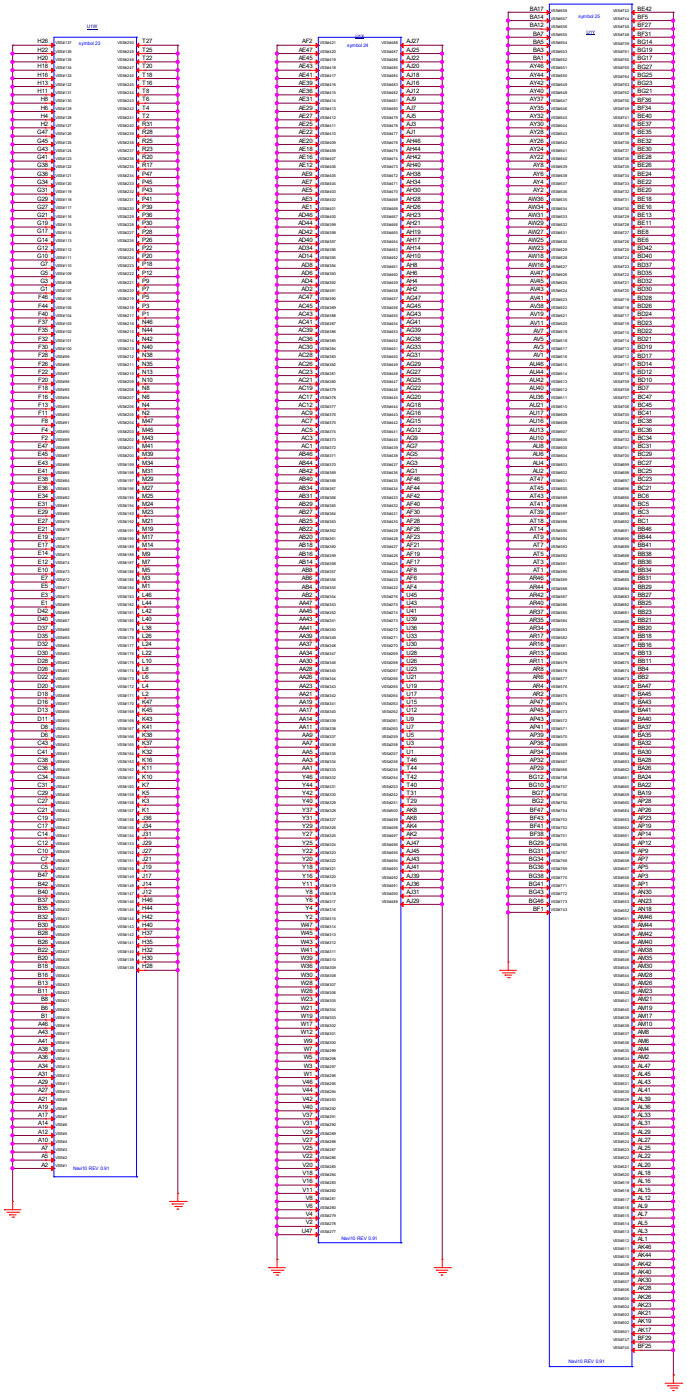
+VDDCI_MEM decoupling caps (22uF - 0805)

C1684 - C1687 C1640 - C1642

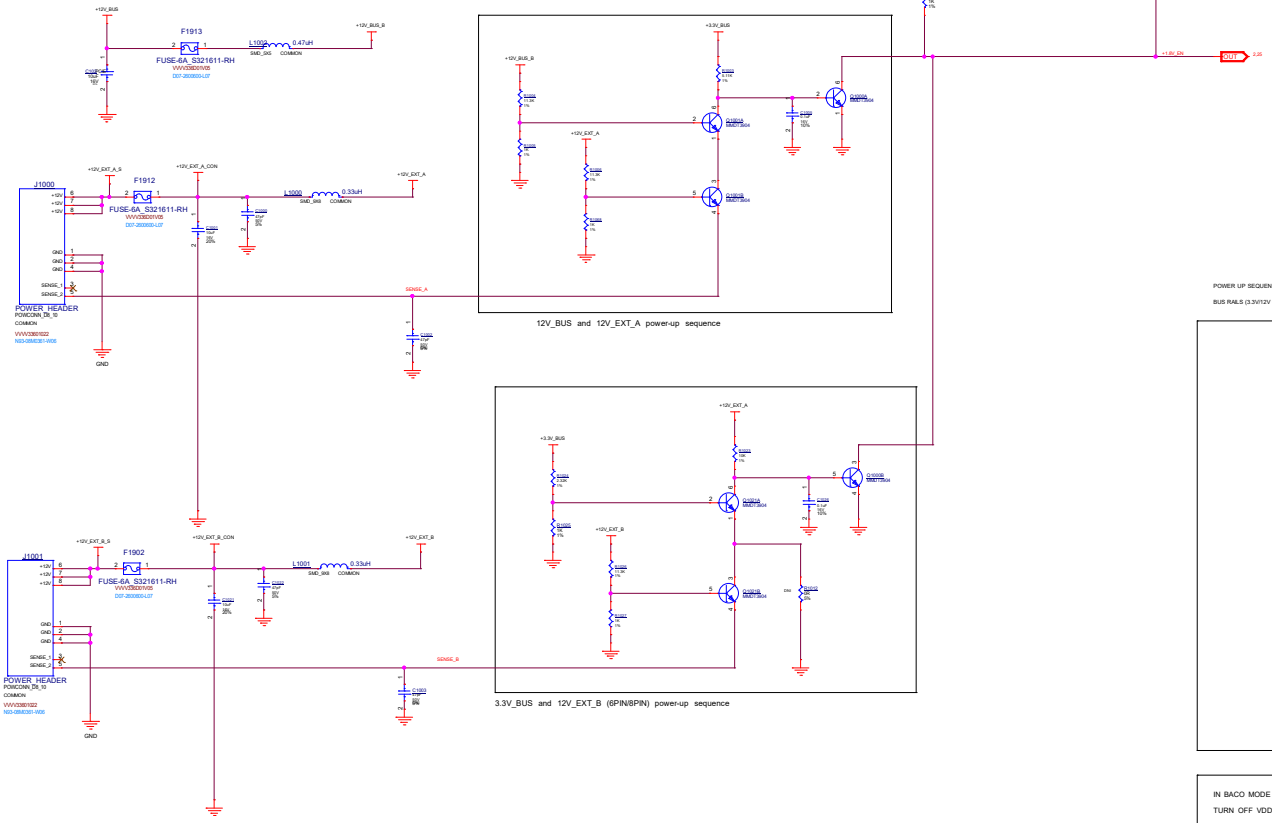


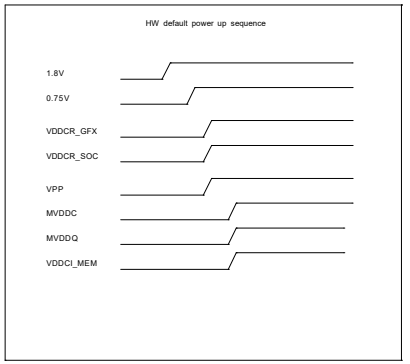
+VDDCI_MEM decoupling caps (10uF - 0402)





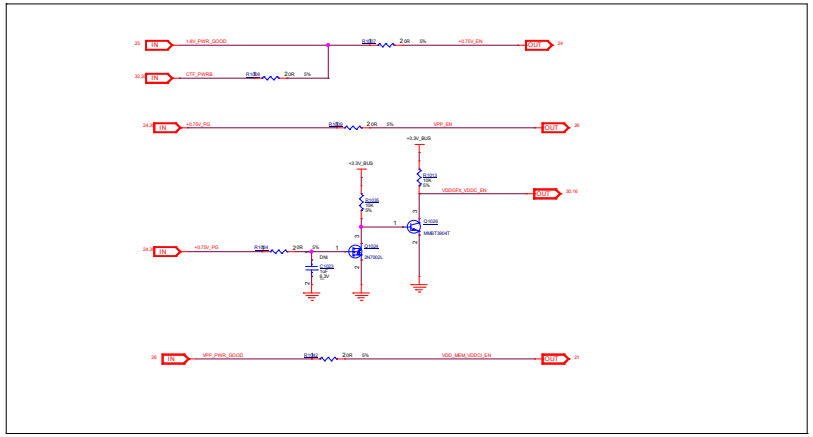
PRELIMINARY AND SUBJECT TO CHANGE





POWER UP SEQUENCE

BUS RAILS (3.3V/12V UP) -> +1.8V -> 0.75V -> VDDGFX/VDDSOC
-> VPP -> VDDCI/MVDD

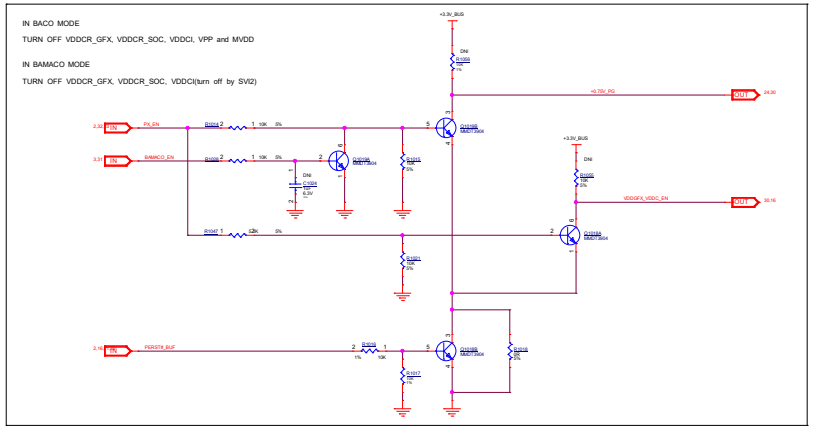


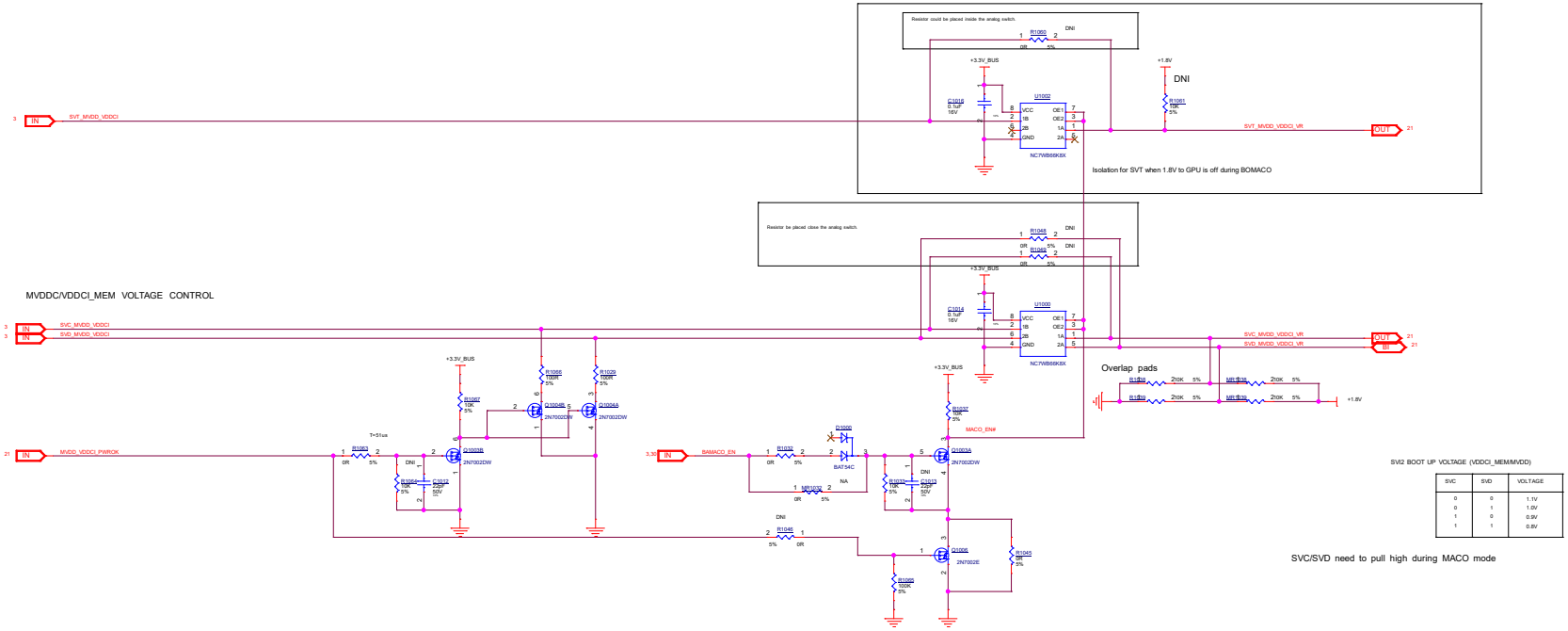
IN BACO MODE

TURN OFF VDDCR_GFX, VDDCR_SOC, VDDCI, VPP and MVDD

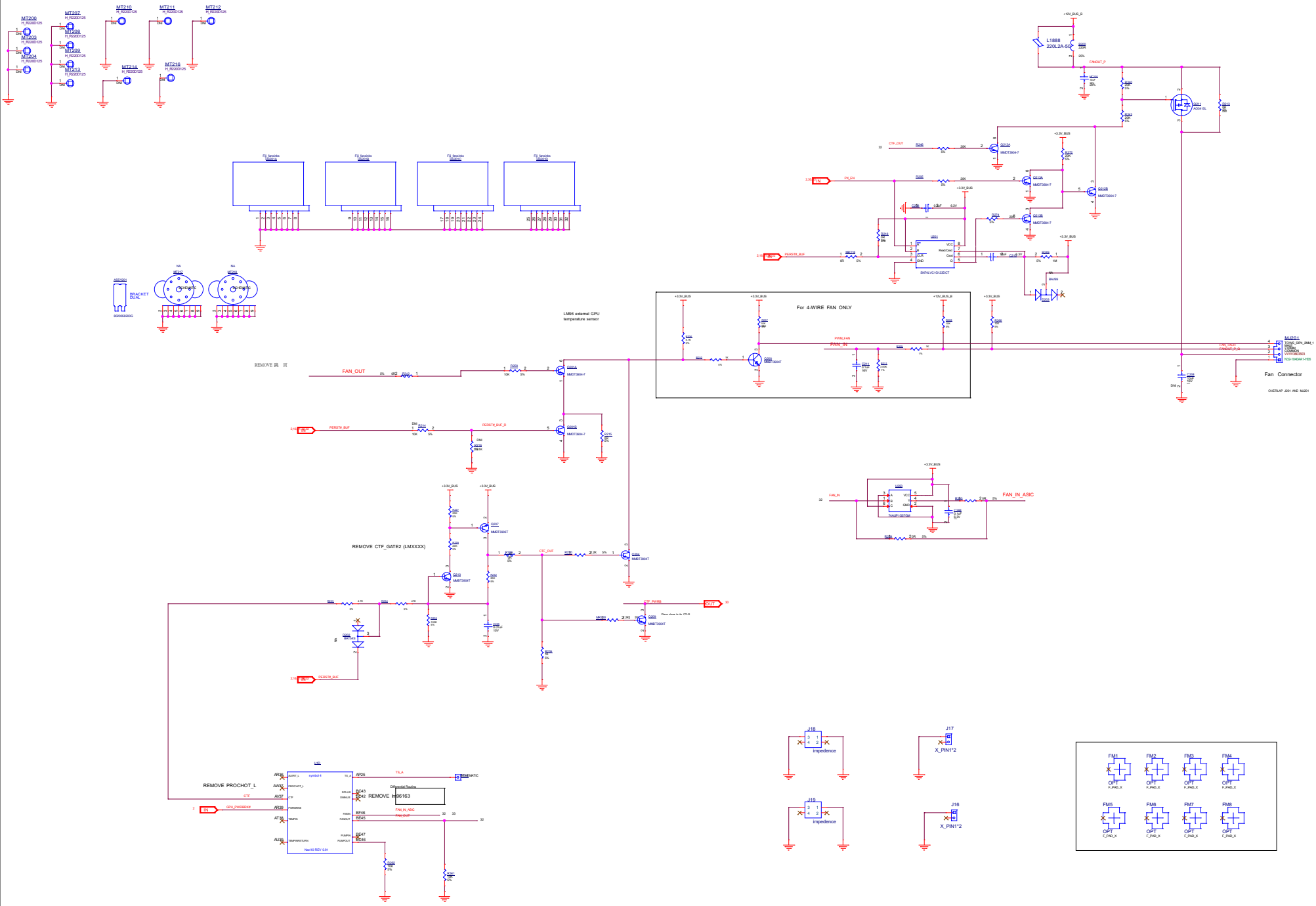
IN BAMACO MODE

TURN OFF VDDCR_GFX, VDDCR_SOC, VDDCI(turn off by SVI2)

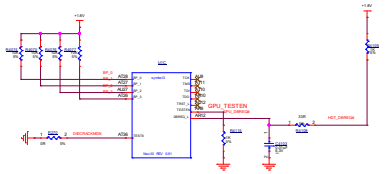



MVDDC/VDDCI_MEM VOLTAGE CONTROL
SVT_MVDD_VDDCI
SVC_MVDD_VDDCI
SVD_MVDD_VDDCI
MVDD_VDDCI_PWROK
BAMACO_EN
MACO_EN#
Resistor could be placed inside the analog switch.
Resistor be placed close the analog switch.
Isolation for SVT when 1.8V to GPU is off during BOMACO
Overlap pads
SVT_MVDD_VDDCI_VR
SVC_MVDD_VDDCI_VR
SVD_MVDD_VDDCI_VR
SVI2 BOOT UP VOLTAGE (VDDCI_MEM/MVDD)
SVC
SVD
VOLTAGE
0
0
1.1V
0
1
1.0V
1
0
0.9V
1
1
0.8V
SVC/SVD need to pull high during MACO mode

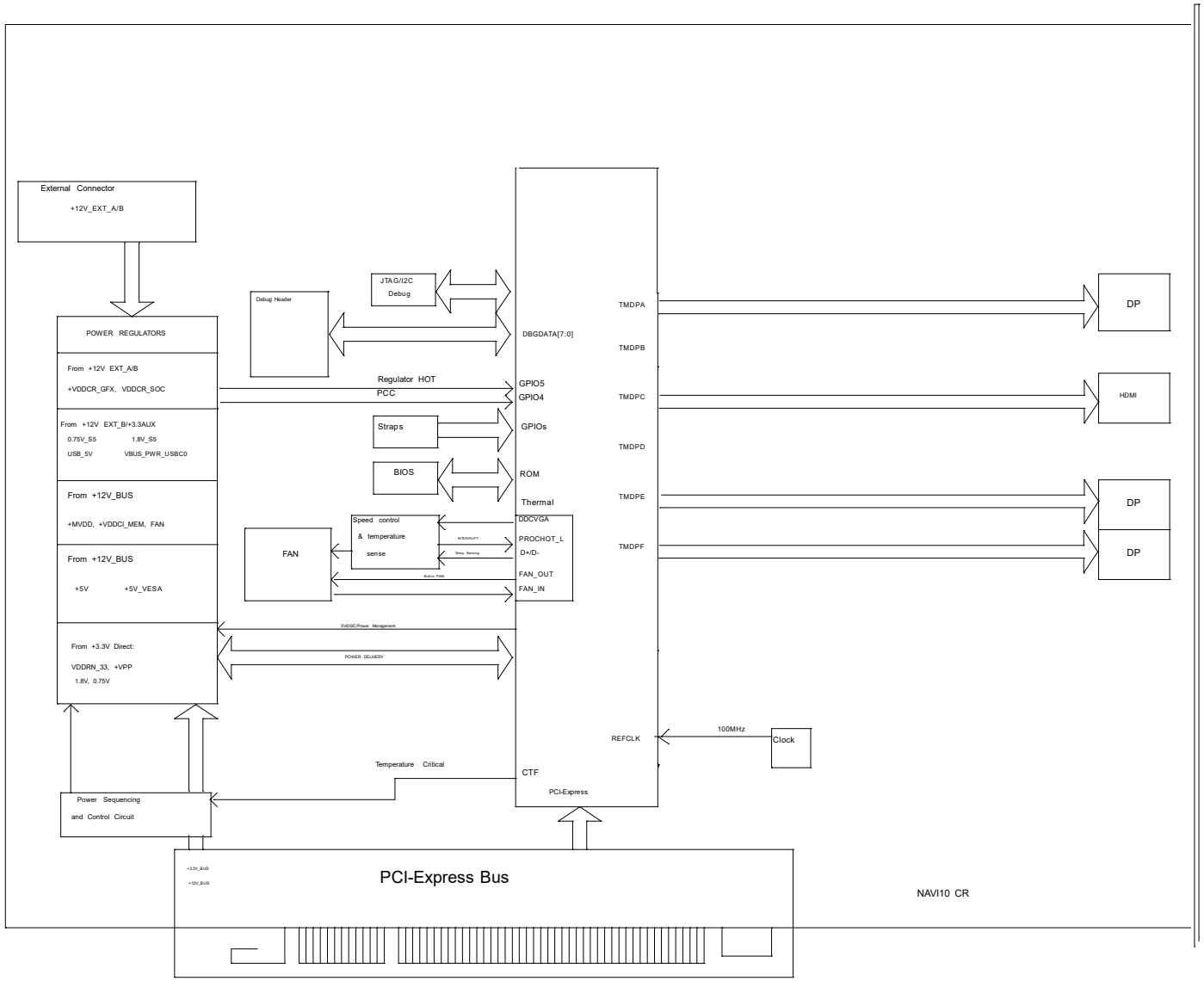
PRELIMINARY AND SUBJECT TO CHANGE

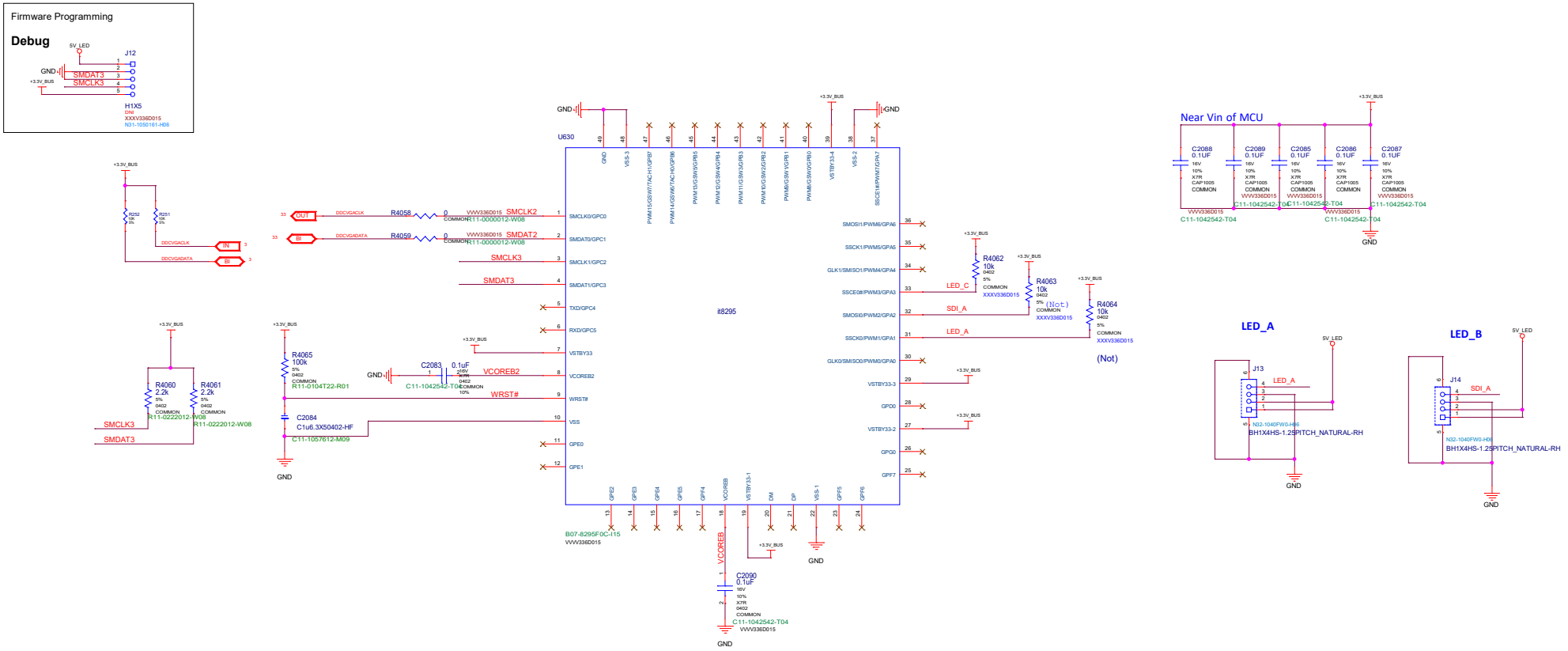


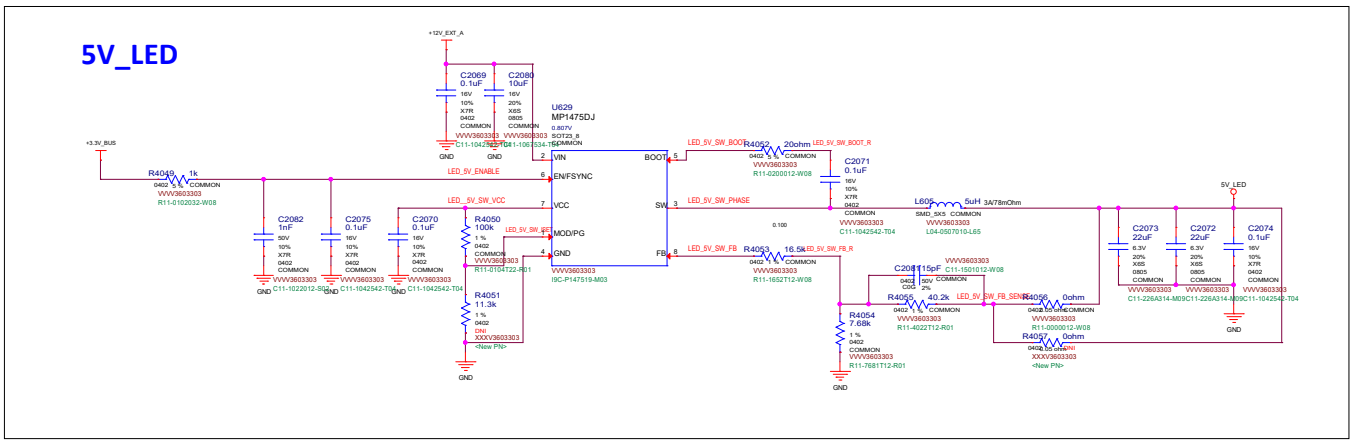
PRELIMINARY AND SUBJECT TO CHANGE



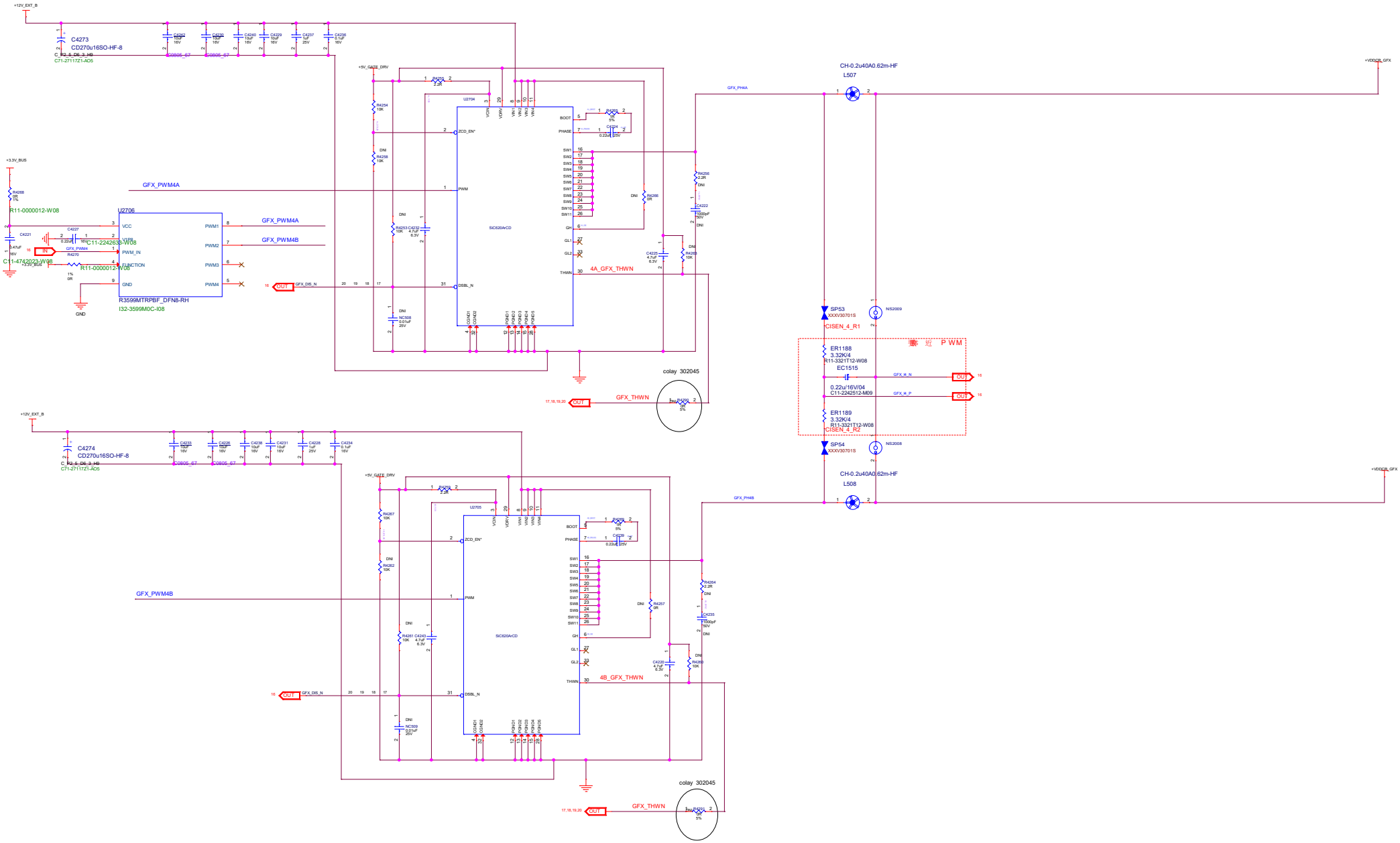
RADEON Lightbar header


External Connector
+12V_EXT_A/B
POWER REGULATORS
From +12V EXT_A/B
+VDDCR_GFX, VDDCR_SOC
From +12V EXT_B/+3.3AUX
0.75V_S5
1.8V_S5
USB_5V
VBUS_PWR_USBC0
From +12V_BUS
+MVDD, +VDDCI_MEM, FAN
From +12V_BUS
+5V
+5V_VESA
From +3.3V Direct:
VDDRN_33, +VPP
1.8V, 0.75V
Power Sequencing
and Control Circuit
Debug Header
JTAG/I2C
Debug
Regulator HOT
PCC
Straps
BIOS
FAN
Speed control
& temperature
sense
SVID/I2C Power Management
POWER DELIVERY
Temperature Critical
DBGDATA[7:0]
GPIO5
GPIO4
GPIOs
ROM
Thermal
DDCVGA
PROCHOT_L
D+/D-
FAN_OUT
FAN_IN
CTF
PCI-Express
TMDPA
TMDPB
TMDPC
TMDPD
TMDPE
TMDPF
DP
HDMI
DP
DP
REFCLK
100MHz
Clock
PCI-Express Bus
+3.3V_BUS
+12V_BUS
NAVI10 CR


Firmware Programming
Debug
5V_LED
J12
GND
SMDAT3
SMCLK3
+3.3V_BUS
H1X5
DNI
XXXV336D015
N31-1050161-H06
U630
i28295
SMCLK2
SMDAT2
SMCLK3
SMDAT3
WRST#
VCOREB2
VCOREB
R4062
10k
R4063
10k
(Not)
R4064
10k
LED_C
SDI_A
LED_A
Near Vin of MCU
C2088
C2089
C2085
C2086
C2087
0.1UF
C11-1042542-T04
LED_A
LED_B
J13
J14
BH1X4HS-1.25PITCH_NATURAL-RH
R4060
2.2k
R4061
2.2k
R11-0222012-W08
R4065
100k
R11-0104T22-R01
C2083
0.1uF
C2084
C1u6.3X50402-HF
C11-1057612-M09
B07-8295F0C-I15
VVV336D015


5V_LED
+12V_EXT_A
U629
MP1475DJ
C2069
0.1uF
C2080
10uF
R4040
1k
C2082
1nF
C2075
0.1uF
C2070
0.1uF
R4050
100k
R4051
11.3k
R4052
20ohm
C2071
0.1uF
L605
5uH
3A/78mOhm
R4053
16.5k
R4054
7.68k
R4055
40.2k
C2081
15pF
R4056
0ohm
R4057
0ohm
C2073
22uF
C2072
22uF
C2074
0.1uF
LED_5V_ENABLE
LED_5V_SW_VCC
LED_5V_SW_EN
LED_5V_SW_BOOT
LED_5V_SW_PHASE
LED_5V_SW_FB
LED_5V_SW_FB_R
LED_5V_SW_FB_SENSE
EN/SYNC
VCC
MOD/PG
VIN
BOOT
SW
FB
GND

PRELIMINARY AND SUBJECT TO CHANGE



PRELIMINARY AND SUBJECT TO CHANGE

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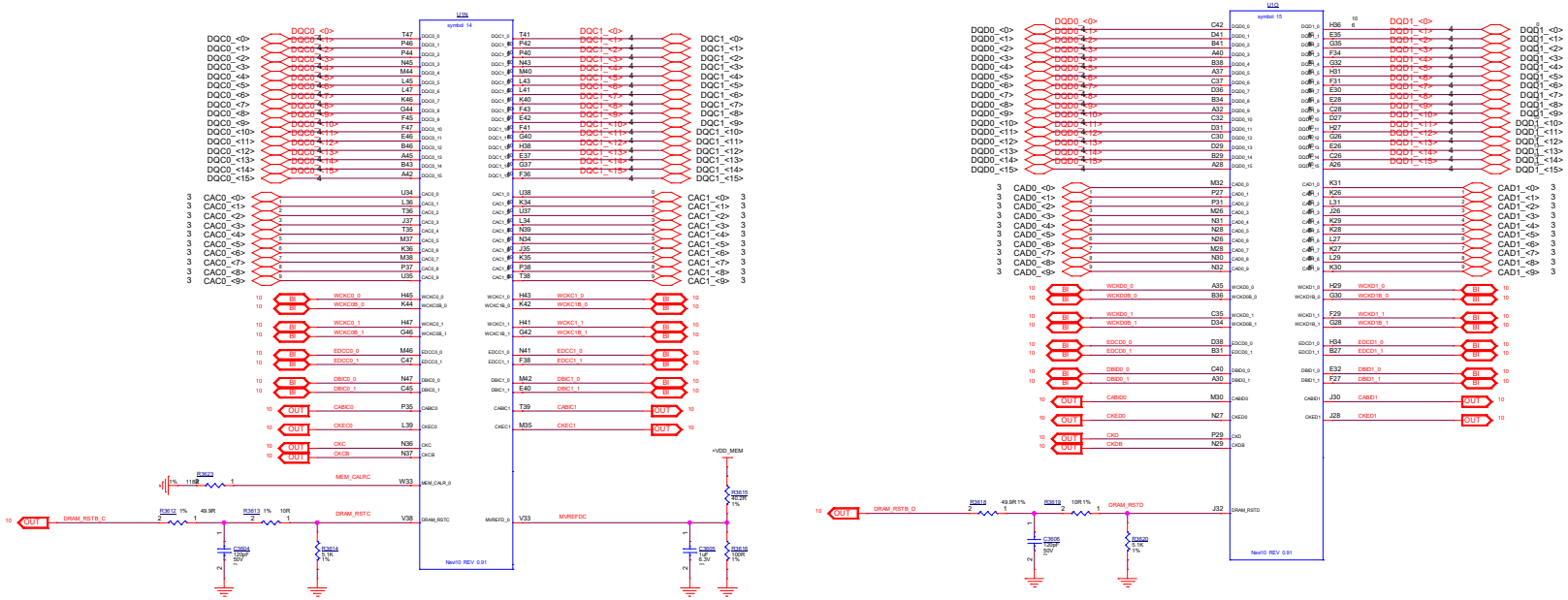
NOTES: NOTE

TITLE: NAVI10 G6X16Mode DP DP HDMI DP

NAVI 10 MEM INTERFACE CH C/D

PRELIMINARY AND SUBJECT TO CHANGE



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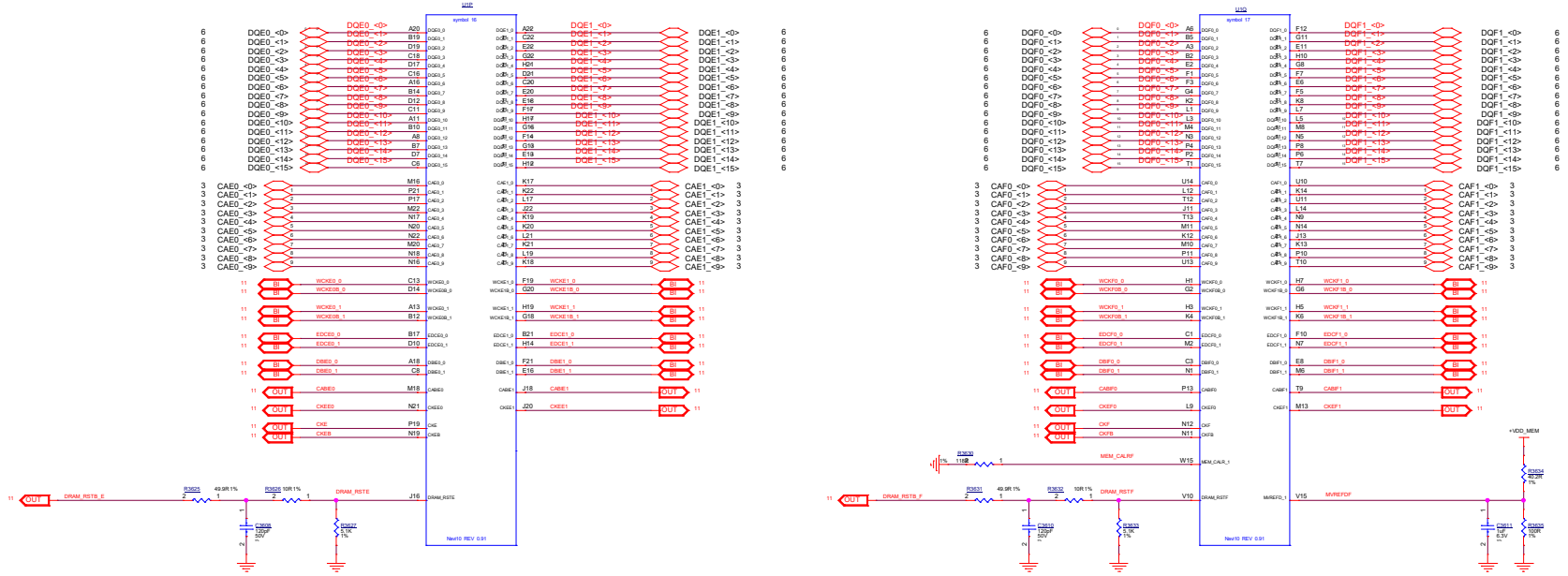
DOCUMENT NUMBER: 105_D199xx_00A	
NOTES: NOTE	

NAVI 10 MEM INTERFACE CH E/F

PRELIMINARY AND SUBJECT TO CHANGE



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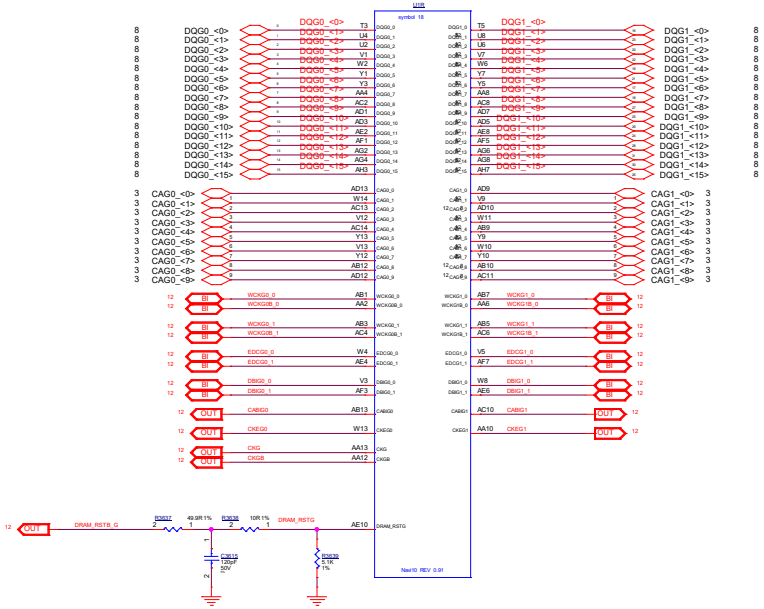
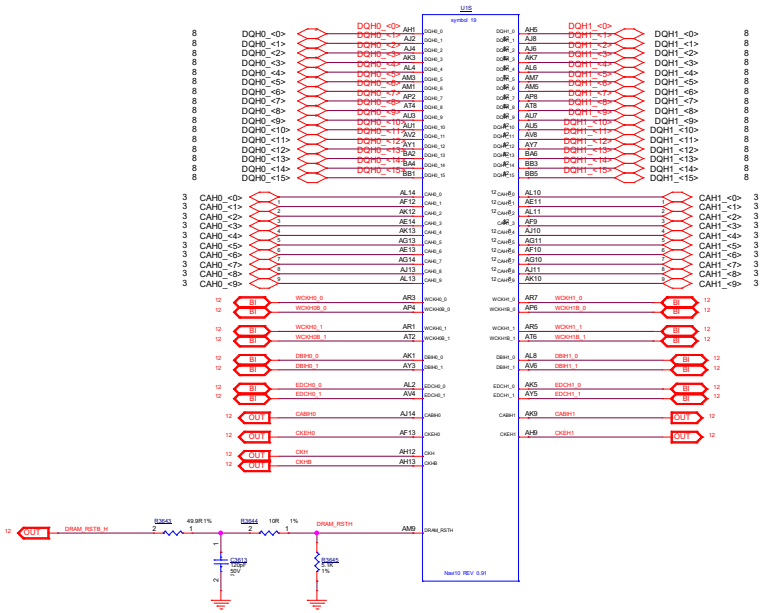
TITLE: NAVI10 G6X16Mode DP DP HDMI DP

NAVI 10 MEM INTERFACE CH G/H

PRELIMINARY AND SUBJECT TO CHANGE





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