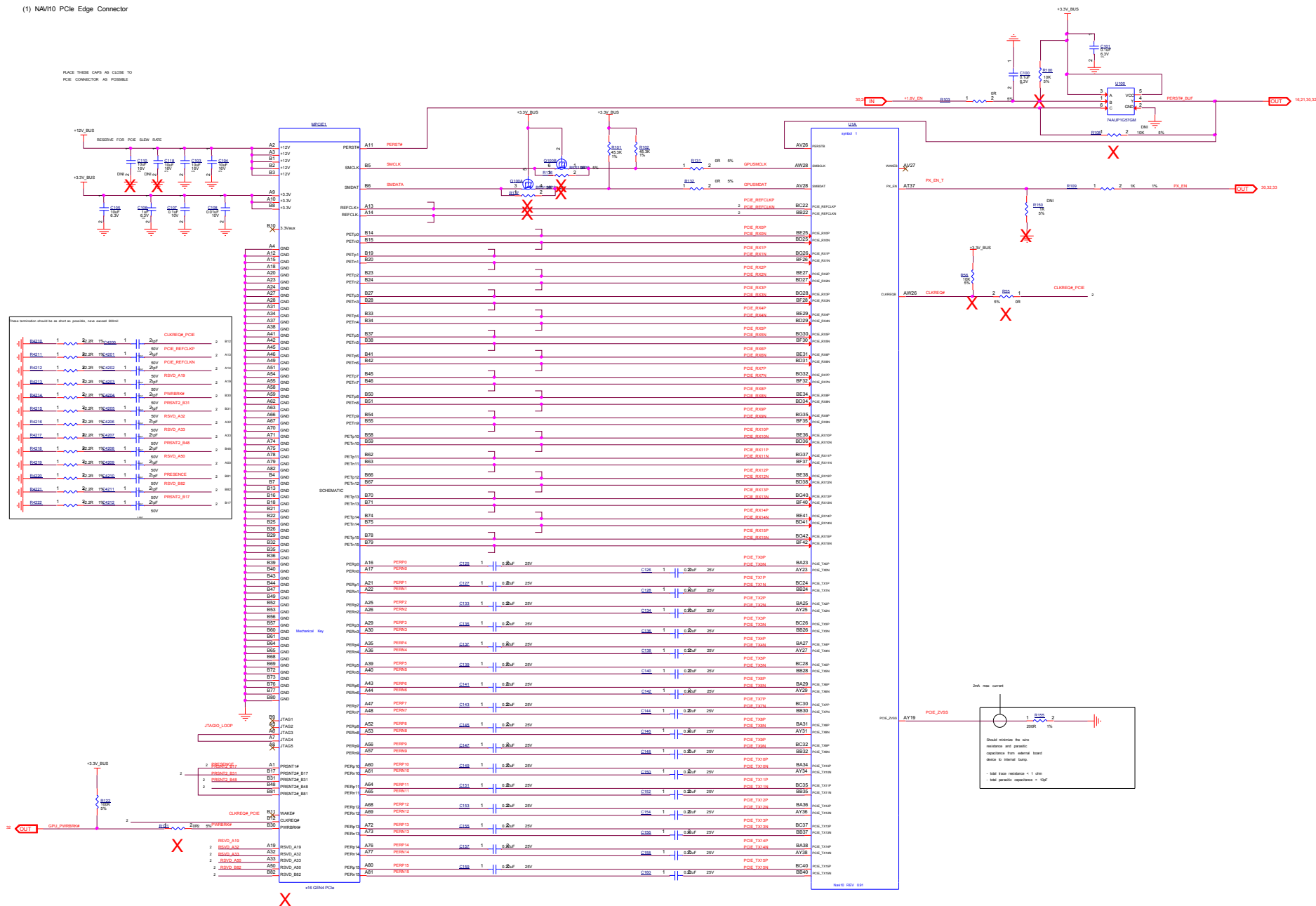


TABLE OF CONTENTS

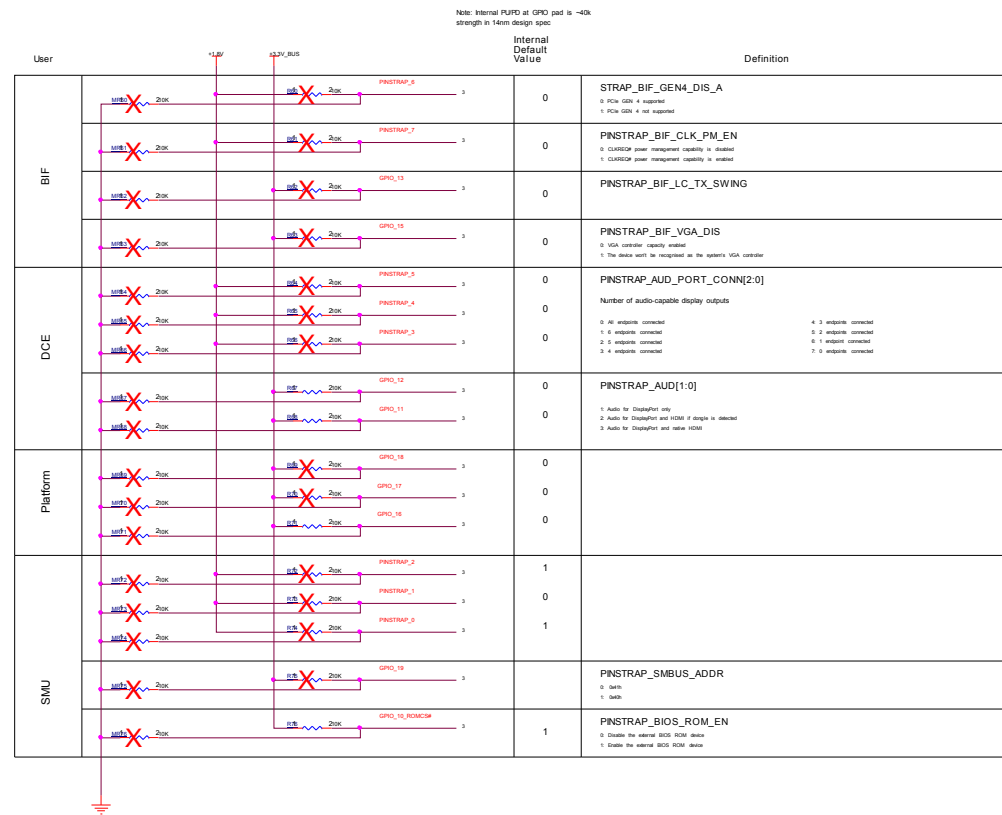
SHEET NO.	SHEET NAME	SHEET NO.	SHEET NAME
1	TOC	26	SMALL RAIL REGULATORS
2	NAV110 PCIe Interface	27	NAV110 DECAPS
3	NAV110 GPIOs	28	NAV110 POWER
4	NAV110 XTAL	29	NAV110 GND
5	NAV110 MEM CHAB	30	POWER MANAGEMENT
6	NAV110 MEM CHCD	31	SVR2 & BAMACO
7	NAV110 MEM CHEF	32	MECHANICAL & THERMAL
8	NAV110 MEM CHGH	33	DEBUG
9	GDDR6 MEM CHAB	34	BLOCK DIAGRAM
10	GDDR6 MEM CHCD	35	REVISION HISTORY
11	GDDR6 MEM CHEF		
12	GDDR6 MEM CHGH		
13	NAV110 TMDPA - DP		
14	NAV110 TMDPC - HDMI		
15	NAV110 TMDPEF - DP DP		
16	GFX & SOC CONTROLLER		
17	VDDCR_GFX PHASES 2 and 5		
18	VDDCR_GFX PHASES 1 and 4		
19	VDDCR_GFX PHASES 3 and 7		
20	VDDCR_GFX PHASES 6 and VDDCR_SOC		
21	MVDD_VDDCI CONTROLLER		
22	REG MVDD		
23	REG VDDCI		
24	REG 0.75V		
25	REG 1.8V		

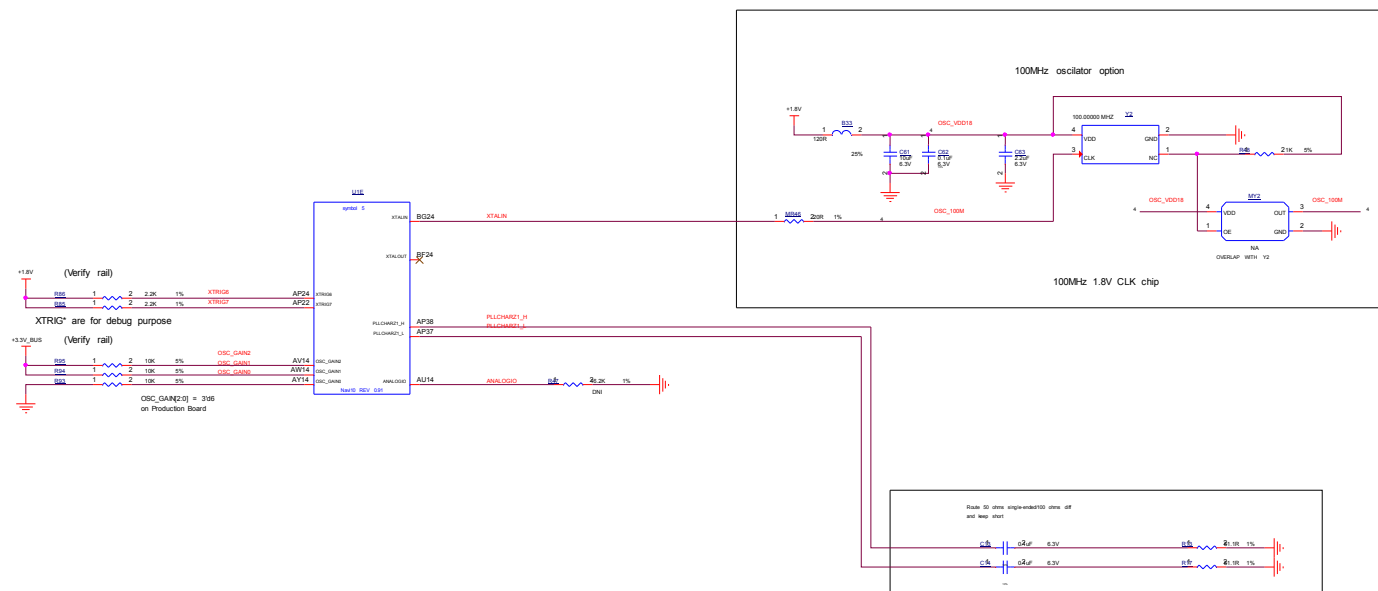
(1) NAVI10 PCIe Edge Connector

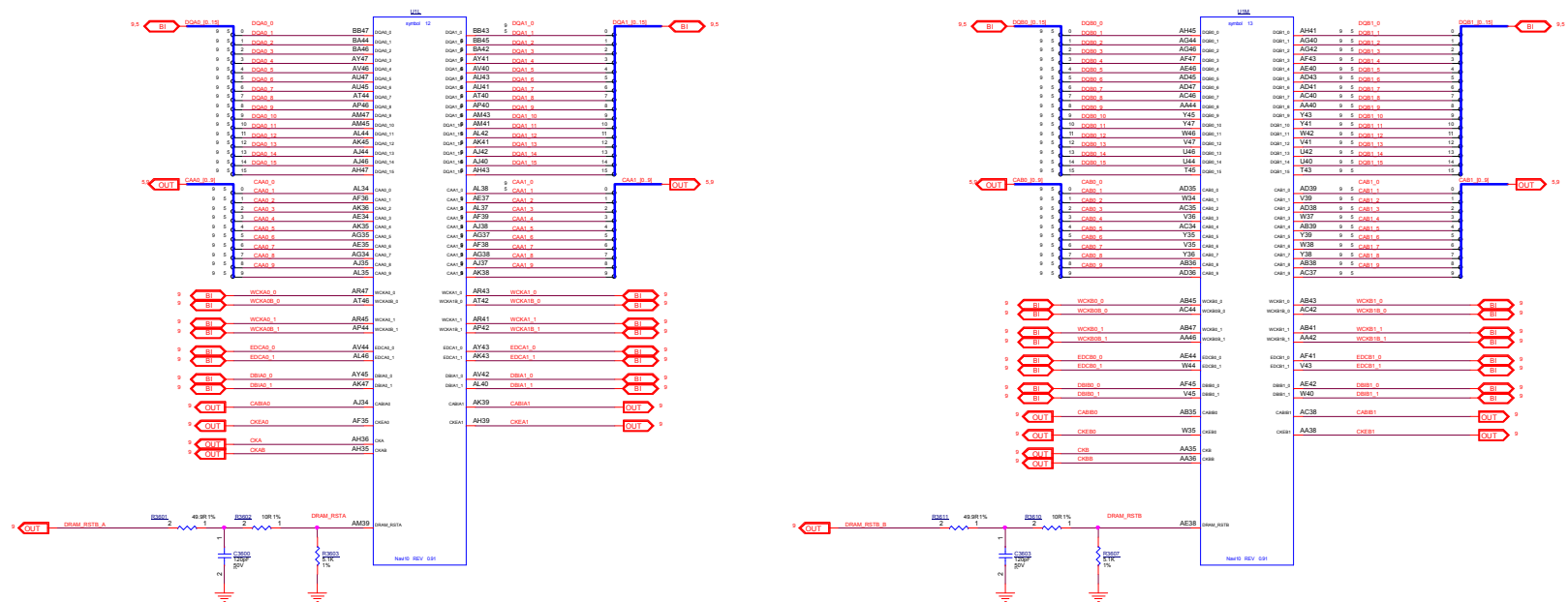
PLACE THESE CAPS AS CLOSE TO
PCI-E CONNECTOR AS POSSIBLE



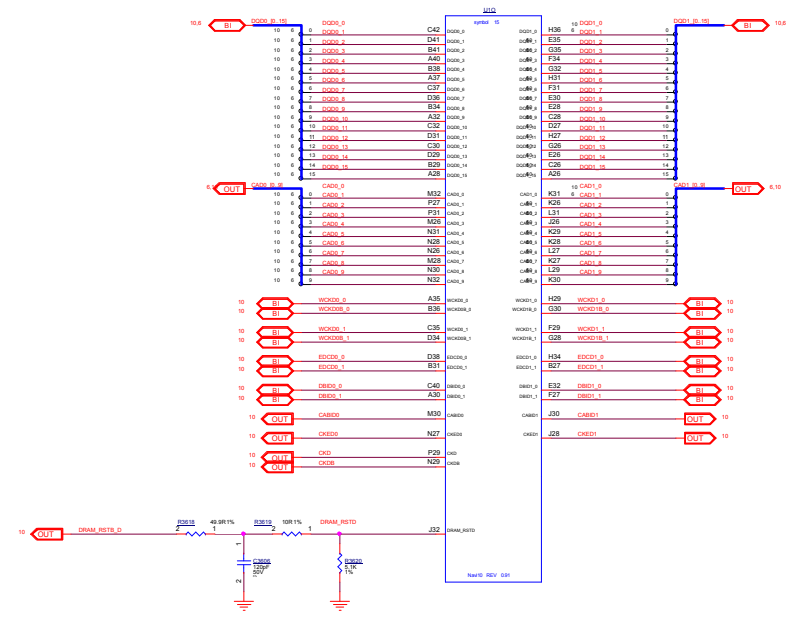
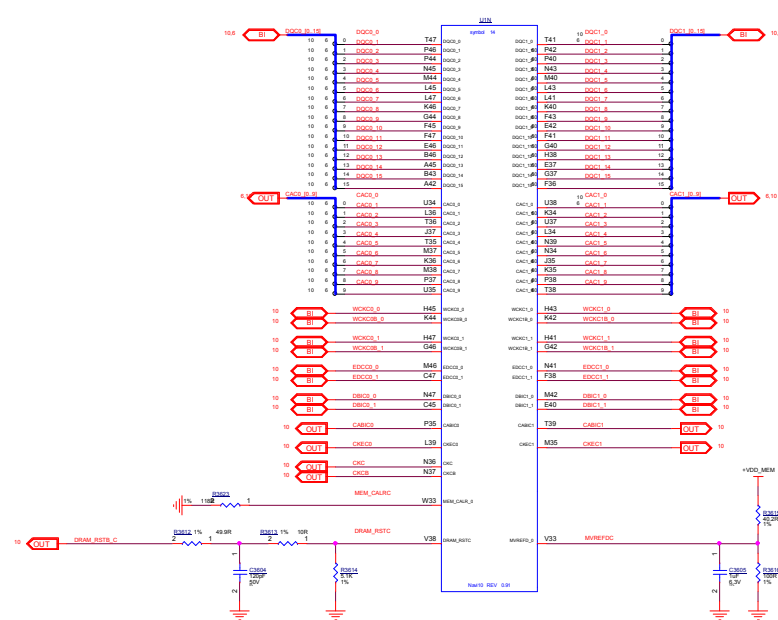
SYMBOL LEGEND	
DO	DO NOT INSTALL
S or P	ACTIVE LOW
BUO	BRING UP ONLY
	DIGITAL GROUND
	ANALOG GROUND

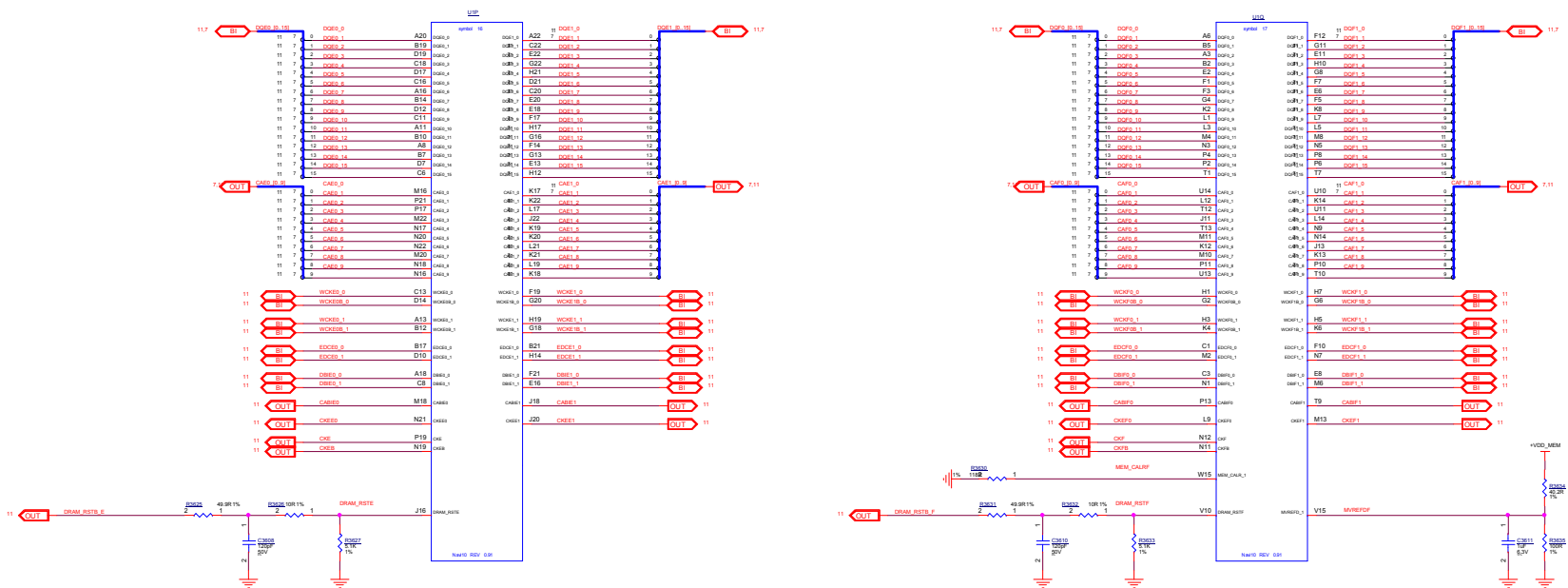




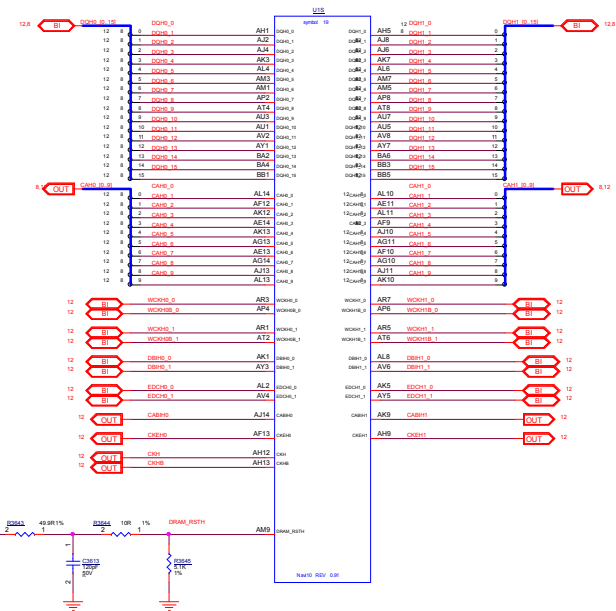
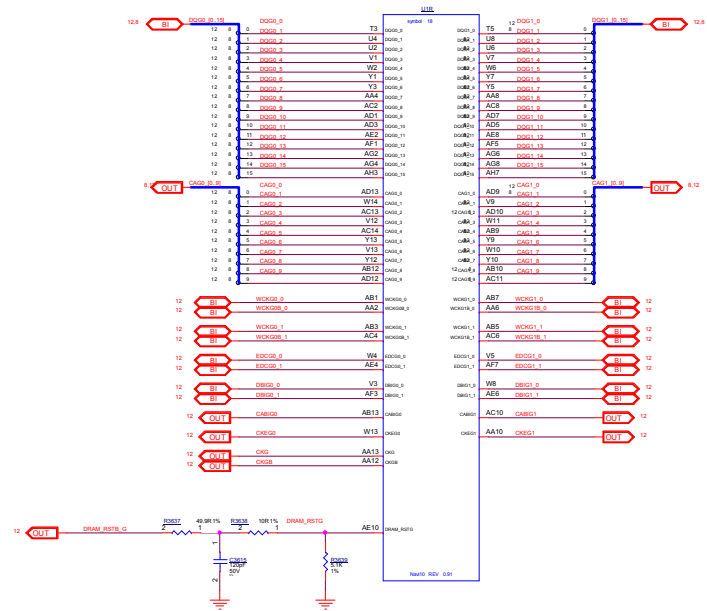


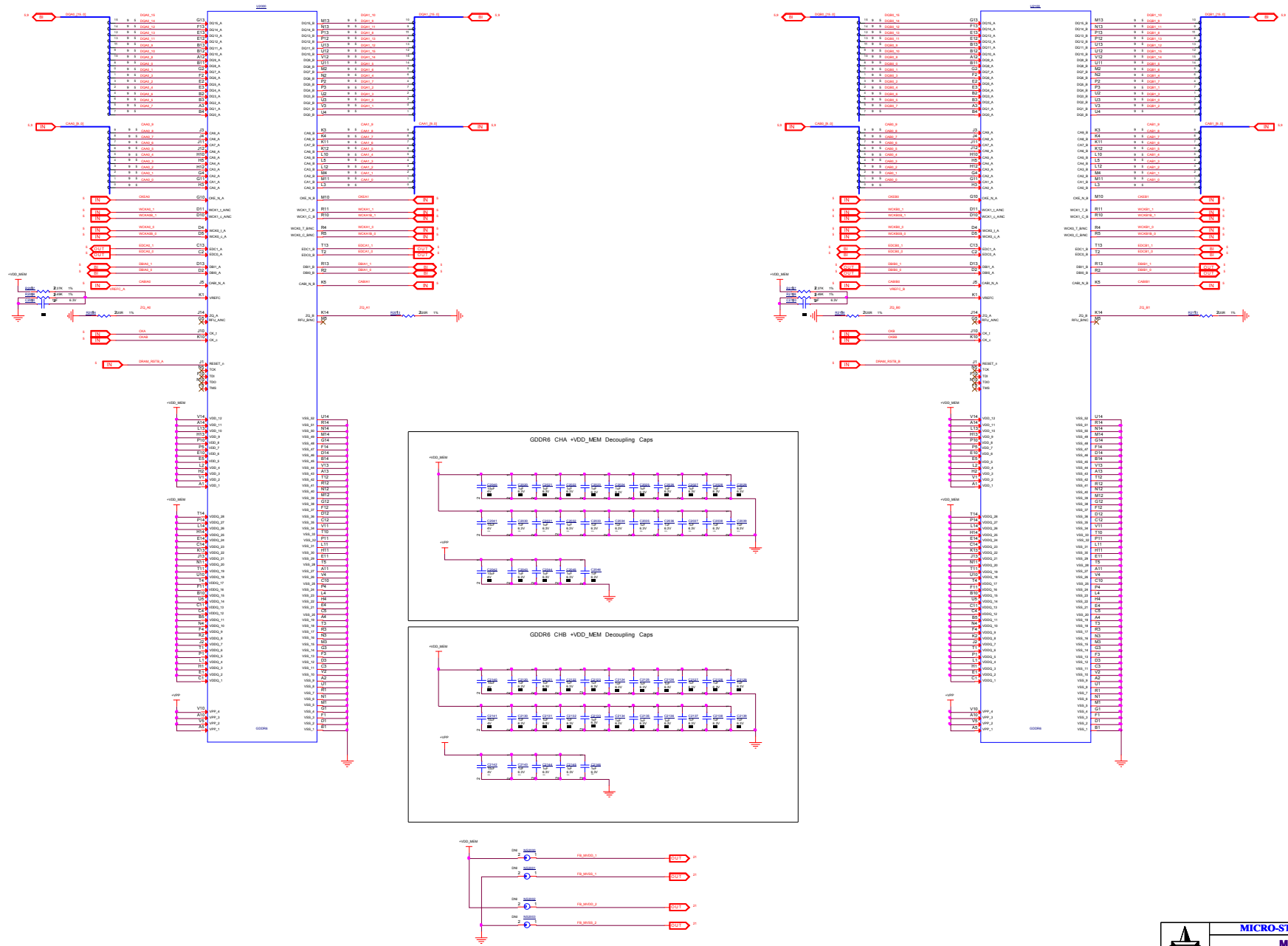
NAVI 10 MEM INTERFACE CH C/D

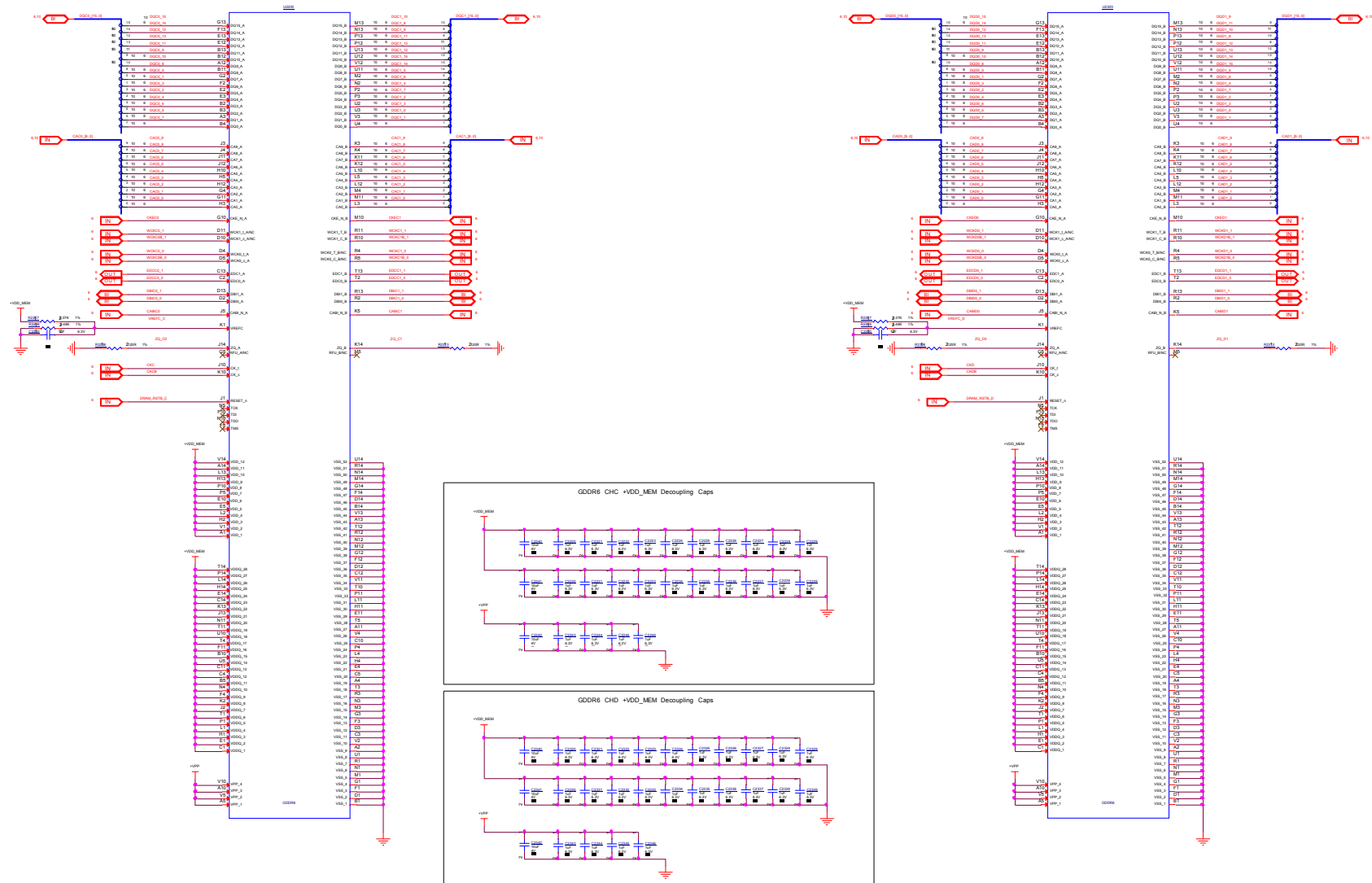


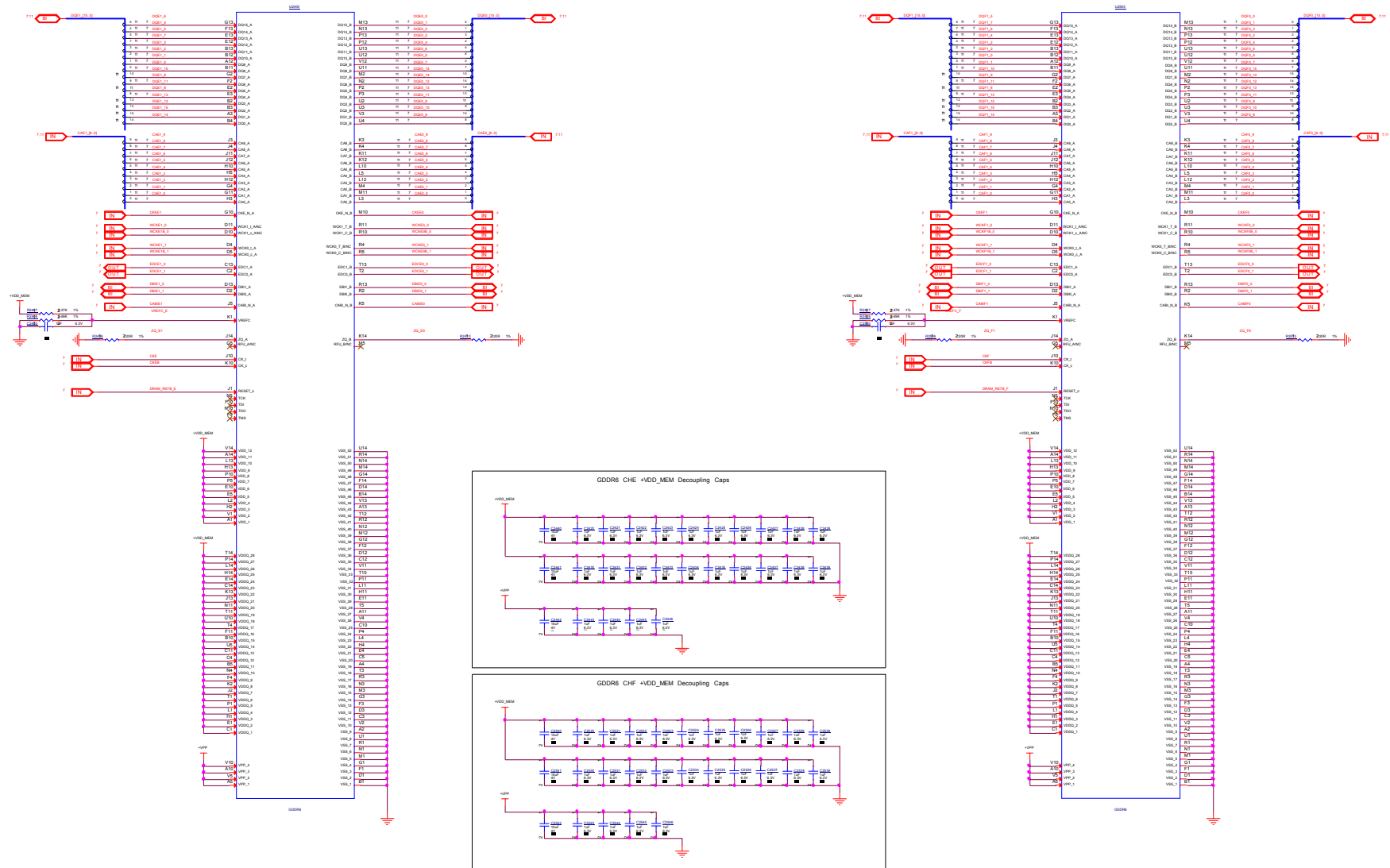


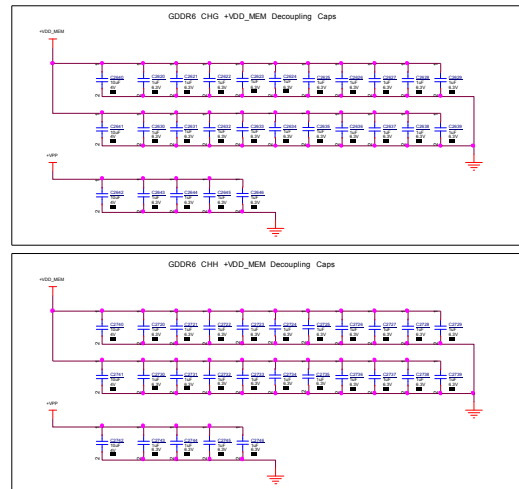
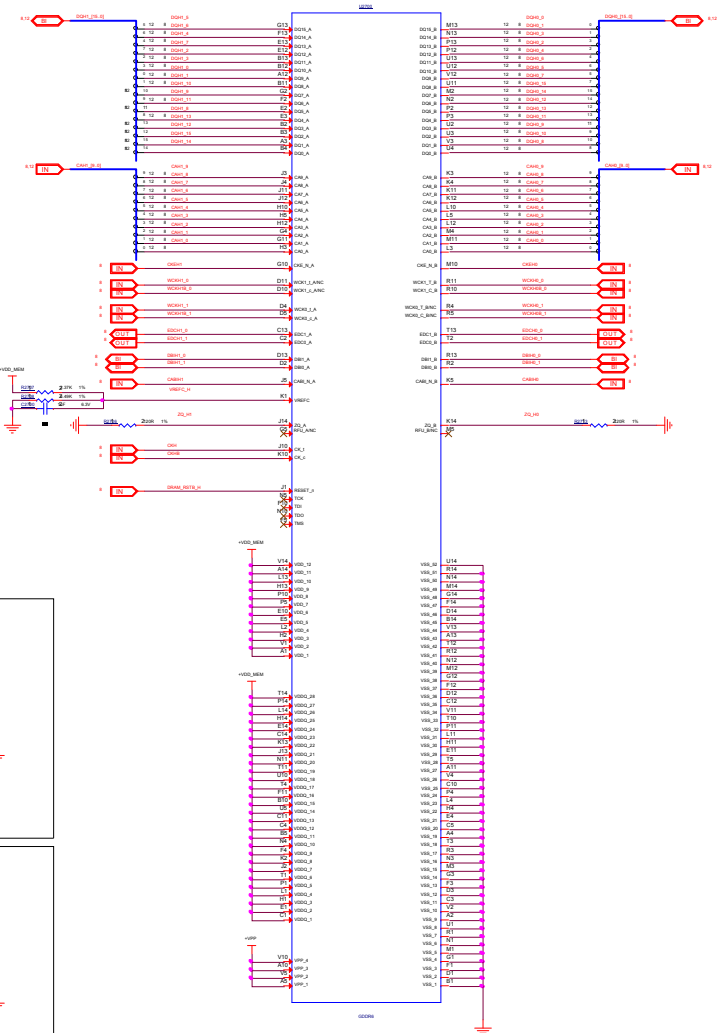
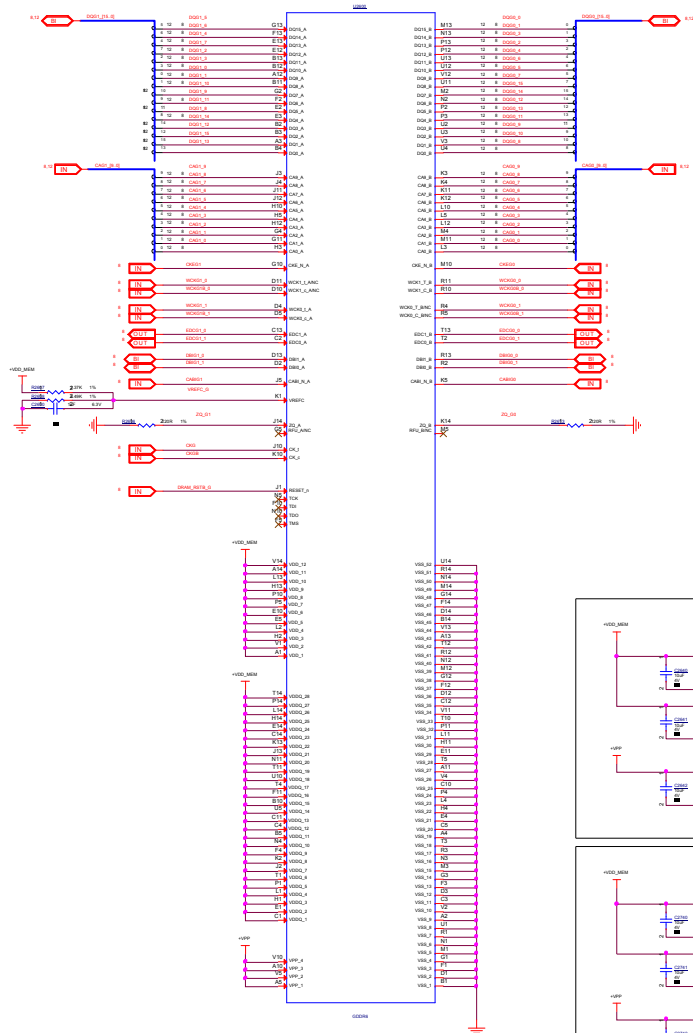
NAVI 10 MEM INTERFACE CH G/H

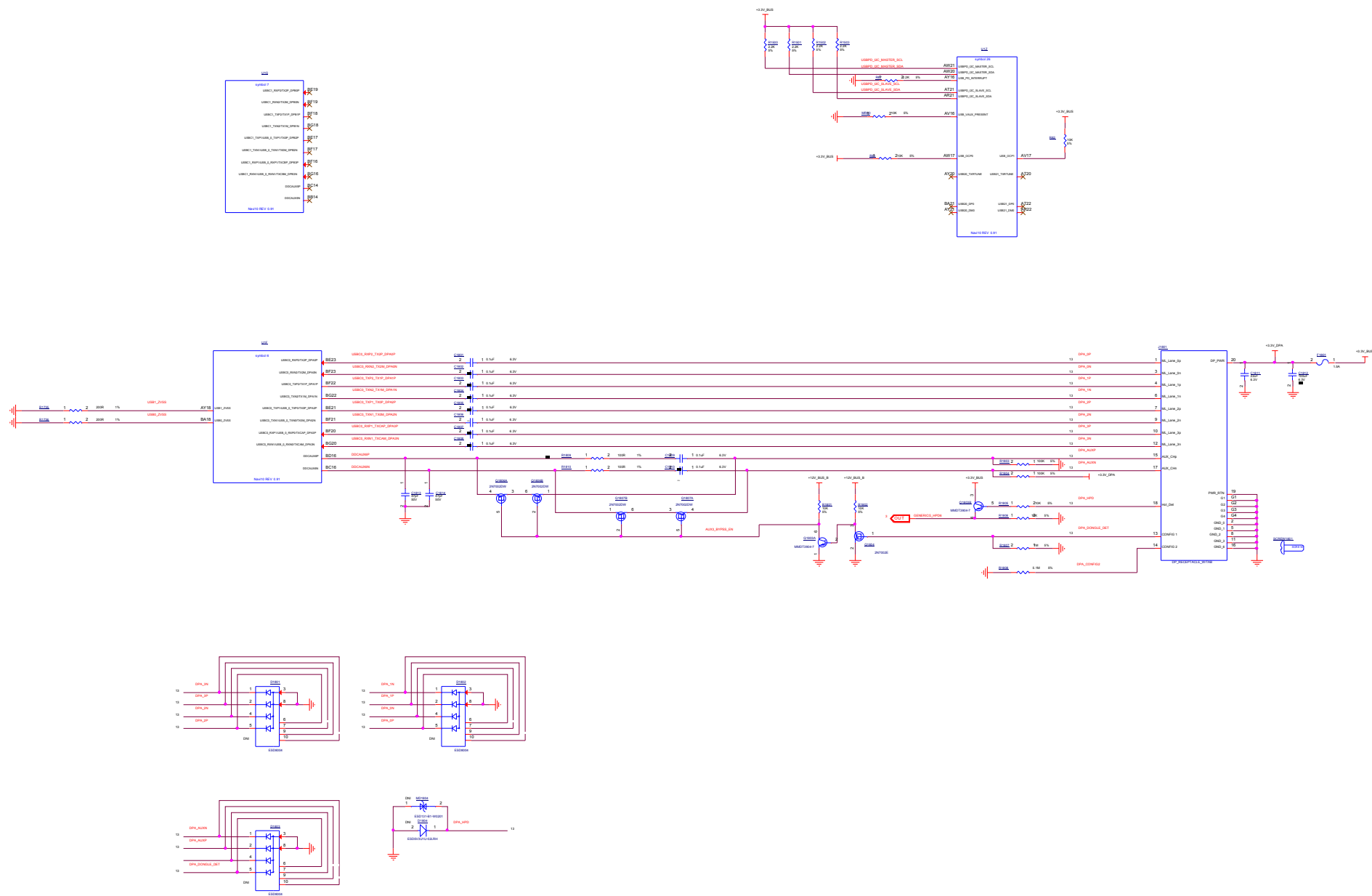


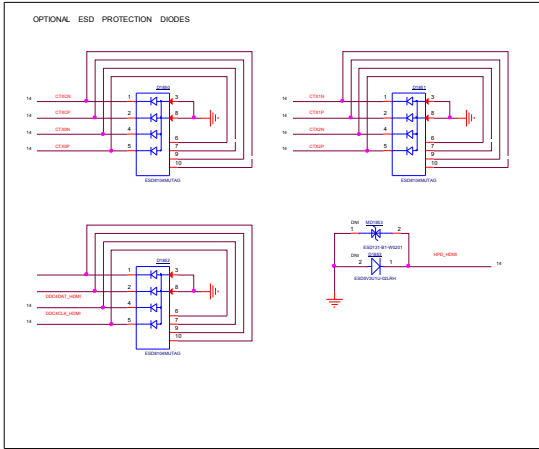
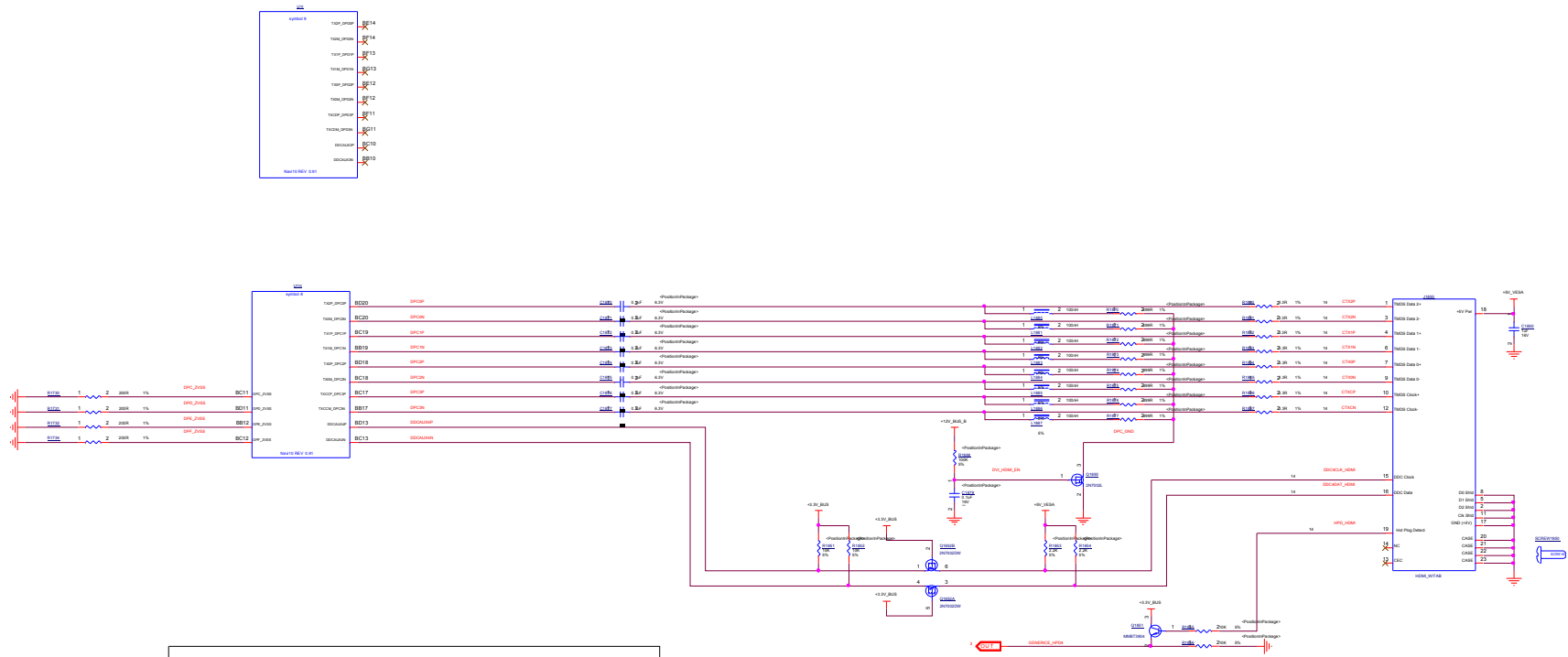




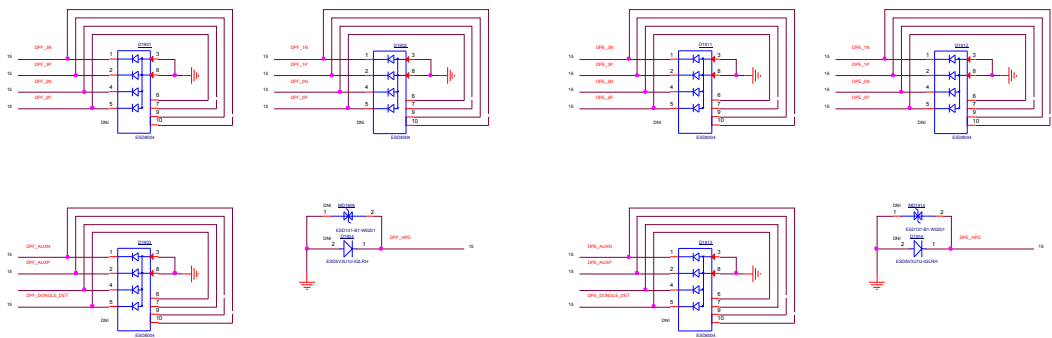
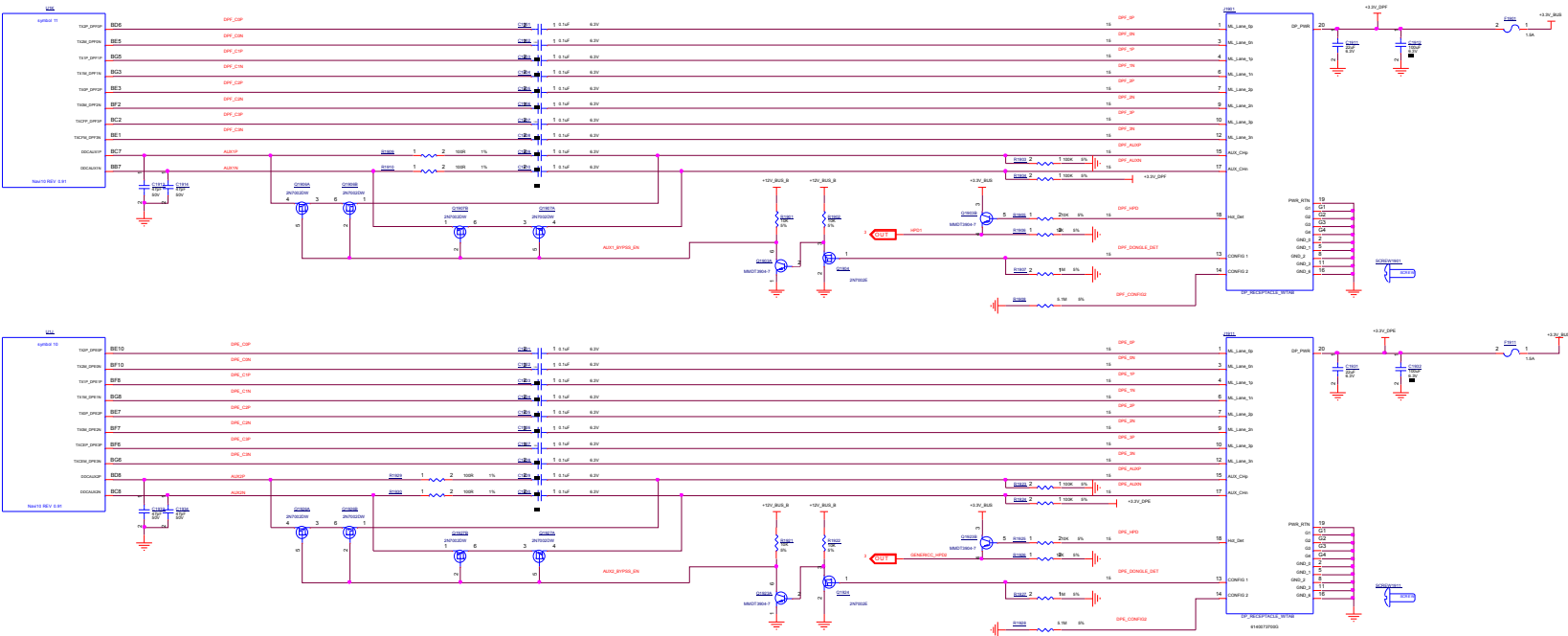


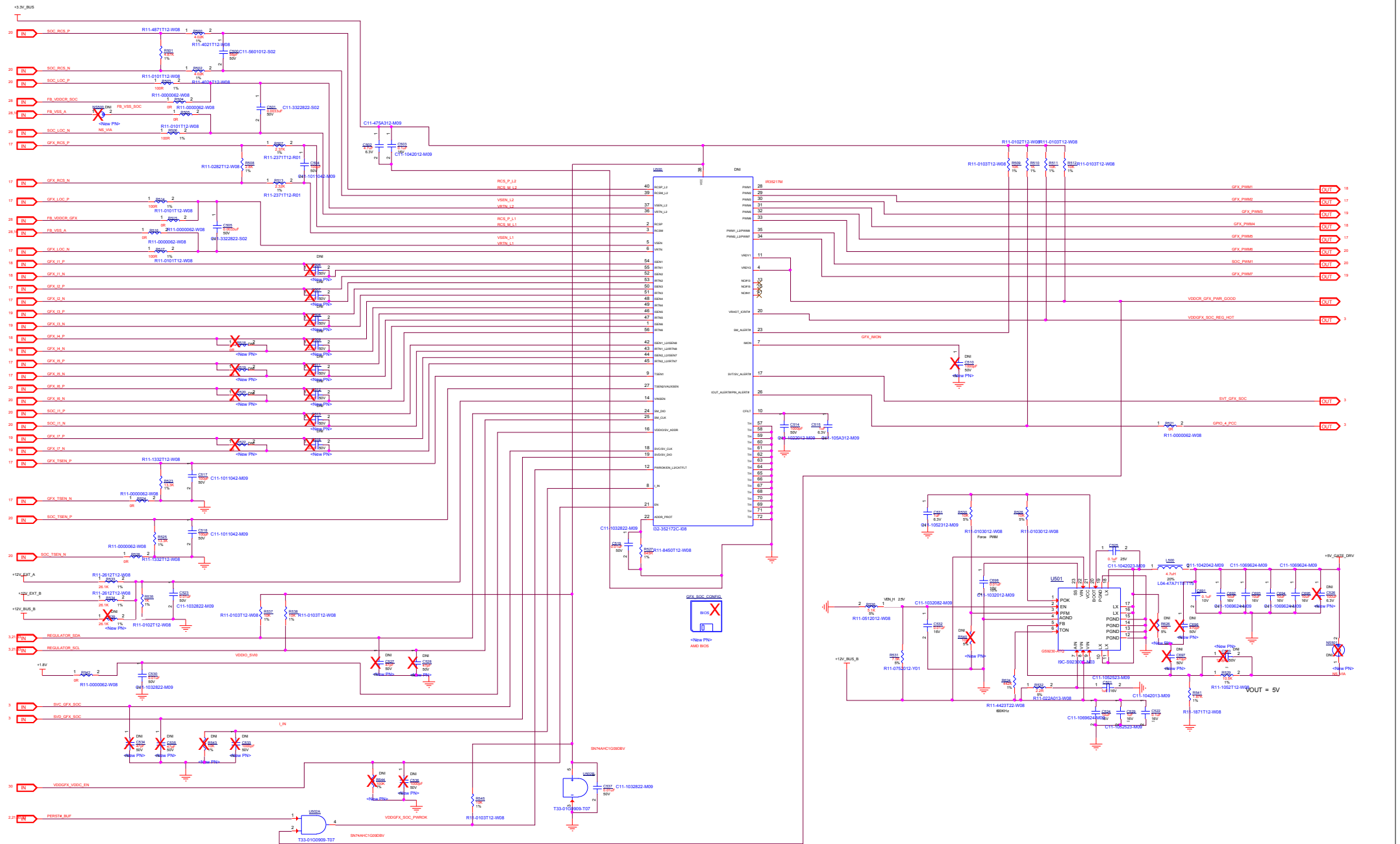


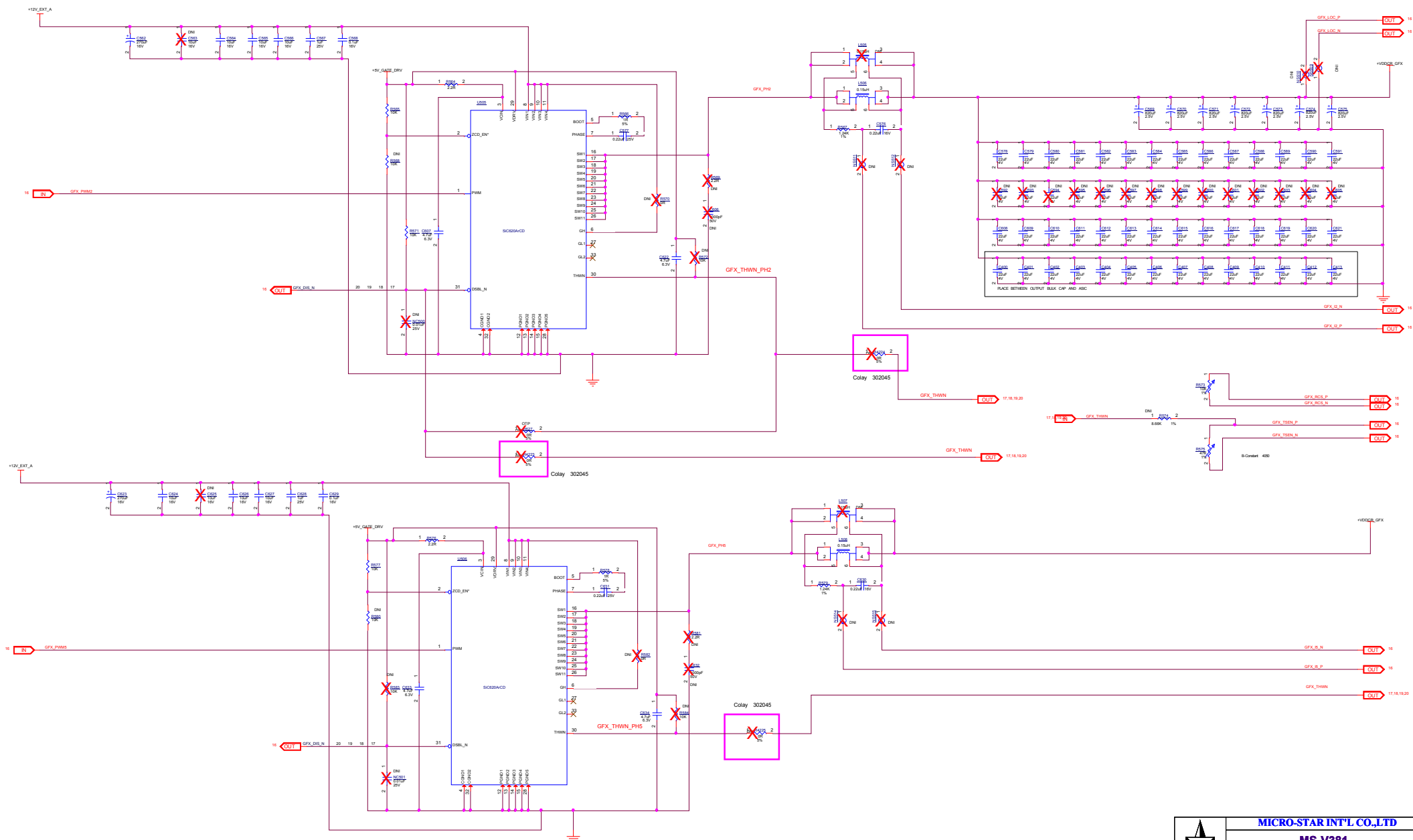


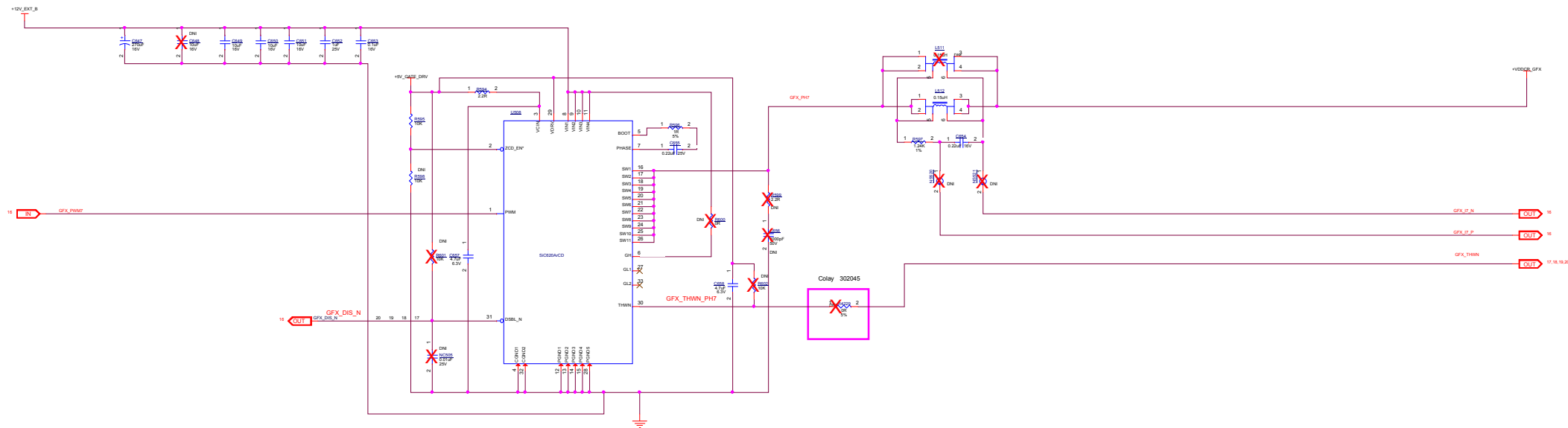
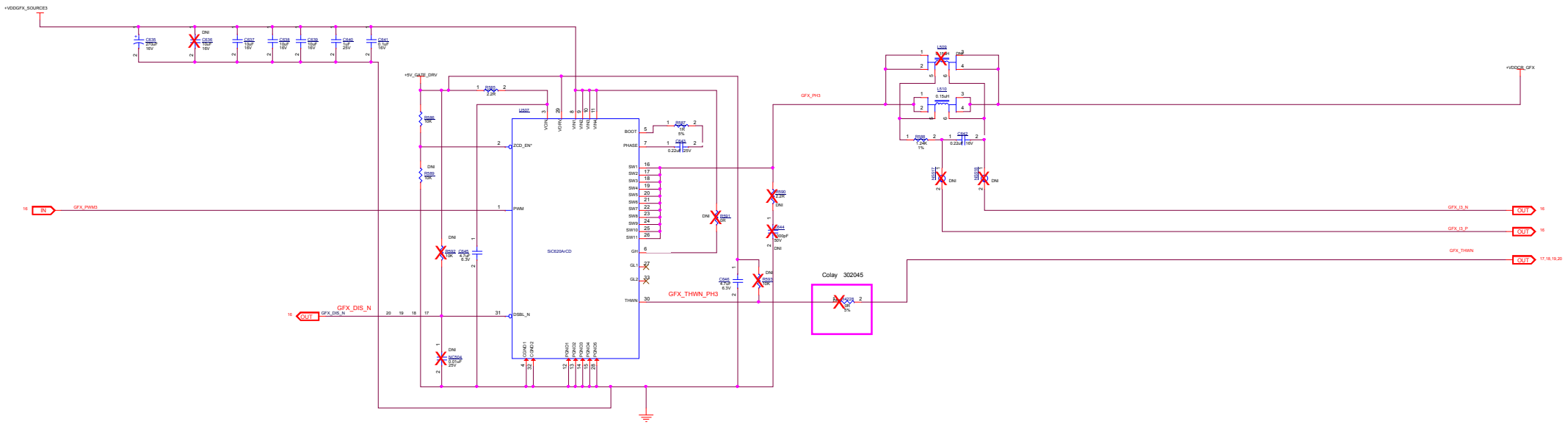


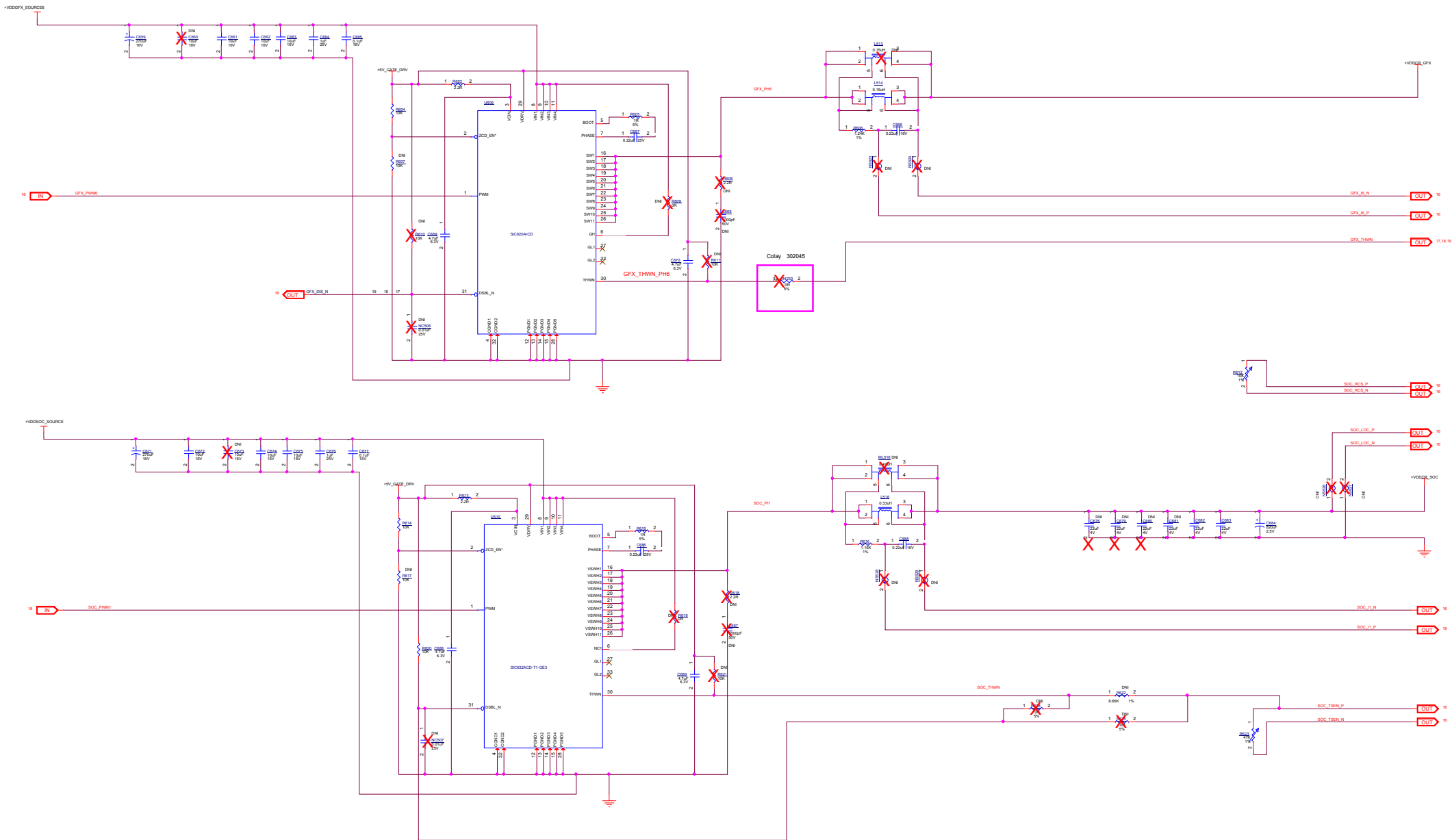
(9) NAVI10 TMDP E/F

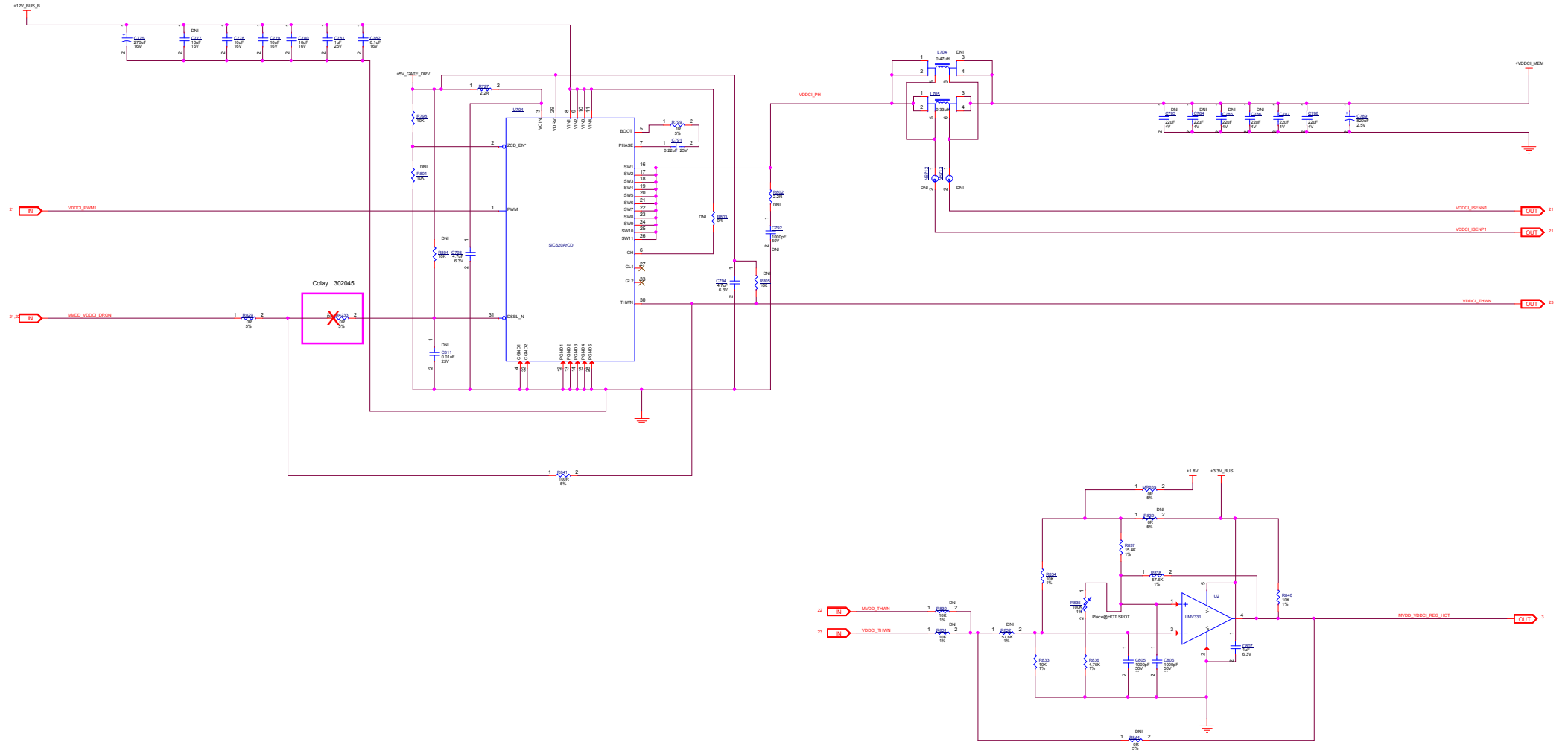


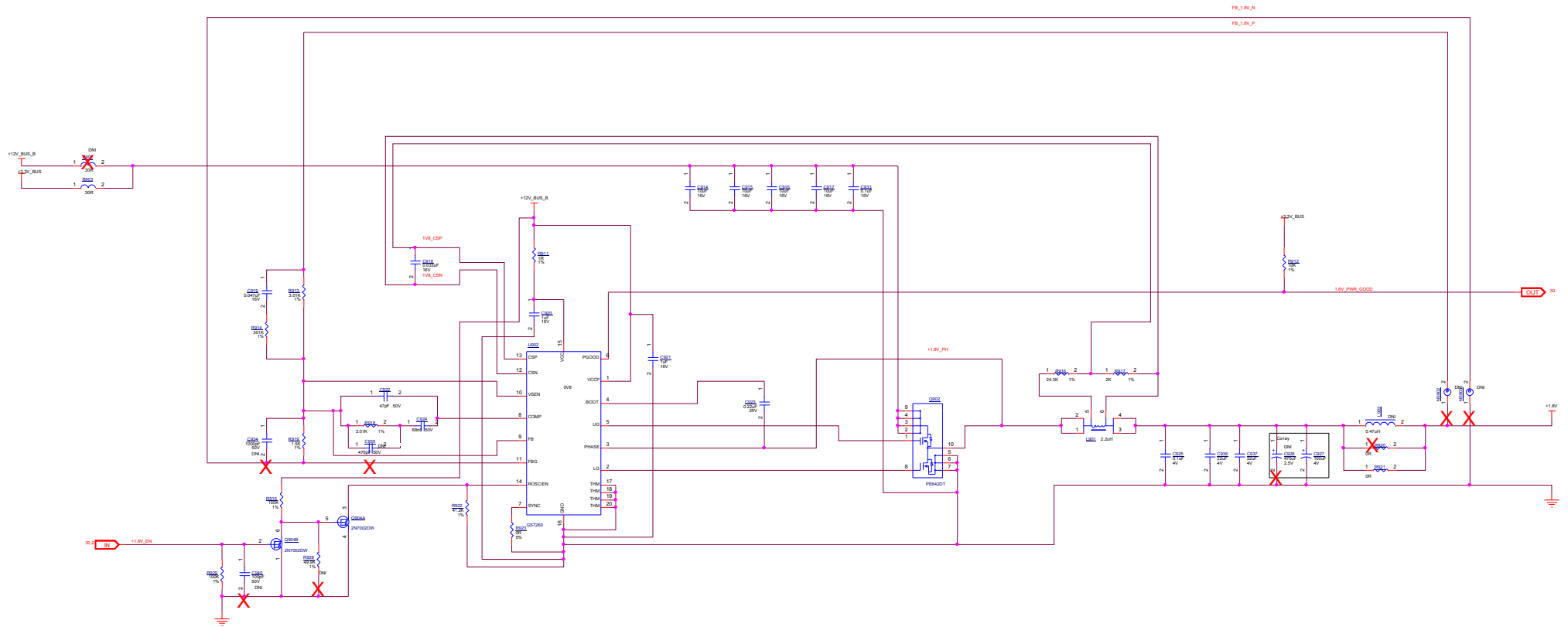




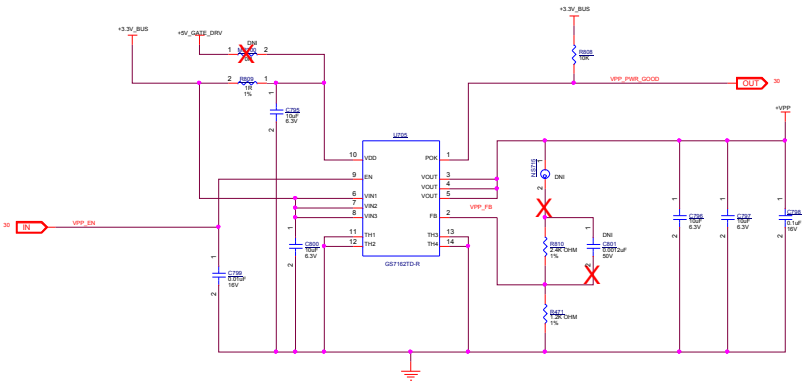
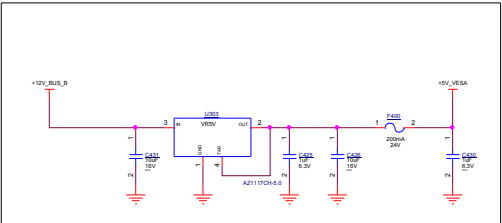


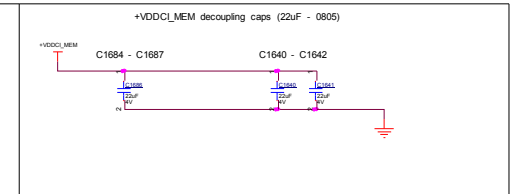
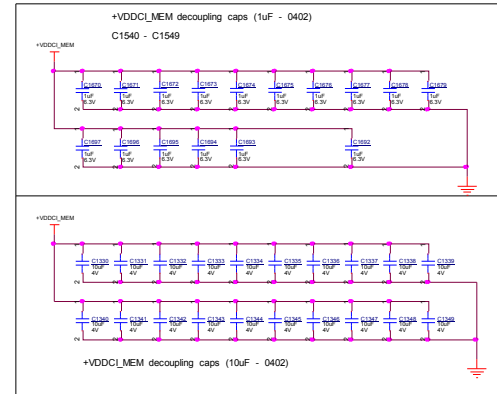
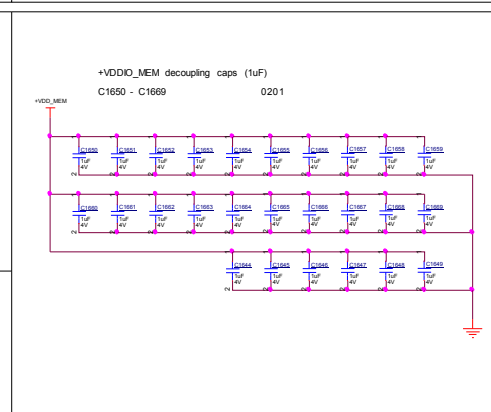
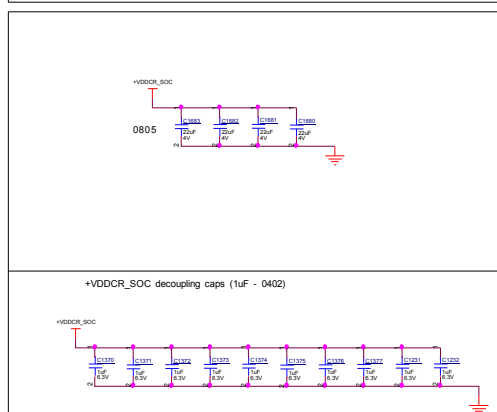
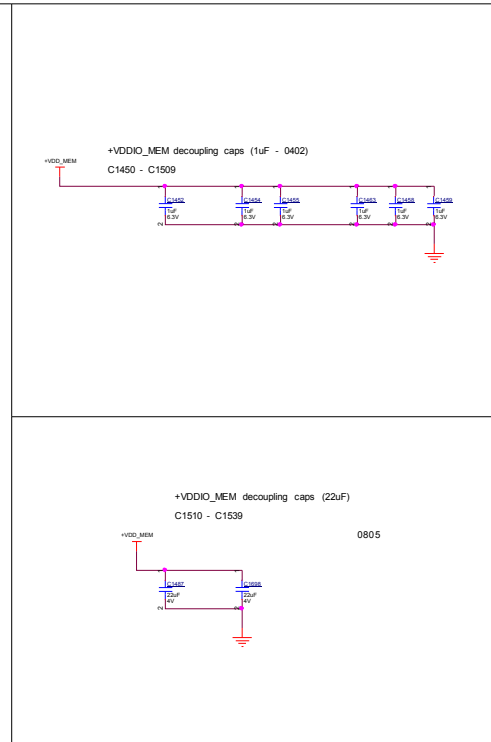
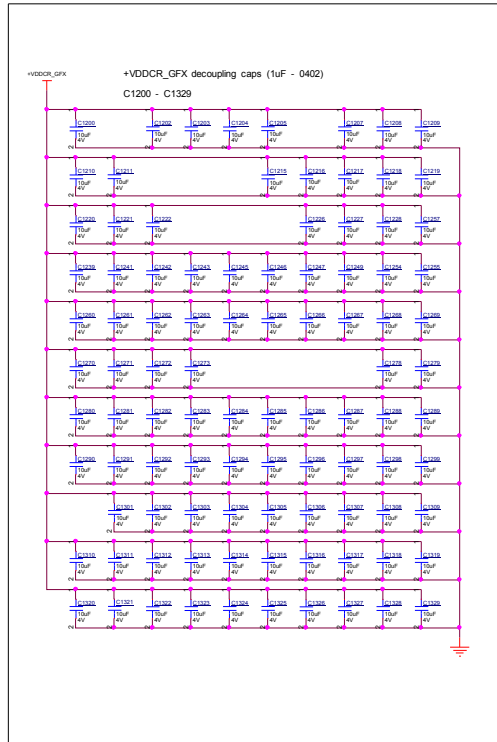




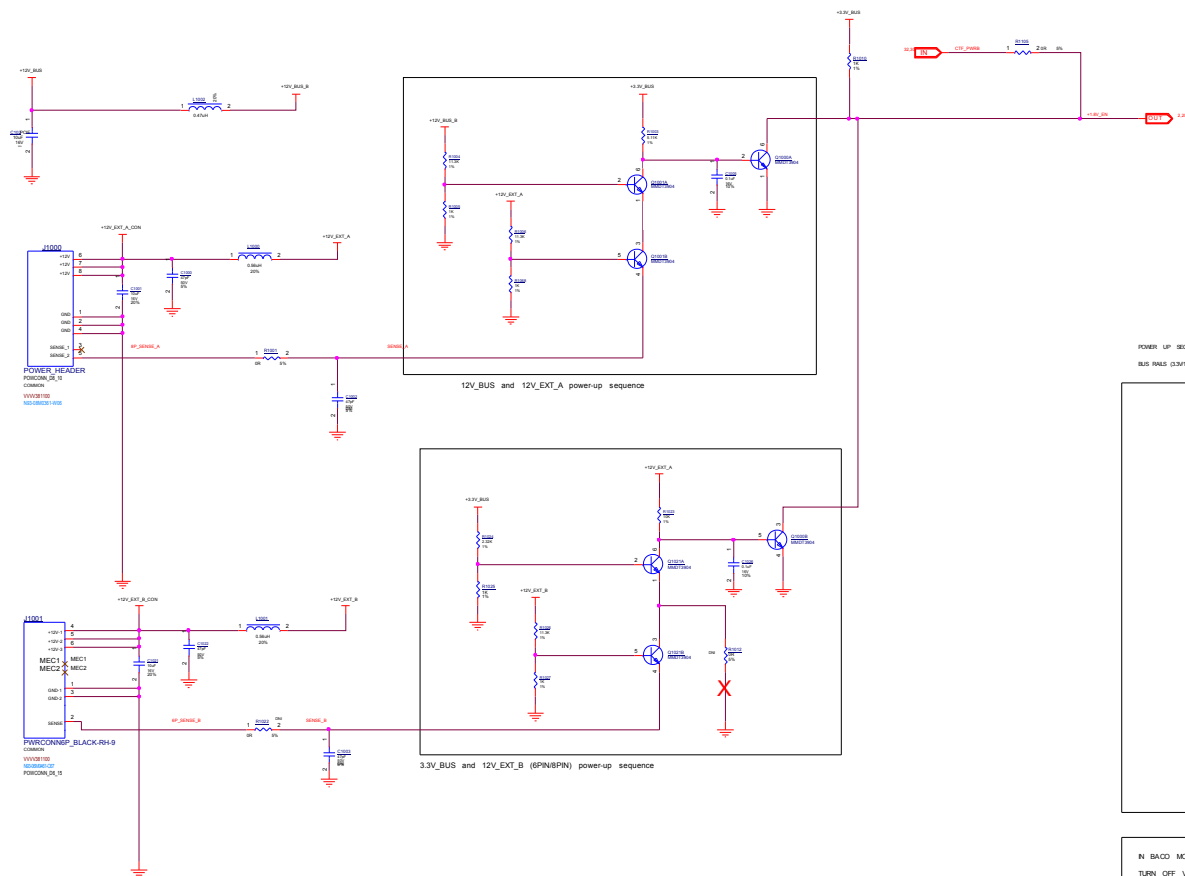


REGULATOR FOR +5V Rails
IOUT = 50mA

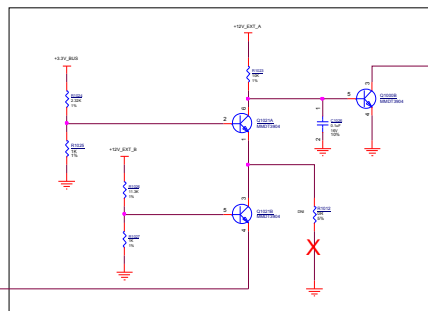




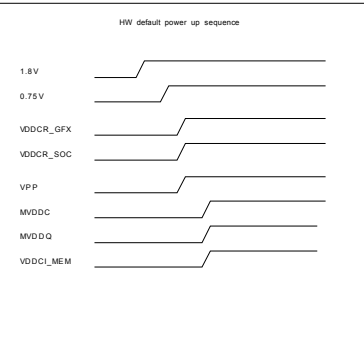
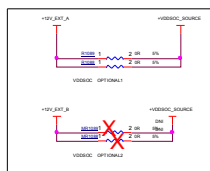
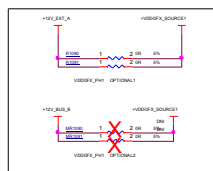
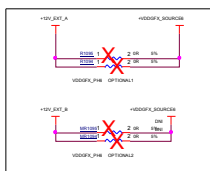
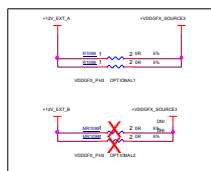




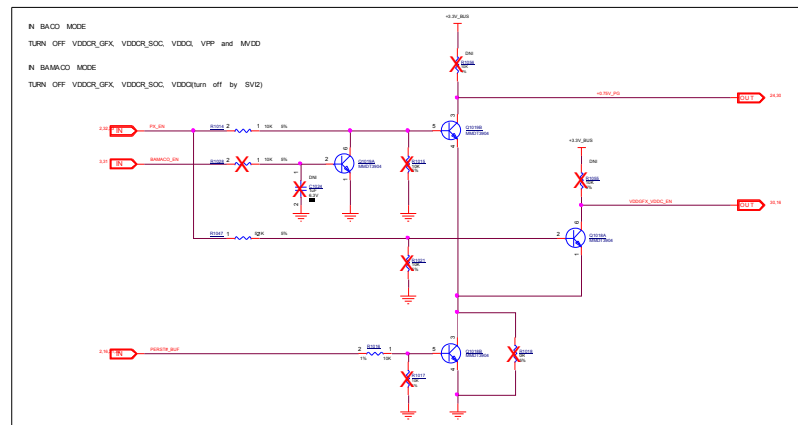
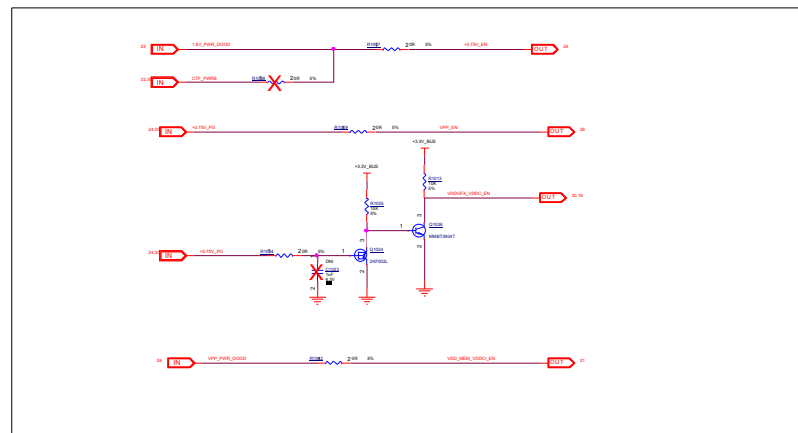
12V_BUS and 12V_EXT_A power-up sequence



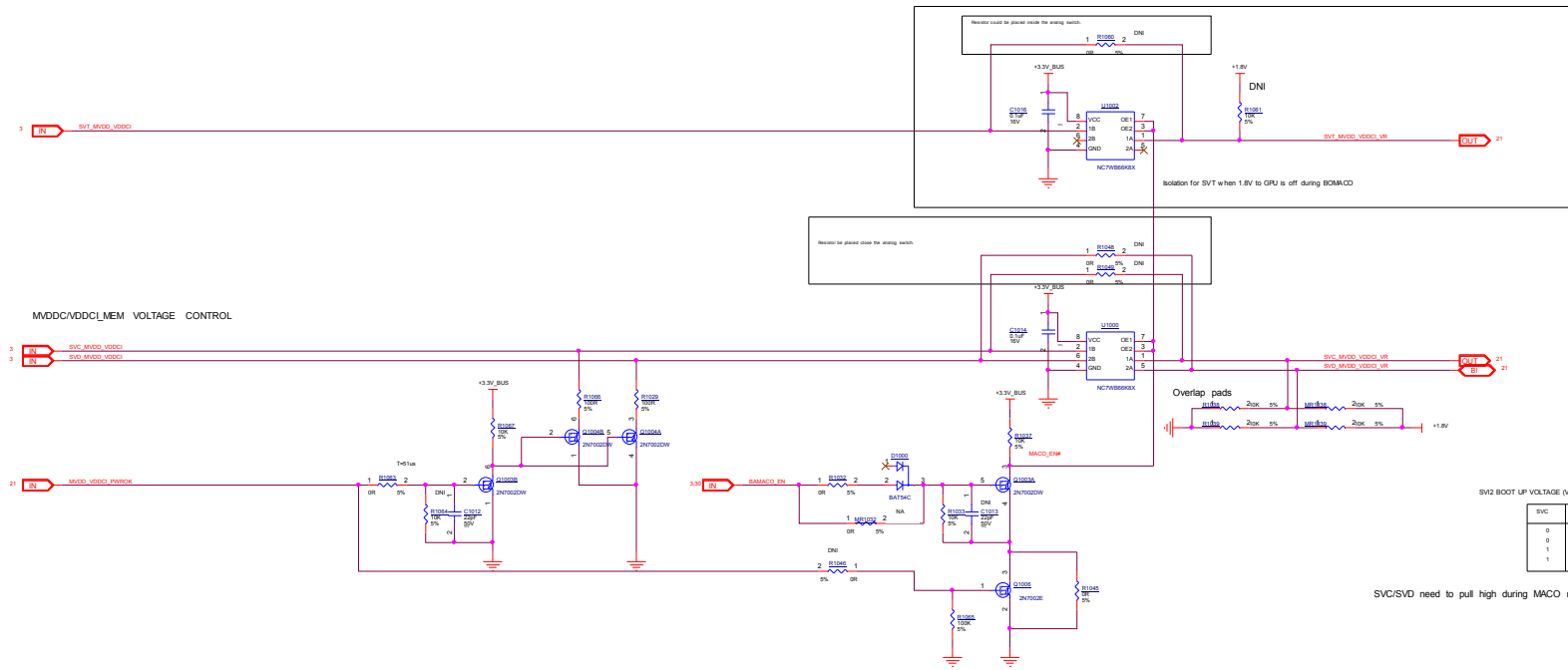
3.3V_BUS and 12V_EXT_B (6PIN/8PIN) power-up sequence



POWER UP SEQUENCE
BUS RAILS (3.3V/12V UP) → +1.8V → 0.75V → VDDCR_GFX/SOC
→ VPP → VDDCI_MEM



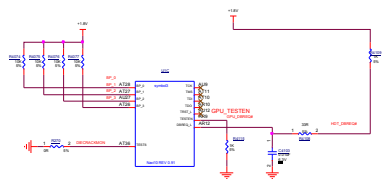
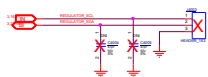
IN BACD MODE
TURN OFF VDDCR_GFX, VDDCR_SOC, VDDCI, VPP and MVDCC
IN BAMAQ MODE
TURN OFF VDDCR_GFX, VDDCR_SOC, VDDCI (turn off by SW)



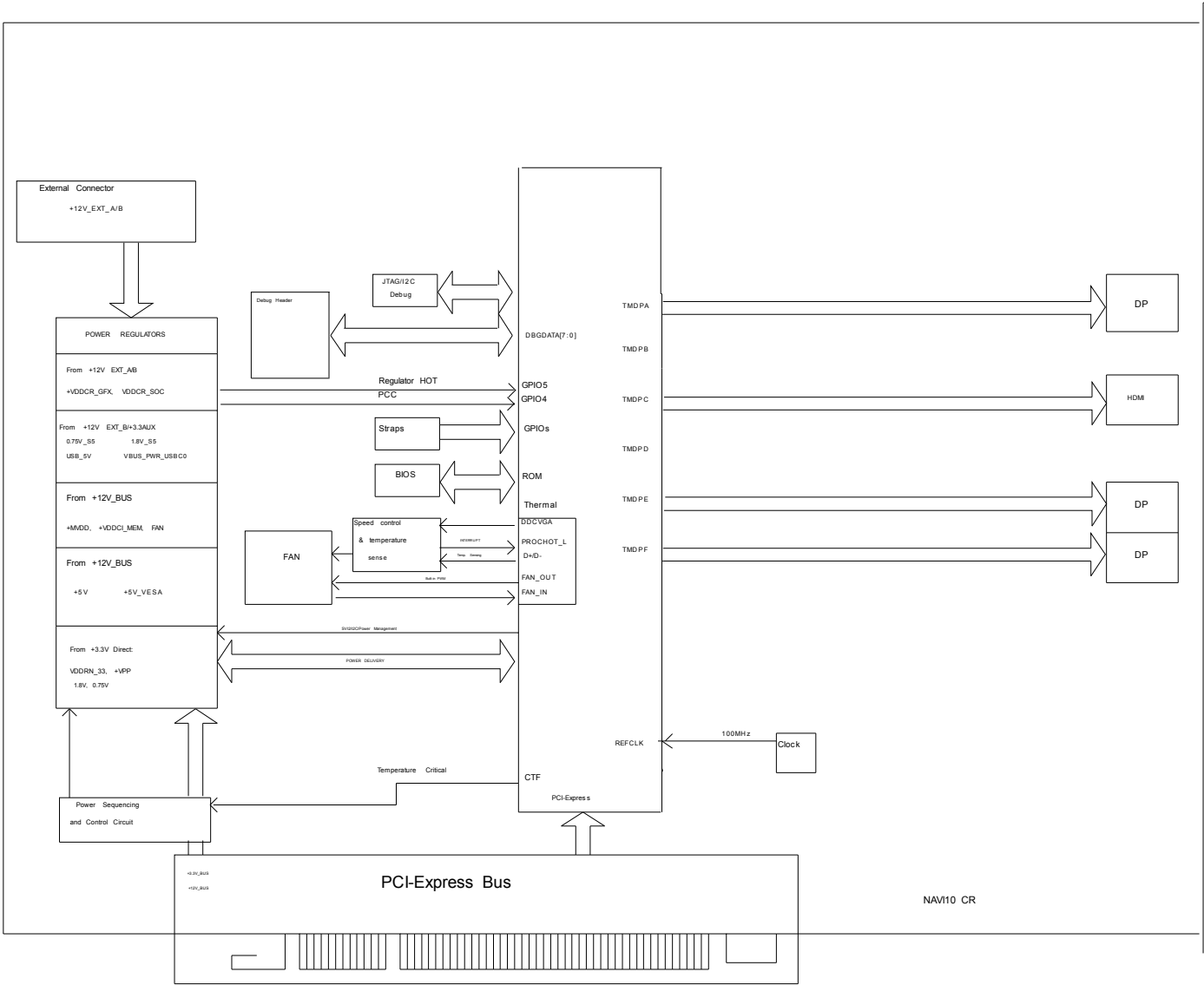
SV2 BOOT UP VOLTAGE (VDDQ_MEM/MVDD)

SVC	SVD	VOLTAGE
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

SVC/SVD need to pull high during MACO mode



RADEON Lightbar header



8		7		6		5		4		3		2		1	
AMD				TITLE: NAVI10 G6X16mode DP DP HDMI DP		DOCUMENT NUMBER: 106_D199rev_00B		DATE: Fri Jun 21 03:44:58 2019		SHEET NUMBER: 35 OF 35		REV: 1.00			
REVISION HISTORY				ENGINEER: Peak, Dong		NOTES: NOTE		CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES, INC. This AMD-based schematic and design is the exclusive property of AMD, and is provided only to fulfill under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a valid Technology License Agreement with AMD. AMD makes no representation or warranty of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.				AMD - PLATFORM HARDWARE ENG No.669, HUANKE ROAD SHANGHAI, CHINA 201203			
SCH Rev		PCB Rev		Date		REVISION DESCRIPTION									
1		-00A		FEB 11 2019		-00A schematics									
2		-00B		JUN 21 2019		ADD FULL HIGH ON THE PWBERRB									

2019_11_07 GFX_MEM_SOC_VDDCI Co-Lay 302045 and Power PIN fix to 8+6 reverse type Only

2019_11_11 Add Fan_IN output back Page 32, Change Footprint con_dp_astron_r6890020_tab > con_tab , edgecon_pci_express_gen4_16 > edgecon_16 , Remove MT203, MT 211, MT208 Screw Hole

2019_11_14 add Cross Light point , Remove Page 2 TP detect point, Remove lightbar header, Remove CTF & J4100 debug Pin