PRELIMINARY AND SUBJECT TO CHANGE

TABLE OF CONTENTS

Sapphire Tech

6F , No.18, WenHu Street , NeiHu District , Taipei City, 114, Taiwan

Title

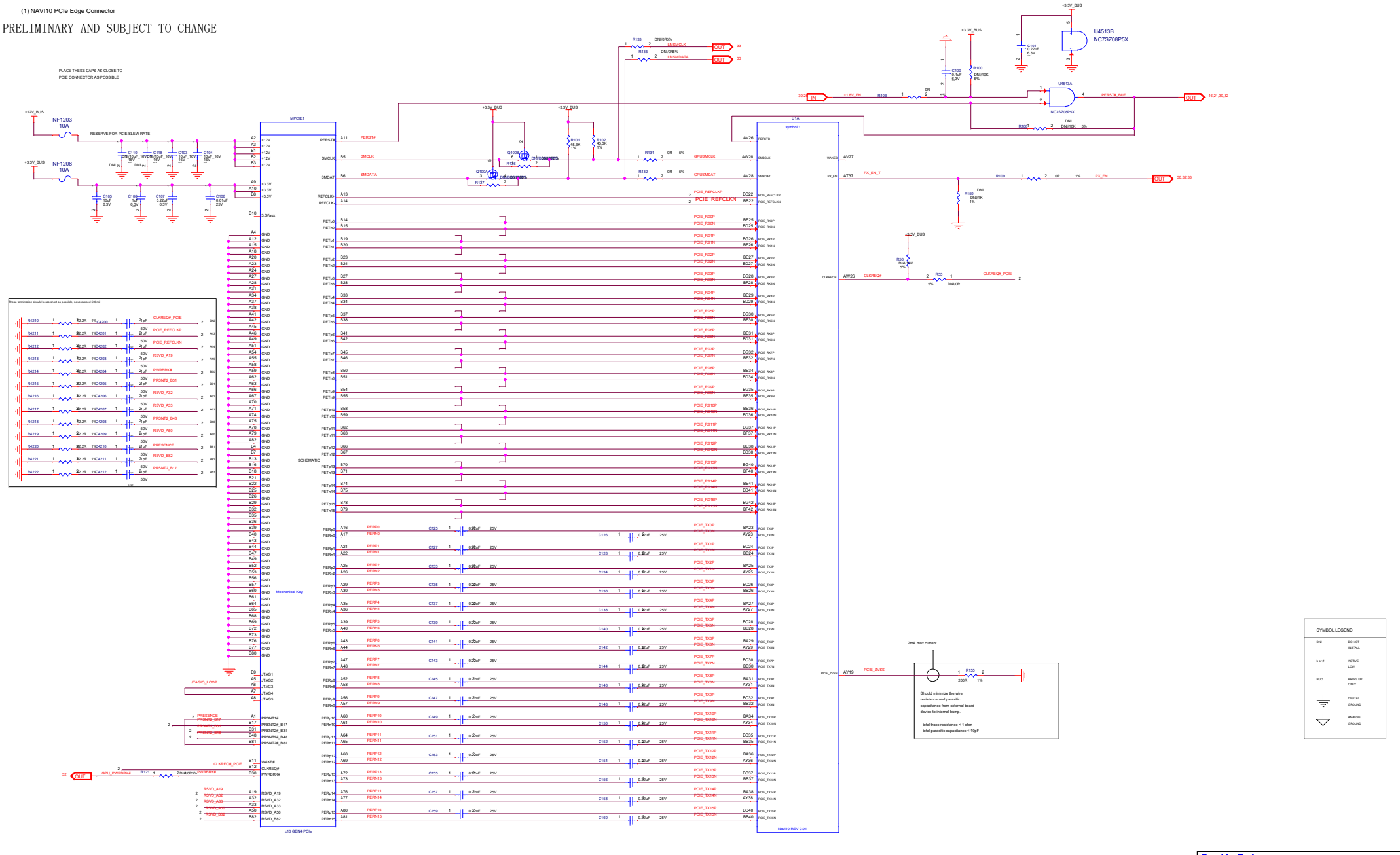
Page 01. TABLE OF CONTENTS

Size	Document Number	Rev
Custom	E411-00_FINAL	00

Date: Tuesday, June 11, 2019 Sheet 1 of 35

(1) NAVI10 PCIe Edge Connector

PRELIMINARY AND SUBJECT TO CHANGE



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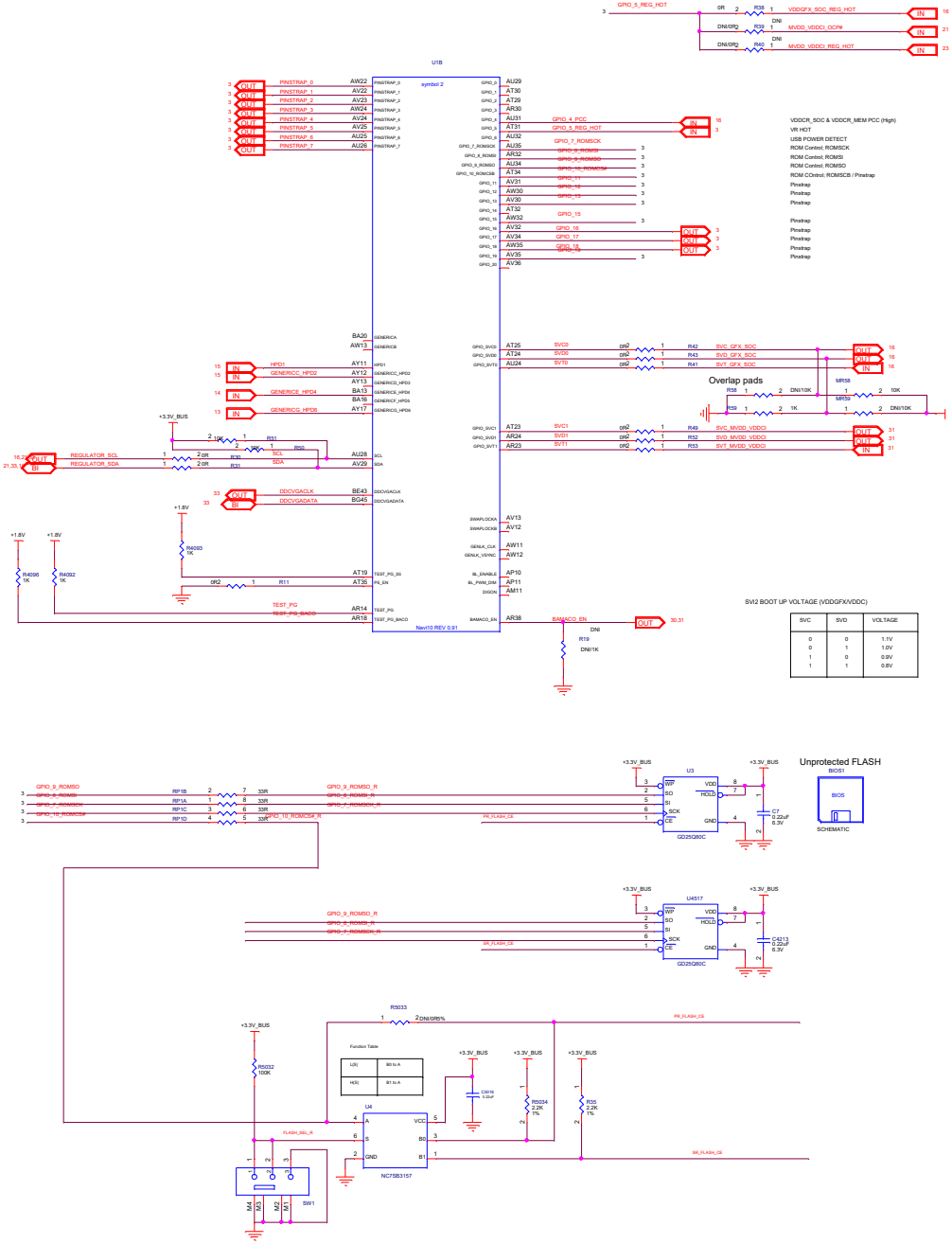


Note: Internal PU/PD at GPIO pad is ~40k
strength in 14nm design spec

User		Internal Default Value	Definition
BIF	MR60	0	STRAP_BIF_GEN4_DIS_A 0: PCIe GEN 4 supported 1: PCIe GEN 4 not supported
	MR61	0	PINSTRAP_BIF_CLK_PM_EN 0: CLKREQ# power management capability is disabled 1: CLKREQ# power management capability is enabled
	MR62	0	PINSTRAP_BIF_LC_TX_SWING
	MR63	0	PINSTRAP_BIF_VGA_DIS 0: VGA controller capacity enabled 1: The device won't be recognised as the system's VGA controller
DCE	MR64	0	PINSTRAP_AUD_PORT_CONN[2:0] Number of audio-capable display outputs 0: All endpoints connected 1: 6 endpoints connected 2: 5 endpoints connected 3: 4 endpoints connected 4: 3 endpoints connected 5: 2 endpoints connected 6: 1 endpoint connected 7: 0 endpoints connected
	MR65	0	
	MR66	0	
	MR67	0	PINSTRAP_AUD[1:0] 1: Audio for DisplayPort only 2: Audio for DisplayPort and HDMI if dongle is detected 3: Audio for DisplayPort and native HDMI
	MR68	0	
Platform	MR69	0	
	MR70	0	
	MR71	0	
SMU	MR72	1	
	MR73	0	
	MR74	1	
	MR75		PINSTRAP_SMBUS_ADDR 0: 0x41h 1: 0x40h
	MR76	1	PINSTRAP_BIOS_ROM_EN 0: Disable the external BIOS ROM device 1: Enable the external BIOS ROM device

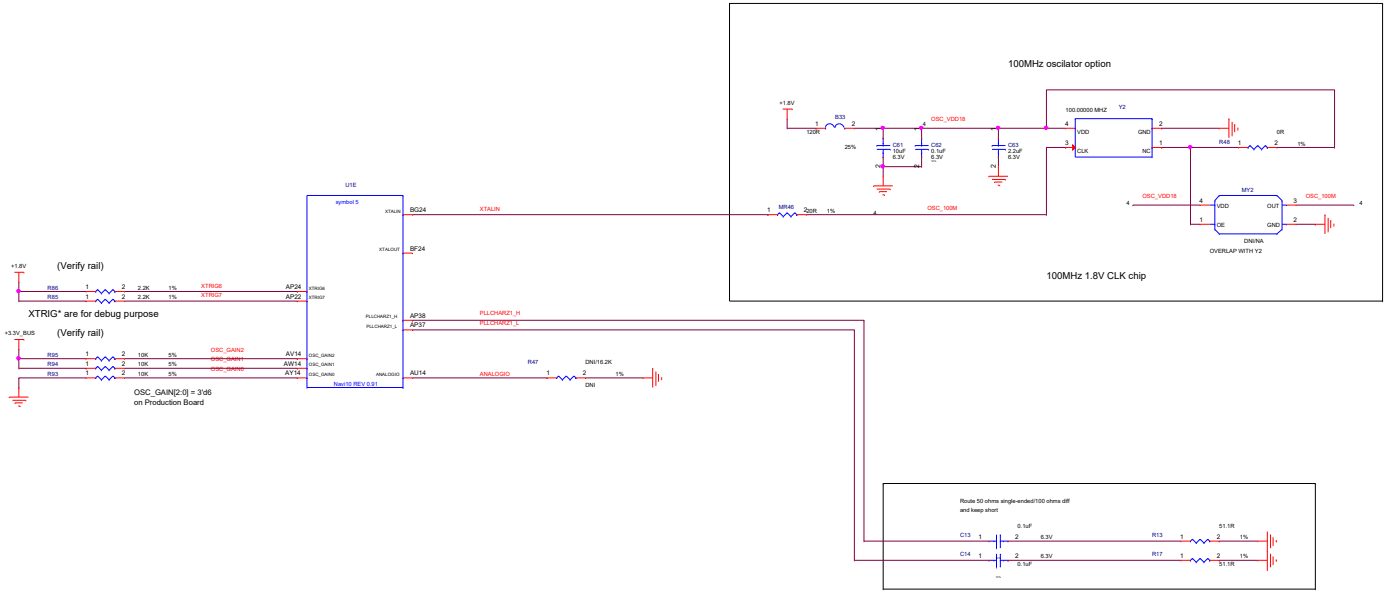
Sapphire Tech
6F , No.18, WenHu Street , NeiHu District , Taipei City, 114, Taiwan

Title
Page 03. NAV110 GPIOs

Size	Document Number	Rev
Custom	E411-00_FINAL	00

Date: Tuesday, June 18, 2019 Sheet 3 of 35

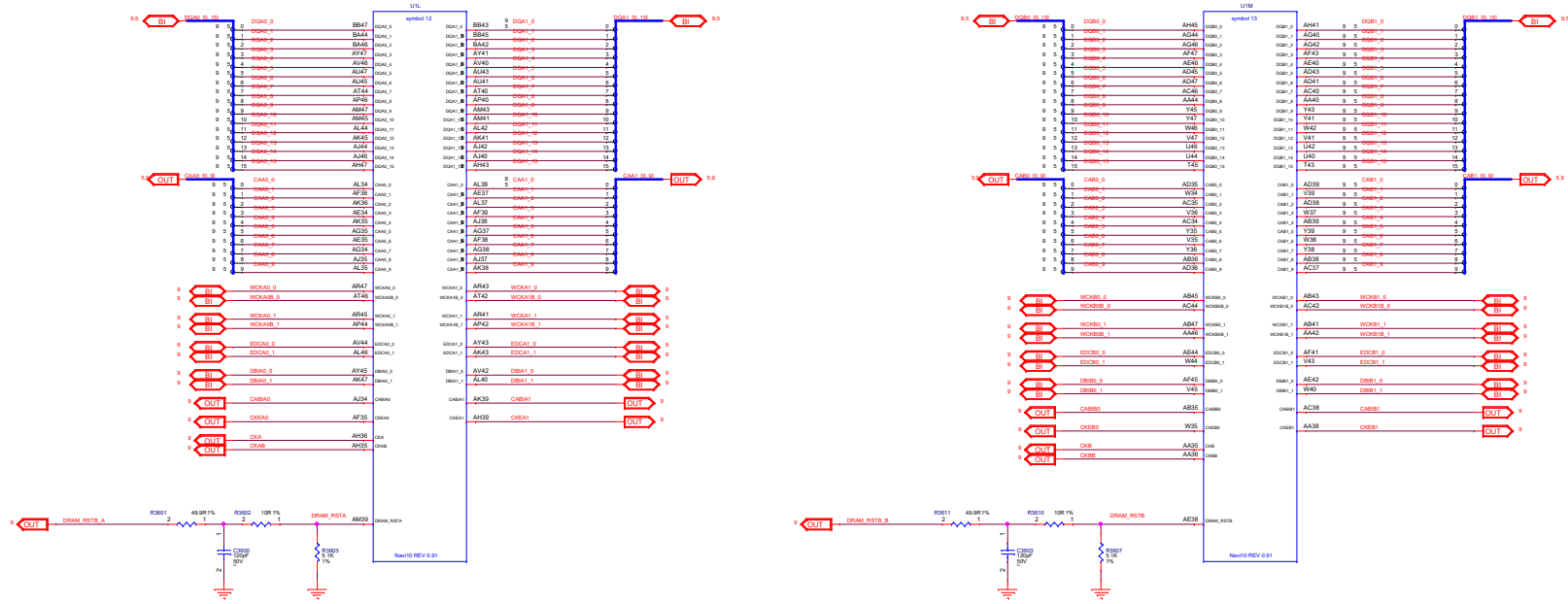
PRELIMINARY AND SUBJECT TO CHANGE



Sapphire Tech			
6F , No.18, WenHu Street , NeiHu District , Taipei City, 114, Taiwan			
Title: Page 04. NAVI10 XTAL			
Size: Custom	Document Number: E411-00_FINAL		Rev: 00
Date: Tuesday, June 18, 2019	Sheet 4 of 35		

NAVI 10 MEM INTERFACE CH A/B

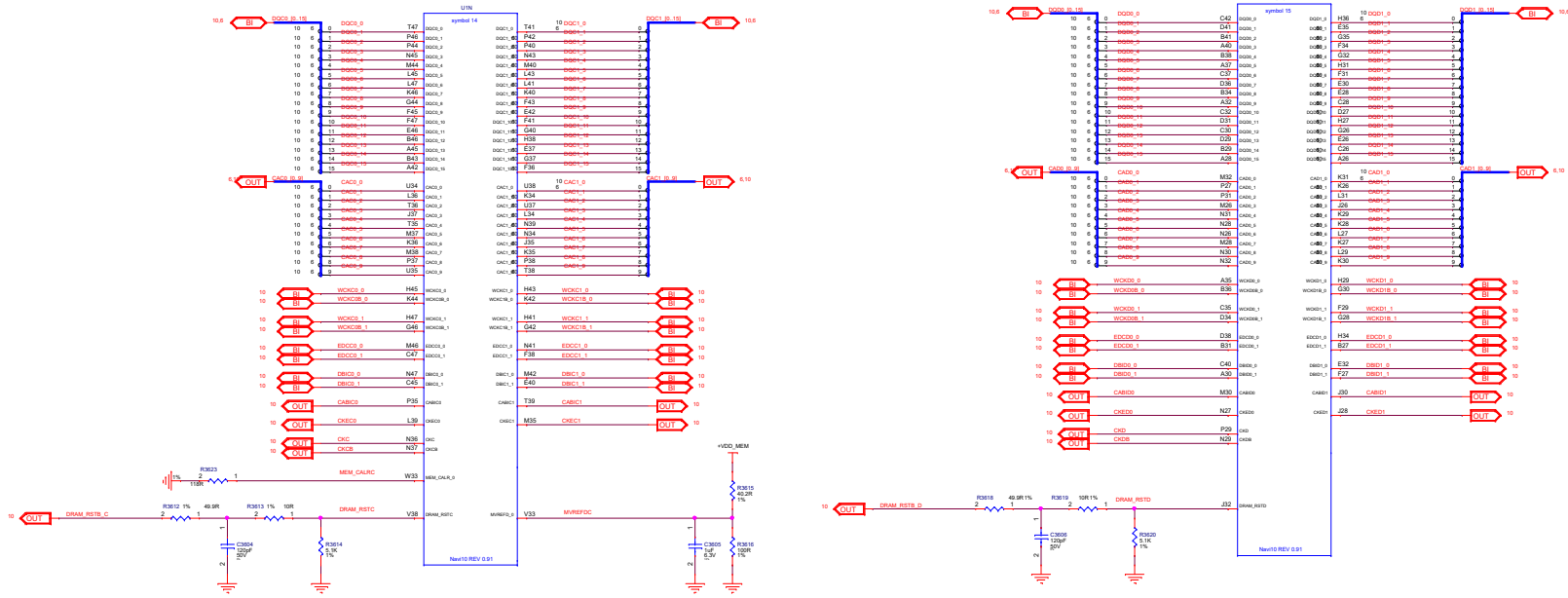
PRELIMINARY AND SUBJECT TO CHANGE



Sapphire Tech			
6F , No.18, WenHu Street , NeiHu District , Taipei City, 114, Taiwan			
Title: Page 05. NAVI10 MEM CHAB			
Size: Custom	Document Number: E411-00_FINAL		Rev: 00
Date: Tuesday, June 18, 2019	Sheet 5 of 35		

NAVI 10 MEM INTERFACE CH C/D

PRELIMINARY AND SUBJECT TO CHANGE



Sapphire Tech

6F , No.18, WenHu Street , NeiHu District , Taipei City, 114, Taiwan

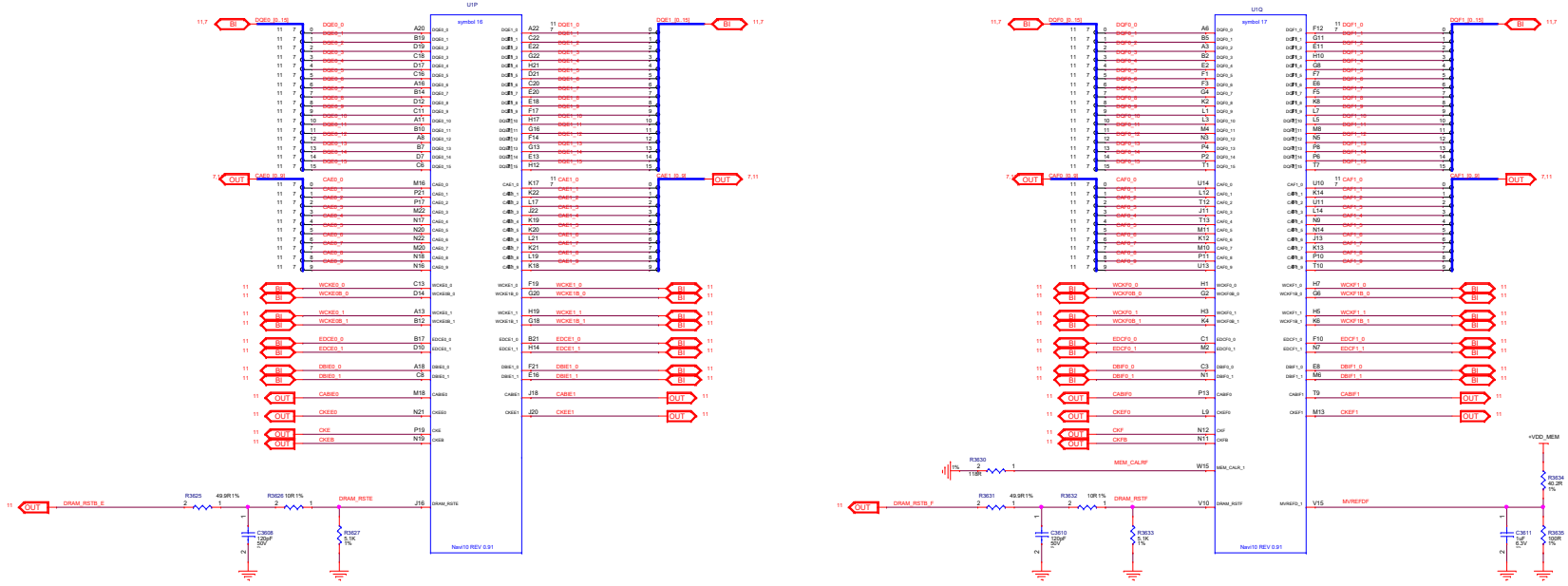
Title: Page 06. NAVI10 MEM CHCD

Size: Custom | Document Number: E411-00_FINAL | Rev: 00

Date: Tuesday, June 18, 2019 | Sheet 6 of 35

NAVI 10 MEM INTERFACE CH E/F

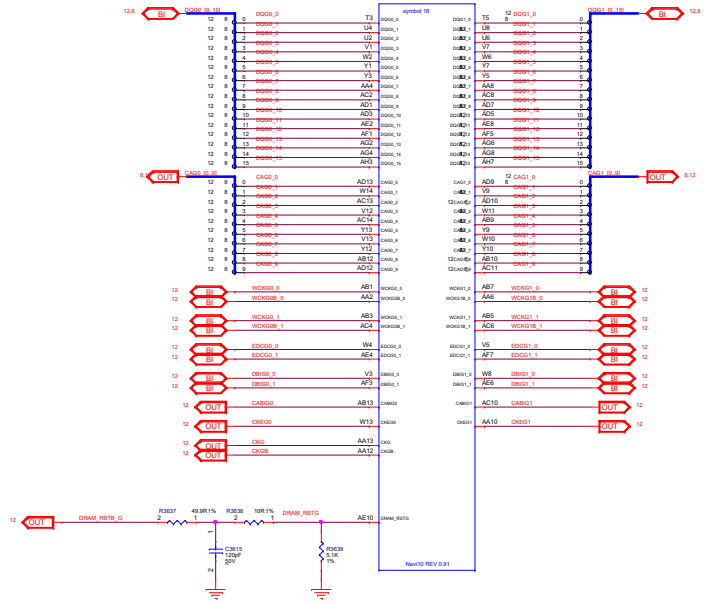
PRELIMINARY AND SUBJECT TO CHANGE

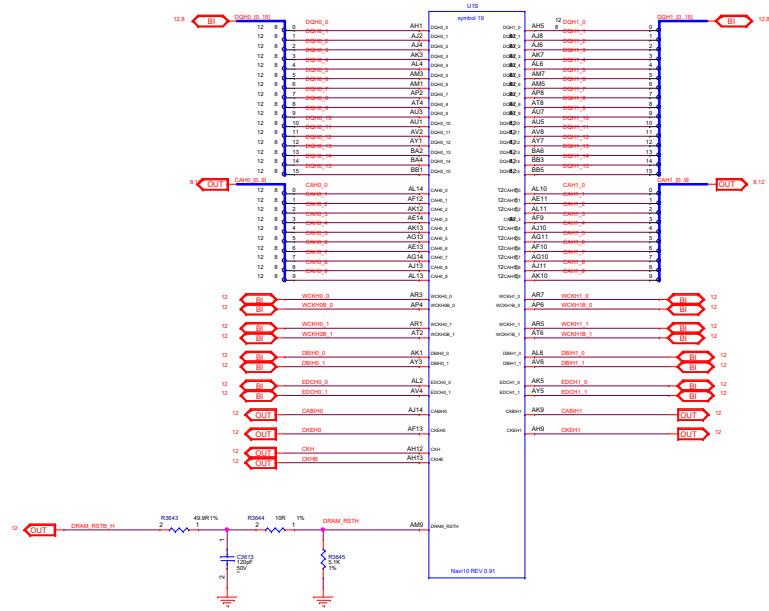


Sapphire Tech			
6F , No.18, WenHu Street , NeiHu District , Taipei City, 114, Taiwan			
Title: Page 07. NAVI10 MEM CHEF			
Size: Custom	Document Number: E411-00_FINAL		Rev: 00
Date: Tuesday, June 18, 2019	Sheet 7 of 35		

NAVI 10 MEM INTERFACE CH G/H

PRELIMINARY AND SUBJECT TO CHANGE

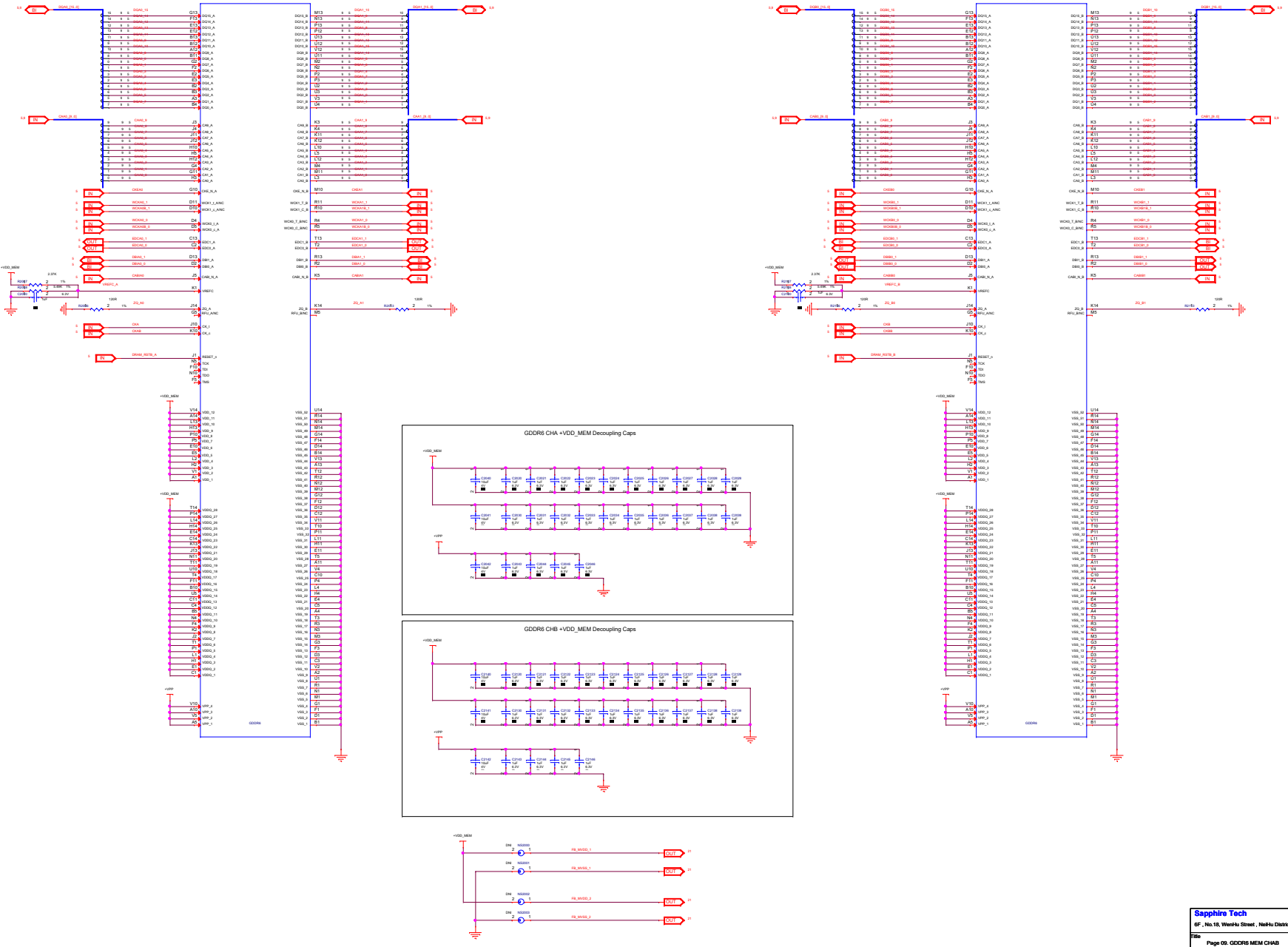




Sapphire Tech			
6F , No.18, WenHu Street , NeiHu District , Taipei City, 114, Taiwan			
Title: Page 08. NAVI10 MEM CHGH			
Size: Custom	Document Number: E411-00_FINAL		Rev: 00
Date: Tuesday, June 18, 2019	Sheet 8 of 35		

GDDR6x16 CHAB Memory

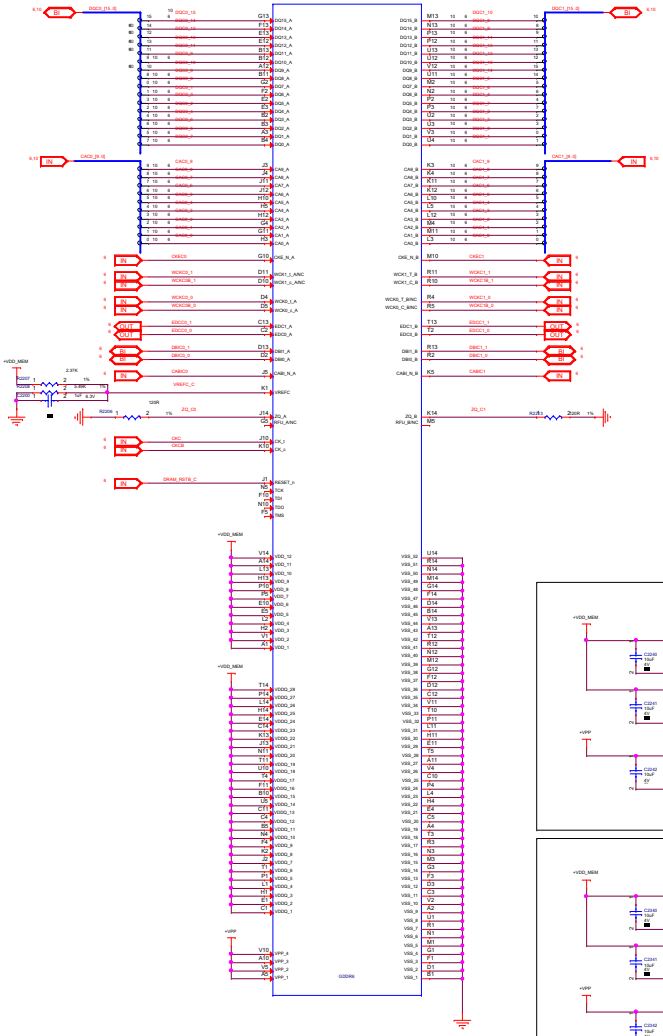
PRELIMINARY AND SUBJECT TO CHANGE

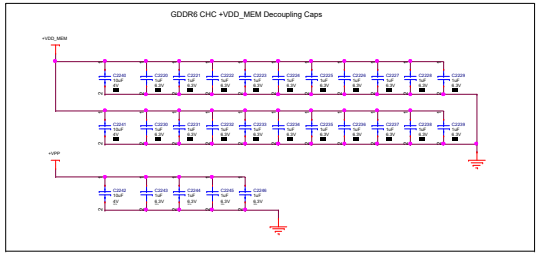


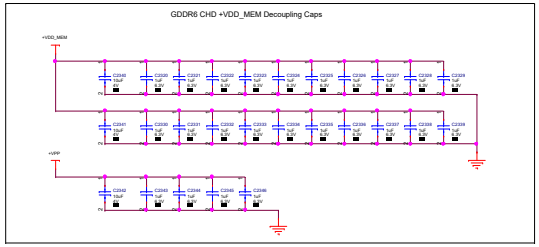
Sapphire Tech		
6F , No.18, Wenhu Street , Neihu District , Taipei City, 114, Taiwan		
Title	Page 09. GDDR6 MEM CHAB	
Size: Custom	Document Number: E411-00_FINAL	Rev: 00
Date: Tuesday, June 18, 2019	Sheet 9 of 35	

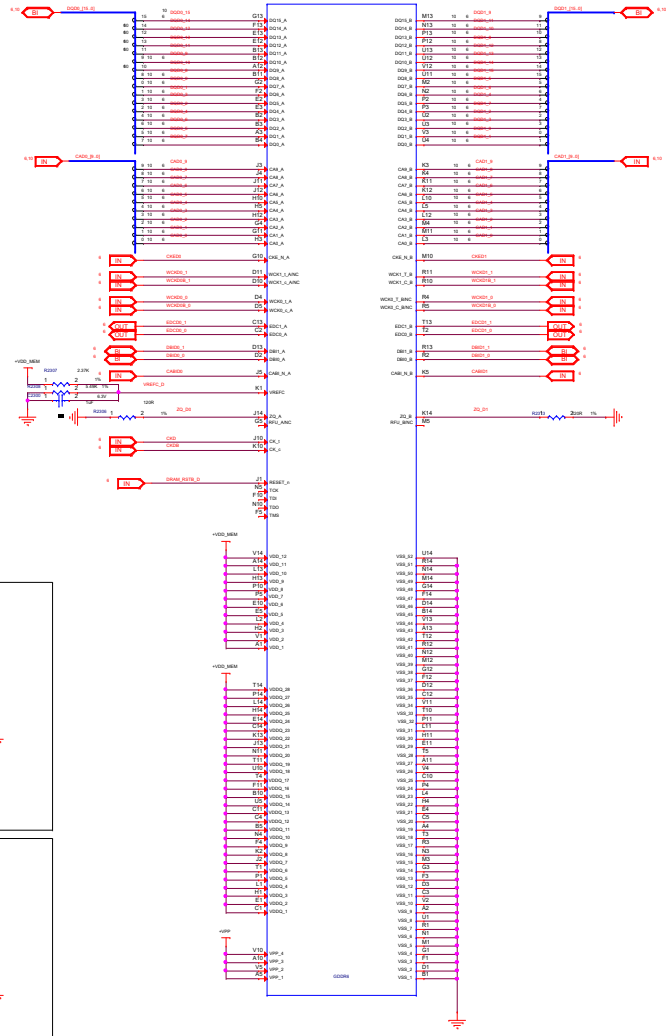
GDDR6x16 CHCD Memory

PRELIMINARY AND SUBJECT TO CHANGE





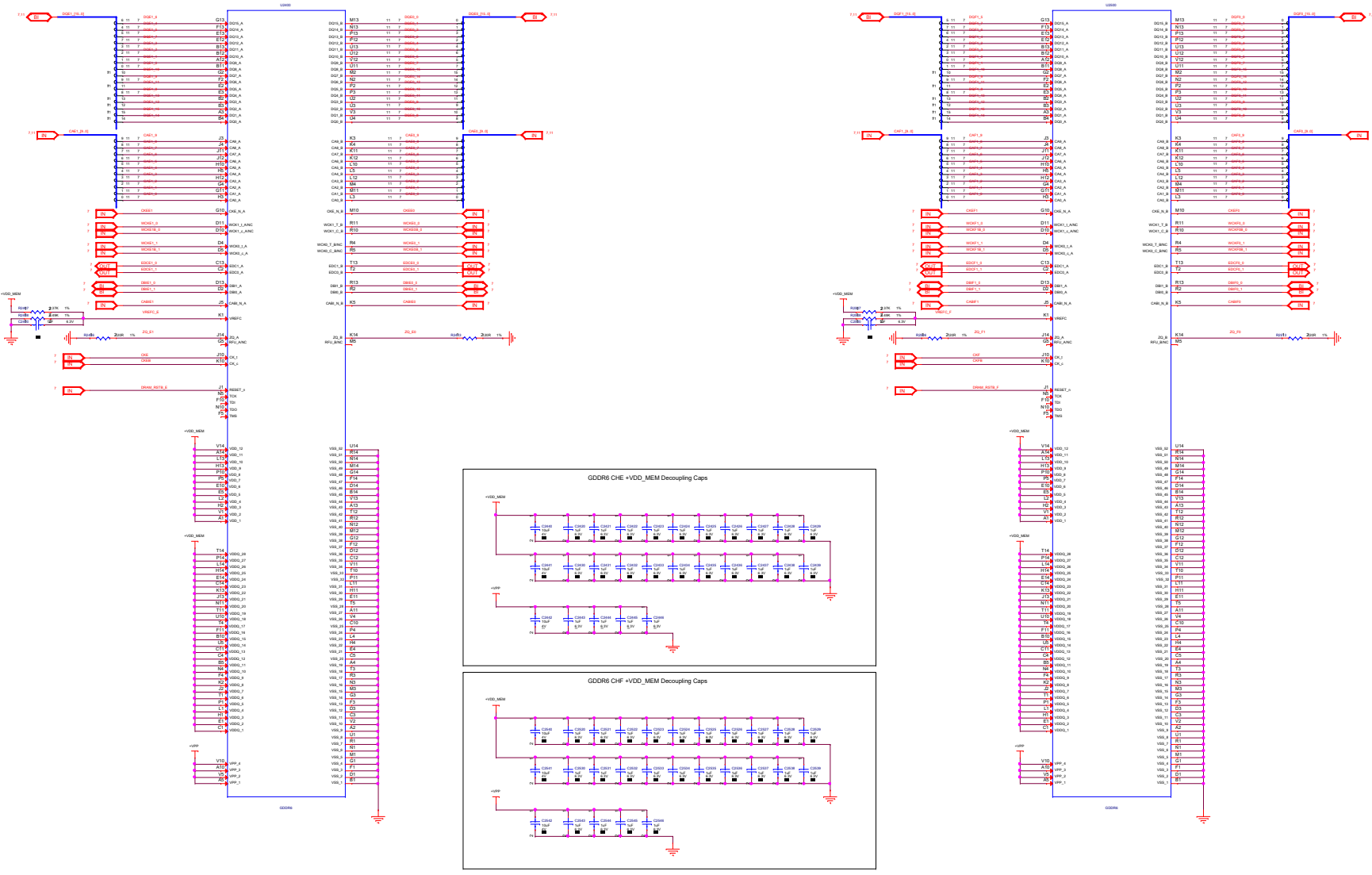




Sapphire Tech			
6F , No.18, Wenhu Street , Neihu District , Taipei City, 114, Taiwan			
Title	Page 10. GDDR6 MEM CHCD		
Size Custom	Document Number E411-00_FINAL		Rev 00
Date: Tuesday, June 18, 2019	Sheet 10 of 35		

GDDR6x16 CHEF Memory

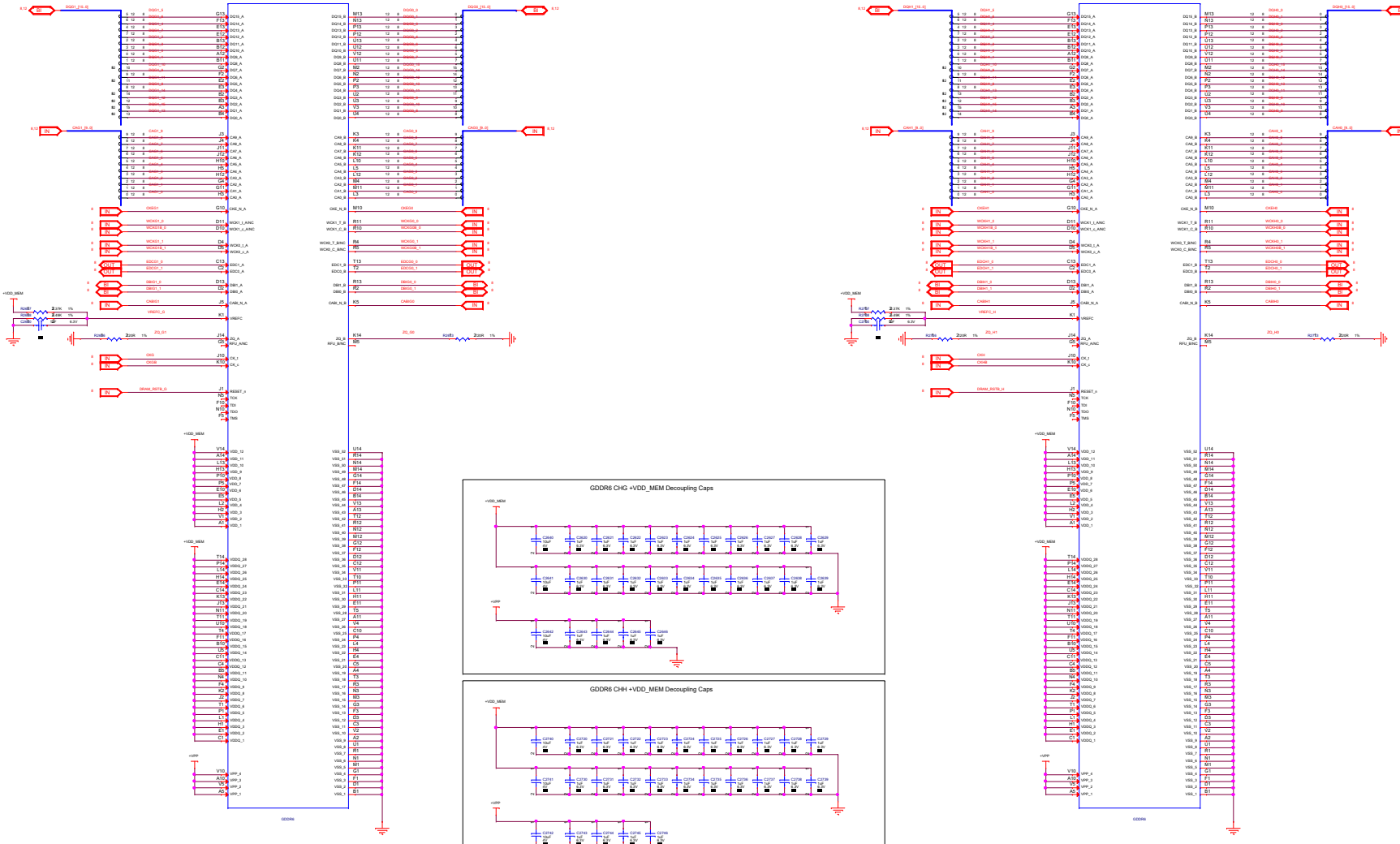
PRELIMINARY AND SUBJECT TO CHANGE



Sapphire Tech			
6F , No.18, Wenhu Street , Neihu District , Taipei City, 114, Taiwan			
Title	Page 11. GDDR6 MEM CHEF		
Size: Custom	Document Number: E411-00_FINAL		Rev: 00
Date: Tuesday, June 18, 2019	Sheet 11 of 35		

GDDR6x16 CHGH Memory

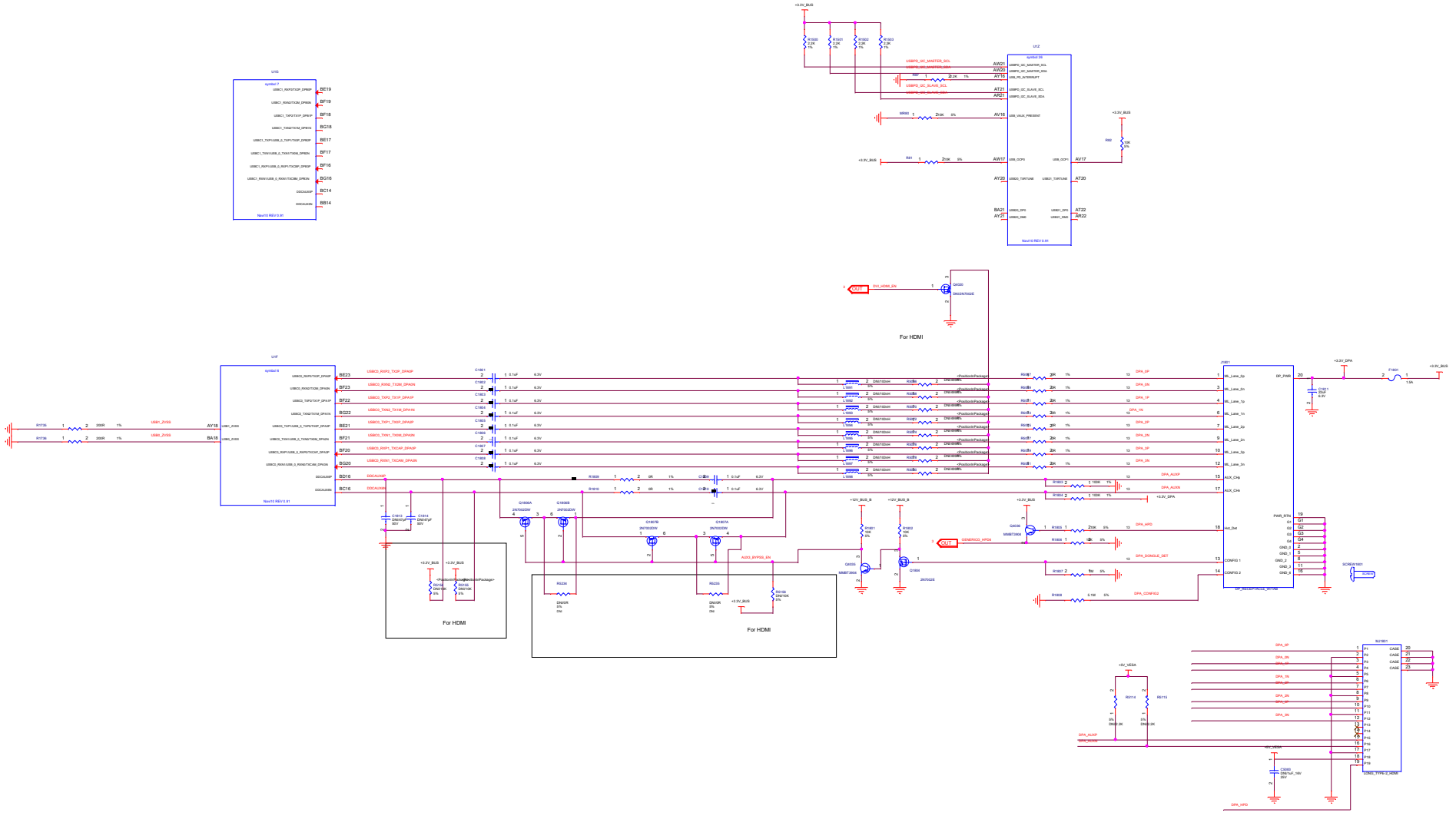
PRELIMINARY AND SUBJECT TO CHANGE



Sapphire Tech			
6F , No.18, Wenhu Street , Neihu District , Taipei City, 114, Taiwan			
Title	Page 12. GDDR6 MEM CHGH		
Size: Custom	Document Number: E411-00_FINAL		Rev: 00
Date: Tuesday, June 18, 2019	Sheet 12 of 35		

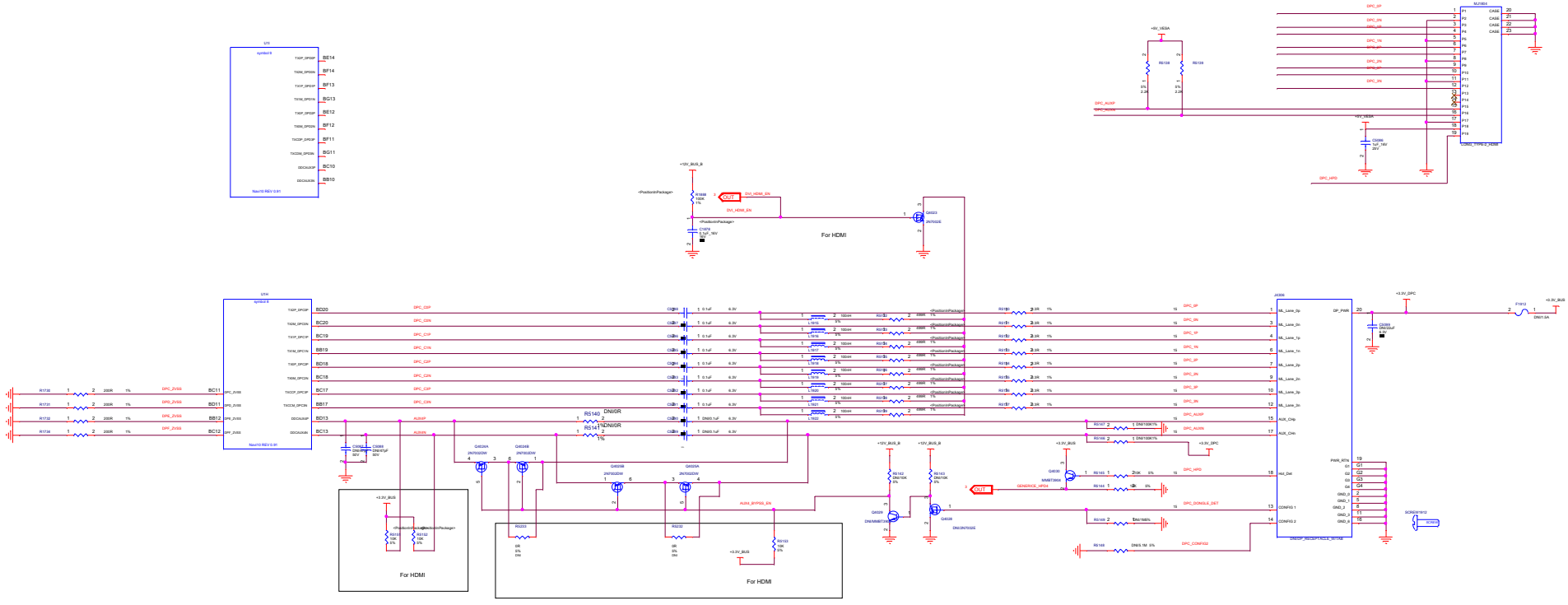
NAVI10 TMDP A/B

PRELIMINARY AND SUBJECT TO CHANGE



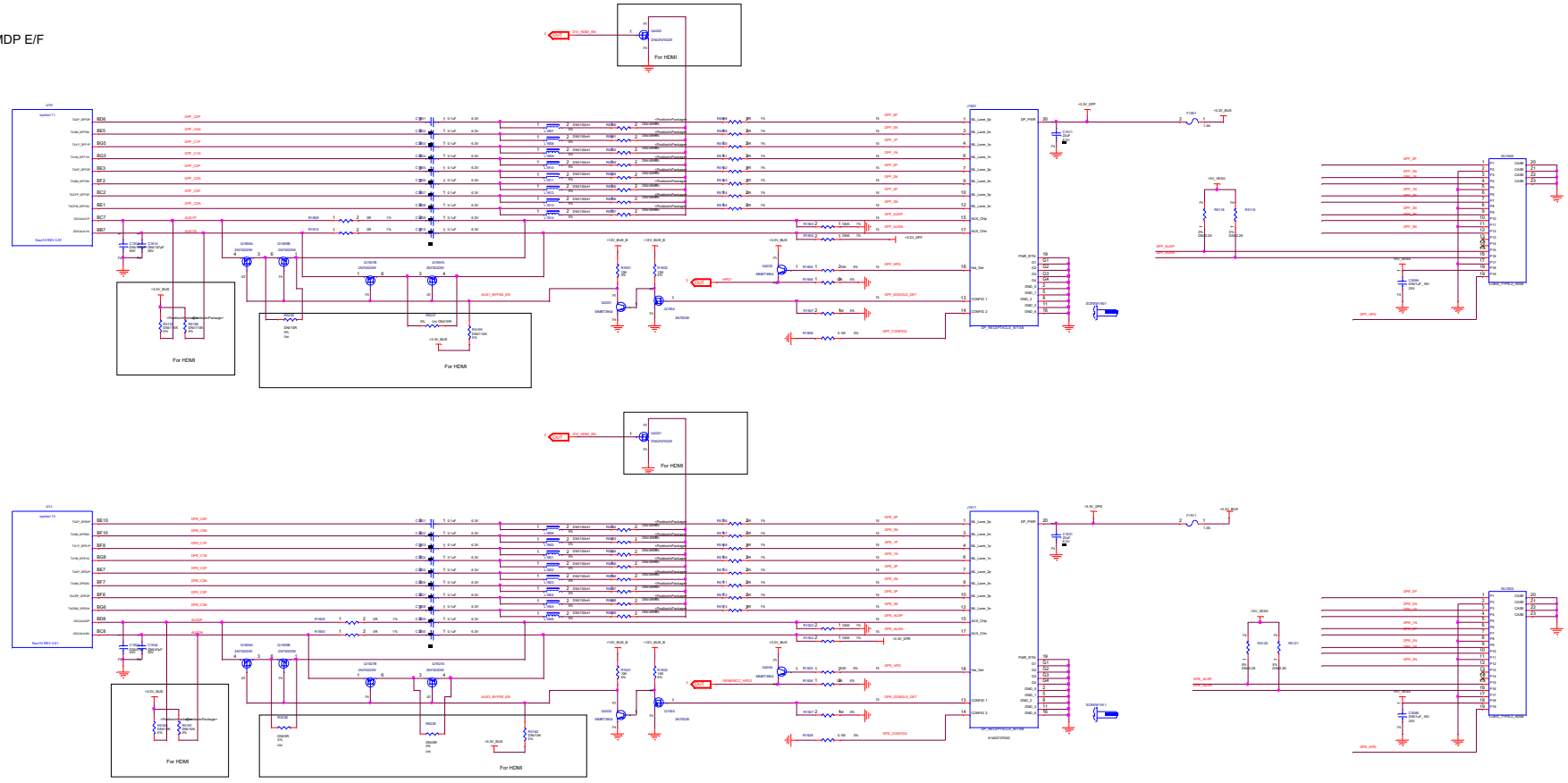
Sapphire Tech			
6F , No.18, WenHu Street , NeiHu District , Taipei City, 114, Taiwan			
Title	Page 13. NAVI10 TMDPA - DP		
Size: Custom	Document Number: E411-00_FINAL		Rev: 00
Date: Tuesday, June 18, 2019	Sheet 13 of 35		

NAVI10 TMDP C/D

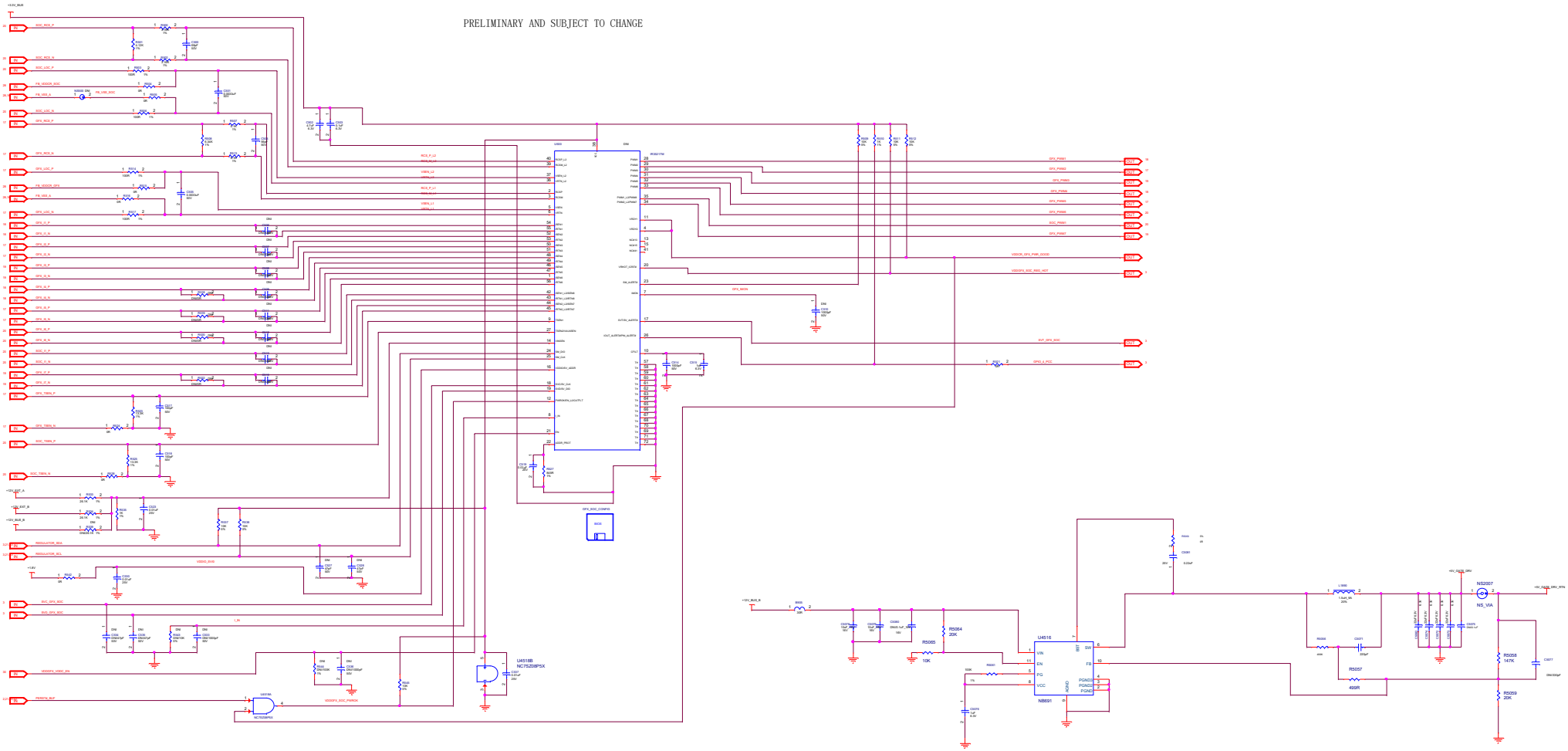


Sapphire Tech		
6F , No.18, WenHu Street , NeiHu District , Taipei City, 114, Taiwan		
Title: Page 14. NAVI10 TMDPC HDMI		
Size: Custom	Document Number: E411-00_FINAL	Rev: 00
Date: Tuesday, June 18, 2019	Sheet 14 of 35	

(9) NAVI10 TMDP E/F

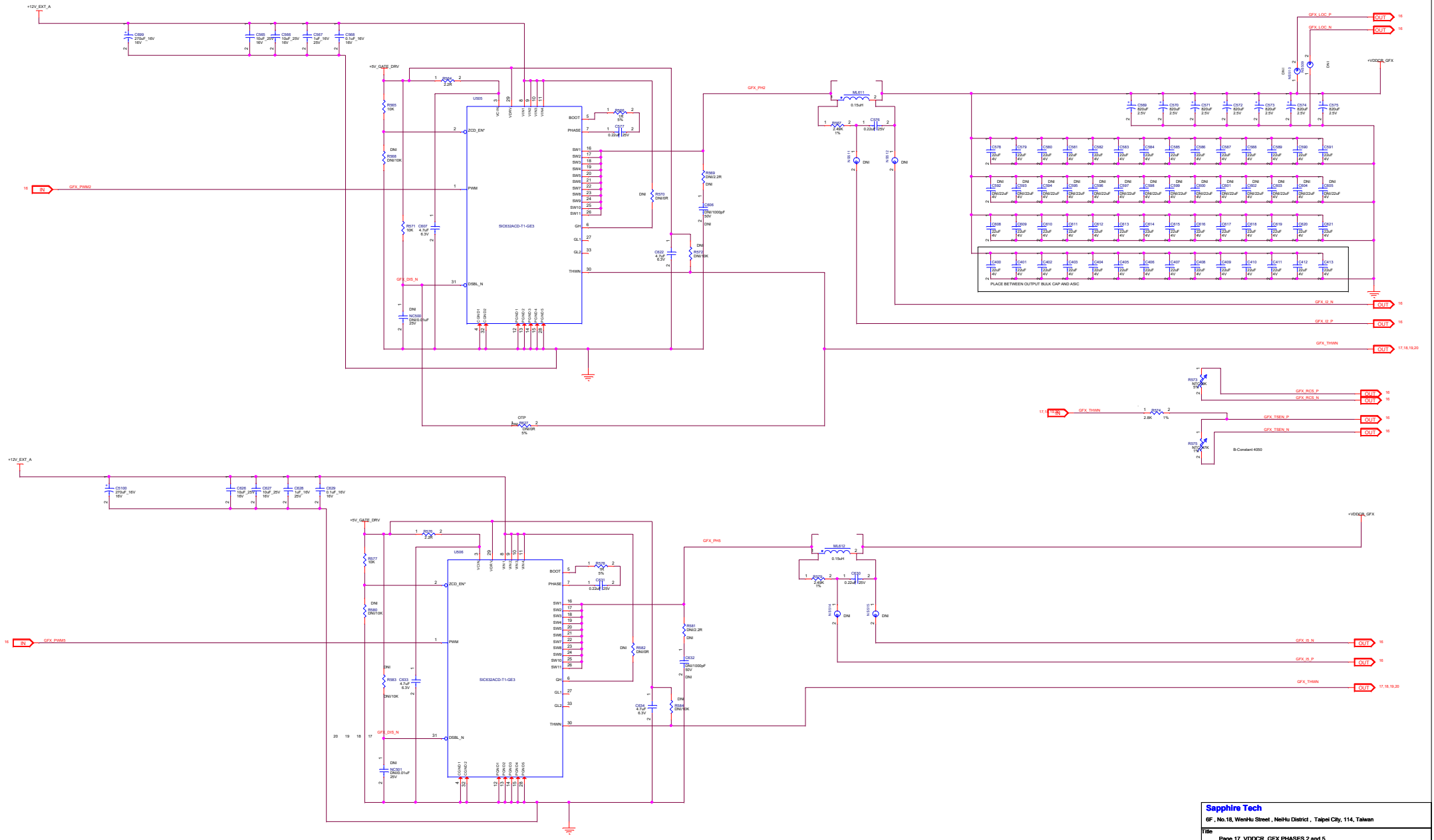


PRELIMINARY AND SUBJECT TO CHANGE



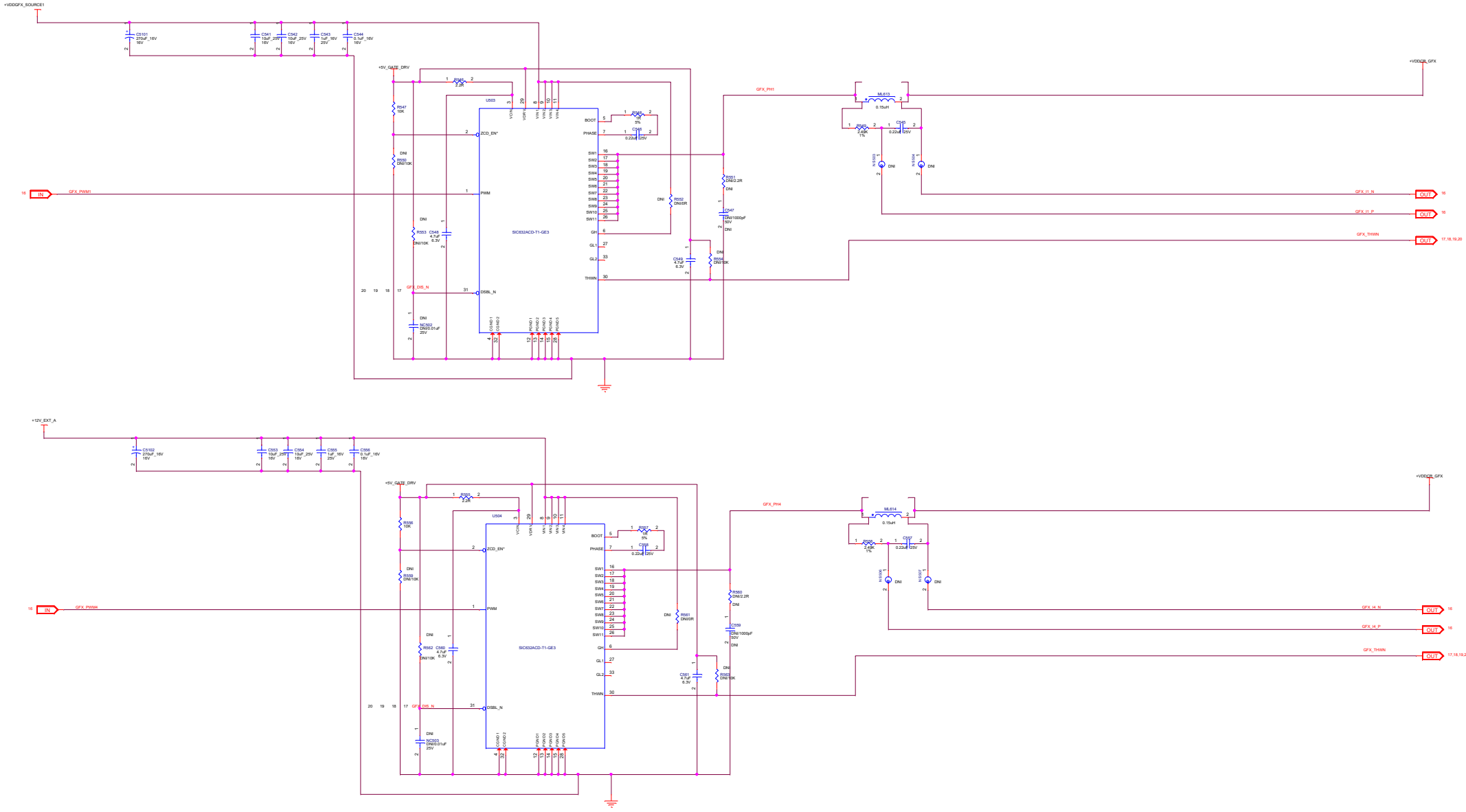
Sapphire Tech		
6F., No.18, Wenhu Street , Neihu District , Taipei City, 114, Taiwan		
Title: Page 16. GFX & SOC CONTROLLER		
Size: D	Document Number: E411-00_FINAL	Rev: 00
Date: Thursday, June 20, 2019	Sheet 16 of 35	

PRELIMINARY AND SUBJECT TO CHANGE



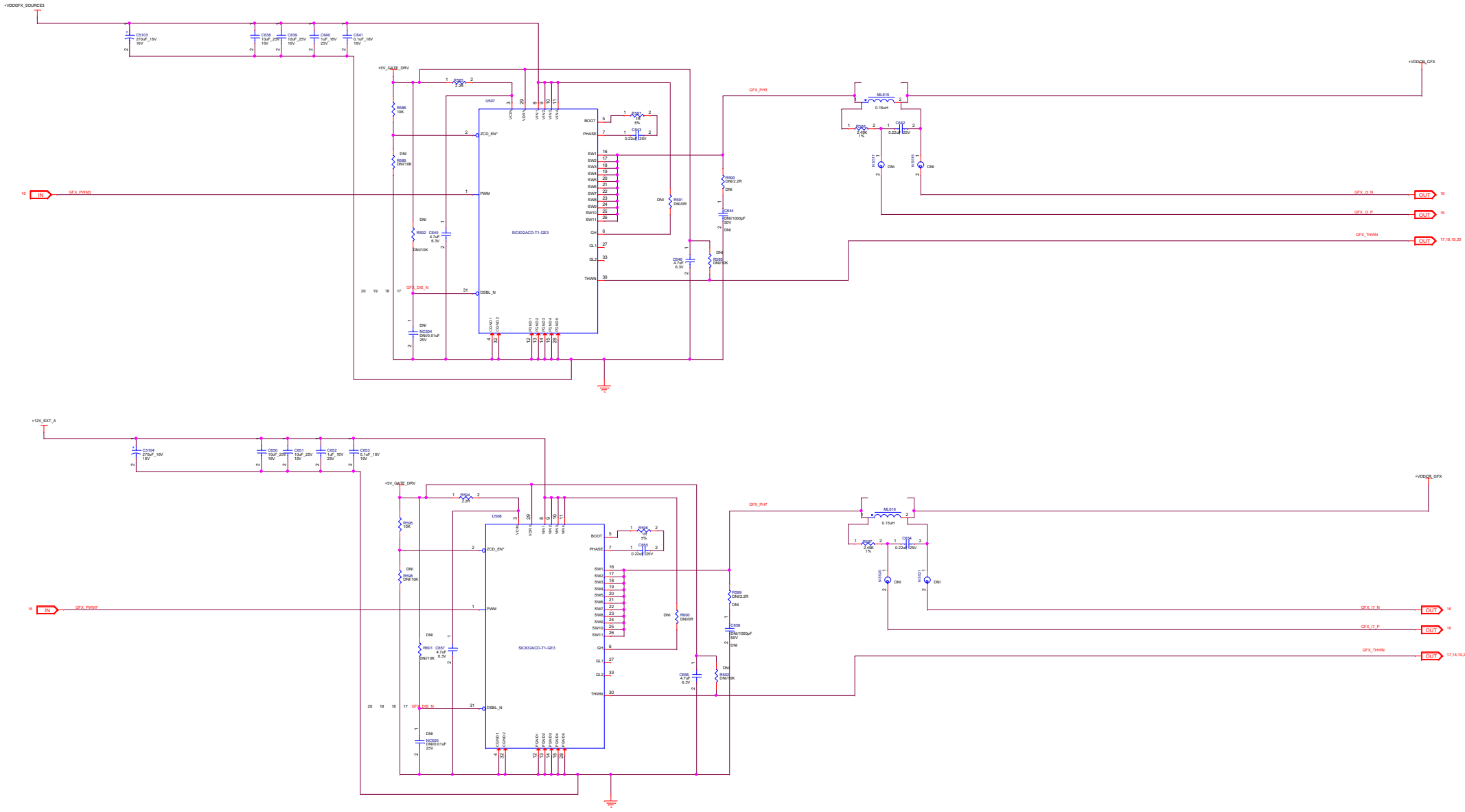
Sapphire Tech			
6F , No.18, WenHu Street , NeiHu District , Taipei City, 114, Taiwan			
Title: Page 17. VDDCR_GFX PHASES 2 and 5			
Size: Custom	Document Number: E411-00_FINAL		Rev: 00
Date: Thursday, June 20, 2019	Sheet 17 of 35		

PRELIMINARY AND SUBJECT TO CHANGE



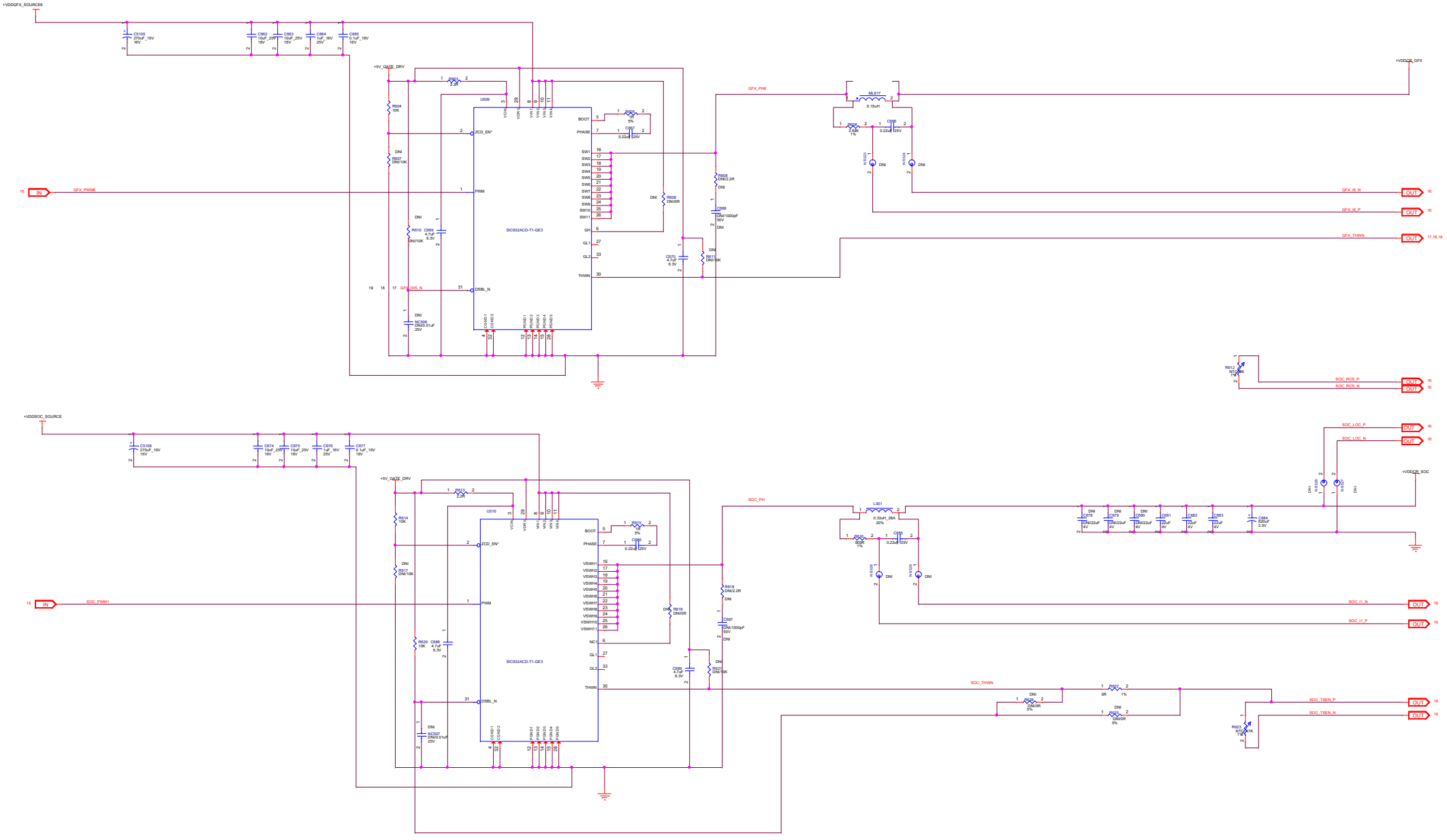
Sapphire Tech		
6F , No.18, WenHu Street , NeiHu District , Taipei City, 114, Taiwan		
Title: Page 18. VDDCR_GFX PHASES 1 and 4		
Size: Custom	Document Number: E411-00_FINAL	Rev: 00
Date: Thursday, June 20, 2019	Sheet 18 of 35	

PRELIMINARY AND SUBJECT TO CHANGE



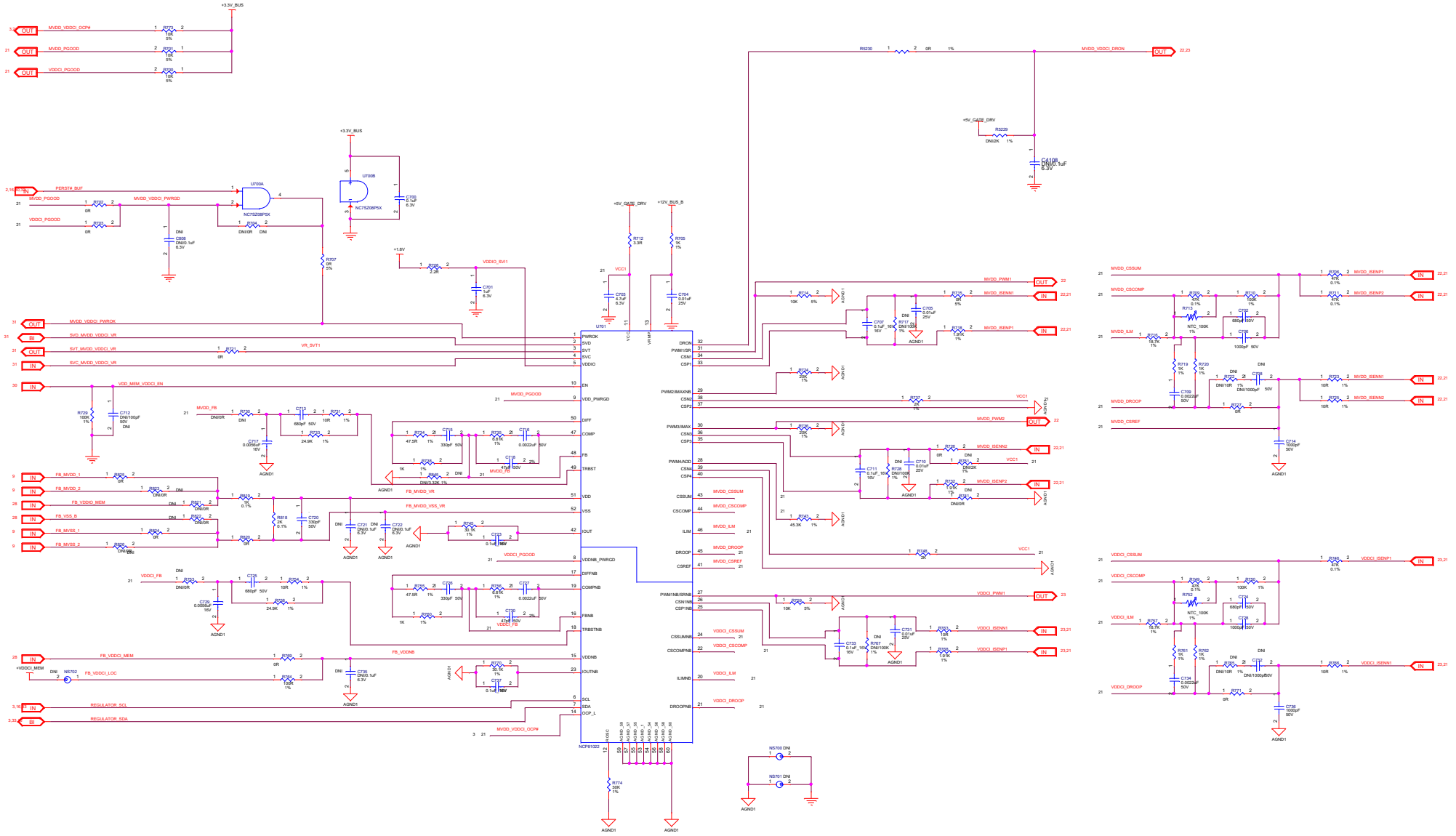
Sapphire Tech		
6F , No.18, WenHu Street , NeiHu District , Taipei City, 114, Taiwan		
Title: Page 19. VDDCR_GFX PHASES 3 and 7		
Size: Custom	Document Number: E411-00_FINAL	Rev: 00
Date: Thursday, June 20, 2019	Sheet 19 of 35	

PRELIMINARY AND SUBJECT TO CHANGE



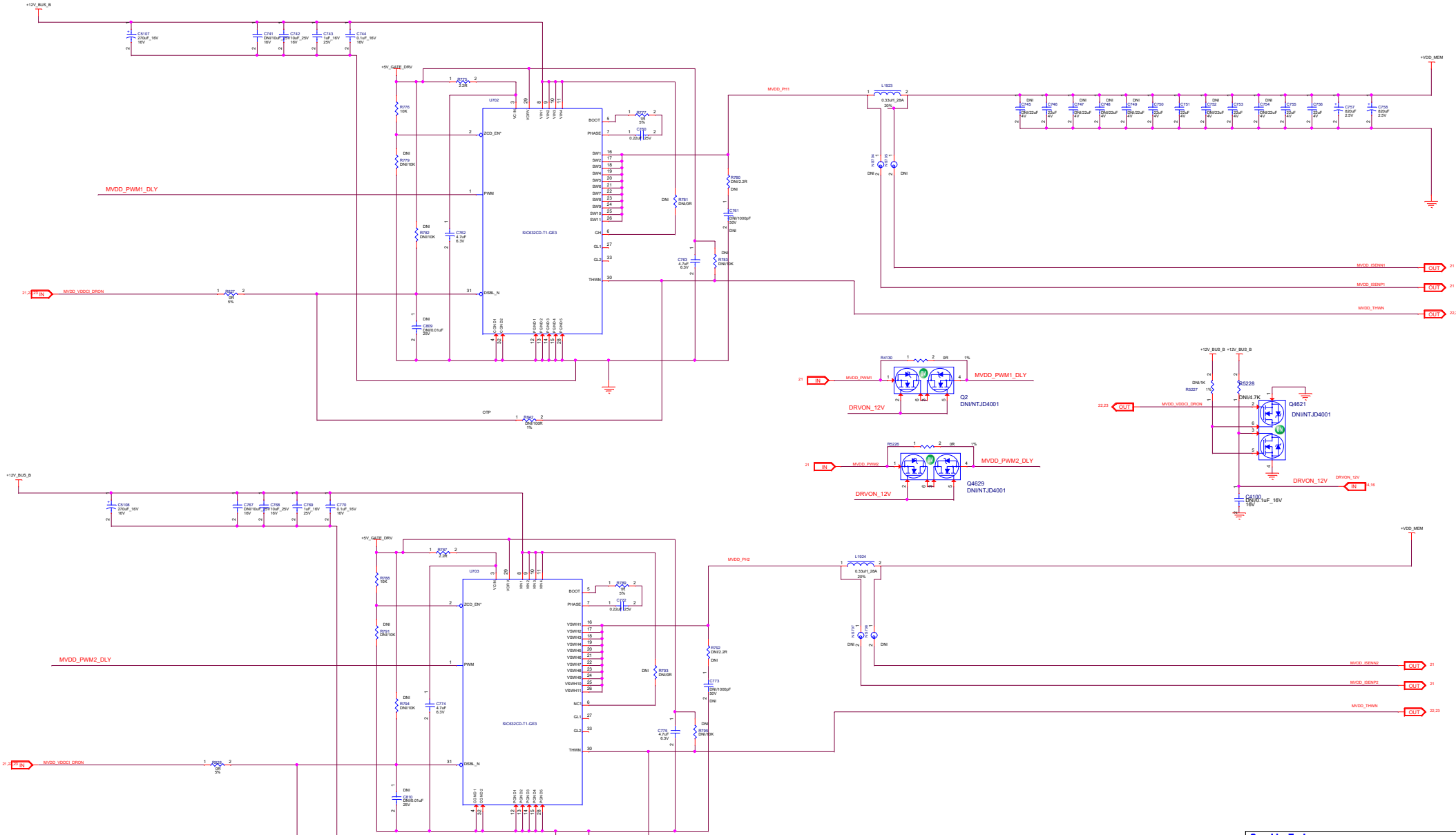
Sapphire Tech		
6F , No.18, WenHu Street , NeiHu District , Taipei City, 114, Taiwan		
Title: Page 20. VDDCR_GFX PHASES 6 and VDDC		
Size: Custom	Document Number: E411-00_FINAL	Rev: 00
Date: Thursday, June 20, 2019	Sheet 20 of 35	

PRELIMINARY AND SUBJECT TO CHANGE



Sapphire Tech			
6F , No.18, WenHu Street , NeiHu District , Taipei City, 114, Taiwan			
Title: Page 21.MVDD_VDDCI CONTROLLER			
Size: Custom	Document Number: E411-00_FINAL		Rev: 00
Date: Thursday, June 20, 2019	Sheet 21 of 35		

PRELIMINARY AND SUBJECT TO CHANGE



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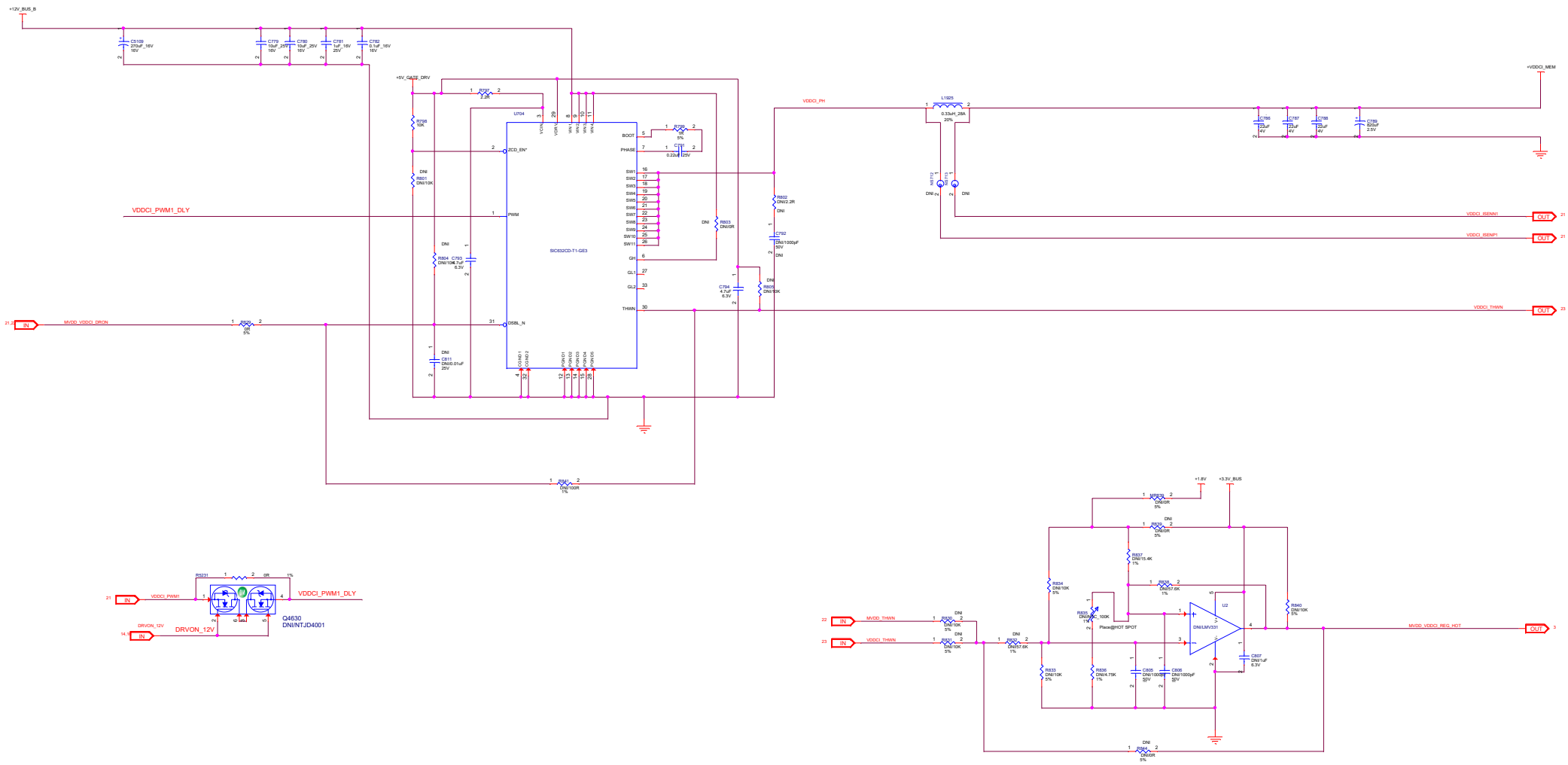
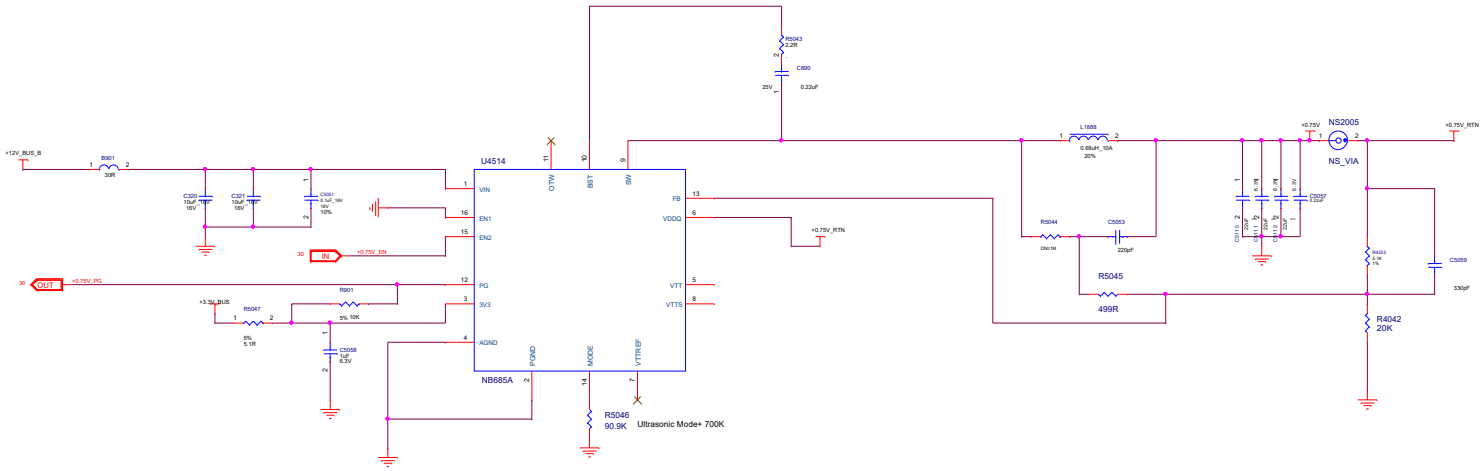
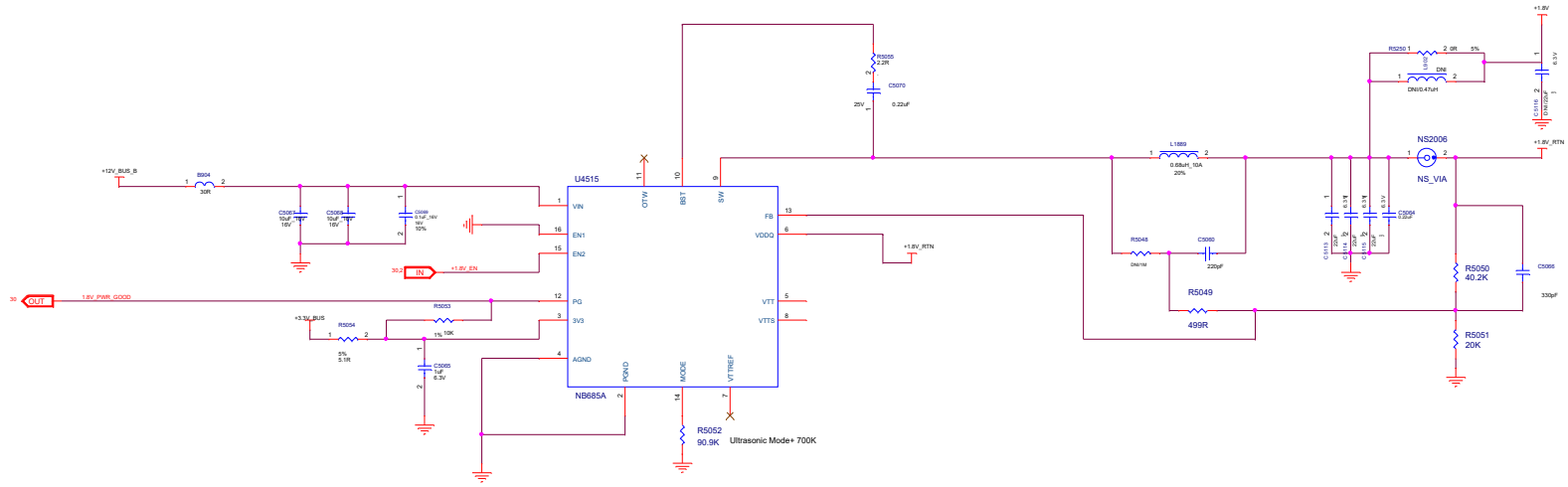


Sapphire Tech			
6F , No.18, WenHu Street , NeiHu District , Taipei City, 114, Taiwan			
Title: Page 23. REG VDDCI			
Size: Custom	Document Number: E411-00_FINAL		Rev: 00
Date: Thursday, June 20, 2019	Sheet 23 of 35		



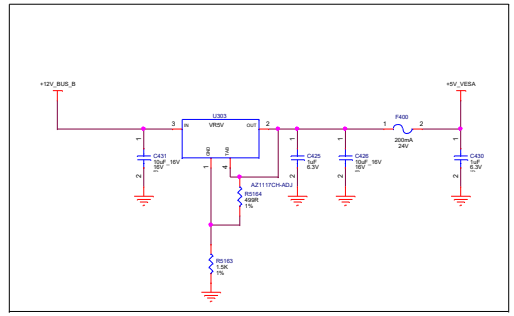
Sapphire Tech		
6F , No.18, WenHu Street , NeiHu District , Taipei City, 114, Taiwan		
Title: Page 24. REG 0.75V		
Size: Custom	Document Number: E411-00_FINAL	Rev: 00
Date: Tuesday, June 18, 2019	Sheet 24 of 35	

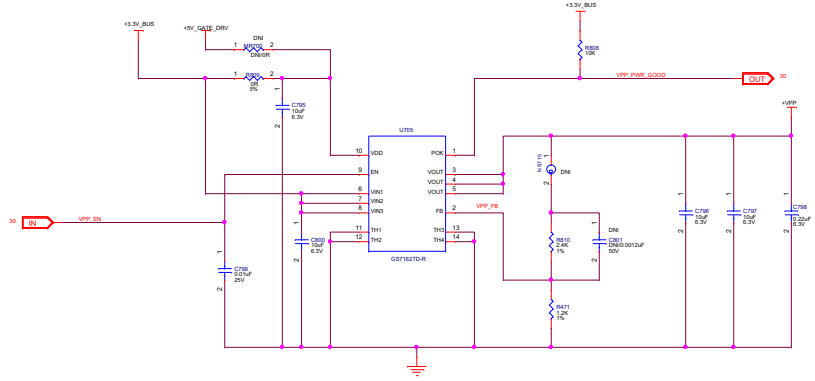


Sapphire Tech			
6F , No.18, WenHu Street , NeiHu District , Taipei City, 114, Taiwan			
Title: Page 25. REG 1.8V			
Size: Custom	Document Number: E411-00_FINAL		Rev: 00
Date: Tuesday, June 18, 2019	Sheet 25 of 35		

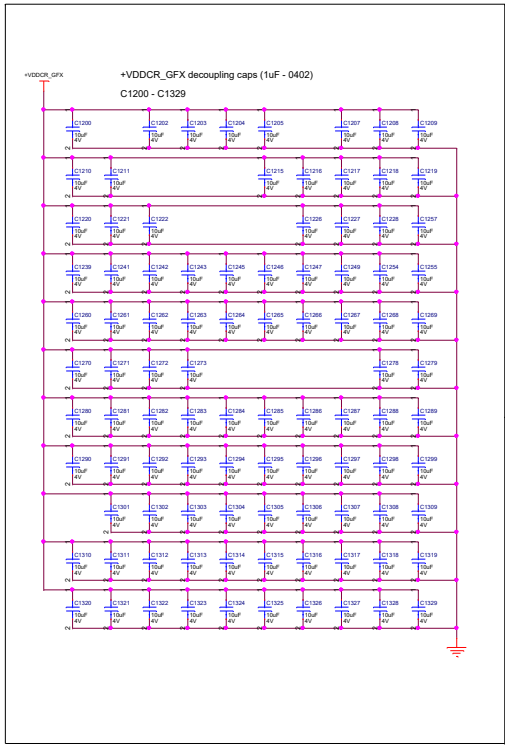
REGULATOR FOR +5V RAILS

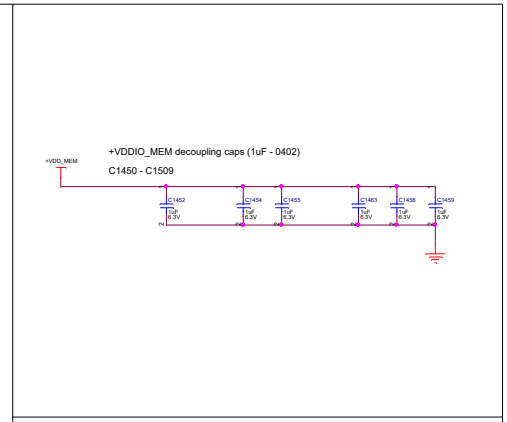
IOUT = 50mA

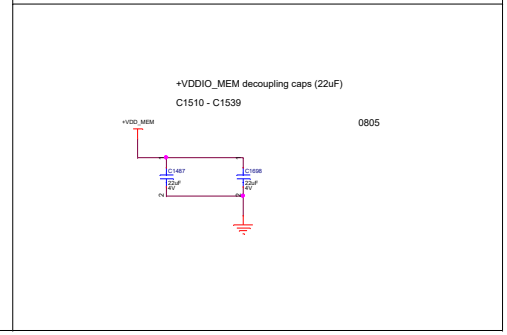


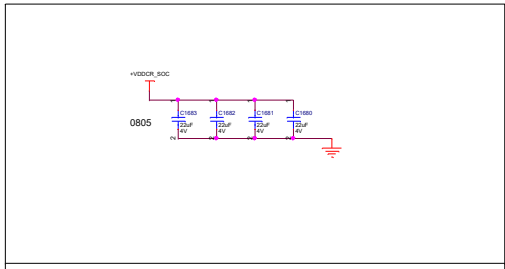


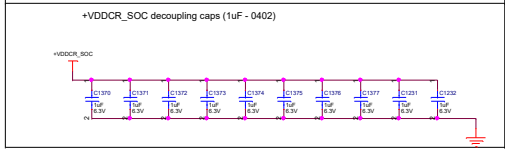
Sapphire Tech		
6F , No.18, WenHu Street , NeiHu District , Taipei City, 114, Taiwan		
Title: Page 26. SMALL RAIL REGULATORS		
Size: Custom	Document Number: E411-00_FINAL	Rev: 00
Date: Tuesday, June 18, 2019	Sheet 26 of 35	

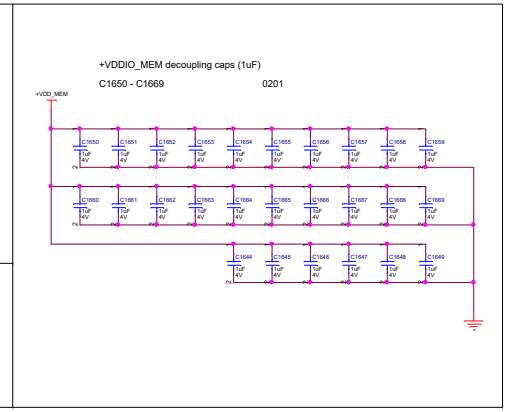


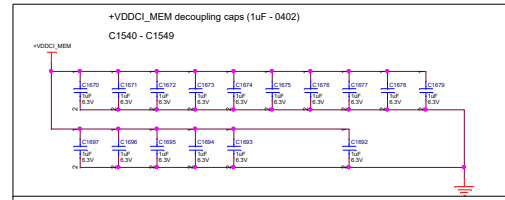


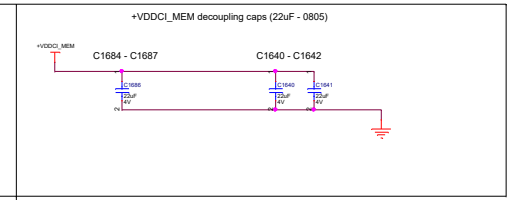


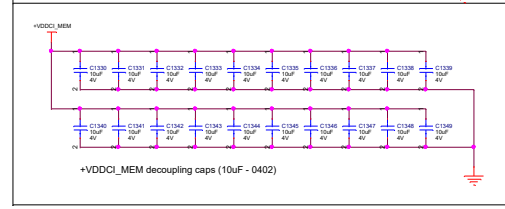




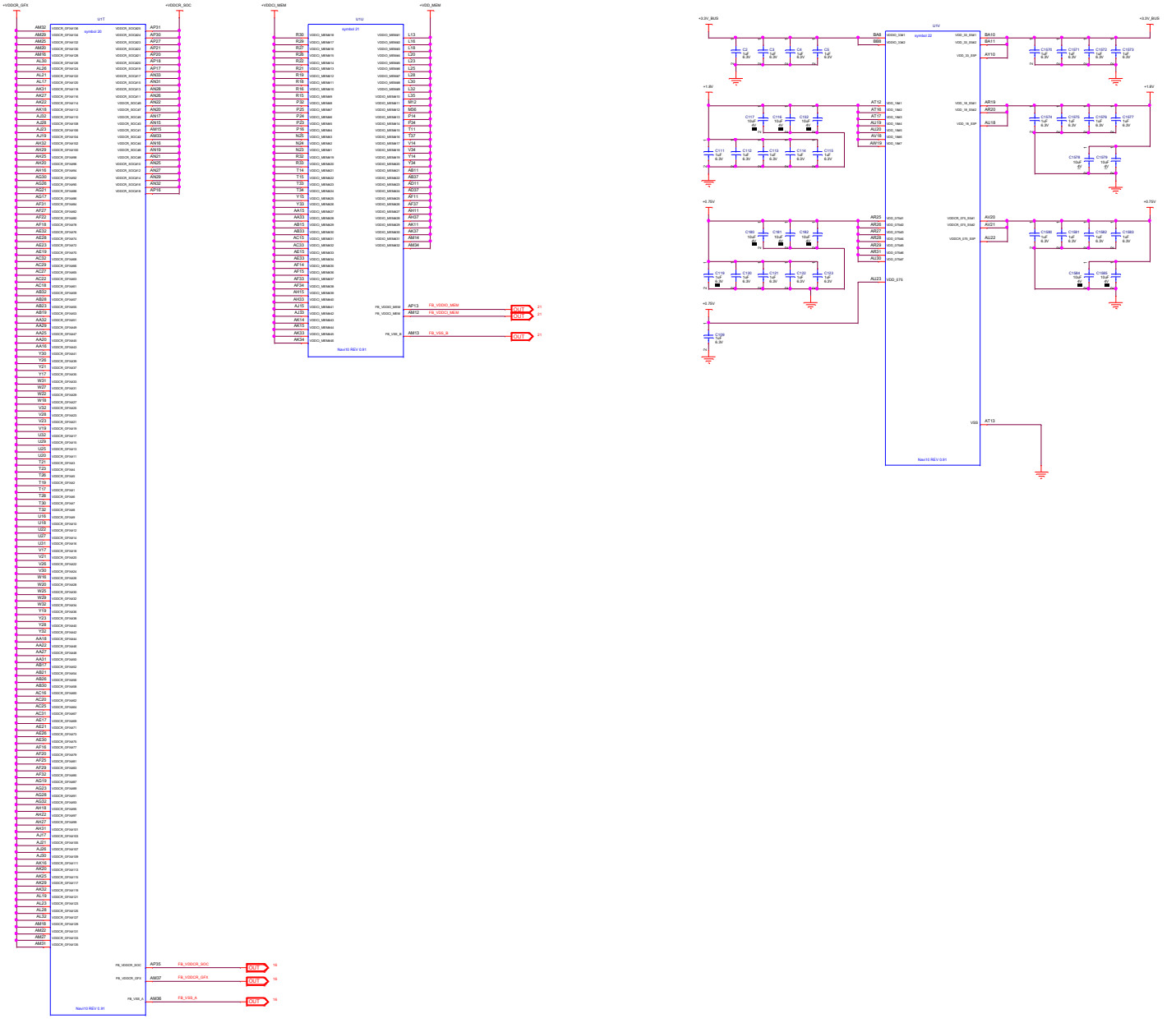








Sapphire Tech			
6F , No.18, WenHu Street , NeiHu District , Taipei City, 114, Taiwan			
Title: Page 27. NAVI10 DECAPS			
Size: Custom	Document Number: E411-00_FINAL		Rev: 00
Date: Tuesday, June 18, 2019	Sheet 27 of 35		



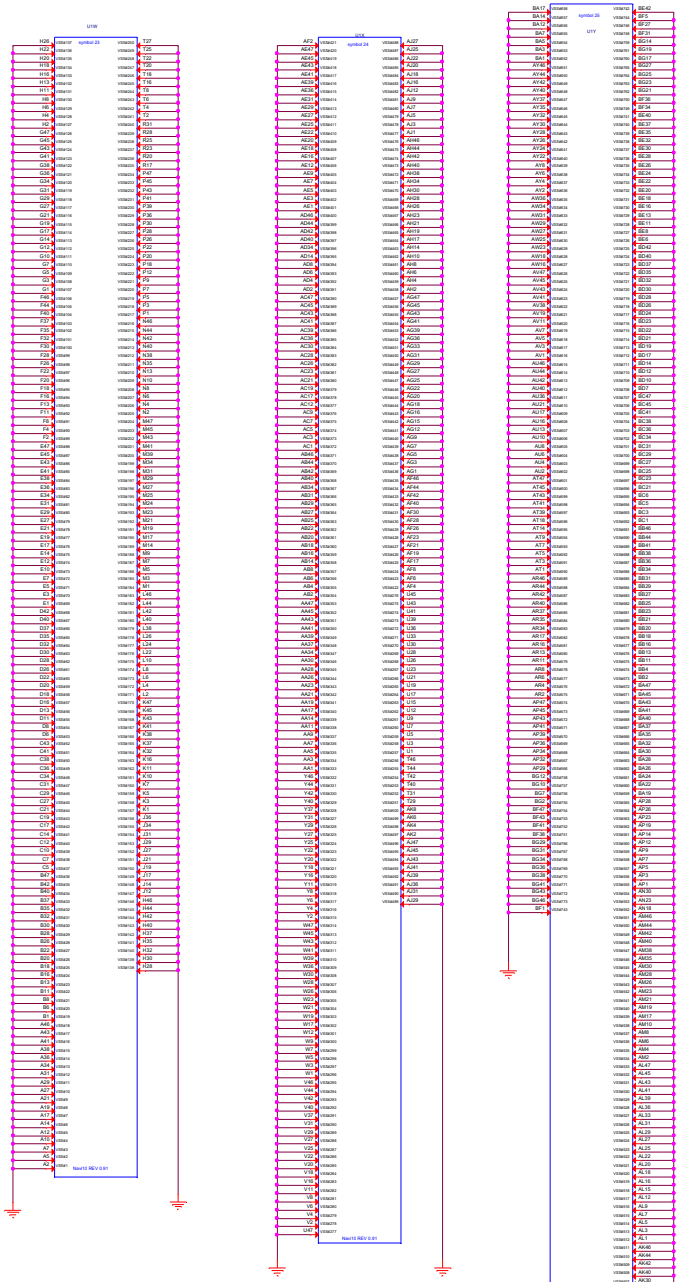
Sapphire Tech
6F , No.18, Wenhu Street , Neihu District , Taipei City, 114, Taiwan

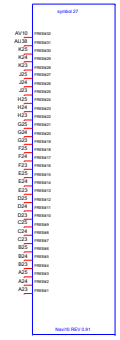
Title
Page 28. NAVI10 POWER

Size	Document Number	Rev
Custom	E411-08_FINAL	00

Date: Tuesday, June 18, 2019 Sheet 28 of 35

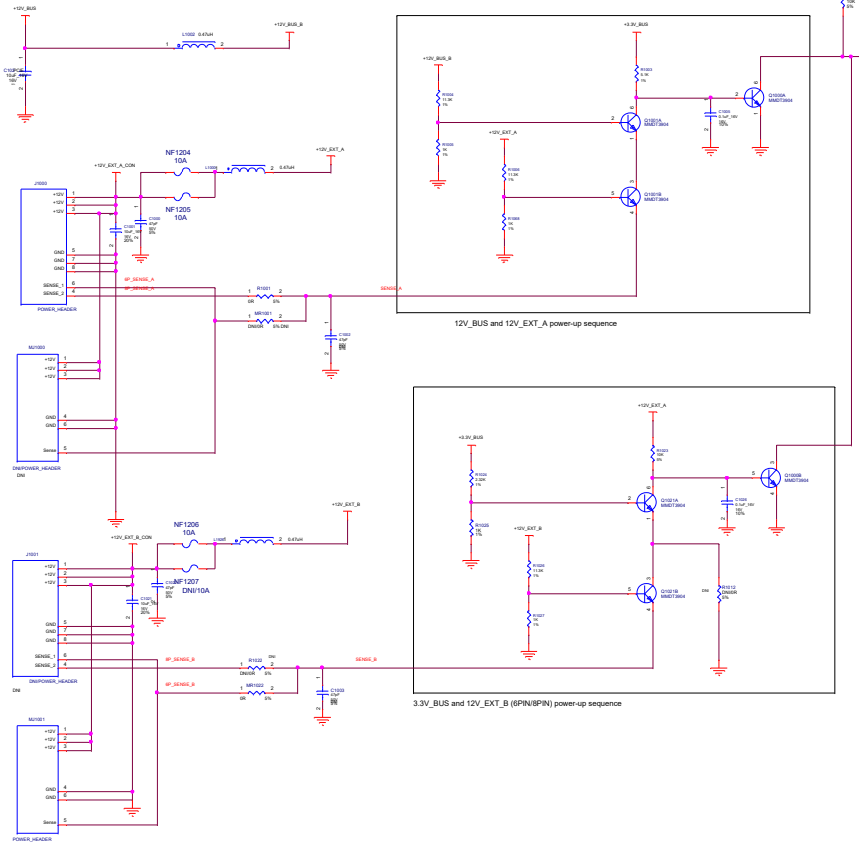
PRELIMINARY AND SUBJECT TO CHANGE





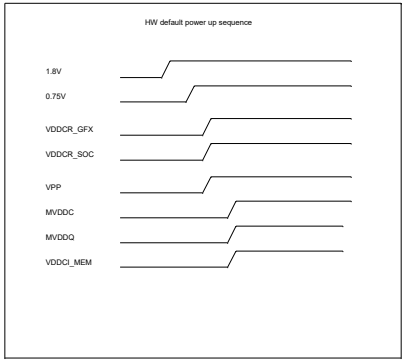
Sapphire Tech			
6F , No.18, Wenhu Street , Neihu District , Taipei City, 114, Taiwan			
Title	Page 29. NAVI10 GND		
Size: Custom	Document Number: E411-09_FINAL		Rev: 00
Date: Tuesday, June 18, 2019	Sheet 29 of 35		

PRELIMINARY AND SUBJECT TO CHANGE



12V_BUS and 12V_EXT_A power-up sequence

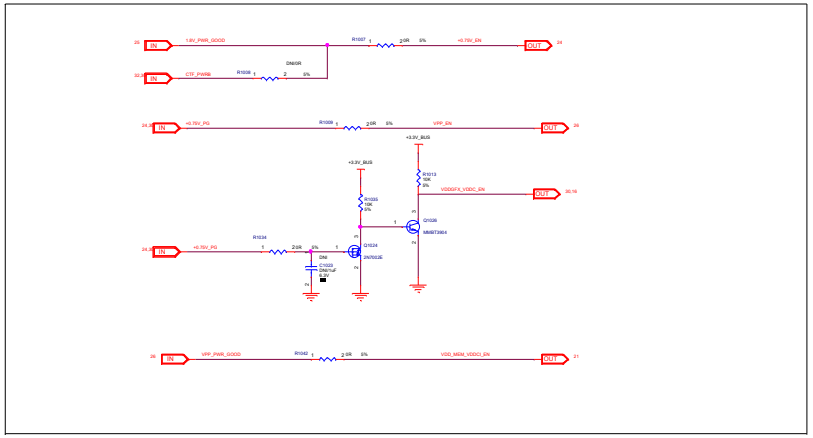
3.3V_BUS and 12V_EXT_B (6PIN/8PIN) power-up sequence



POWER UP SEQUENCE

BUS RAILS (3.3V/12V UP) -> +1.8V -> 0.75V -> VDDGFX/VDDSOC

-> VPP -> VDDCI/MVDD

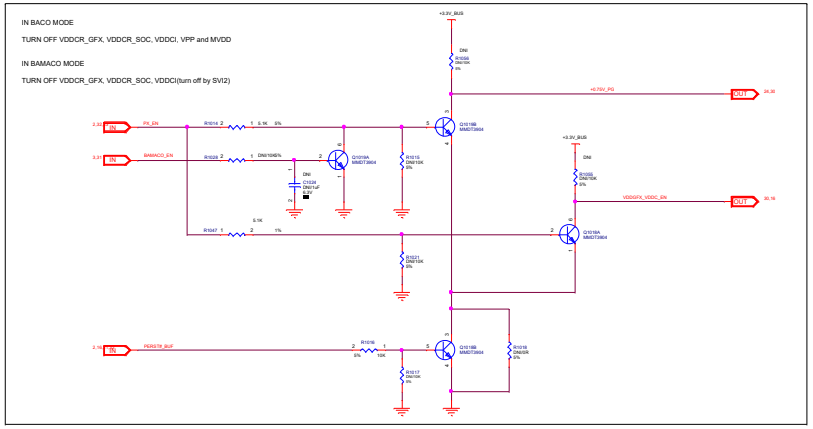


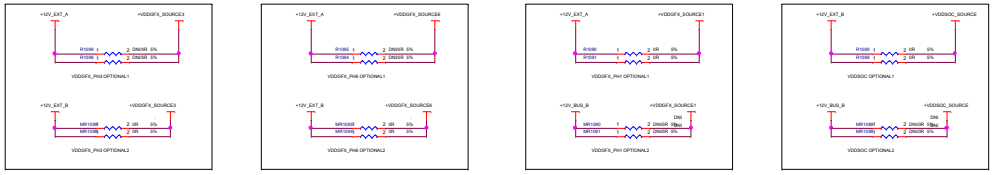
IN BACO MODE

TURN OFF VDDCR_GFX, VDDCR_SOC, VDDCI, VPP and MVDD

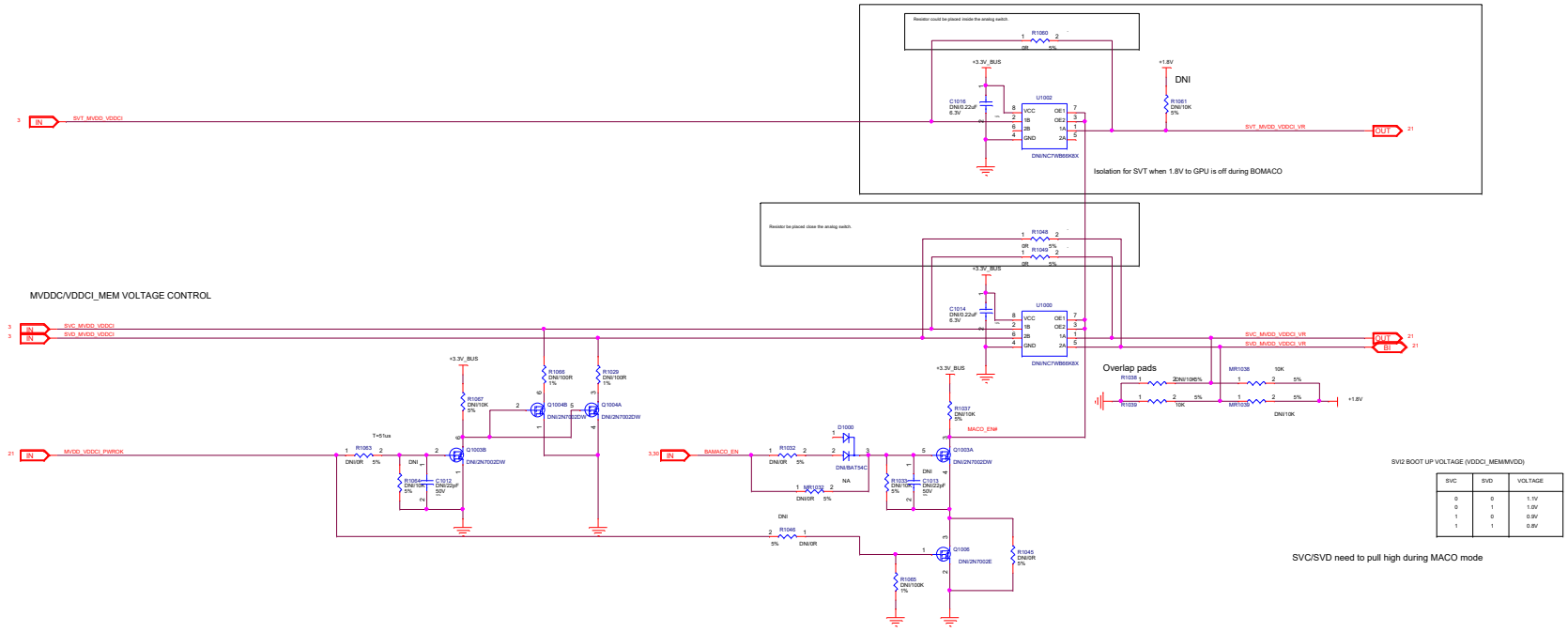
IN BAMACO MODE

TURN OFF VDDCR_GFX, VDDCR_SOC, VDDCI(turn off by SVI2)





Sapphire Tech		
6F , No.18, Wenhu Street , Neihu District , Taipei City, 114, Taiwan		
Title: Page 30. POWER MANAGEMENT		
Size: Custom	Document Number: E411-00_FINAL	Rev: 00
Date: Tuesday, June 18, 2019	Sheet 30 of 35	



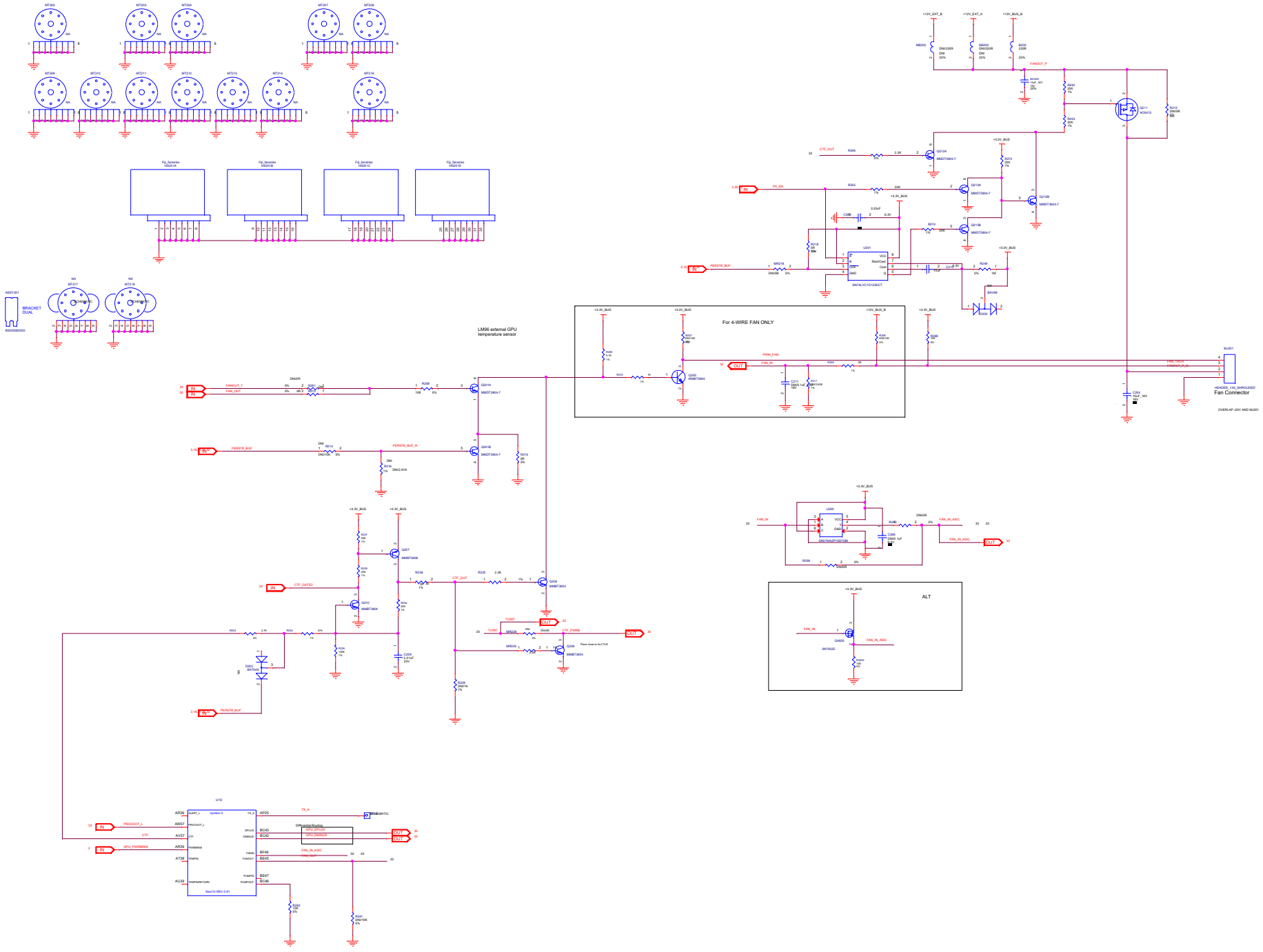
Sapphire Tech
6F , No.18, WenHu Street , NeiHu District , Taipei City, 114, Taiwan

Title
Page 31. SVI2 & BAMACO

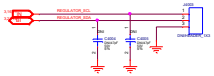
Size: Custom | Document Number: E411-00_FINAL | Rev: 00

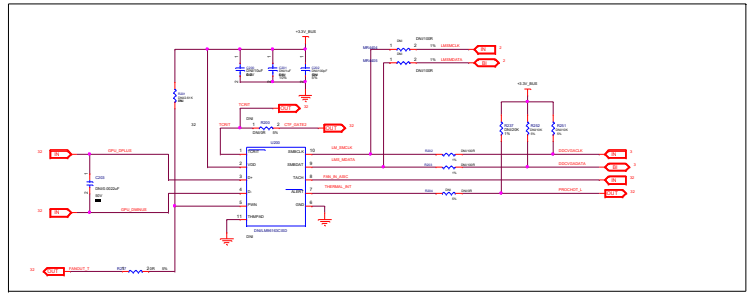
Date: Tuesday, June 18, 2019 | Sheet 31 of 35

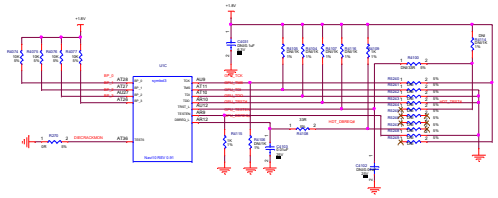
PRELIMINARY AND SUBJECT TO CHANGE

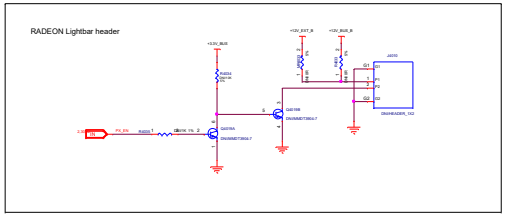


PRELIMINARY AND SUBJECT TO CHANGE





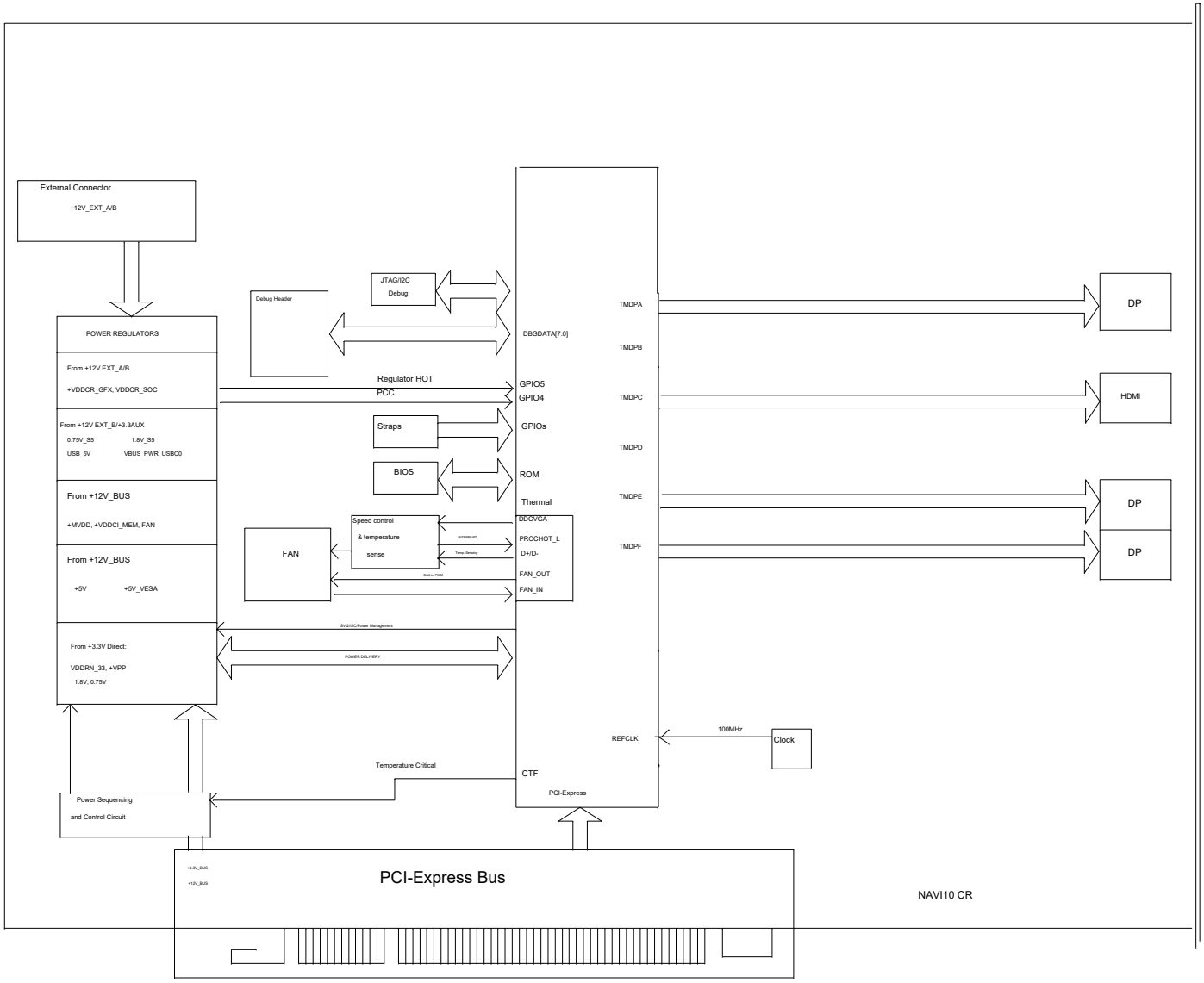




Sapphire Tech

6F ., No.16, Wenhu Street , Neihu District , Taipei City, 114, Taiwan

Title	Page 33. DEBUG		
Size: Custom	Document Number: 6411-00_FINAL		Rev: 00
Date: Tuesday, June 18, 2019	Sheet 33 of 35		



Sapphire Tech		
6F , No.18, Wenhu Street , Neihu District , Taipei City, 114, Taiwan		
Title: Page 34. BLOCK DIAGRAM		
Size: Custom	Document Number: E411-00_FINAL	Rev: 00
Date: Tuesday, June 11, 2019	Sheet 34 of 35	

1	-00A	FEB 11 2019	-00A schematics

Sapphire Tech

6F , No.18, WenHu Street , NeiHu District , Taipei City, 114, Taiwan

Title	Page 35. REVISION HISTORY	
Size: Custom	Document Number: E411-00_FINAL	Rev: 00
Date: Tuesday, June 11, 2019	Sheet 35 of 35	