PRELIMINARY AND SUBJECT TO CHANGE

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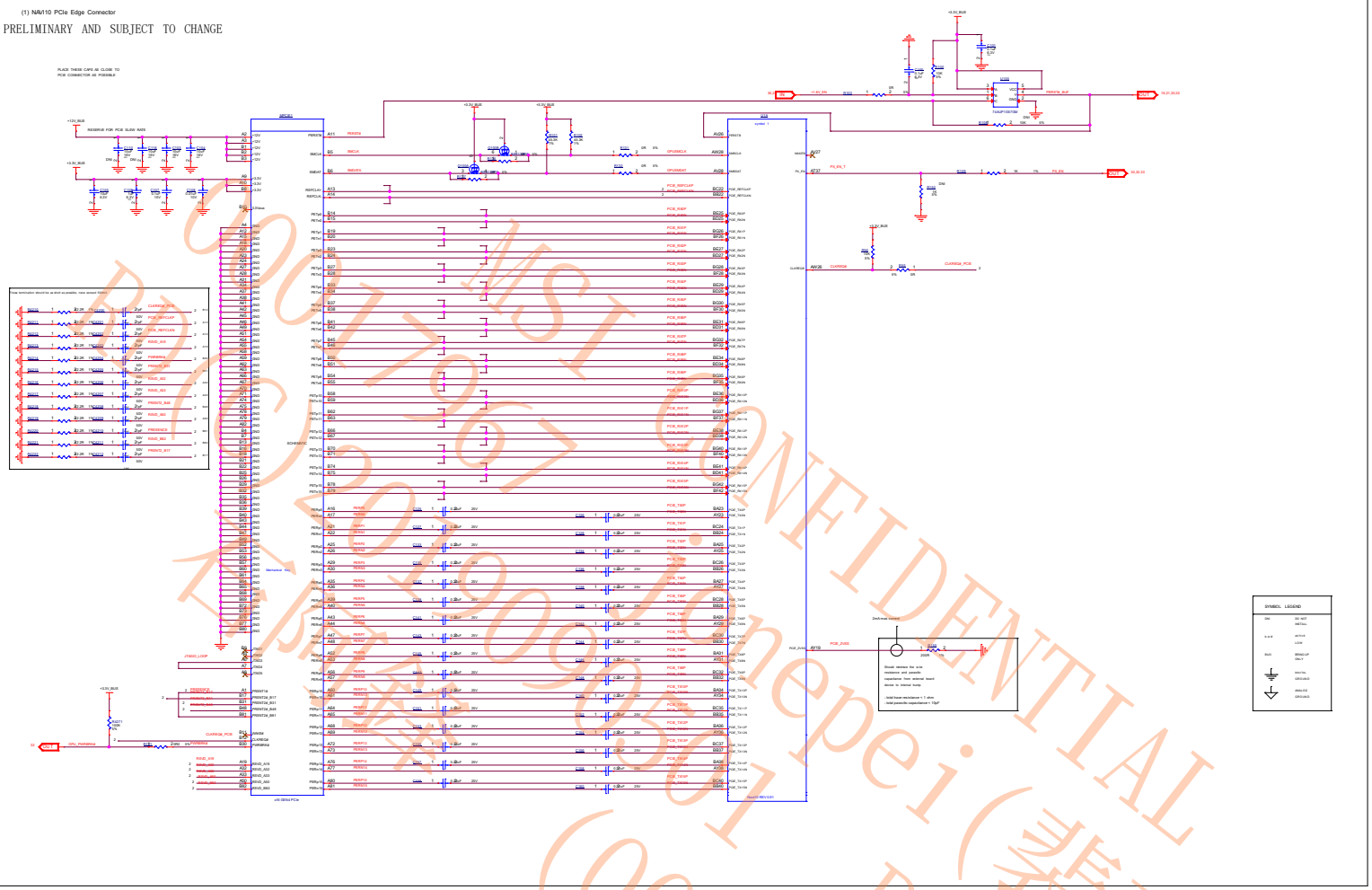
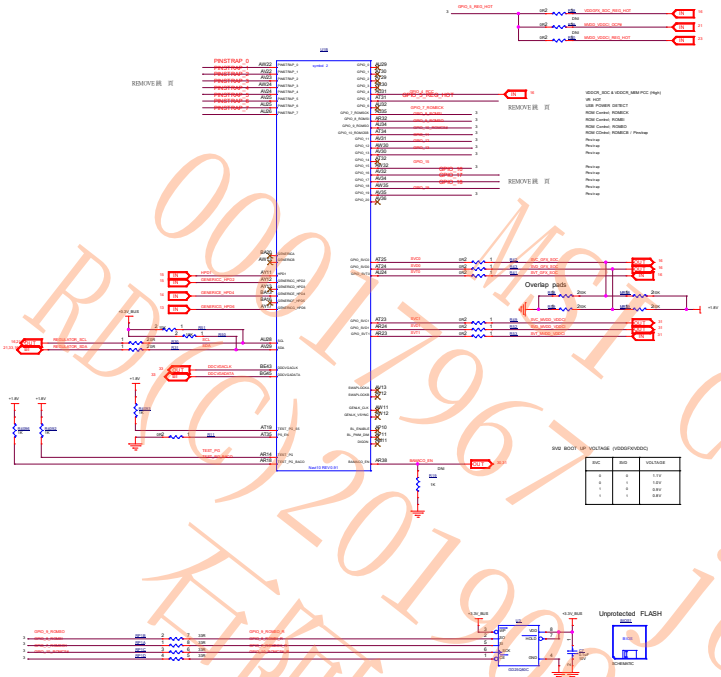
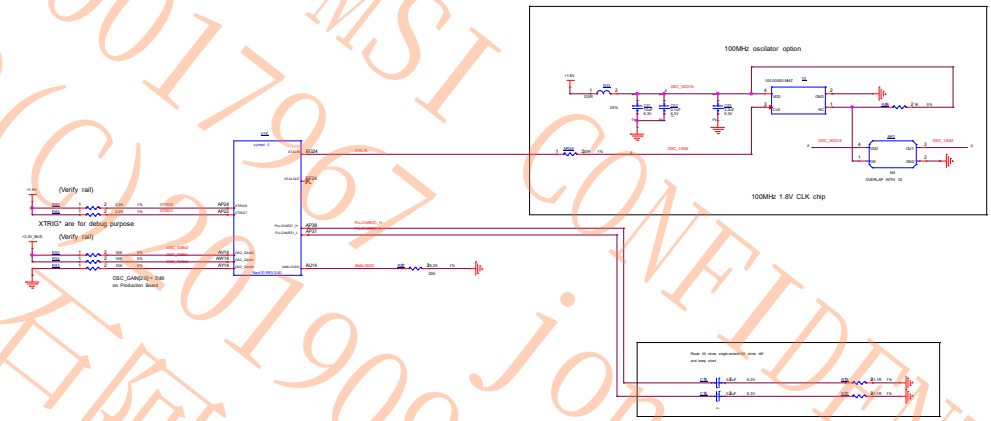
PRELIMINARY AND SUBJECT TO CHANGE

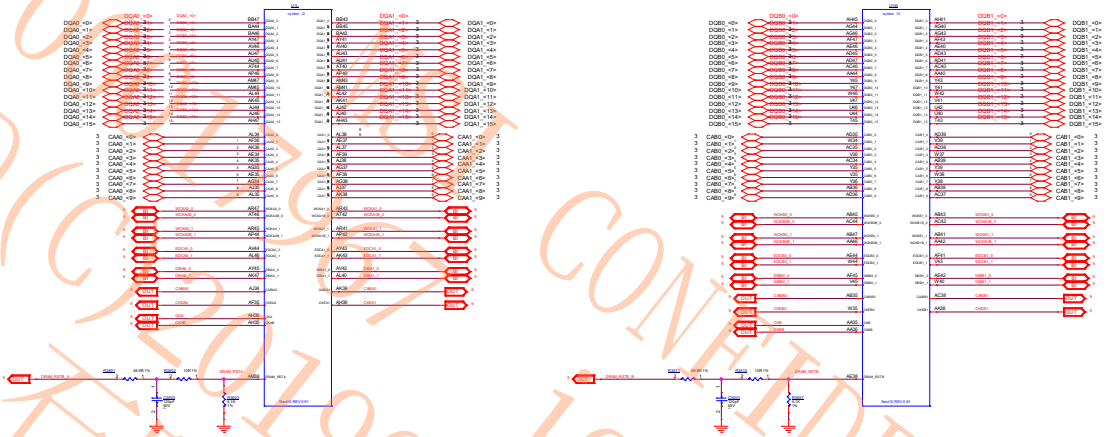




Note: Internal PU/PD at GPIO pad is ~40k
ohm(with in 14nm design spec

User		Internal Default Value	Definition
BIF		0	STRAP_BIF_GEN4_DIS_A 0: PCIe GEN 4 supported 1: PCIe GEN 4 not supported
		0	PINSTRAP_BIF_CLK_PM_EN 0: CLKREQ# pin-w management capability is disabled 1: CLKREQ# pin-w management capability is enabled
		0	PINSTRAP_BIF_LC_TX_SWING
		0	PINSTRAP_BIF_VGA_DIS 0: VGAcontroller reportly enabled 1: The device wou1ldbe recognized as the system's VGAcontroller
DCE		0 0 0	PINSTRAP_AUID_PORT_CONN[2:0] Number of audio-capable display outputs 0: All endpoints connected 1: 5 endpoints connected 2: 4 endpoints connected 3: 3 endpoints connected 4: 3 endpoints connected 5: 2 endpoints connected 6: 1 endpoint connected 7: 0 endpoints connected
		0 0	PINSTRAP_AUD[1:0] 1: Audio for DisplayPort only 2:Audio for DisplayPort and HDMI if dongle is detected 3:Audio for DisplayPort and native HDMI
Platform		0 0 0	
SMU		1 0 1	
			PINSTRAP_SMBUS_ADDR 0: 0x01h 1: 0x03h
		1	PINSTRAP_BIOS_ROM_EN 0: Disable the external BIOS ROM device 1: Enable the external BIOS ROM device





GDDR6x16 CHAB Memory

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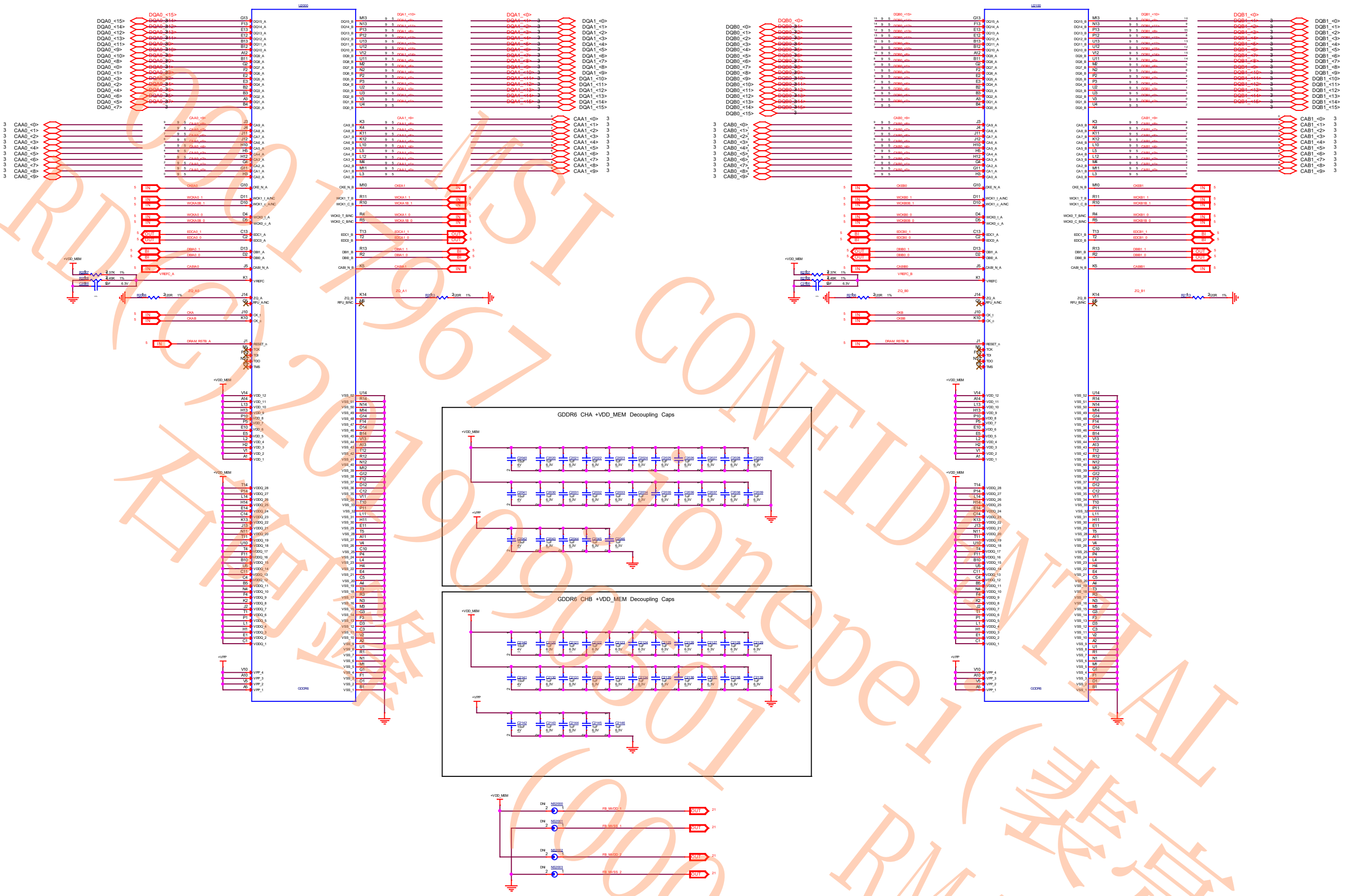

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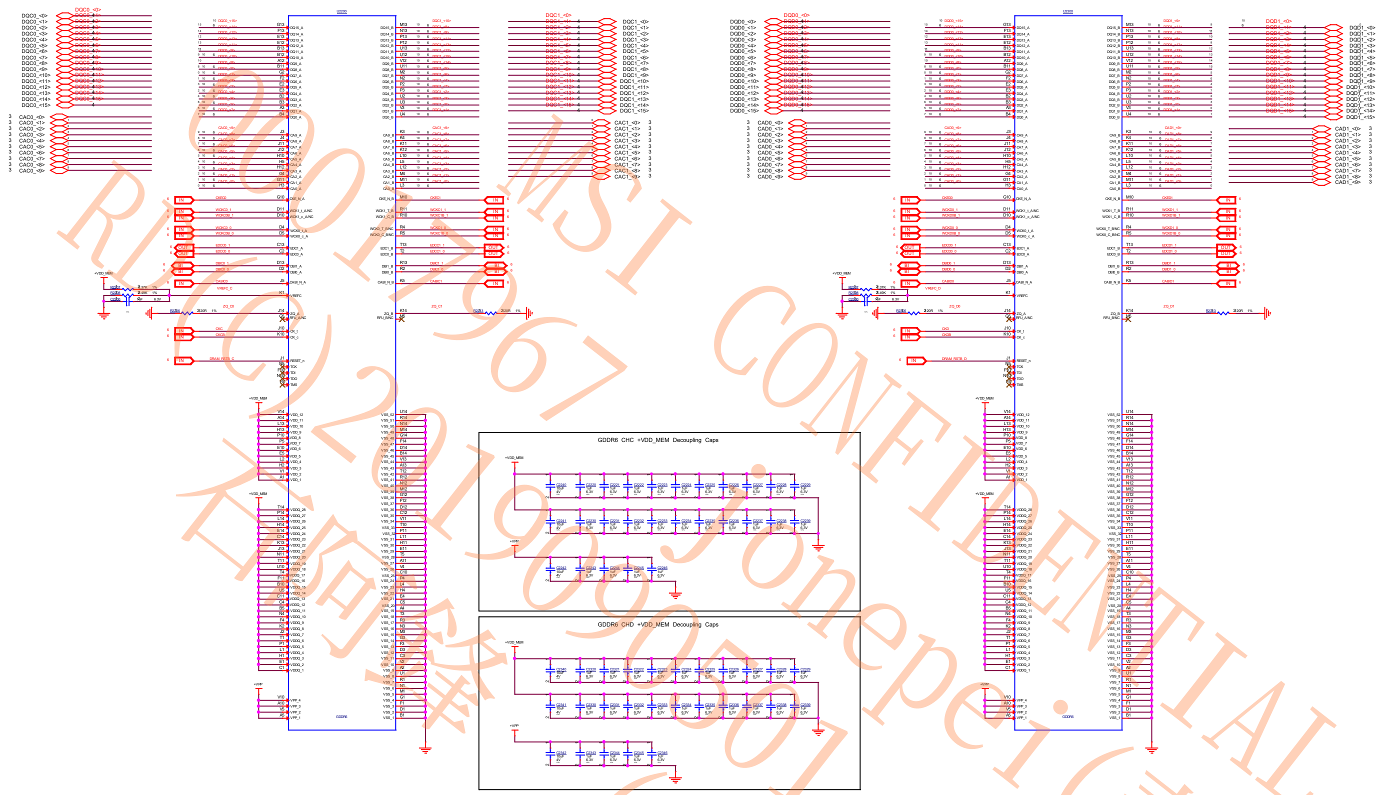

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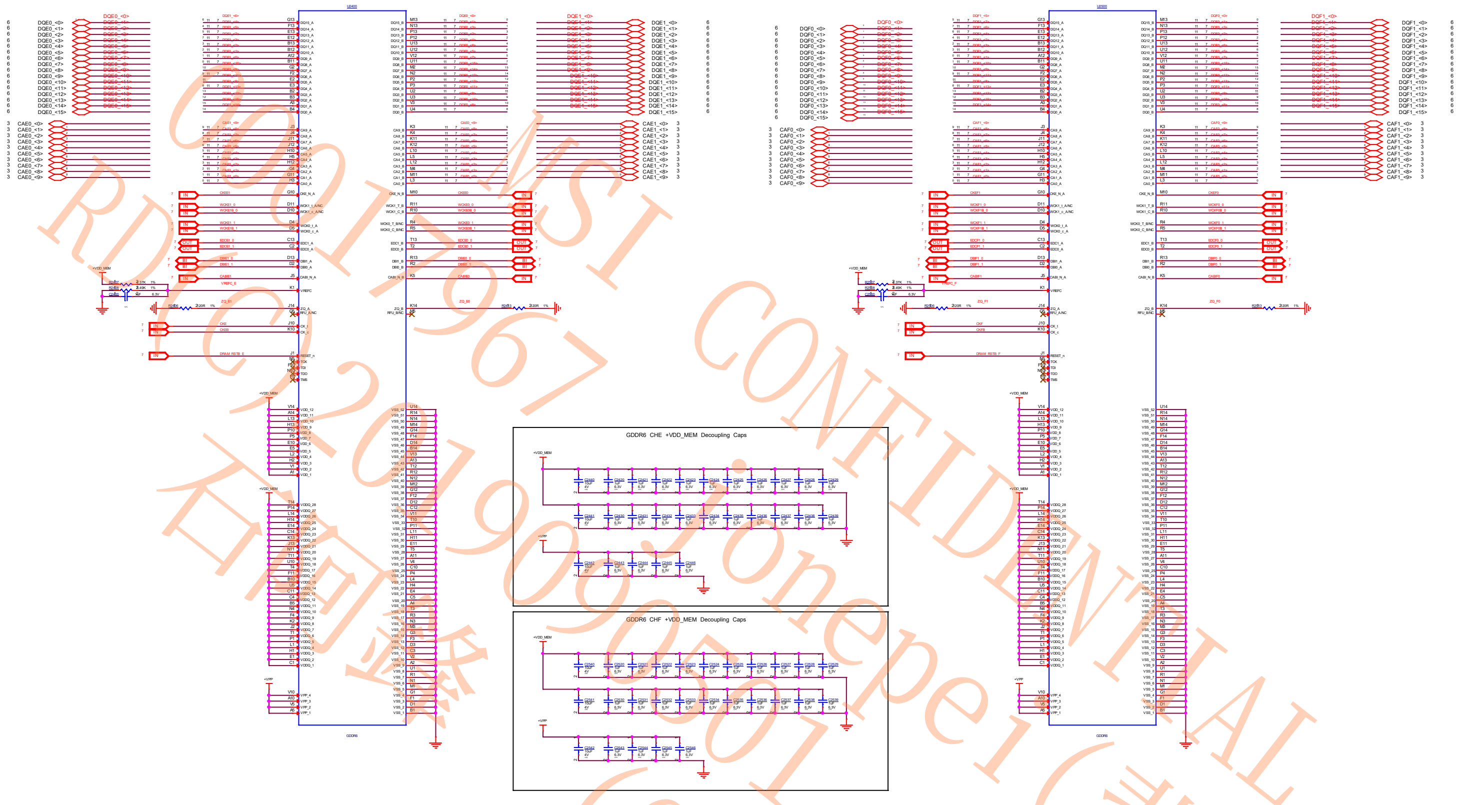

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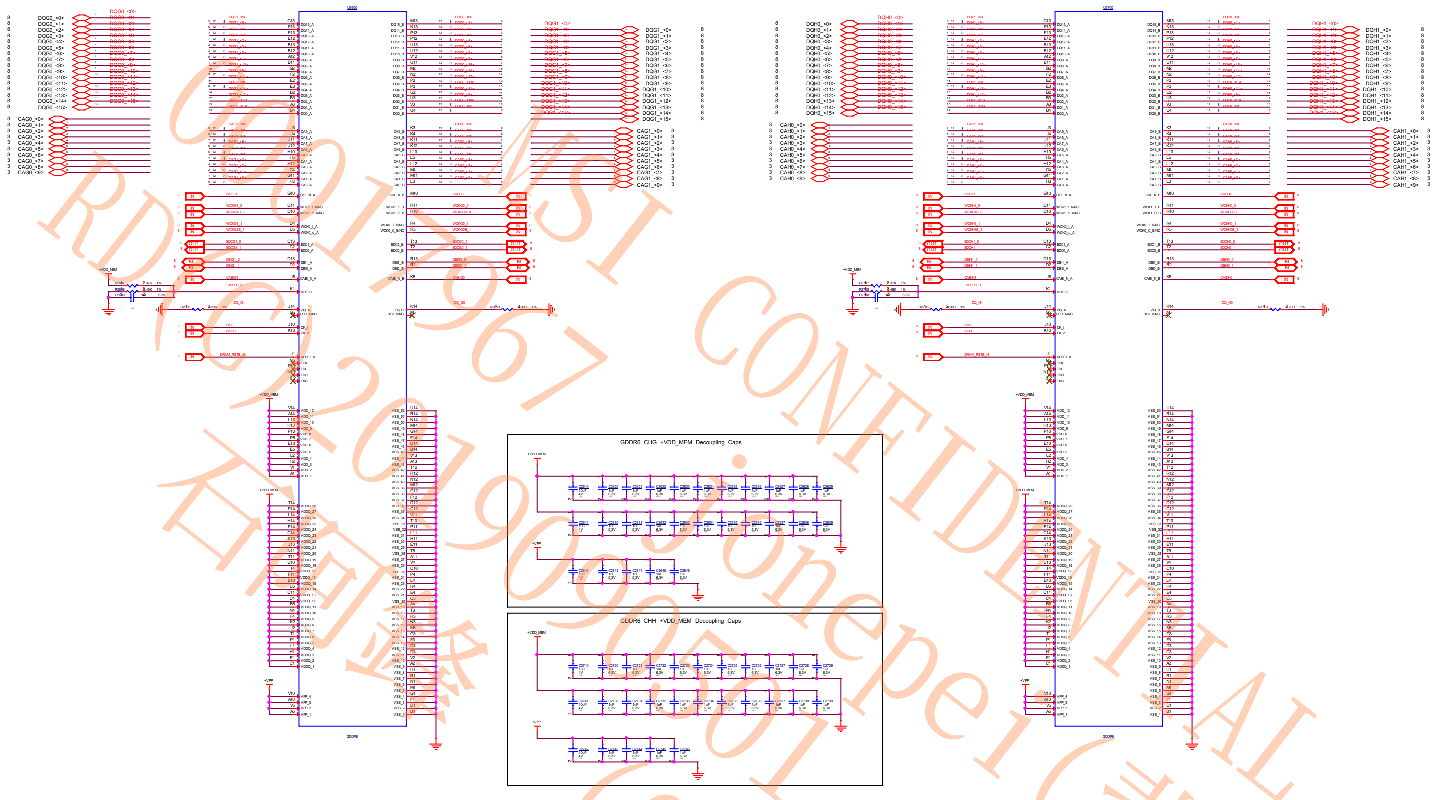
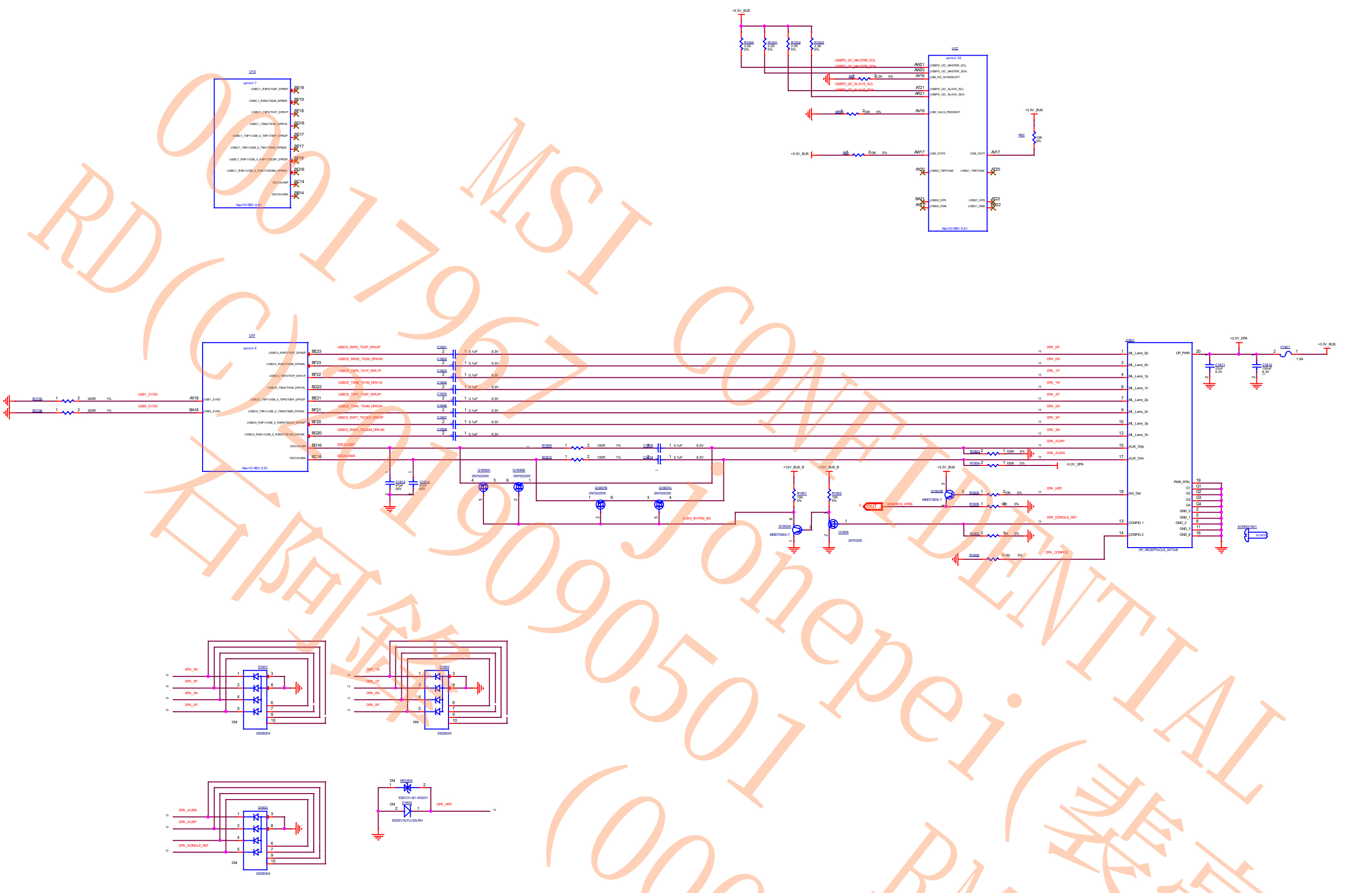


NAVI10 TMDP A/B

PRELIMINARY AND SUBJECT TO CHANGE



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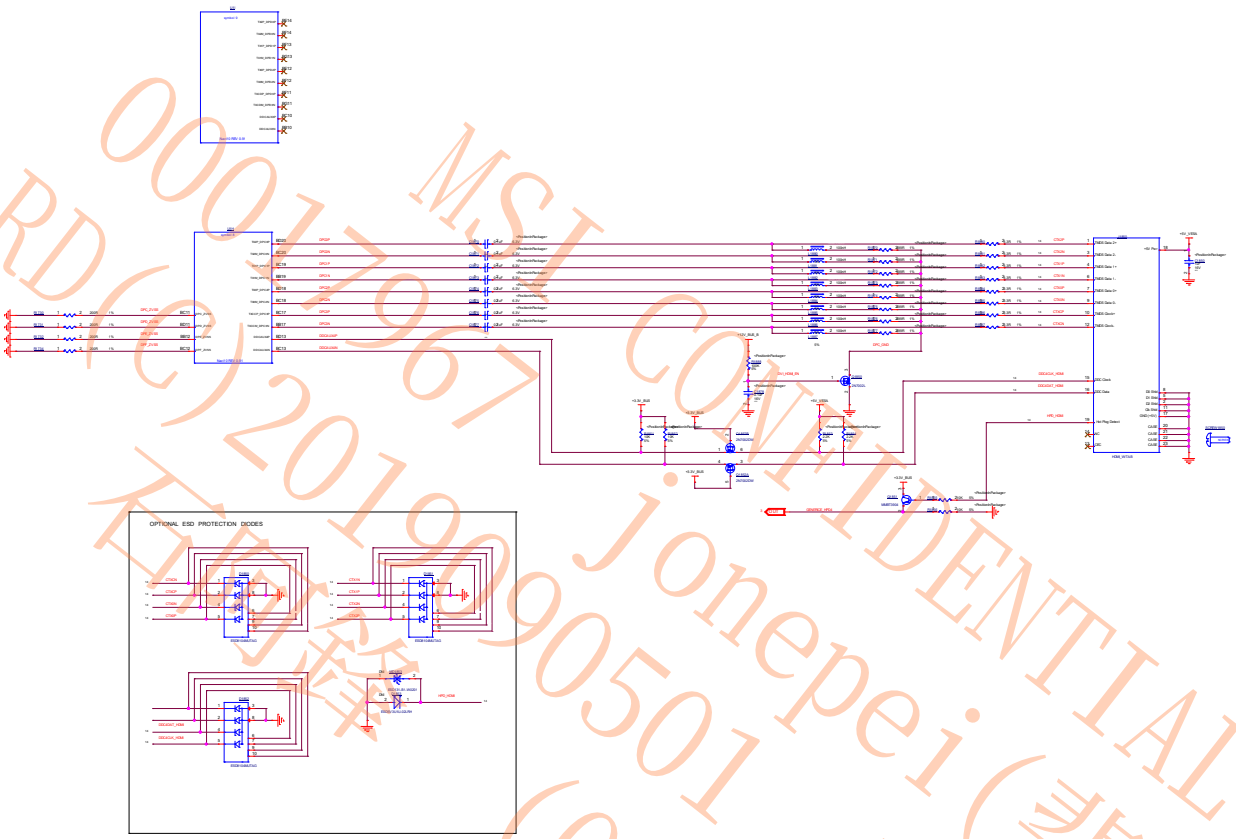
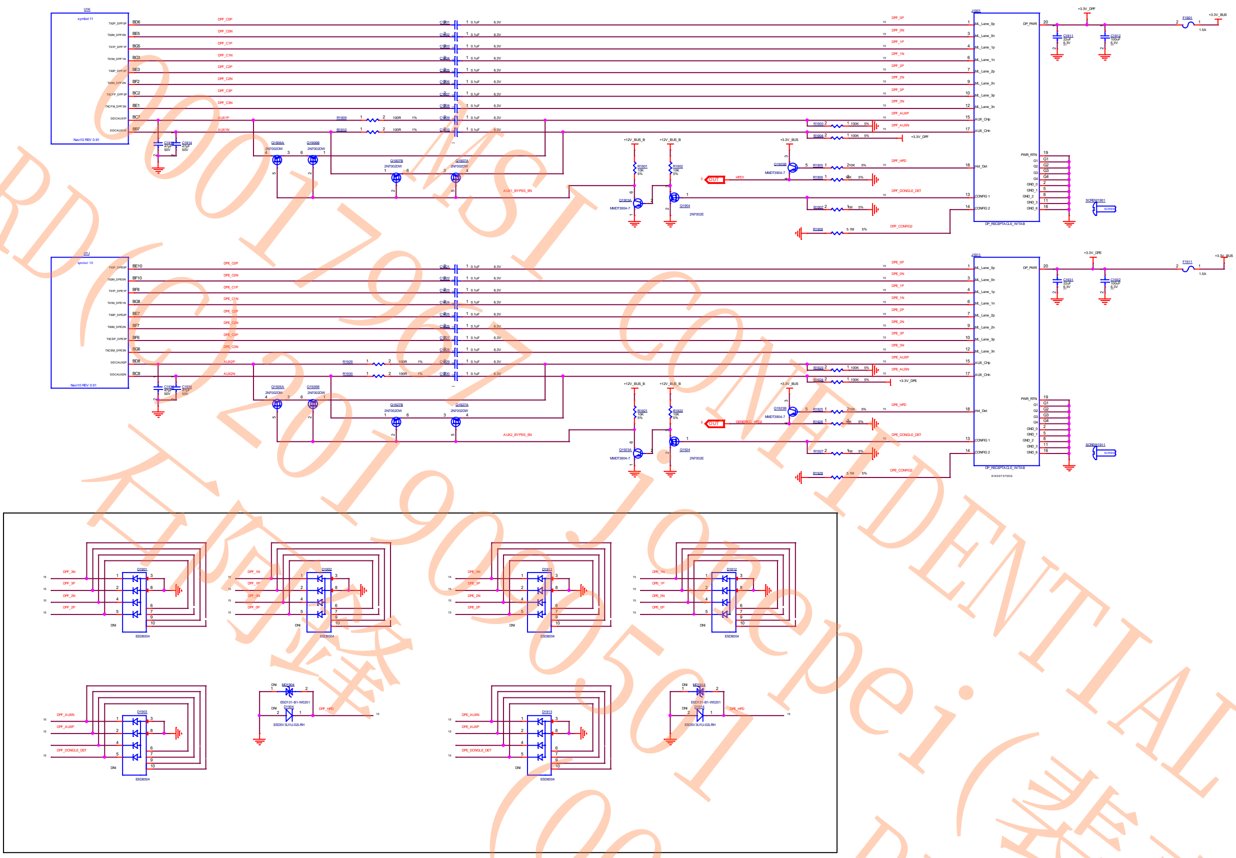
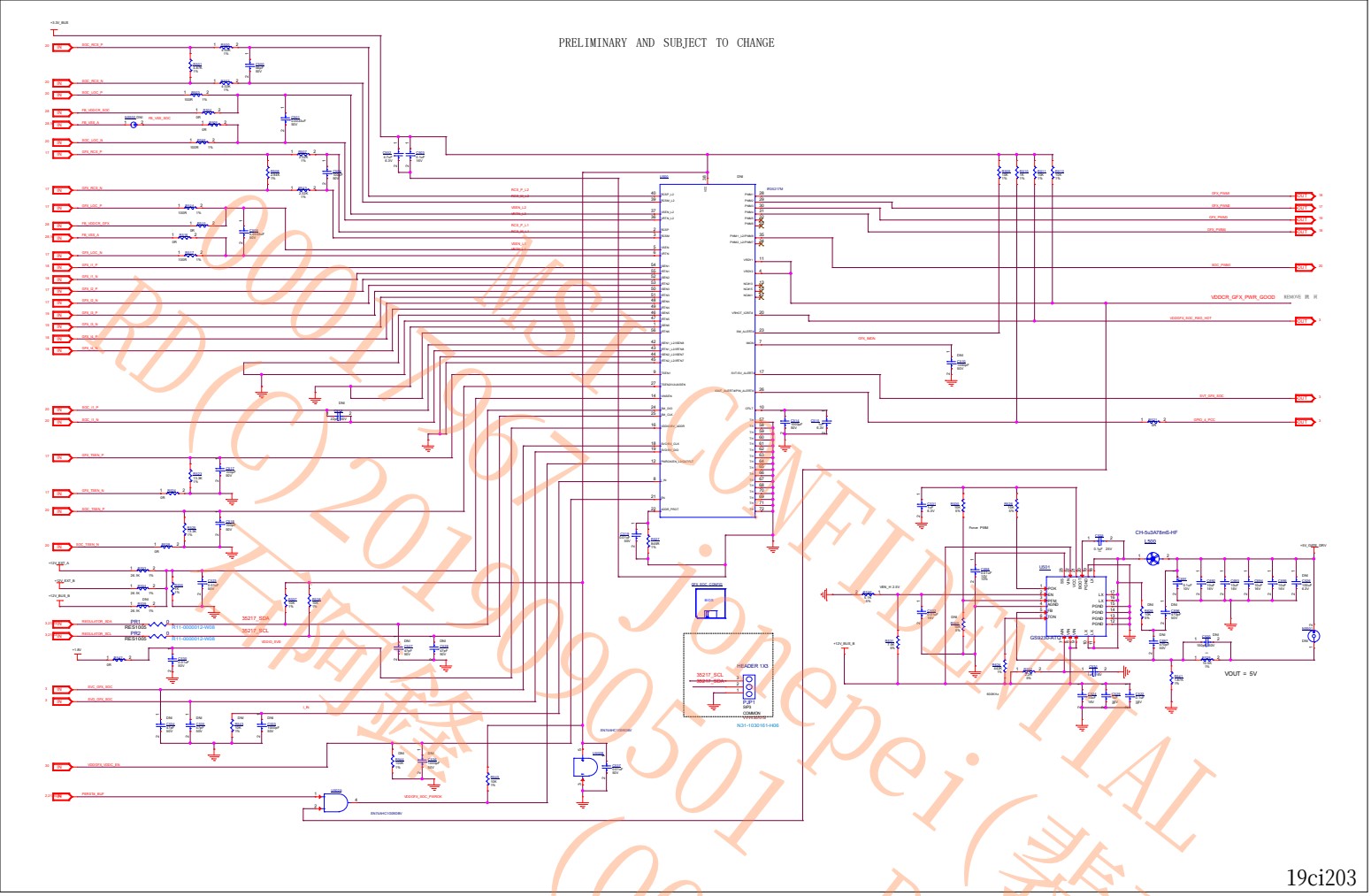


(9) NAVI10 TMDP E/F





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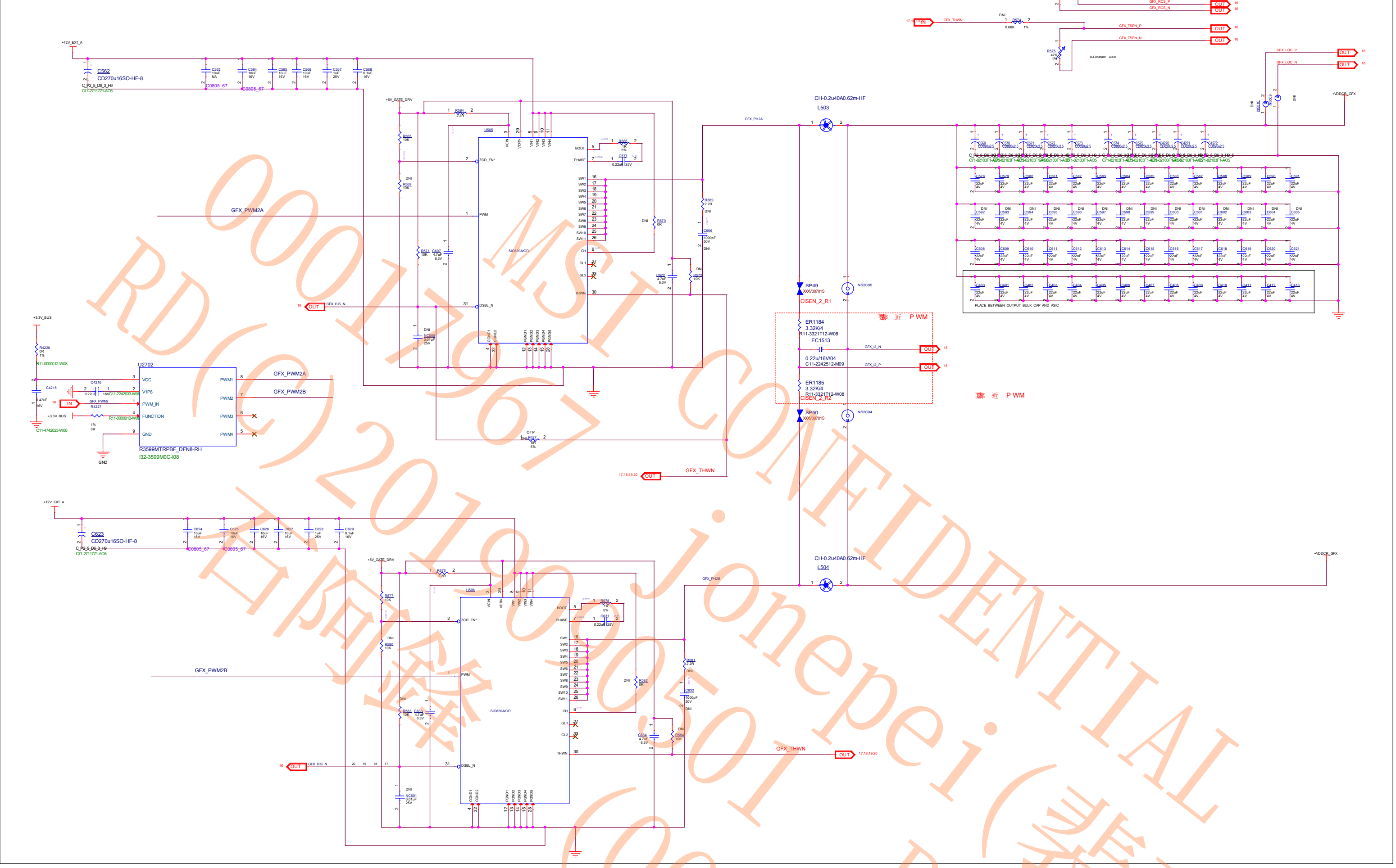

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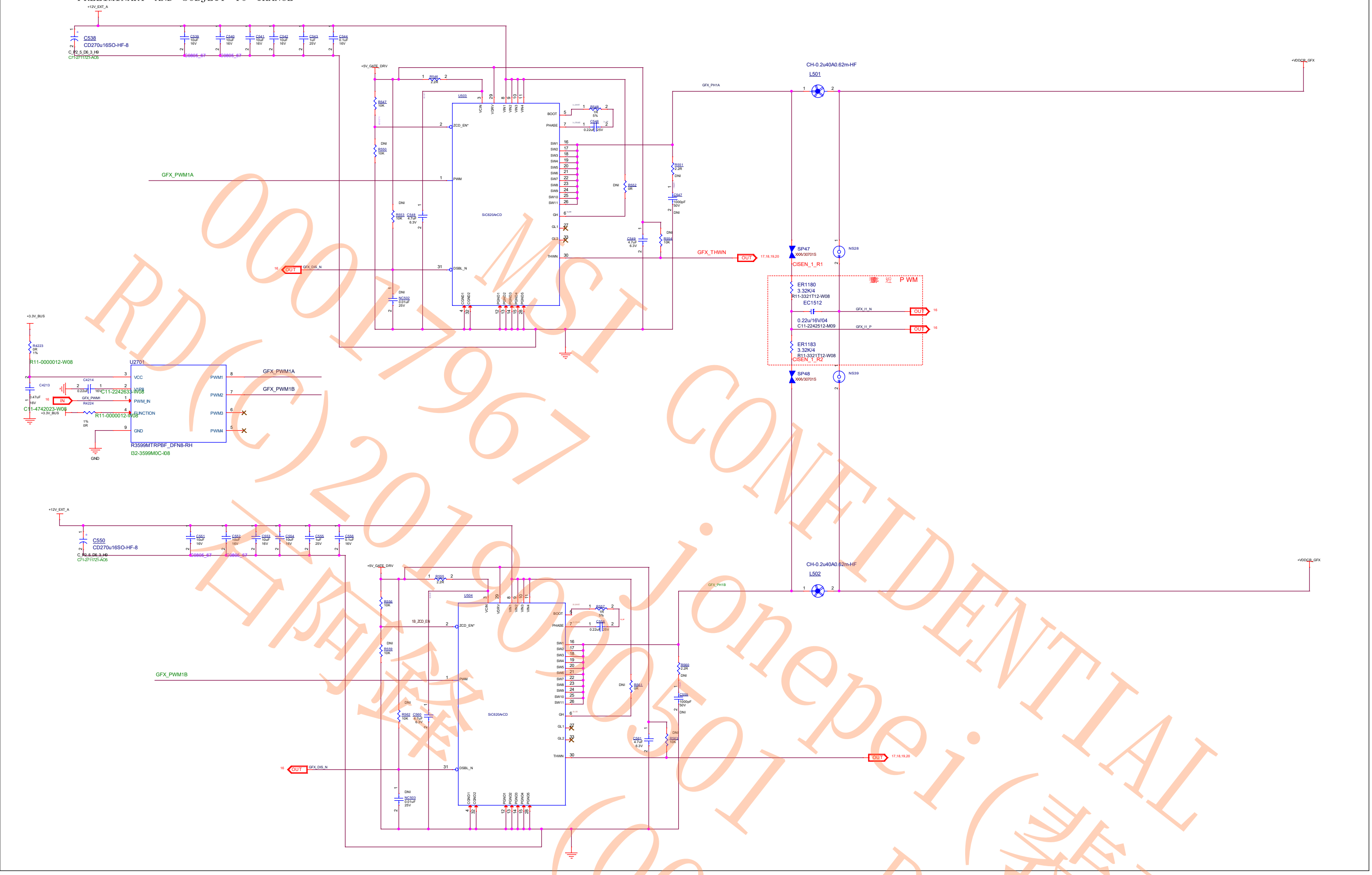

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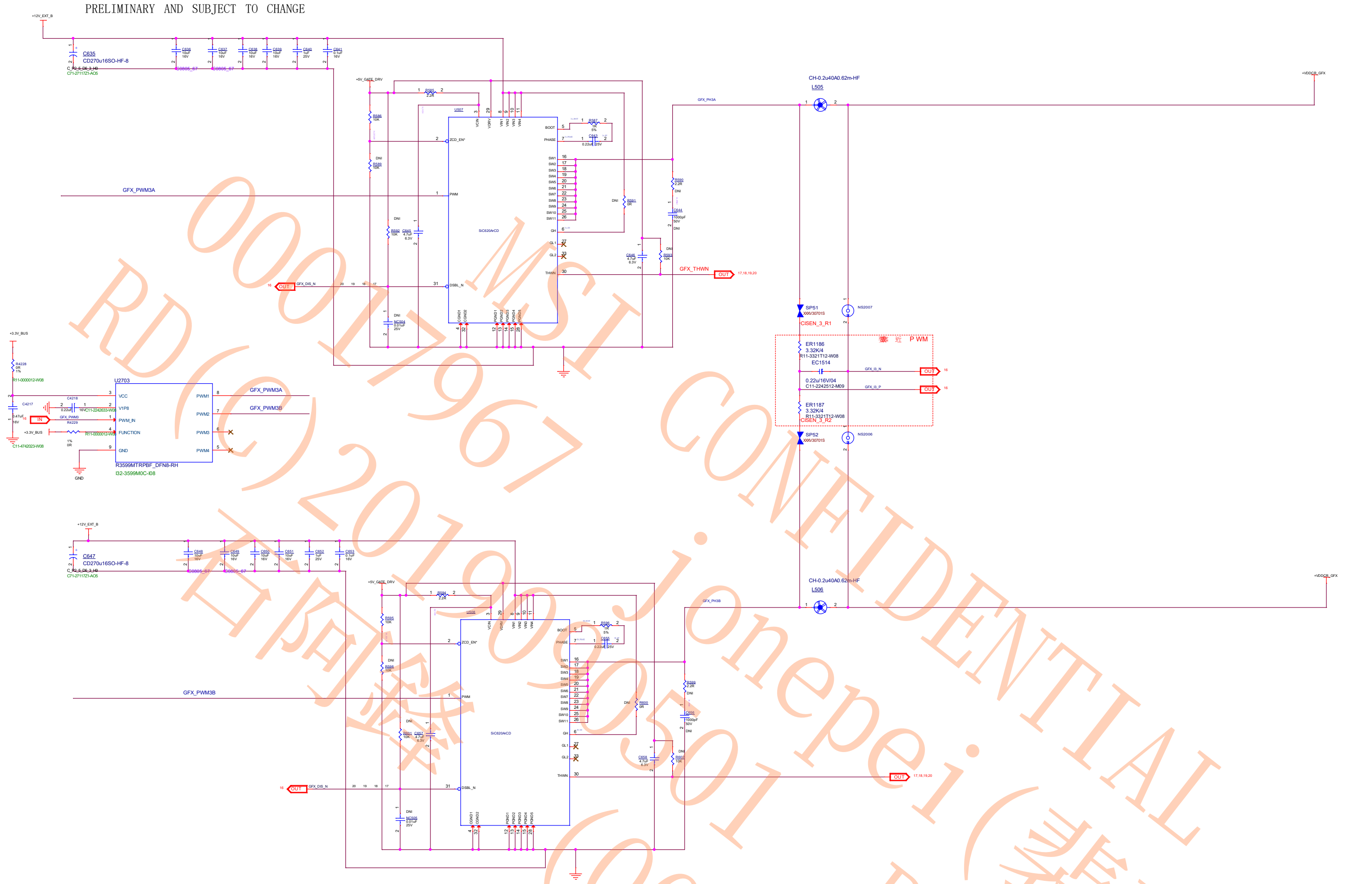

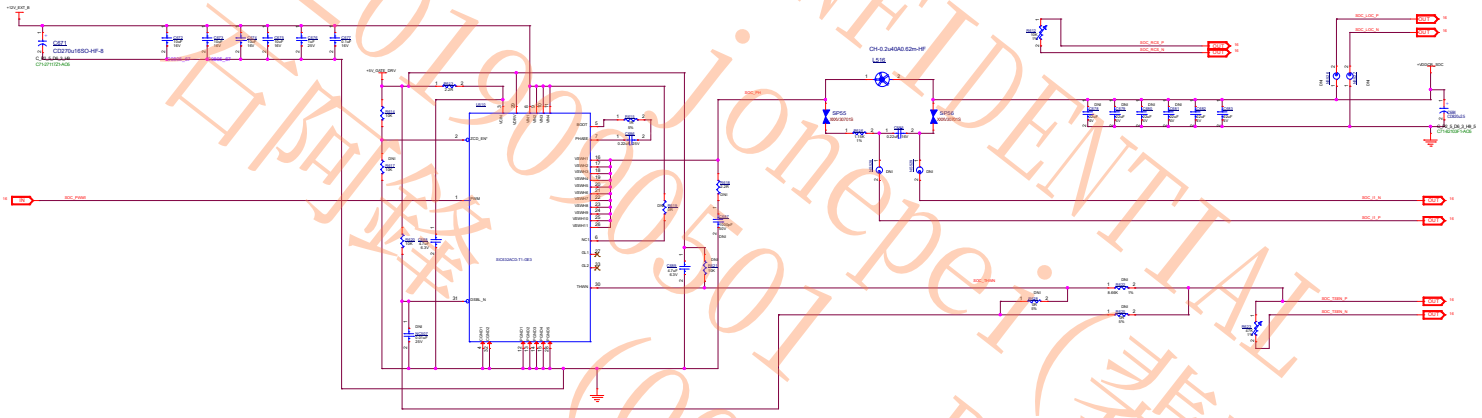

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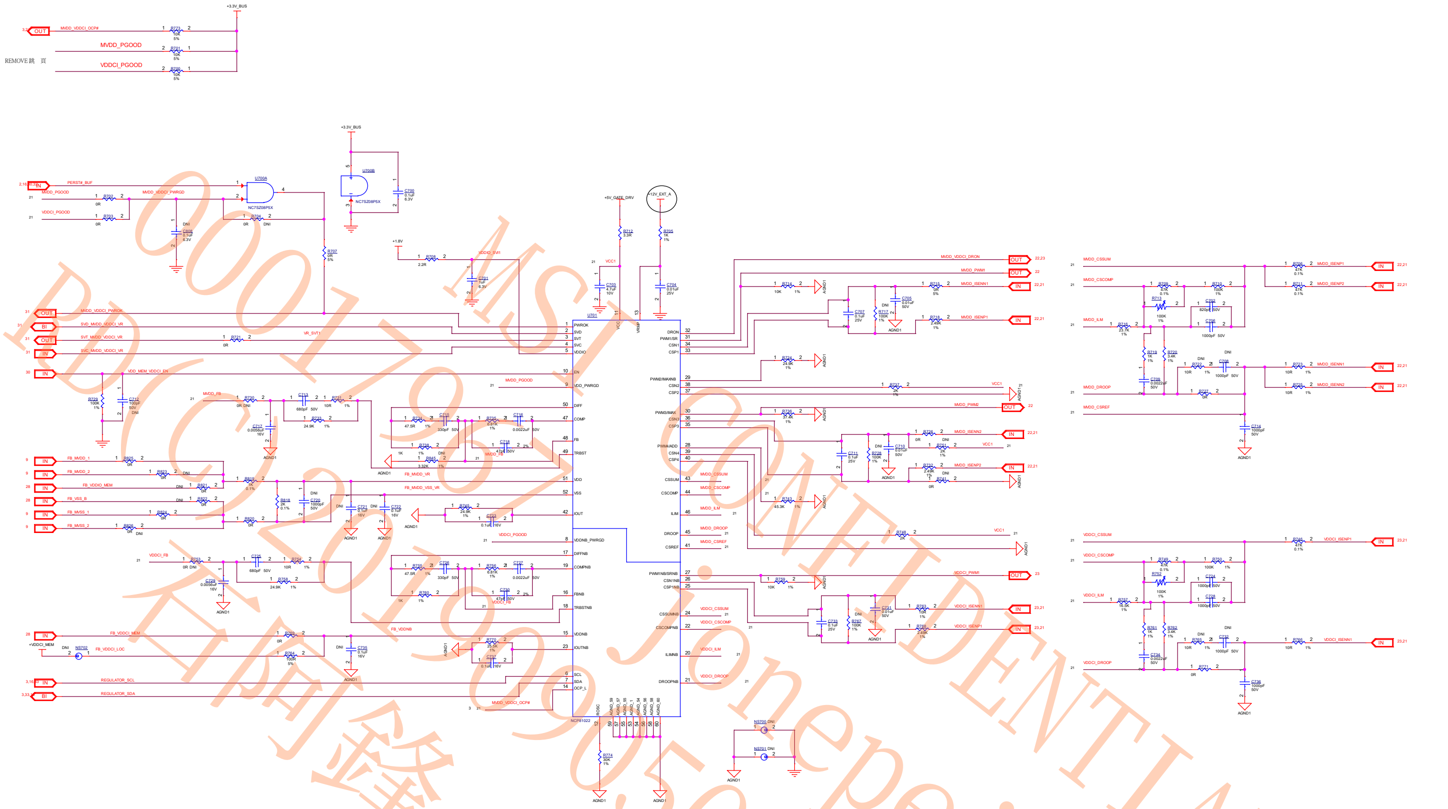

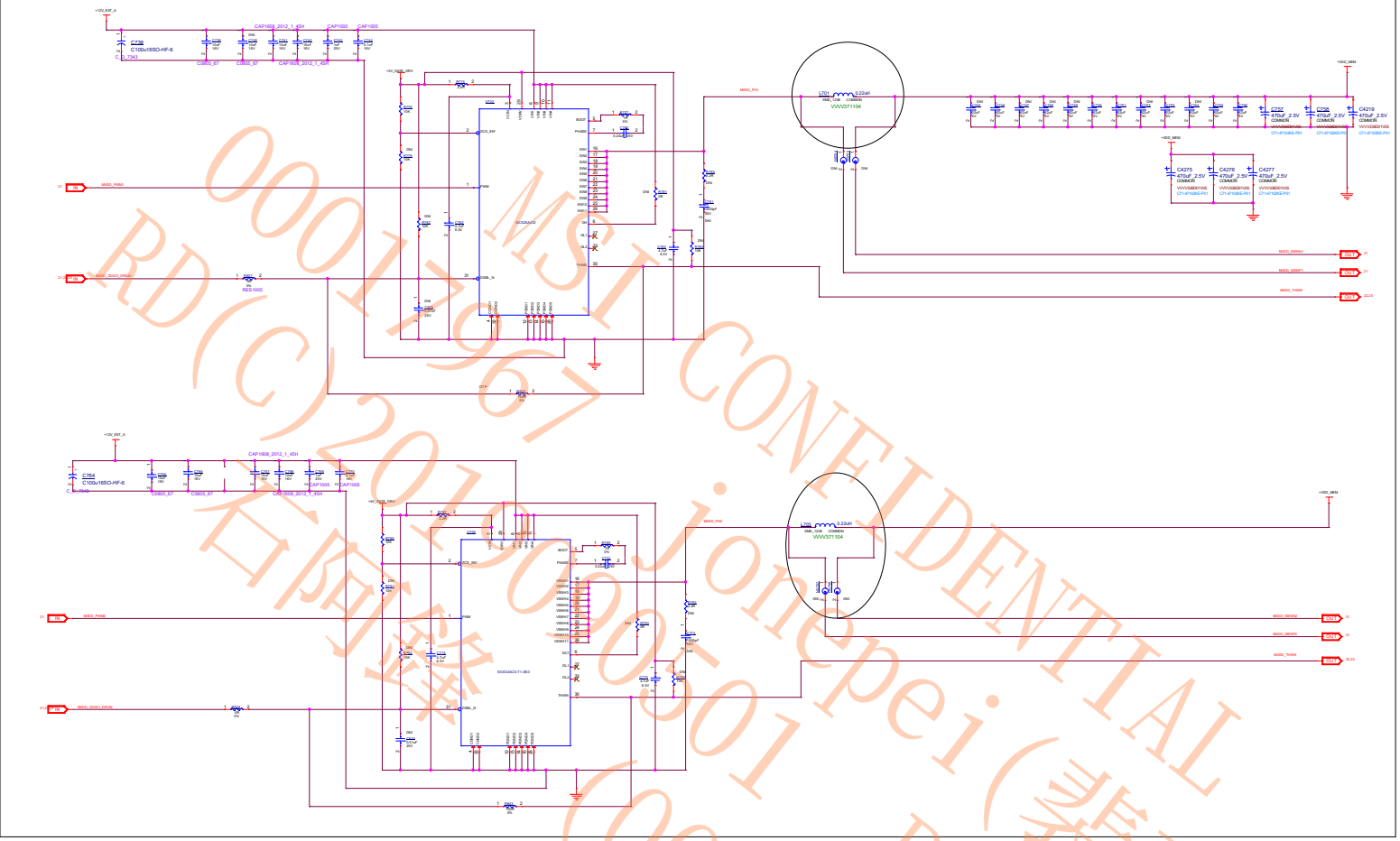

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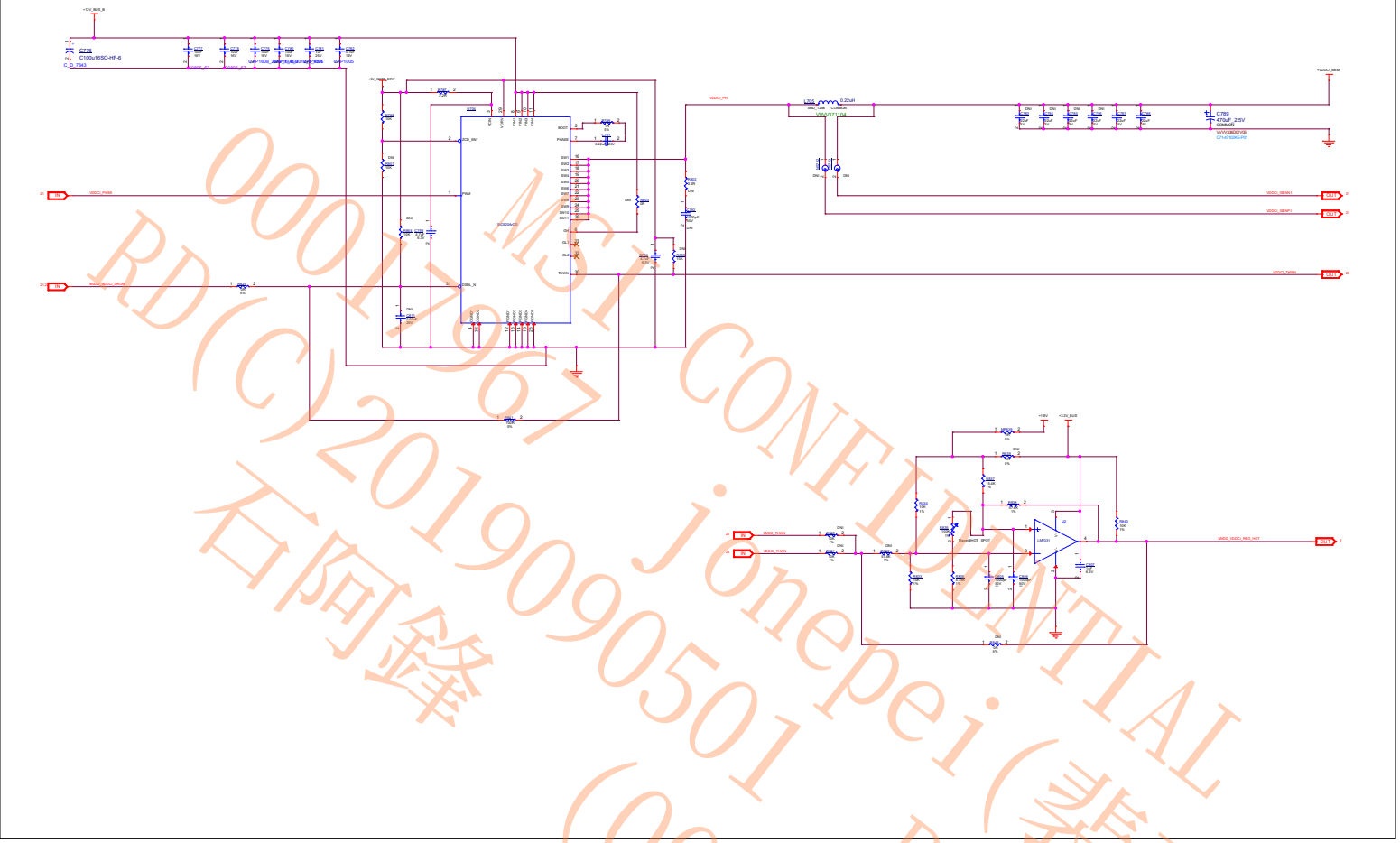

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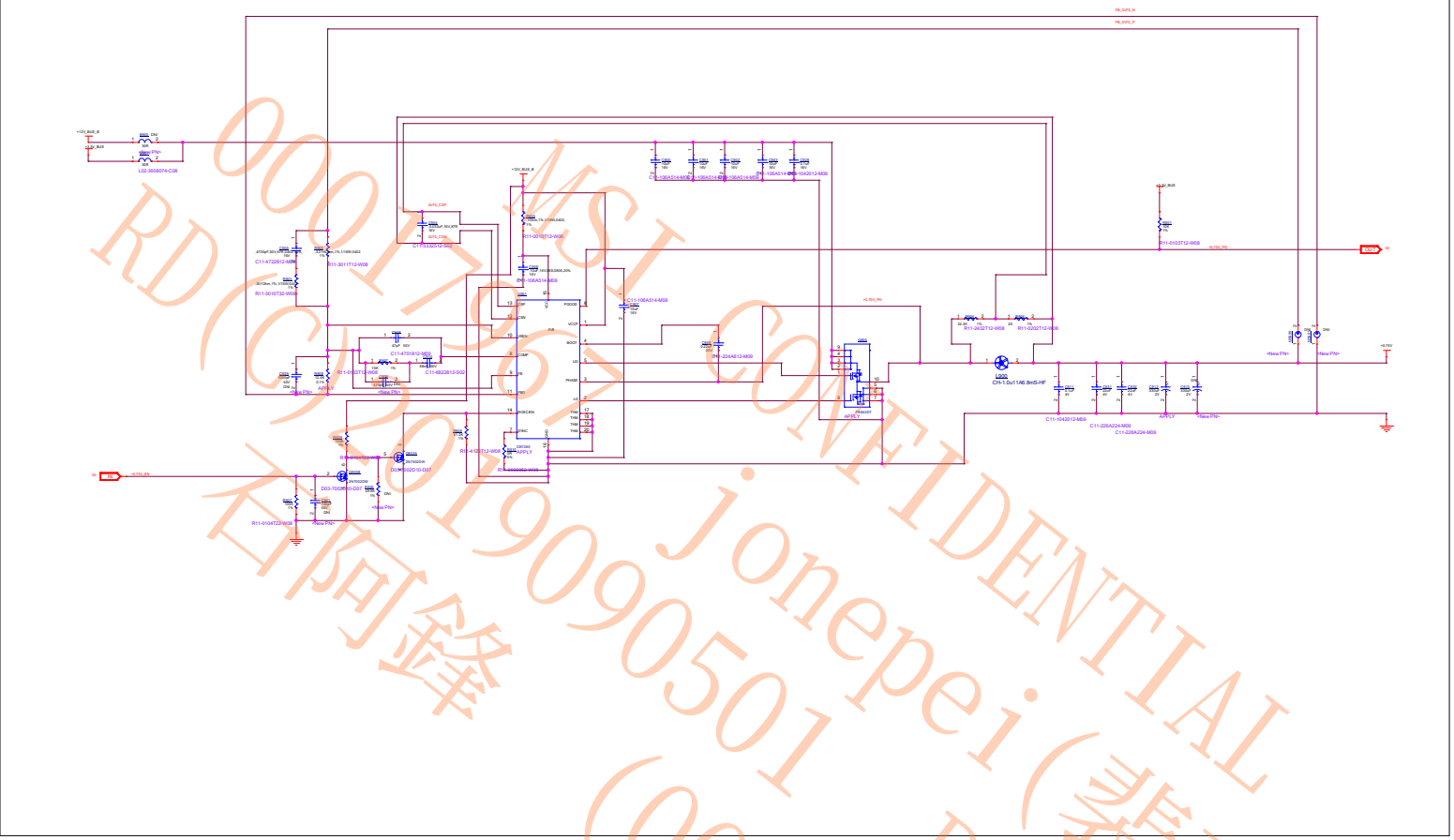

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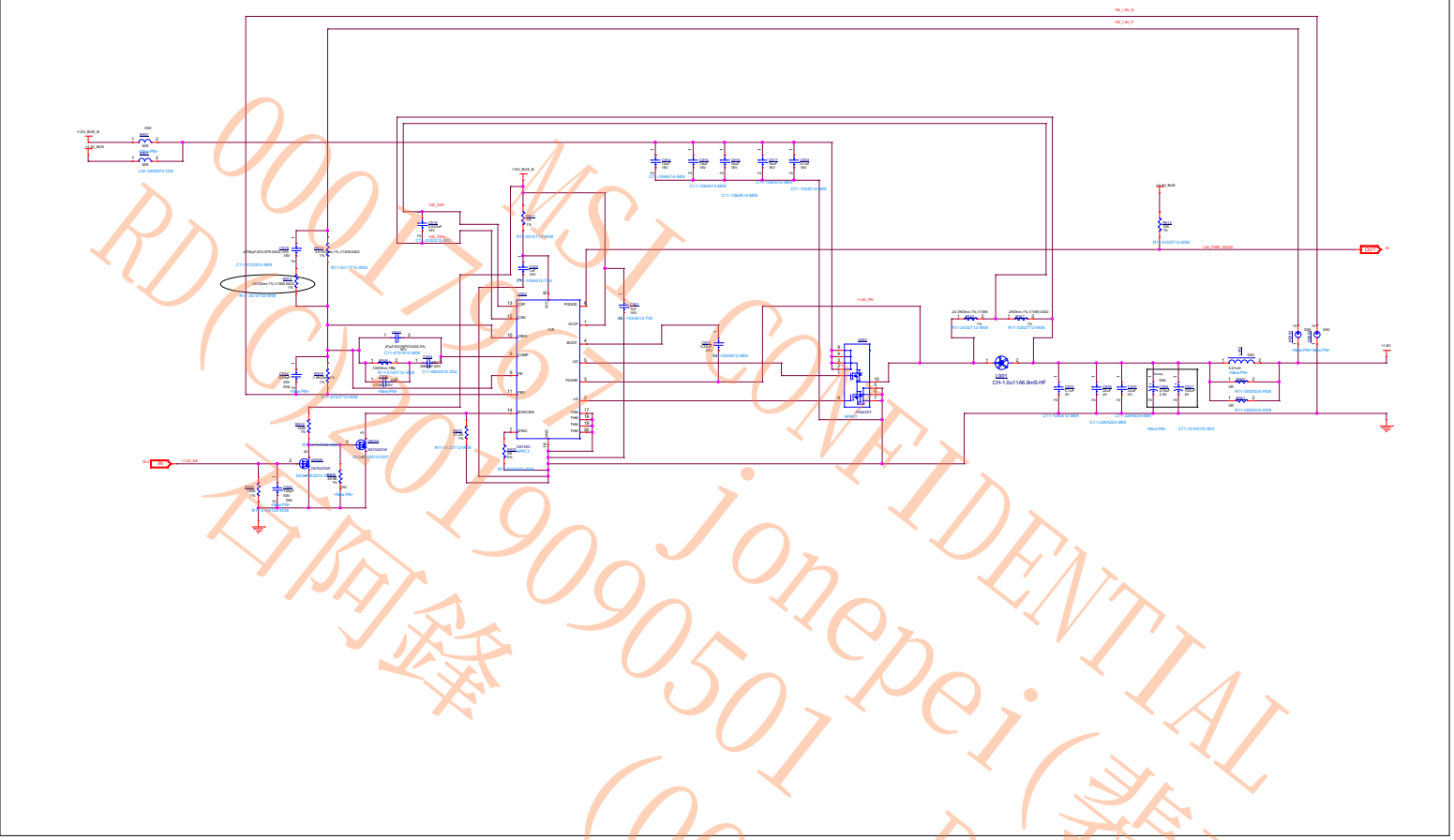
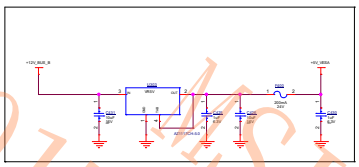
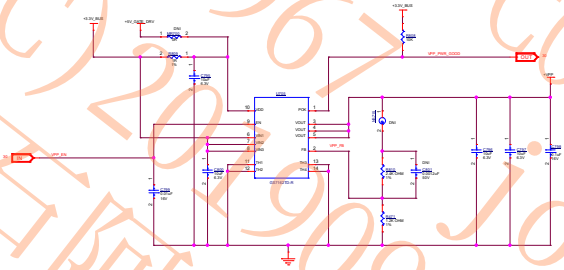
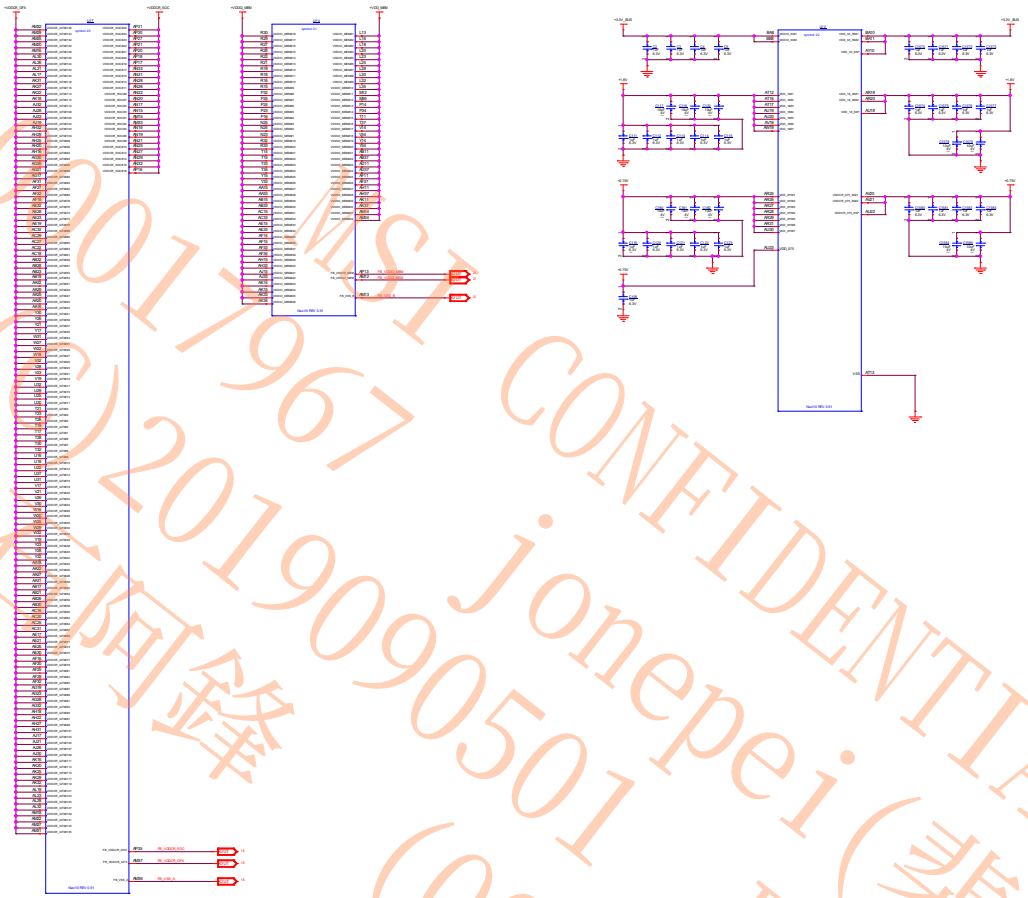


REGULATOR FOR +5V RAILS

IOUT = 50mA







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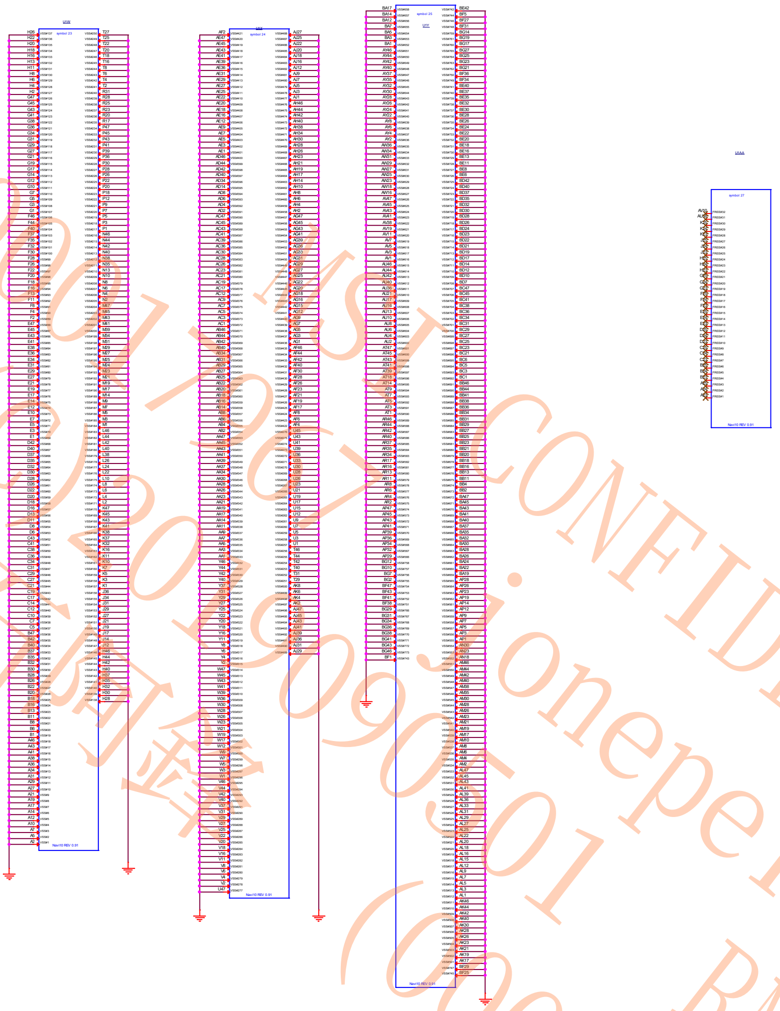

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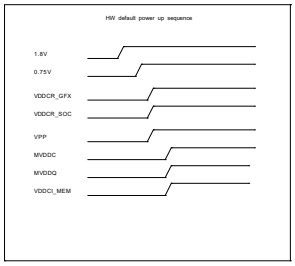

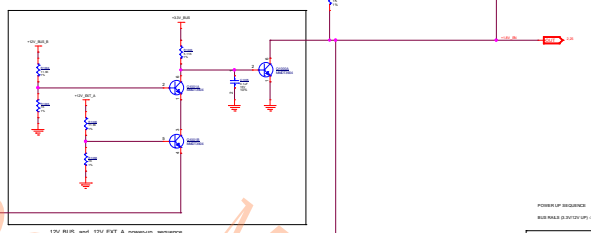

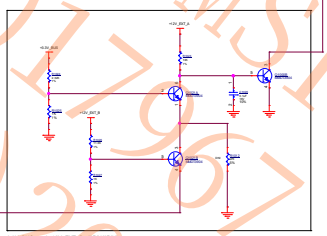

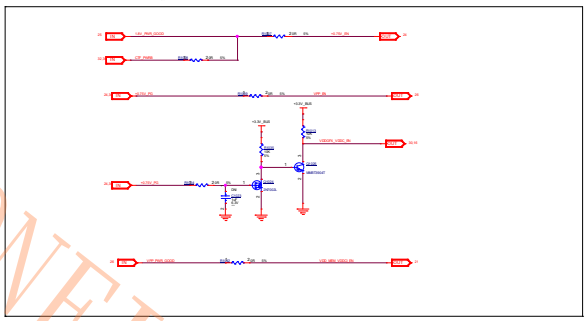

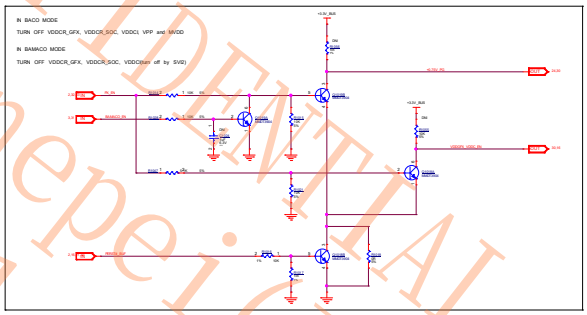

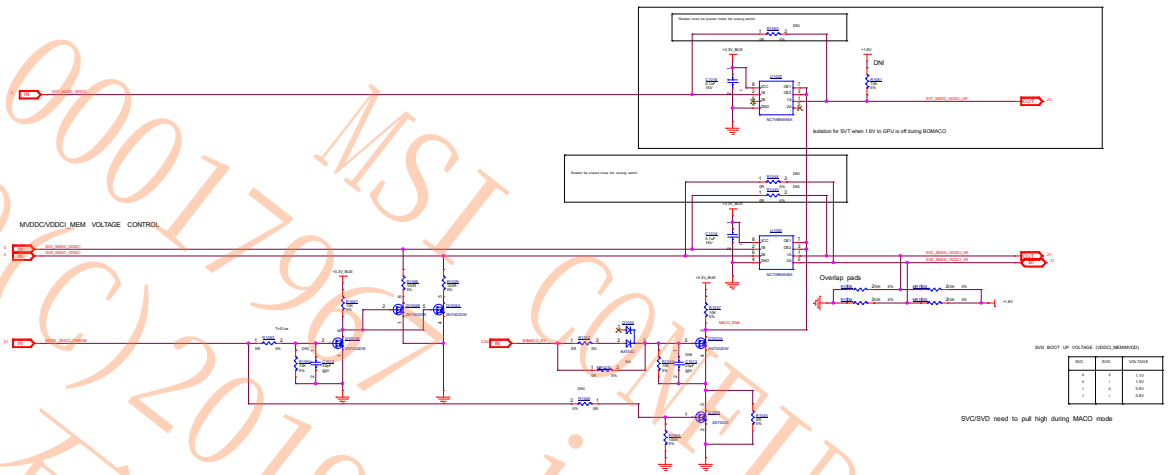

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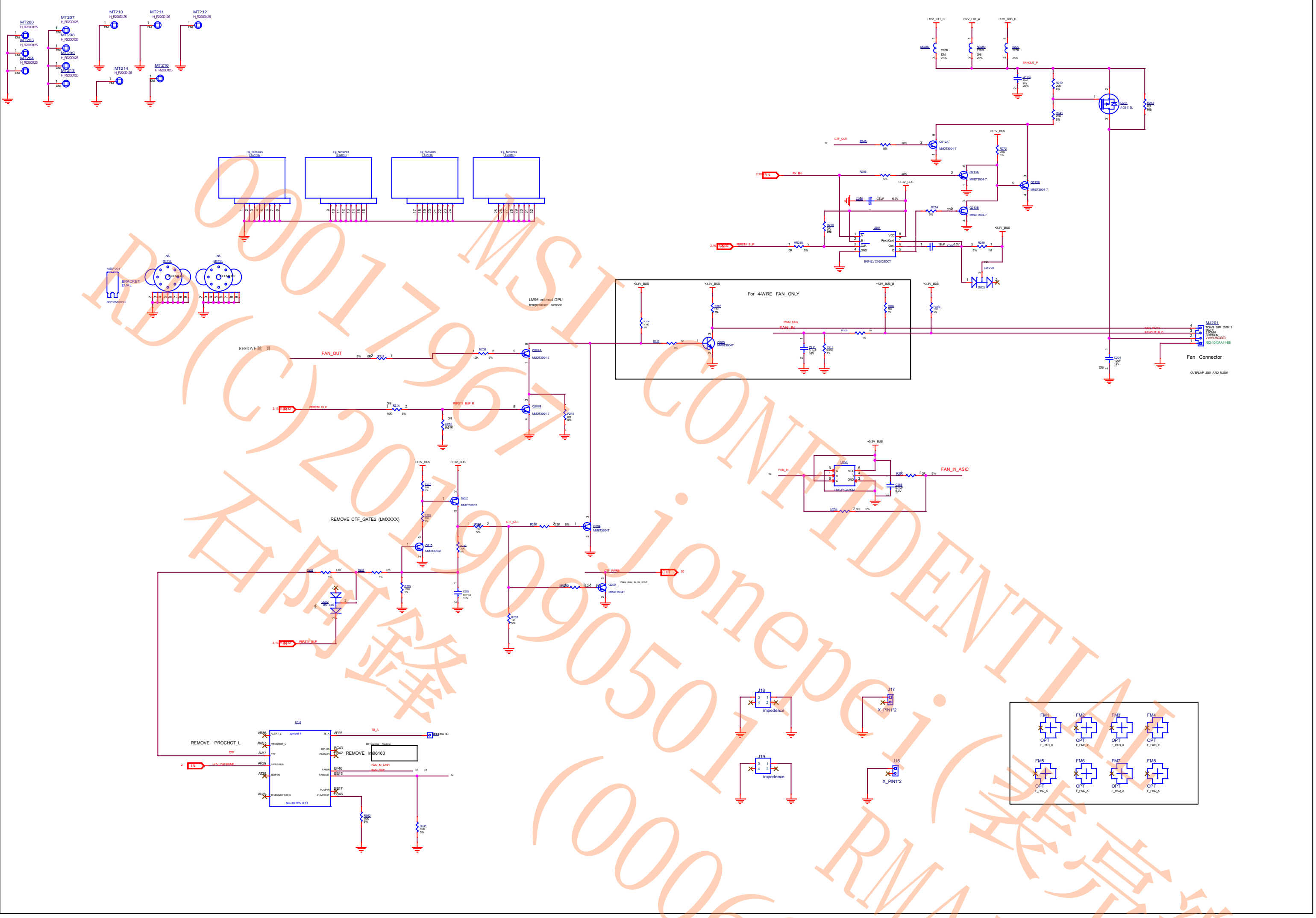
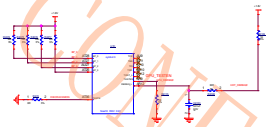
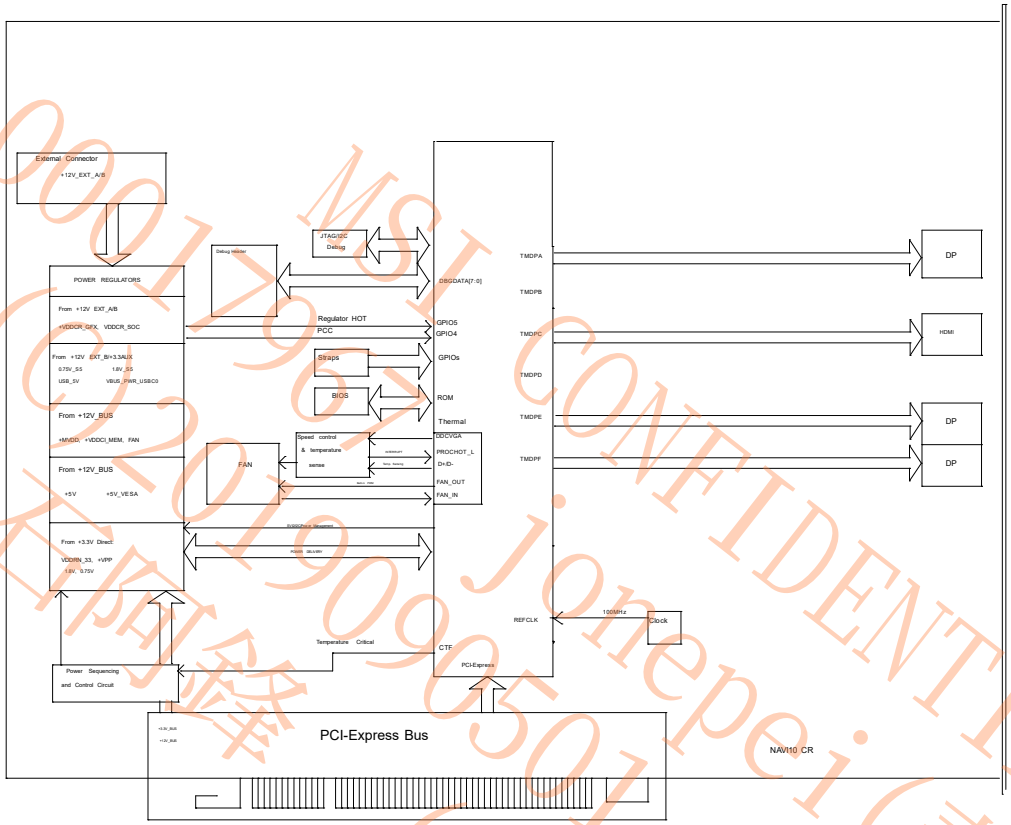
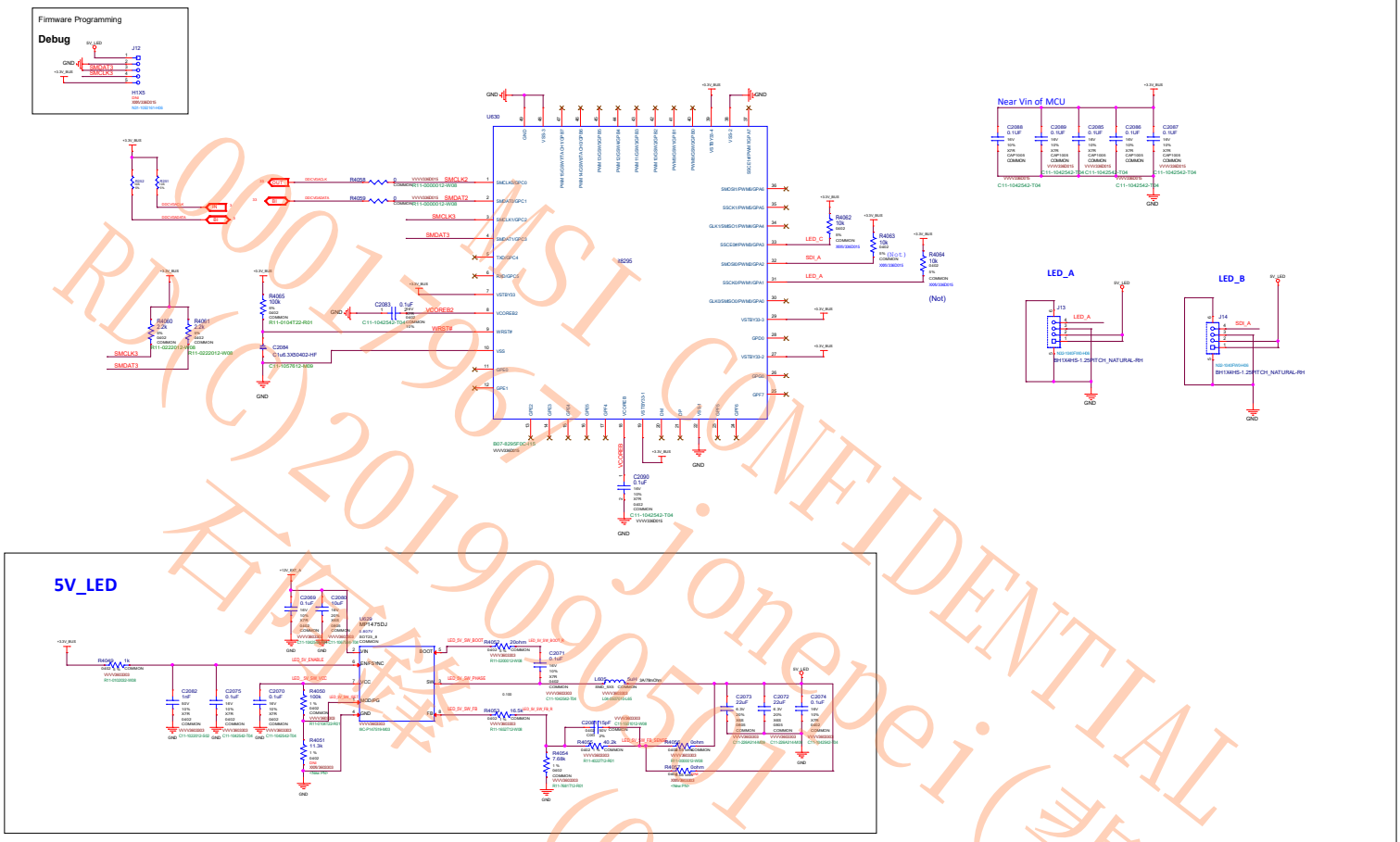




RADEON Lightbar header





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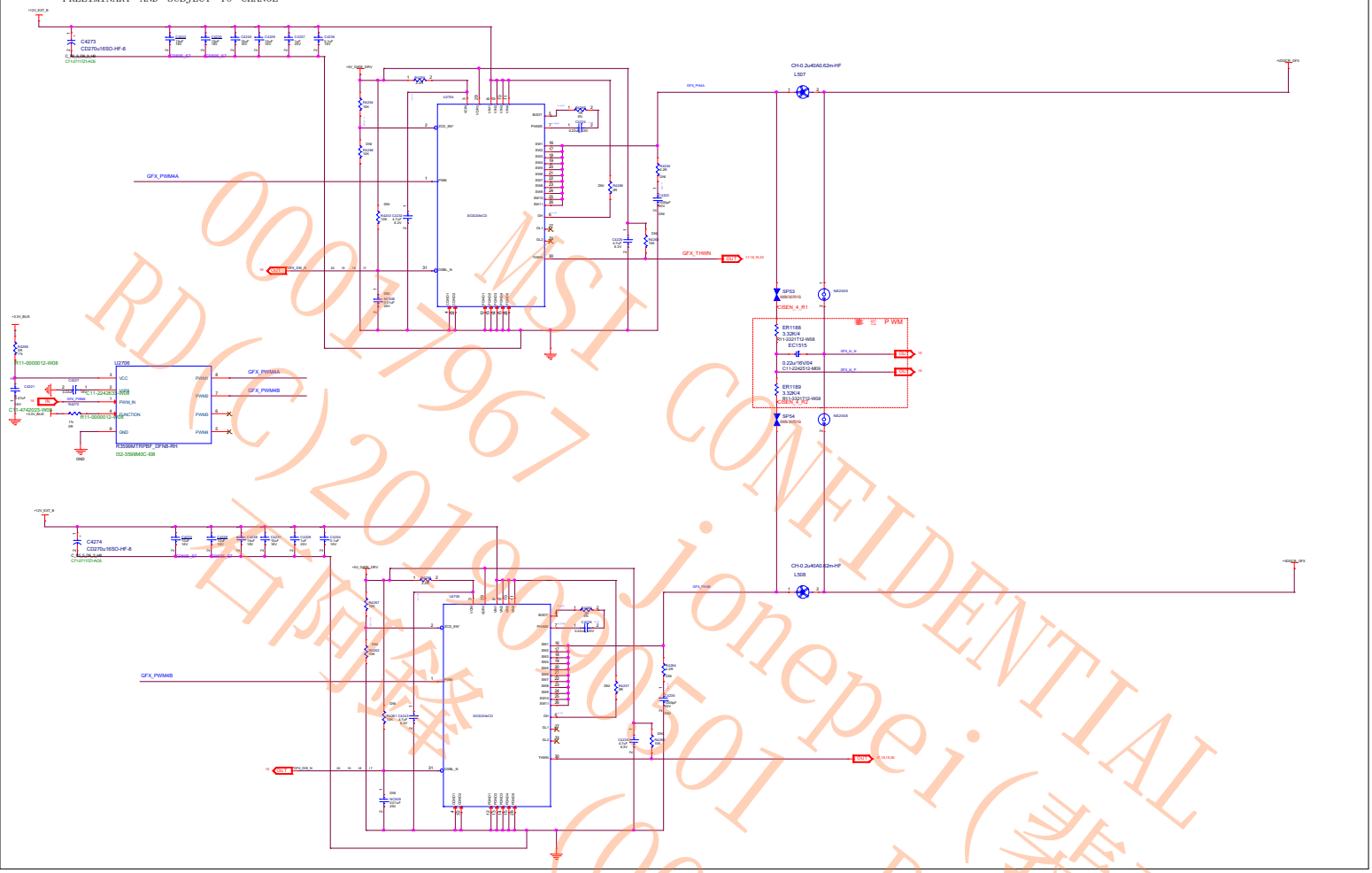

NAVI 10 MEM INTERFACE CH C/D

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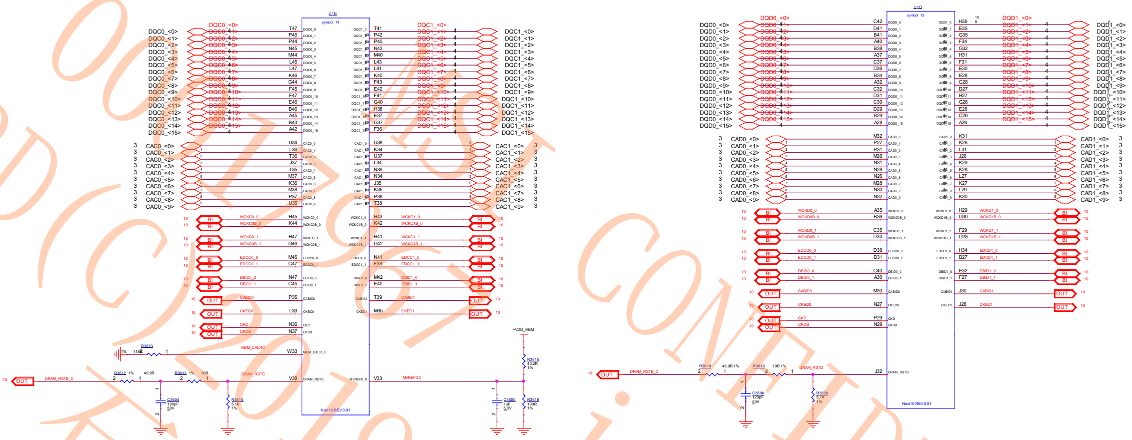

AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

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DATE:	Mon Apr 15 05:57:57 2019	REV:	1.00
SHEET NUMBER:	6	OF	35
DOCUMENT NUMBER:	105_D199xx_00A		
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NAVI 10 MEM INTERFACE CH E/F

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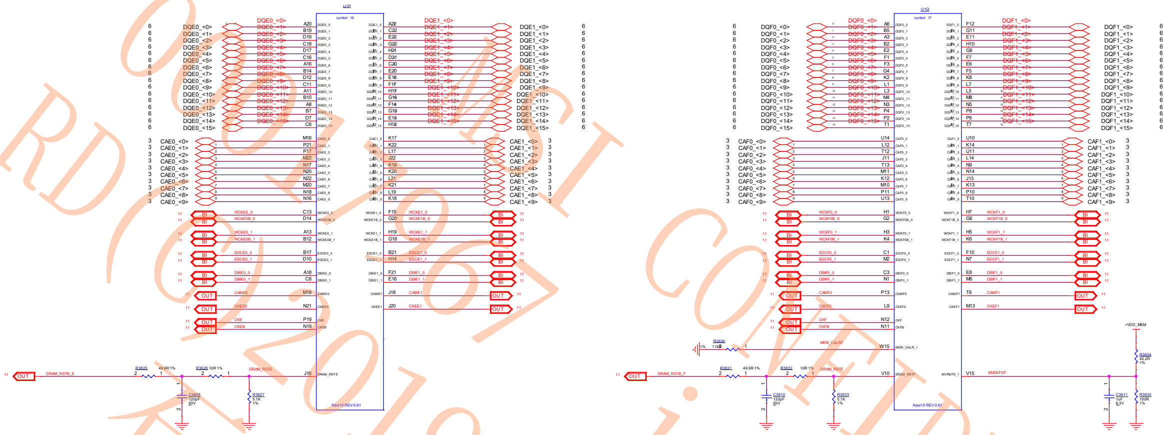

AMD - PLATFORM HARDWARE ENG
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SHEET:	NAVI10 MEM CHEF
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REV:	1.00
SHEET NUMBER:	7 OF 35
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NAVI 10 MEM INTERFACE CH G/H

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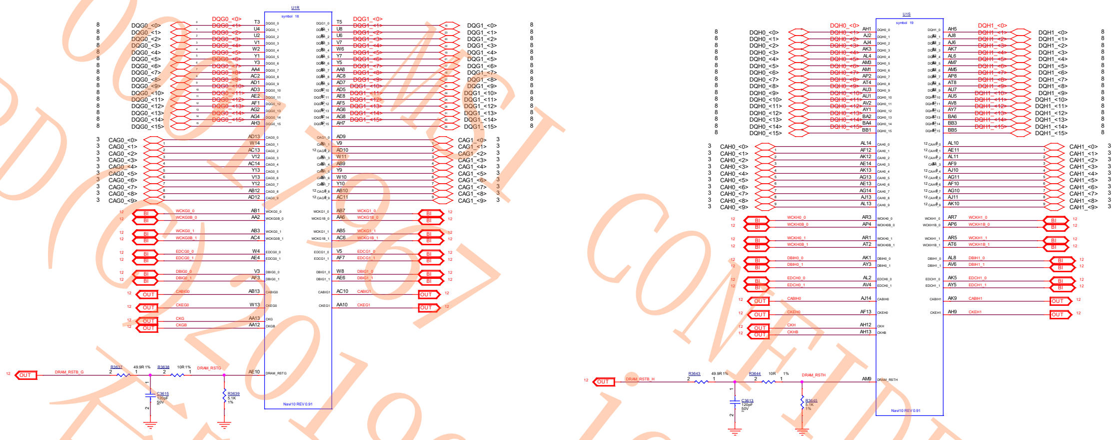

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