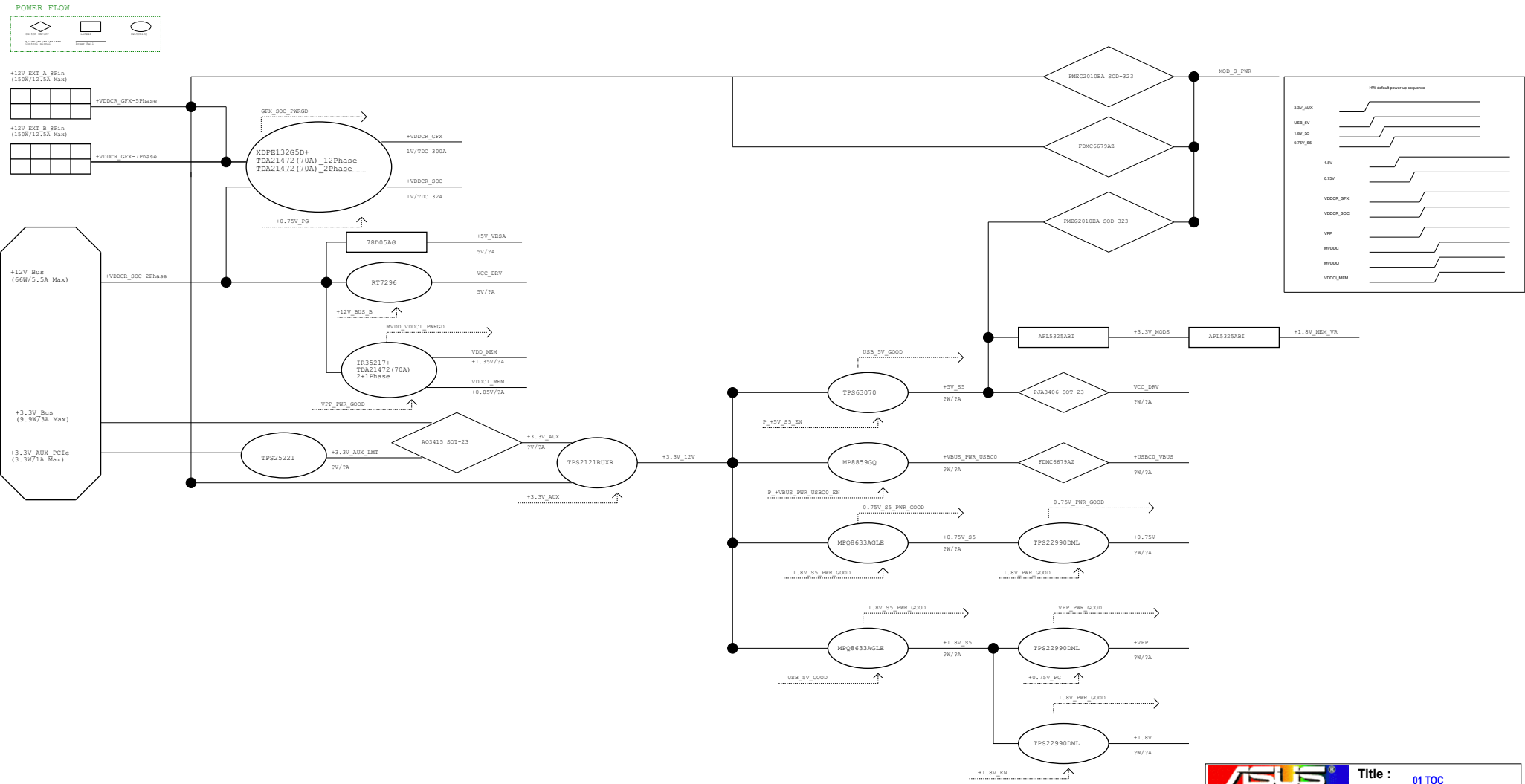

<OrgName>	Title : 01 TOC	
	Engineer: Sam Hom	
Size: Custom	Project Name: D412BS	Rev: 1.00X
Date: Monday, August 24, 2020	Sheet	

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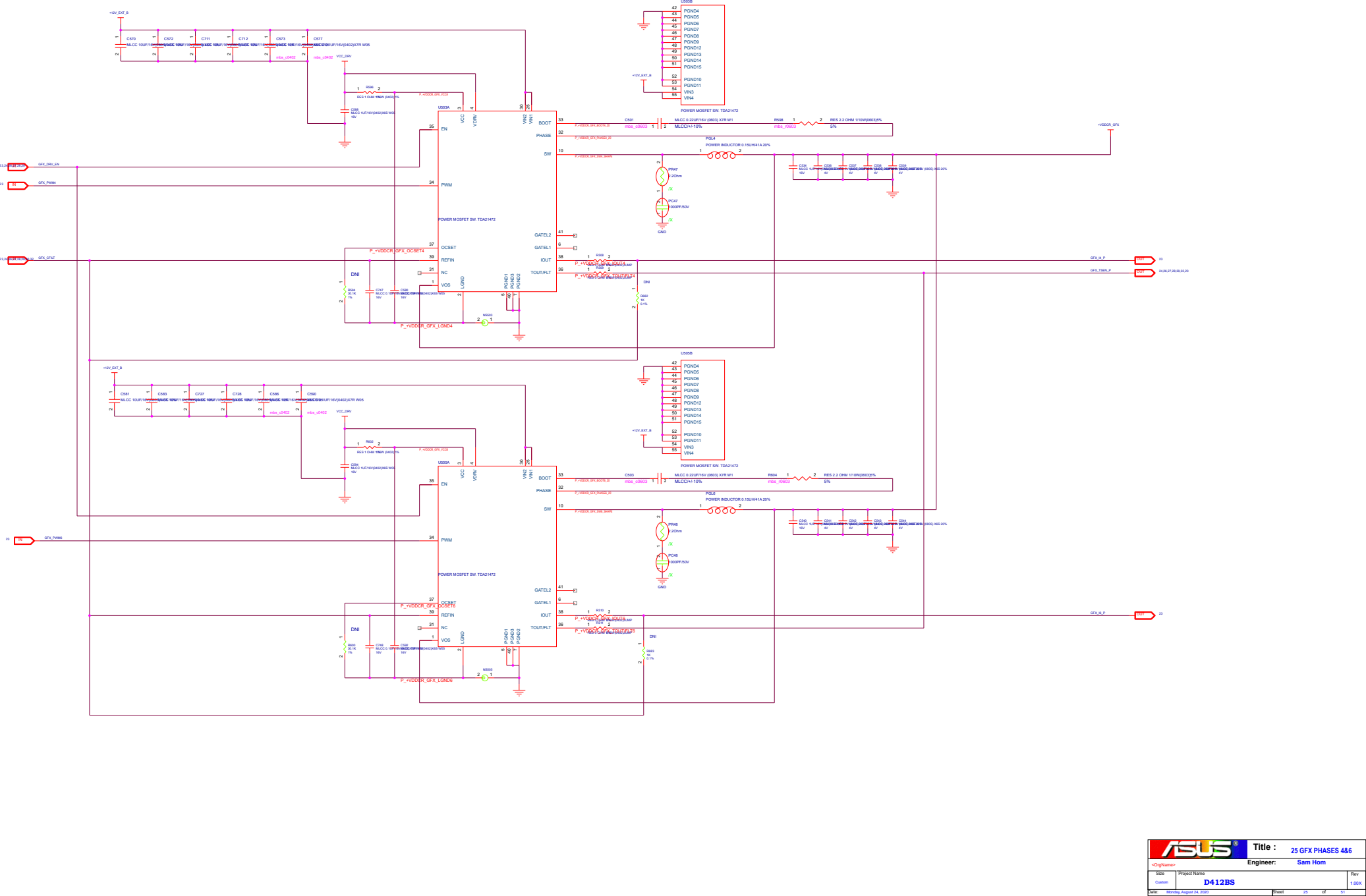
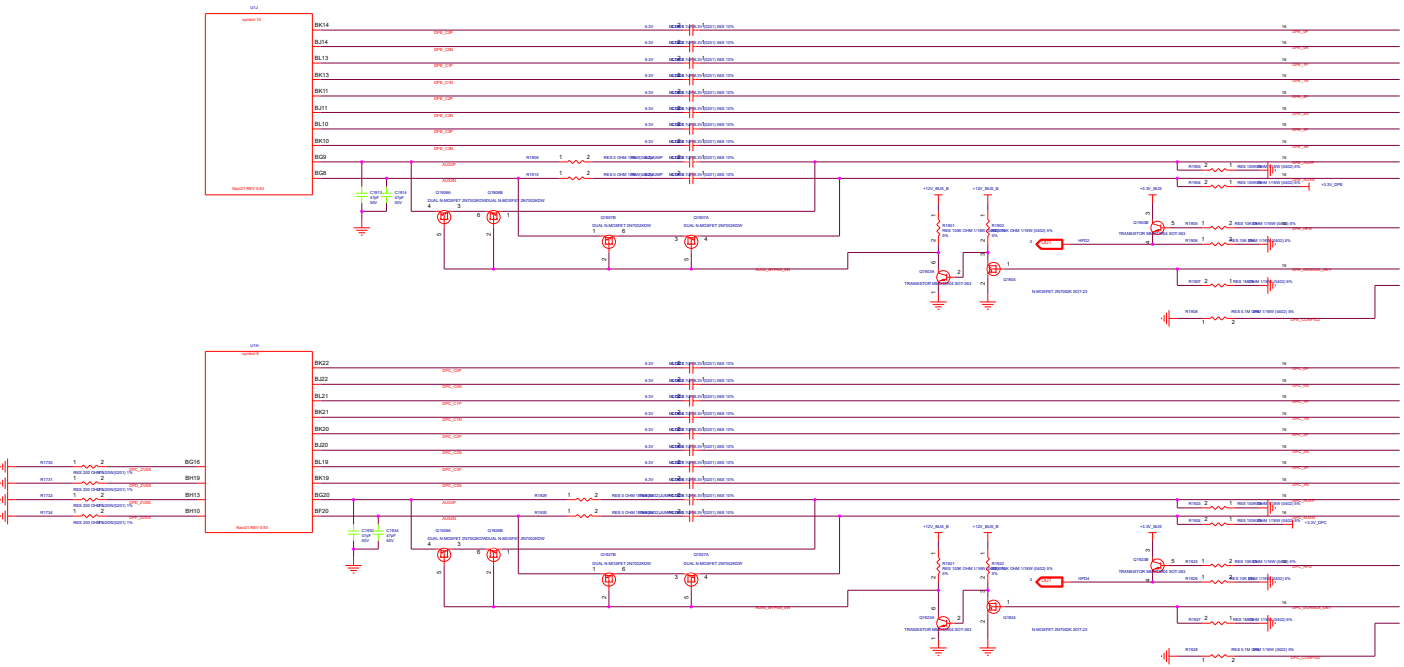
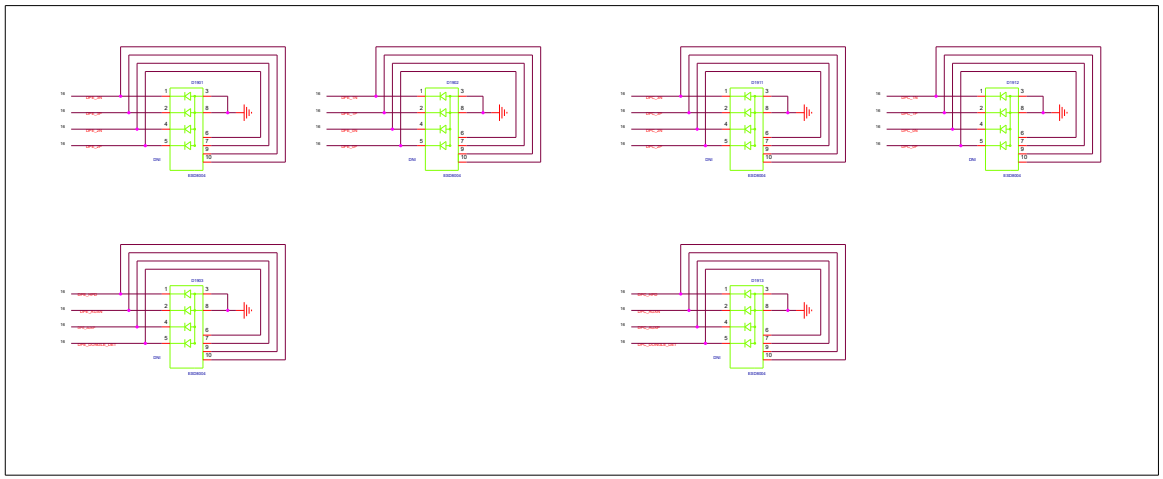
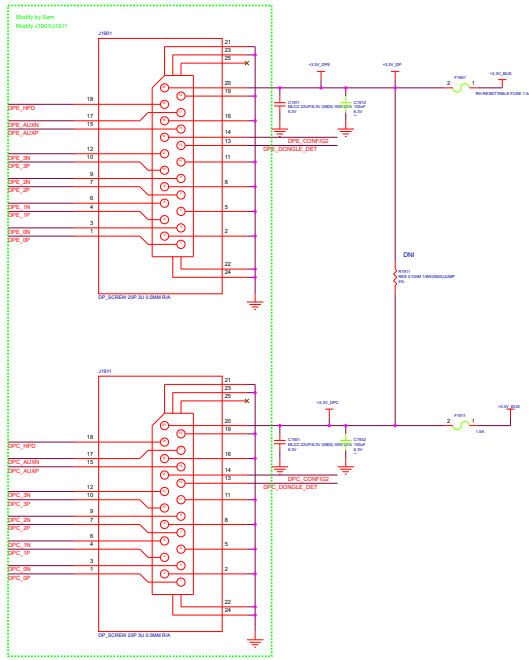
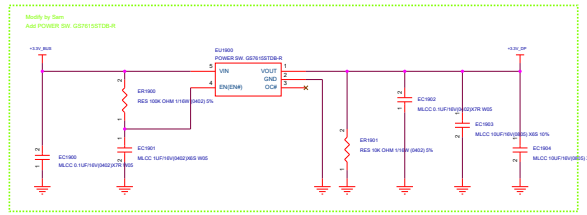


Title :	25 GFX PHASES 4&6		
<OrgName>	Engineer:	Sam Hom	
Size: Custom	Project Name: D412BS		Rev: 1.00X
Date: Monday, August 24, 2020	Sheet 25 of 51		

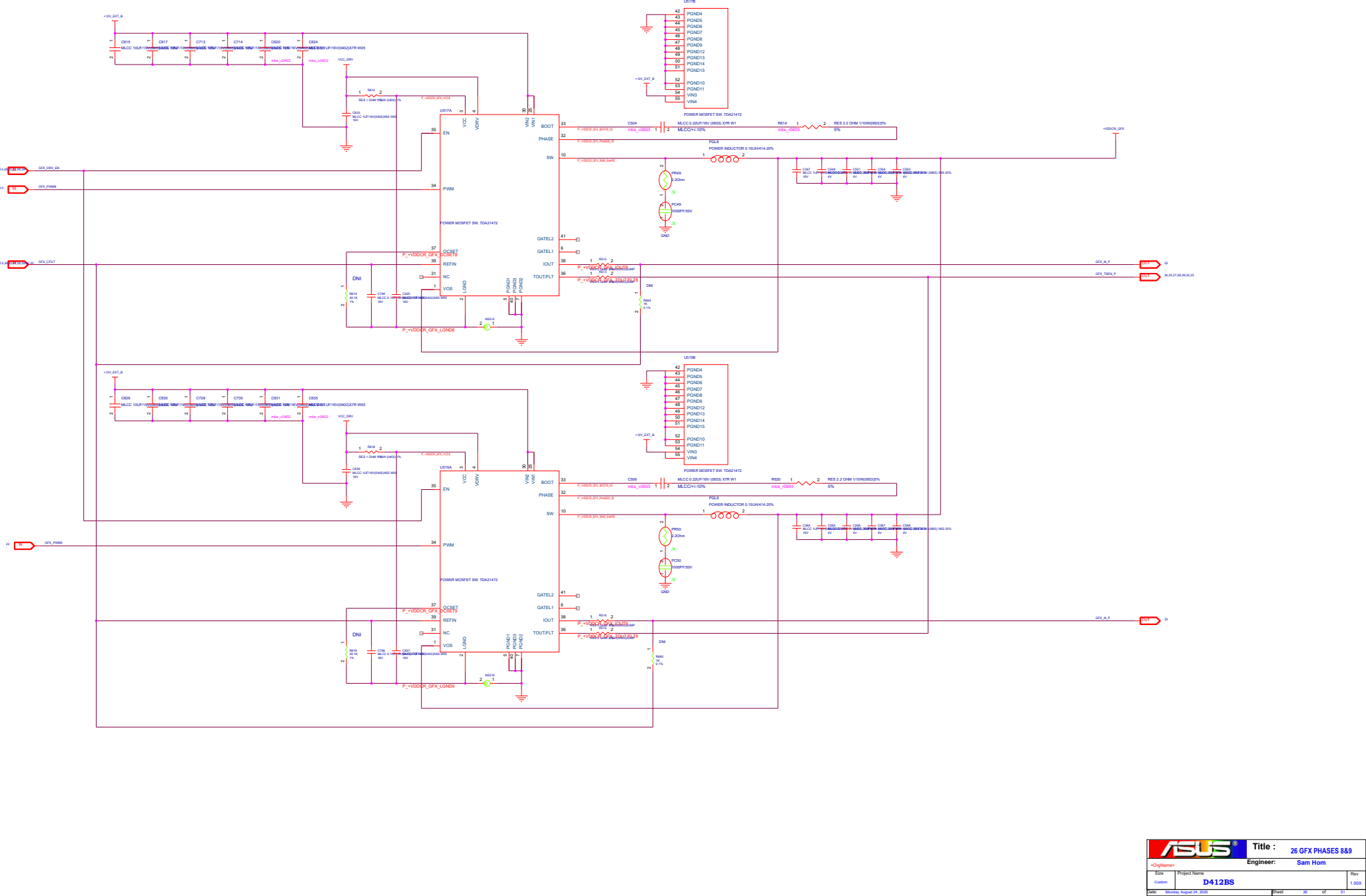




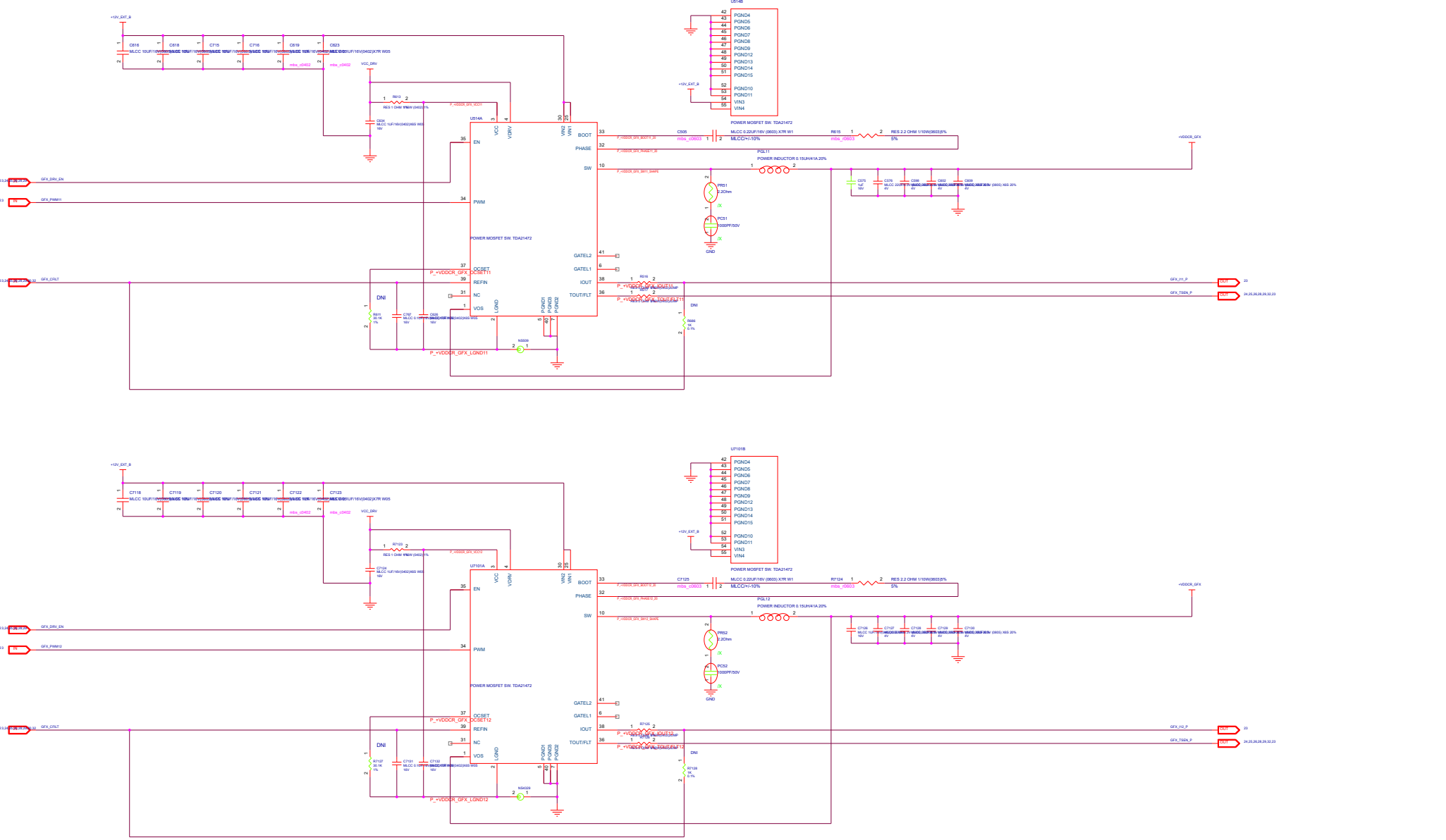




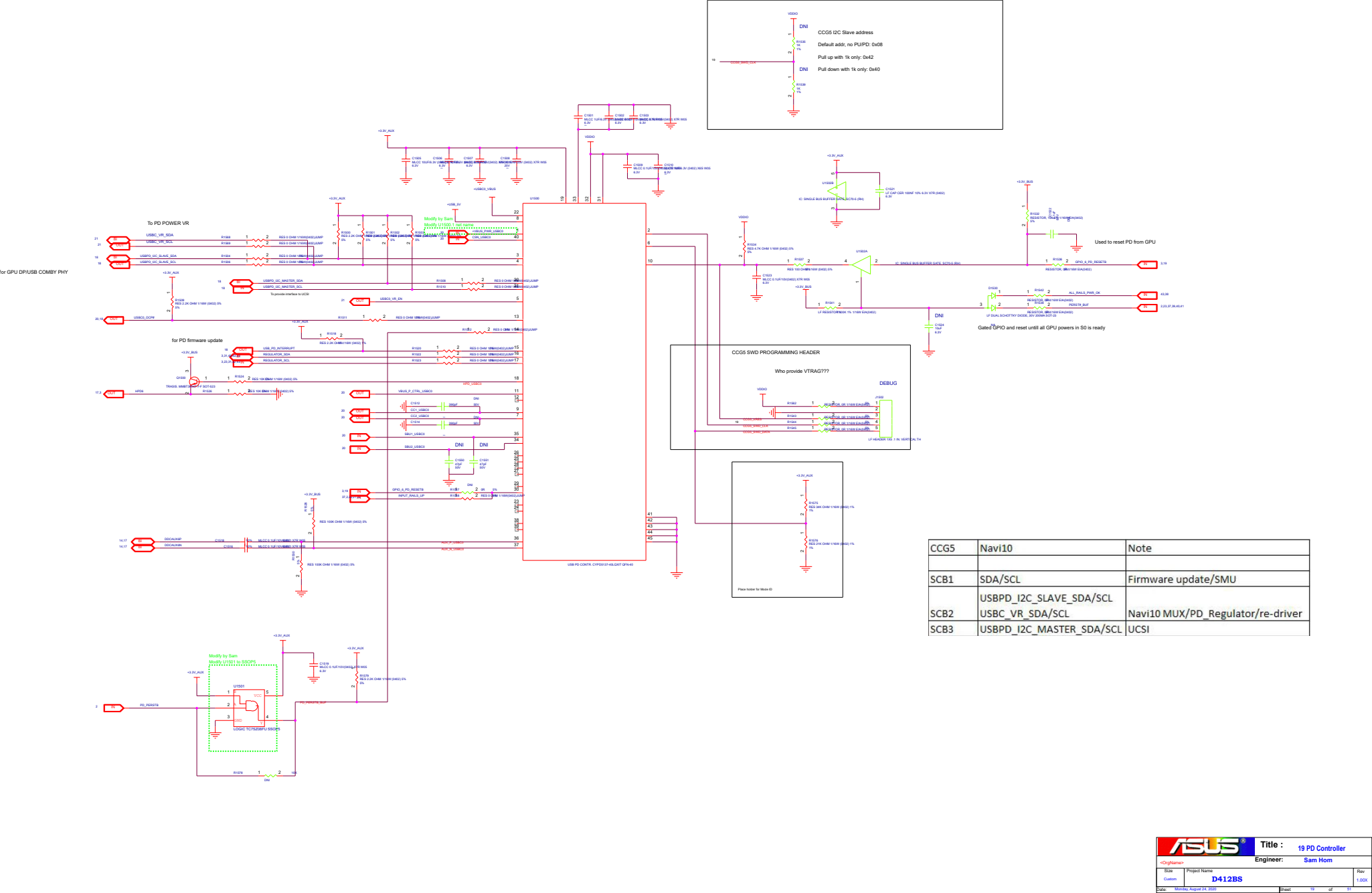
Title :	16 NAVI21 TMDPC&E - DP		
<OrgName>	Engineer:	Sam Hom	
Size: Custom	Project Name: D412BS		Rev: 1.00X
Date: Monday, August 24, 2020	Sheet 16 of 31		



ASUS	Title :	26 GFX PHASES 8&9	
<OrgName>	Engineer:	Sam Hom	
Size: Custom	Project Name: D412BS		Rev: 1.00X
Date: Monday, August 24, 2020	Sheet: 26	of: 51	

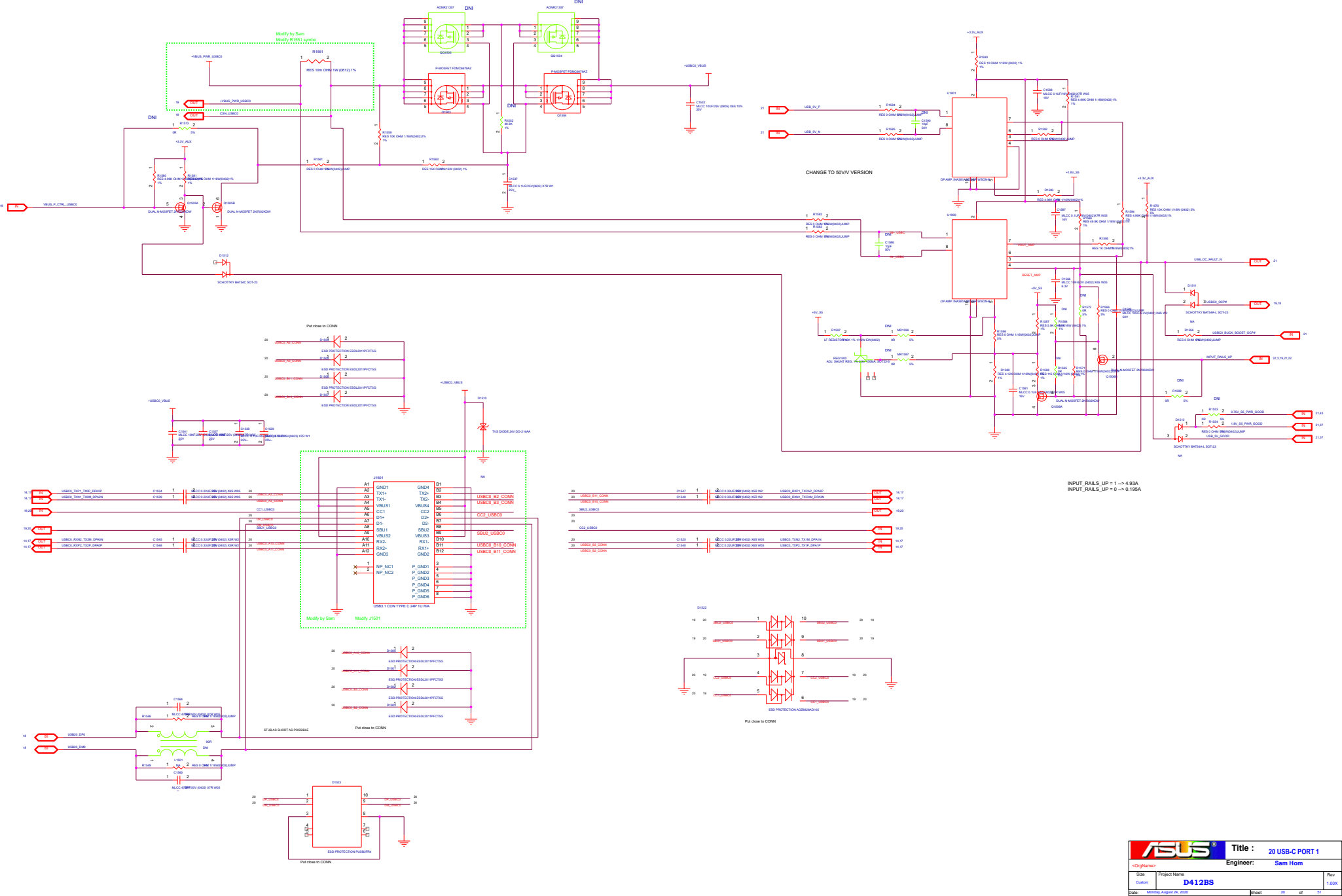


<OrgName>	Title :	27 GFX PHASES 11&12	
	Engineer:	Sam Hom	
Size: Custom	Project Name: D412BS		Rev: 1.00X
Date: Monday, August 24, 2020	Sheet 27 of 51		

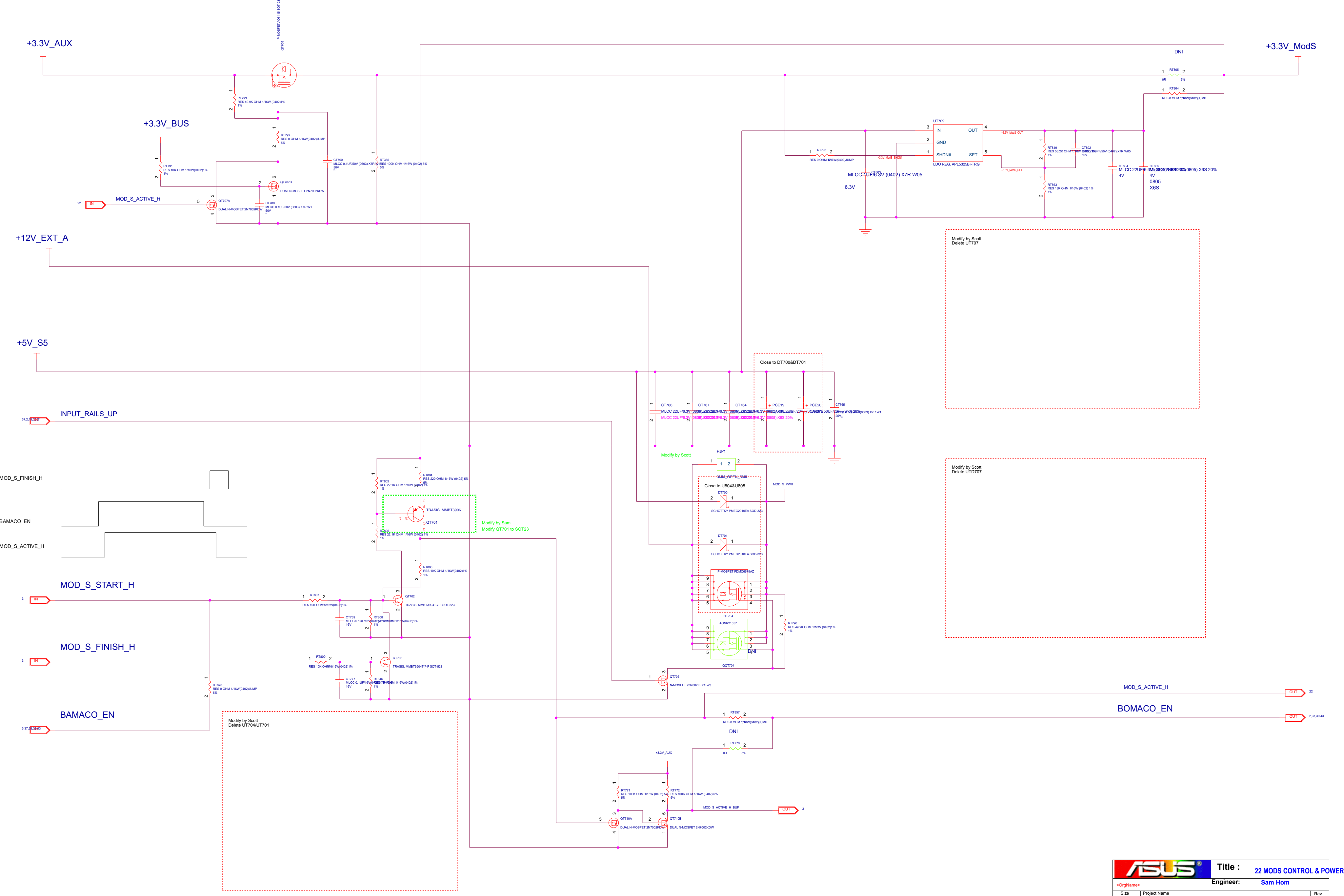


CCG5	Navi10	Note
SCB1	SDA/SCL	Firmware update/SMU
SCB2	USBPD_I2C_SLAVE_SDA/SCL USBC_VR_SDA/SCL	Navi10 MUX/PD_Regulator/re-driver
SCB3	USBPD_I2C_MASTER_SDA/SCL	UCSI

ASUS	Title :	19 PD Controller
<OrgName>	Engineer:	Sam Hom
Size: Custom	Project Name: D412BS	Rev: 1.00X
Date: Monday, August 24, 2020	Sheet: 19 of 51	



ASUS	Title :	20 USB-C PORT 1	
<OrgName>	Engineer:	Sam Hom	
Size: Custom	Project Name: D412BS		Rev: 1.00X
Date: Monday, August 24, 2020	Sheet: 20	of: 51	


+3.3V_AUX
+3.3V_ModS
DNI
+3.3V_BUS
MOD_S_ACTIVE_H
+12V_EXT_A
+5V_S5
UT709
IN
OUT
GND
SHDN#
SET
LDO REG. APL5325BI-TRG
Modify by Scott
Delete UT707
Close to DT700&DT701
INPUT_RAILS_UP
PJP1
Modify by Scott
Close to U804&U805
DT700
SCHOTTKY PMEG2010EA SOD-323
DT701
SCHOTTKY PMEG2010EA SOD-323
MOD_S_FINISH_H
BAMACO_EN
MOD_S_ACTIVE_H
TRASIS. MMBT3906
QT701
Modify by Sam
Modify QT701 to SOT23
MOD_S_START_H
MOD_S_FINISH_H
BAMACO_EN
Modify by Scott
Delete UT704/UT701
Modify by Scott
Delete UTD707
QT705
N-MOSFET 2N7002K SOT-23
MOD_S_ACTIVE_H
BOMACO_EN
DNI
+3.3V_AUX
MOD_S_ACTIVE_H_BUF
QT710A
DUAL N-MOSFET 2N7002KDW
QT710B
DUAL N-MOSFET 2N7002KDW

Title : 22 MODS CONTROL & POWER

<OrgName>

Engineer: Sam Hom

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Custom	D412BS	1.00X

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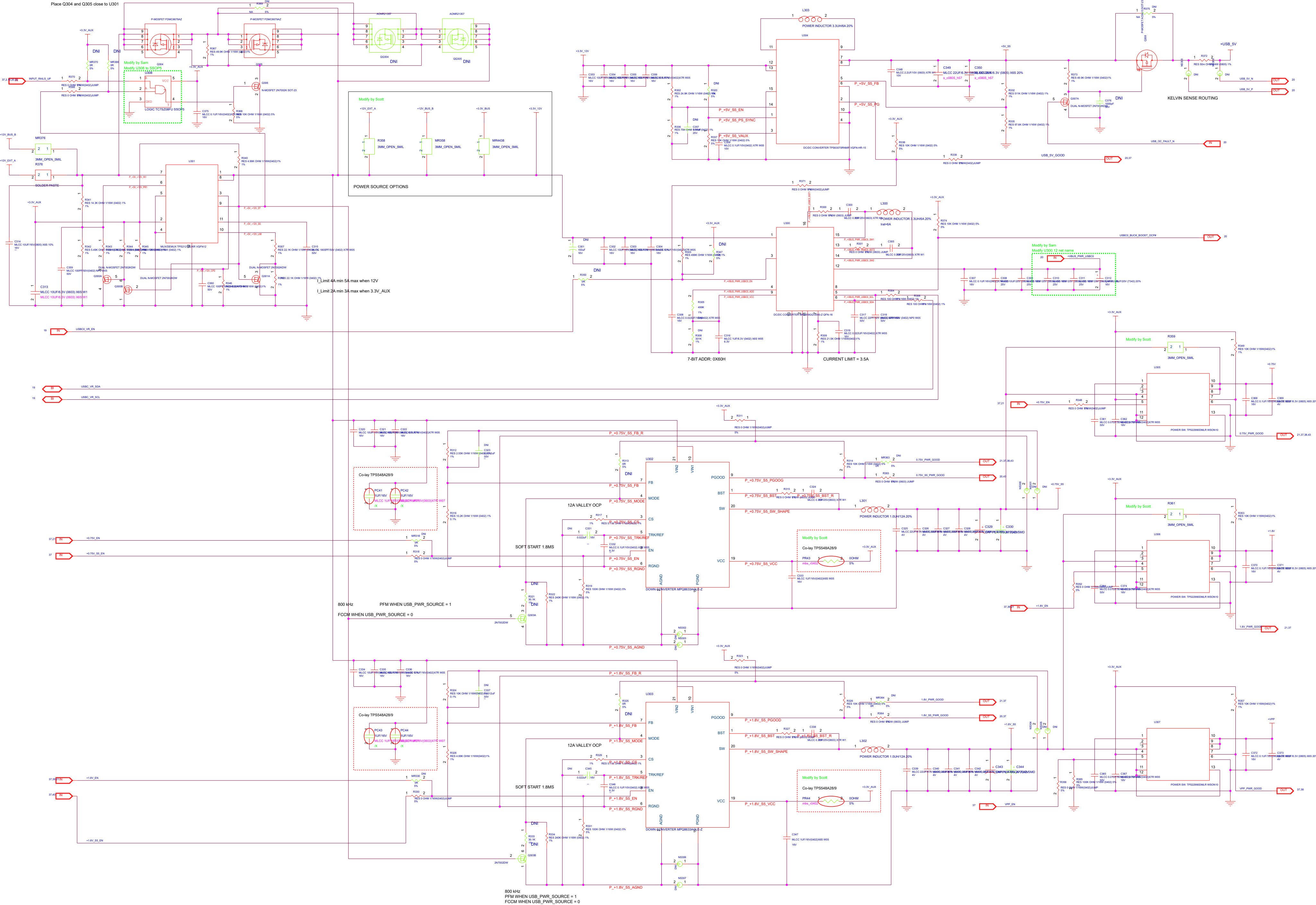
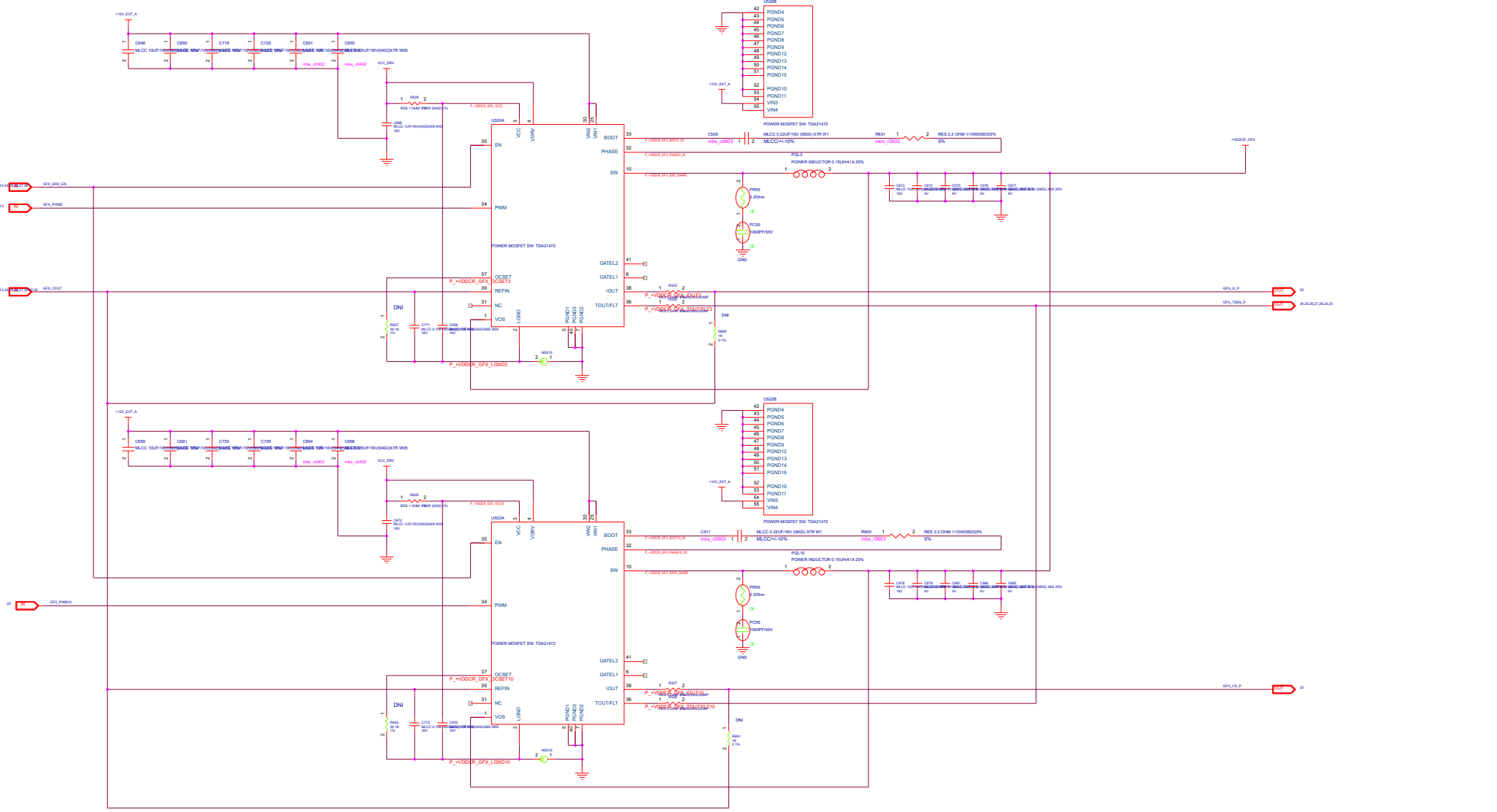

Place Q304 and Q305 close to U301
P-MOSFET FDMC8679AZ
AONR21357
DNI
Modify by Sam
Modify U308 to SSOP5
LOGIC TC7SZ08FU SSOP5
N-MOSFET 2N7002K SOT-23
Modify by Scott
POWER SOURCE OPTIONS
3MM_OPEN_5MIL
SOLDER PASTE
MUX/DEMUX TPS2121RUXR VQFN12
DUAL N-MOSFET 2N7002KDW
I_Limit 4A min 5A max when 12V
I_Limit 2A min 3A max when 3.3V_AUX
POWER INDUCTOR 3.3UH/6A 20%
DC/DC CONVERTER TPS63070RNMR VQFN-HR-15
KELVIN SENSE ROUTING
USB_5V_GOOD
USB_OC_FAULT_N
Modify by Sam
Modify U300.12 net name
7-BIT ADDR: 0X60H
CURRENT LIMIT = 3.5A
USBC0_VR_EN
USBC_VR_SDA
USBC_VR_SCL
Co-lay TPS548A28/9
12A VALLEY OCP
SOFT START 1.8MS
DOWN CONVERTER MPQ8633AGLE-Z
800 kHz
PFM WHEN USB_PWR_SOURCE = 1
FCCM WHEN USB_PWR_SOURCE = 0
POWER INDUCTOR 1.0UH/12A 20%
POWER SW. TPS22990DMLR WSON10
0.75V_PWR_GOOD
1.8V_PWR_GOOD
VPP_PWR_GOOD



Title :	29 GFX PHASES 3&10		
<OrgName>	Engineer:	Sam Hom	
Size: Custom	Project Name: D412BS		Rev: 1.00X
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Navi21 XGMI LINK 0 & 1

Title :	05 XGMI		
Engineer:	Sam Hom		
<OrgName>			
Size: Custom	Project Name: D412BS		Rev: 1.00X
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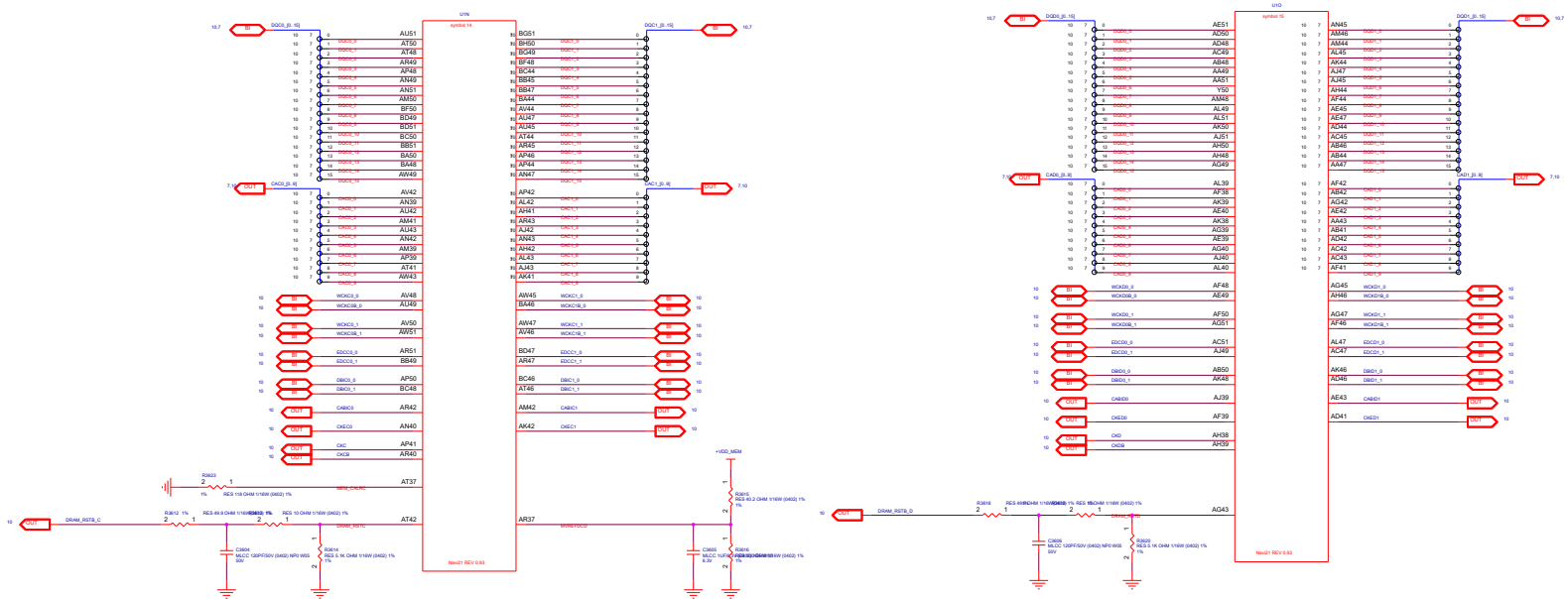
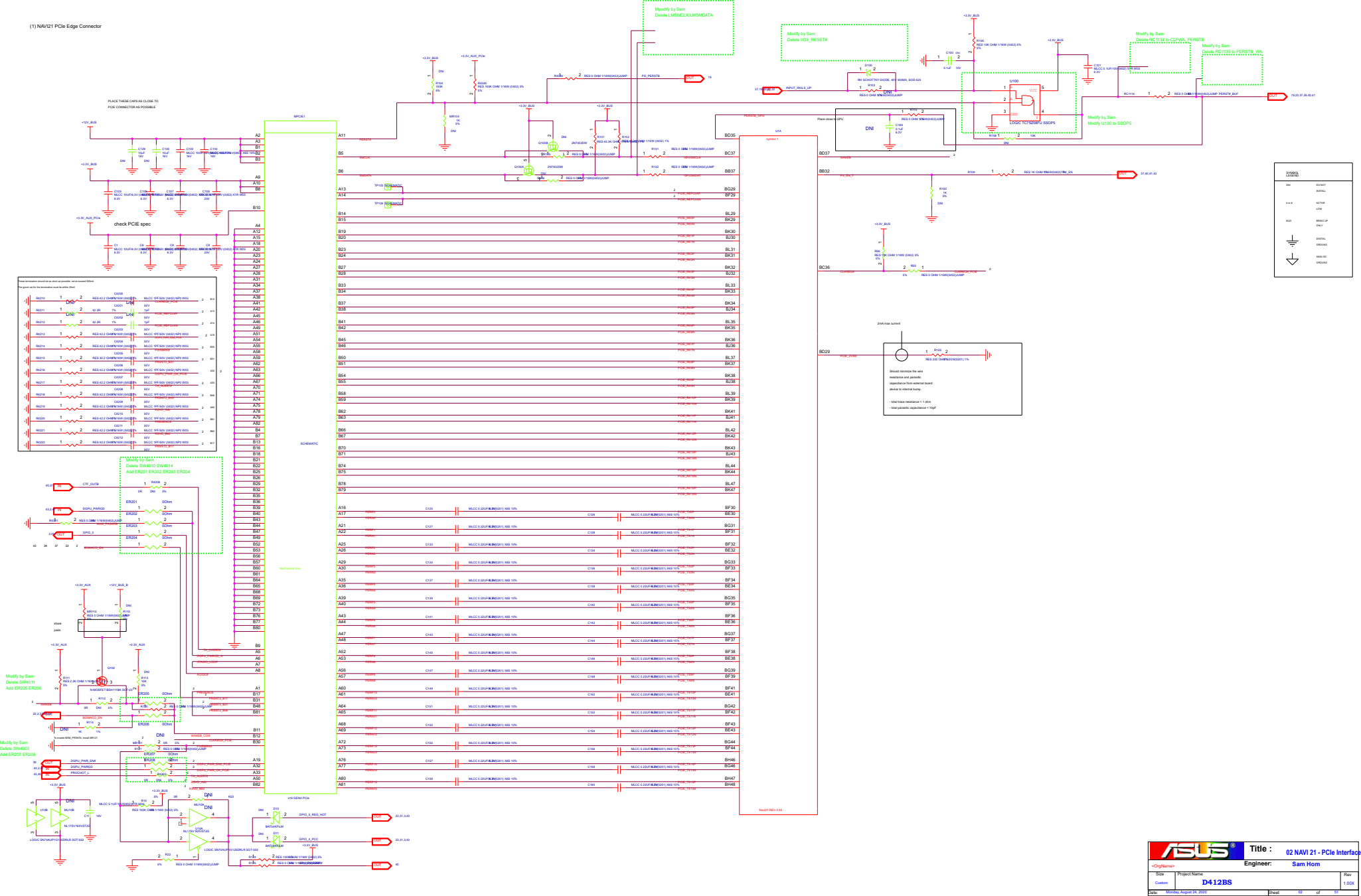


Title :	07 NAVI 21 MEM CH CD		
<OrgName>	Engineer:	Sam Hom	
Size: Custom	Project Name: D412BS		Rev: 1.00X
Date: Monday, August 24, 2020	Sheet: 07 of 51		


(1) NAVI21 PCIe Edge Connector
Modify by Sam
Delete LMSMCLK/LMSMDATA
Modify by Sam
Delete I/O3_RESET#
Modify by Sam
Delete RC1134 to CLPWA_PERSTB
Modify by Sam
Delete RC1135 to PERSTB_WA
PLACE THESE CAPS AS CLOSE TO PCIE CONNECTOR AS POSSIBLE
check PCIE spec
MPCIE1
SCHEMATIC
Mechanical Key
x16 GEN4 PCIe
Place close to GPU
LOGIC TC7SZ08FU SSOP5
Modify by Sam
Modify U100 to SSOP5
Modify by Sam
Delete SW4010 SW4014
Add ER201 ER202 ER203 ER204
Modify by Sam
Delete SW4011
Add ER205 ER206
Modify by Sam
Delete SW4003
Add ER207 ER208
2mA max current
Should minimize the wire resistance and parasitic capacitance from external board device to internal bump.
- total trace resistance < 1 ohm
- total parasitic capacitance < 10pF
SYMBOL LEGEND
DO NOT INSTALL
ACTIVE LOW
BRING UP ONLY
DIGITAL GROUND
ANALOG GROUND
Title : 02 NAVI 21 - PCIe Interface
Engineer: Sam Hom
Project Name: D412BS
Rev: 1.00X
Date: Monday, August 24, 2020
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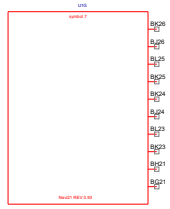
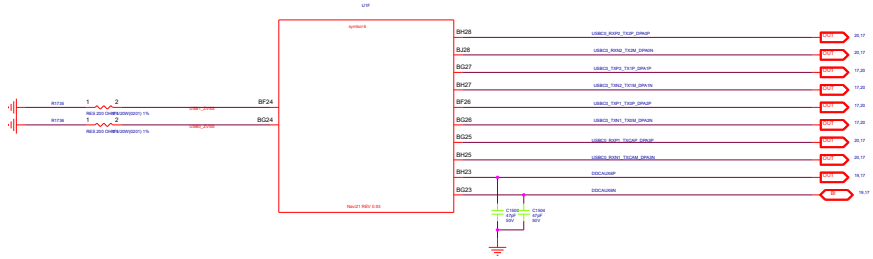
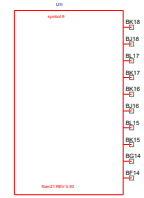
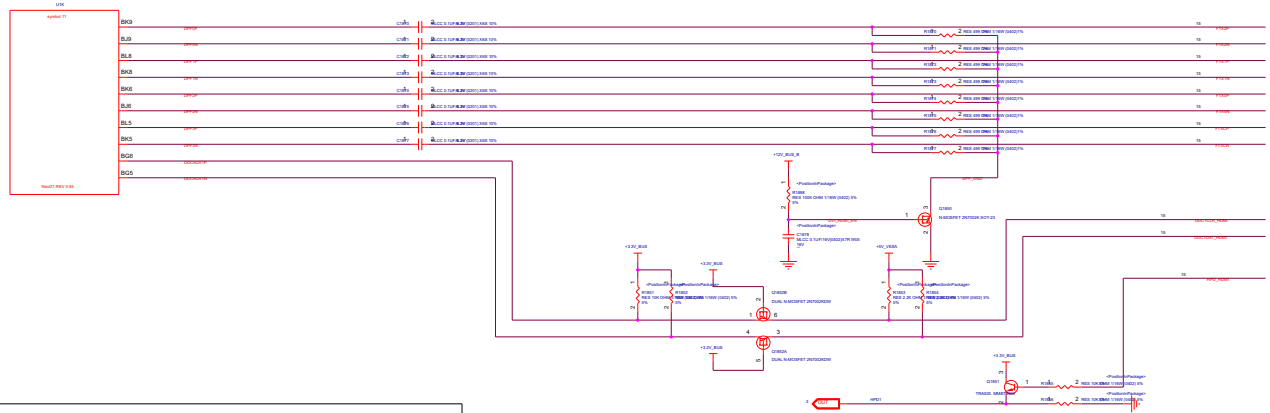
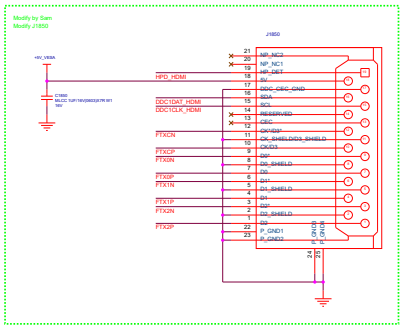


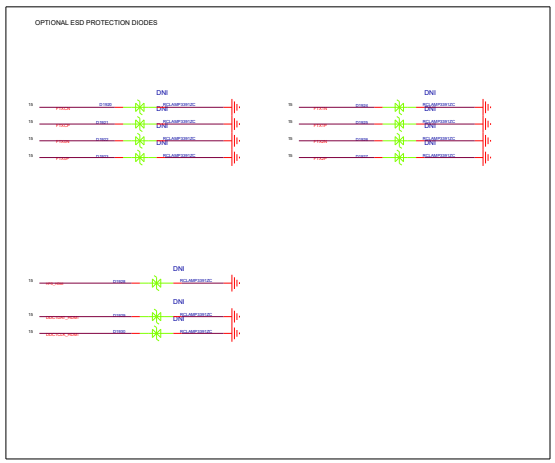


Title :	14 NAVI21 TMDPA - USB-C		
<OrgName>	Engineer:	Sam Hom	
Size: Custom	Project Name: D412BS		Rev: 1.00X
Date: Monday, August 24, 2020	Sheet 14 of 31		









Title :	15 NAVI21 TMDPF - HDMI		
<OrgName>	Engineer:	Sam Hom	
Size: Custom	Project Name: D412BS		Rev: 1.00X
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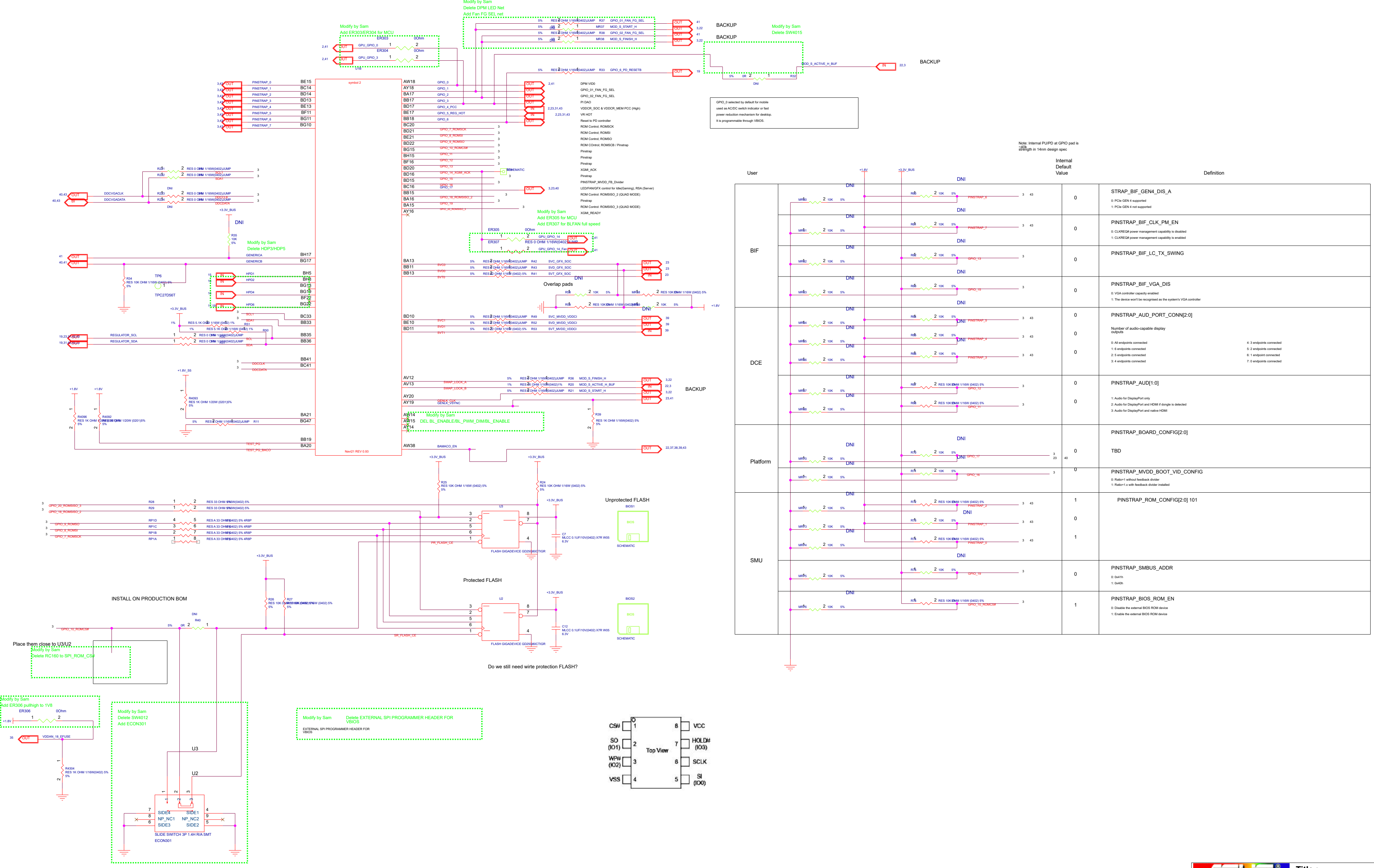

Title :	03 NAVI 21 - GPIOs
<OrgName> Engineer:	Sam Hom
Size: Custom	Project Name: D412BS	Rev: 1.00X
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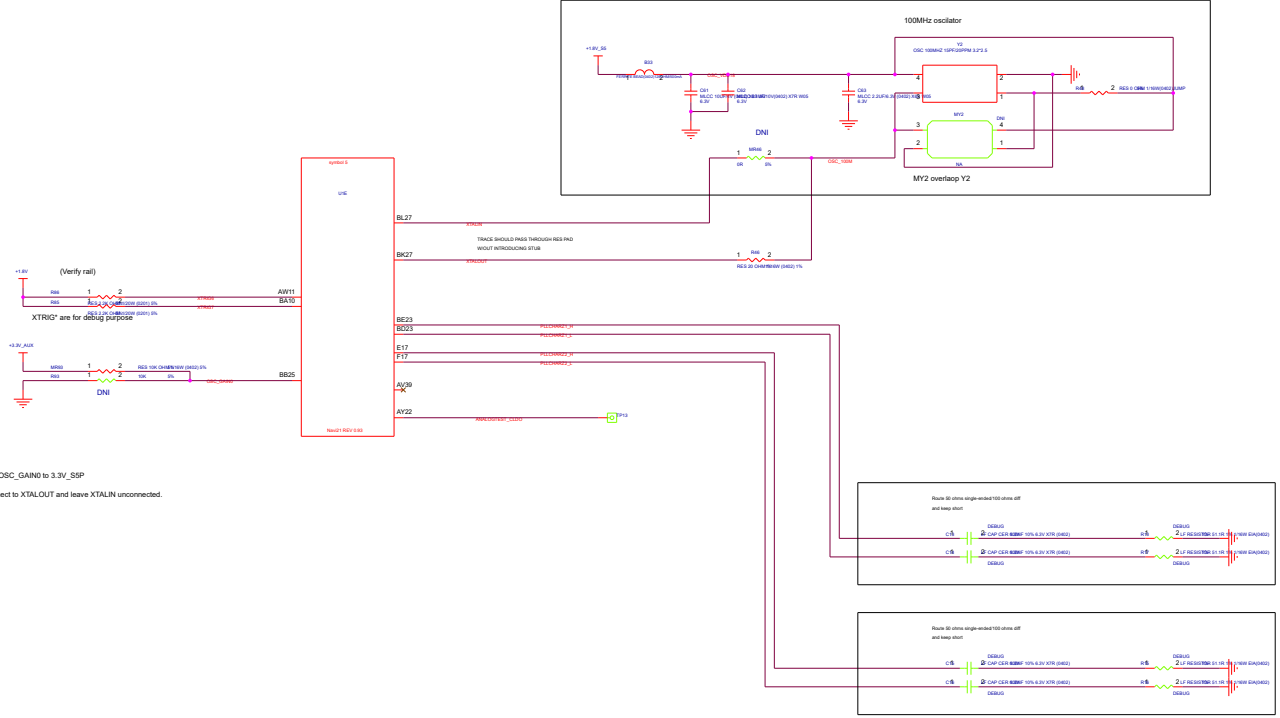

Default OSC_GAIN is 0x7. Pull-up OSC_GAIN0 to 3.3V_S5P

When 0x7, external clock chip connect to XTALOUT and leave XTALIN unconnected.

<OrgName>	Title :	04 NAVI 21 XTAL	
	Engineer:	Sam Hom	
Size: Custom	Project Name: D412BS		Rev: 1.00X
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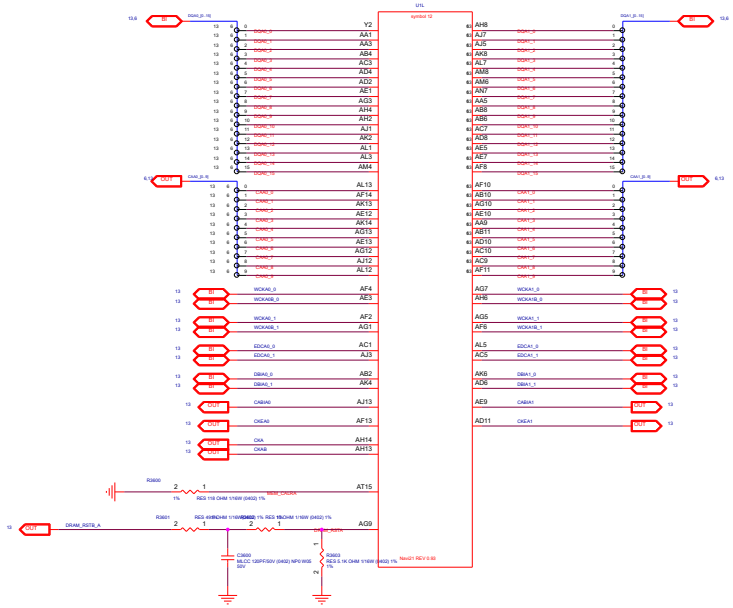
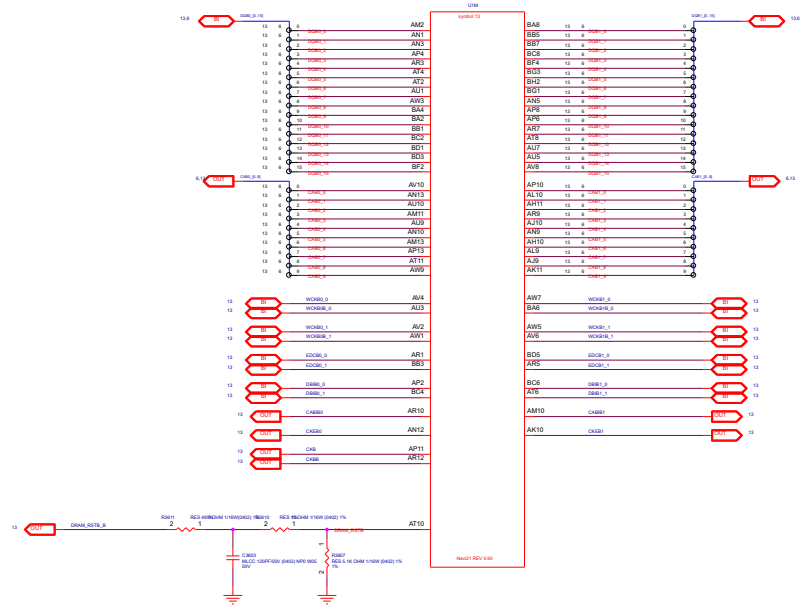
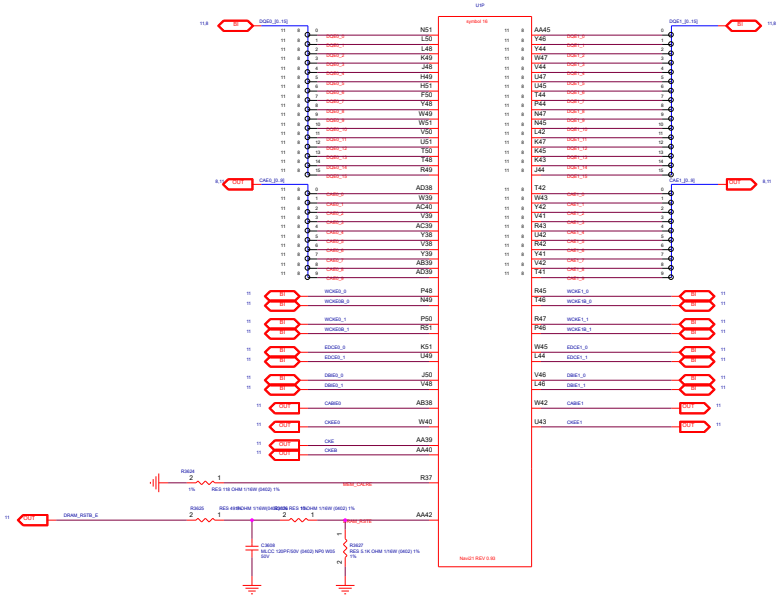
(1) NAVI 10 MEM INTERFACE CH A/B

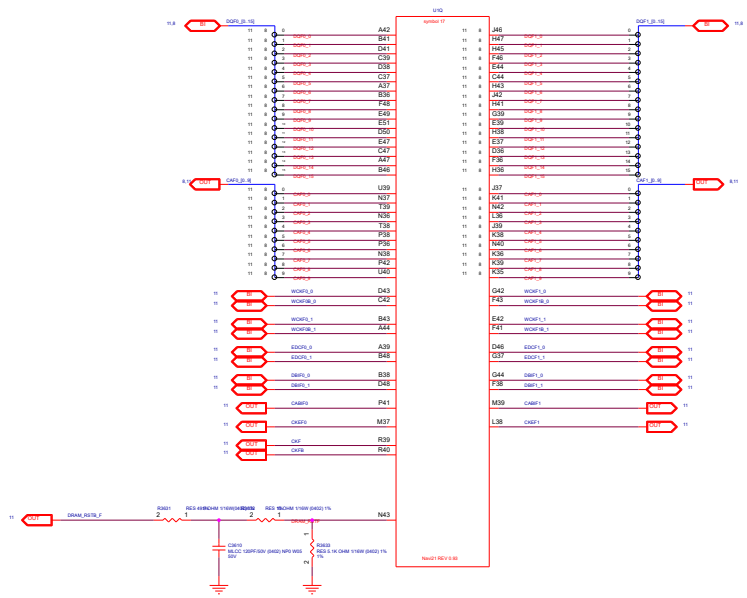




ASUS	Title :	06 NAVI 21 MEM CH AB	
<OrgName>	Engineer:	Sam Hom	
Size: Custom	Project Name: D412BS		Rev: 1.00X
Date: Monday, August 24, 2020	Sheet: 06	of: 51	

(3) NAVI 10 MEM INTERFACE CH E/F





<OrgName>		Title :	08 NAVI 21 MEM CH EF
		Engineer:	Sam Hom
Size: Custom	Project Name: D412BS		Rev: 1.00X
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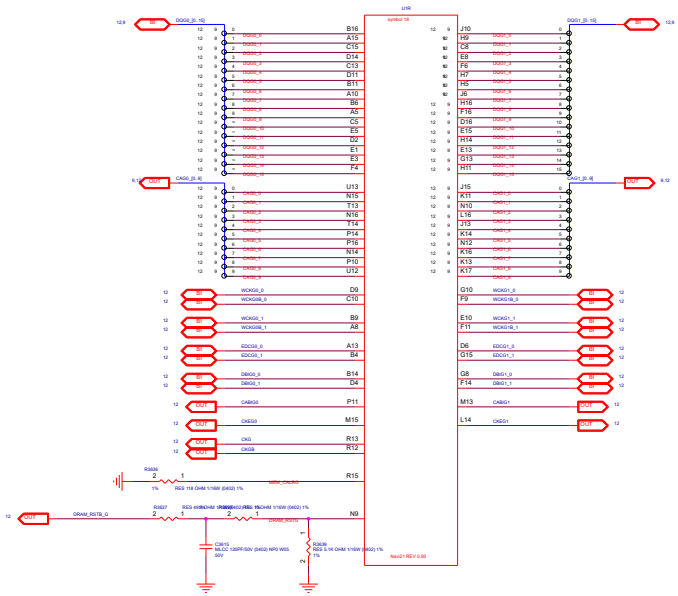

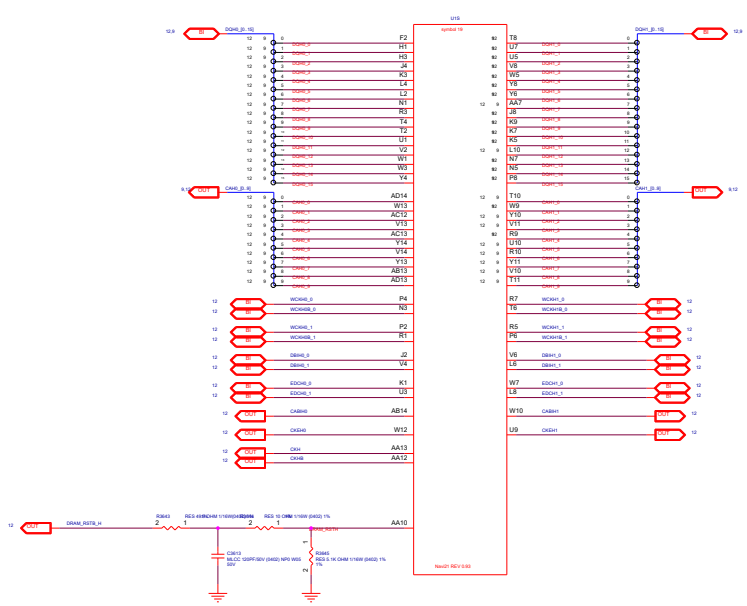

Title :	09 NAVI 21 MEM CH GH		
<OrgName>	Engineer:	Sam Hom	
Size: Custom	Project Name: D412BS		Rev: 1.00X
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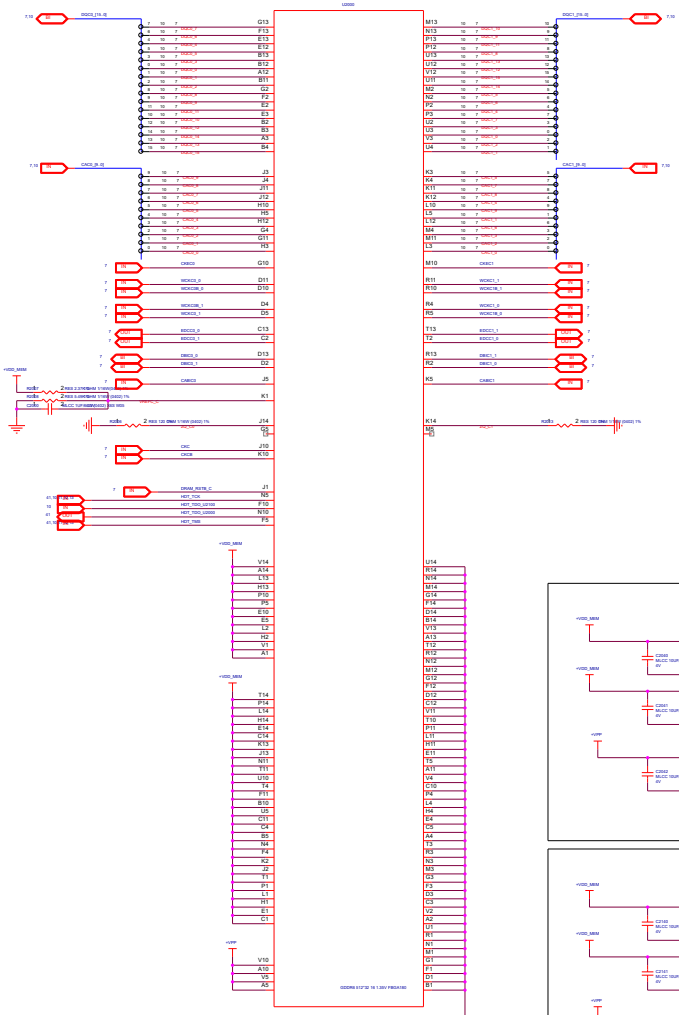
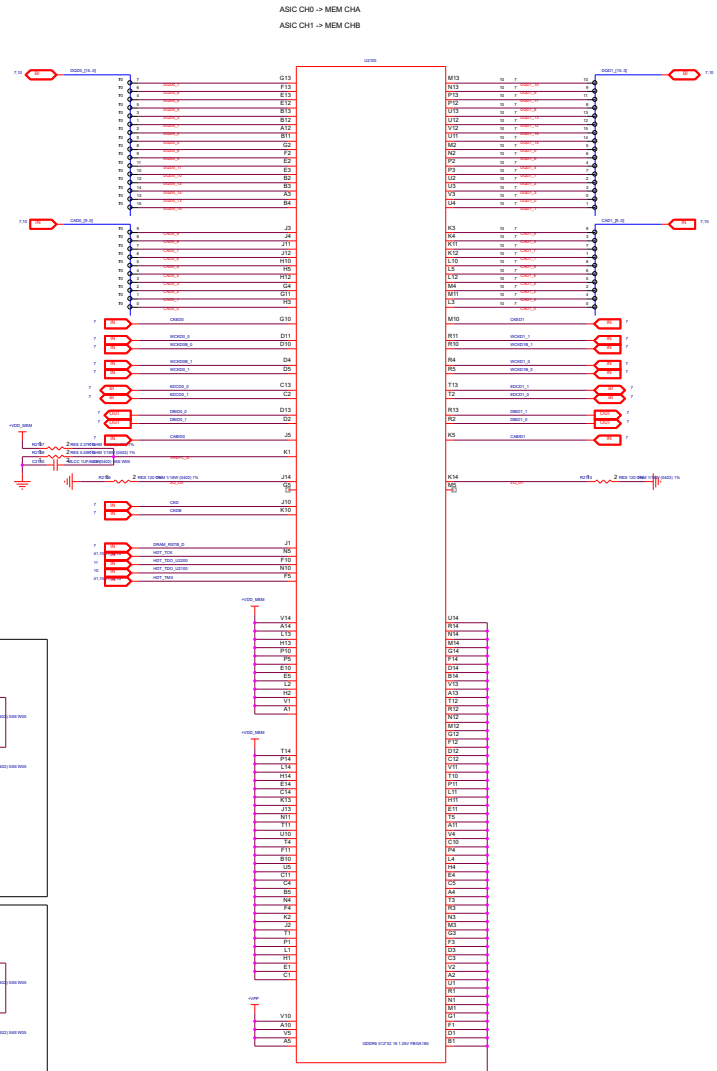
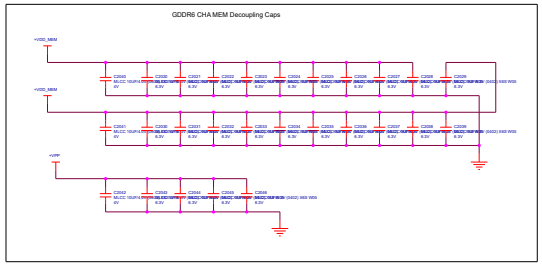
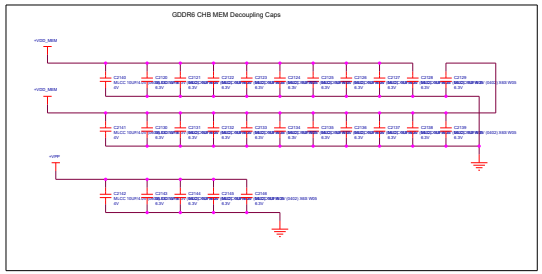
ASIC CH0 -> MEM CHA

ASIC CH1 -> MEM CHB









ASUS	Title :	10 GDDR6 MEM CH CD	
<OrgName>	Engineer:	Sam Hom	
Size: Custom	Project Name: D412BS		Rev: 1.00X
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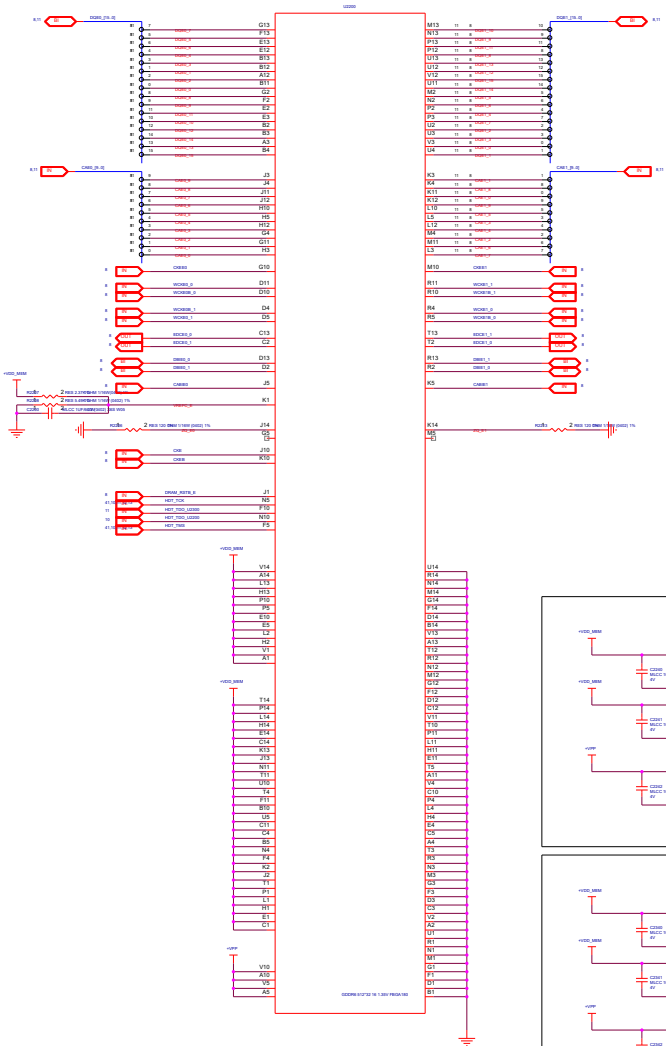
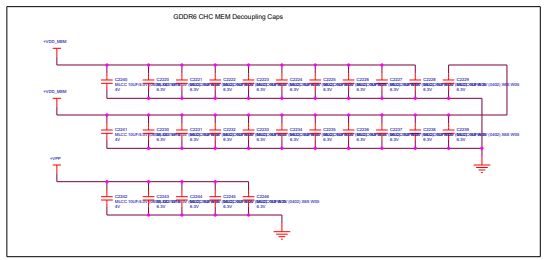
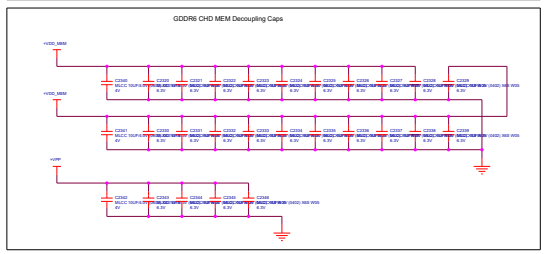
ASIC CH0 -> MEM CHA

ASIC CH1 -> MEM CHB

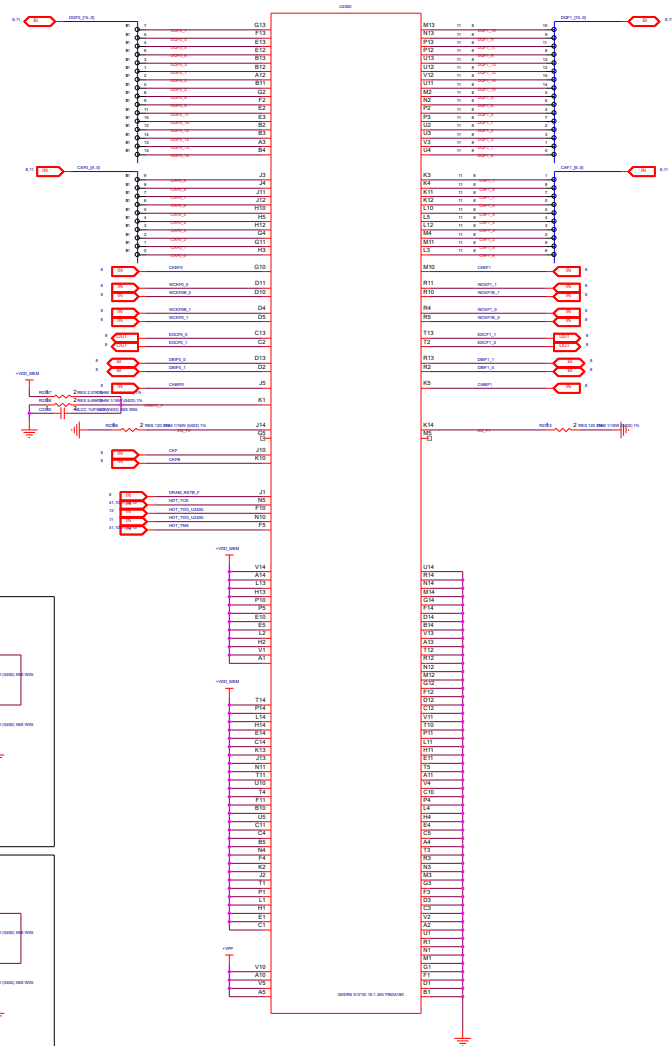






ASIC CH0 -> MEM CHA

ASIC CH1 -> MEM CHB



Title :	11 GDDR6 MEM CH EF		
<OrgName>	Engineer:	Sam Hom	
Size: Custom	Project Name: D412BS		Rev: 1.00X
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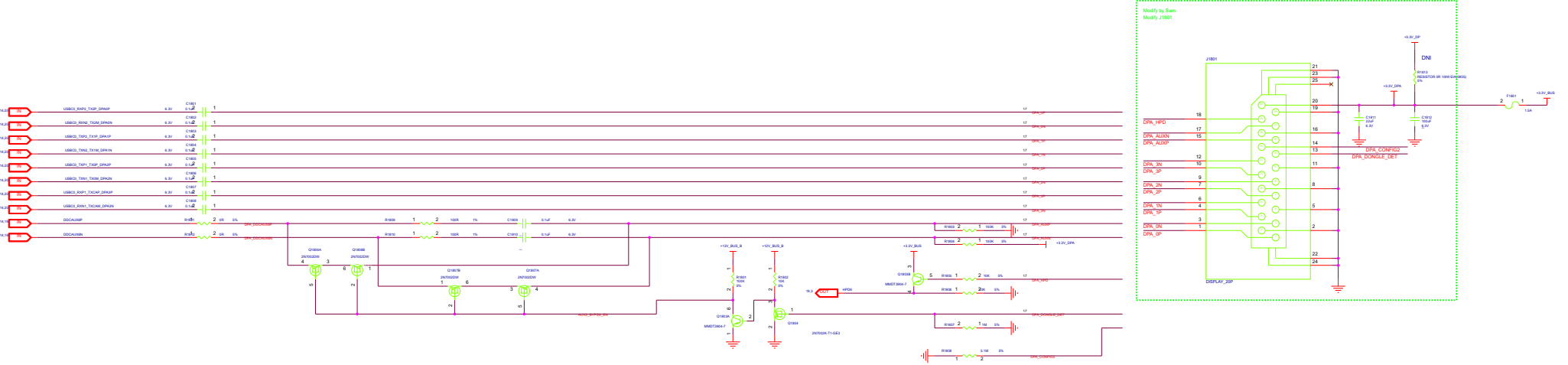

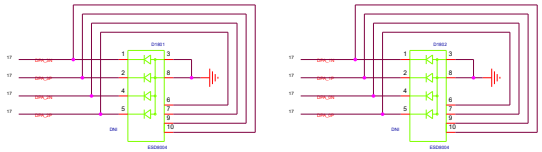

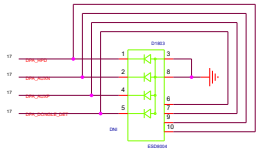

ASUS	Title :	17 NAVI21 TMDPA	
<OrgName>	Engineer:	Sam Hom	
Size: Custom	Project Name: D412BS		Rev: 1.00X
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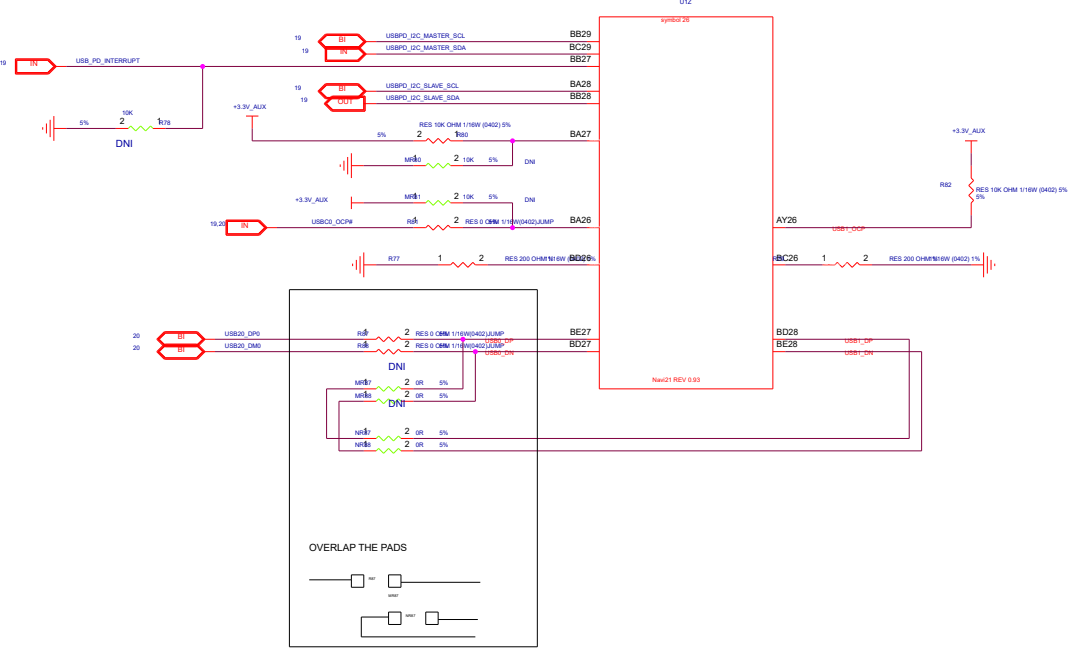
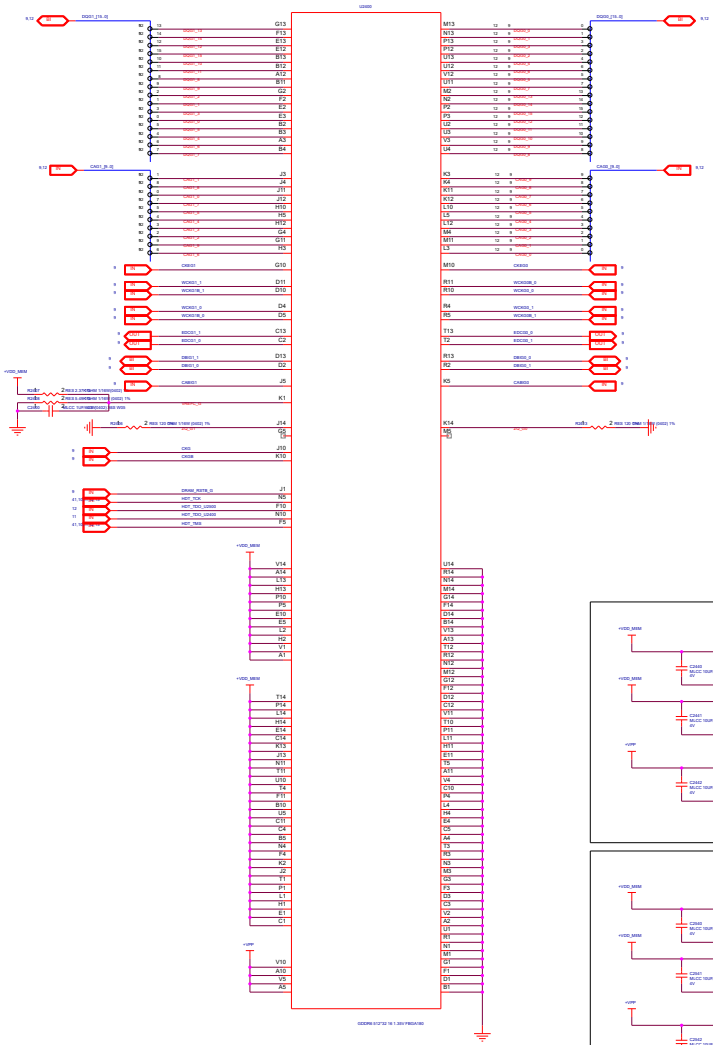
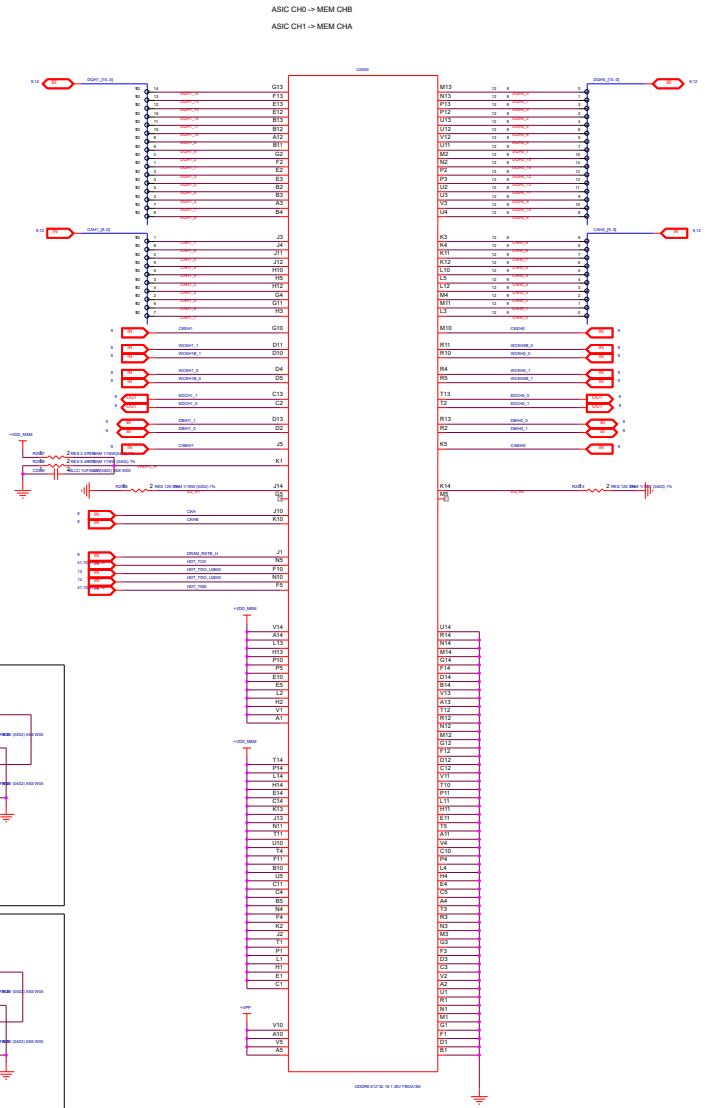


Title :	18 NAVI21 USB		
<OrgName>	Engineer:	Sam Hom	
Size: Custom	Project Name: D412BS		Rev: 1.00X
Date: Monday, August 24, 2020	Sheet 18 of 51		

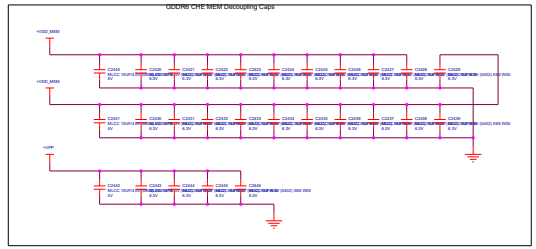
ASIC CH0 -> MEM CHB

ASIC CH1 -> MEM CHA

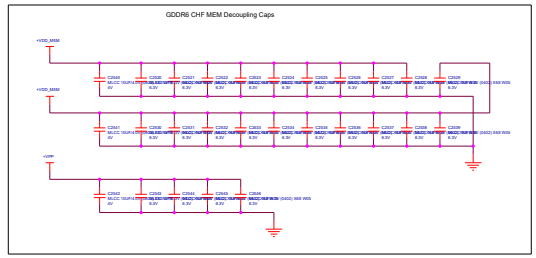




GDDR6 CHE MEM Decoupling Caps



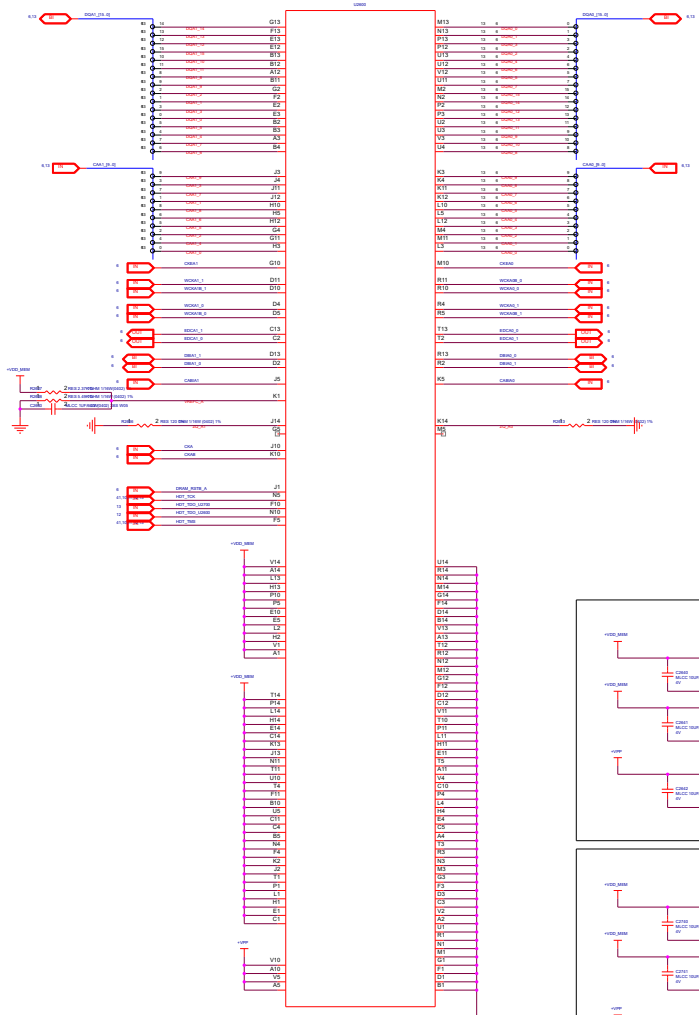
GDDR6 CHF MEM Decoupling Caps

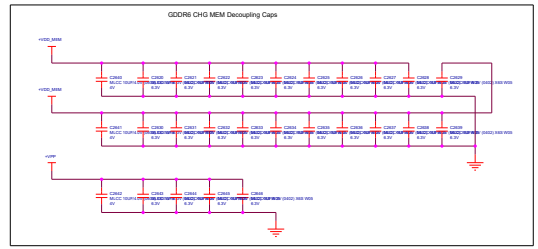


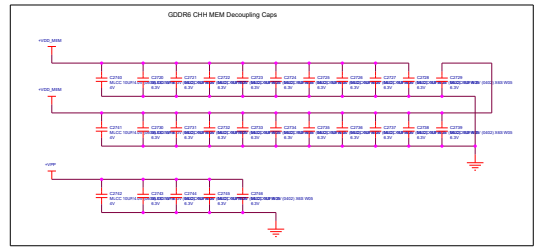
ASUS	Title :	12 GDDR6 MEM CH GH	
<OrgName>	Engineer:	Sam Hom	
Size: Custom	Project Name: D412BS		Rev: 1.00X
Date: Monday, August 24, 2020	Sheet 12 of 51		

ASIC CH0 -> MEM CHB

ASIC CH1 -> MEM CHA

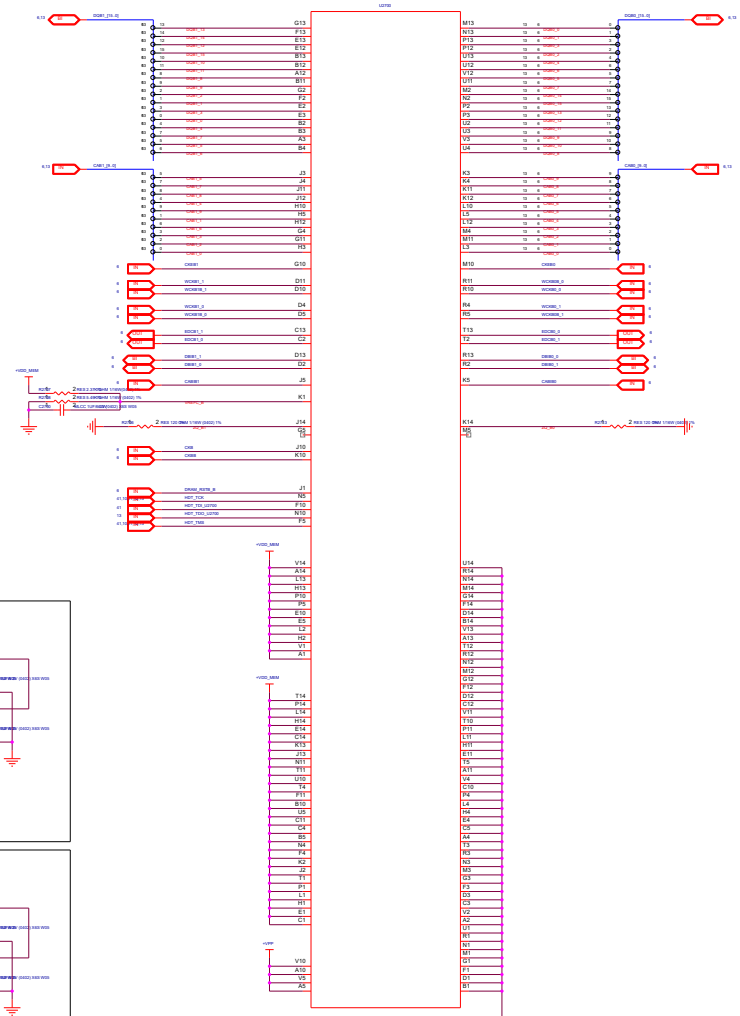




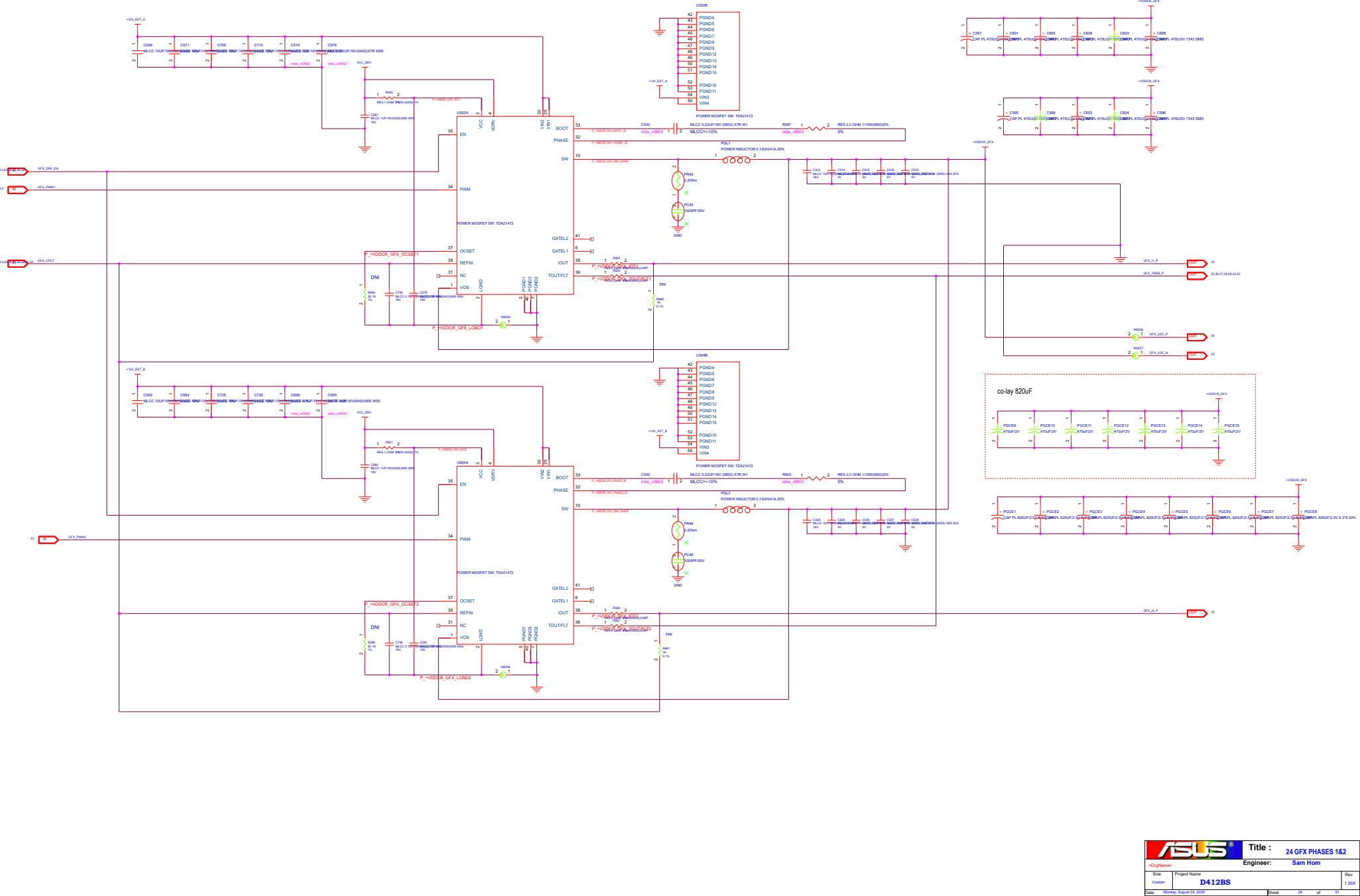


ASIC CH0 -> MEM CHB

ASIC CH1 -> MEM CHA

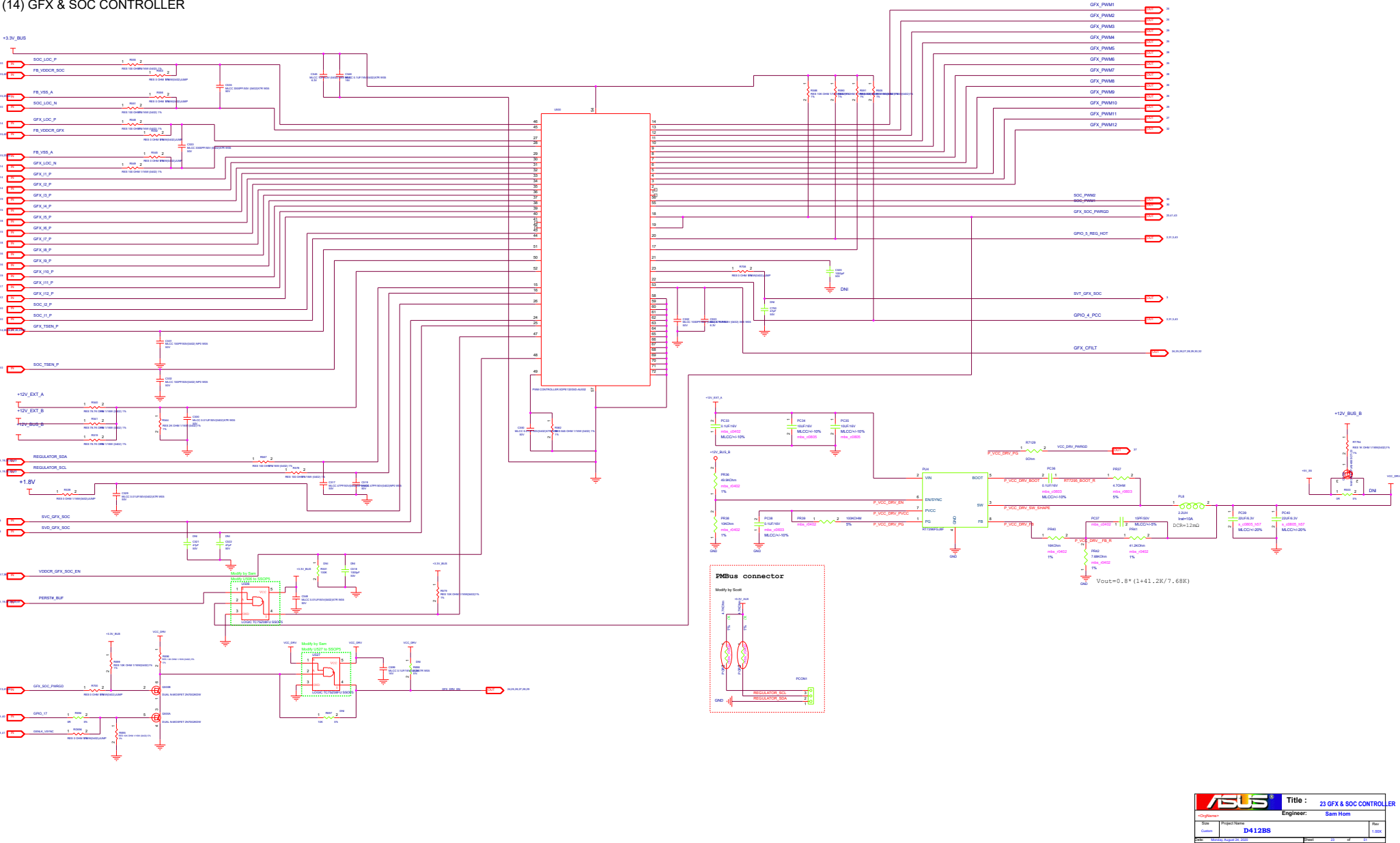


Title :	13 GDDR6 MEM CH AB		
<OrgName>	Engineer:	Sam Hom	
Size: Custom	Project Name: D412BS		Rev: 1.00X
Date: Monday, August 24, 2020	Sheet 13 of 51		

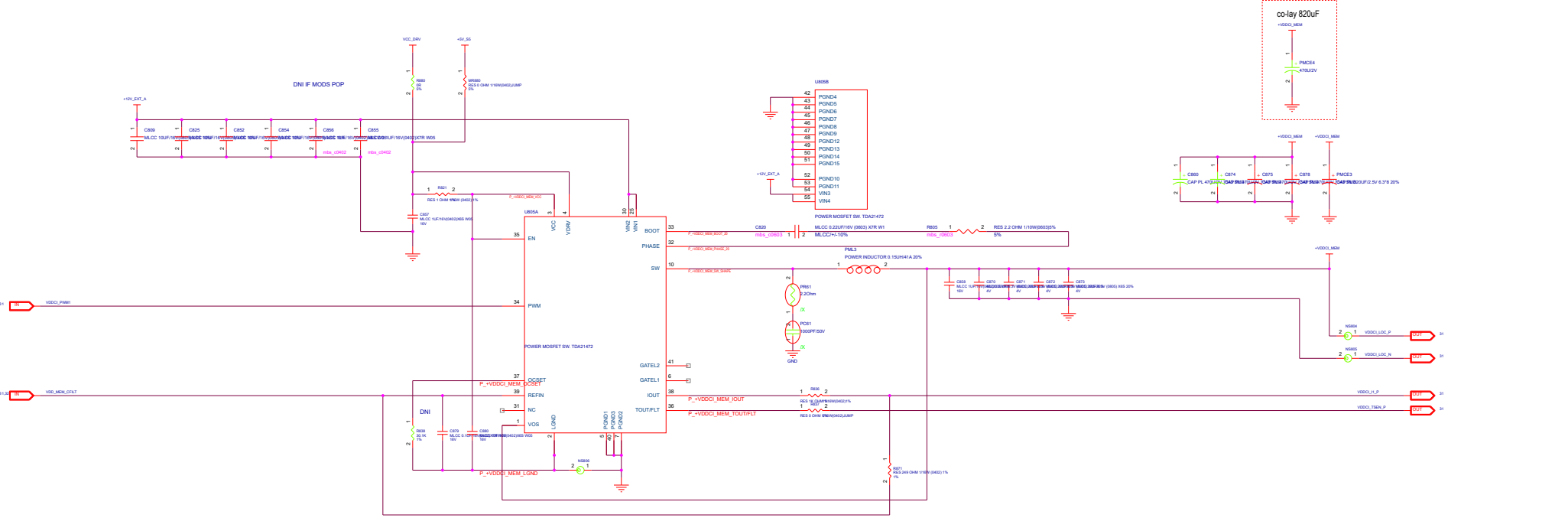


Title :	24 GFX PHASES 1&2		
<OrgName>	Engineer:	Sam Hom	
Size: Custom	Project Name: D412BS		Rev: 1.00X
Date: Monday, August 24, 2020	Sheet 24 of 51		

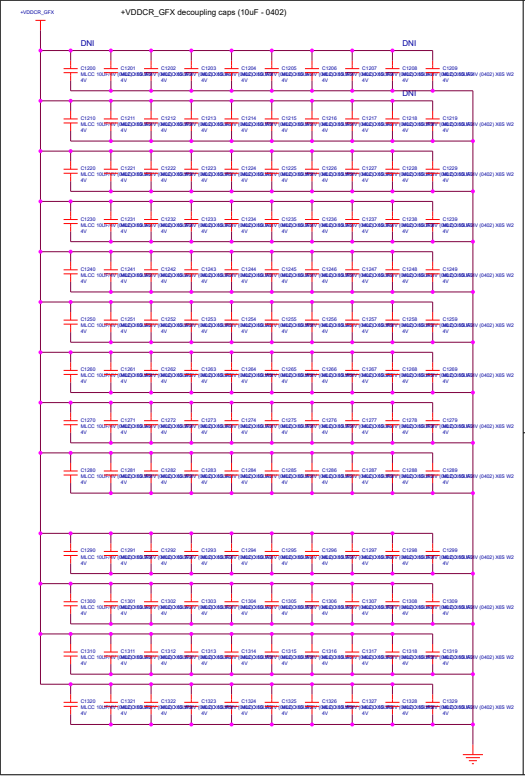
(14) GFX & SOC CONTROLLER

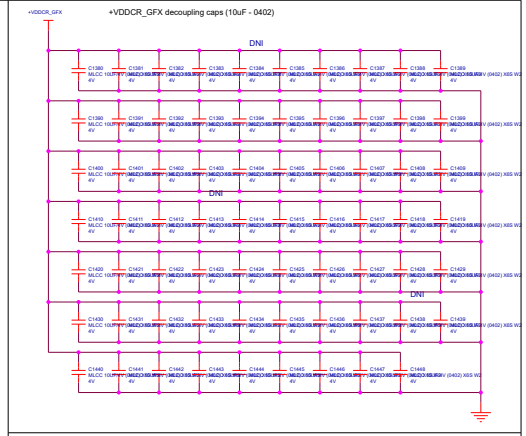


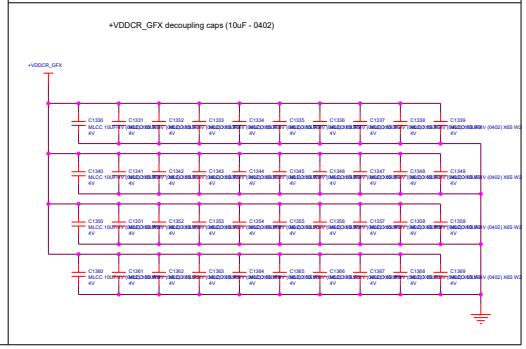
Title :	23 GFX & SOC CONTROLLER		
Engineer:	Sam Hom		
Size: Custom	Project Name: D412BS		Rev: 1.00
Date: Monday, August 24, 2020	Sheet: 23	of: 31	

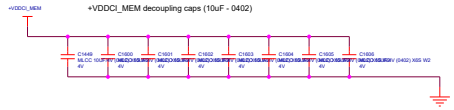


ASUS	Title :	33 VDDCI_MEM PHASE 1	
<OrgName>	Engineer:	Sam Hom	
Size: Custom	Project Name: D412BS		Rev: 1.00X
Date: Monday, August 24, 2020	Sheet 33 of 51		



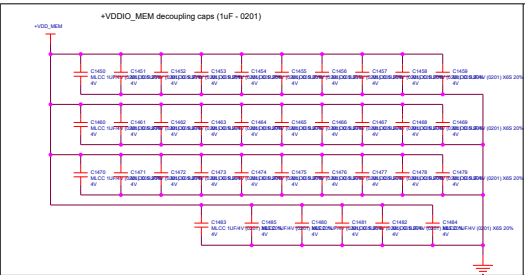


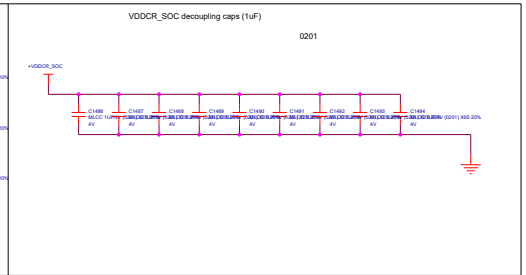


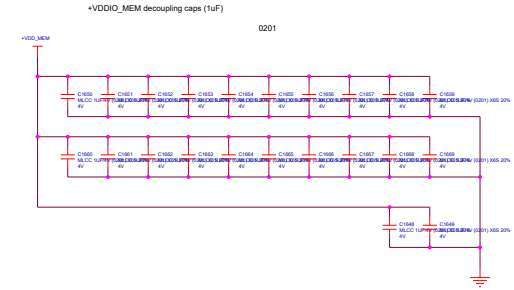


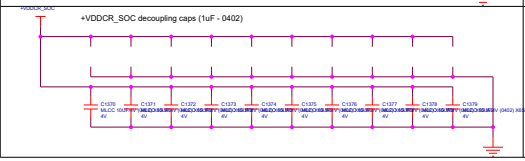
DNI these six caps to match SLT board and keep the design consistent across SKUs

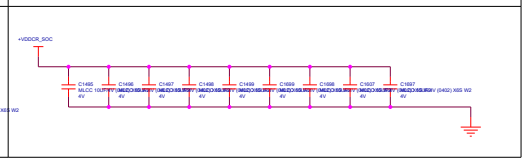
C1218
C1208
C1200
C1438
C1413
C1384

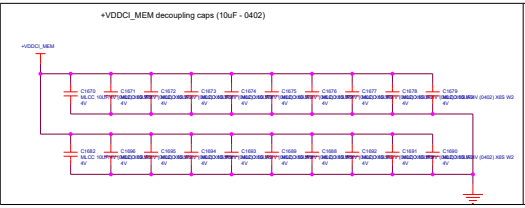


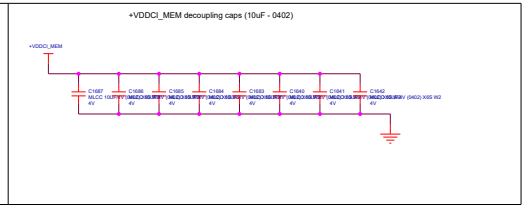




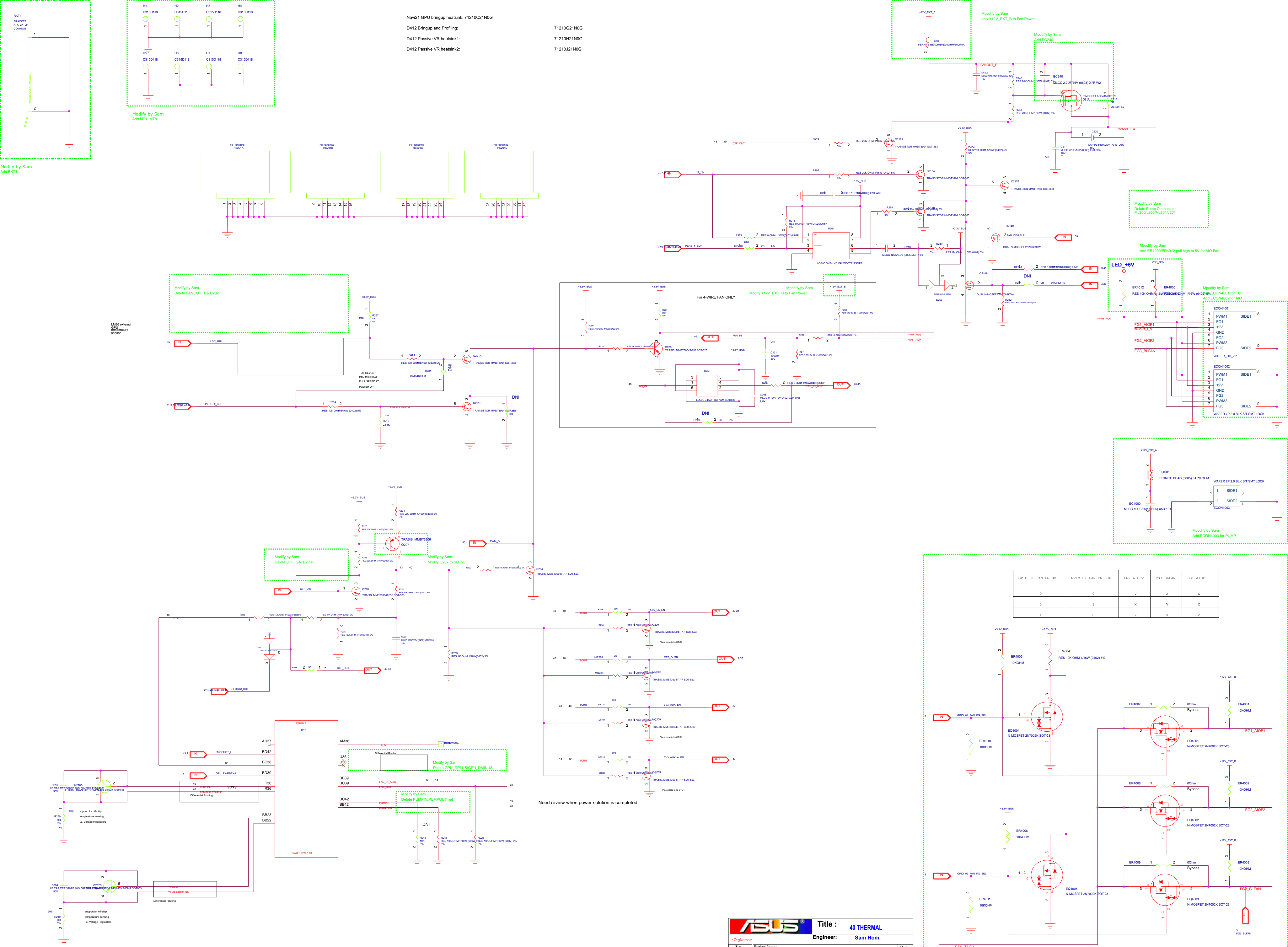








ASUS	Title :	34 NAVI 21 DECAPS	
<OrgName>	Engineer:	Sam Hom	
Size: Custom	Project Name: D412BS		Rev: 1.00X
Date: Monday, August 24, 2020	Sheet 34 of 51		

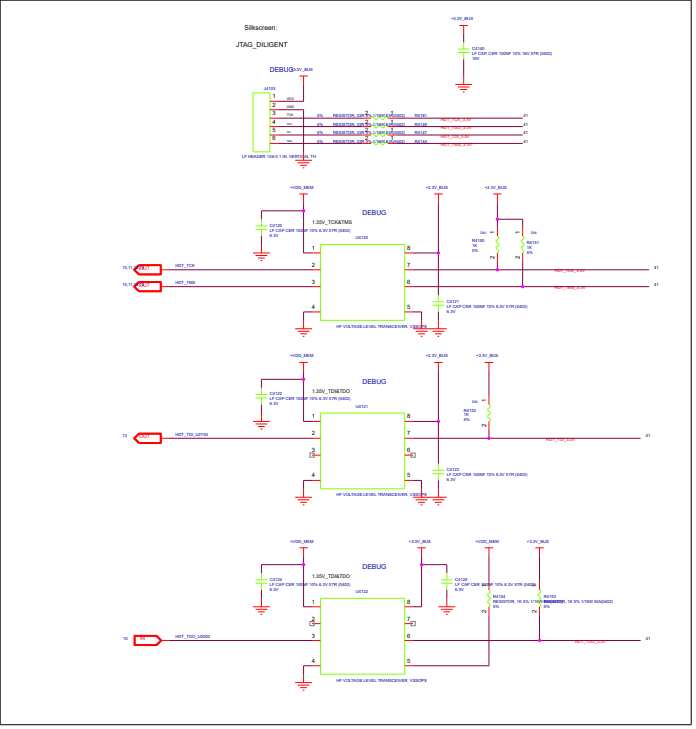

Navi21 GPU bringup heatsink: 71210C21N0G
D412 Bringup and Profiling: 71210G21N0G
D412 Passive VR heatsink1: 71210H21N0G
D412 Passive VR heatsink2: 71210J21N0G
Modify by Sam
Add BKT1
Modify by Sam
Add MT1~MT8
Modify by Sam
Delete FANOUT_T & U202
LM96 external GPU temperature sensor
TO PREVENT FAN RUNNING FULL SPEED AT POWER UP
For 4-WIRE FAN ONLY
Mpodify by Sam
Modify +12V_EXT_B to Fan Power
Mpodify by Sam
only +12V_EXT_B to Fan Power
Mpodify by Sam
Add EC240
Mpodify by Sam
Delete Pump Connector MJ200/J200/MJ201/J201
Mpodify by Sam
Add ER4009/ER4012 pull high to 5V for AIO Fan
LED_+5V
Mpodify by Sam
Add ECON4001 for TUF
Add ECON4002 for AIO
Mpodify by Sam
Add ECON4003 for PUMP
Modify by Sam
Delete CTF_GATE2 net
Modify by Sam
Modify Q207 to SOT23
Modify by Sam
Delete GPU_DPLUS/GPU_DMINUS
Modify by Sam
Delete PUMPIN/PUMPOUT net
Need review when power solution is completed
support for off-chip temperature sensing
i.e. Voltage Regulators
Differential Routing

GPIO_01_FAN_FG_SEL	GPIO_02_FAN_FG_SEL	FG2_AIOF2	FG3_BLFAN	FG1_AIOF1
0	0	V	X	X
0	1	X	V	X
1	0	X	X	V

Title : 40 THERMAL
<OrgName>
Engineer: Sam Hom

Size	Project Name	Rev
Custom	D412BS	1.00X

Date: Monday, August 24, 2020 Sheet 40 of 51



Modify by Sam
Delete DPM LED

Modify by Sam
Delete RGB LED header
Delete RADEON Lightbar header

<OrgName>	Title :	41 DPM_Status_LED & GDDR6_JTAG
	Engineer:	Sam Hom
Size: Custom	Project Name: D412BS	Rev: 1.00X
Date: Monday, August 24, 2020	Sheet 41 of 51	

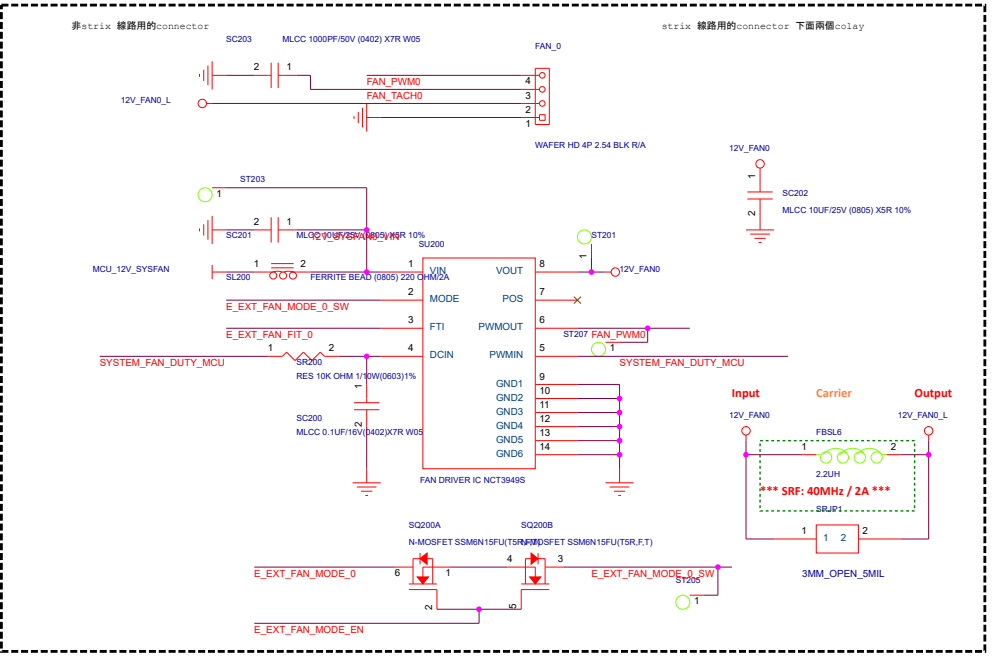
Modify by Sam
Delete U3034/U3033/U3032

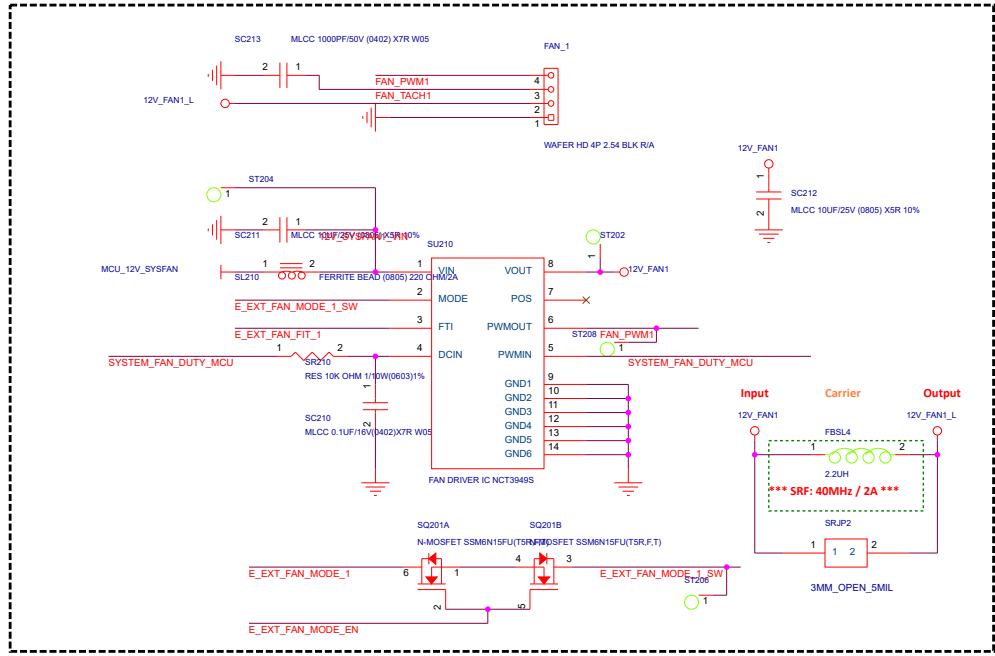
FOR PI DAUGHTER CARD
Modify by Sam
Delete PI DAUGHTER CARD

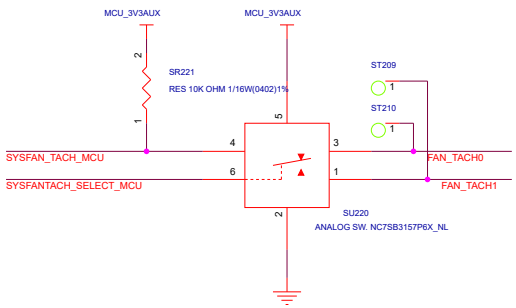
<Orgname>	Title : 42 PI Debug	
	Engineer: Sam Hom	
Size: Custom	Project Name: D412BS	Rev: 1.00X
Date: Monday, August 24, 2020	Sheet 42 of 51	

0	A	07/23/2019	Initial schematic creation
1	-00B	Nov 11 2019	Added MODS circuit
1	-00C	Jan 21 2020	Connected +1.8V_S5 to OSC_VDD18 Gated +VBUS_PWR_USBC0 by USB_5V_GOOD Modified USBC Power protection circuits

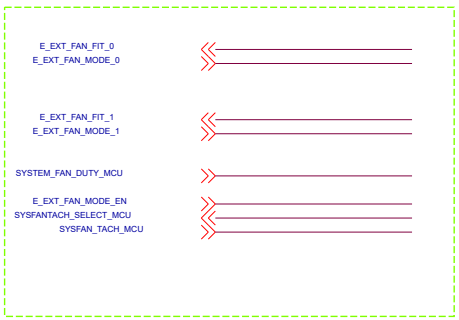
S0002 SYSTEM FAN CONTROL







Fan Control II



<OrgName>	Title :	STRIX004_SYSTEM FAN CONTROL	
	Engineer:	Sam Hom	
Size: B	Project Name: D412BS		Rev: 1.00X
Date: Monday, August 24, 2020	Sheet 50 of 51		

ASUS VGA PCB Logo

LOGO1
1 CE
CE

LOGO2
1 VCCI
VCCI

LOGO3
1 EMI_D33005_H
EMI_D33005_H

LOGO4
1 FCC
FCC

LOGO5
1 RCM
RCM

LOGO6
1 CAN ICES-3(B)/NMB-3(B)
CAN_ICES_3B_NMB_3B

LOGO7
1 KC R-R-MSQ-XXXXXXXXXXXXX
KC_R_R_LOGO

LOGO8
1 UKRAINE
UKRAINE

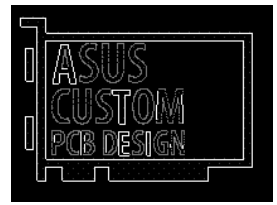
LOGO9
1 PCB MADE IN CHINA
PCB_MADE_IN_CHINA

LOGO10
1 MARK_L
S_MARK_L

LOGO11
1 WEEE_LOGO
WEEE_LOGO

ASUS Re-design logo
Do not place this on reference board

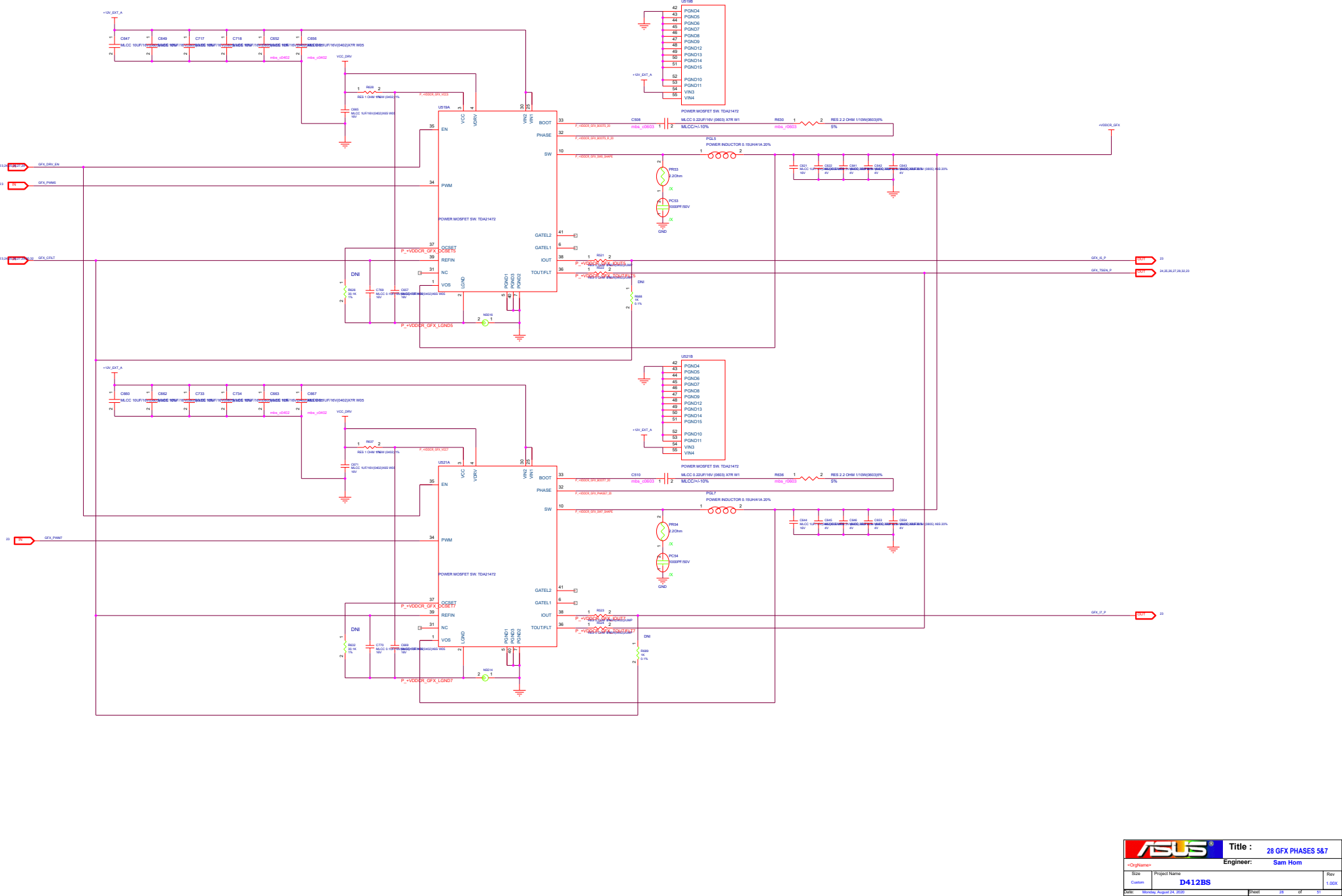
LOGO13
1 ASUS CUSTOM PCB DESIGN
ASUS_CUSTOM_PCB



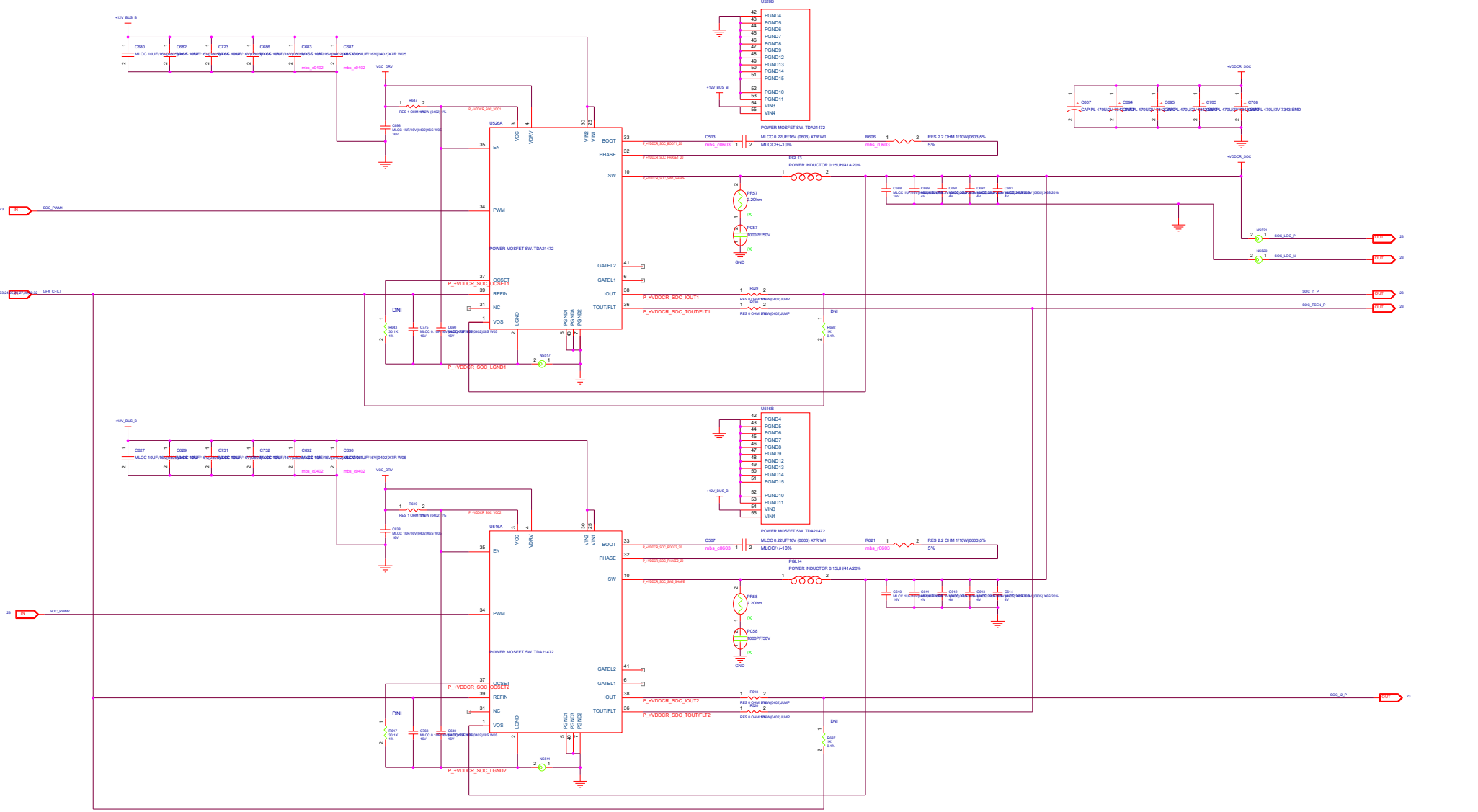
LOGO12
1 SFIS
SFIS

M1
1 PCB_ruler ASUS
PCB_RULER_ASUS

Title :	XX ASUS PCB Logo	
<OrgName>	Engineer:	Sam Hom
Size: A3	Project Name: D412BS	Rev: 1.00X
Date: Monday, August 24, 2020	Sheet 51 of 51	

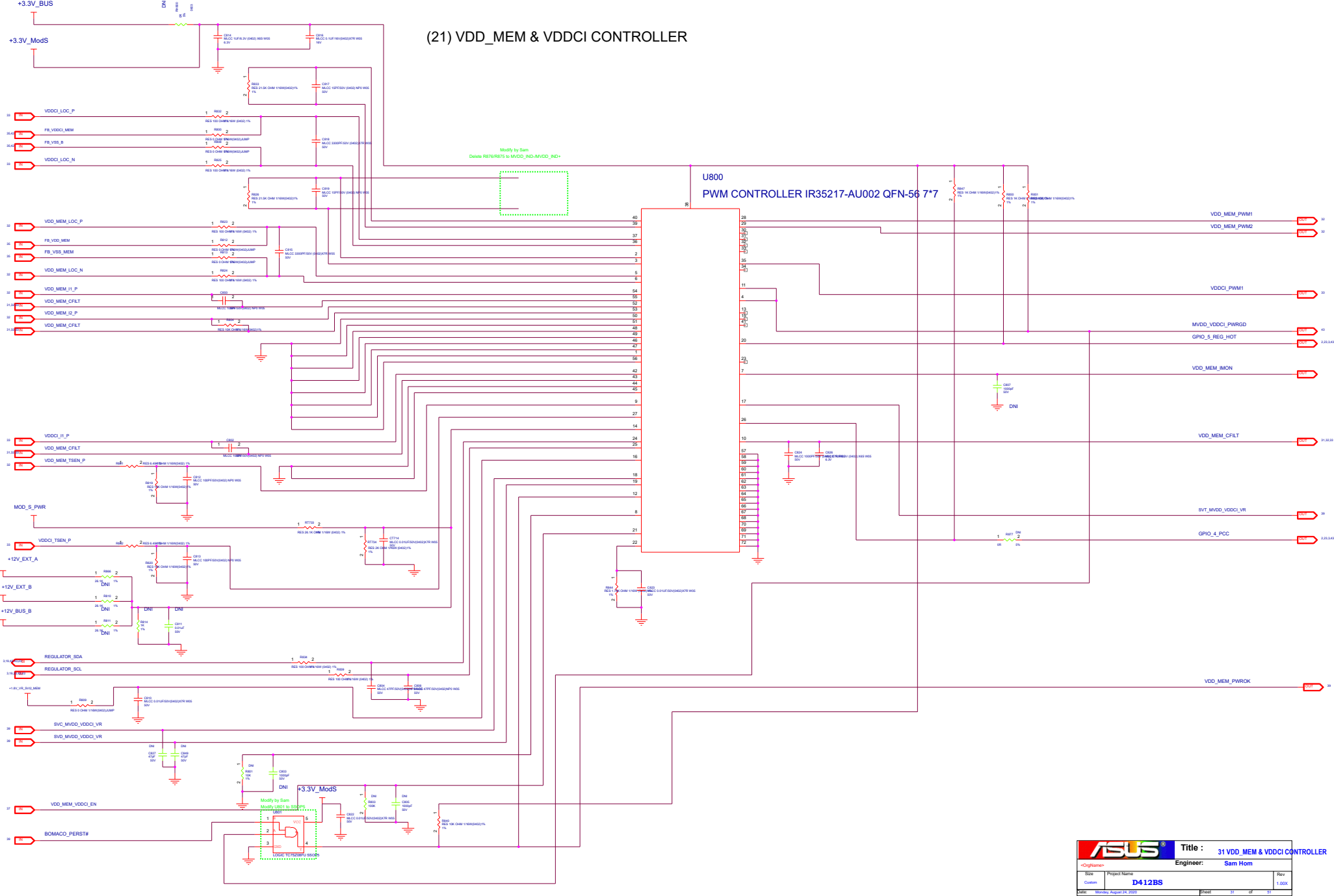


ASUS	Title :	28 GFX PHASES 5&7	
<OrgName>	Engineer:	Sam Hom	
Size: Custom	Project Name: D412BS		Rev: 1.00X
Date: Monday, August 24, 2020	Sheet 28 of 51		

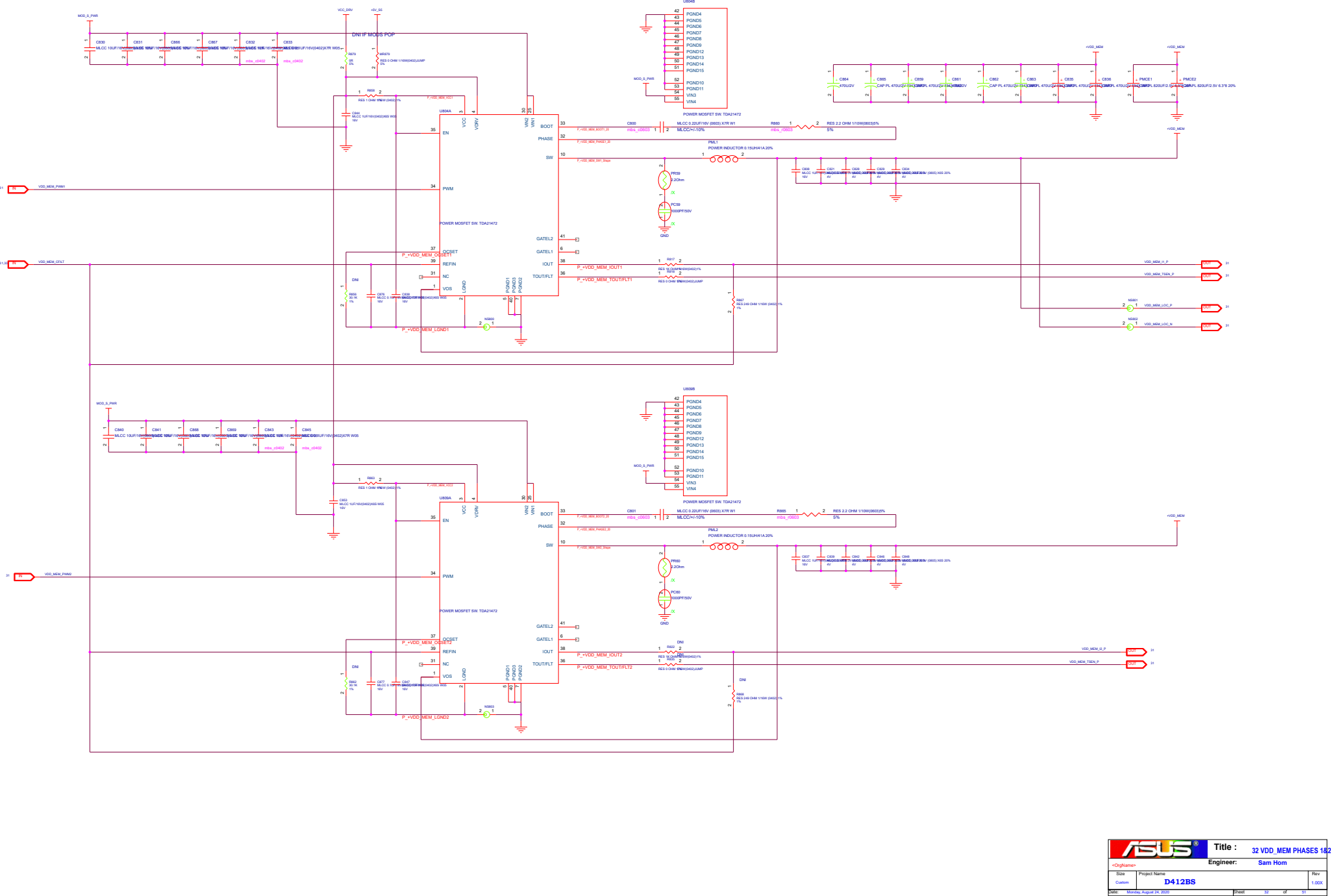


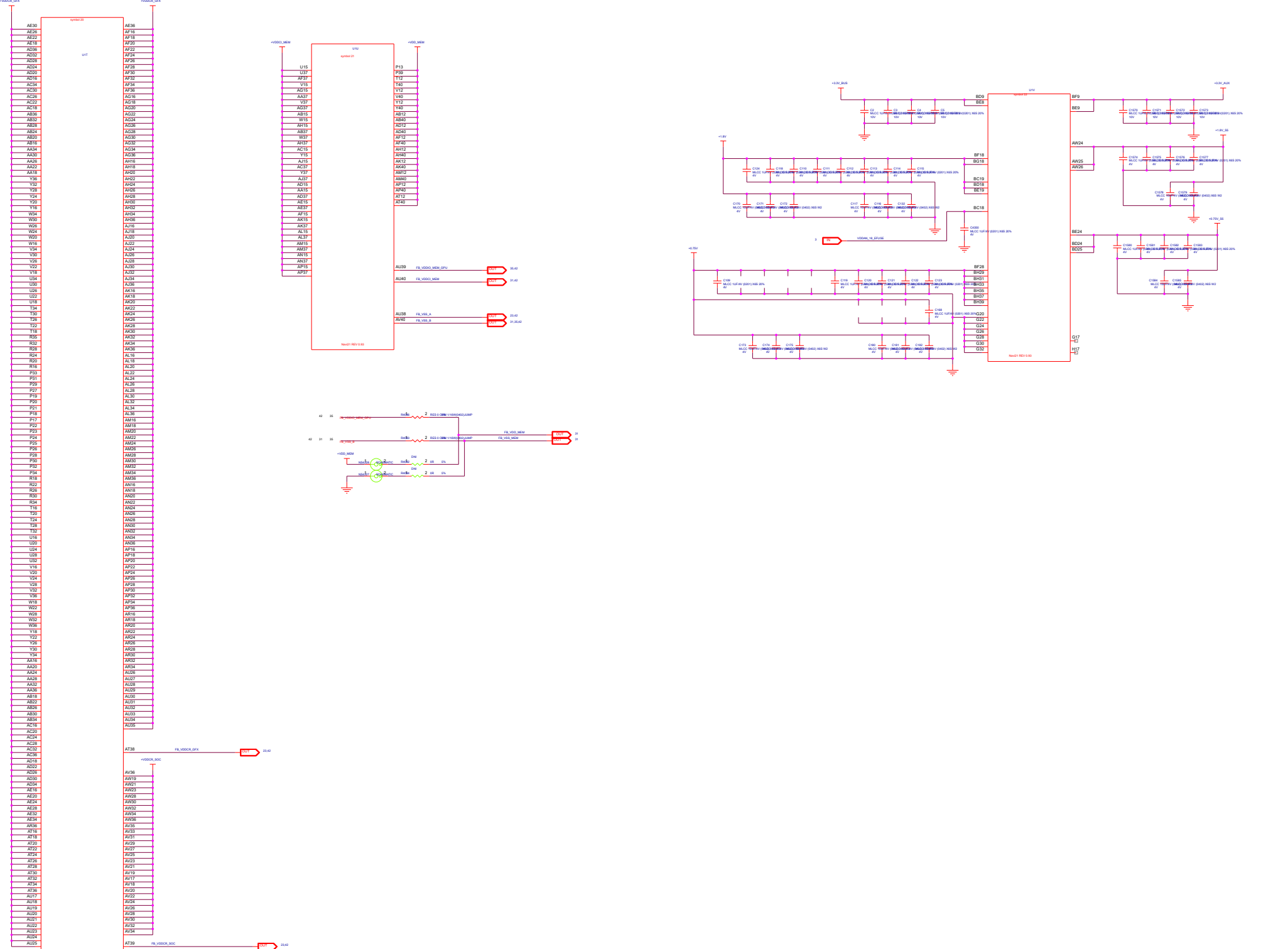
Title :	30 SOC PHASE 1&2		
<OrgName>		Engineer:	Sam Hom
Size: Custom	Project Name: D412BS		Rev: 1.00X
Date: Monday, August 24, 2020		Sheet 30 of 51	

(21) VDD_MEM & VDDCI CONTROLLER



Title :	31 VDD_MEM & VDDCI CONTROLLER
Engineer:	Sam Hom
Size	Project Name / Rev
Customs	D412BS / 1.00X
Date: Monday, August 24, 2020	Sheet 31 of 51


DNI IF MOBS POP
U804B
U804A
U809B
U809A
POWER MOSFET SW. TDA21472
POWER INDUCTOR 0.15UH/41A 20%
VDD_MEM_PWM1
VDD_MEM_PWM2
VDD_MEM_CFILT
P_+VDD_MEM_IOUT1
P_+VDD_MEM_TOUT/FLT1
P_+VDD_MEM_IOUT2
P_+VDD_MEM_TOUT/FLT2
P_+VDD_MEM_LGND1
P_+VDD_MEM_LGND2
VDD_MEM_IT_P
VDD_MEM_TSEN_P
VDD_MEM_LOC_P
VDD_MEM_LOC_N
VDD_MEM_IT_P
VDD_MEM_TSEN_P
+VDD_MEM
Title : 32 VDD_MEM PHASES 1&2
Engineer: Sam Hom
Project Name D412BS
Rev 1.00X
Date: Monday, August 24, 2020
Sheet 32 of 51



ASUS

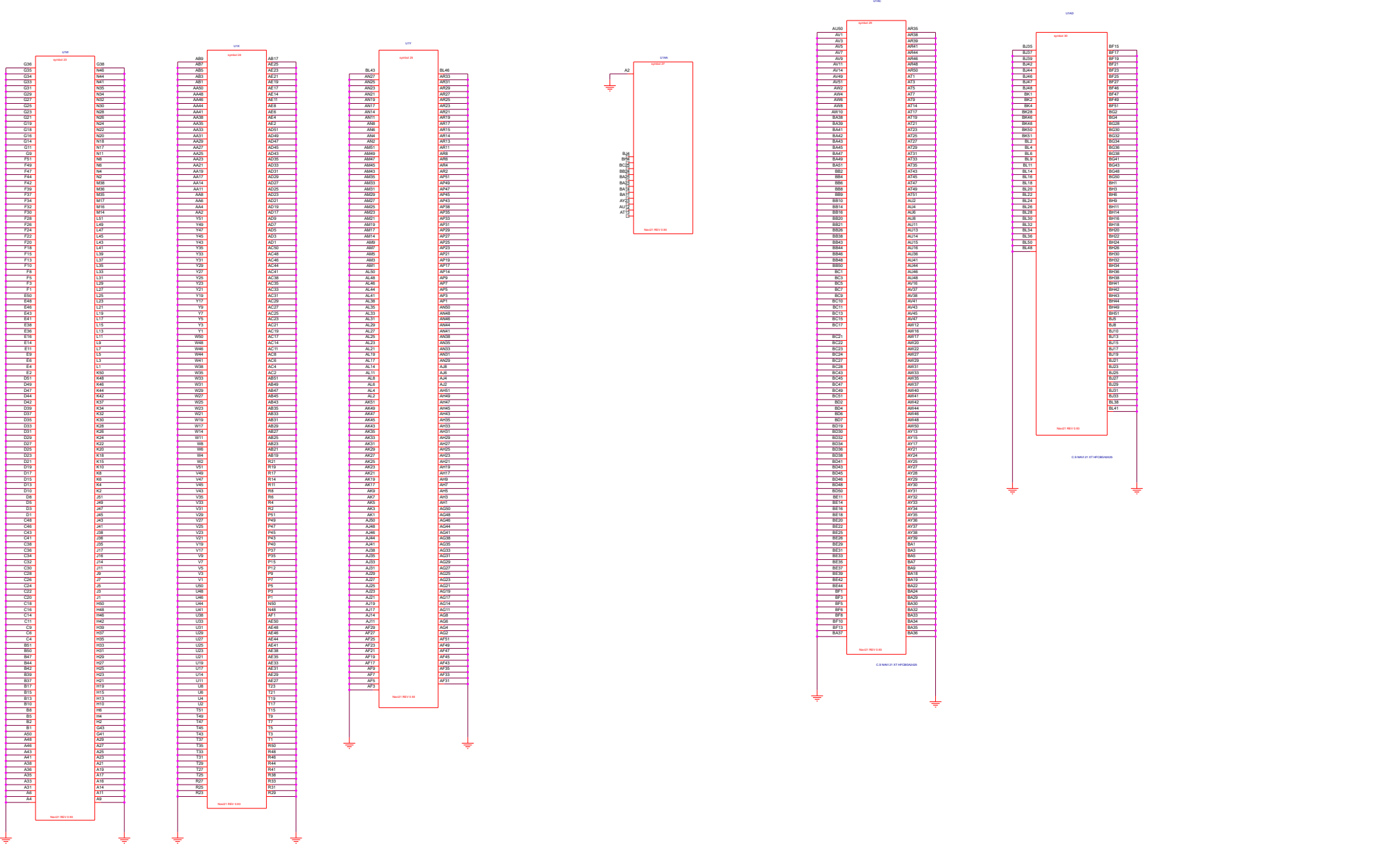
Title : 35 NAVI 21 POWER

<OrgName>

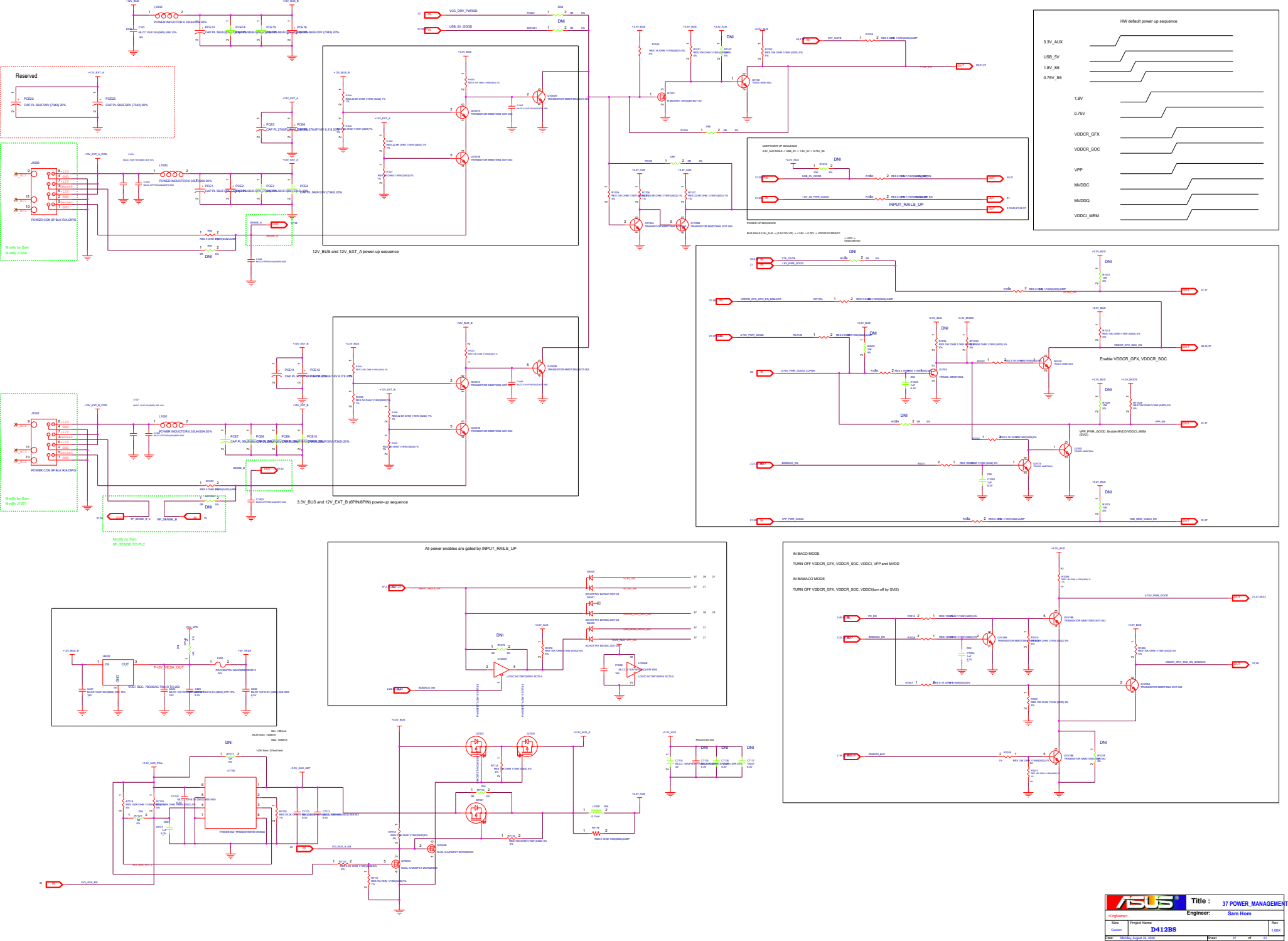
Engineer: Sam Hom

Size: Custom | Project Name: D412BS | Rev: 1.00X

Date: Monday, August 24, 2020 | Sheet 35 of 51



Title :	36 NAVI 21 POWER and GND
<OrgName>	Engineer: Sam Hom
Size: Custom	Project Name: D412BS
Rev: 1.00X	
Date: Monday, August 24, 2020	Sheet 36 of 51



Title :	37 POWER_MANAGEMENT		
Engineer:	Sam Hom		
<OrgName>			
Size	Project Name		Rev
Custom	D412BS		1.00X
Date:	Monday, August 24, 2020	Sheet	37 of 69

Modify by Scott

Delete QC1112/QC1113/QC1110/QC1114/QC1115/UC1119

Modify by Scott

Delete UC1110/UC1111/UC1112/UC1113/UC1114
UC1115/UC1116/UC1117/UC1118/UC1119

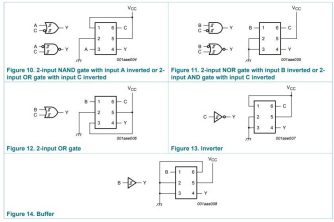


Figure 10. 2-input NAND gate with input A inverted or 2-input OR gate with input C inverted

Figure 11. 2-input NOR gate with input B inverted or 2-input AND gate with input C inverted

Figure 12. 2-input OR gate

Figure 13. Inverter

Figure 14. Buffer

Figure 8. 2-input MUX

Figure 9. 2-input AND gate

Modify by Scott

Delete QC1116/QC1117

<OrgName>		Title :	38 ClampWA
		Engineer:	Sam Hom
Size: Custom	Project Name: D412BS		Rev: 1.00X
Date: Monday, August 24, 2020		Sheet 38 of 51	

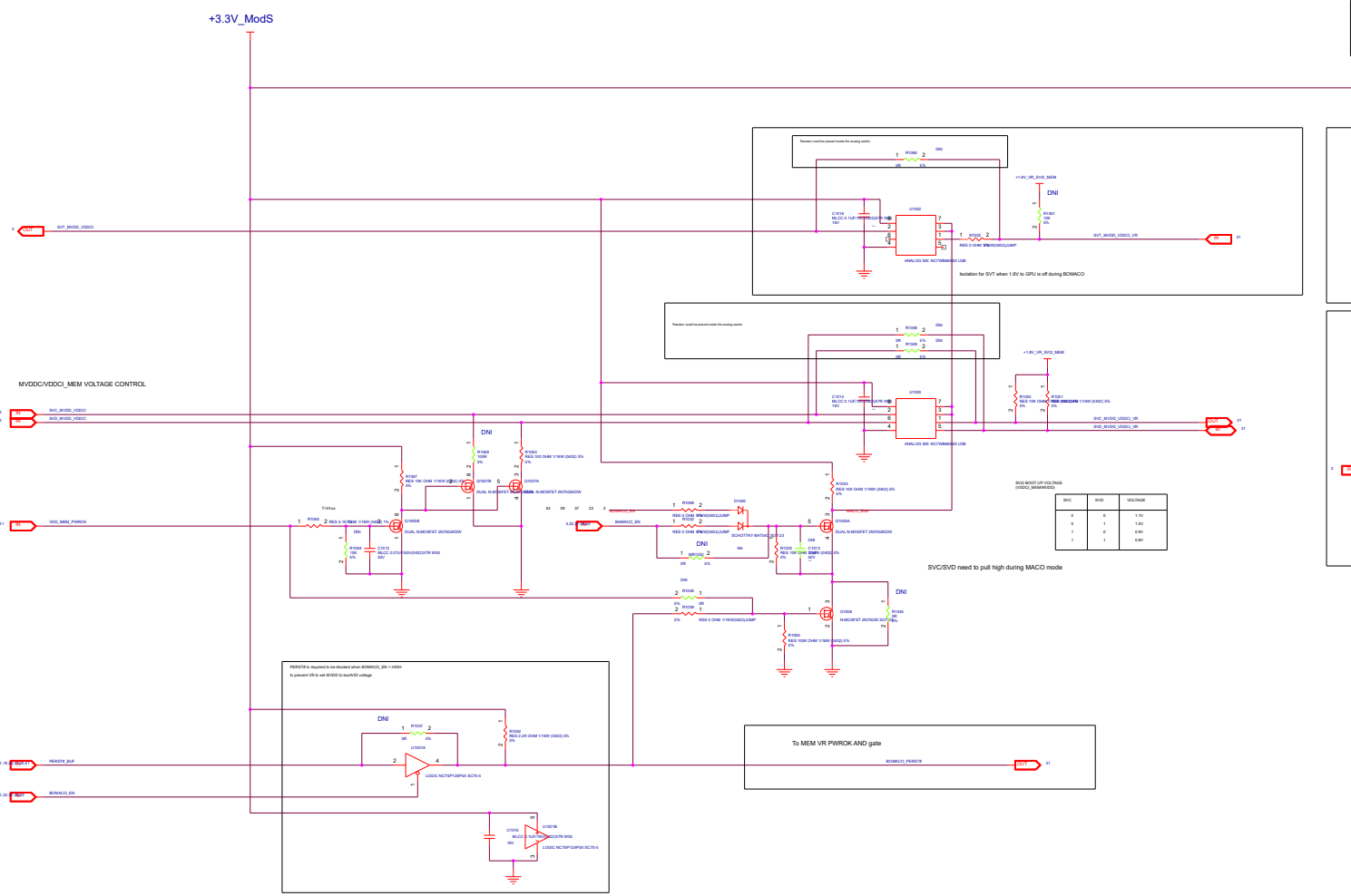


Table 3 Power Rails Status at BAMACO Mode

Power Rail at ASIC	Used logic	ON/OFF Status
VDDCR_GFX	GFX IP, SDMA, GFXCLK CLKIP	OFF
VDDCR_SOC	SYS IPs	OFF
VDDCI_MEM	MEM PHY	OFF
VDDIO_MEM	MEM PHY	ON
MVDDC/MVDDQ/VPP	DRAM	ON
VDDCR_BACO	NBIO/THM/MP1/USB	ON
VDDIO_PCIE	PCIe PHY	ON
VDDAN_C	PHY	ON
VDDAN_18	PLL, PHY, etc	ON
VDDIO_18	1.8V GPIO, I2C, etc	ON
VDDIO_33	3.3V GPIO	ON
VDDAN_*_EFUSE	EFUSE	ON
VDDCR_S5*	USB	ON

Table 4 Key Signals at Different PM Modes

Signals	Default	BOCO	BOMACO
PX_EN	LOW	N/A	N/A
MACO_EN	N/A	N/A	N/A
PERSTB	HIGH	1->0->1	1->0->1
PWR_EN	HIGH	LOW	LOW
BOMACO_EN	LOW	LOW	HIGH

Table 5 Platform to Support BOMACO

BOMACO_EN	SVC PU/PD	SVD PU/PD
HIGH	PU	PU
LOW	bootVID	bootVID

Table 3 Power Rails Status at BOMACO Mode

Power Rail at ASIC	Used logic	ON/OFF Status for BOMACO-A
VDDCR_GFX	GFX IP, SDMA, GFXCLK CLKIP	OFF
VDDCR_SOC	SYS IPs	OFF
VDDCI_MEM	MEM PHY	OFF
VDDIO_MEM	MEM PHY	ON
MVDDC/MVDDQ/VPP	DRAM	ON
VDDCR_BACO	NBIO/THM/MP1/USB	OFF
VDDIO_PCIE	PCIe PHY	OFF
VDDAN_C	PHY	OFF
VDDAN_18	PLL, PHY, etc	OFF
VDDIO_18	1.8V GPIO, I2C, etc	OFF
VDDIO_33	3.3V GPIO	OFF
VDDAN_*_EFUSE	EFUSE	OFF
VDDCR_S5*	USB	ON

<OrgName>	Title : 39 SVI2 & BxMACO	
	Engineer: Sam Hom	
Size: Custom	Project Name: D412BS	Rev: 1.00X
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SWITCHES

Modify by Sam
Delete BYPASS CTF / MAXIMIZE
FAN SWITCHES

Yellow LED shows VRHOT

Modify by Sam
Delete VRHOT LED

FOR FALCON TEST

Modify by Sam
Delete Panel Control Interface

Modify by Sam
Delete PCC LED

PCC LED

Modify by Sam
Delete REGULATOR_SCL/SDA

LED RED ON indicates Fault

Modify by Sam
Delete CTF LED
Delete BACO LED
Delete BAMACO LED
Delete BOMACO LED

Modify by Sam
Delete U200

EMC1412 for EXT TMON to Provide CAL AND OFFSET

Modify by Sam
Delete EMC1412 for EXT TMON to Provide CAL AND OFFSET

7-BIT I2C ADDRESS: 0x7C

THERMAL SENSOR FOR GDDR6

Modify by Sam
Delete THERMAL SENSOR FOR GDDR6

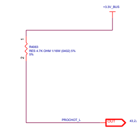
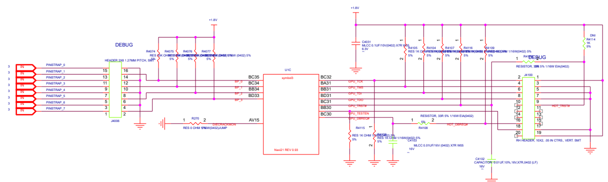


Table 4. Address Pin and Slave Addresses

DEVICE TWO-WIRE ADDRESS	A0 PIN CONNECTION
1001000	Ground
1001001	V+
1001010	SDA
1001011	SCL

DEBUG



Modify by Sam
Delete THERMAL SENSOR FOR VDDGFX

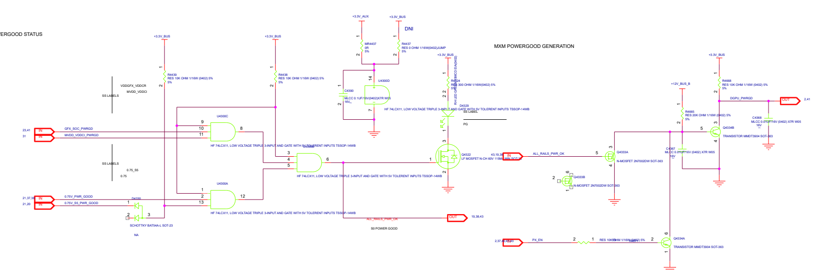
THERMAL SENSOR FOR VDDGFX

Modify by Sam
Delete THERMAL SENSOR FOR MVDD

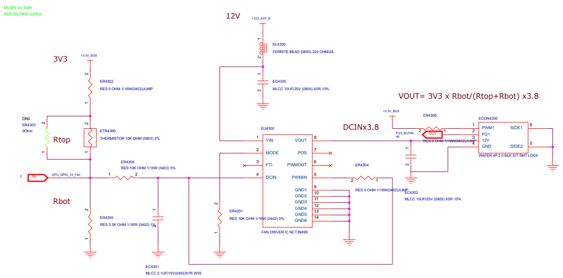
THERMAL SENSOR FOR MVDD

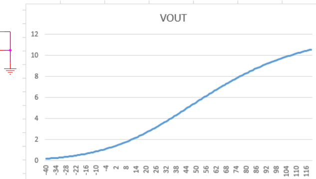
POWERGOOD STATUS

MXM POWERGOOD GENERATION



Modify by Sam
ADD BUFAN control





ASUS	Title :	43 DEBUG	
<OrgName>	Engineer:	Sam Hom	
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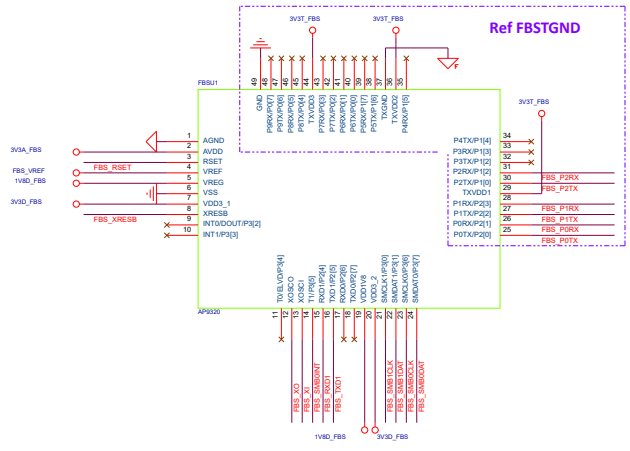
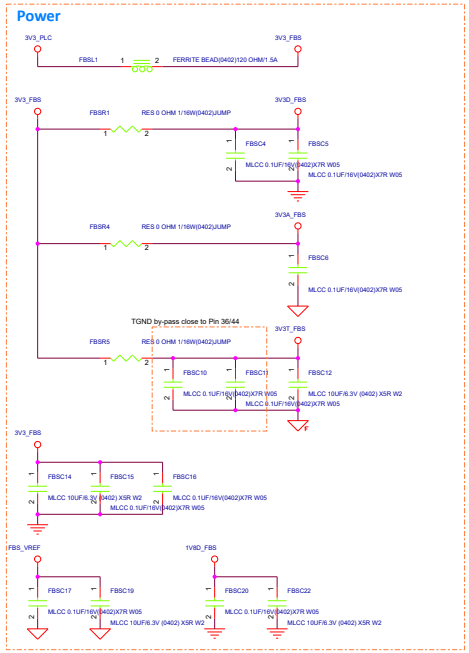
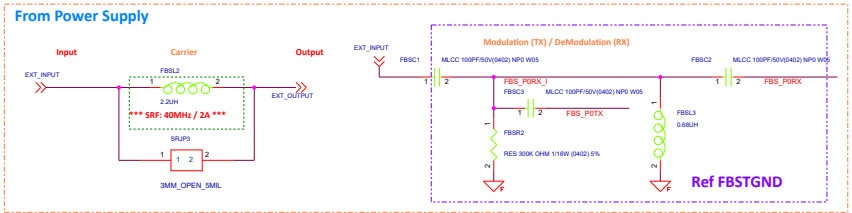
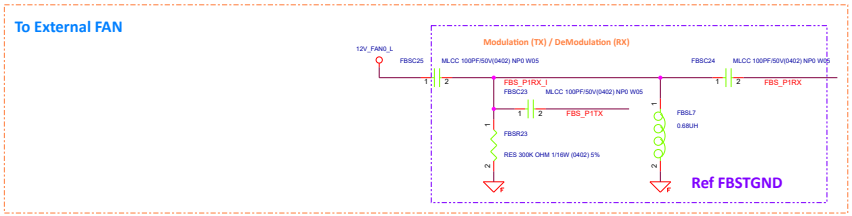
Layout Guide Line

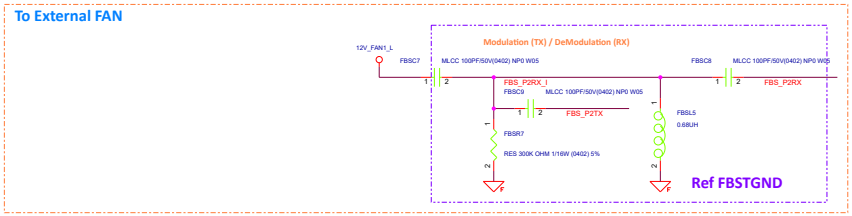
1. FBS_PnRX_I, FBS_PnRX, FBS_PnTX 距離其它net至少20mils space.
2. 紫色框內, 全部都要參考FBSTGND.
3. 隔離電感儘量靠近Connector, 接到PLC可拉一般正常線寬. 間隔20mils space.

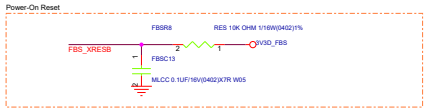


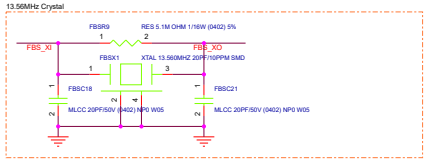


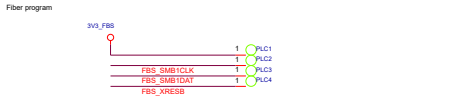


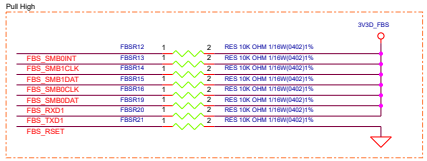


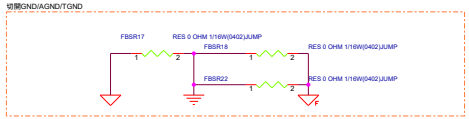


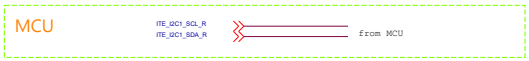


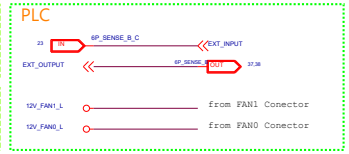


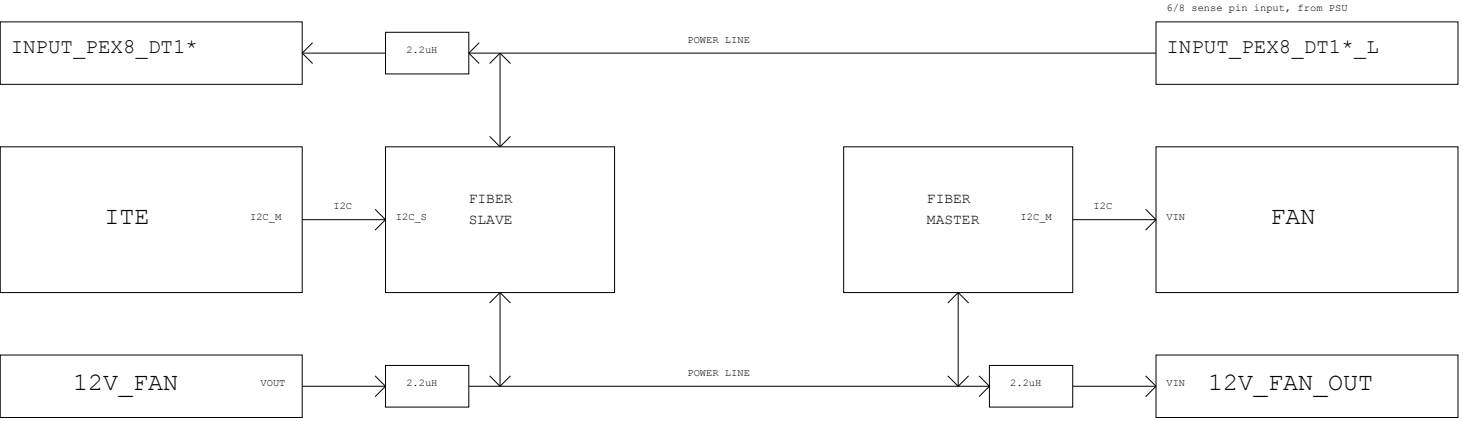


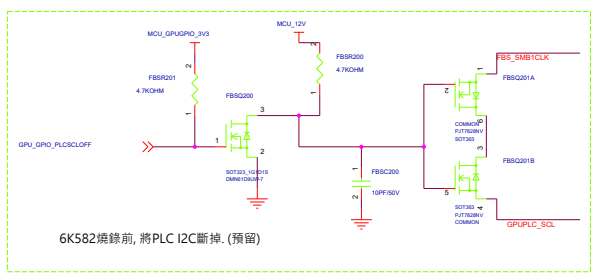












ASUS	Title :	PLC001_PLC COMM	
<OrgName>	Engineer:	Sam Hom	
Size: C	Project Name: D412BS		Rev: 1.00X
Date: Monday, August 24, 2020	Sheet 45 of 51		

Power

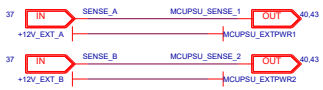
From 12V (for 外接式風扇使用, 任一組12V皆可)

From PCIE 3V3_AUX (for ITE)

From BUS 3V3 (for ITE logic判斷)

For 12V to 5V ARGB PWR

PSU DETECT INPUT

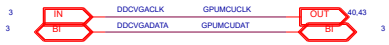


From EXT 0 (外部電源第一組)

From EXT1 (外部電源第二組)

From EXT1 (外部電源第三組)

I2C



GPU I2CB Master (for ITE / ENE)

GPU_GPIO

ASUS	Title : STRIX000_POWER & OFF-PAGE	
<OrgName>	Engineer: Sam Hom	
Size: B	Project Name: D412BS	Rev: 1.00X
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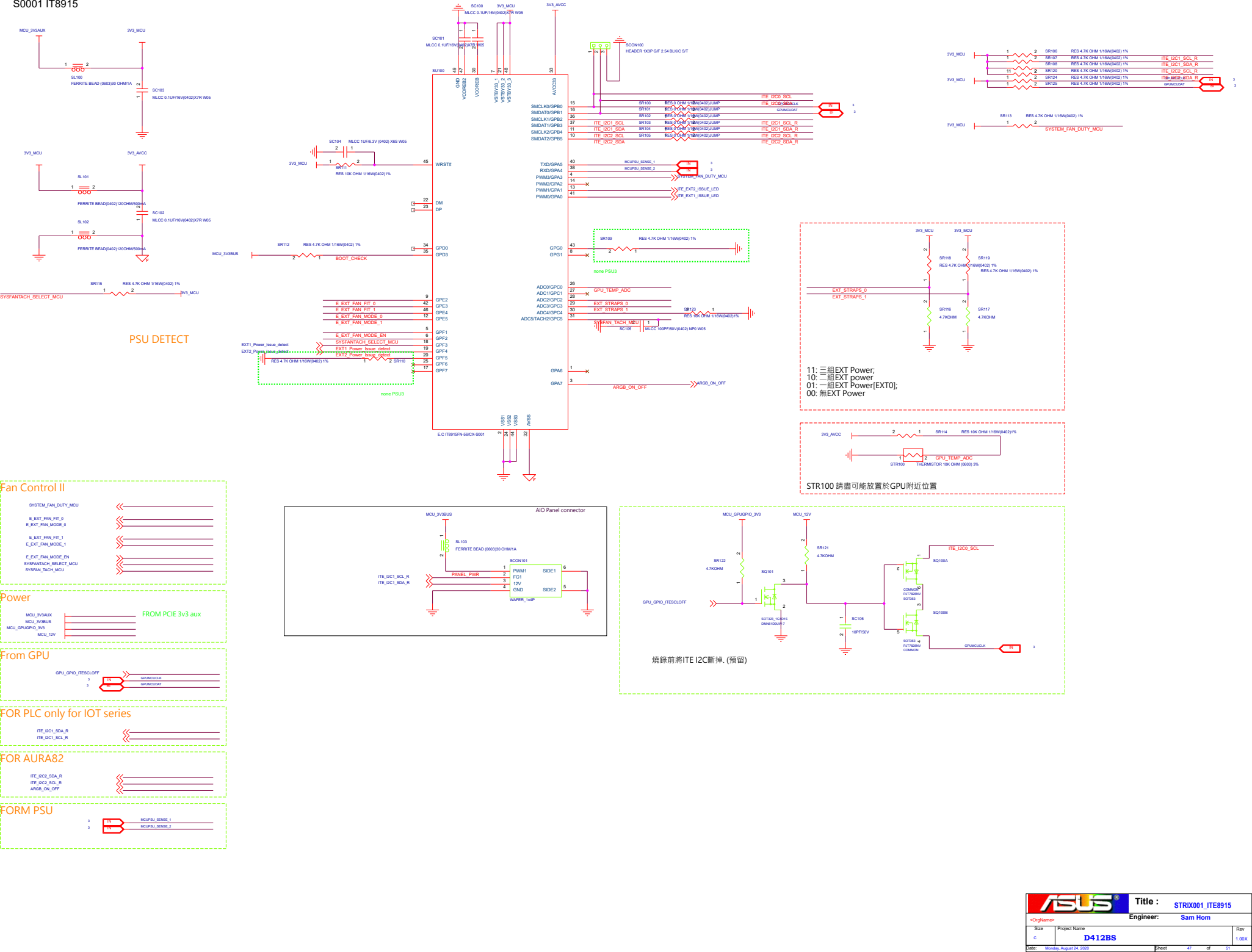
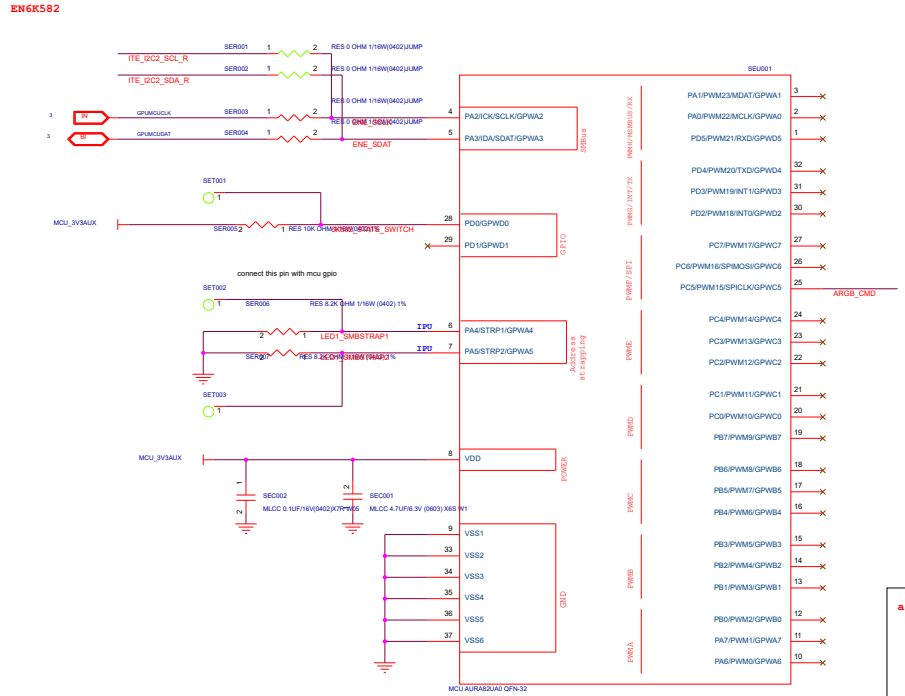
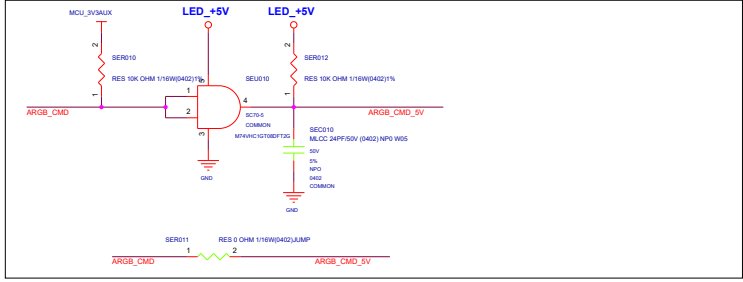
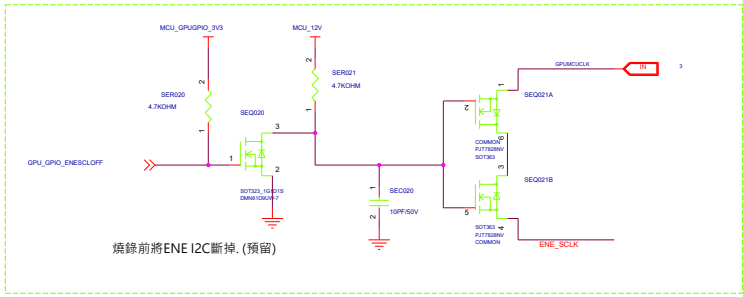
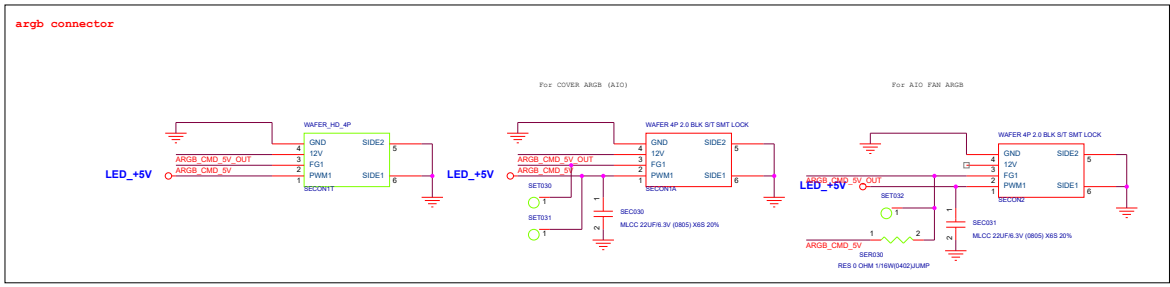


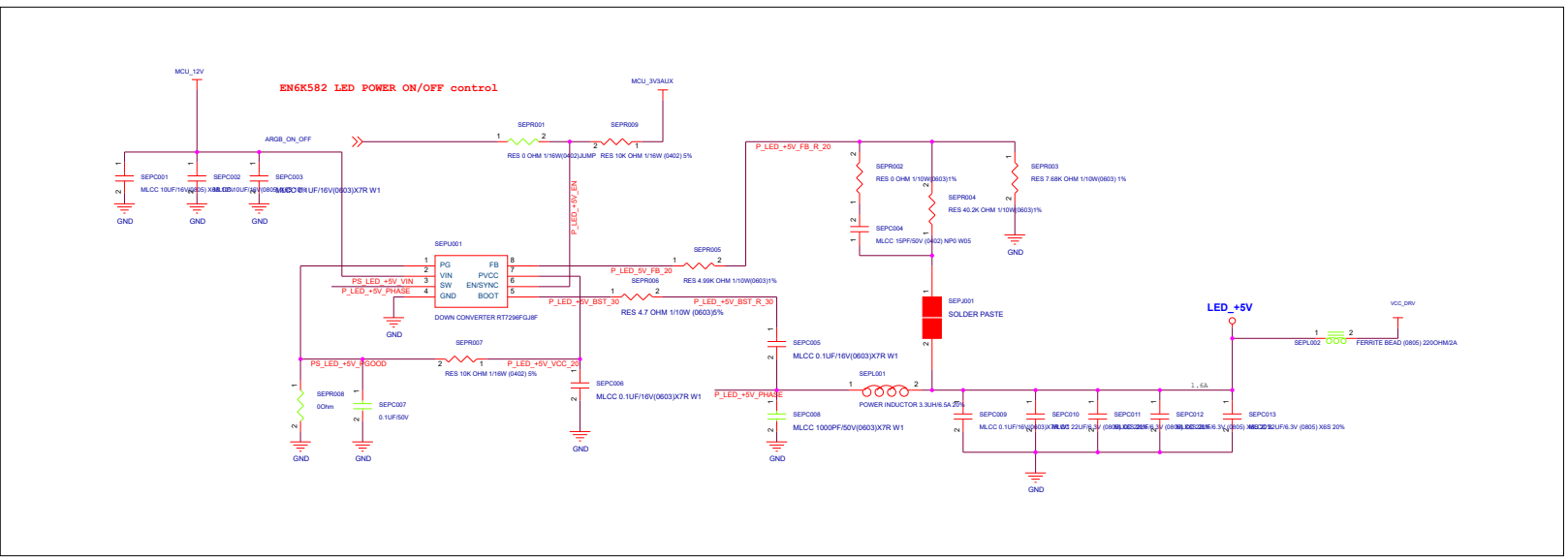
Title :	STRIX001_ITE8915		
<OrgName>	Engineer:	Sam Hom	
Size: C	Project Name: D412BS		Rev: 1.00X
Date: Monday, August 24, 2020	Sheet 47 of 51		

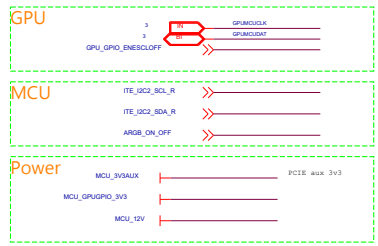












ASUS	Title :	STRIX002_ARUA82UA0	
<OrgName>	Engineer:	Sam Hom	
Size: C	Project Name: D412BS		Rev: 1.00X
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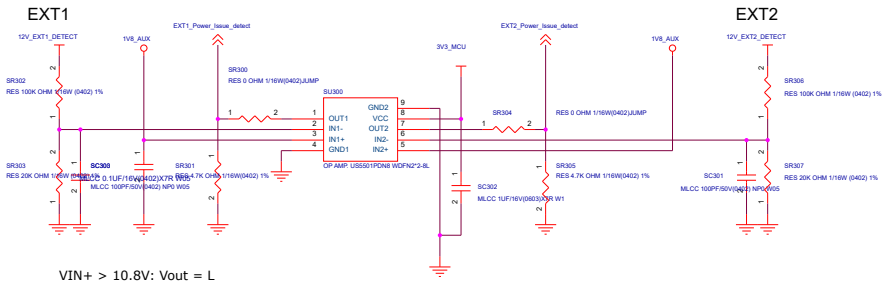
PSU DETECT

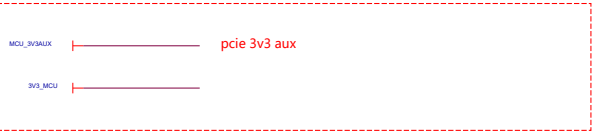


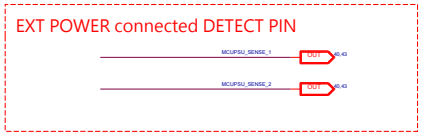
VIN+ > 10.8V: Vout = L

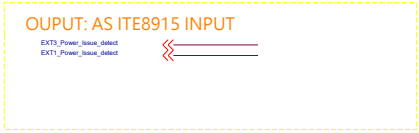
VIN+ < 10.8V: Vout = H

10.8V x 20Kohm / (100Kohm+20Kohm) = 1.8V

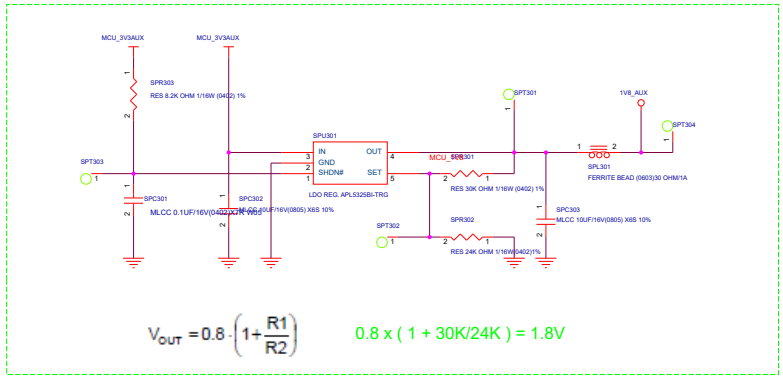
SR301/SR311, 若僅需做一組連接座偵測, 其他零件可以移除, 但SR301/SR310/SR328需上件4.7K





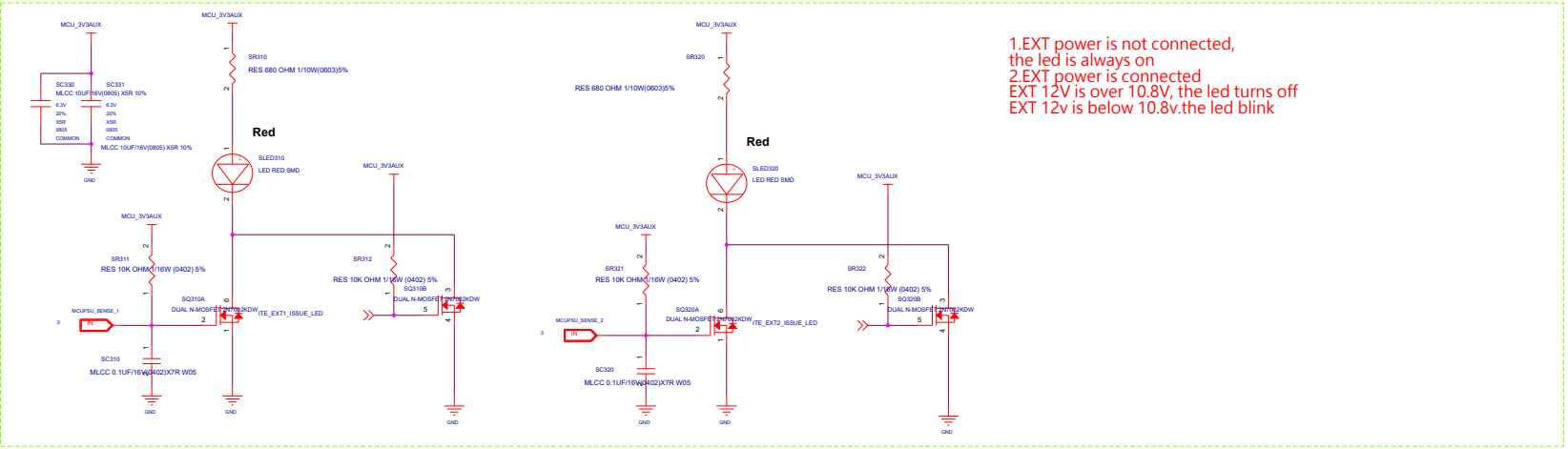


1v8_ref



$$V_{OUT} = 0.8 \cdot \left(1 + \frac{R1}{R2}\right)$$

0.8 x (1 + 30K/24K) = 1.8V



1.EXT power is not connected,
the led is always on
2.EXT power is connected
EXT 12V is over 10.8V, the led turns off
EXT 12v is below 10.8v.the led blink

ASUS	Title :	STRIX003_PSU DETECT
<OrgName>	Engineer:	Sam Hom
Size: C	Project Name: D412BS	Rev: 1.00X
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