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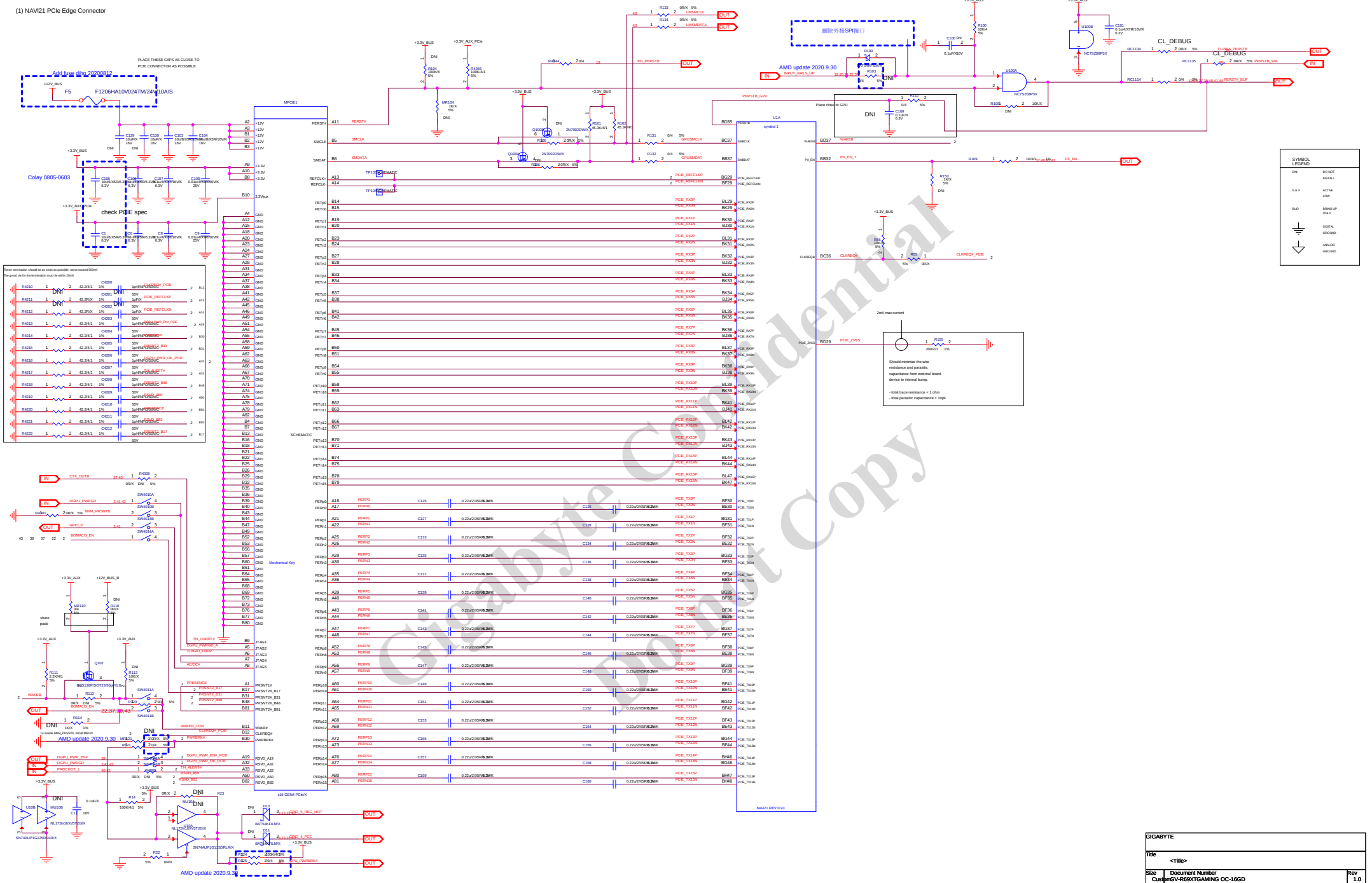
(1) NAVI21 PCIe Edge Connector



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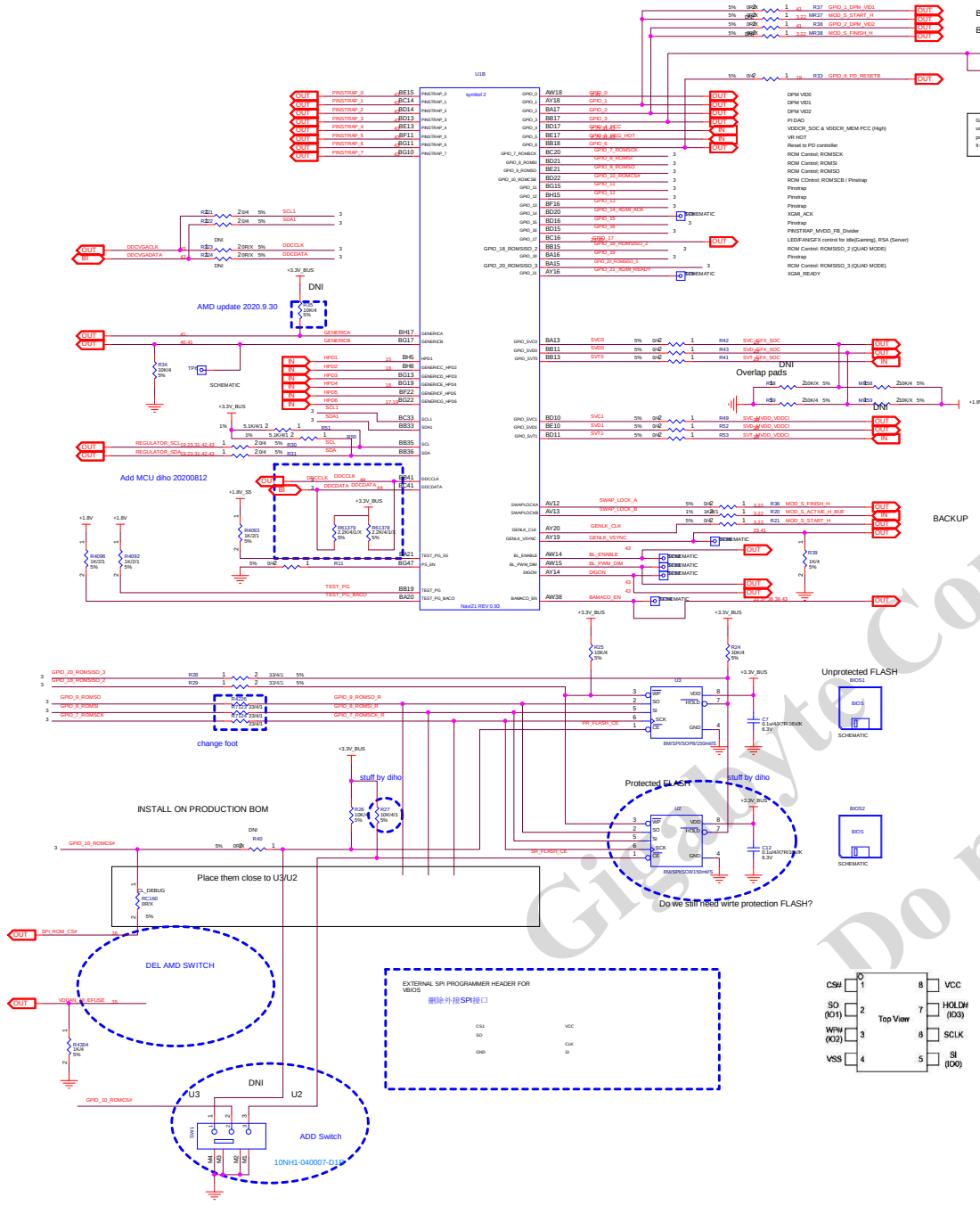

GPIO_0 selected by default for mobile used as ACDC switch indicator or fast power reduction mechanism for desktop. It is programmable through VBIOS.

Note: Internal PU/PD at GPIO pad is strength in 14nm design spec

	User	Internal Default Value	Definition
BIF		0	STRAP_BIF_GEN4_DIS_A 0: PCIe GEN 4 supported 1: PCIe GEN 4 not supported
		0	PINSTRAP_BIF_CLK_PM_EN 0: CLKREQ# power management capability is disabled 1: CLKREQ# power management capability is enabled
		0	PINSTRAP_BIF_LC_TX_SWING
		0	PINSTRAP_BIF_VGA_DIS 0: VGA controller capacity enabled 1: The device won't be recognised as the system's VGA controller
DCE		0 0 0	PINSTRAP_AUD_PORT_CONN[2:0] Number of audio-capable display outputs 0: All endpoints connected 1: 6 endpoints connected 2: 5 endpoints connected 3: 4 endpoints connected 4: 3 endpoints connected 5: 2 endpoints connected 6: 1 endpoint connected 7: 0 endpoints connected
		0 0	PINSTRAP_AUD[1:0] 1: Audio for DisplayPort only 2: Audio for DisplayPort and HDMI if dongle is detected 3: Audio for DisplayPort and native HDMI
Platform		0 0	PINSTRAP_BOARD_CONFIG[2:0] TBD PINSTRAP_MVDD_BOOT_VID_CONFIG 0: Ratio=1 without feedback divider 1: Ratio=1 with feedback divider installed
SMU		1 0 1	PINSTRAP_ROM_CONFIG[2:0] 101
		0	PINSTRAP_SMBUS_ADDR 0: 0x42h 1: 0x40h
		1	PINSTRAP_BIOS_ROM_EN 0: Disable the external BIOS ROM device 1: Enable the external BIOS ROM device

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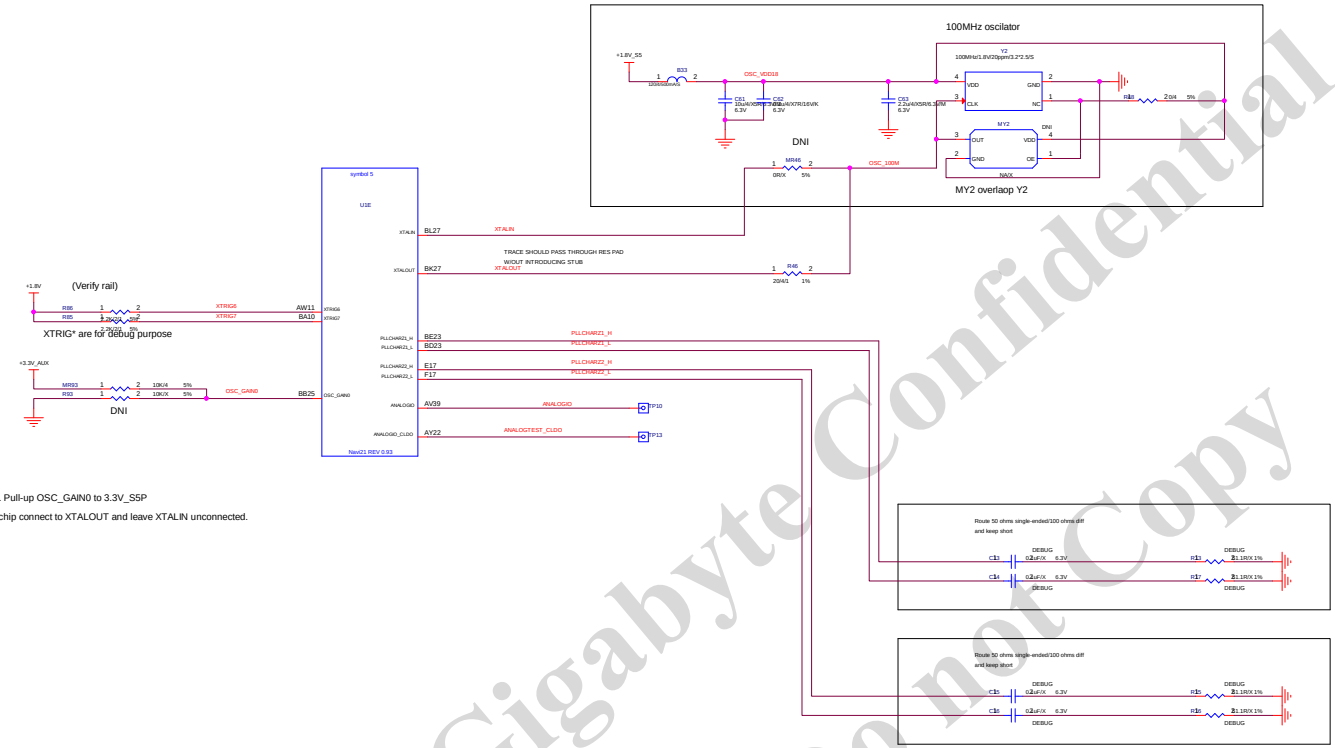

Default OSC_GAIN is 0x7. Pull-up OSC_GAIN0 to 3.3V_S5P

When 0x7, external clock chip connect to XTALOUT and leave XTALIN unconnected.

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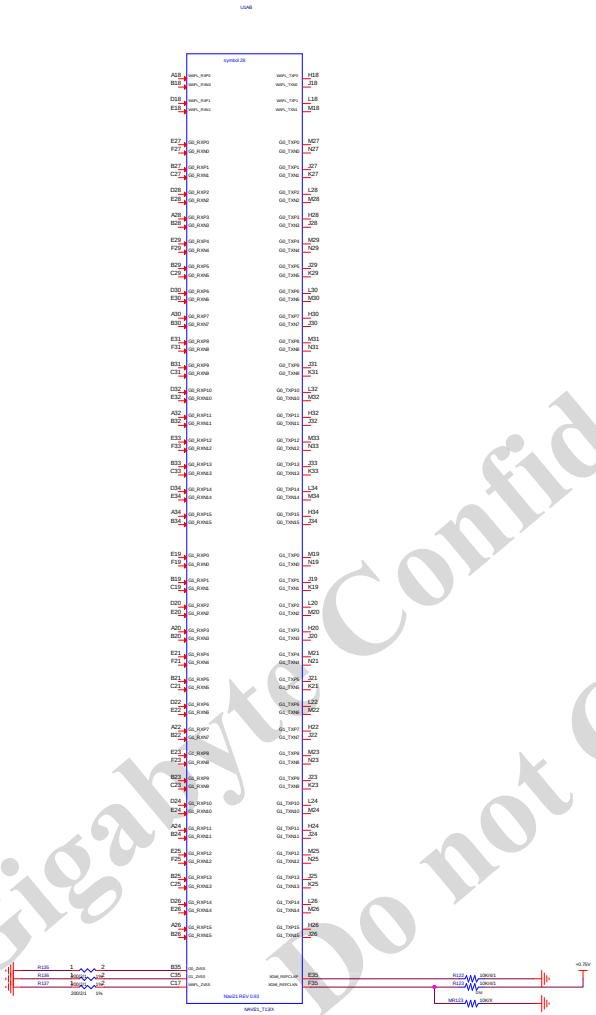
Navi21 XGMI LINK 0 & 1



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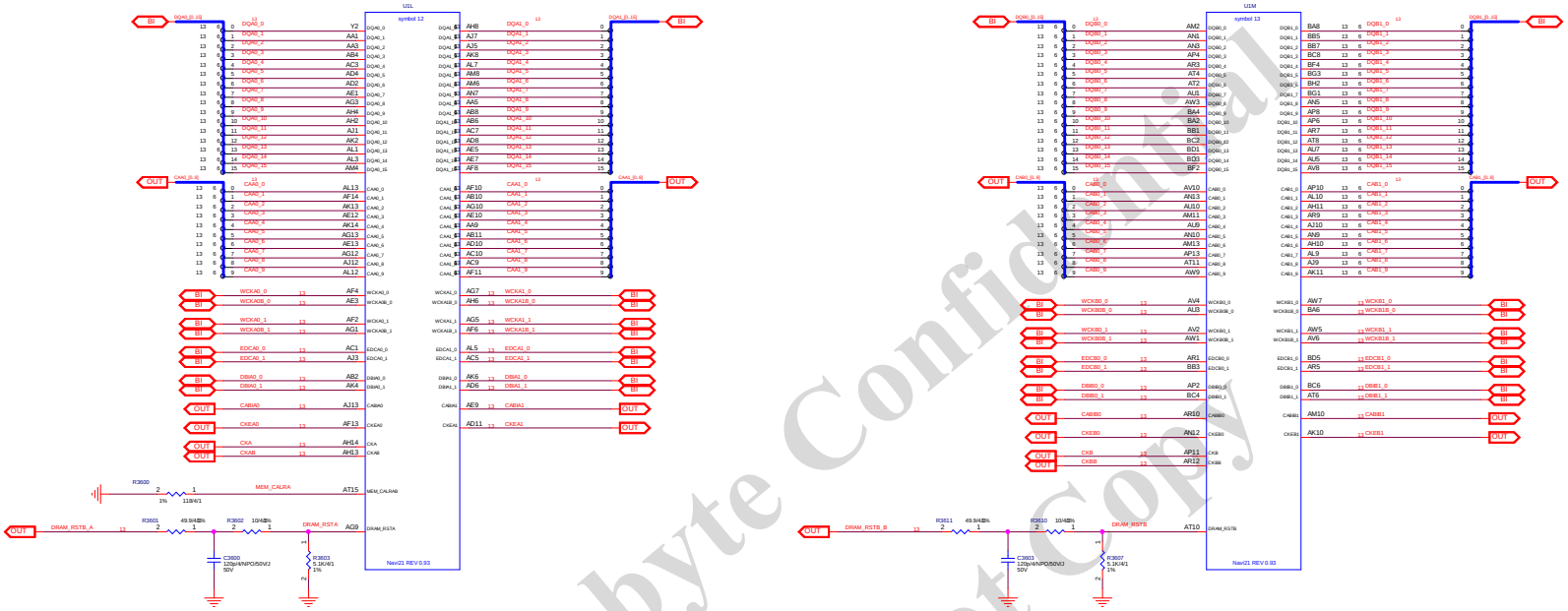
(1) NAVI 10 MEM INTERFACE CH A/B



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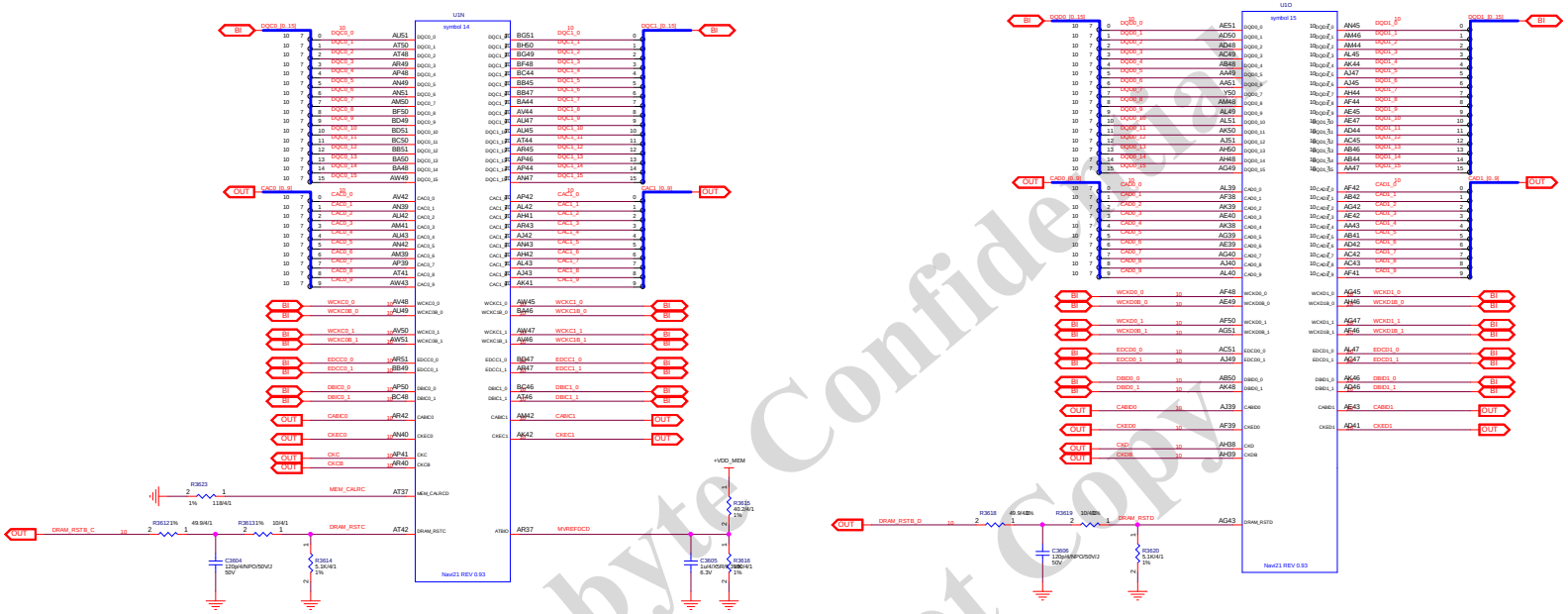
(2) NAVI 10 MEM INTERFACE CH C/D



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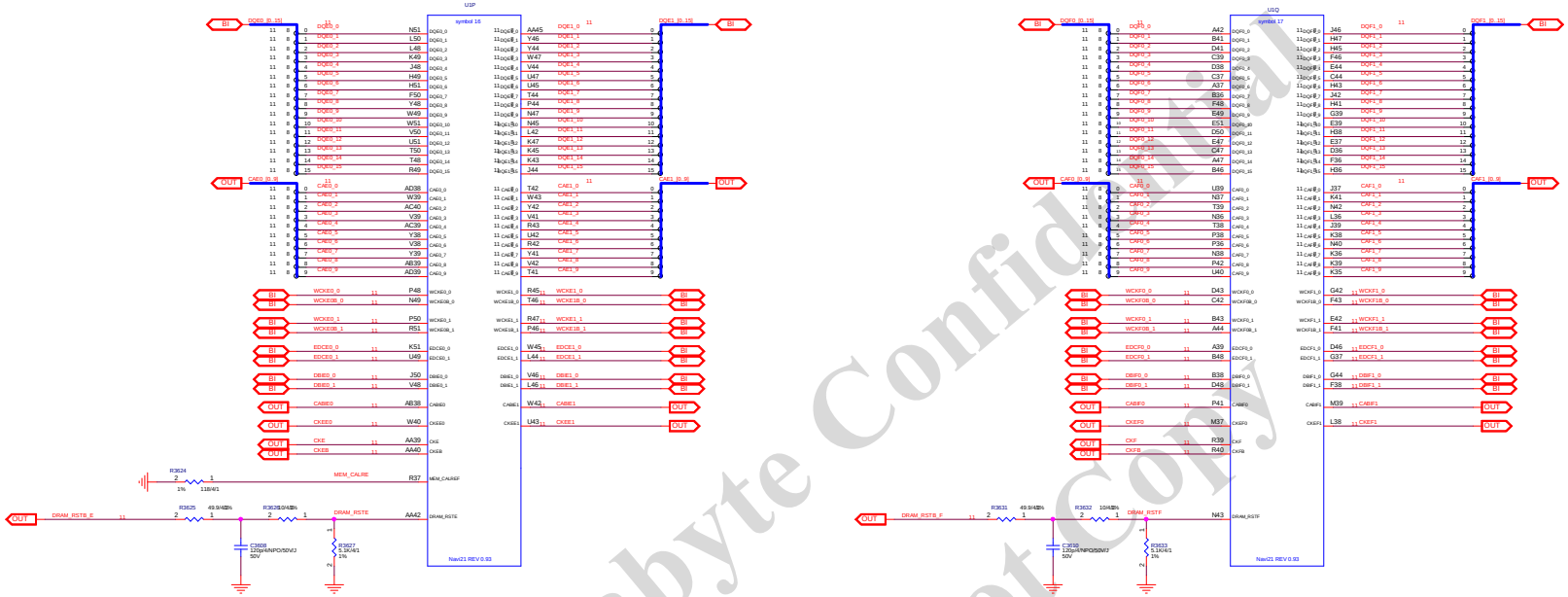
(3) NAVI 10 MEM INTERFACE CH E/F



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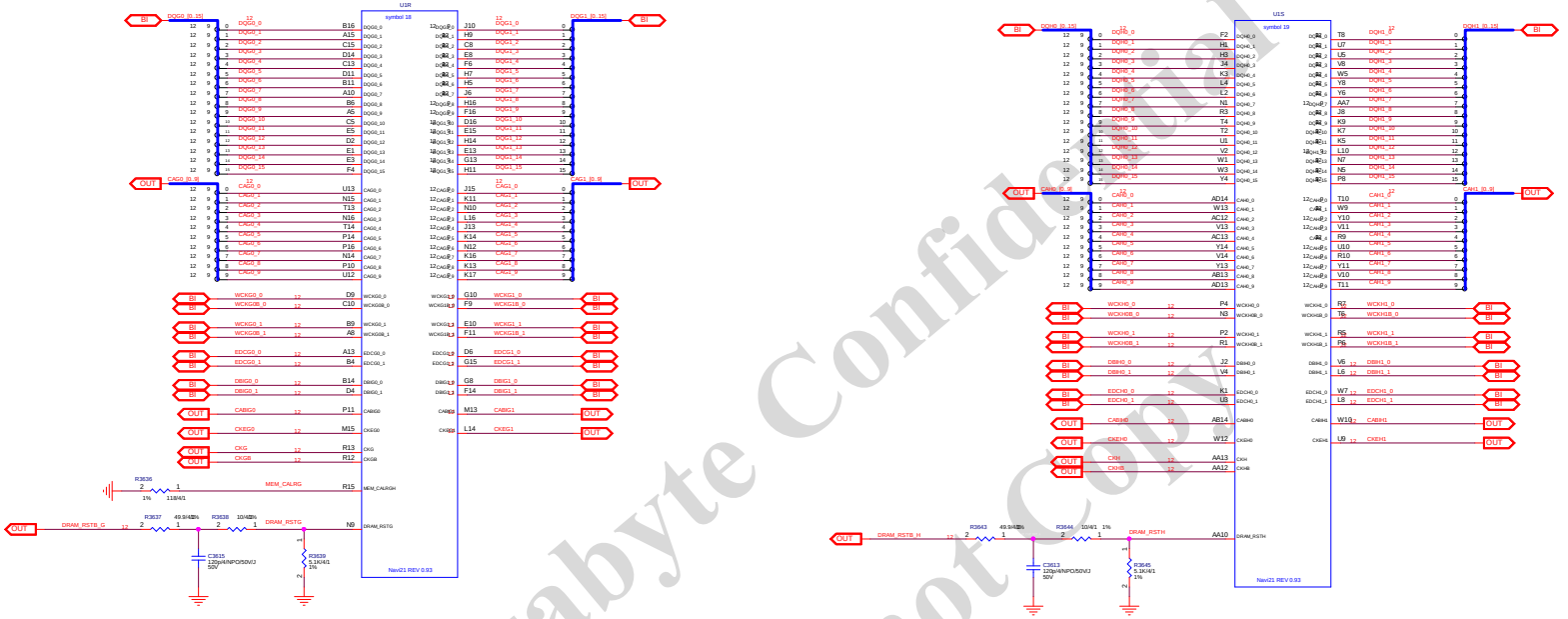
(4) NAVI 10 MEM INTERFACE CH G/H



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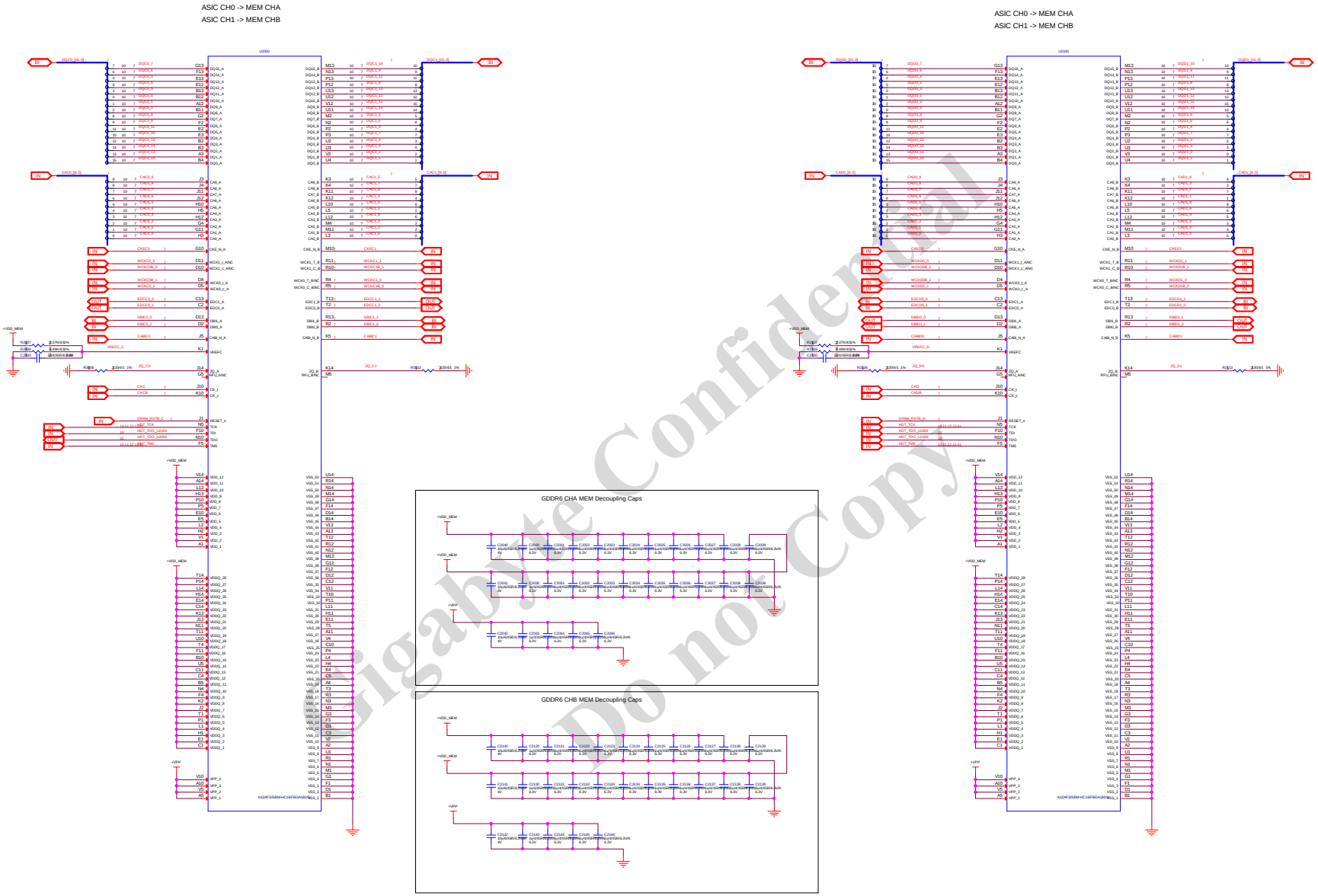
GDDR6x16 CHAB Memory



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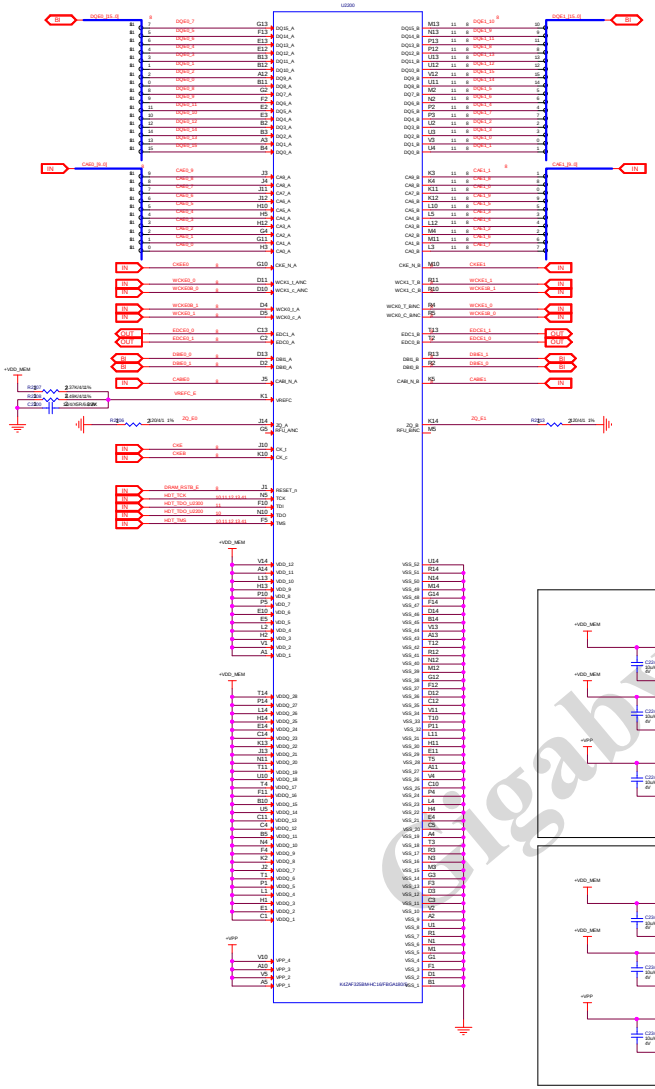
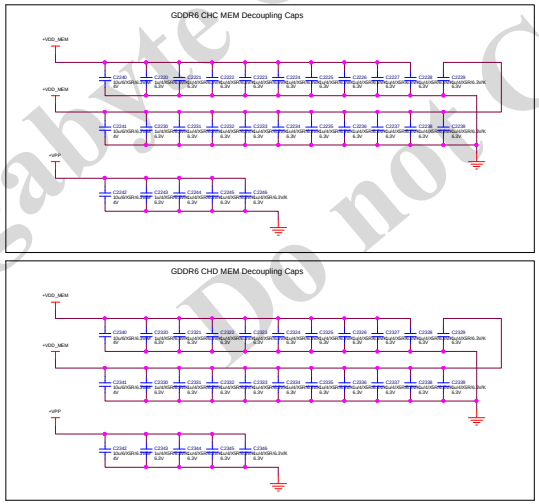
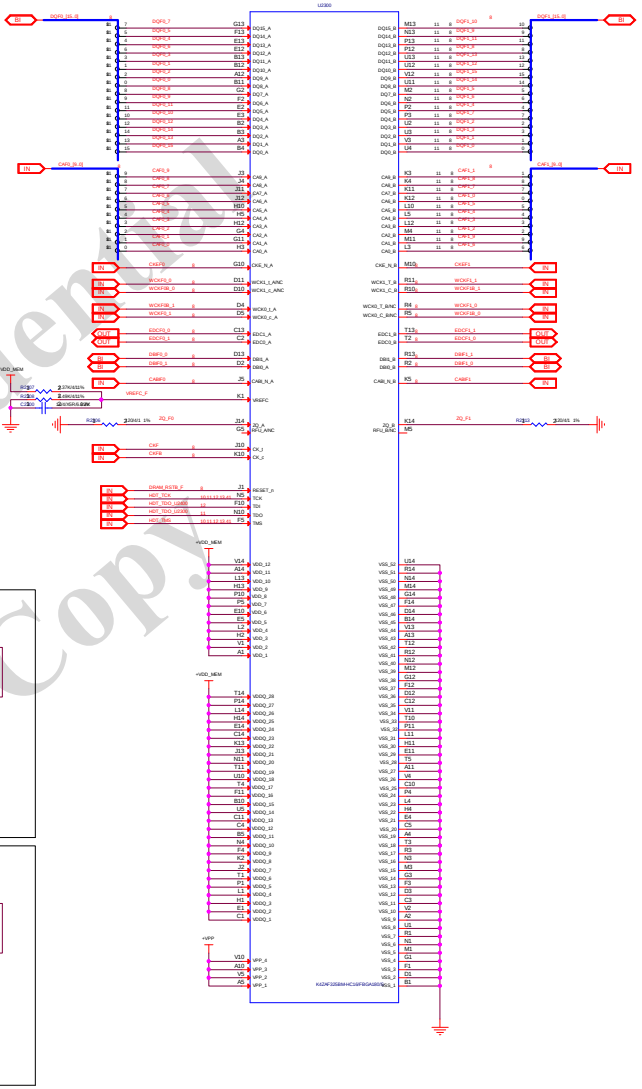
ASIC CH0 -> MEM CHA
ASIC CH1 -> MEM CHB





ASIC CH0 -> MEM CHA
ASIC CH1 -> MEM CHB



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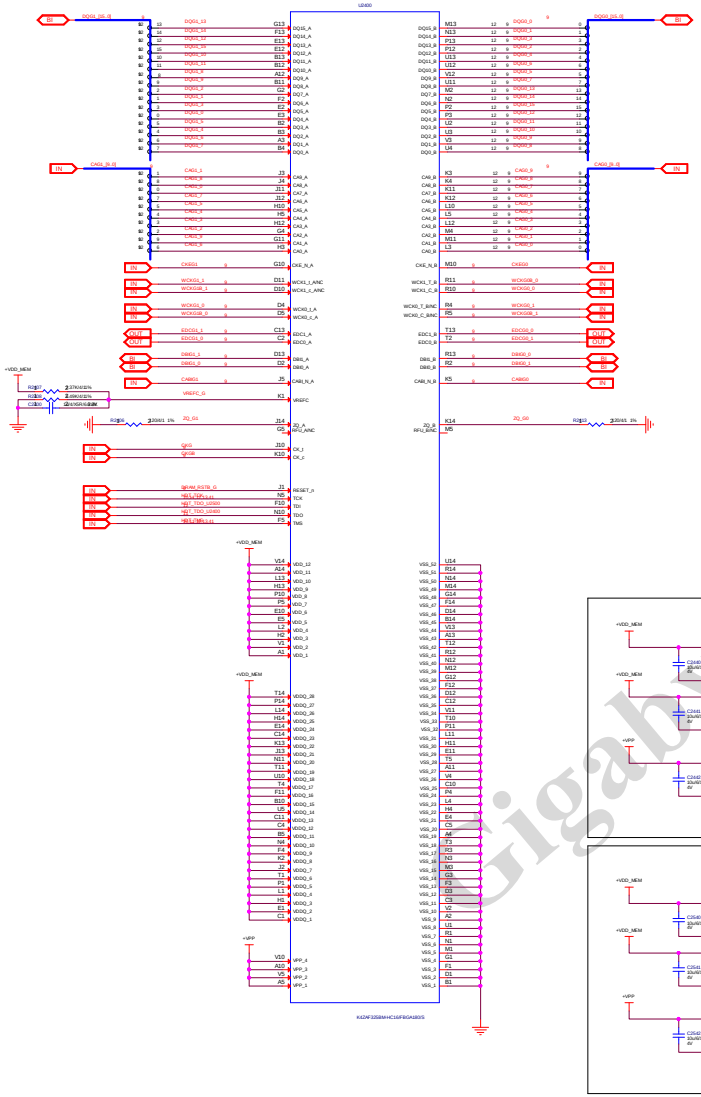
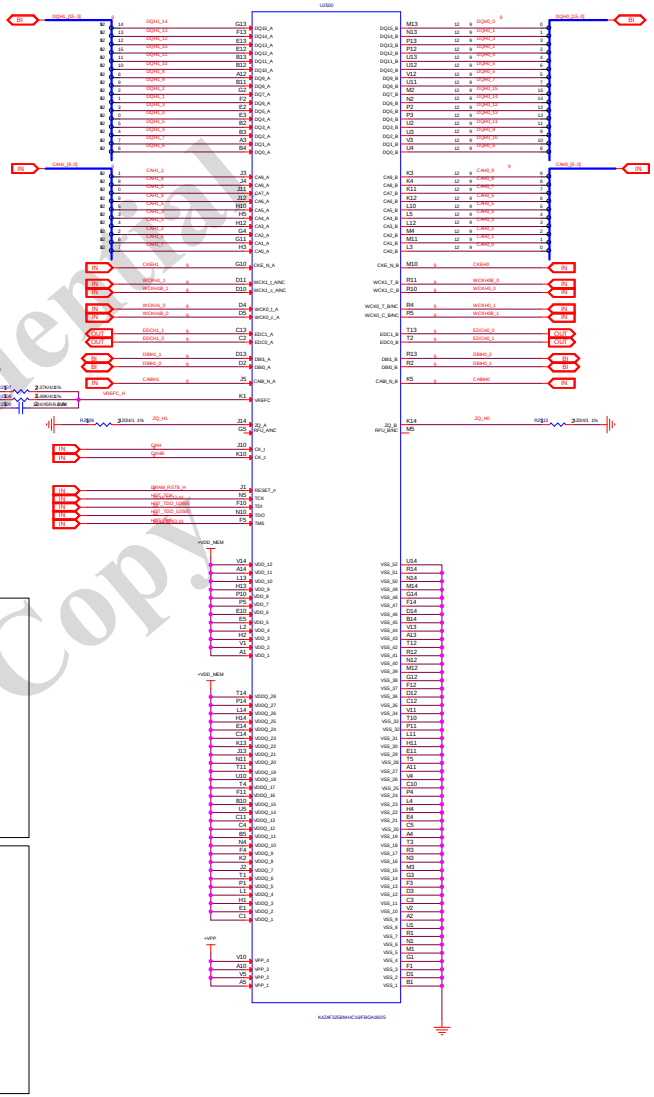
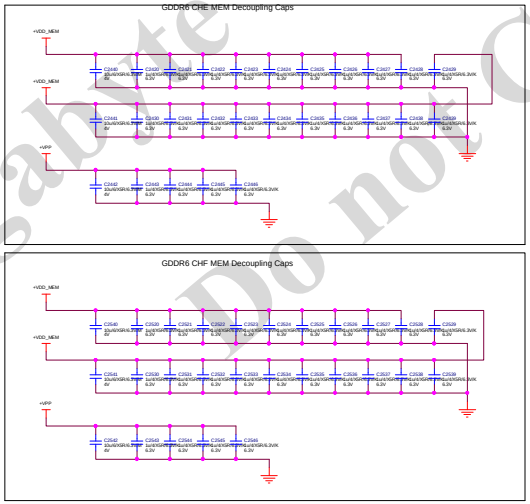
ASIC CH0 -> MEM CHB
ASIC CH1 -> MEM CHA



ASIC CH0 -> MEM CHB
ASIC CH1 -> MEM CHA





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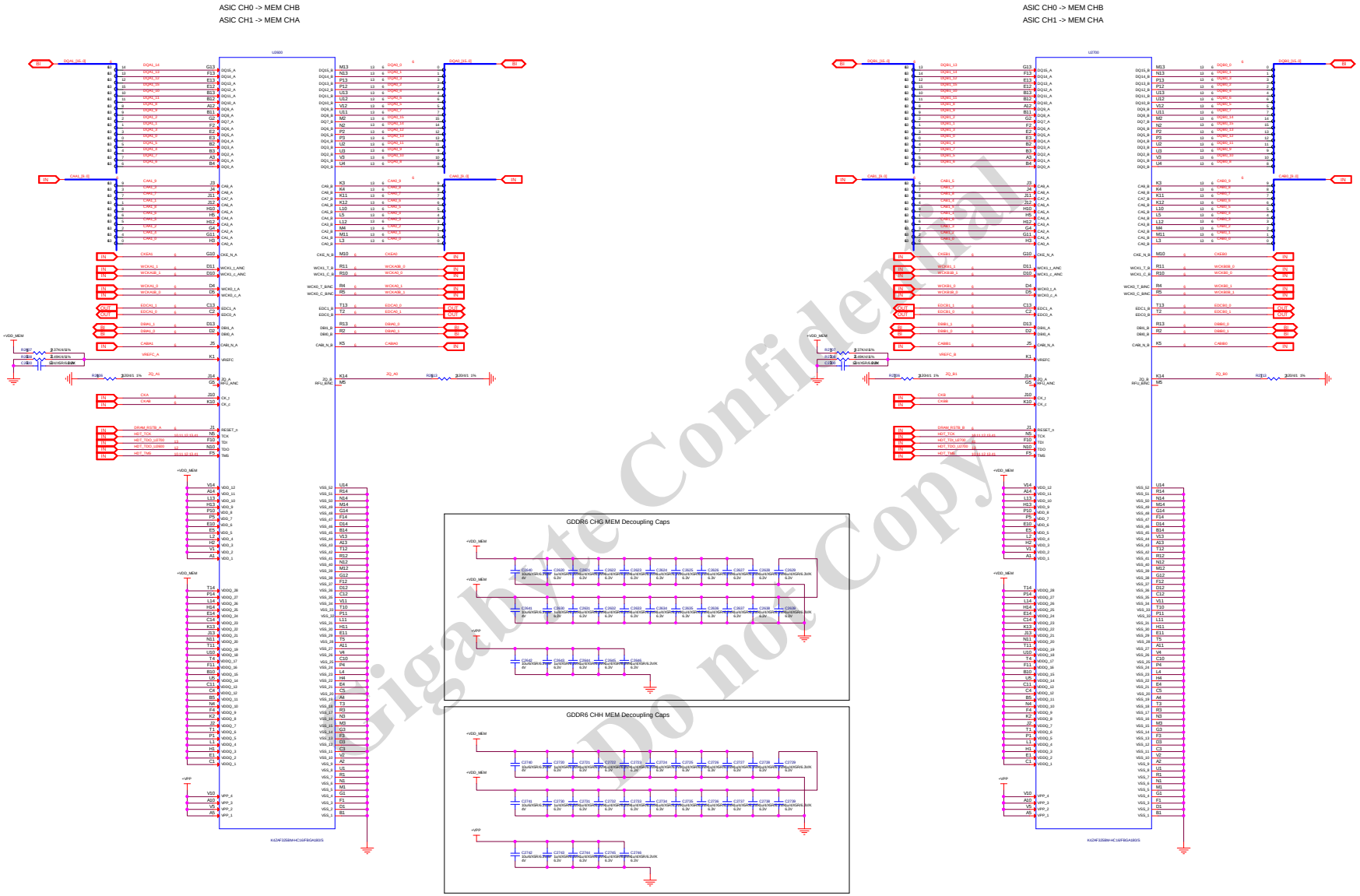
GDDR6x16 CHGH Memory



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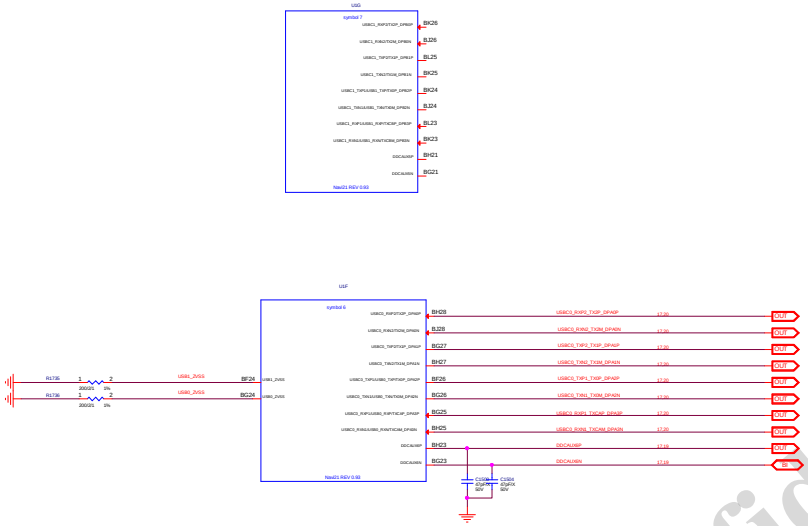
NAVI21 TMDP A/B



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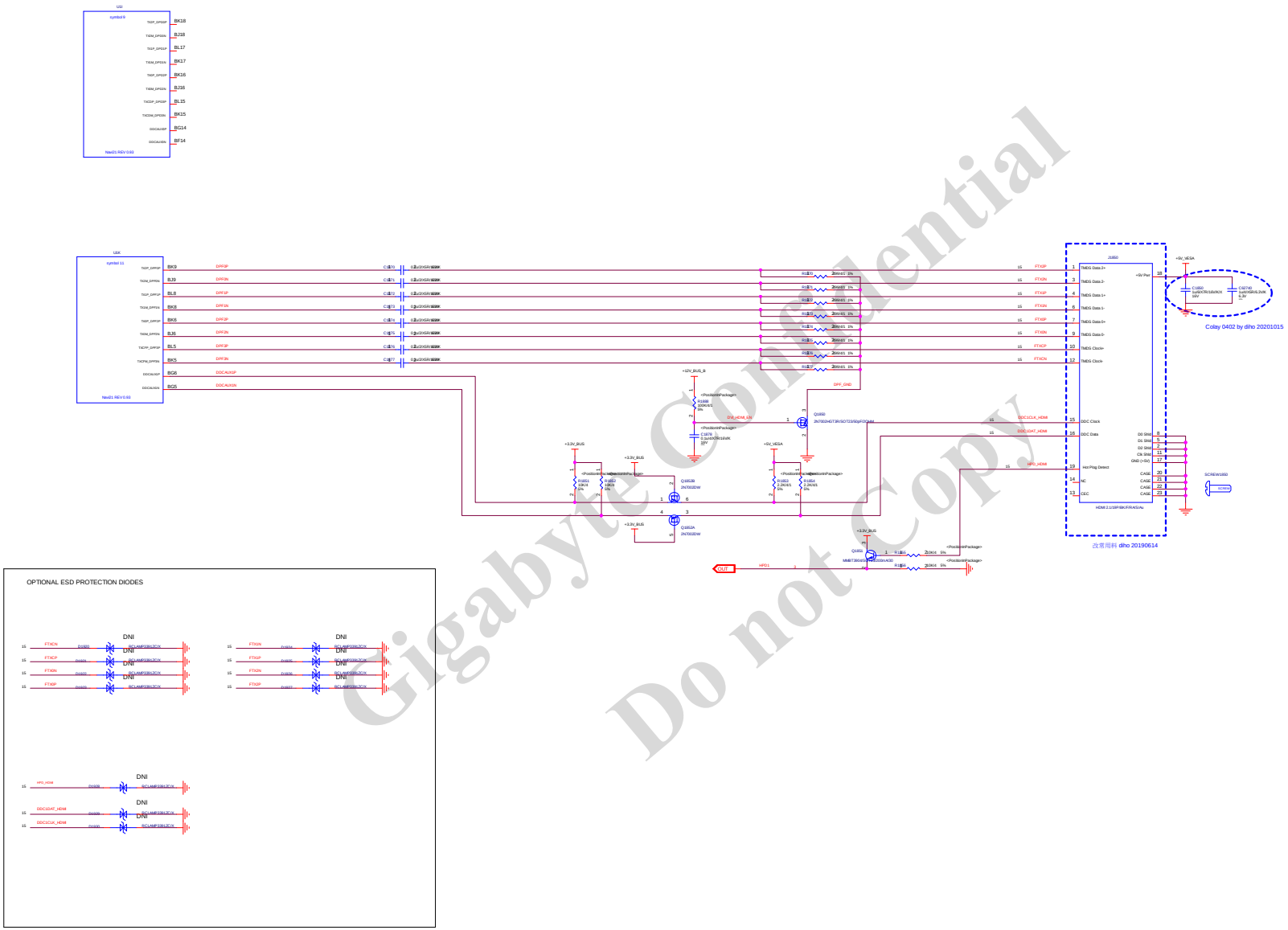

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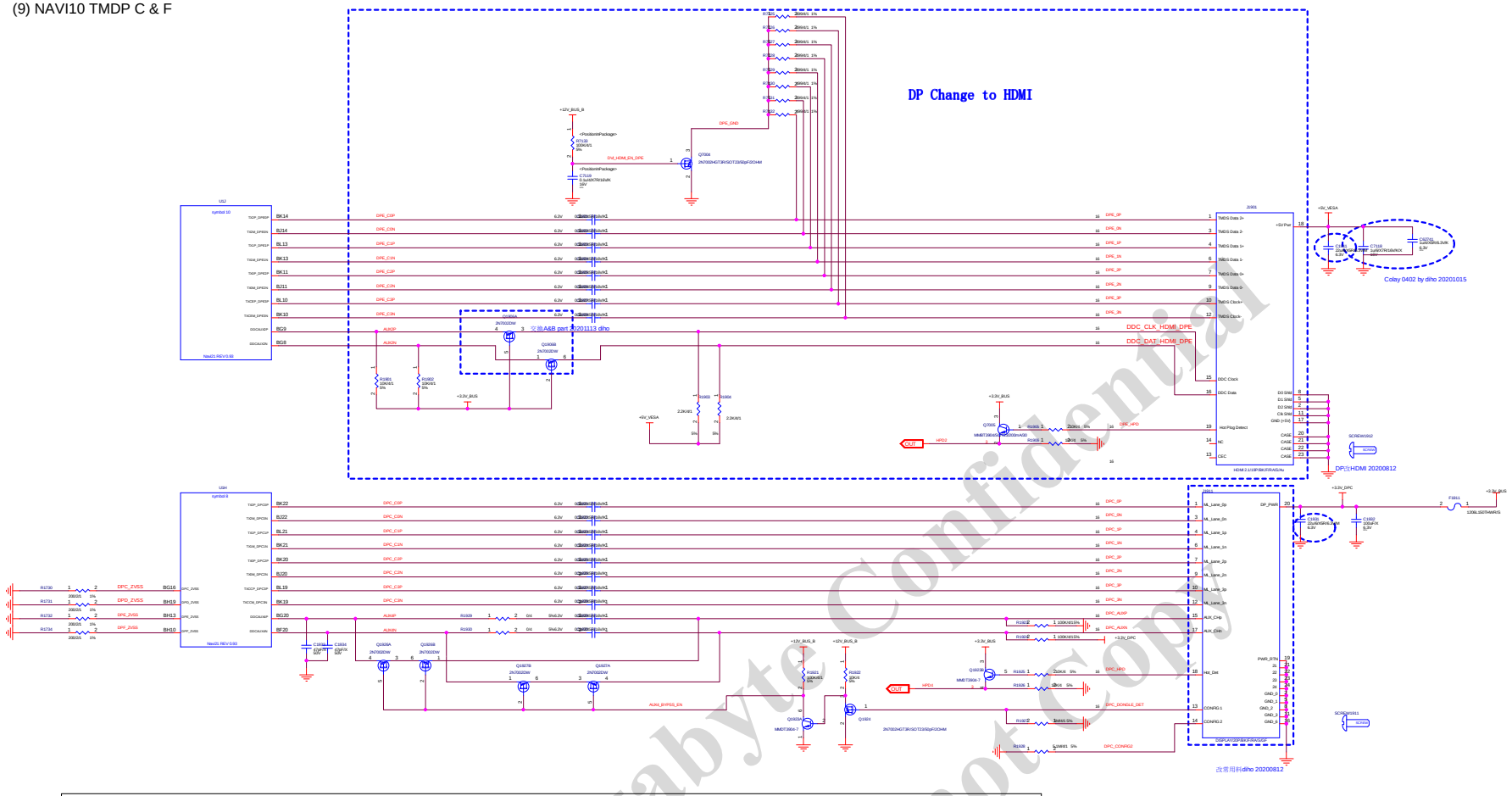
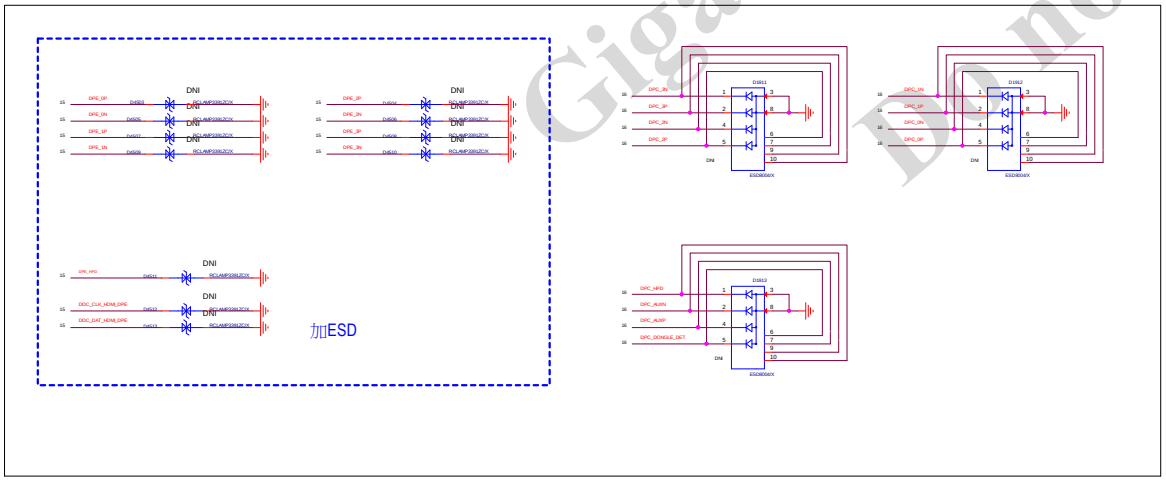
(9) NAVI10 TMDP C & F





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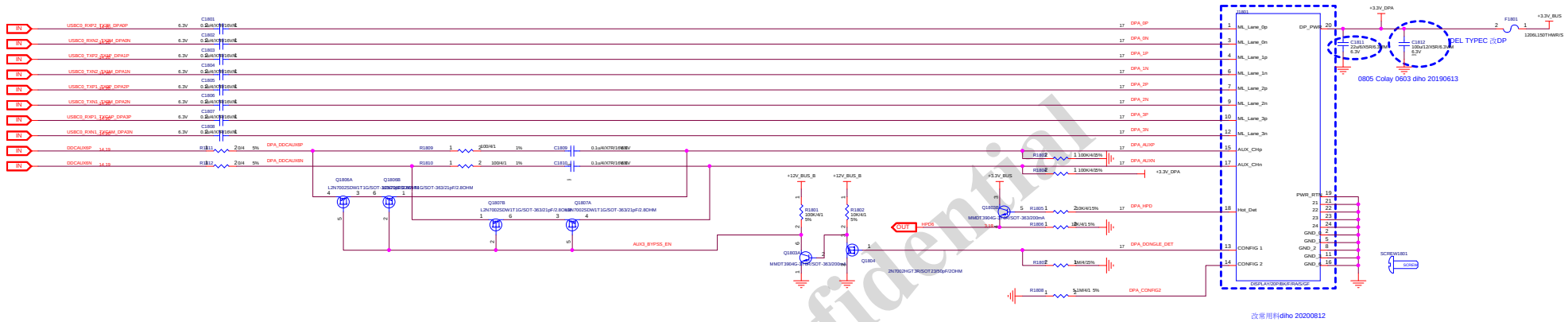

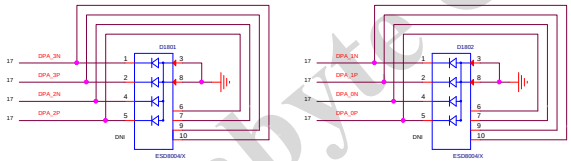

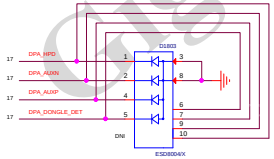

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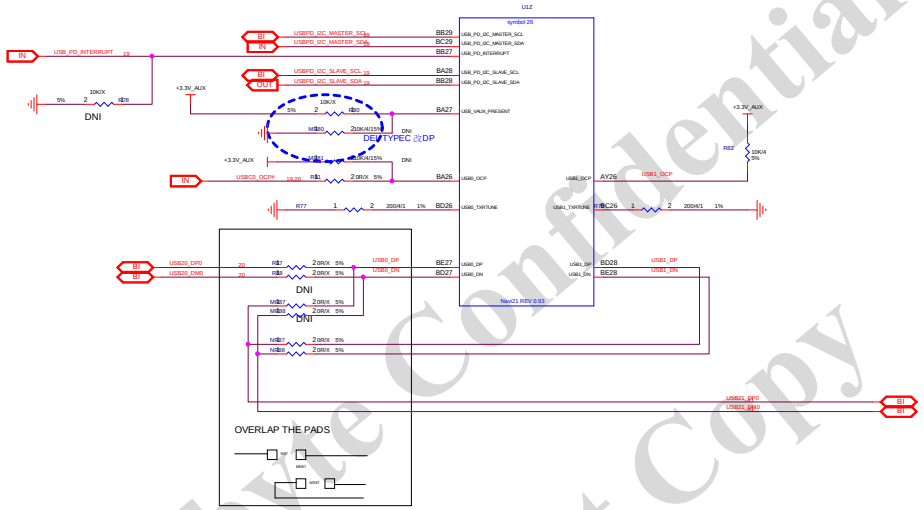

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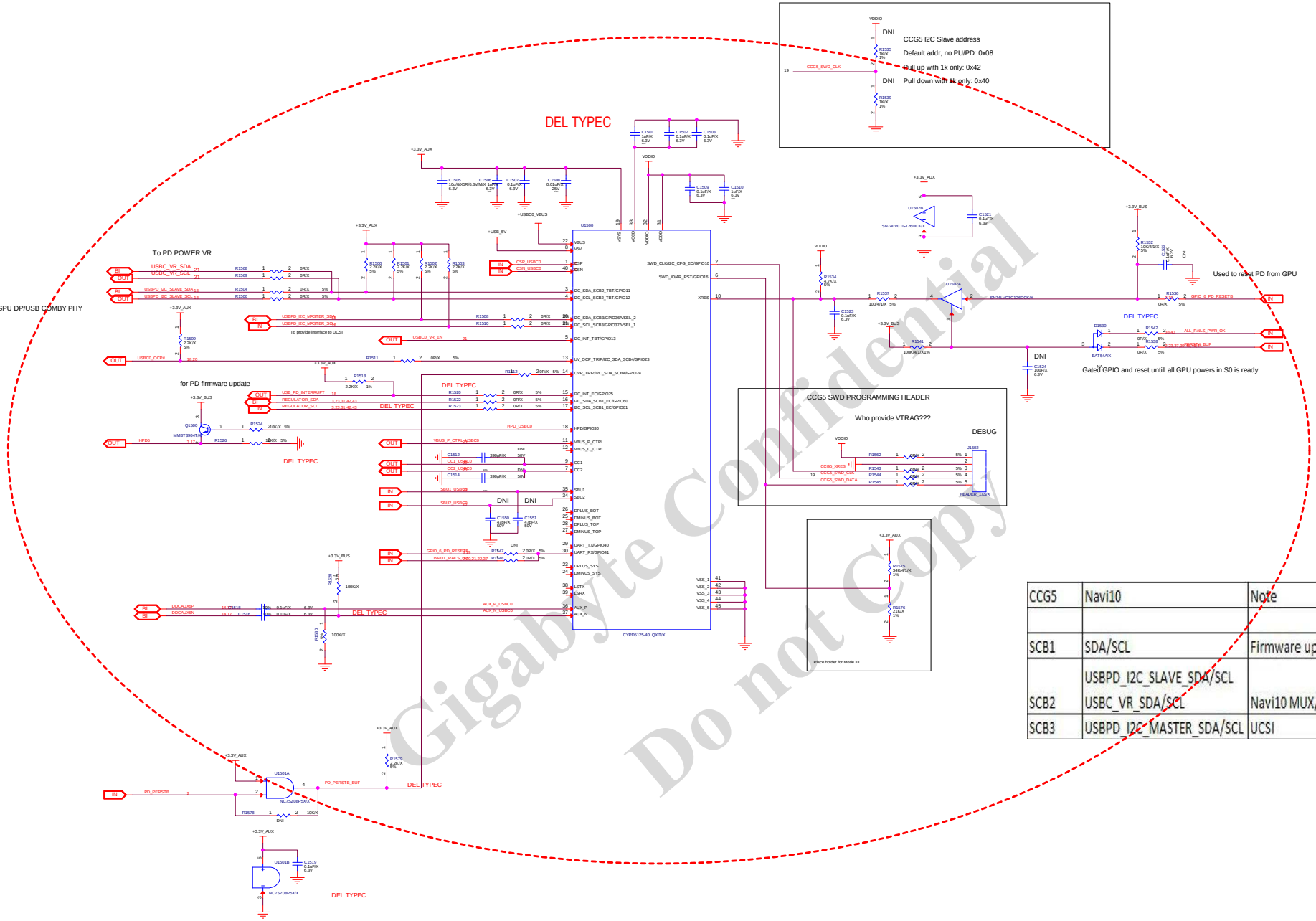

CCG5	Navi10	Note
SCB1	SDA/SCL	Firmware update/SMU
SCB2	USBPD_I2C_SLAVE_SDA/SCL USBC_VR_SDA/SCL	Navi10 MUX/PD_Regulator/re-driver
SCB3	USBPD_I2C_MASTER_SDA/SCL	UCSI

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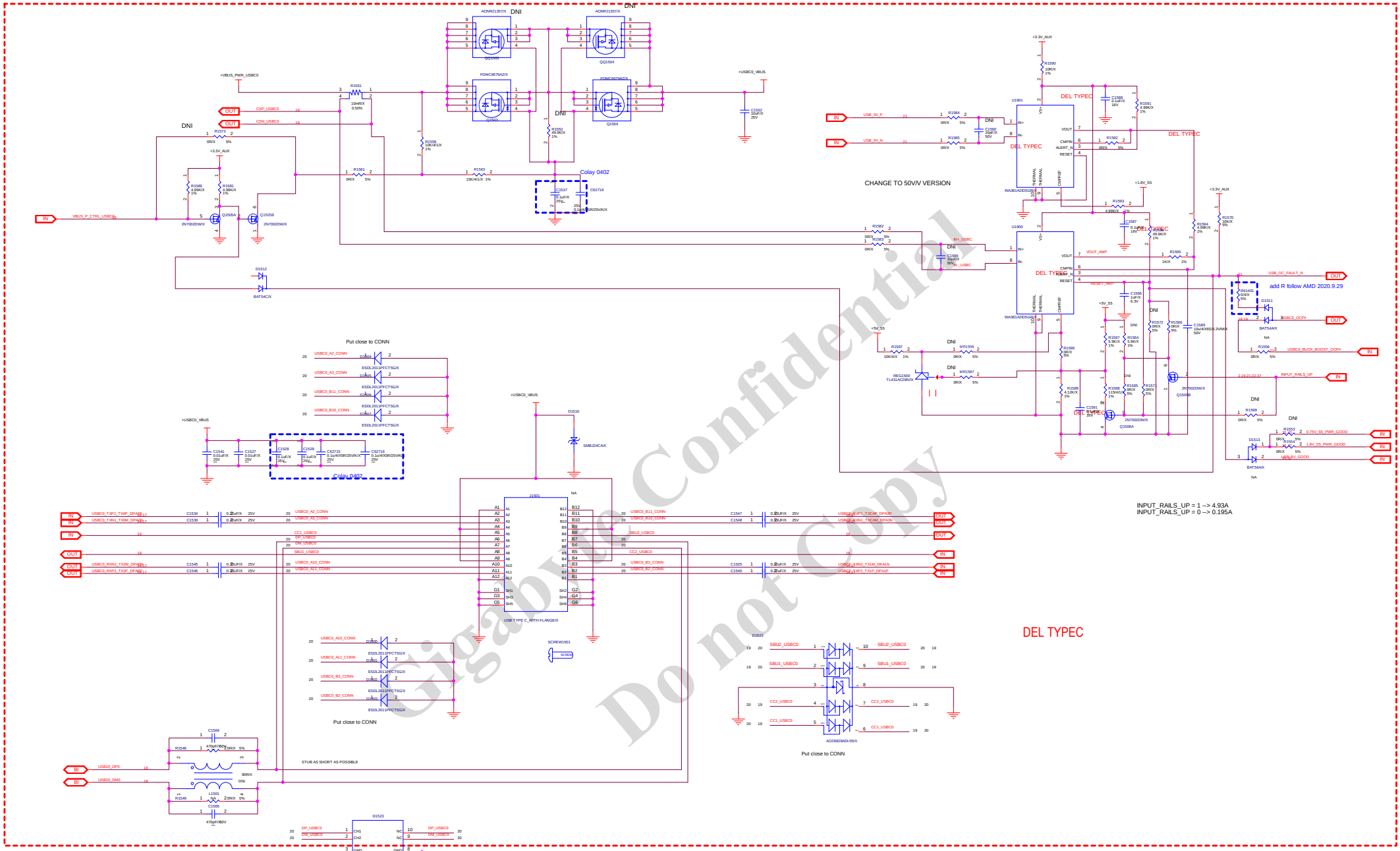

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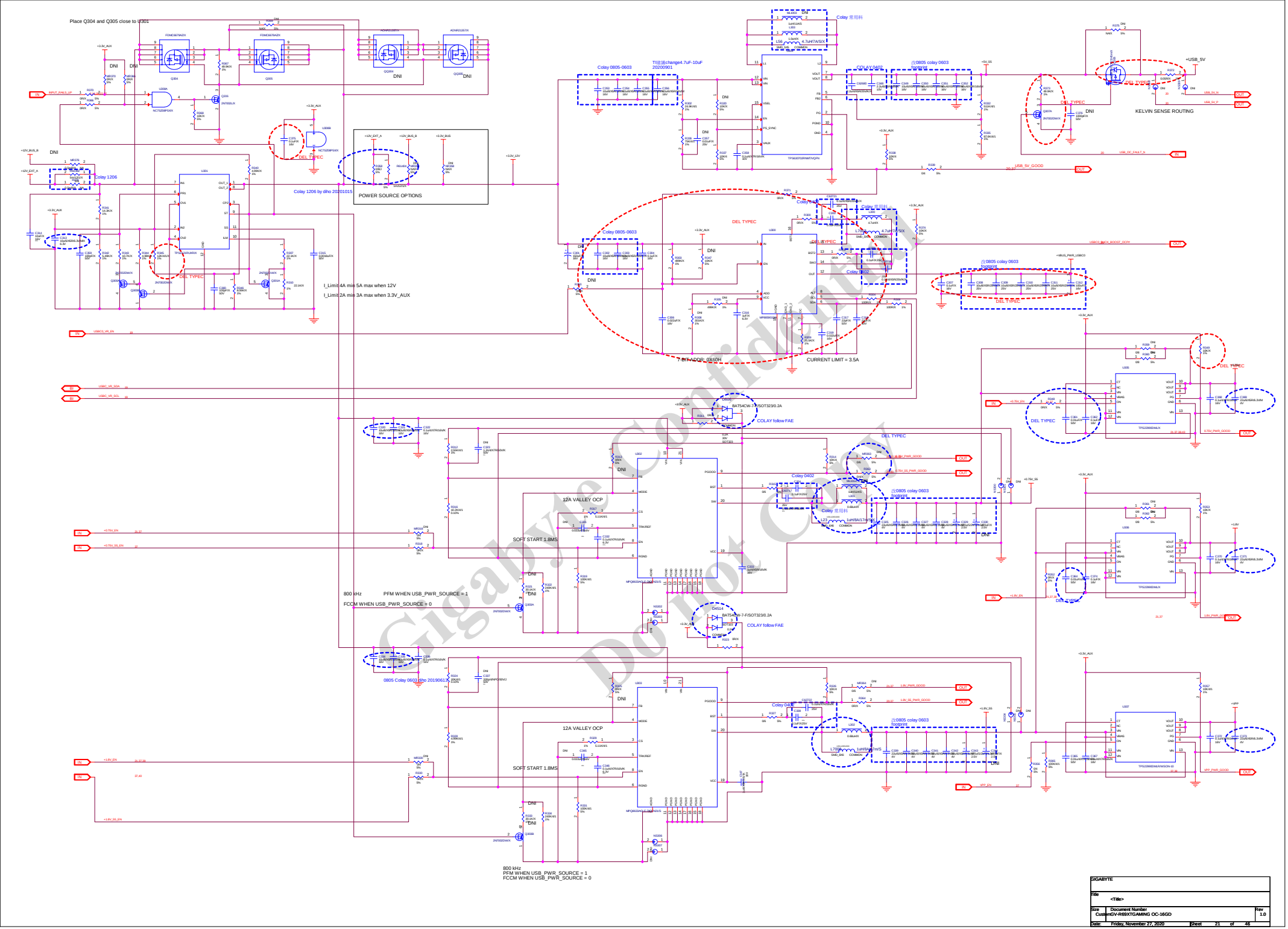

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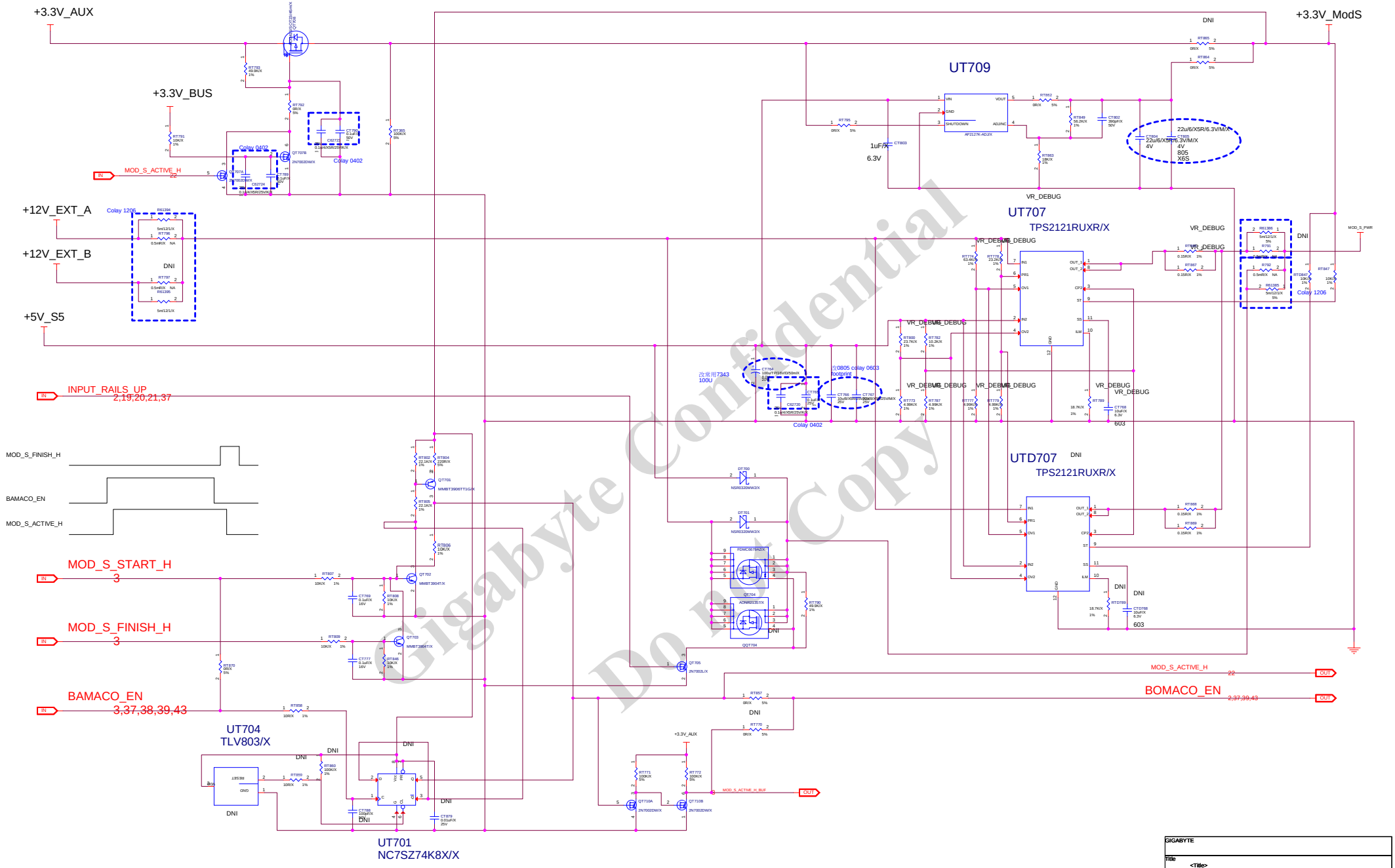

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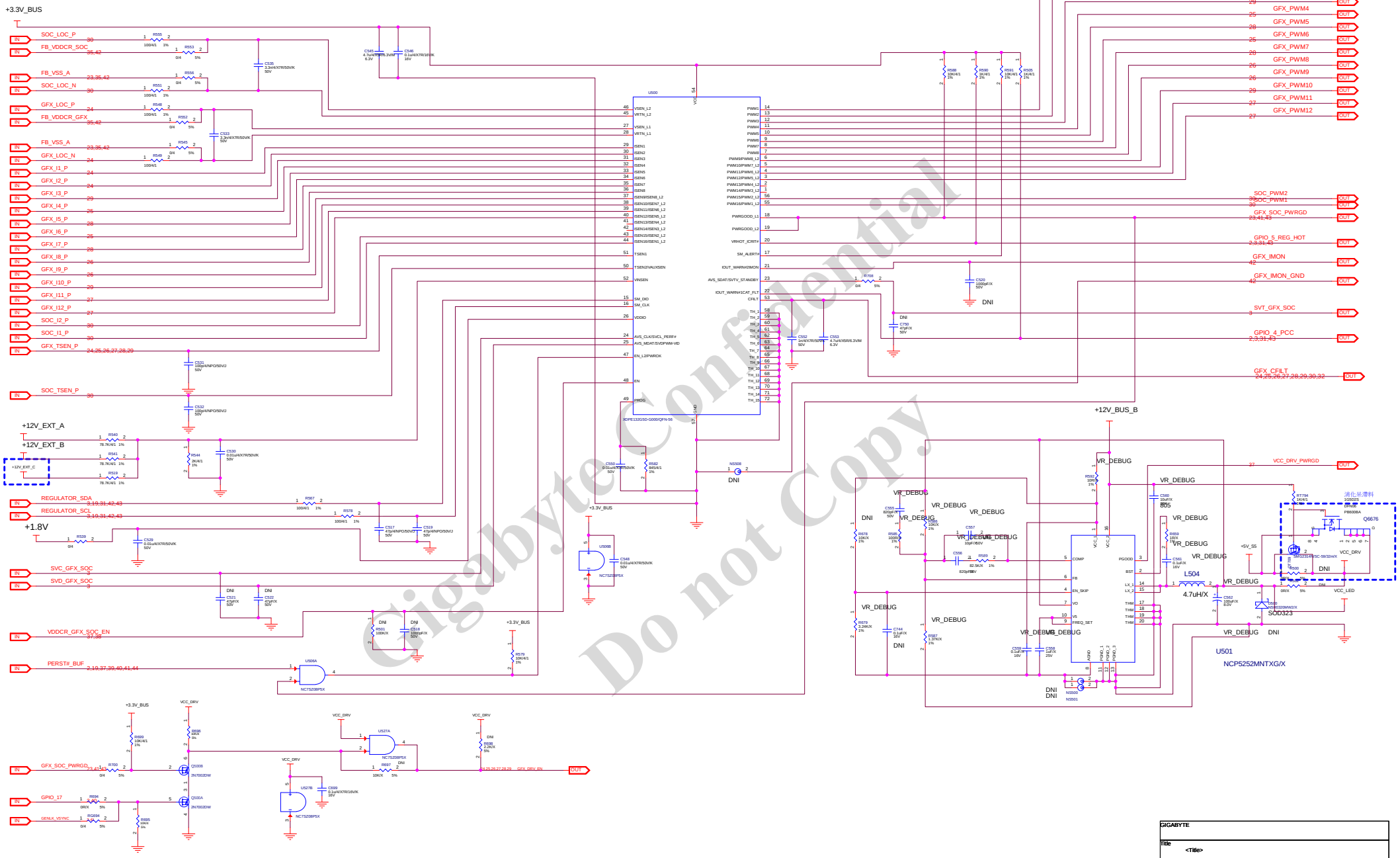
(14) GFX & SOC CONTROLLER



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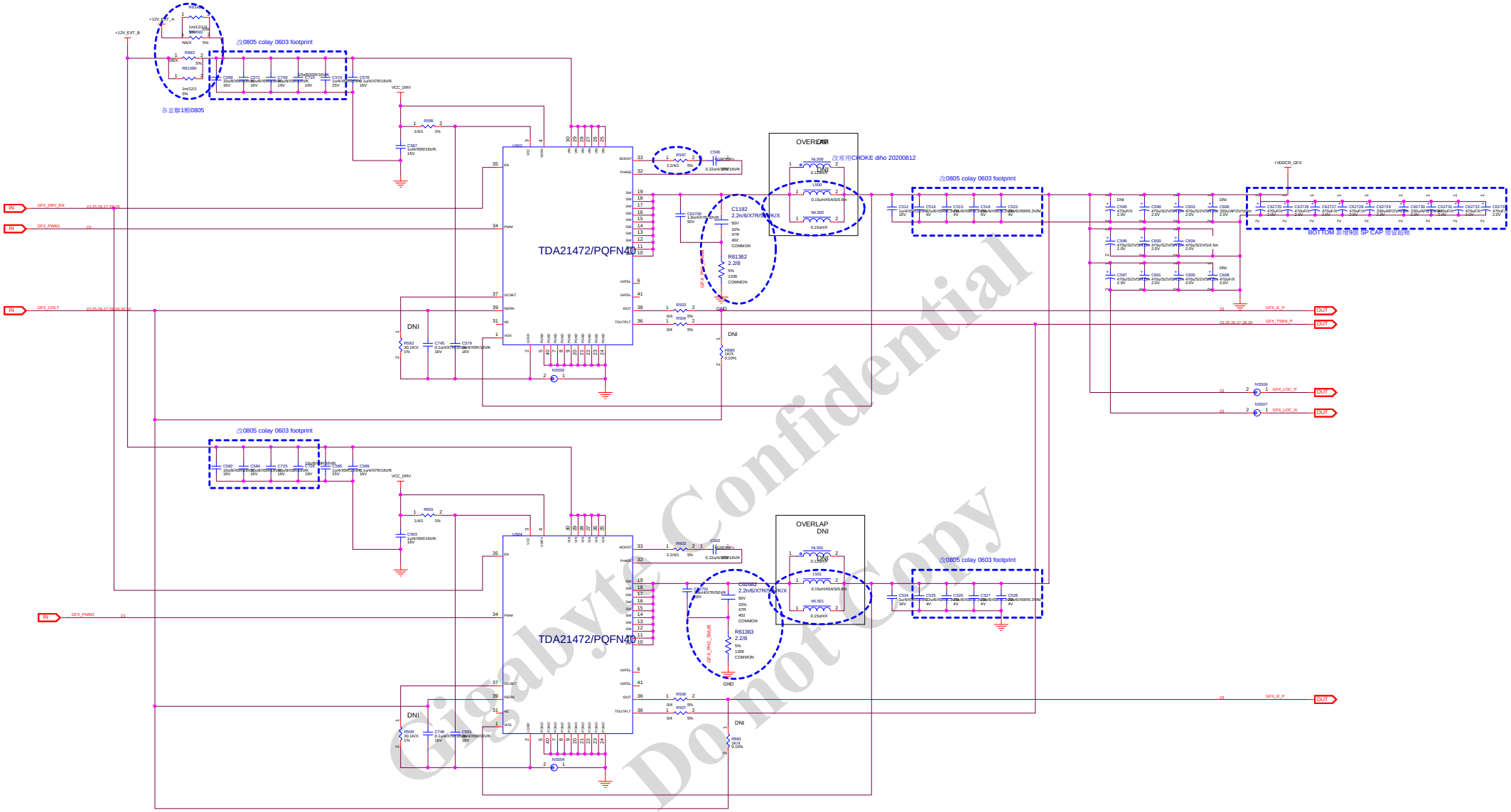

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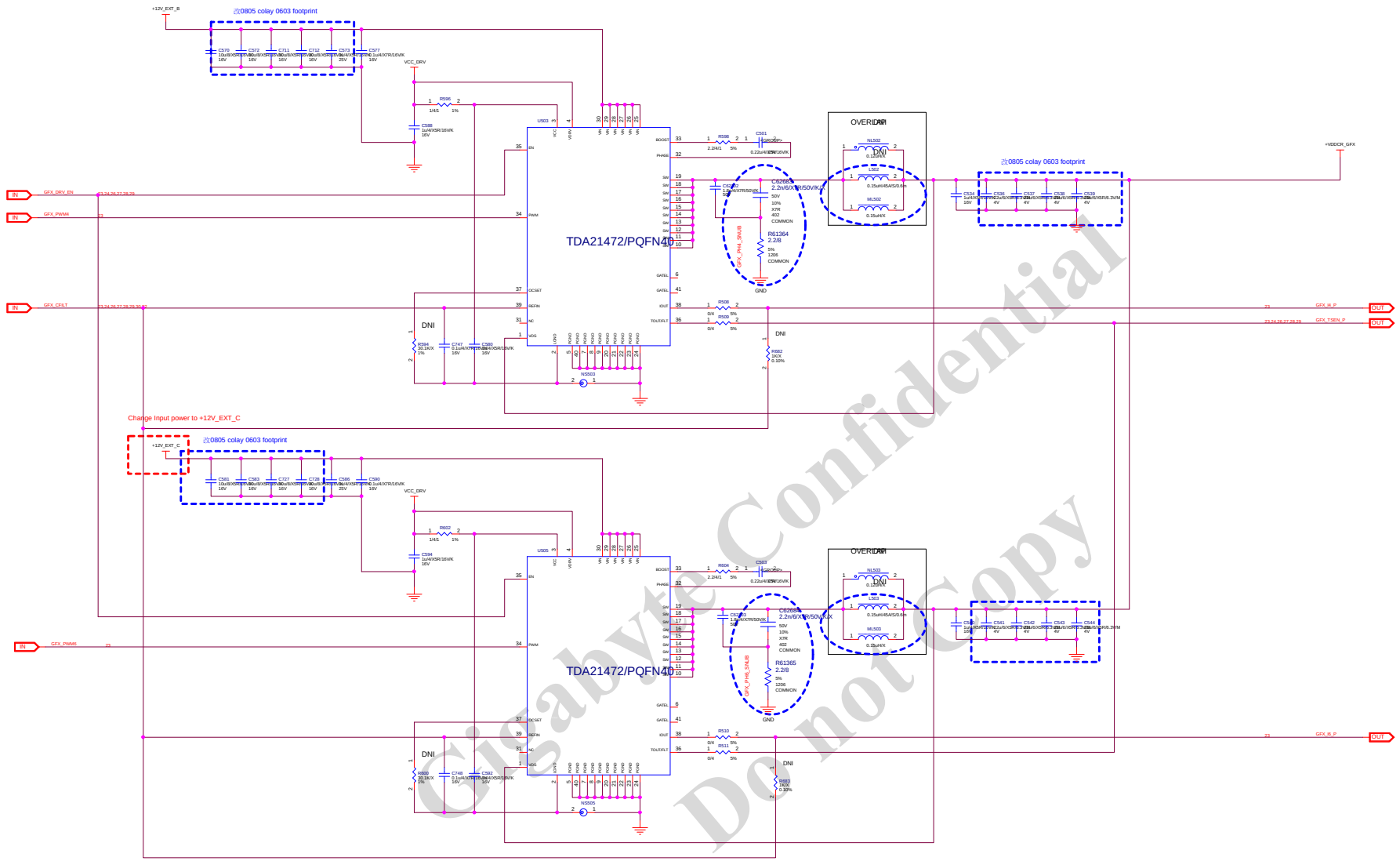

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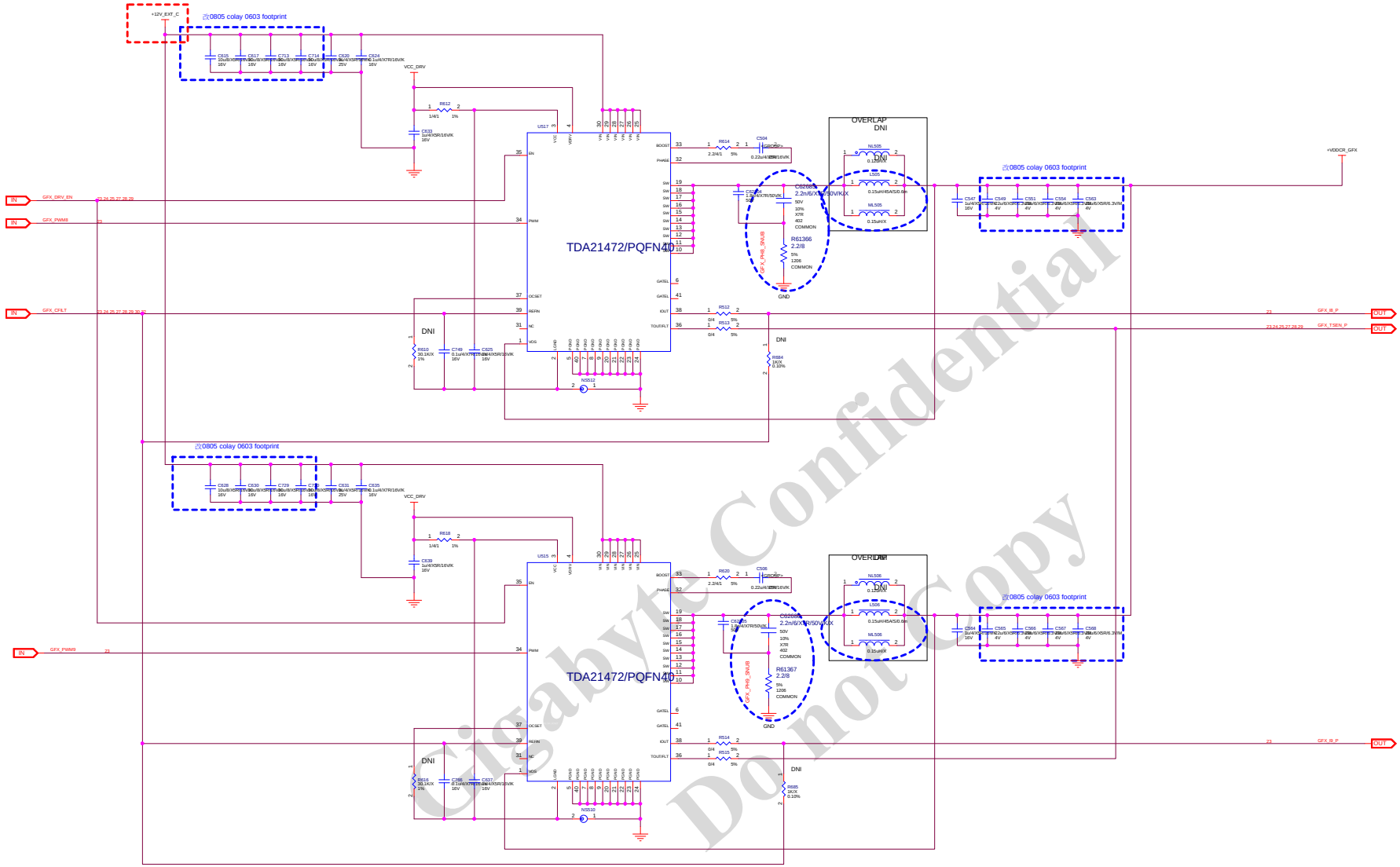
Change Input power to +12V_EXT_C



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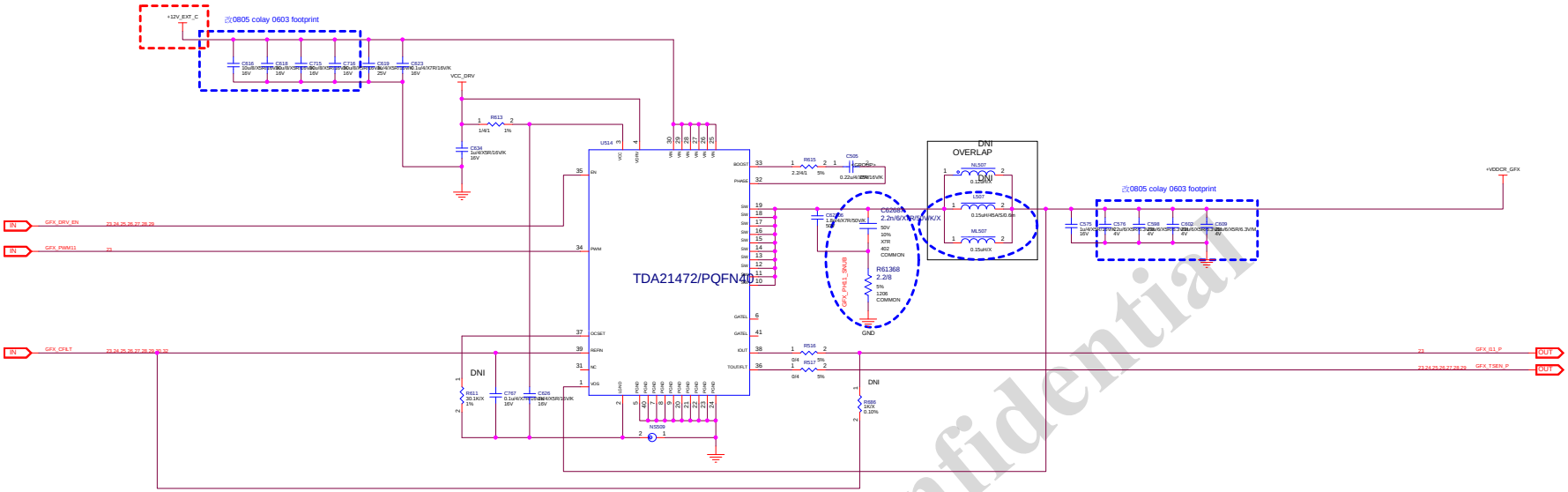
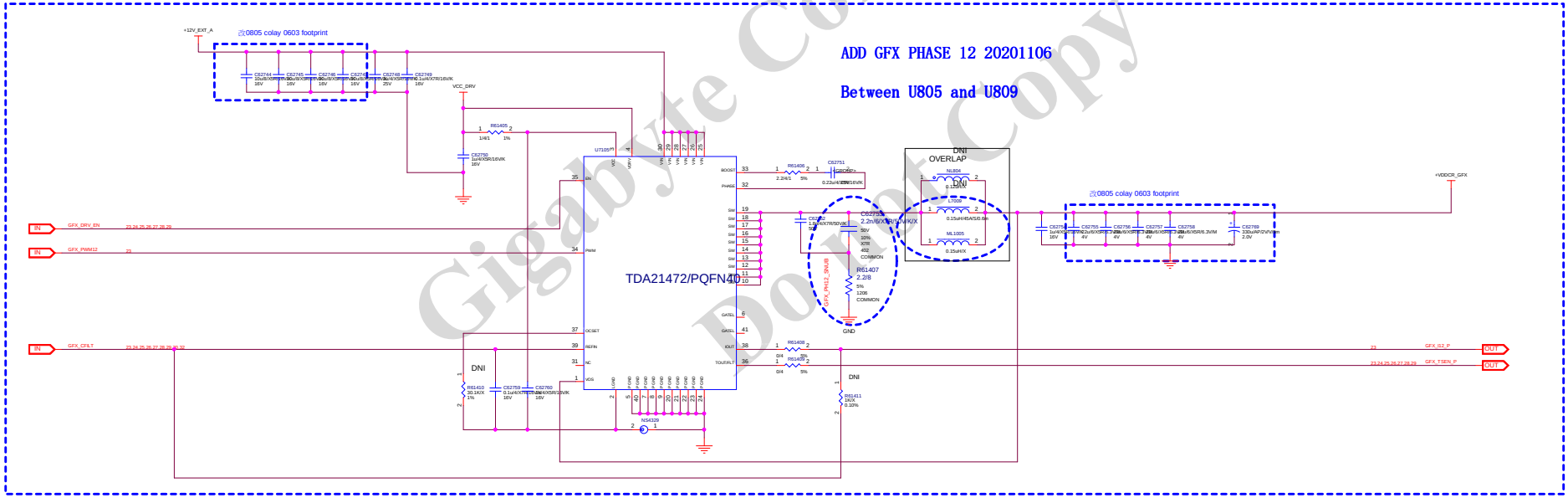
Change Input power to +12V_EXT_C





ADD GFX PHASE 12 20201106

Between U805 and U809

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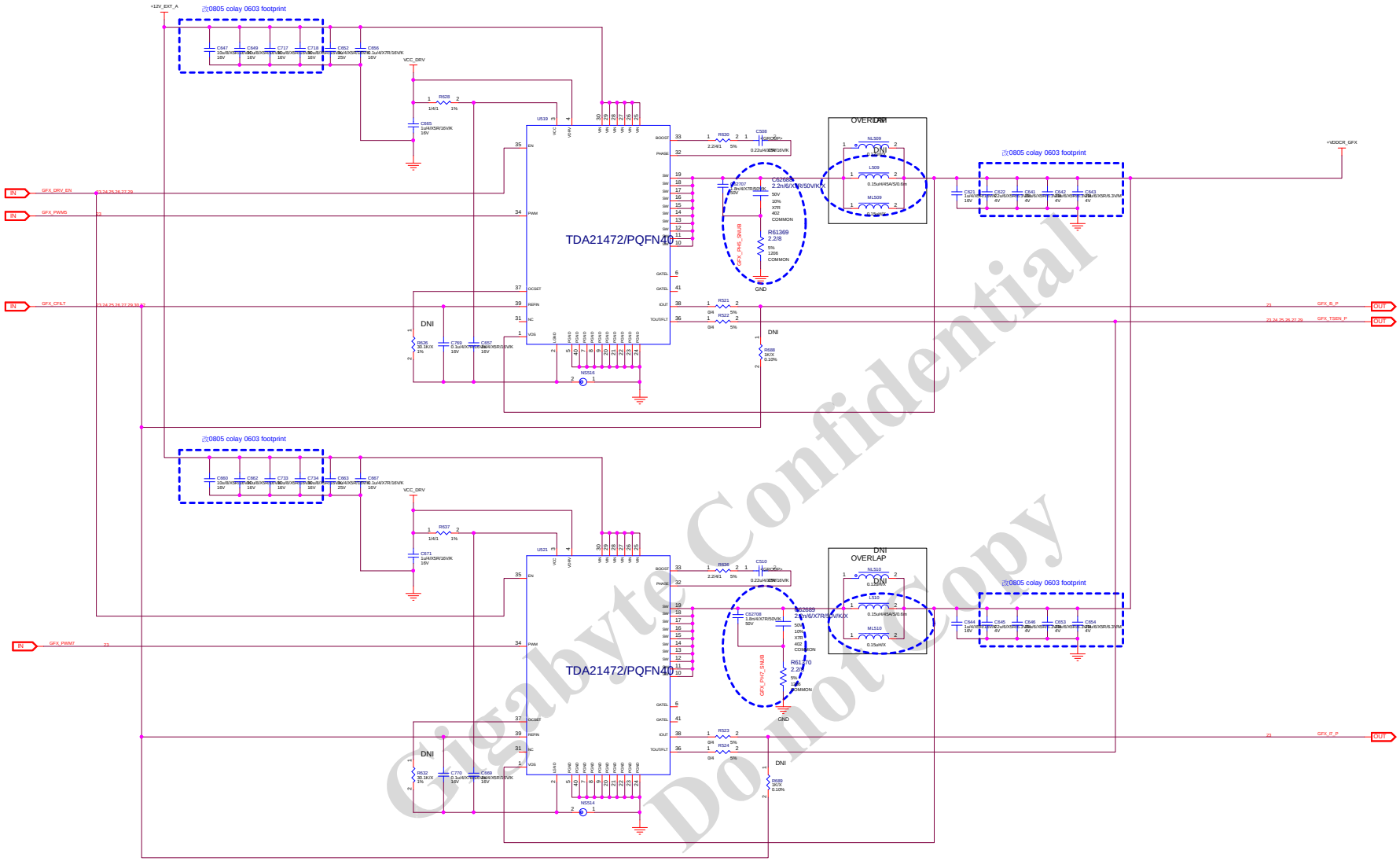

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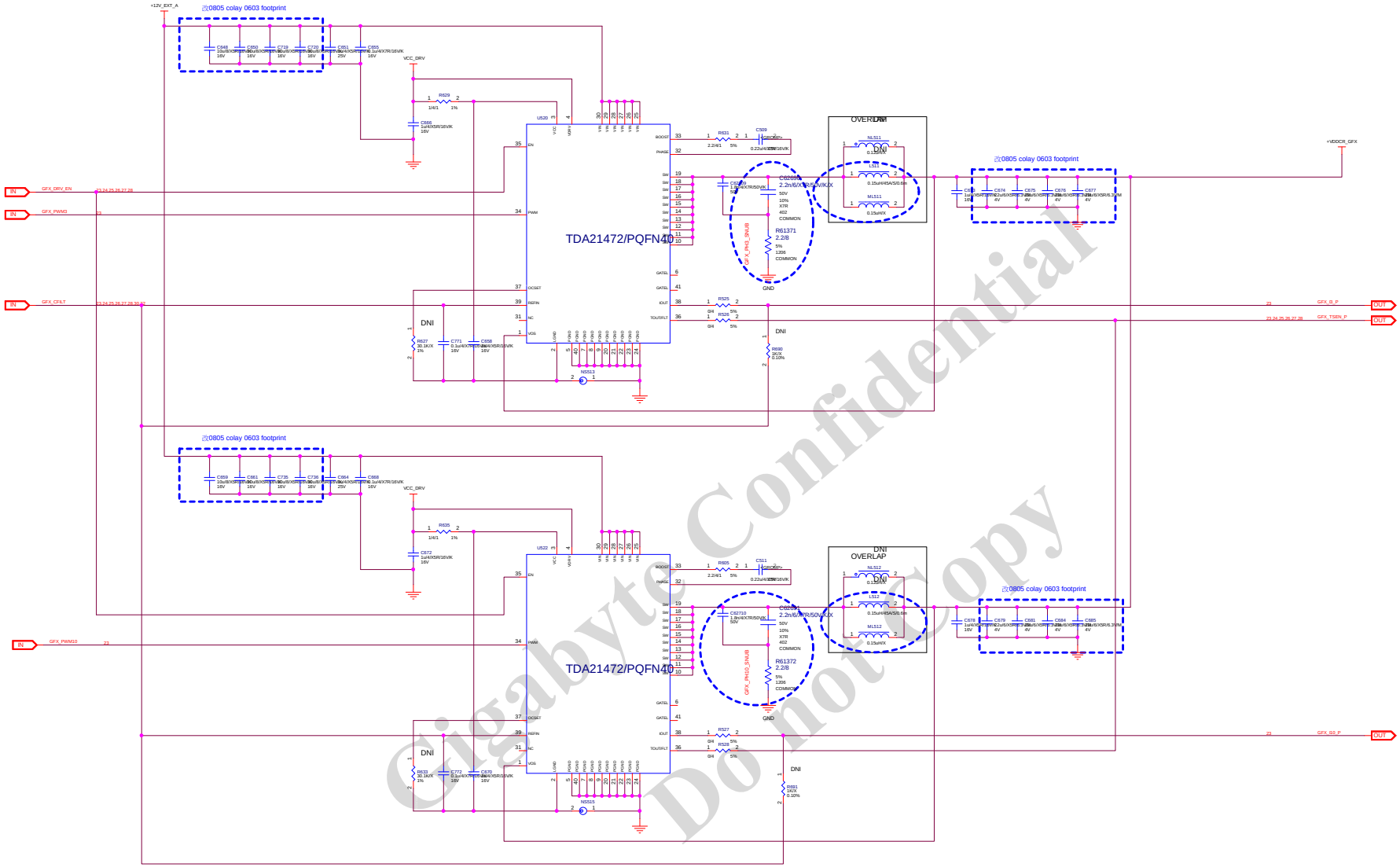

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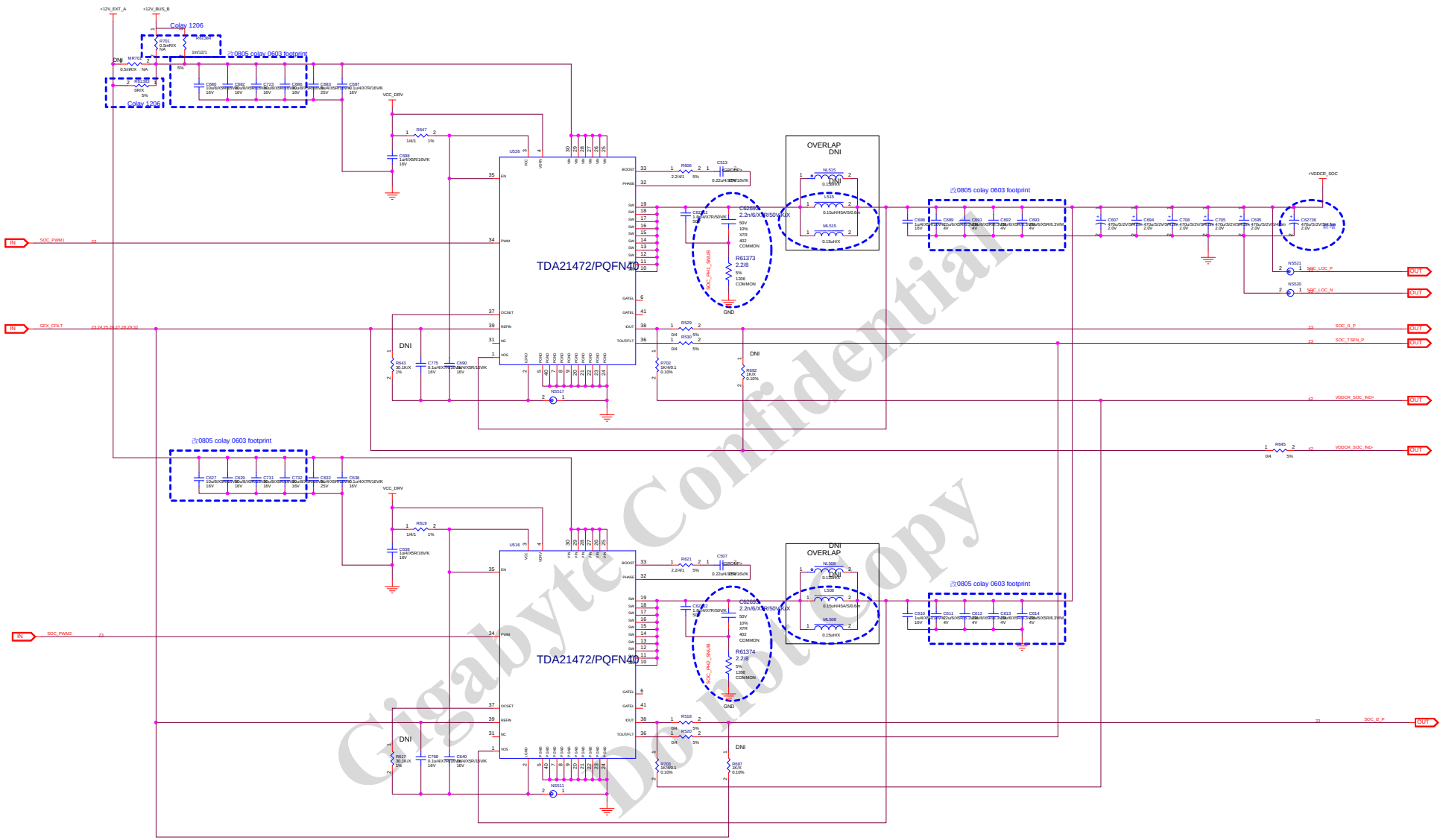

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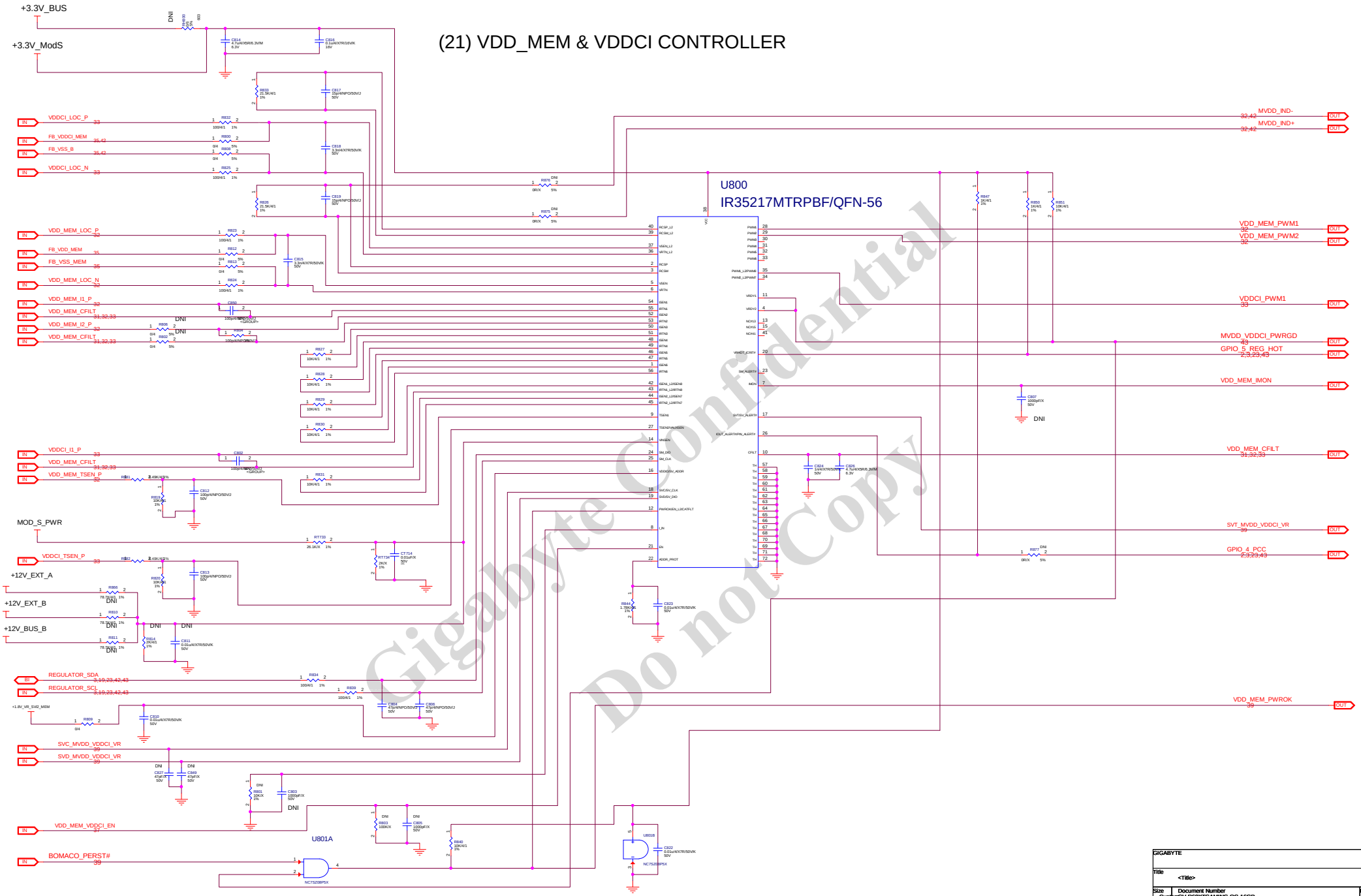
(21) VDD_MEM & VDDCI CONTROLLER



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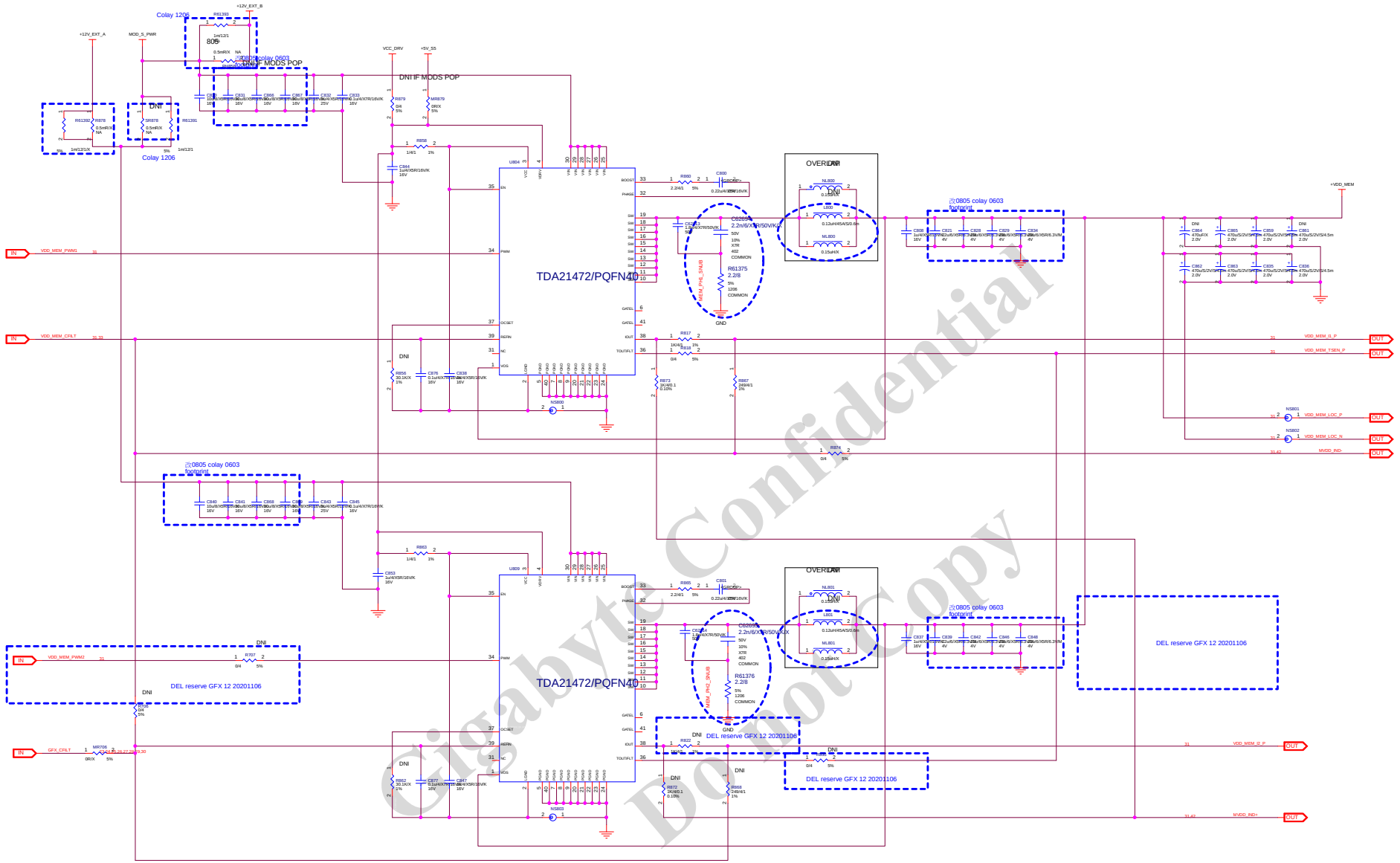

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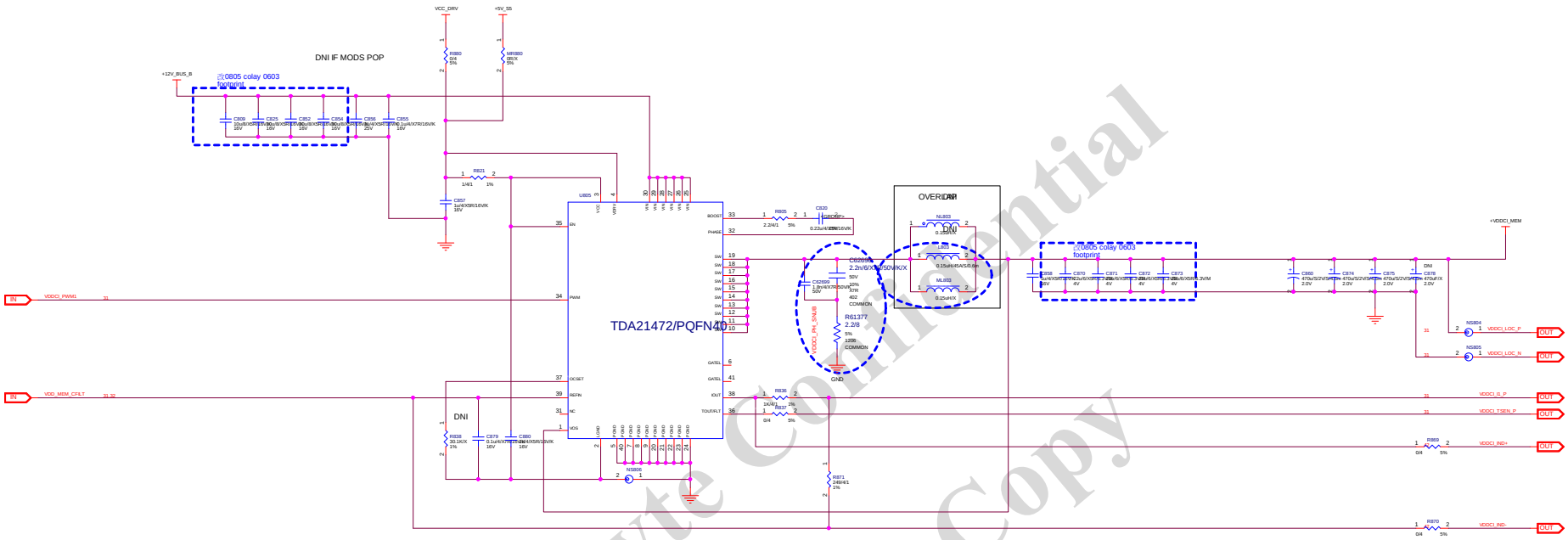

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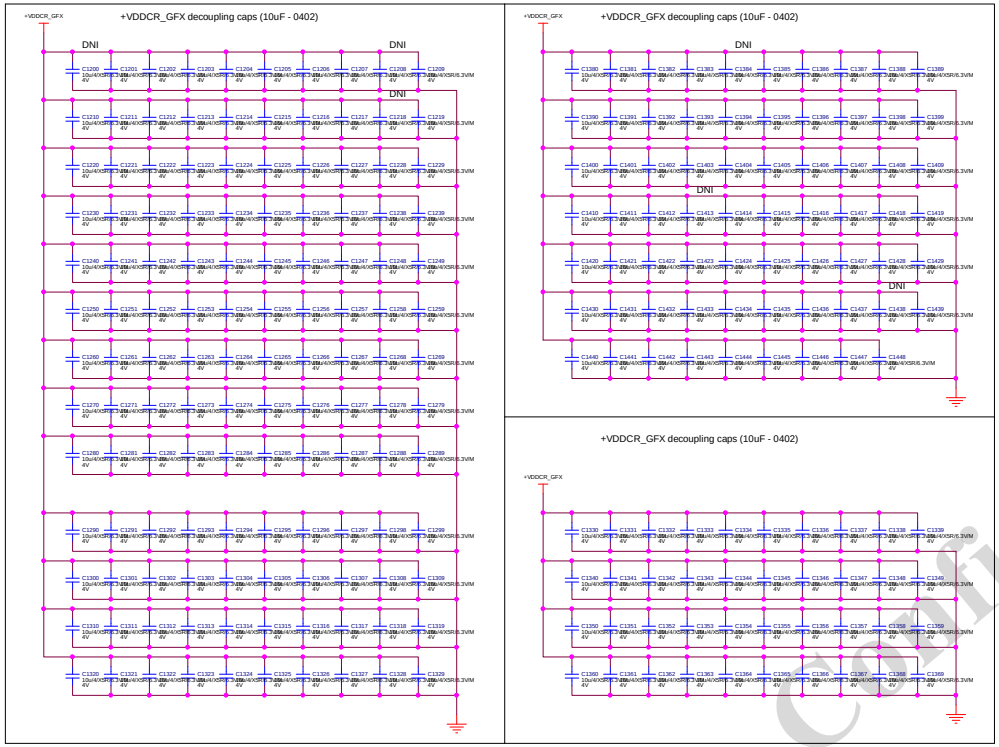

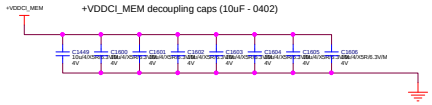

DNI these six caps to match SLT board and keep the design consistent across SKUs

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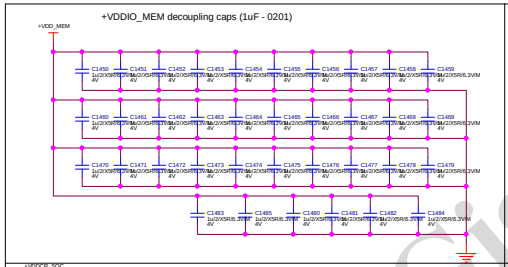
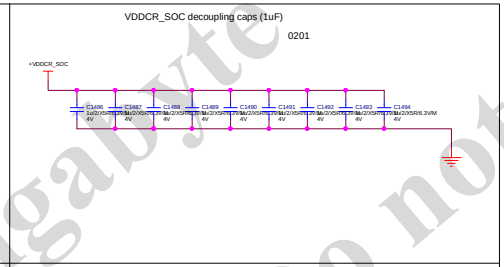
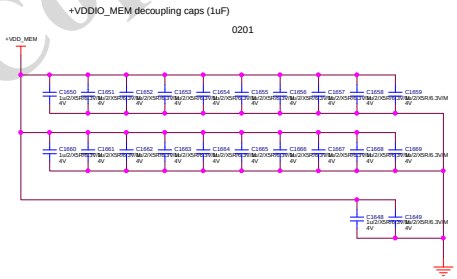
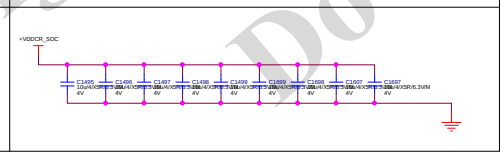
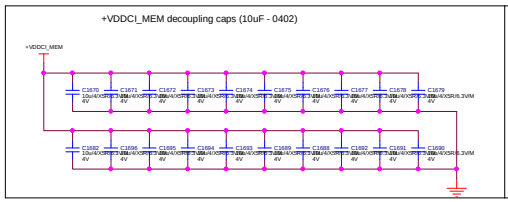
C1208
C1200
C1438
C1413
C1384

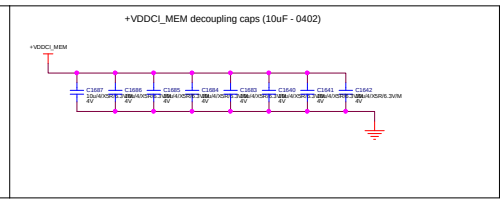












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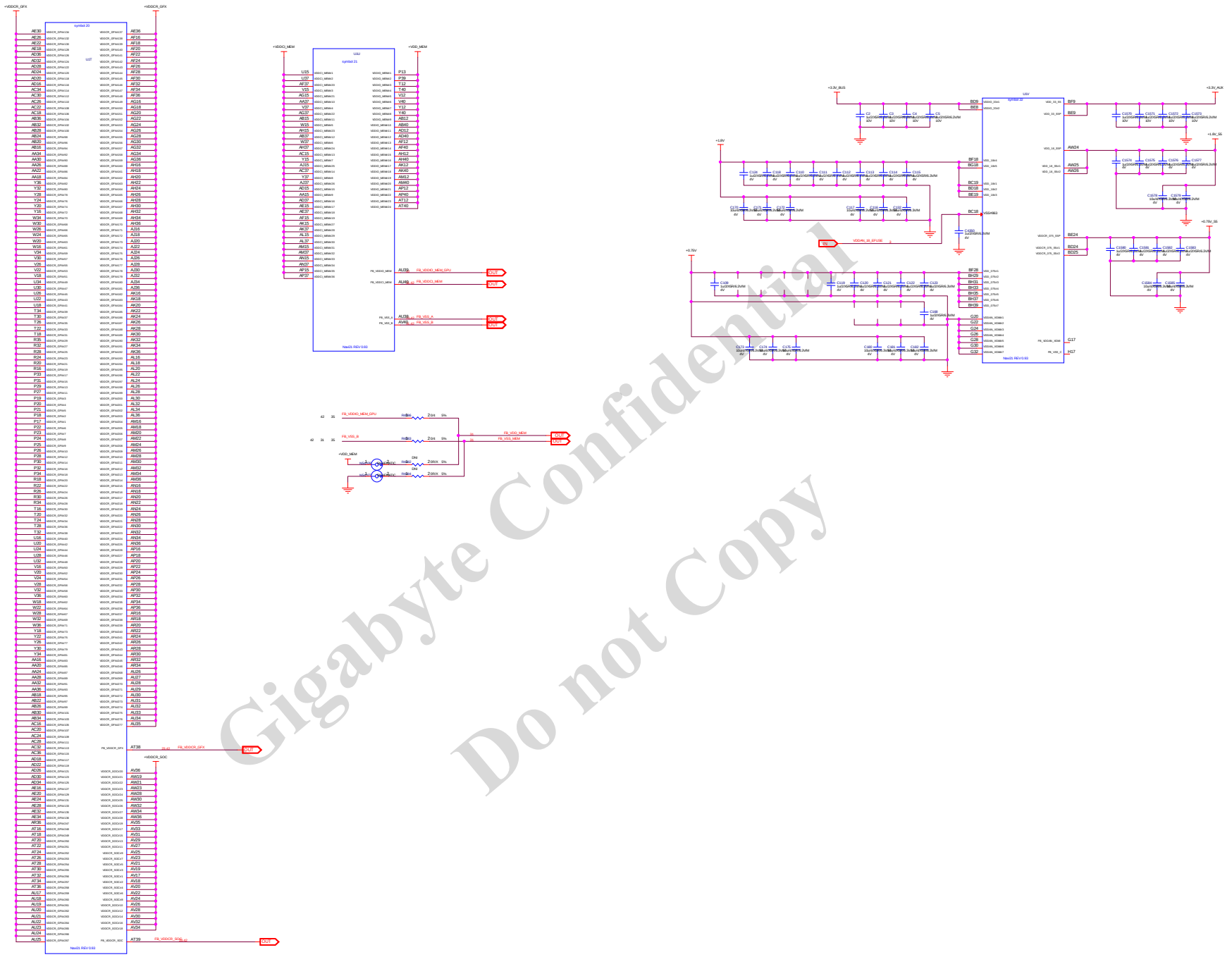

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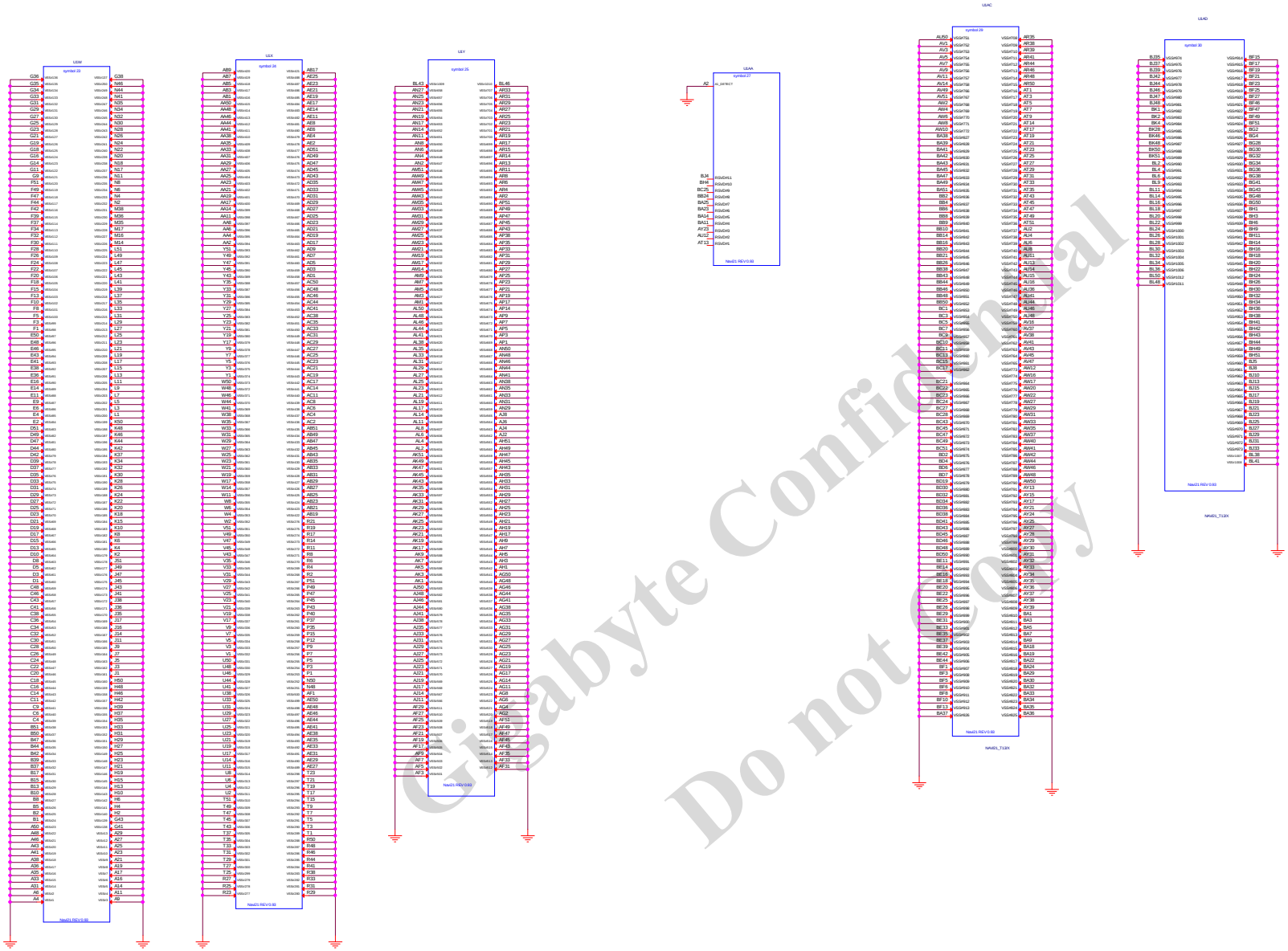

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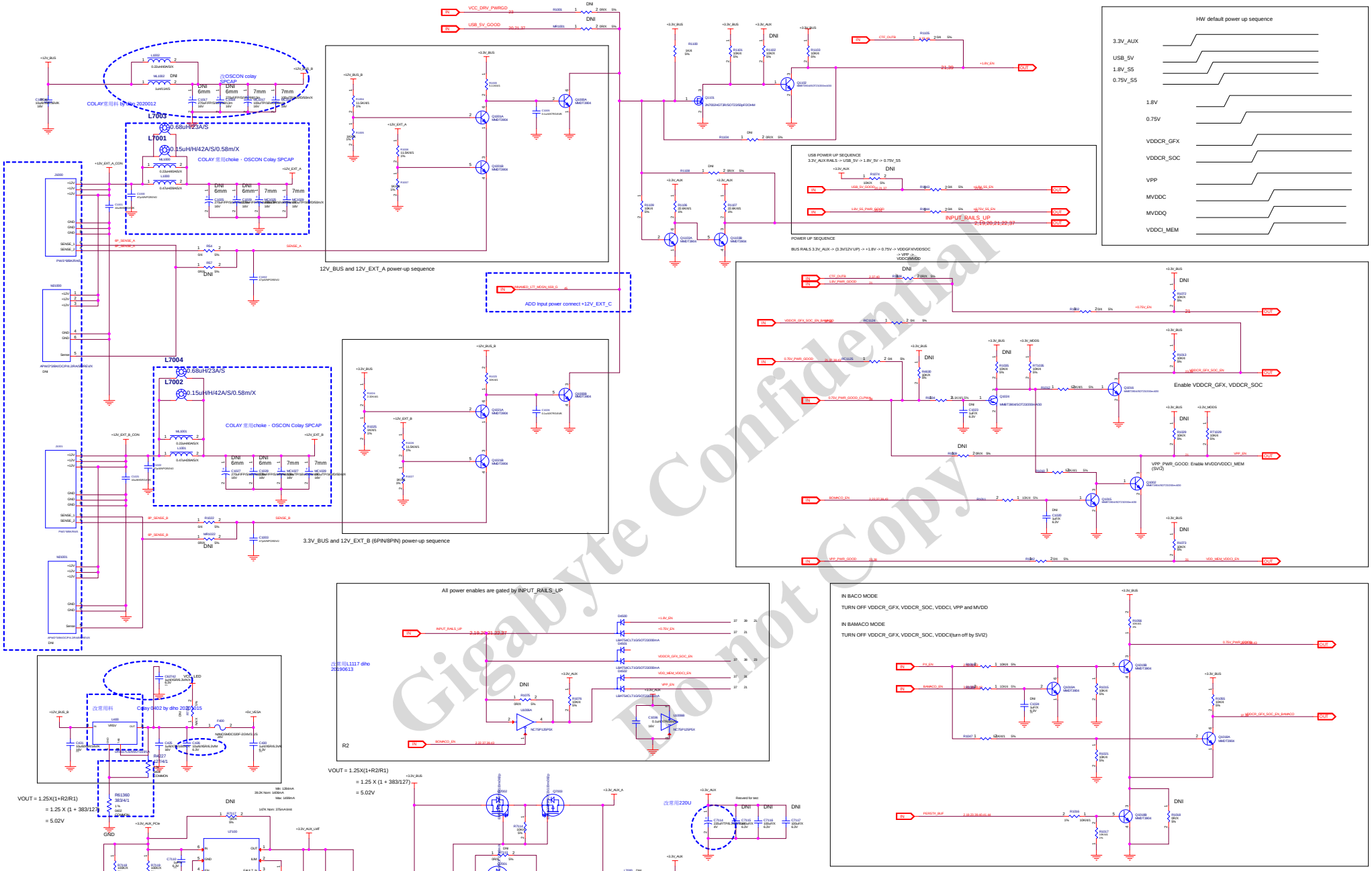

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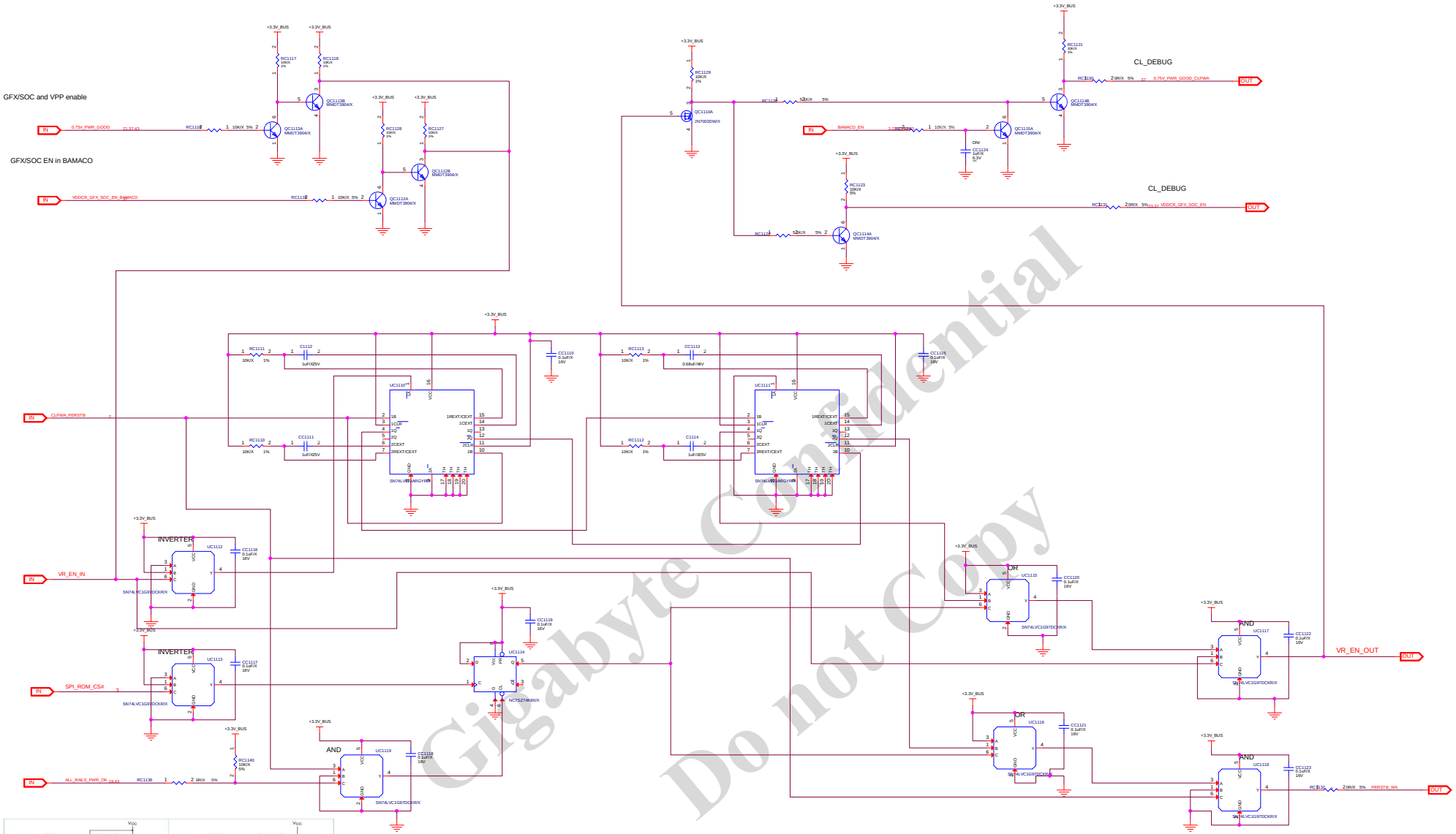

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Figure 10. 2-input NAND gate with input A inverted or 2-input OR gate with input C inverted

Figure 11. 2-input NOR gate with input B inverted or 2-input AND gate with input C inverted

Figure 12. 2-input OR gate

Figure 13. Inverter

Figure 14. Buffer

Figure 8. 2-input MUX

Figure 9. 2-input AND gate

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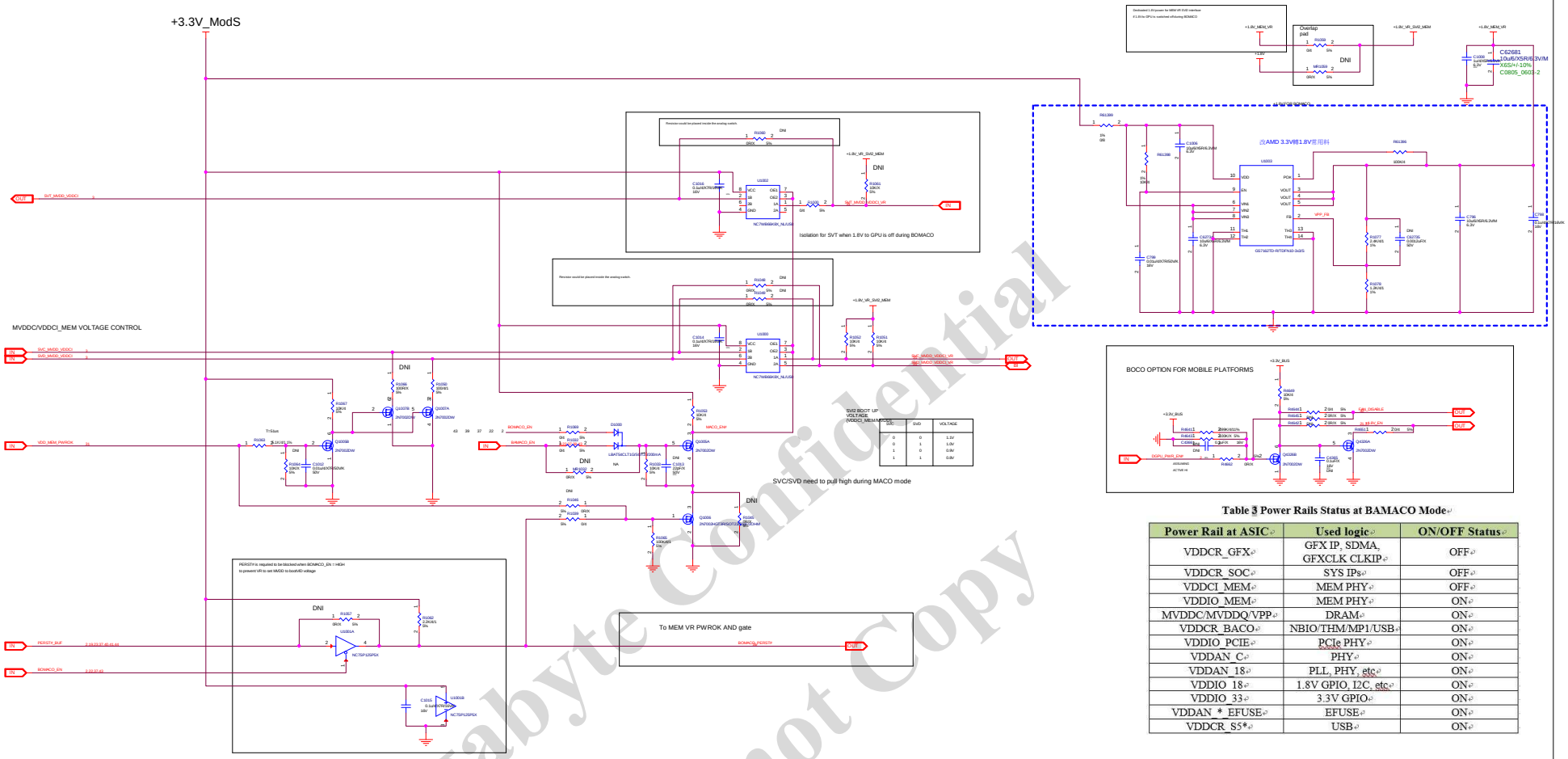

Table 3 Power Rails Status at BAMACO Mode

Power Rail at ASIC	Used logic	ON/OFF Status
VDDCR_GFX	GFX IP, SDMA, GFXCLK CLKIP	OFF
VDDCR_SOC	SYS IPs	OFF
VDDCI_MEM	MEM PHY	OFF
VDDIO_MEM	MEM PHY	ON
MVDDC/MVDDQ/VPP	DRAM	ON
VDDCR_BACO	NBIO/THM/MP1/USB	ON
VDDIO_PCIE	PCIe PHY	ON
VDDAN_C	PHY	ON
VDDAN_18	PLL, PHY, etc	ON
VDDIO_18	1.8V GPIO, I2C, etc	ON
VDDIO_33	3.3V GPIO	ON
VDDAN_*_EFUSE	EFUSE	ON
VDDCR_S5*	USB	ON

Table 4 Key Signals at Different PM Modes

Signals	Default	BOCO	BOMACO
PX_EN	LOW	N/A	N/A
MACO_EN	N/A	N/A	N/A
PERSTb	HIGH	1->0->1	1->0->1
PWR_EN	HIGH	LOW	LOW
BOMACO_EN	LOW	LOW	HIGH

Table 5 Platform to Support BOMACO

BOMACO_EN	SVC PU/PD	SVD PU/PD
HIGH	PU	PU
LOW	bootVID	bootVID

Table 3 Power Rails Status at BOMACO Mode

Power Rail at ASIC	Used logic	ON/OFF Status for BOMACO-A
VDDCR_GFX	GFX IP, SDMA, GFXCLK CLKIP	OFF
VDDCR_SOC	SYS IPs	OFF
VDDCI_MEM	MEM PHY	OFF
VDDIO_MEM	MEM PHY	ON
MVDDC/MVDDQ/VPP	DRAM	ON
VDDCR_BACO	NBIO/THM/MP1/USB	OFF
VDDIO_PCIE	PCIe PHY	OFF
VDDAN_C	PHY	OFF
VDDAN_18	PLL, PHY, etc	OFF
VDDIO_18	1.8V GPIO, I2C, etc	OFF
VDDIO_33	3.3V GPIO	OFF
VDDAN_*_EFUSE	EFUSE	OFF
VDDCR_S5*	USB	ON

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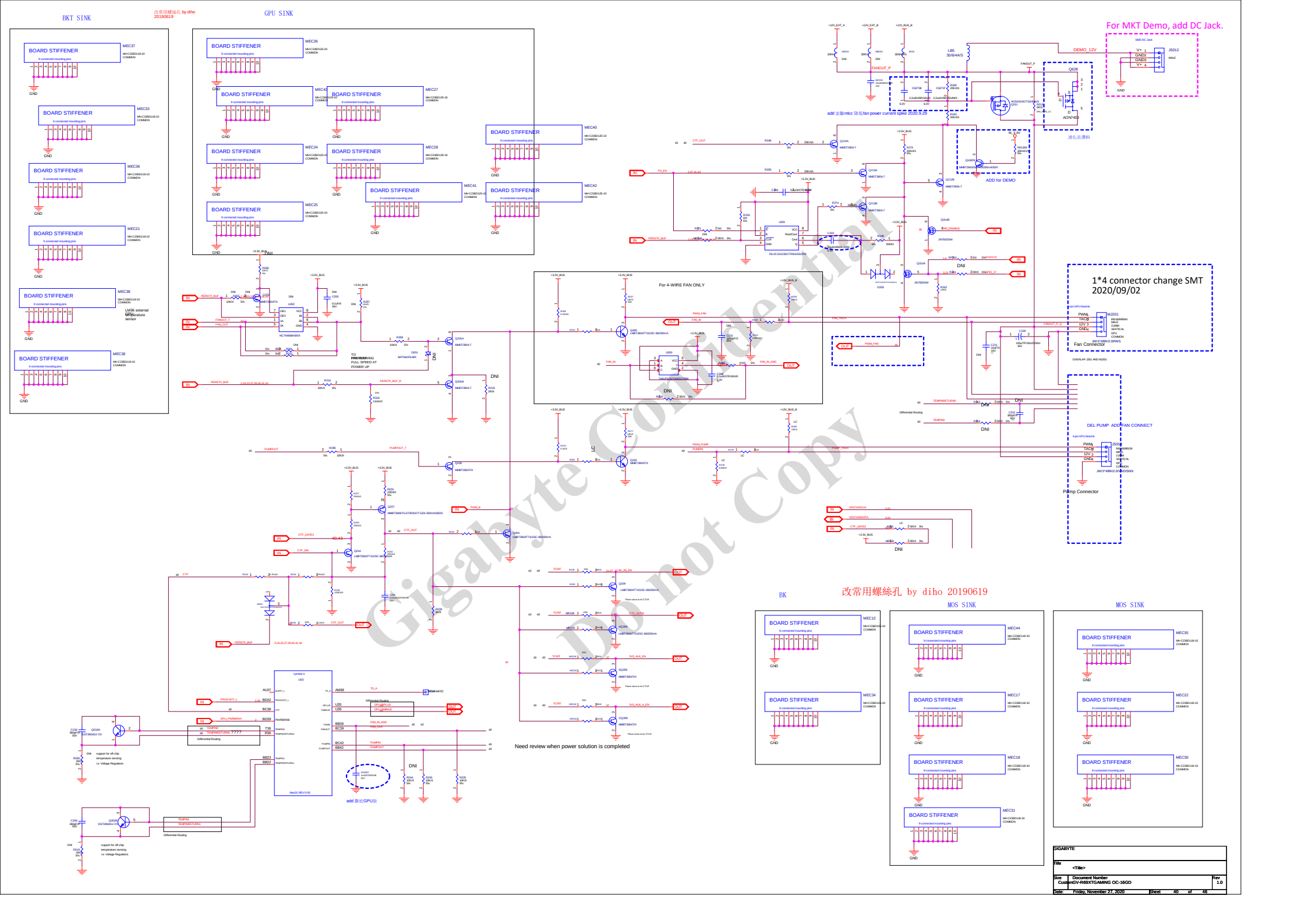

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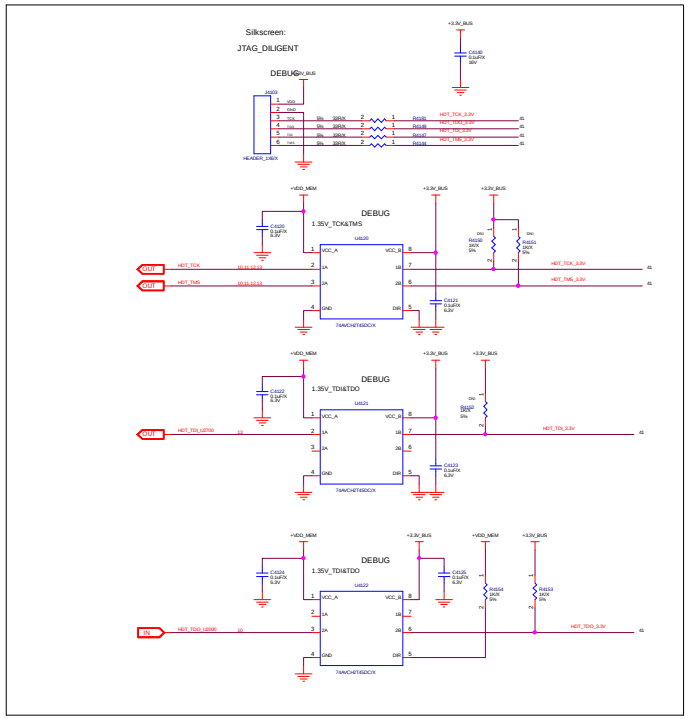

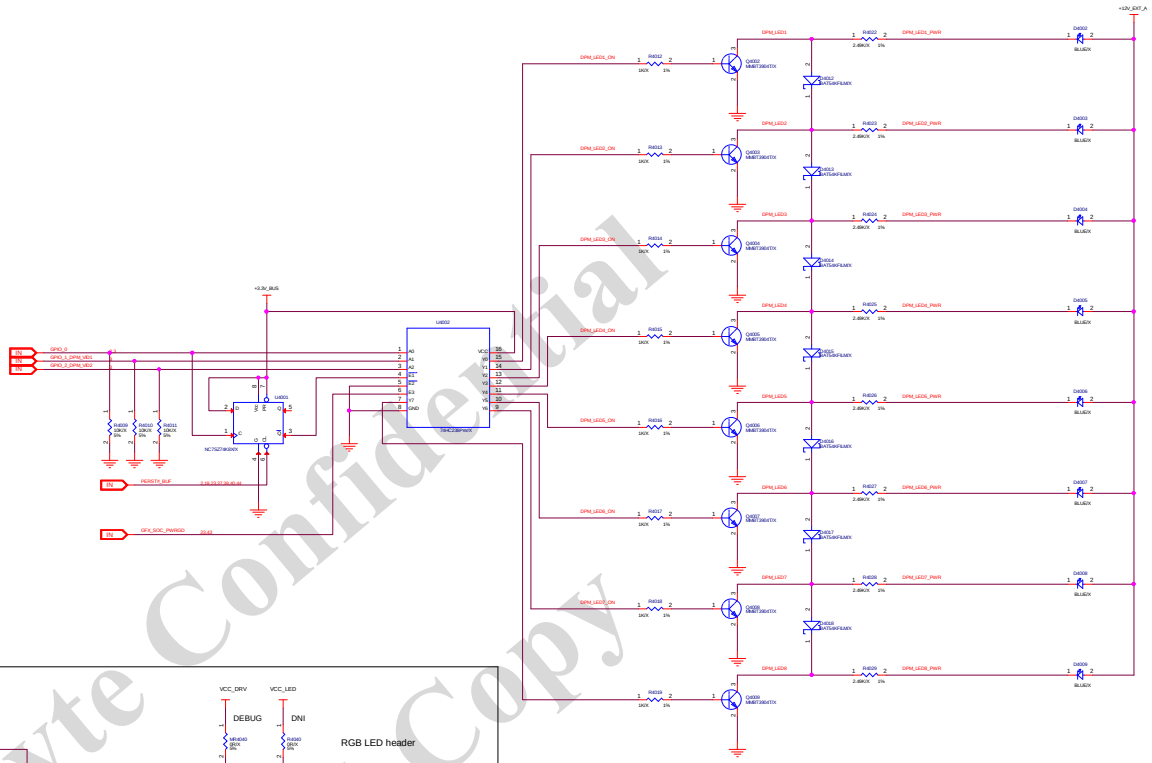

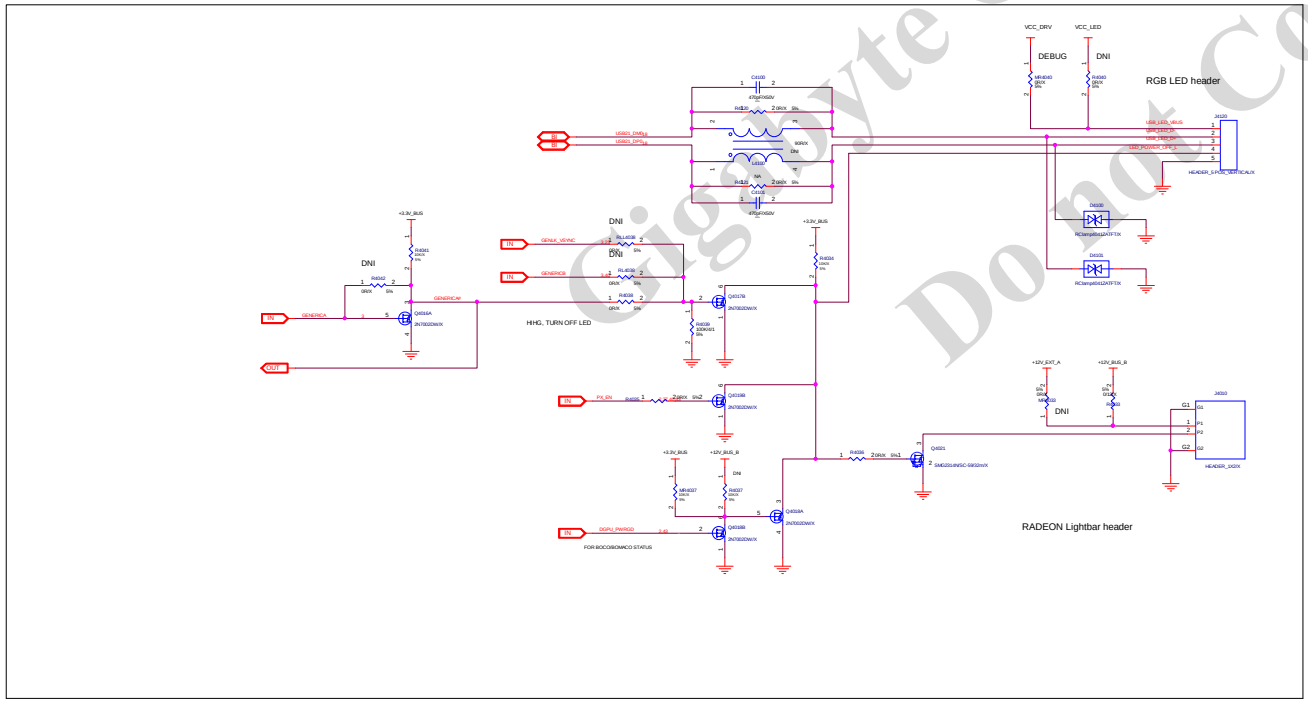

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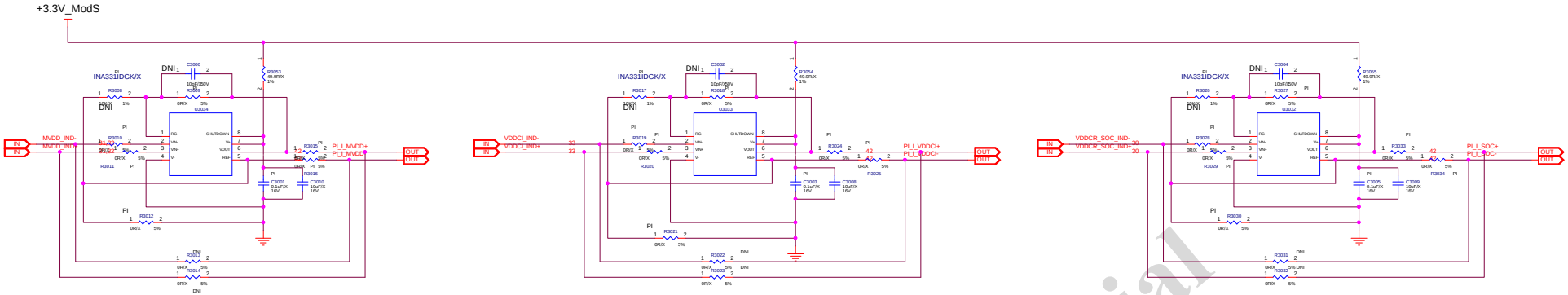

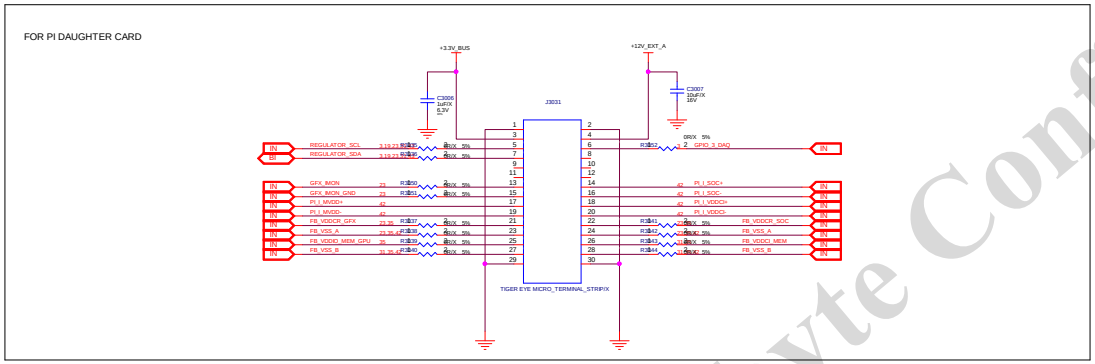

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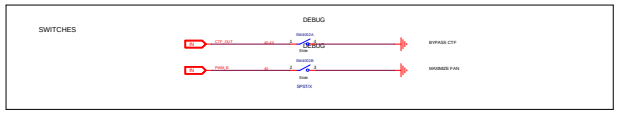
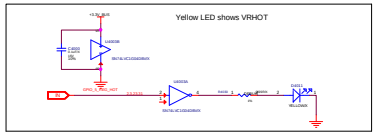
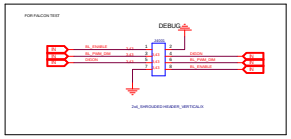
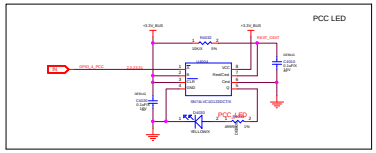
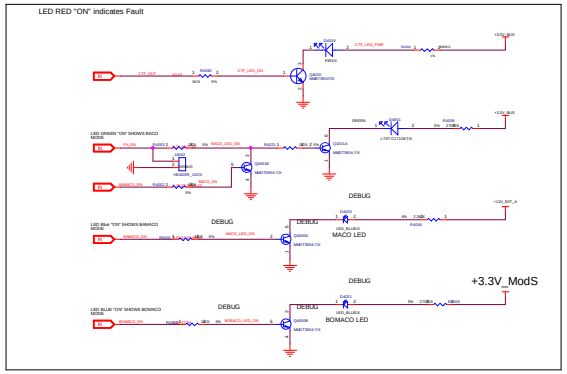
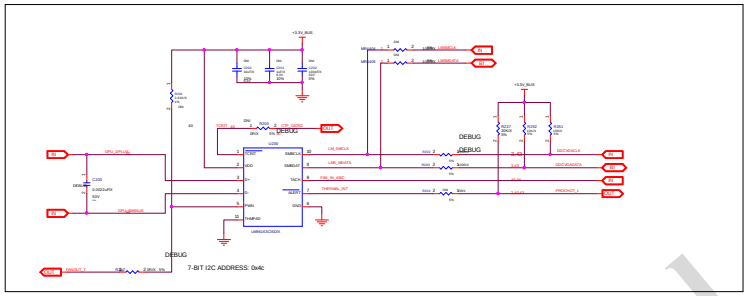


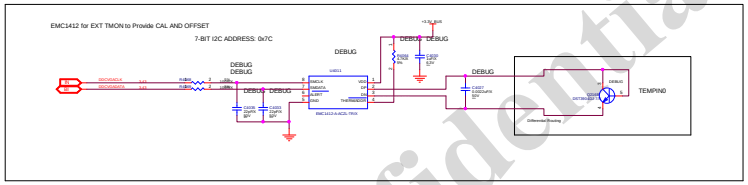


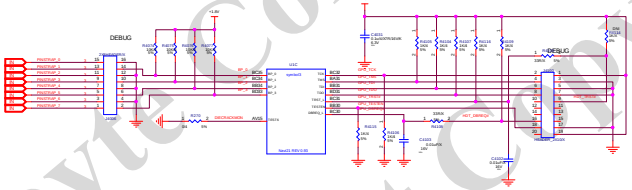












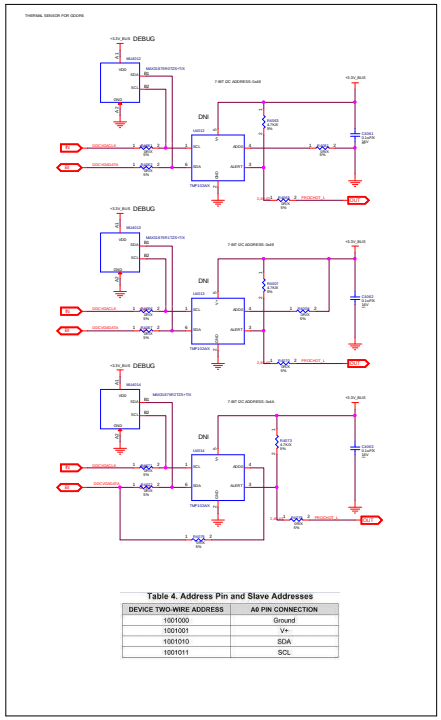
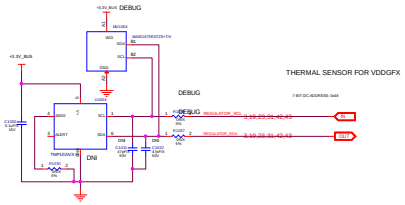
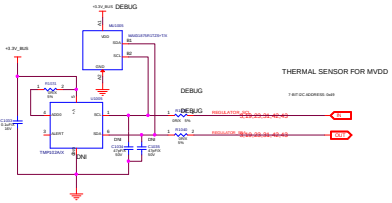
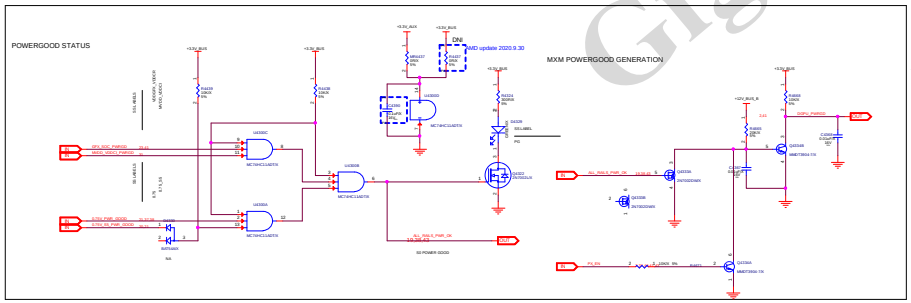


Table 4. Address Pin and Slave Addresses

DEVICE TWO-WIRE ADDRESS	A0 PIN CONNECTION
1001000	Ground
1001001	V+
1001010	SDA
1001011	SCL







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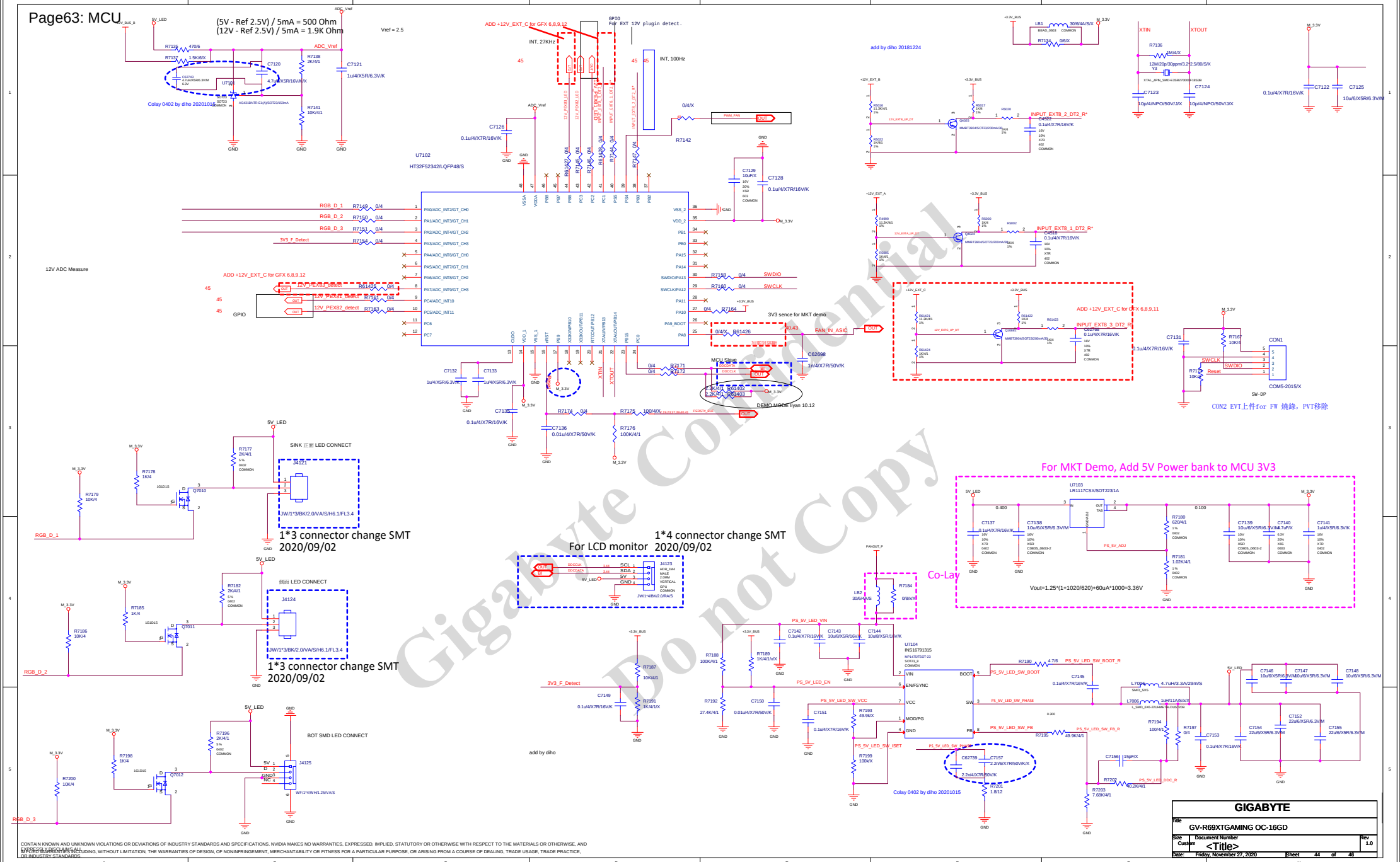

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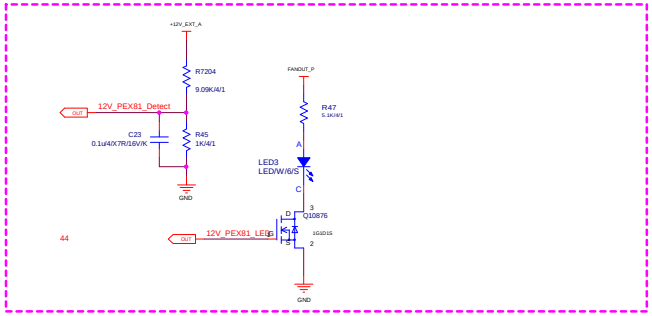

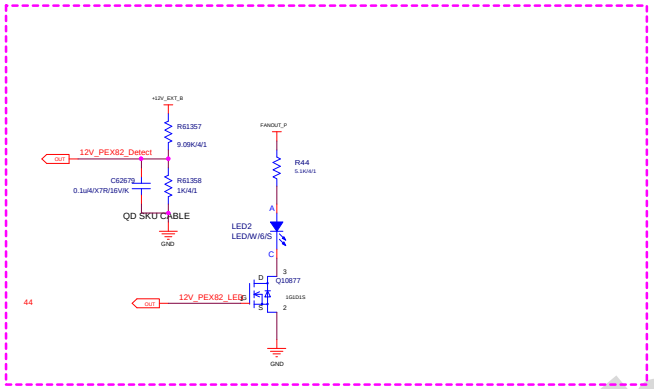

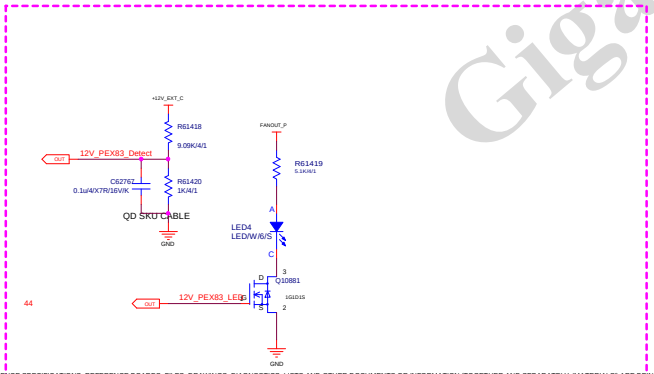

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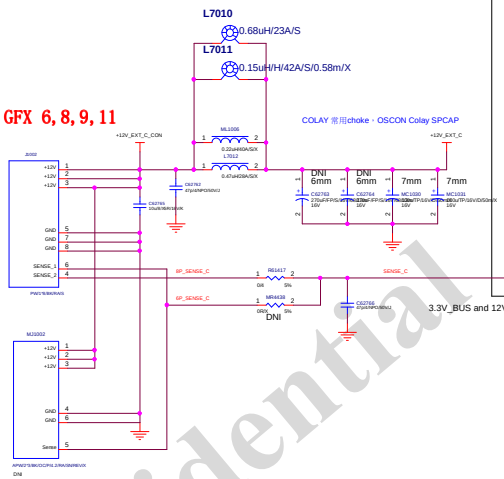
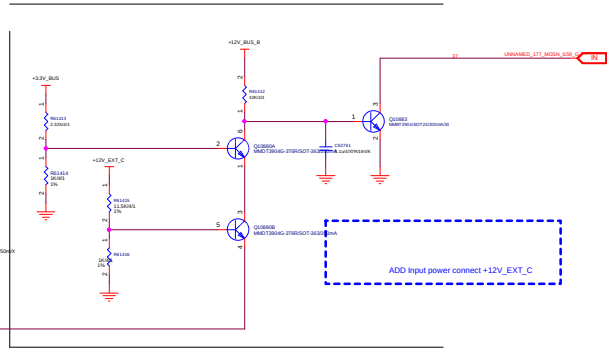
0805 COLAY 0603 diho 2018.12.02





3.3V_BUS and 12V_EXT_C (6PIN/8PIN) power-up sequence

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0	A	07/23/2019	Initial schematic creation
1	-00B	Nov 11 2019	Added MODS circuit
1	-00C	Jan 21 2020	Connected +1.8V_S5 to OSC_VDD18 Gated +VBUS_PWR_USBC0 by MOSFET Modified USBC0 Power protection circuits

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