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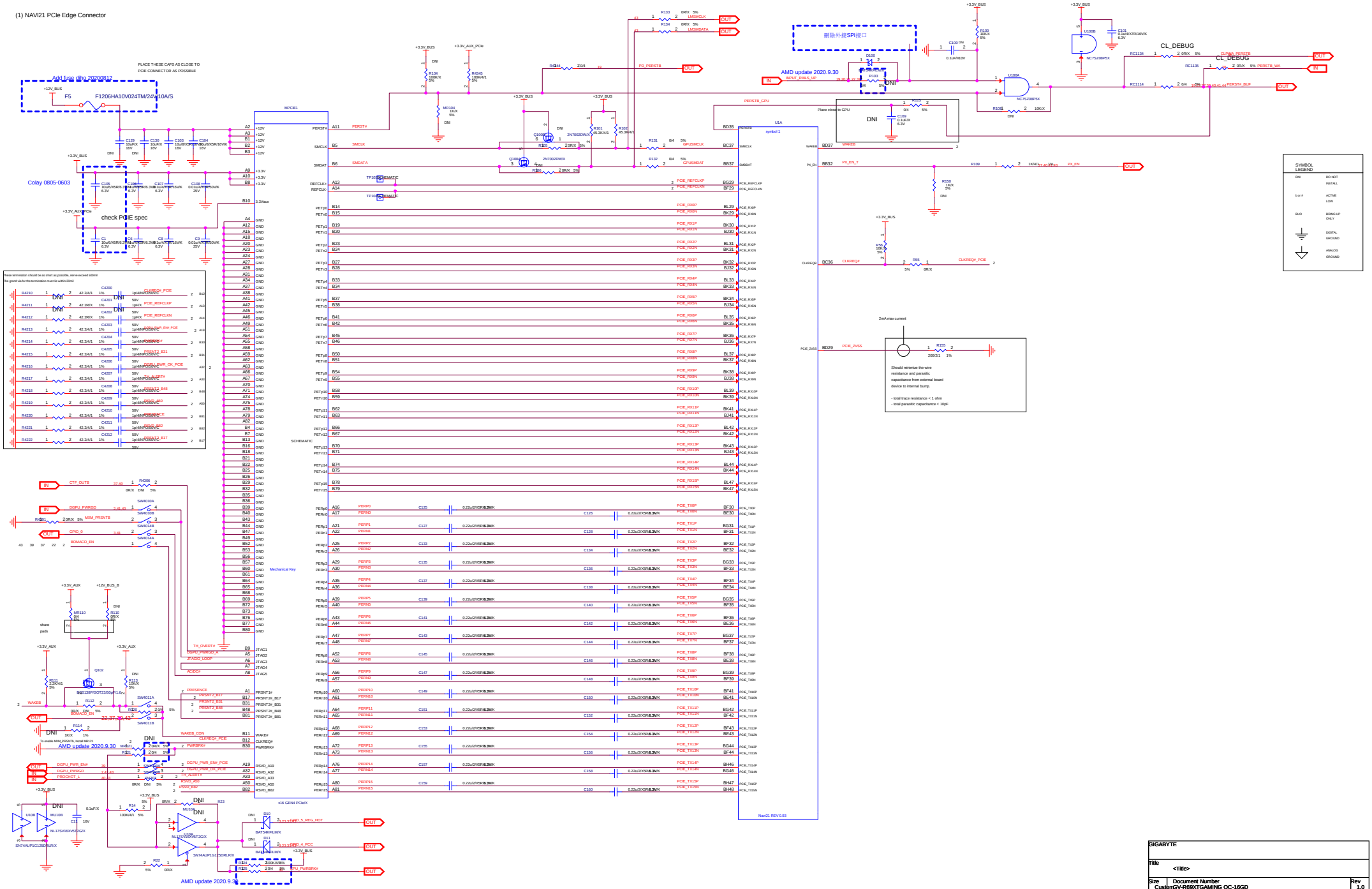
(1) NAVI21 PCIe Edge Connector
PLACE THESE CAPS AS CLOSE TO PCIE CONNECTOR AS POSSIBLE
Add fuse ding 20200812
F5
F1206HA10V024TM/24V/10A/S
Colay 0805-0603
check PCIE spec
MPCIE1
Mechanical Key
x16 GEN4 PCIeX
SCHEMATIC
U1A
symbol 1
Navi21 REV 0.93
AMD update 2020.9.30
删除外接SPI接口
CL_DEBUG
SYMBOL LEGEND
DO NOT INSTALL
ACTIVE LOW
BRING UP ONLY
DIGITAL GROUND
ANALOG GROUND
2mA max current
Should minimize the wire resistance and parasitic capacitance from external board device to internal bump.
- total trace resistance < 1 ohm
- total parasitic capacitance < 10pF
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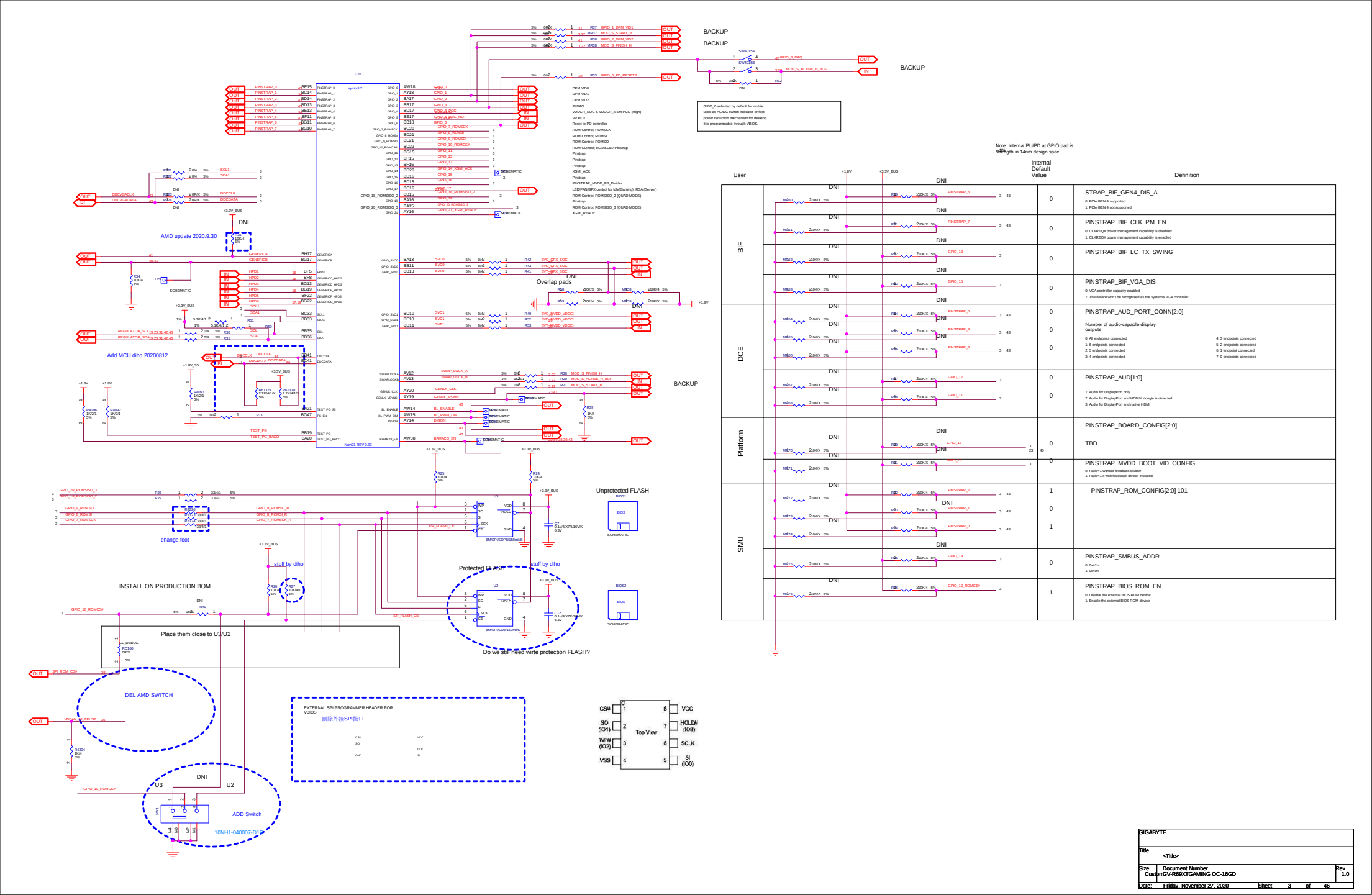

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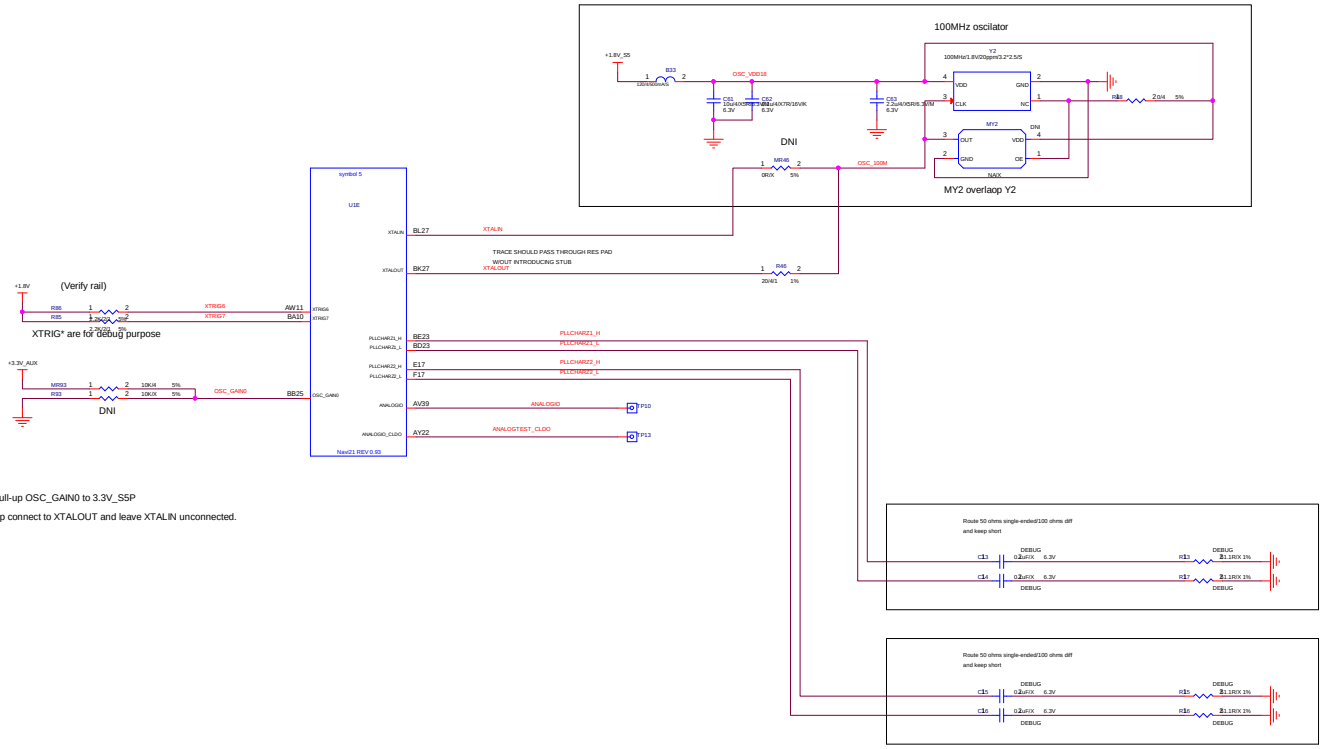

Default OSC_GAIN is 0x7. Pull-up OSC_GAIN0 to 3.3V_S5P

When 0x7, external clock chip connect to XTALOUT and leave XTALIN unconnected.

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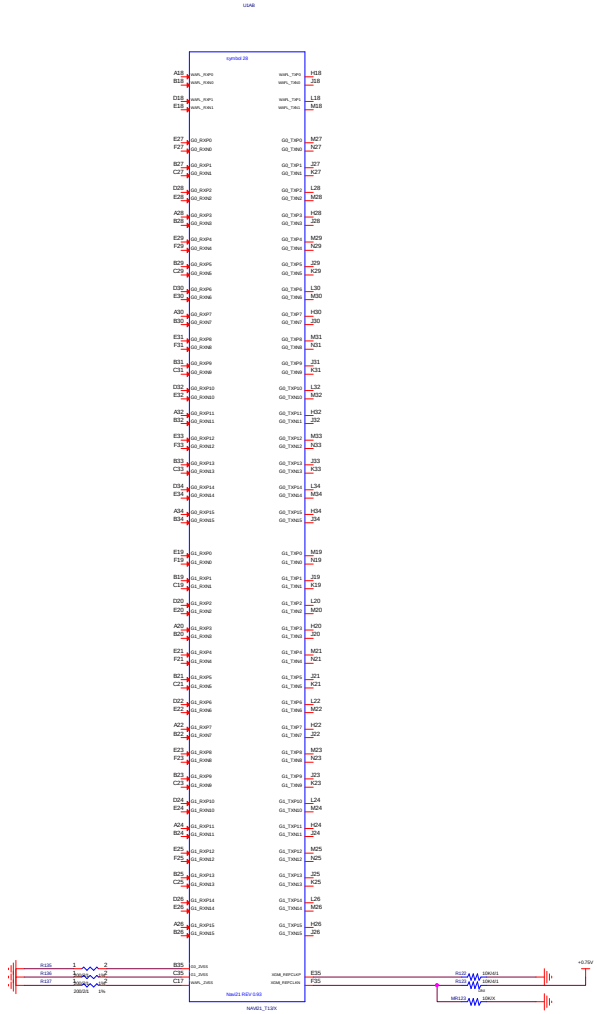
Navi21 XGMI LINK 0 & 1



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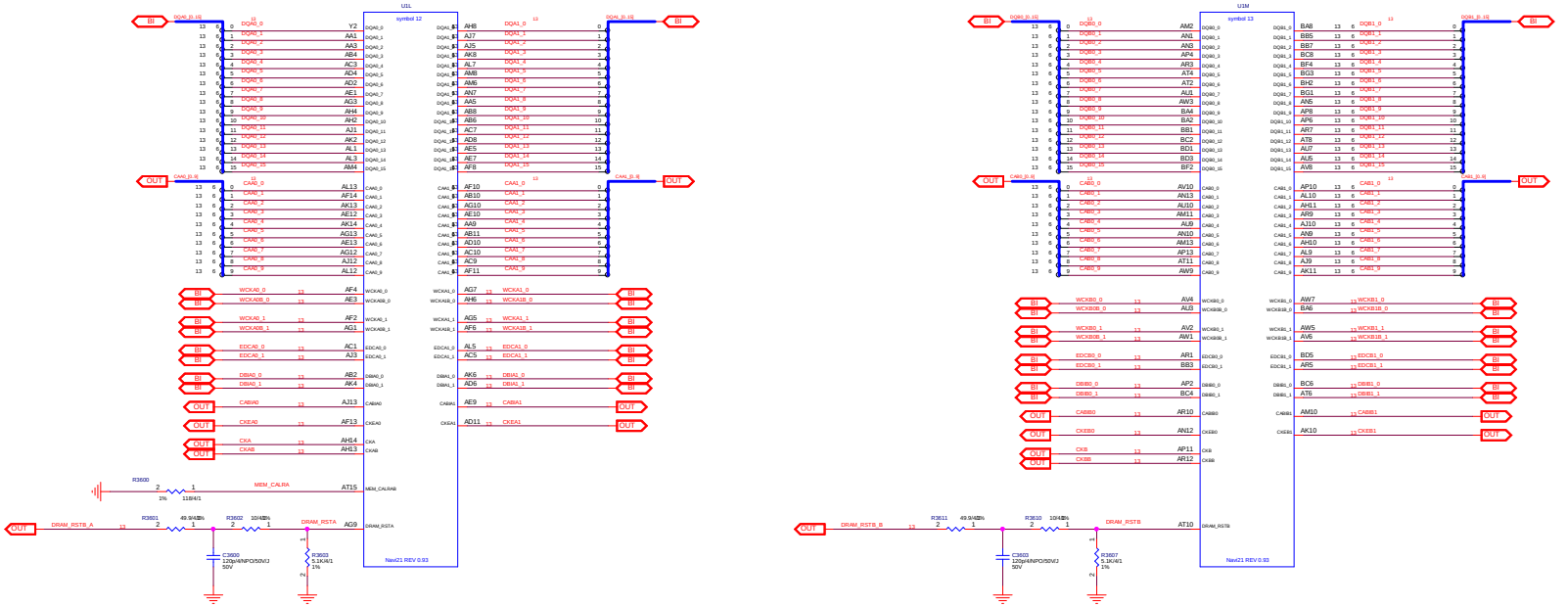
(1) NAVI 10 MEM INTERFACE CH A/B



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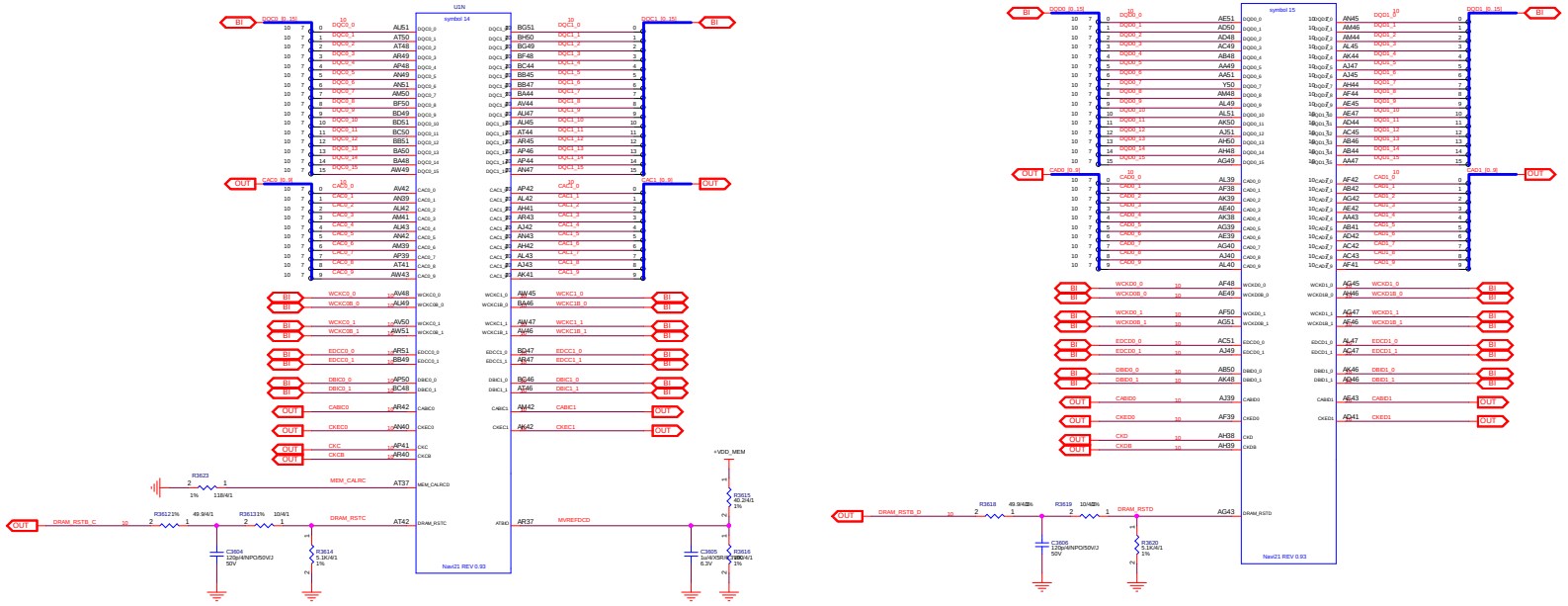
(2) NAVI 10 MEM INTERFACE CH C/D



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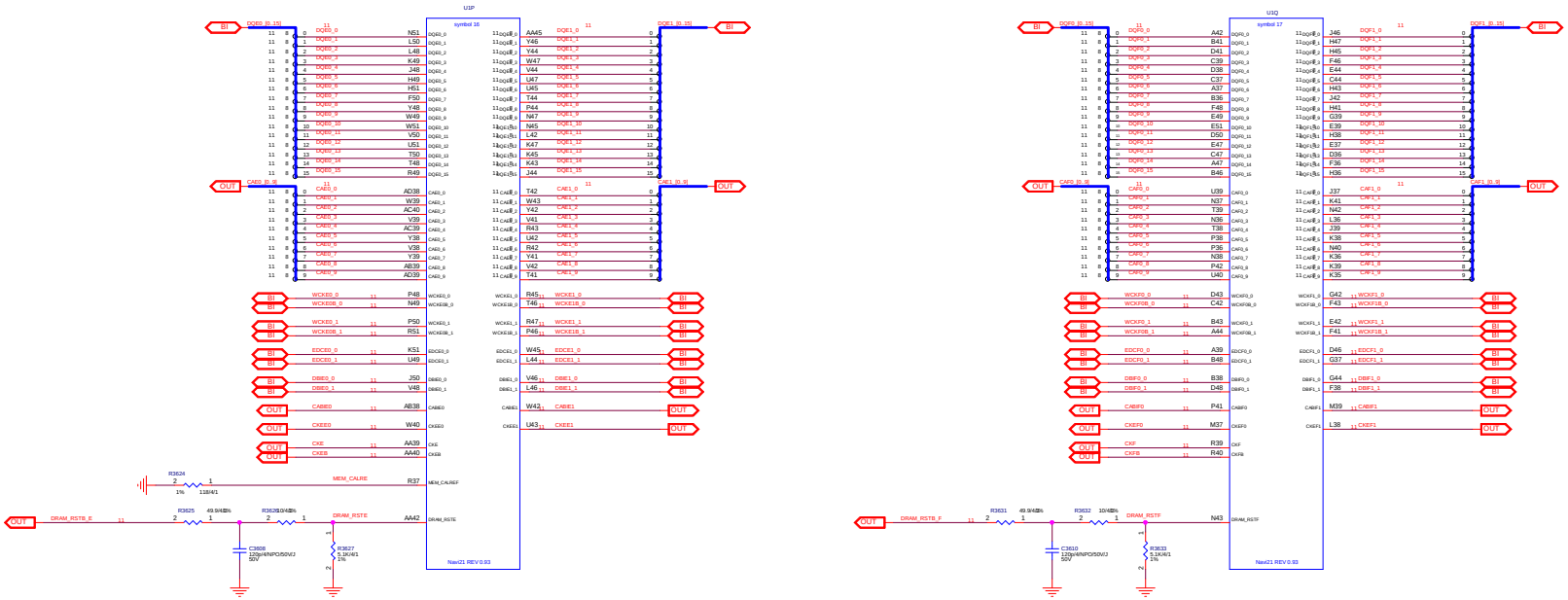
(3) NAVI 10 MEM INTERFACE CH E/F



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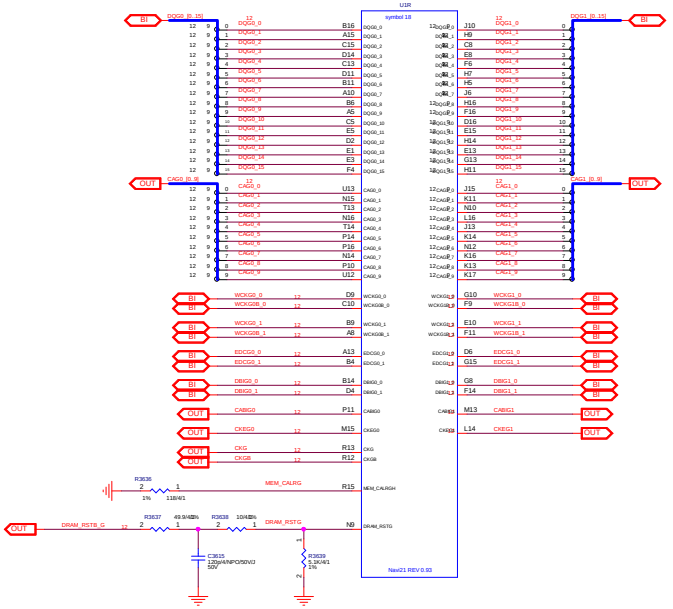
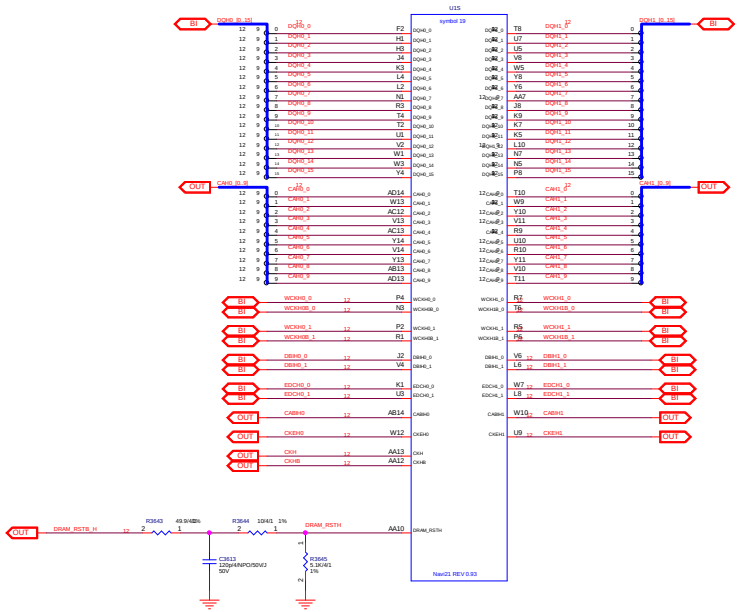
(4) NAVI 10 MEM INTERFACE CH G/H





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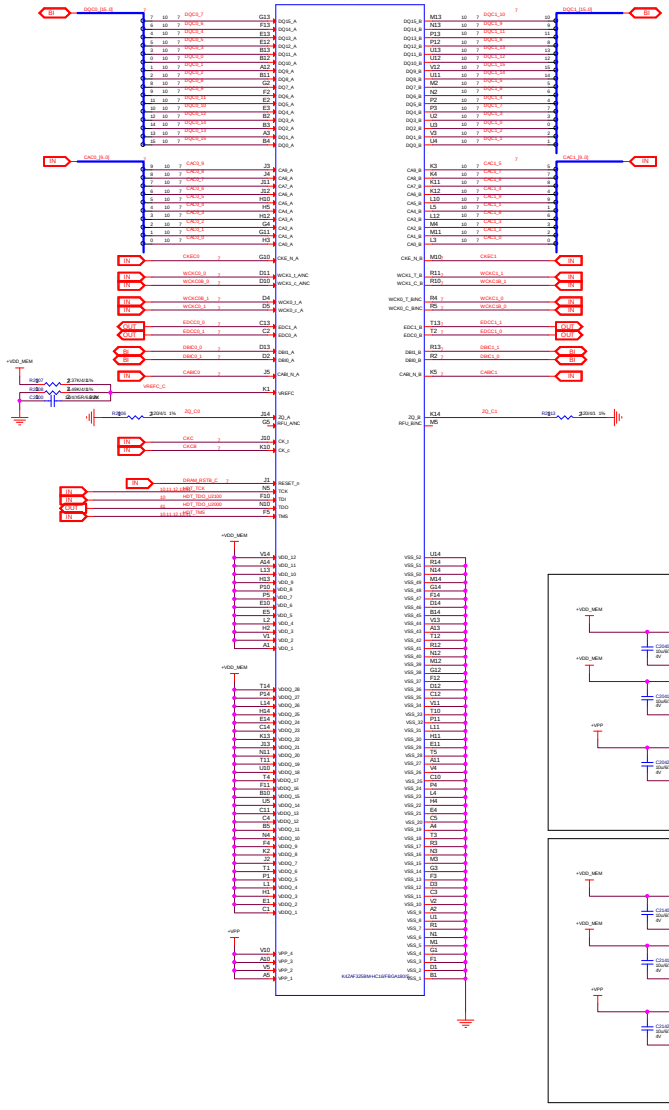
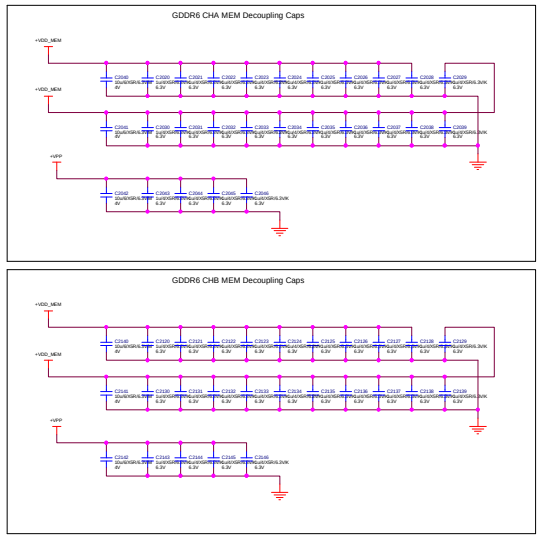
ASIC CH0 -> MEM CHA
ASIC CH1 -> MEM CHB





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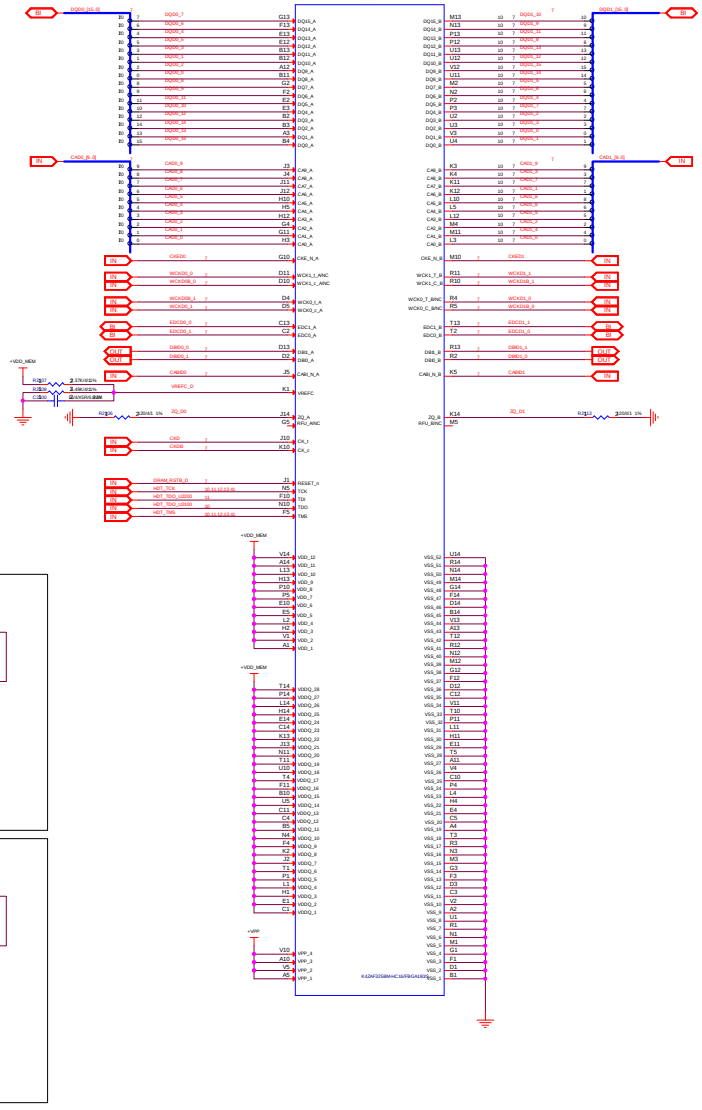

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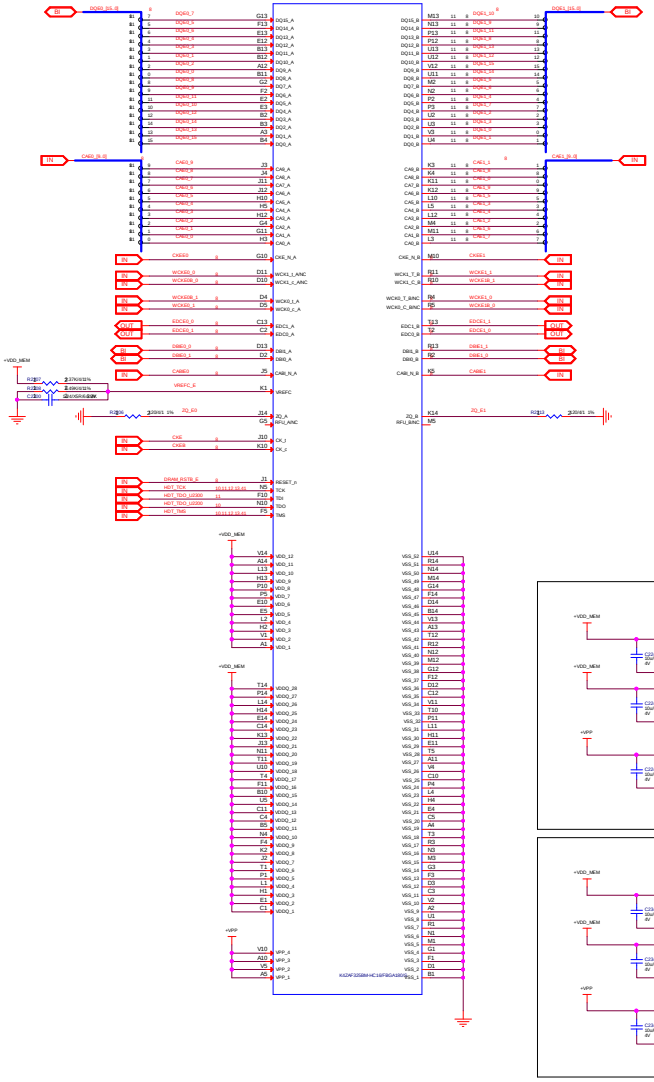
ASIC CH0 -> MEM CHA
ASIC CH1 -> MEM CHB



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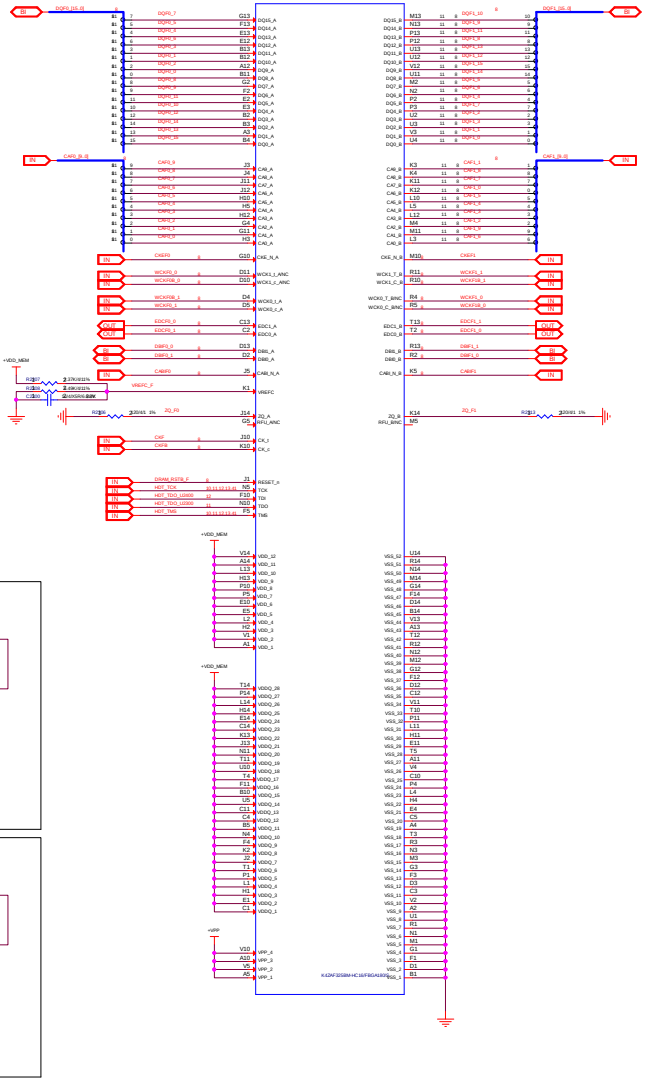

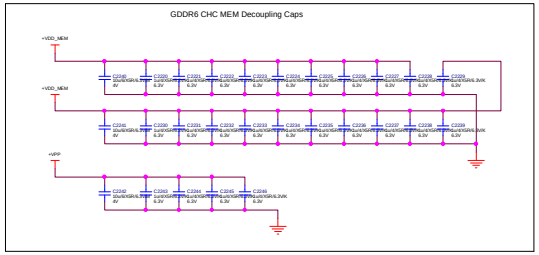

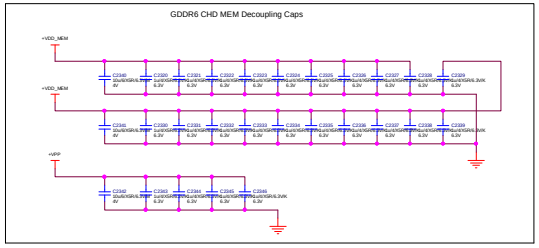

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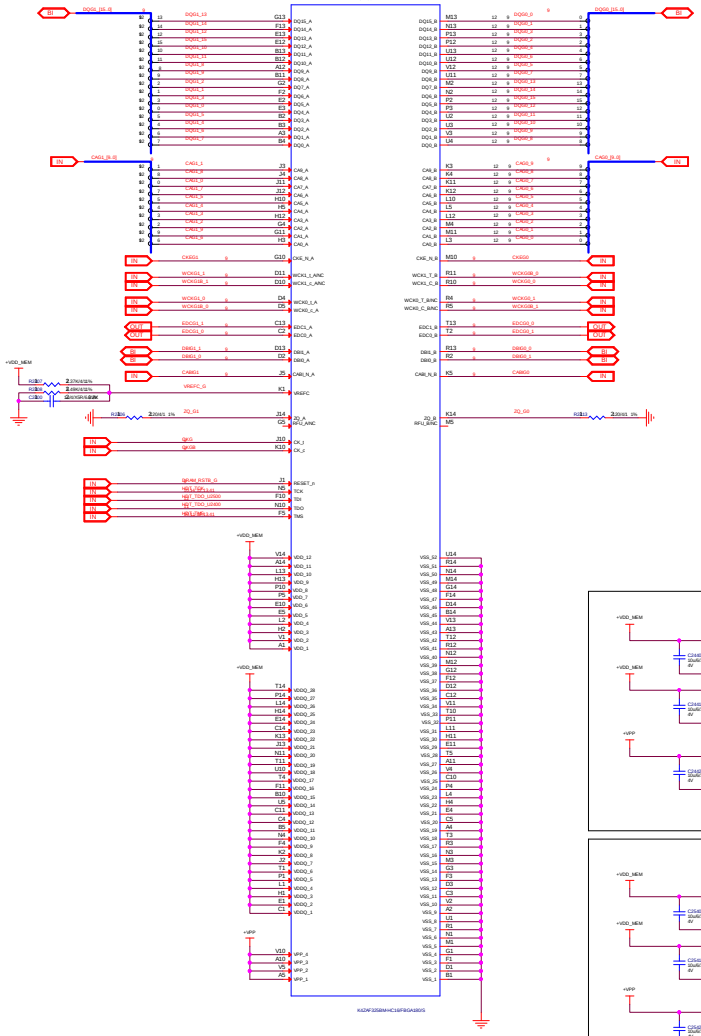
ASIC CH0 -> MEM CHB
ASIC CH1 -> MEM CHA



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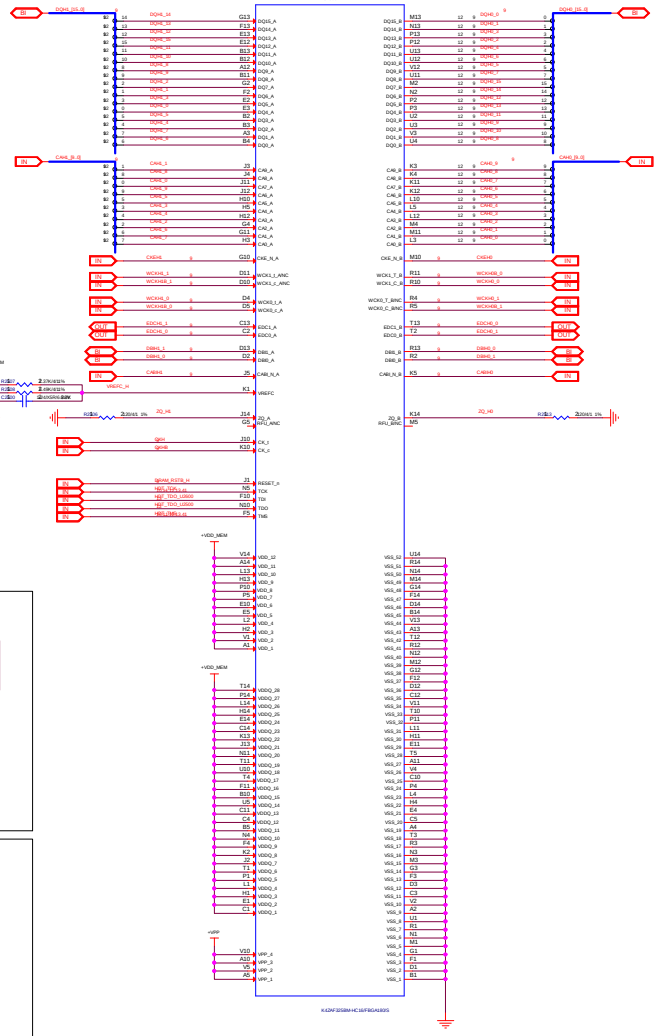
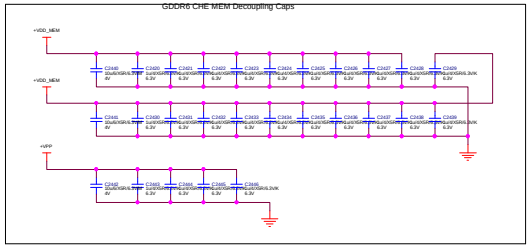
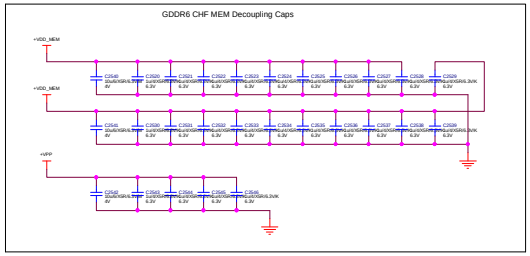
ASIC CH1 -> MEM CHA



GDDR6 CHE MEM Decoupling Caps



GDDR6 CHF MEM Decoupling Caps



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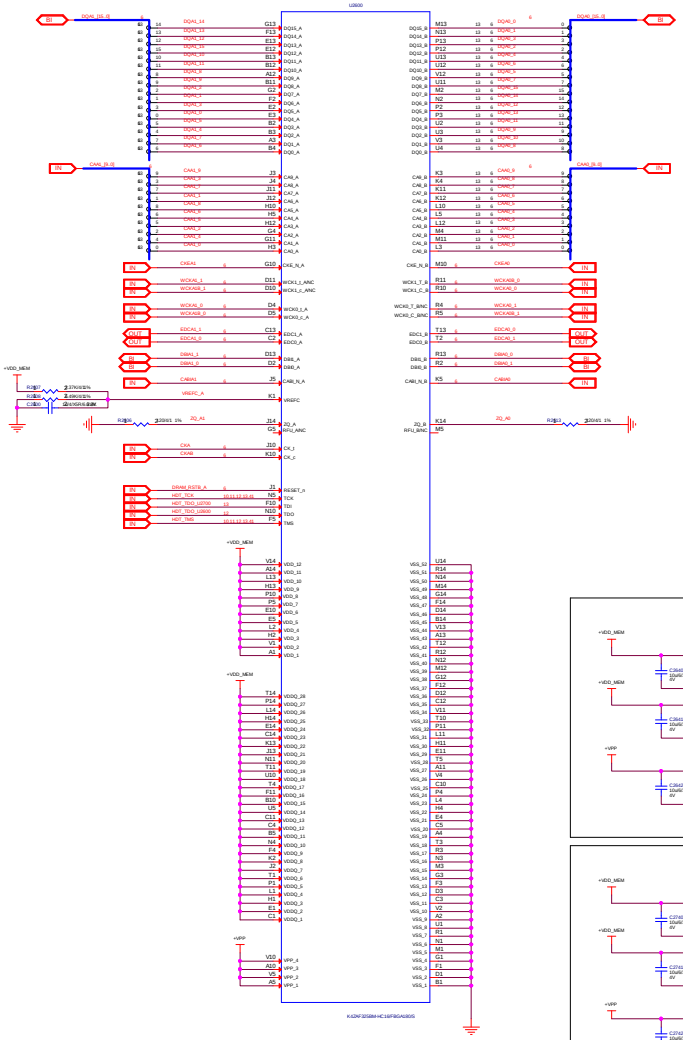

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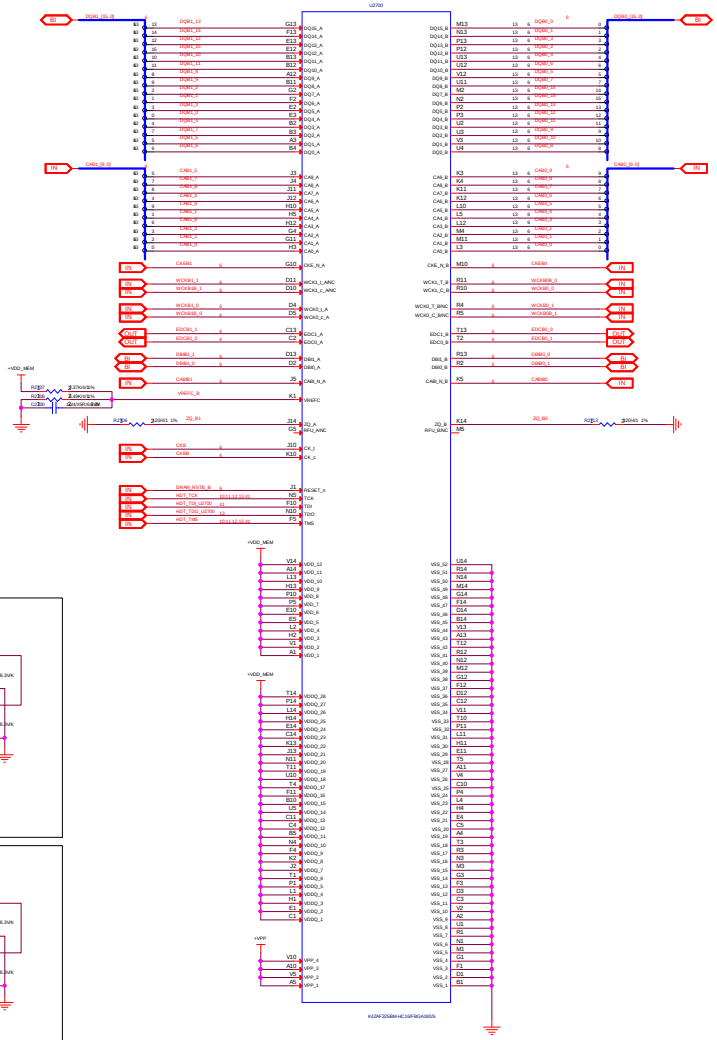

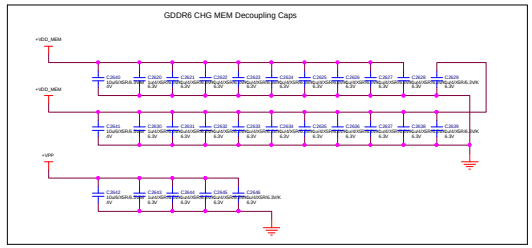

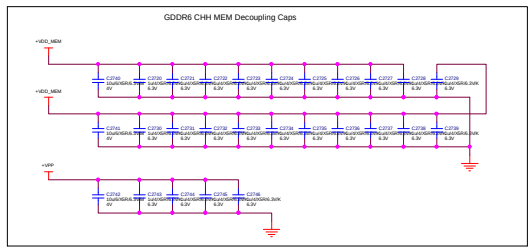

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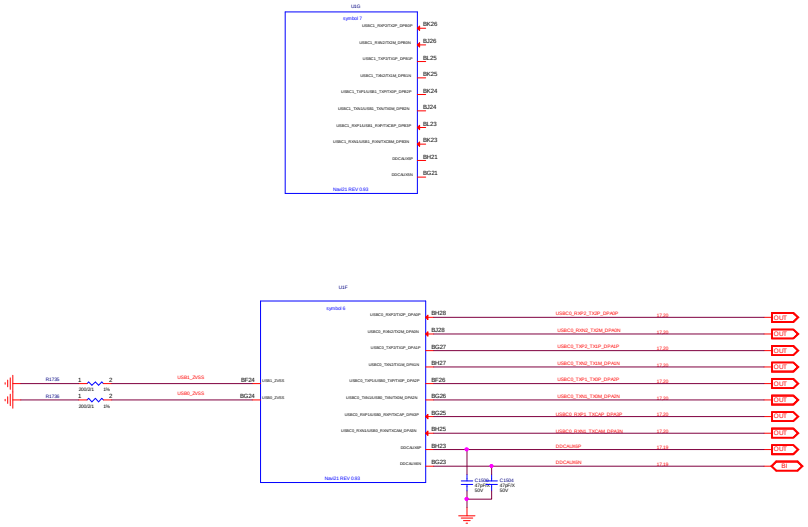
NAVI21 TMDP A/B



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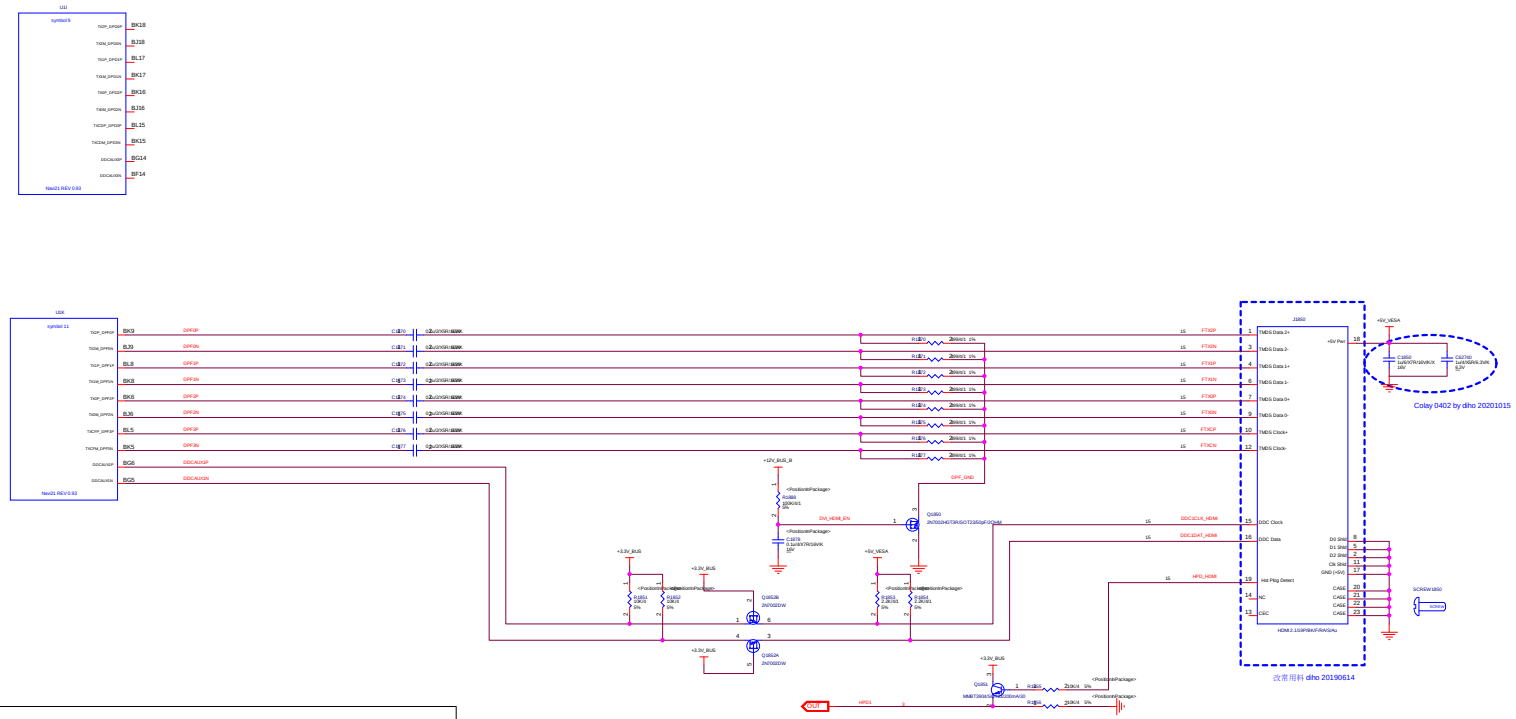

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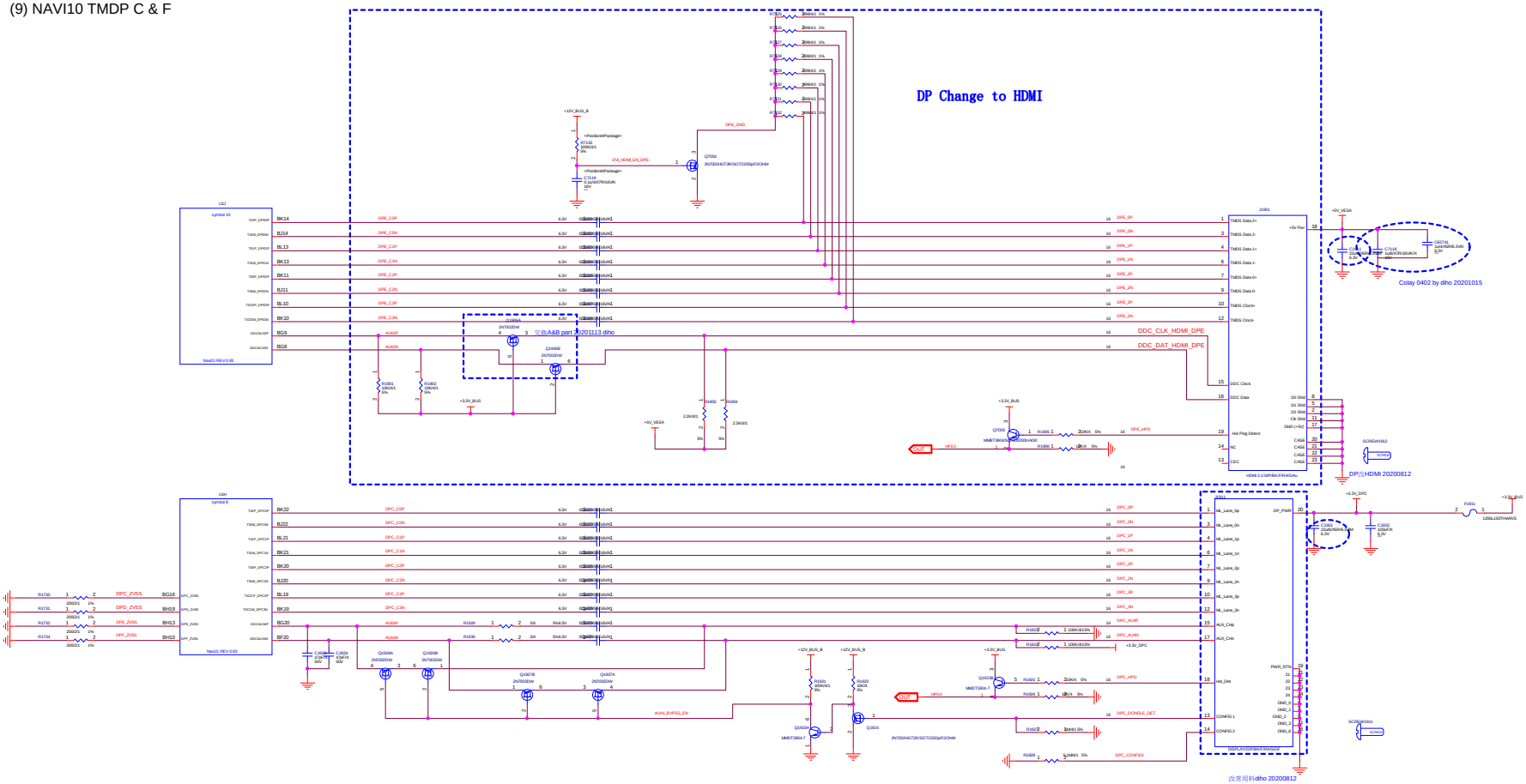
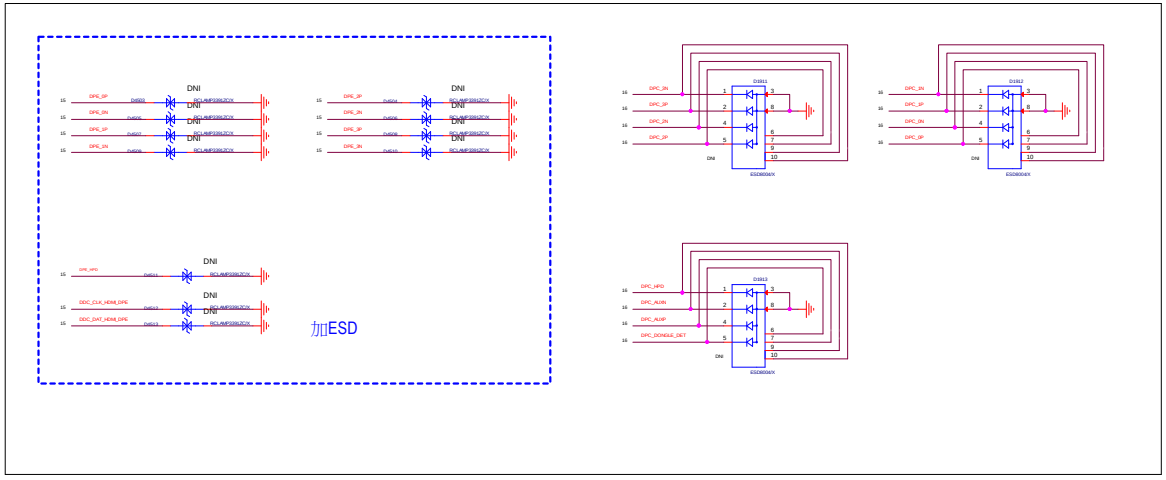
(9) NAVI10 TMDP C & F





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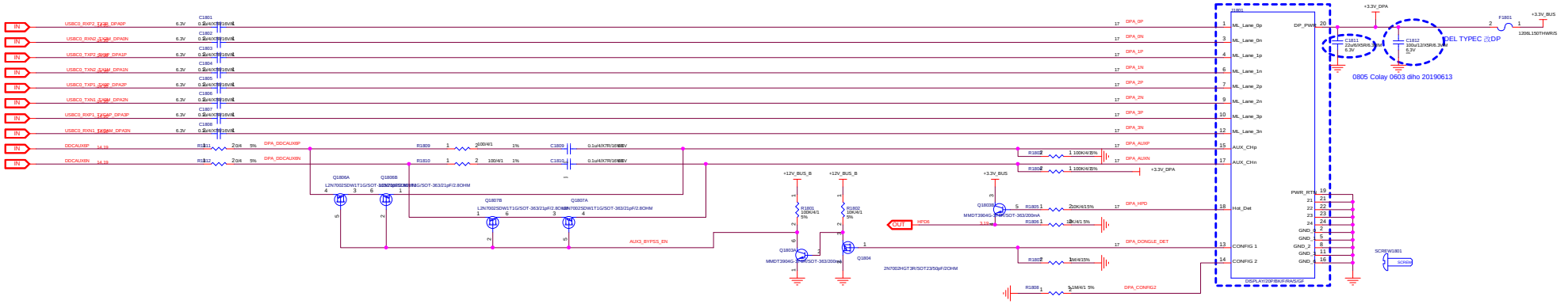

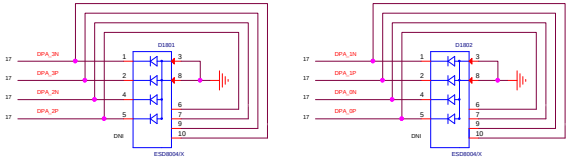

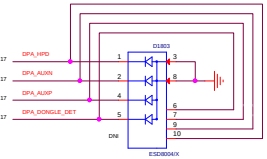

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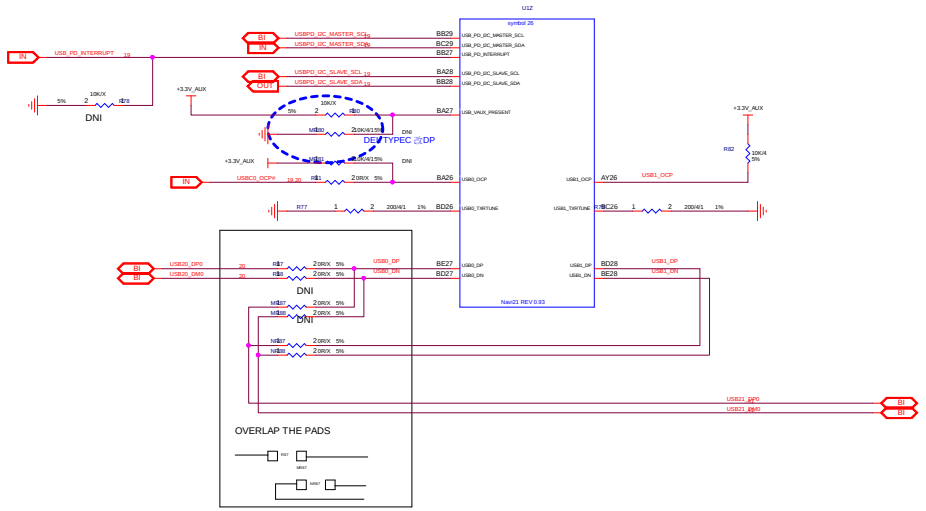

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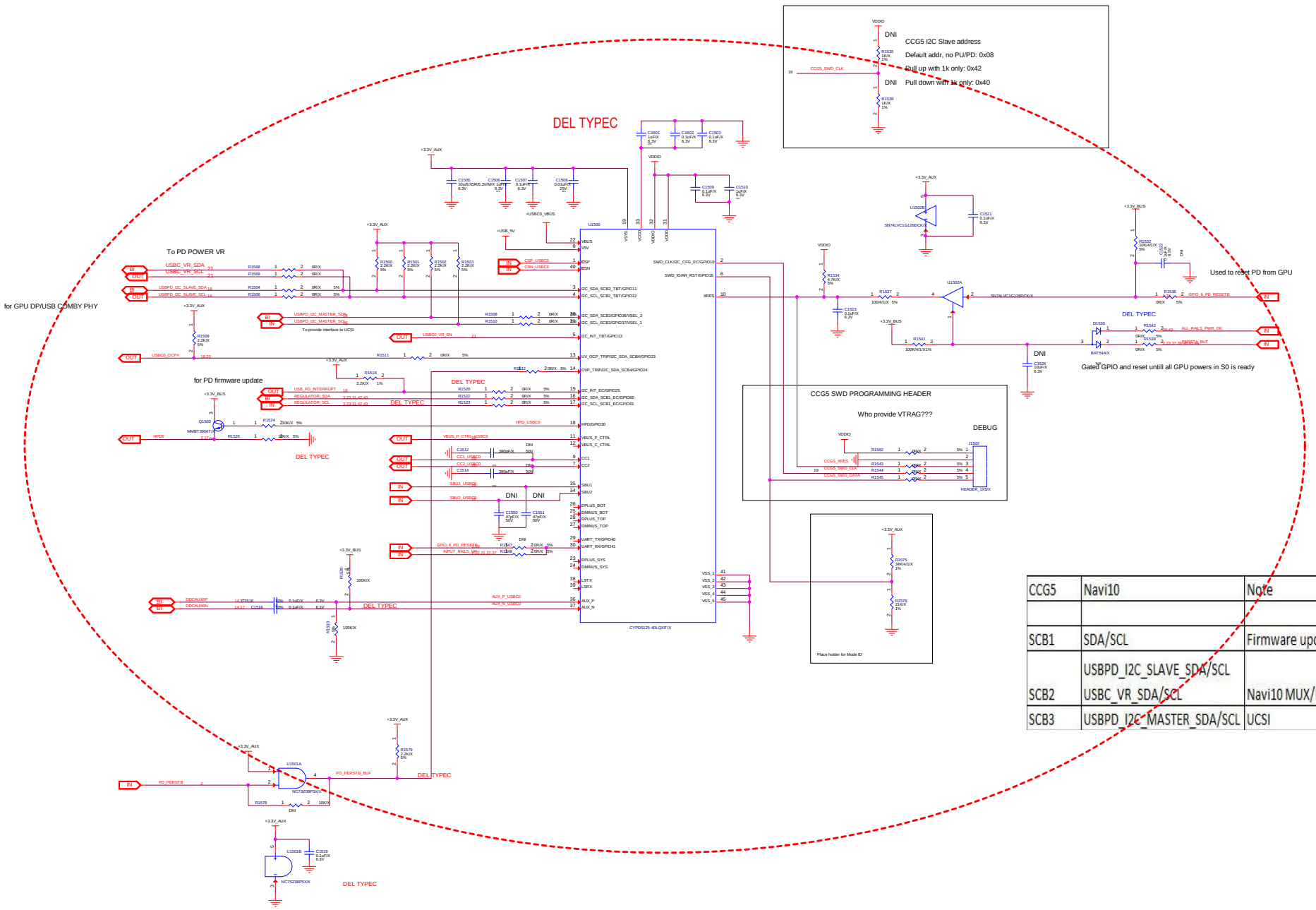

CCG5	Navi10	Note
SCB1	SDA/SCL	Firmware update/SMU
SCB2	USBPD_I2C_SLAVE_SDA/SCL USBC_VR_SDA/SCL	Navi10 MUX/PD_Regulator/re-driver
SCB3	USBPD_I2C_MASTER_SDA/SCL	UCSI

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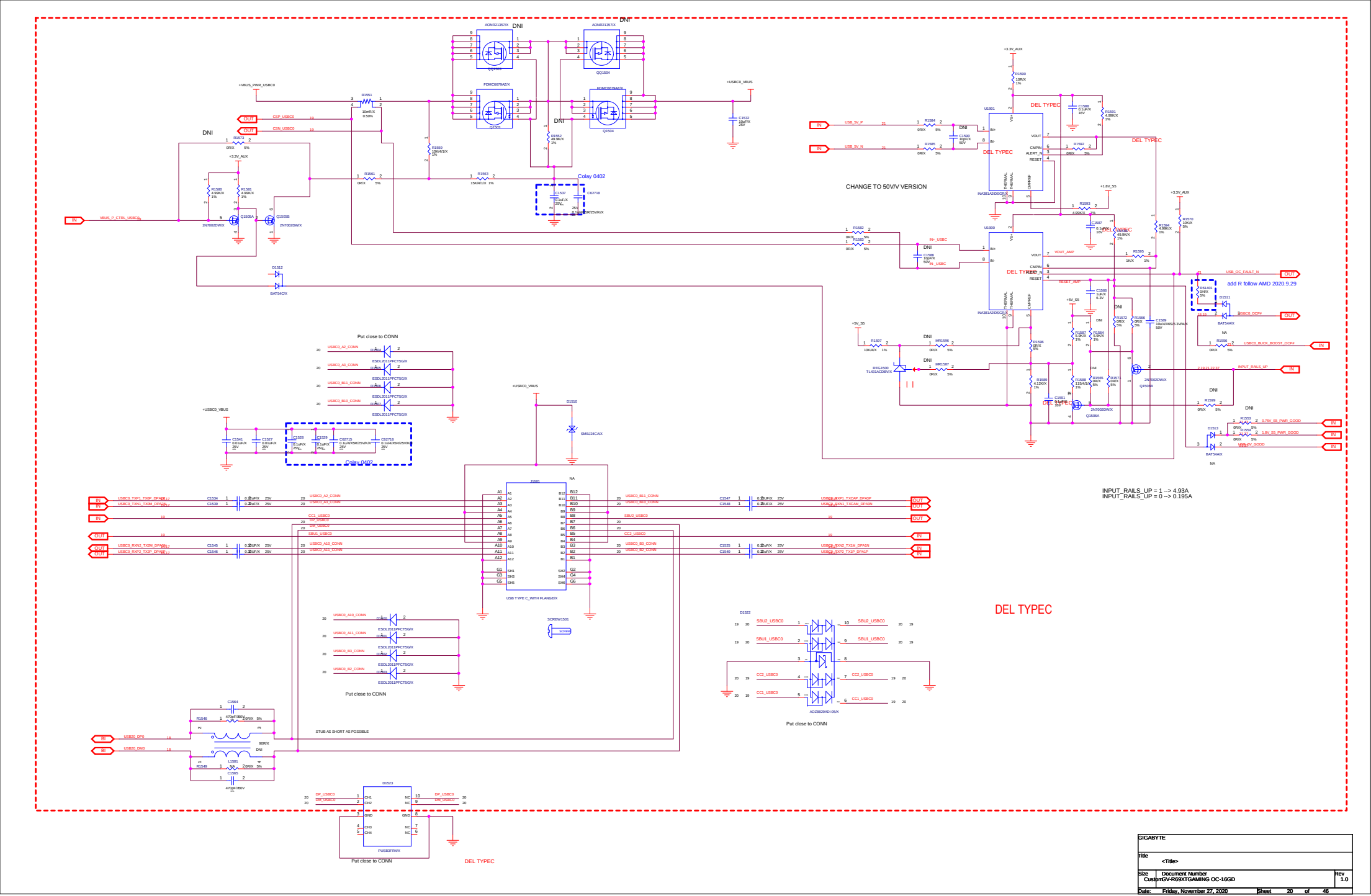

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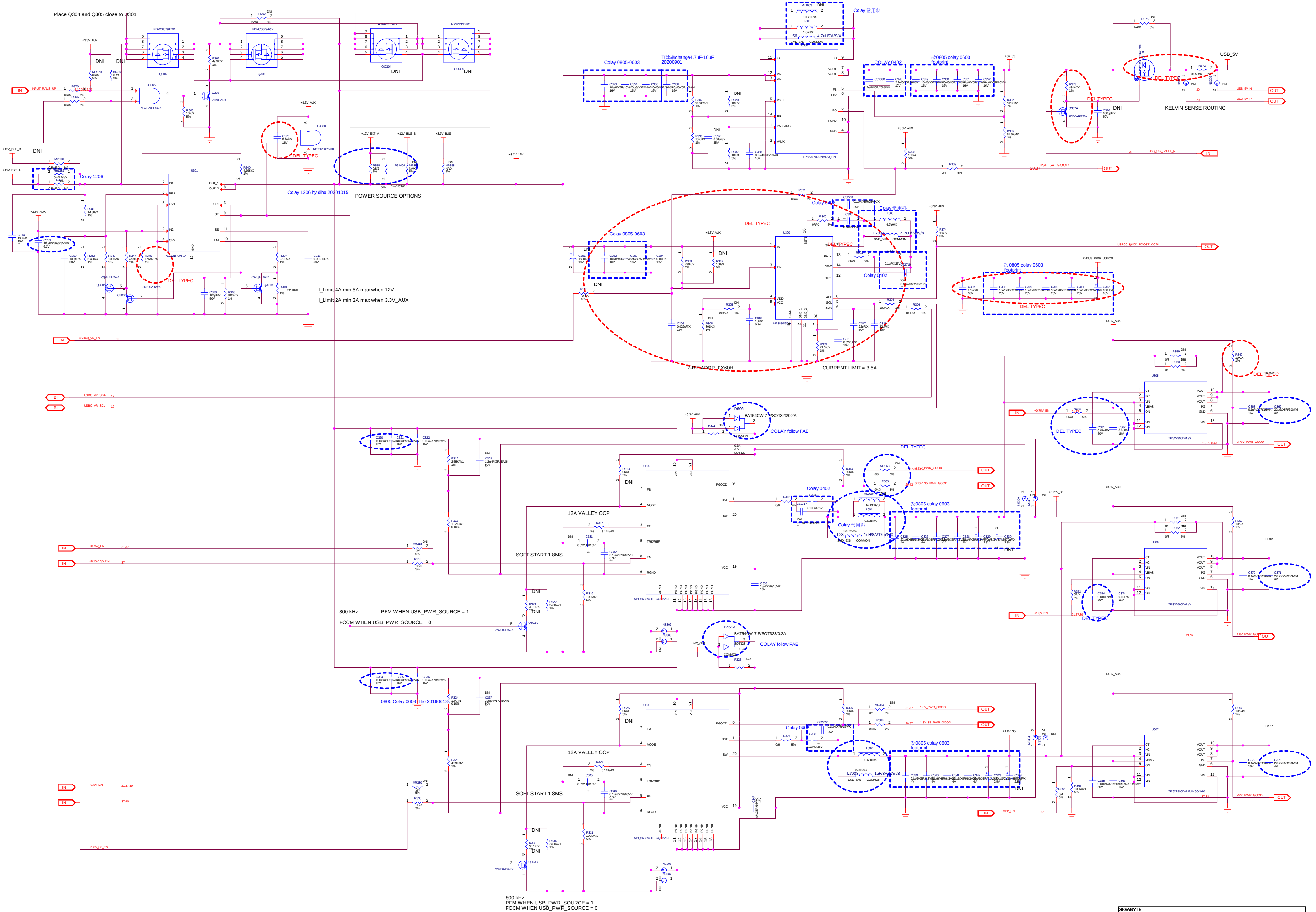

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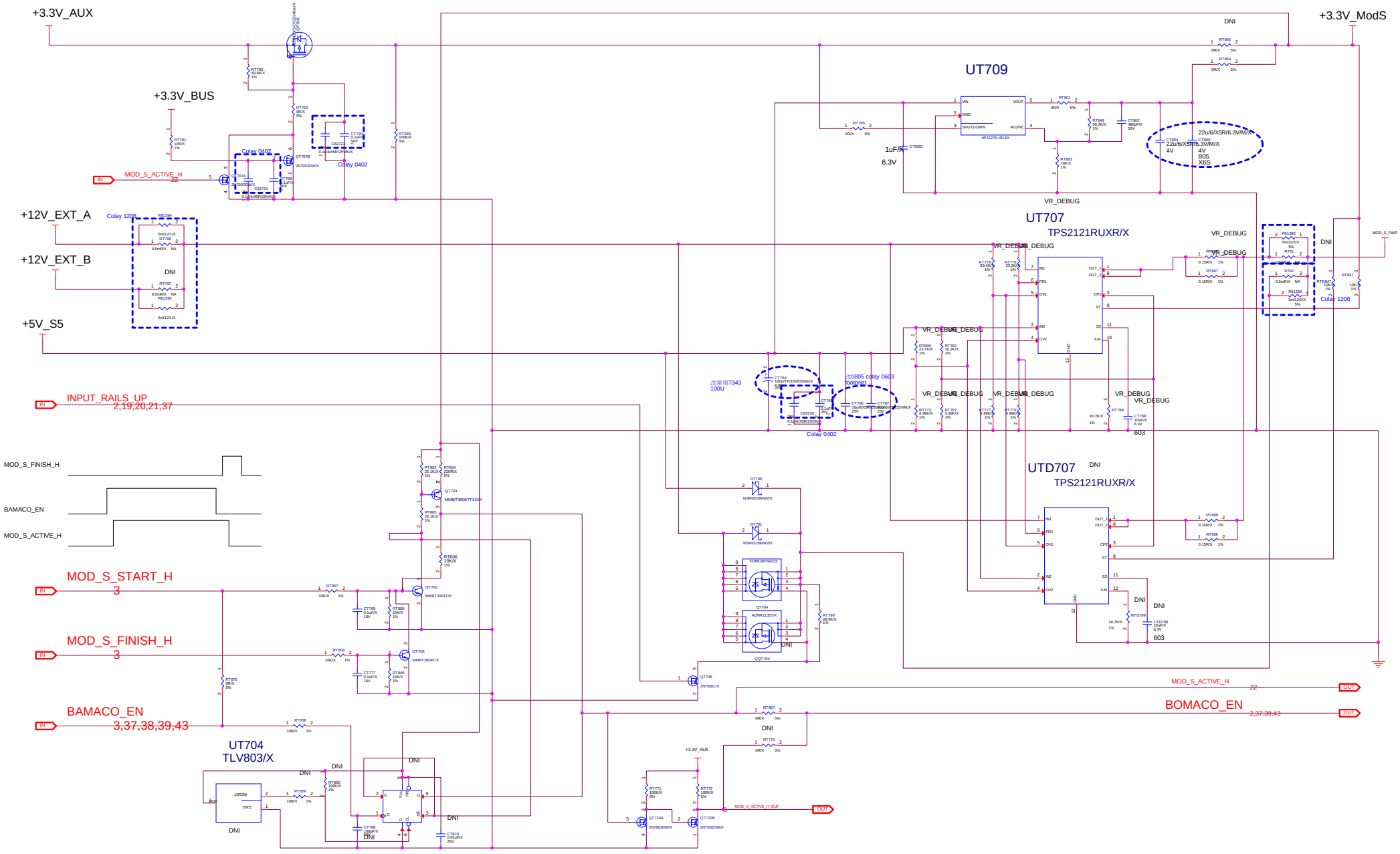
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+3.3V_BUS
+12V_EXT_A
+12V_EXT_B
+5V_S5
+3.3V_ModS
UT709
UT707
TPS2121RUXR/X
UTD707
TPS2121RUXR/X
UT704
TLV803/X
UT701
NC7SZ74K8X/X
DNI
VR_DEBUG
Colay 0402
Colay 1206
MOD_S_ACTIVE_H
22
INPUT_RAILS_UP
2,19,20,21,37
MOD_S_FINISH_H
BAMACO_EN
MOD_S_START_H
3
MOD_S_FINISH_H
3
BAMACO_EN
3,37,38,39,43
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BOMACO_EN
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MOD_S_ACTIVE_H_BUF
MOD_S_PWR
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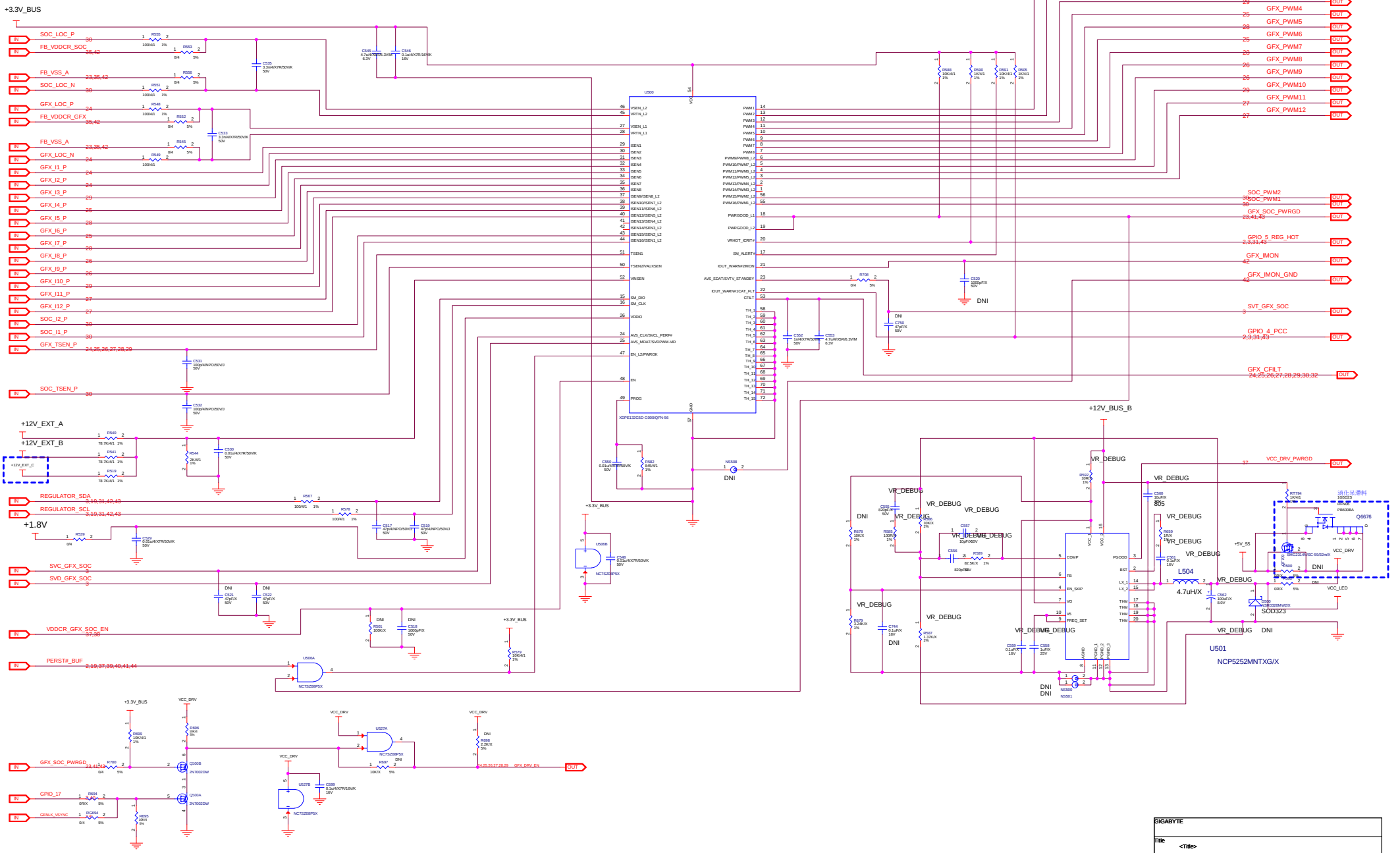
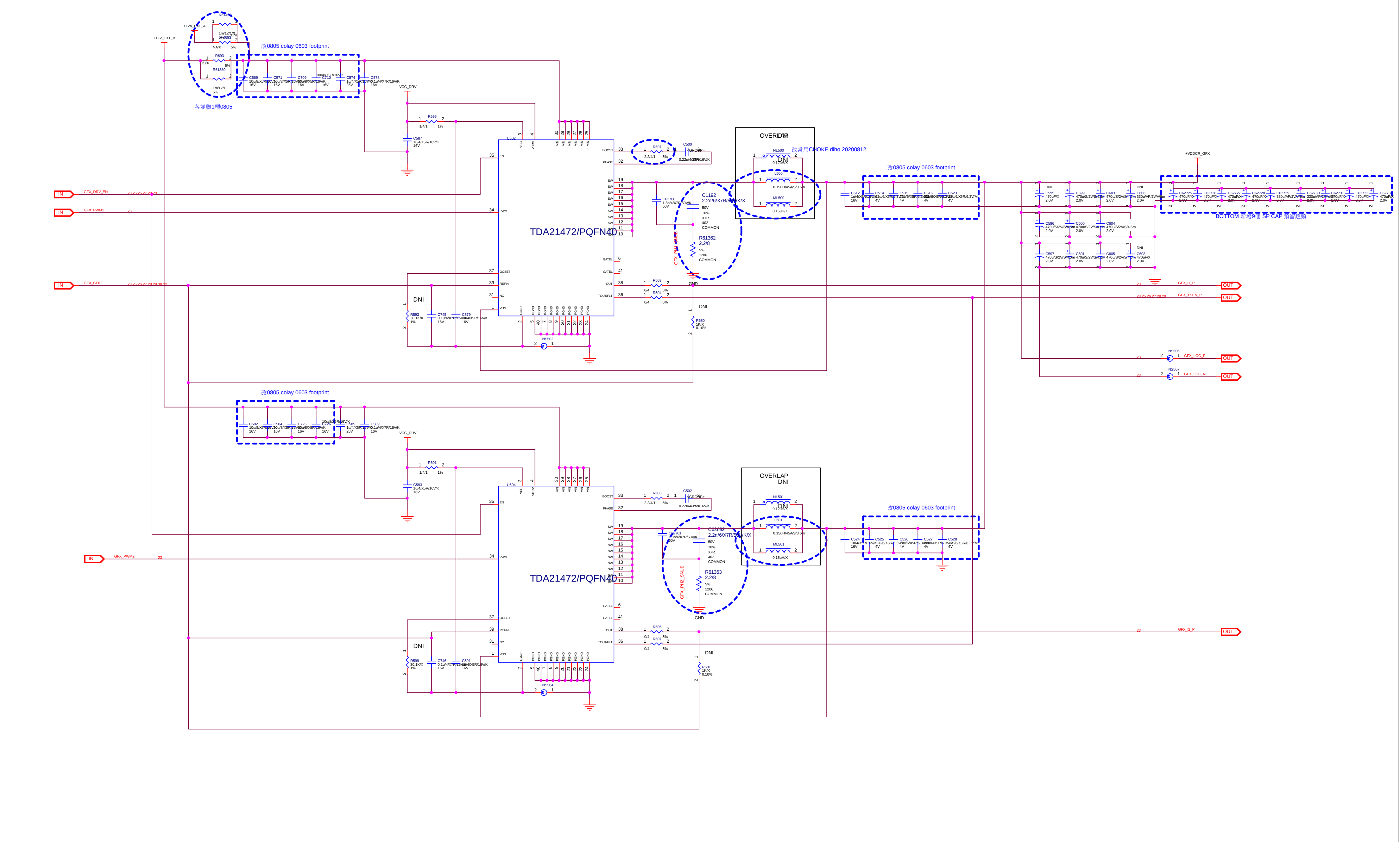
(14) GFX & SOC CONTROLLER





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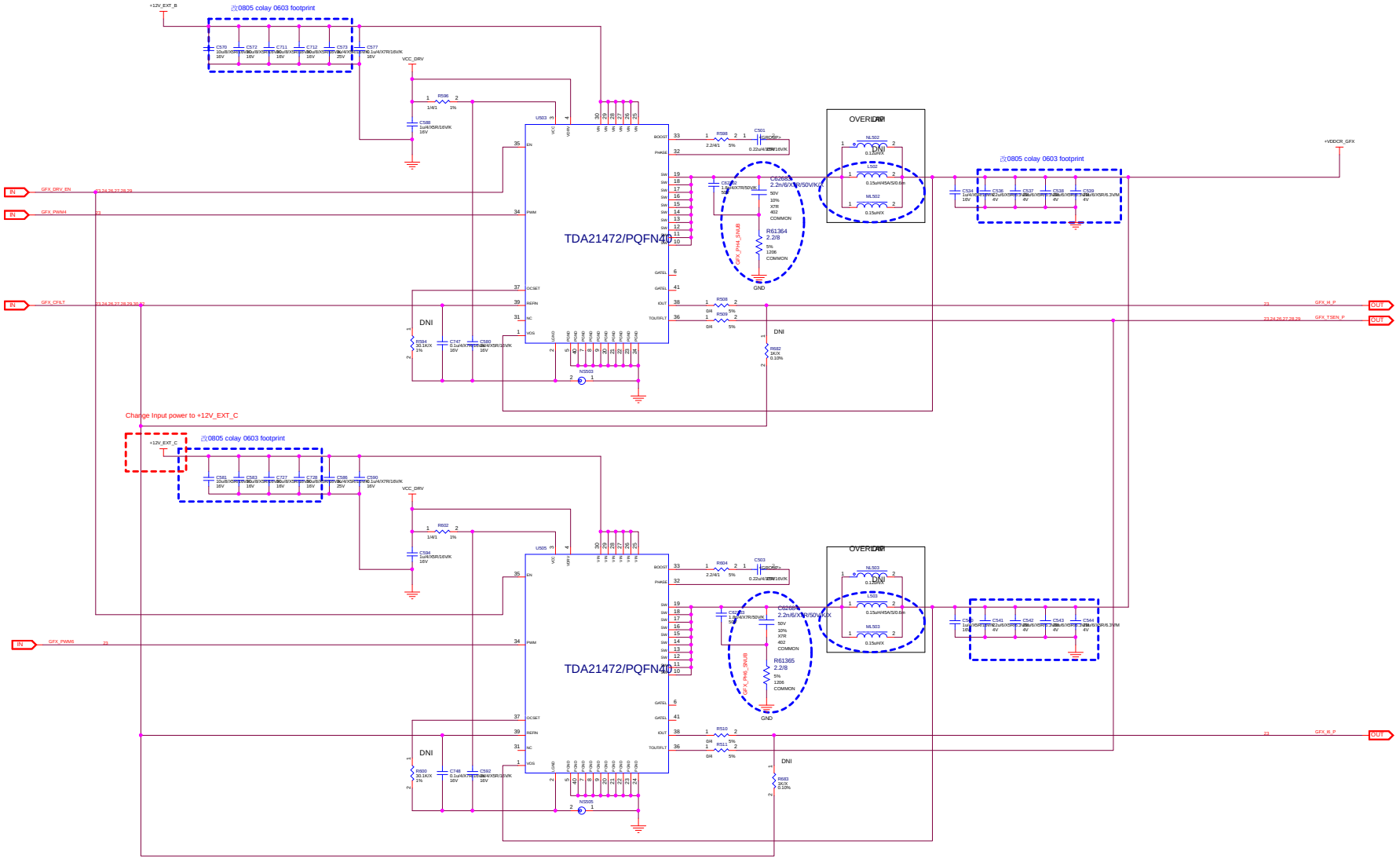

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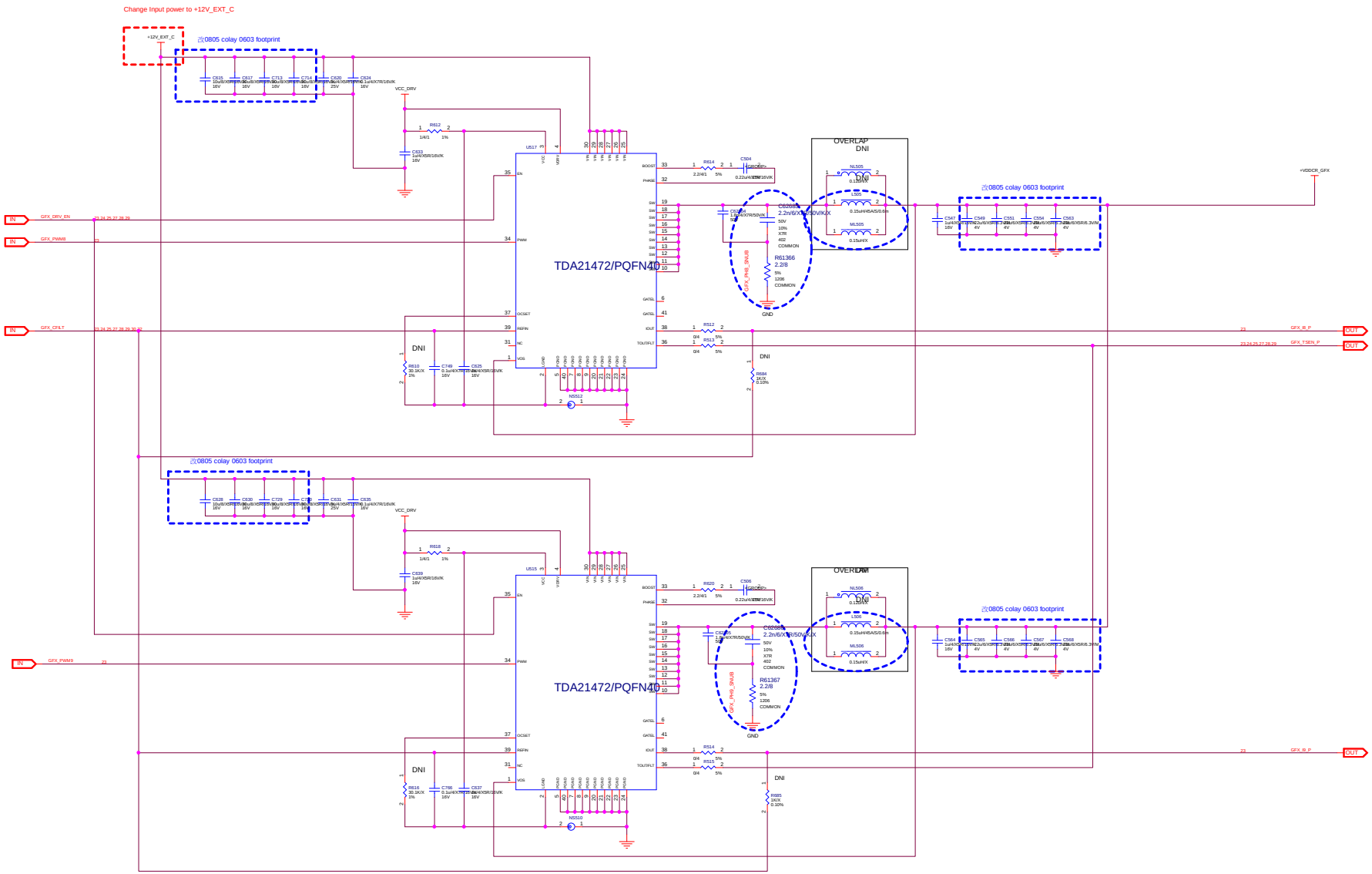

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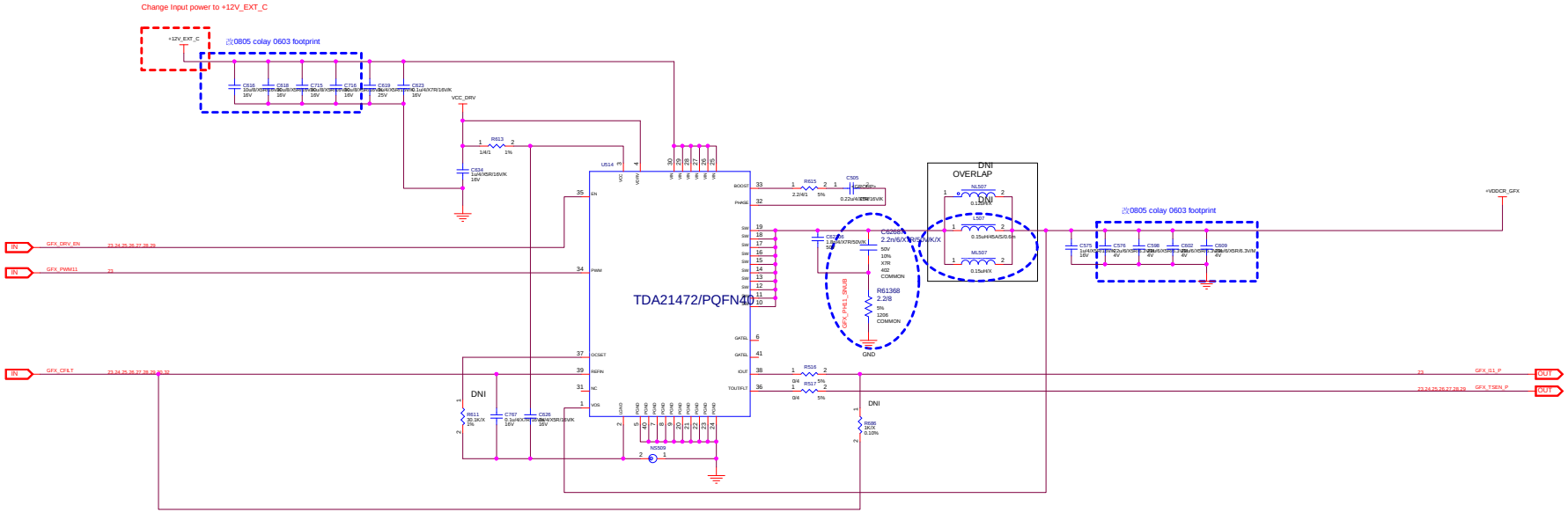

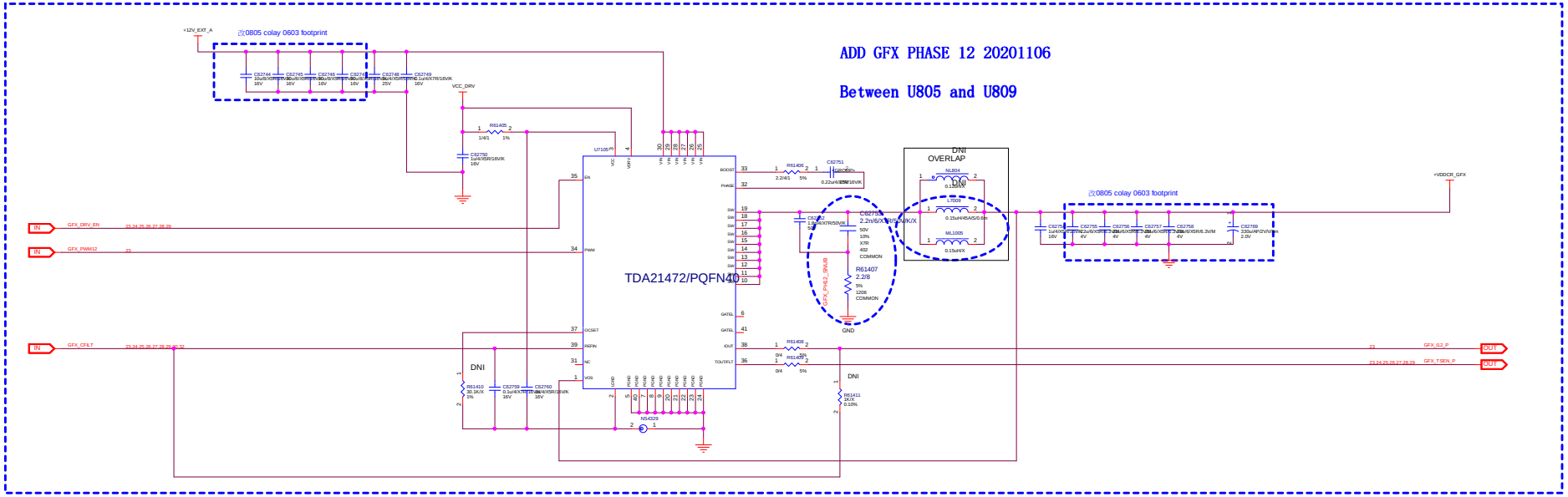

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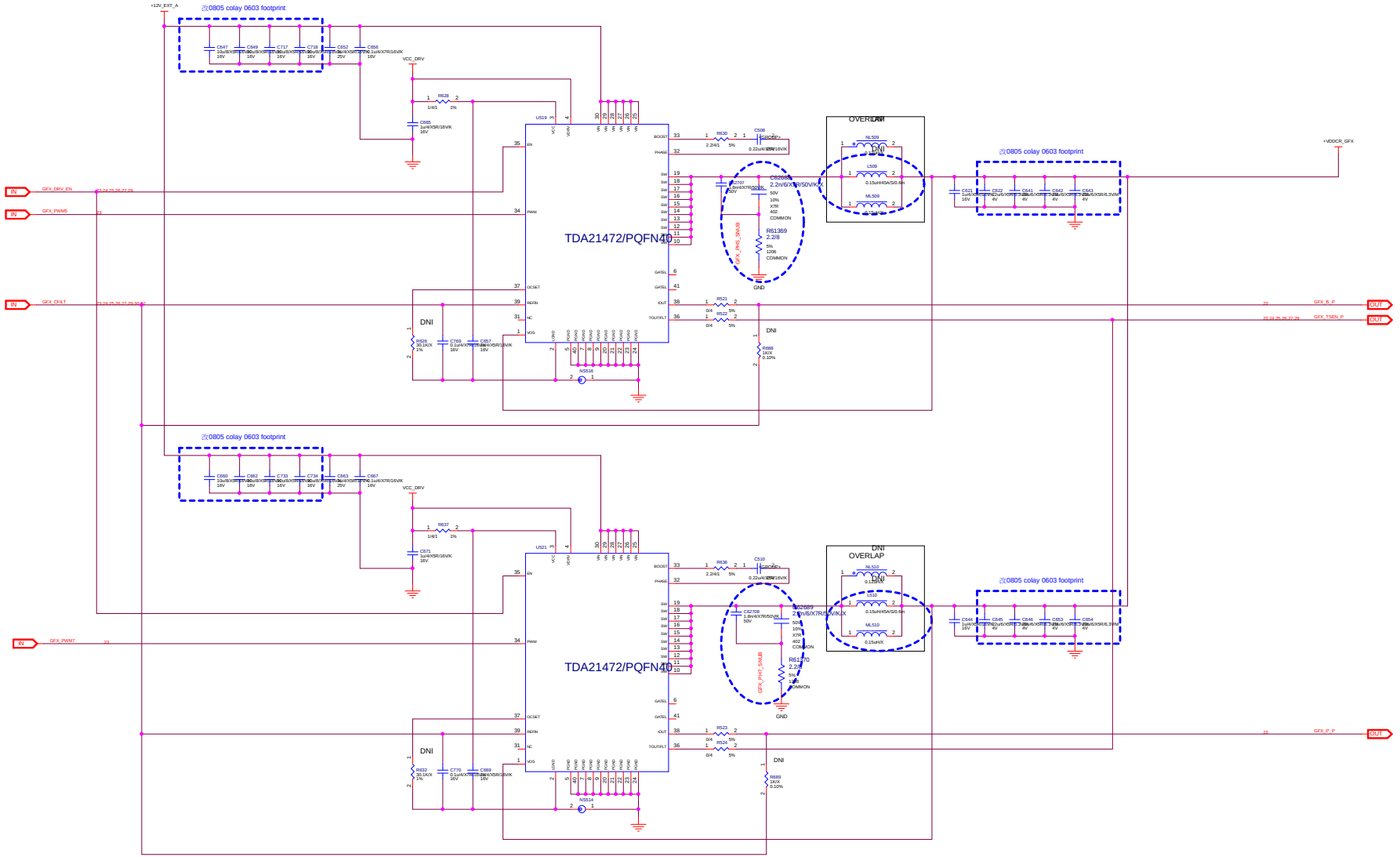

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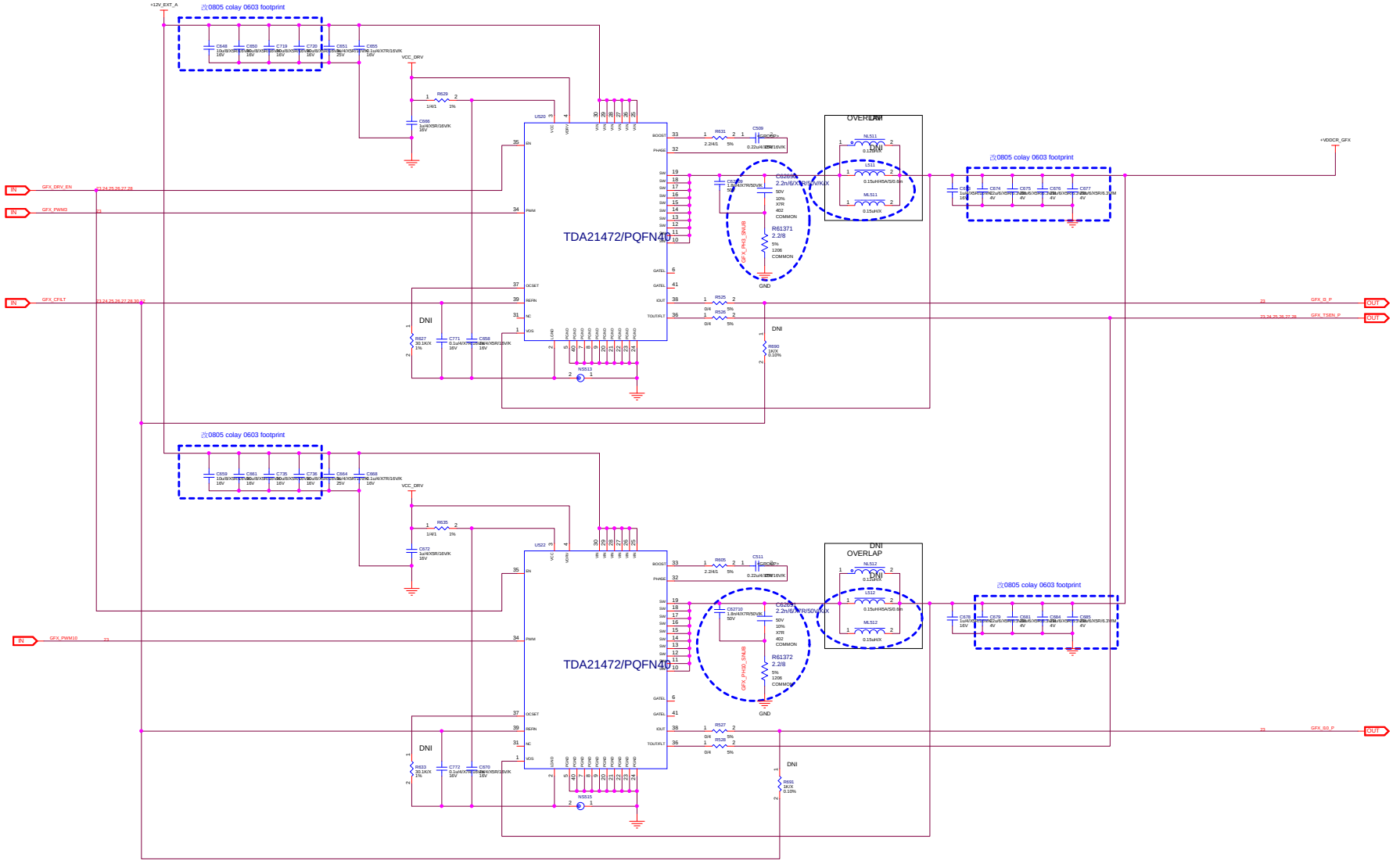

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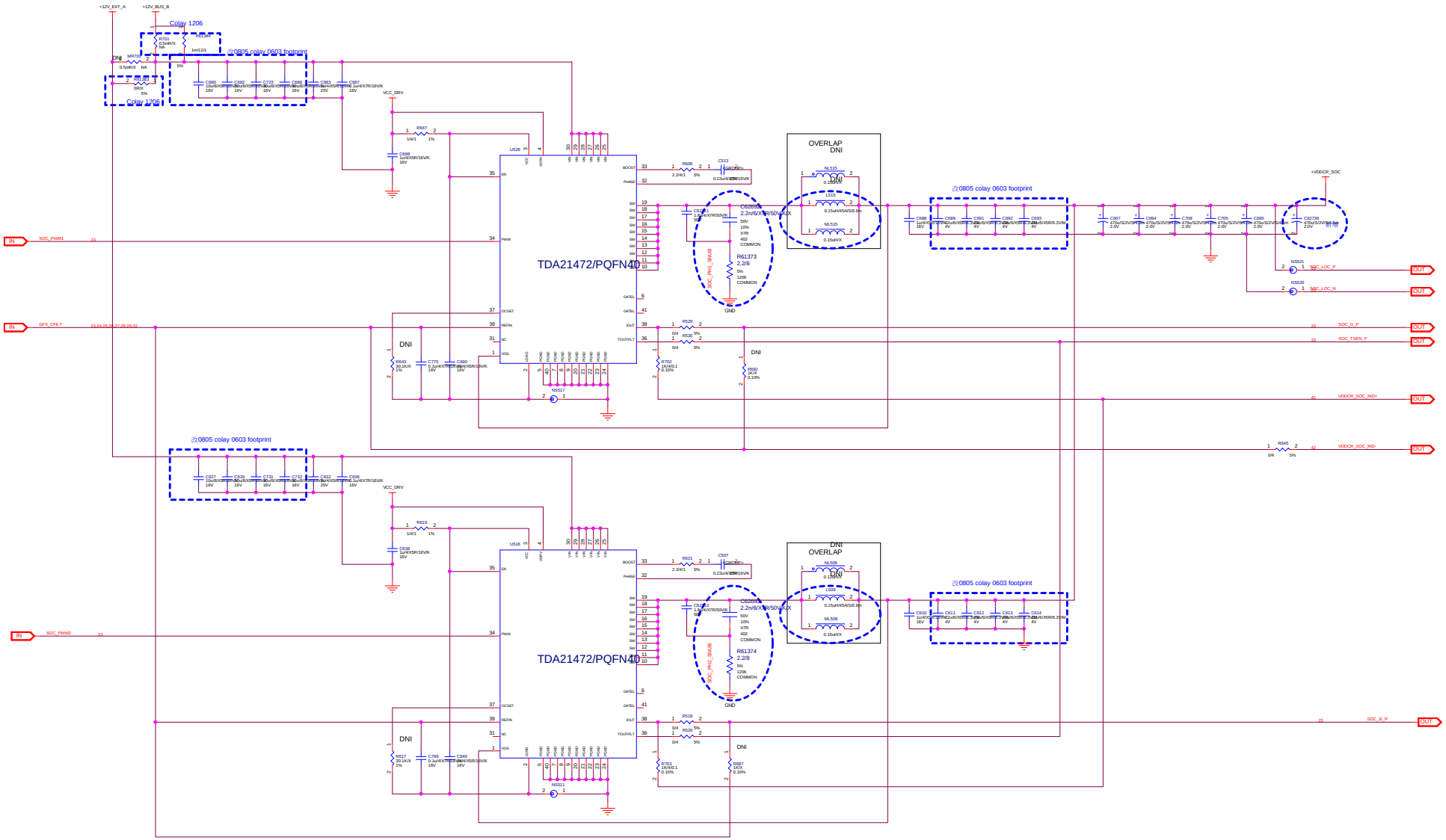

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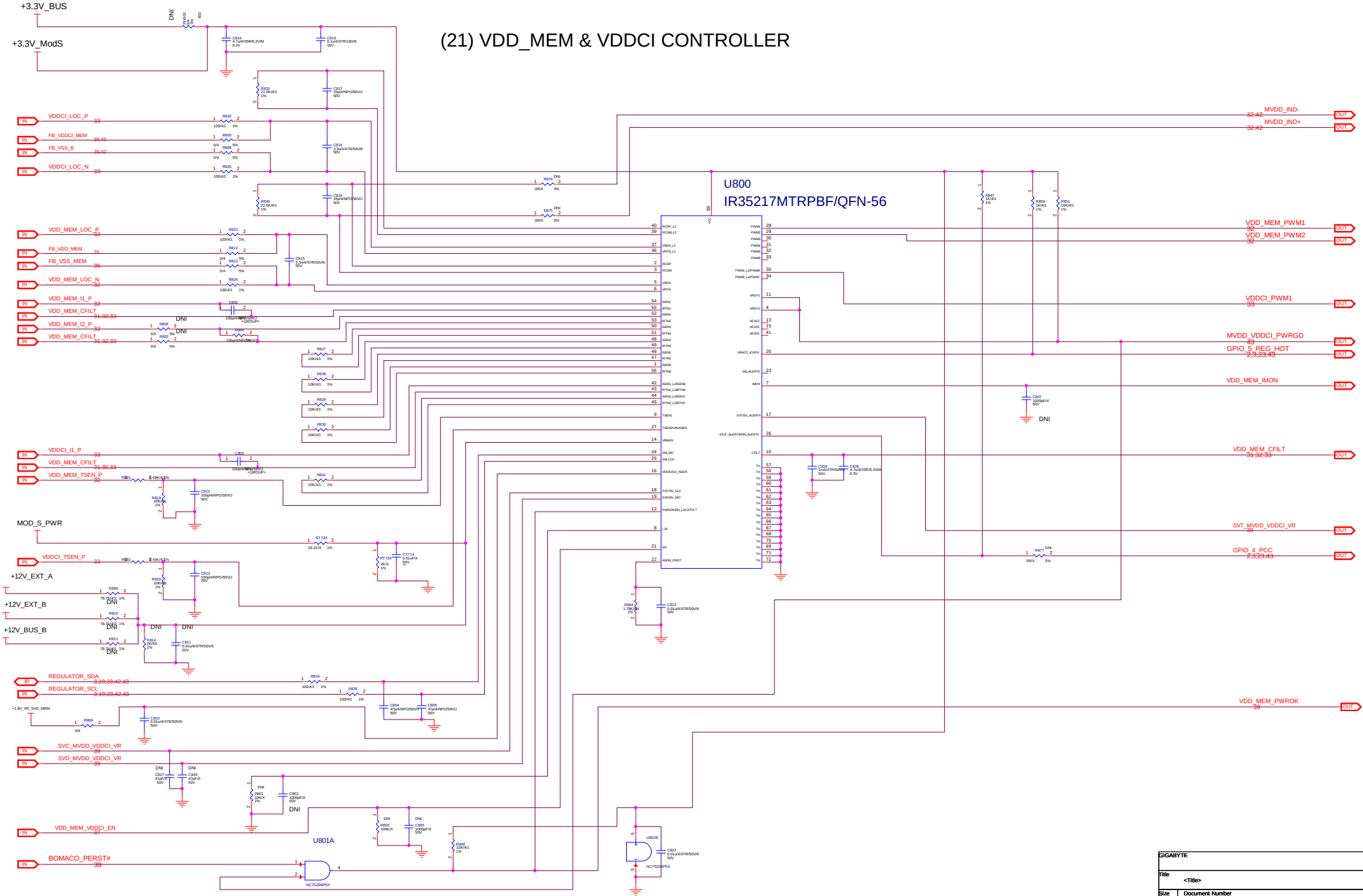
(21) VDD_MEM & VDDCI CONTROLLER



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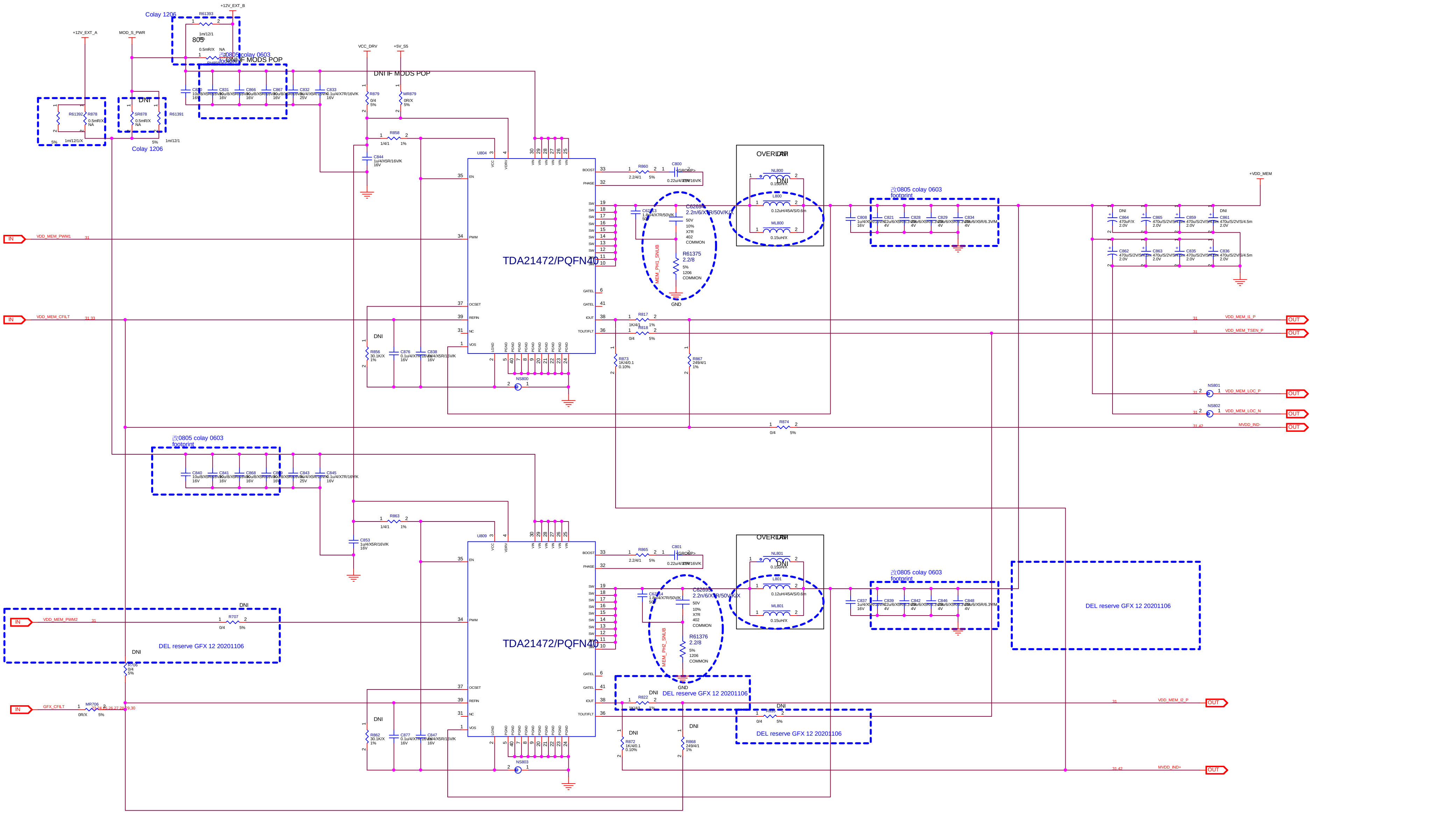

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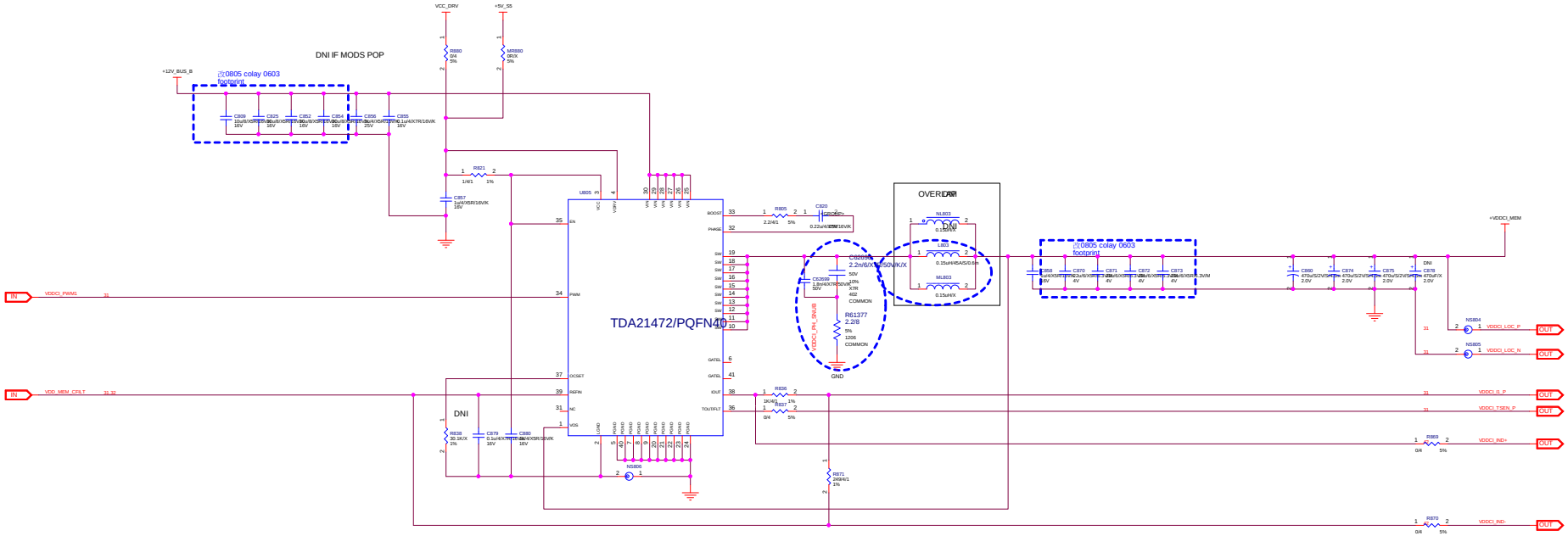

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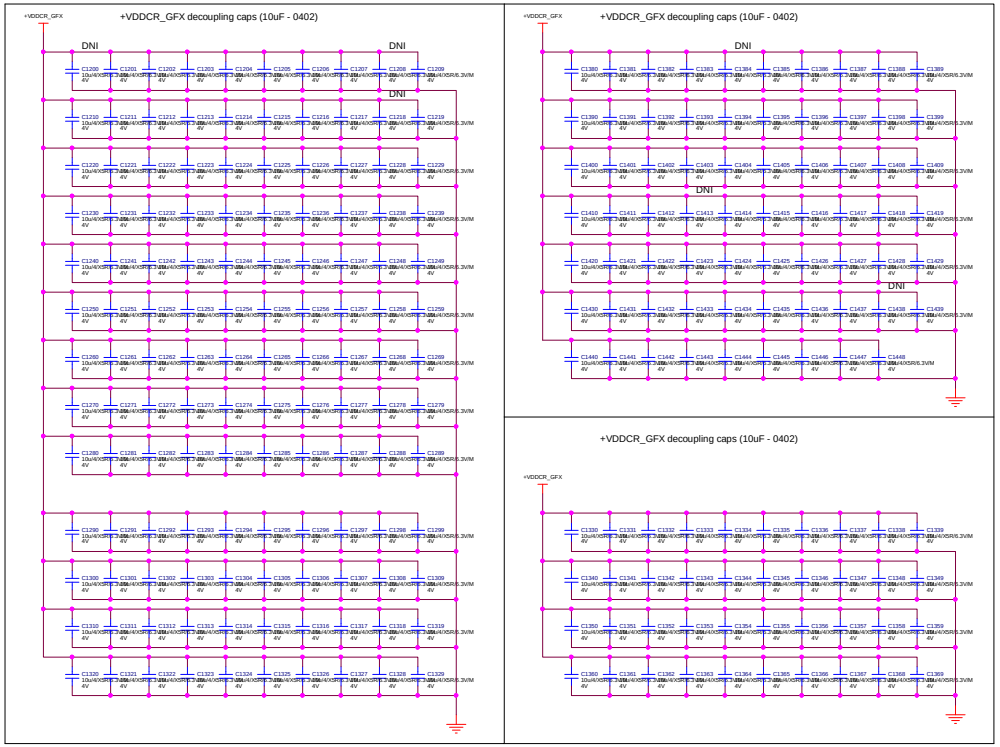
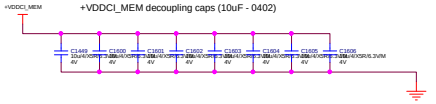
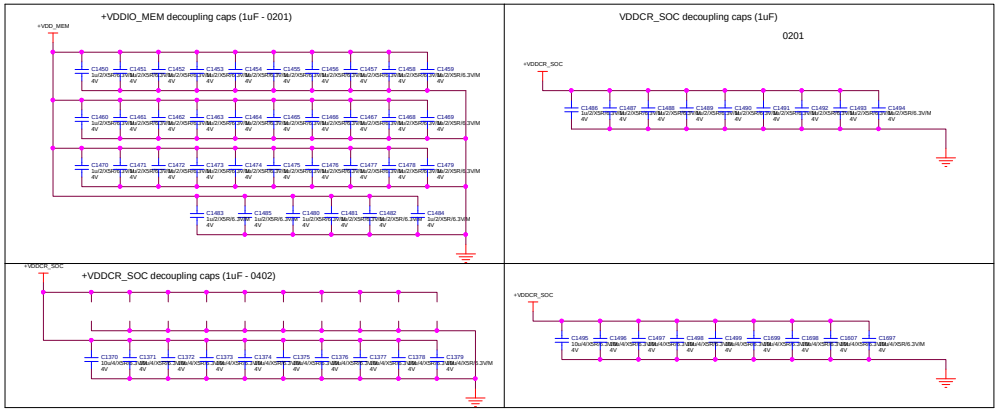
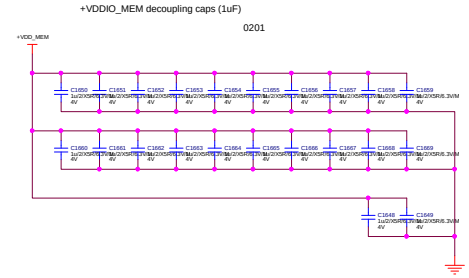


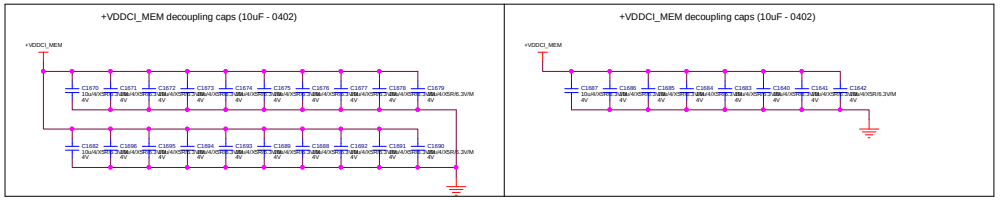


DNI these six caps to match SLT board and keep the design consistent across SKUs

C1218
C1208
C1200
C1438
C1413
C1384







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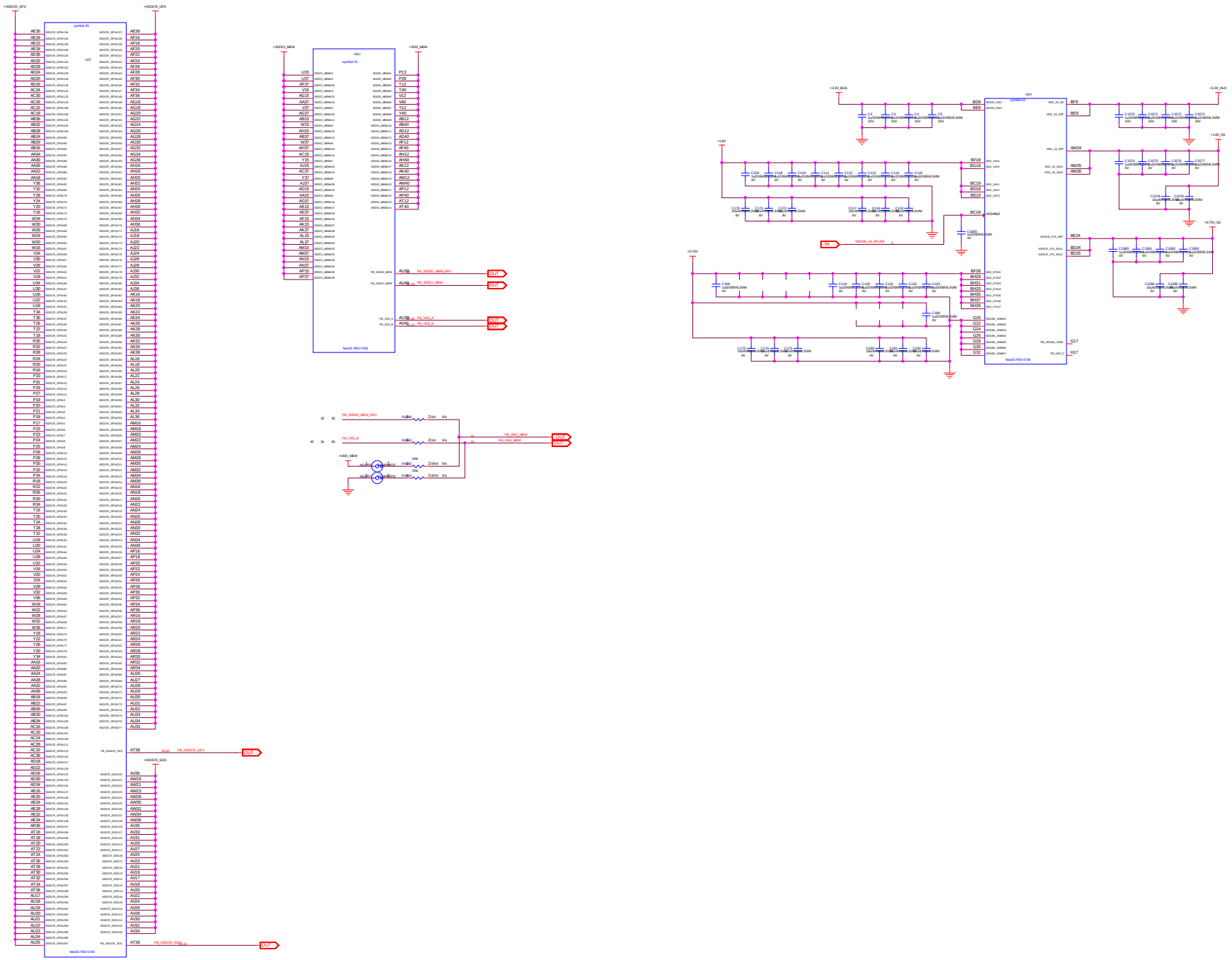
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+VDDCR_SOC
+VDDCI_MEM
+VDD_MEM
+3.3V_BUS
+3.3V_AUX
+1.8V
+1.8V_SS
+0.75V
+0.75V_SS
FB_VDDCR_GFX
FB_VDDCR_SOC
FB_VDDCI_MEM_GPU
FB_VDDCI_MEM
FB_VSS_A
FB_VSS_B
FB_VDD_MEM
FB_VSS_MEM
OUT
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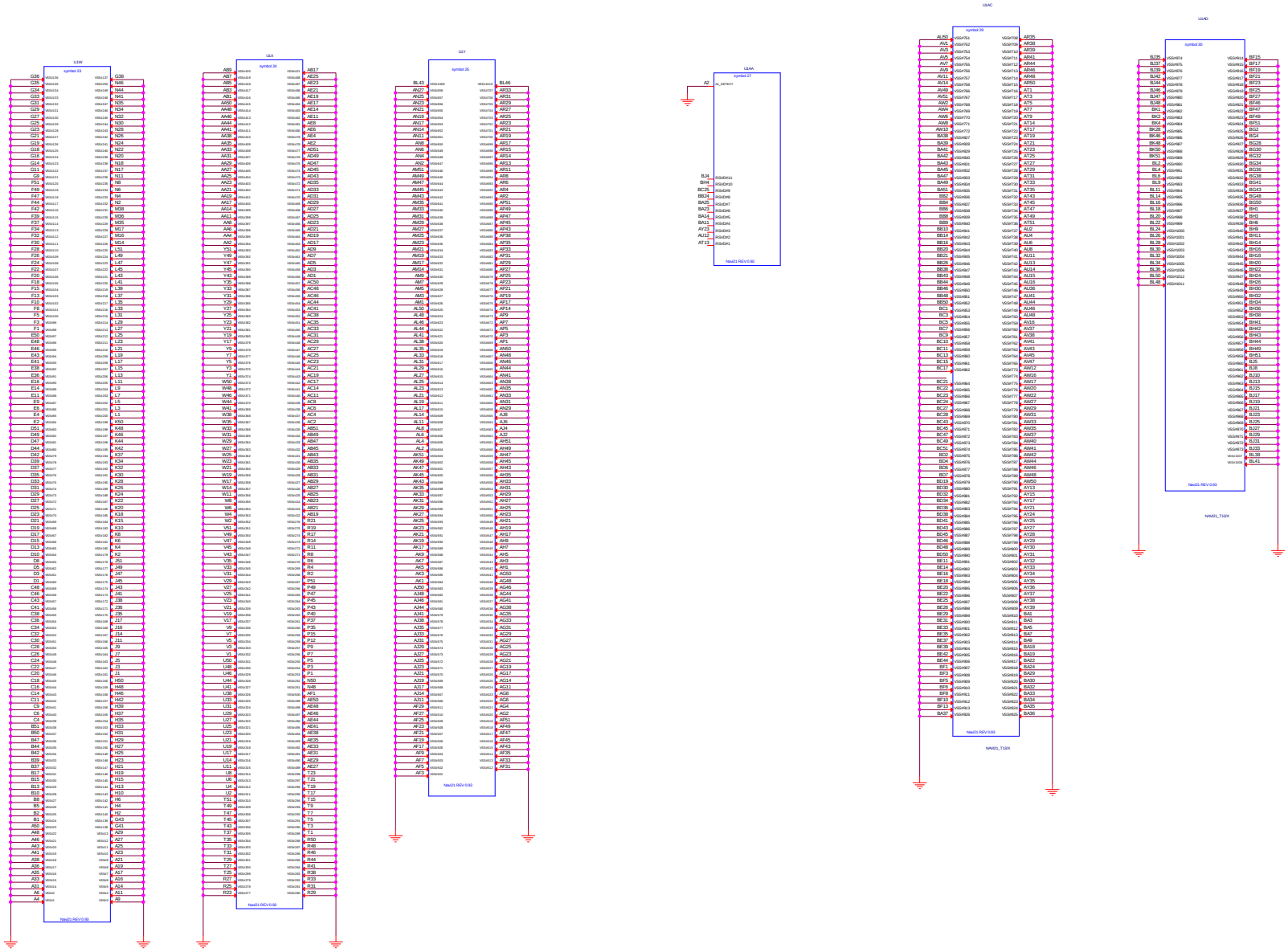

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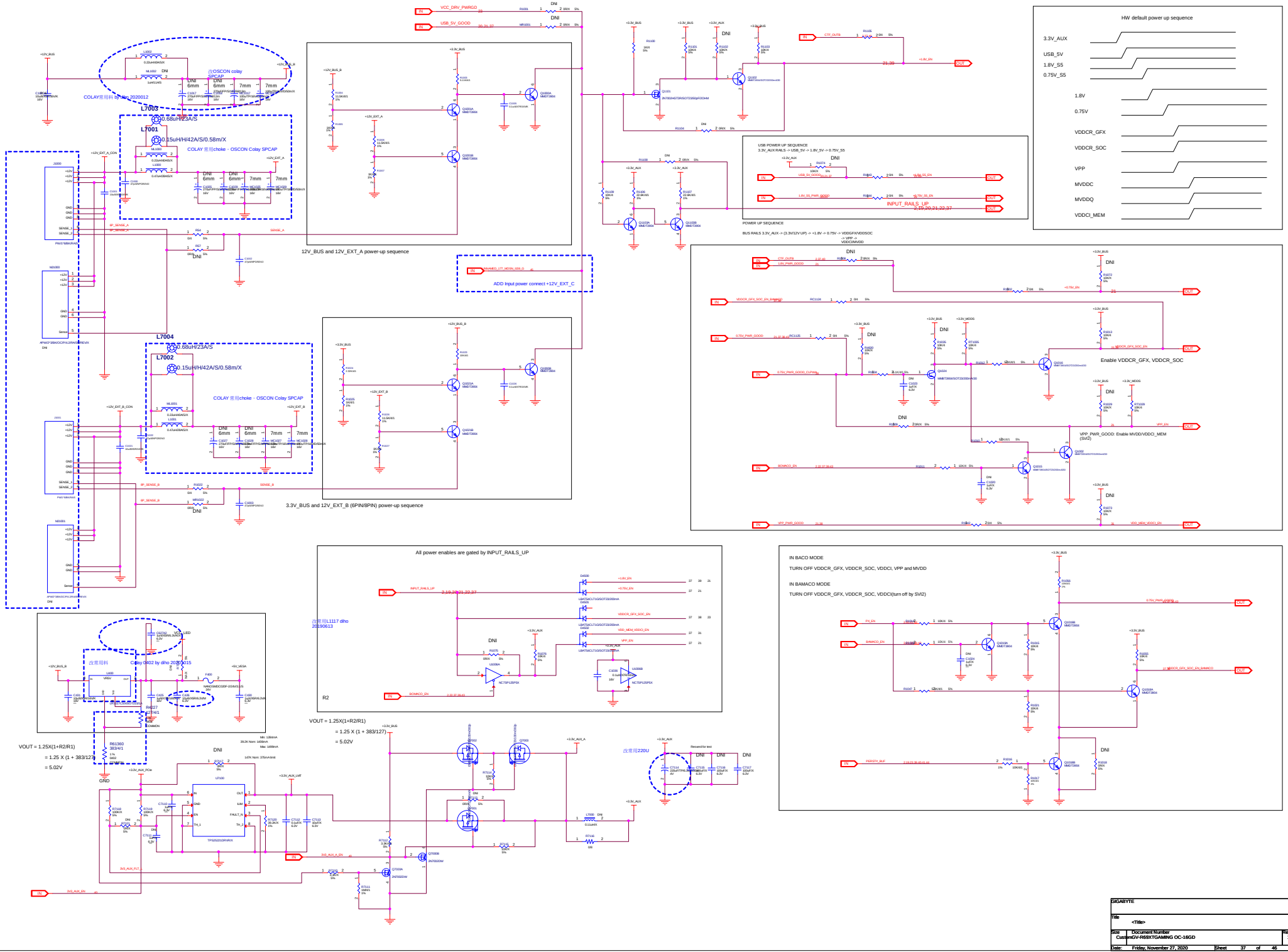

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GFX/SOC and VPP enable

GFX/SOC EN in BAMACO

CL_DEBUG

CL_DEBUG

INVERTER

INVERTER

AND

OR

OR

AND

AND

Figure 10. 2-input NAND gate with input A inverted or 2-input OR gate with input C inverted

Figure 11. 2-input NOR gate with input B inverted or 2-input AND gate with input C inverted

Figure 12. 2-input OR gate

Figure 13. Inverter

Figure 14. Buffer

Figure 8. 2-input MUX

Figure 9. 2-input AND gate

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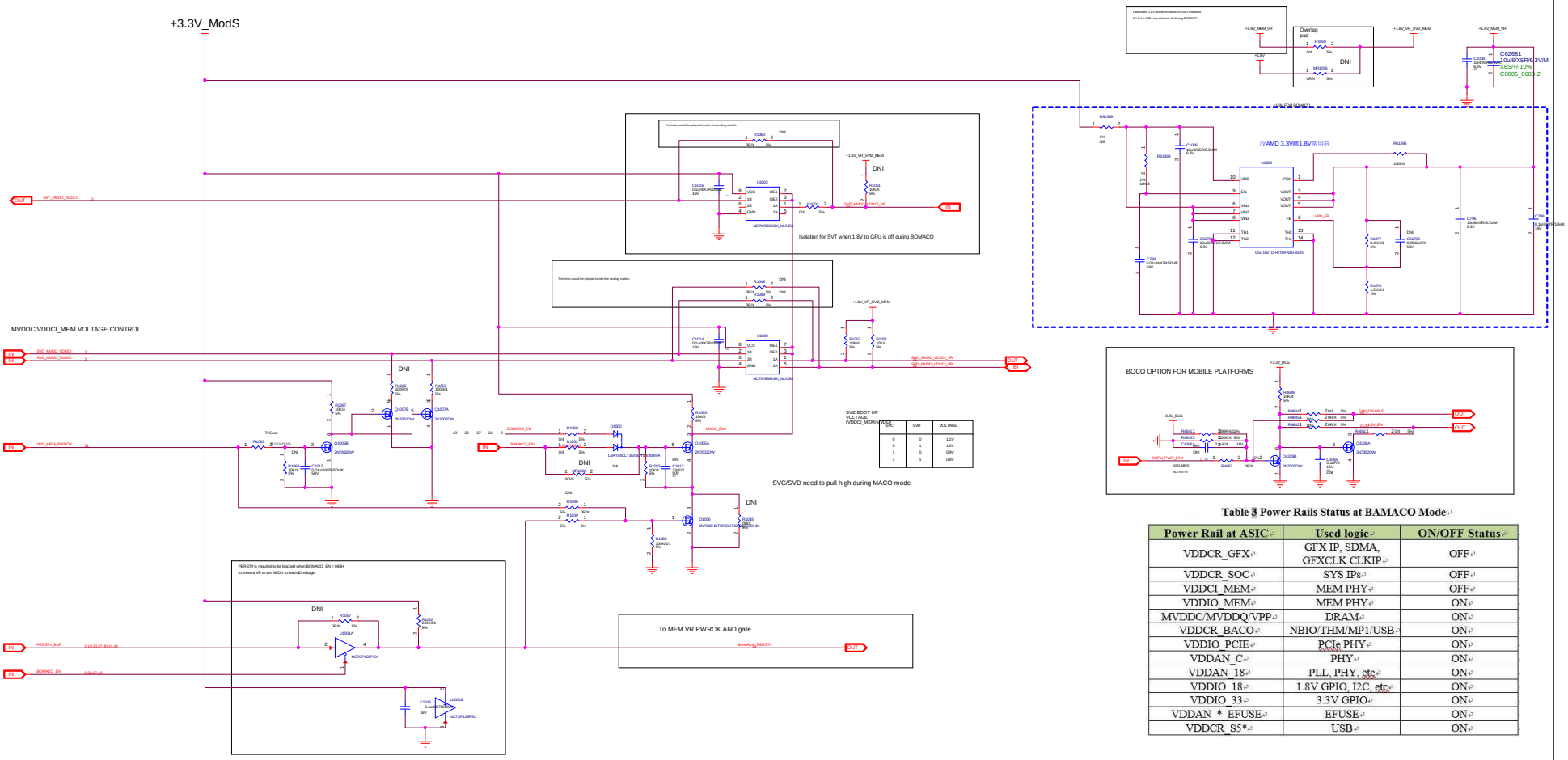

Table 3 Power Rails Status at BAMACO Mode

Power Rail at ASIC	Used logic	ON/OFF Status
VDDCR_GFX	GFX IP, SDMA, GFXCLK CLKIP	OFF
VDDCR_SOC	SYS IPs	OFF
VDDCI_MEM	MEM PHY	OFF
VDDIO_MEM	MEM PHY	ON
MVDDC/MVDDQ/VPP	DRAM	ON
VDDCR_BACO	NBIO/THM/MP1/USB	ON
VDDIO_PCIE	PCIe PHY	ON
VDDAN_C	PHY	ON
VDDAN_18	PLL, PHY, etc	ON
VDDIO_18	1.8V GPIO, I2C, etc	ON
VDDIO_33	3.3V GPIO	ON
VDDAN_*_EFUSE	EFUSE	ON
VDDCR_S5*	USB	ON

Table 4 Key Signals at Different PM Modes

Signals	Default	BOCO	BOMACO
PX_EN	LOW	N/A	N/A
MACO_EN	N/A	N/A	N/A
PERSTb	HIGH	1->0->1	1->0->1
PWR_EN	HIGH	LOW	LOW
BOMACO_EN	LOW	LOW	HIGH

Table 5 Platform to Support BOMACO

BOMACO_EN	SVC PU/PD	SVD PU/PD
HIGH	PU	PU
LOW	bootVID	bootVID

Table 3 Power Rails Status at BOMACO Mode

Power Rail at ASIC	Used logic	ON/OFF Status for BOMACO-A
VDDCR_GFX	GFX IP, SDMA, GFXCLK CLKIP	OFF
VDDCR_SOC	SYS IPs	OFF
VDDCI_MEM	MEM PHY	OFF
VDDIO_MEM	MEM PHY	ON
MVDDC/MVDDQ/VPP	DRAM	ON
VDDCR_BACO	NBIO/THM/MP1/USB	OFF
VDDIO_PCIE	PCIe PHY	OFF
VDDAN_C	PHY	OFF
VDDAN_18	PLL, PHY, etc	OFF
VDDIO_18	1.8V GPIO, I2C, etc	OFF
VDDIO_33	3.3V GPIO	OFF
VDDAN_*_EFUSE	EFUSE	OFF
VDDCR_S5*	USB	ON

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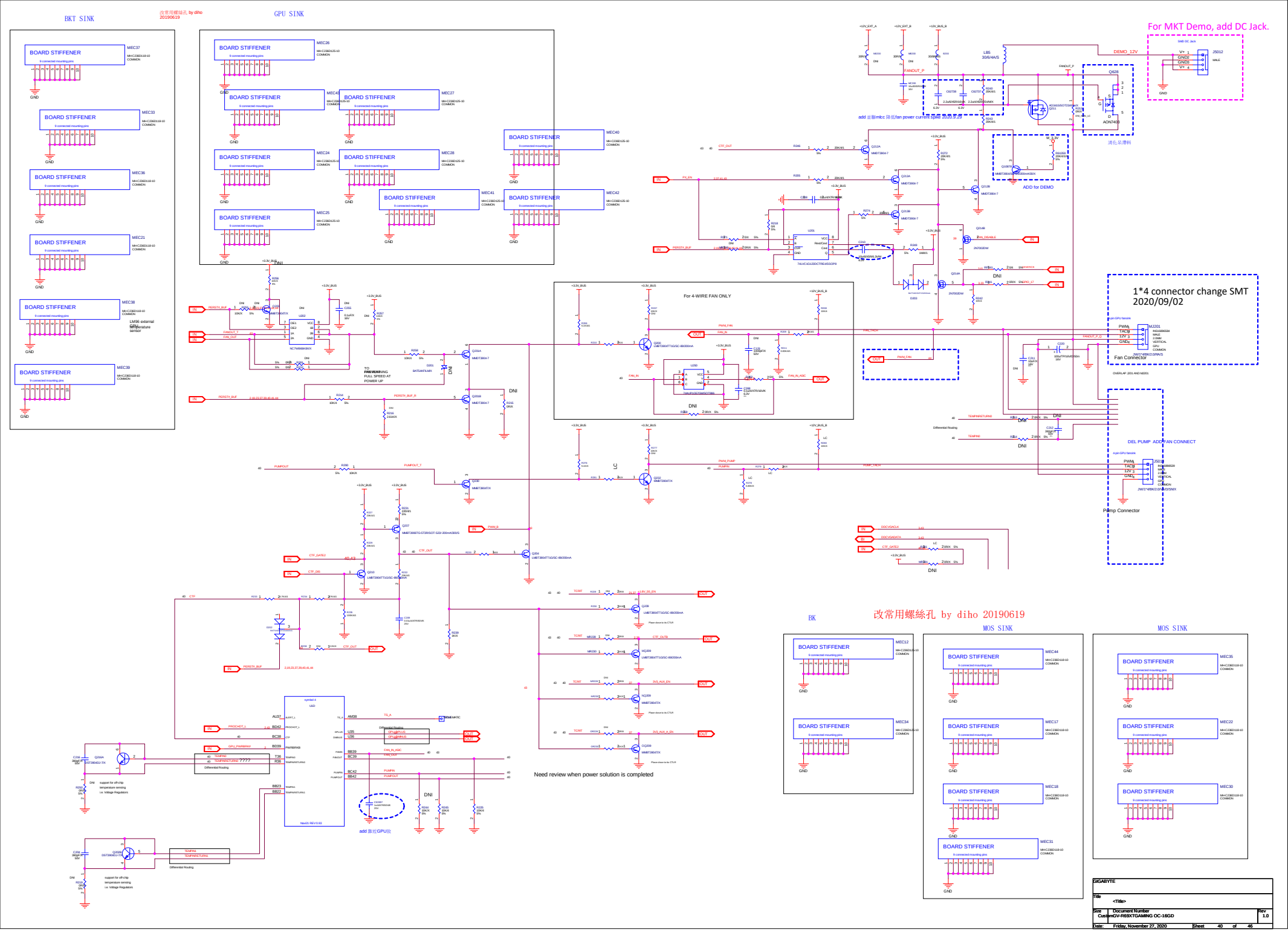
BKT SINK
改常用螺絲孔 by diho
20190619
GPU SINK
For MKT Demo, add DC Jack.
1*4 connector change SMT
2020/09/02
Fan Connector
Pump Connector
DEL PUMP ADD FAN CONNECT
For 4-WIRE FAN ONLY
Need review when power solution is completed
BK
MOS SINK
MOS SINK
GIGABYTE
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GV-R69XTGAMING OC-16GD
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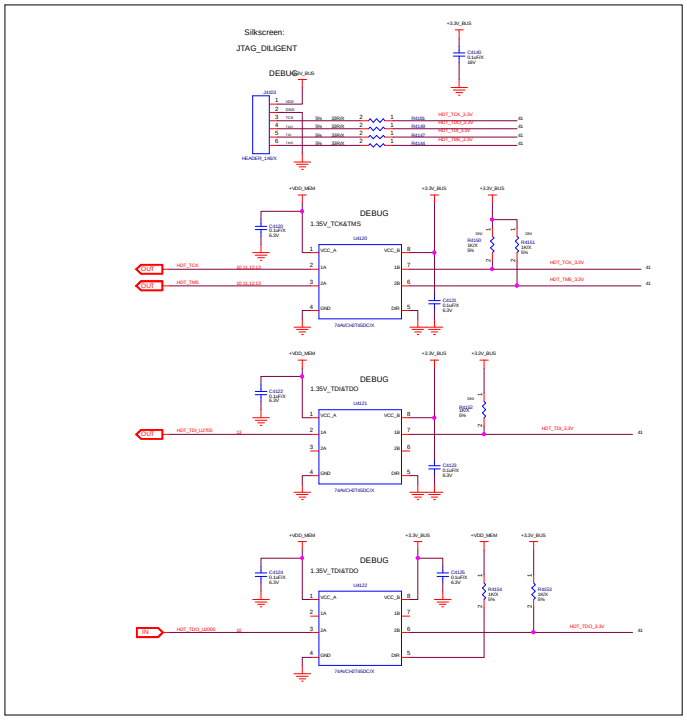

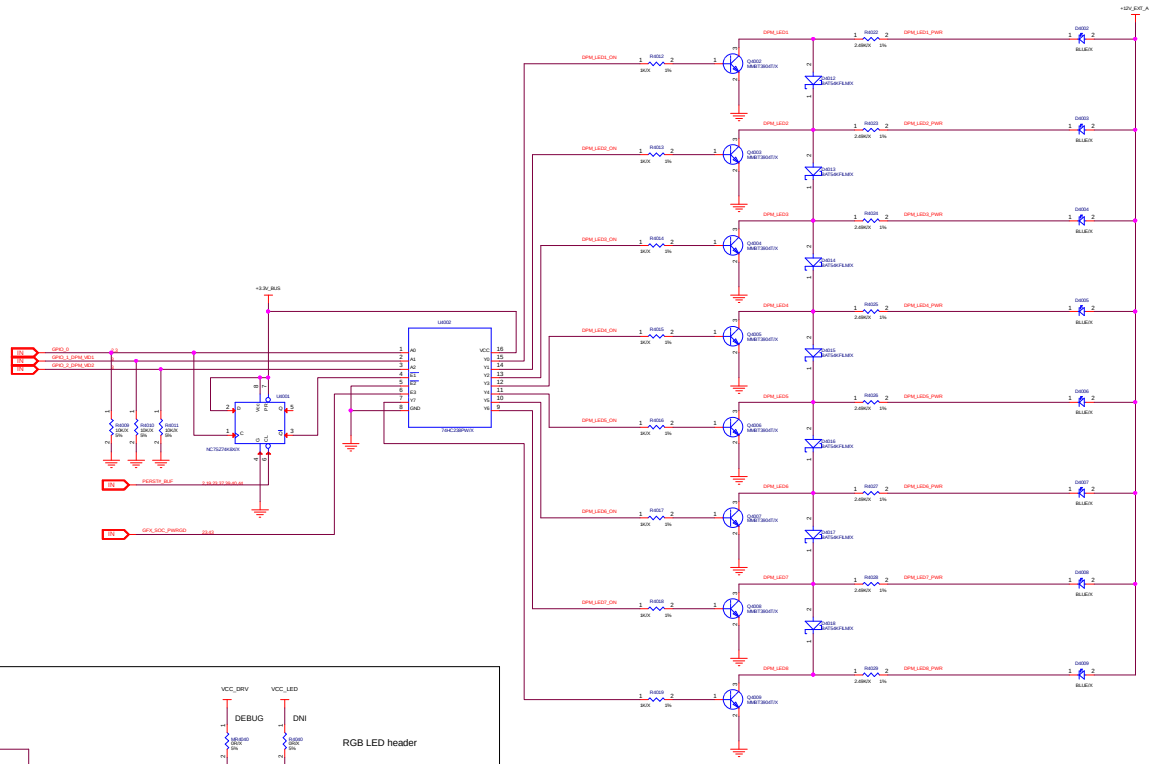

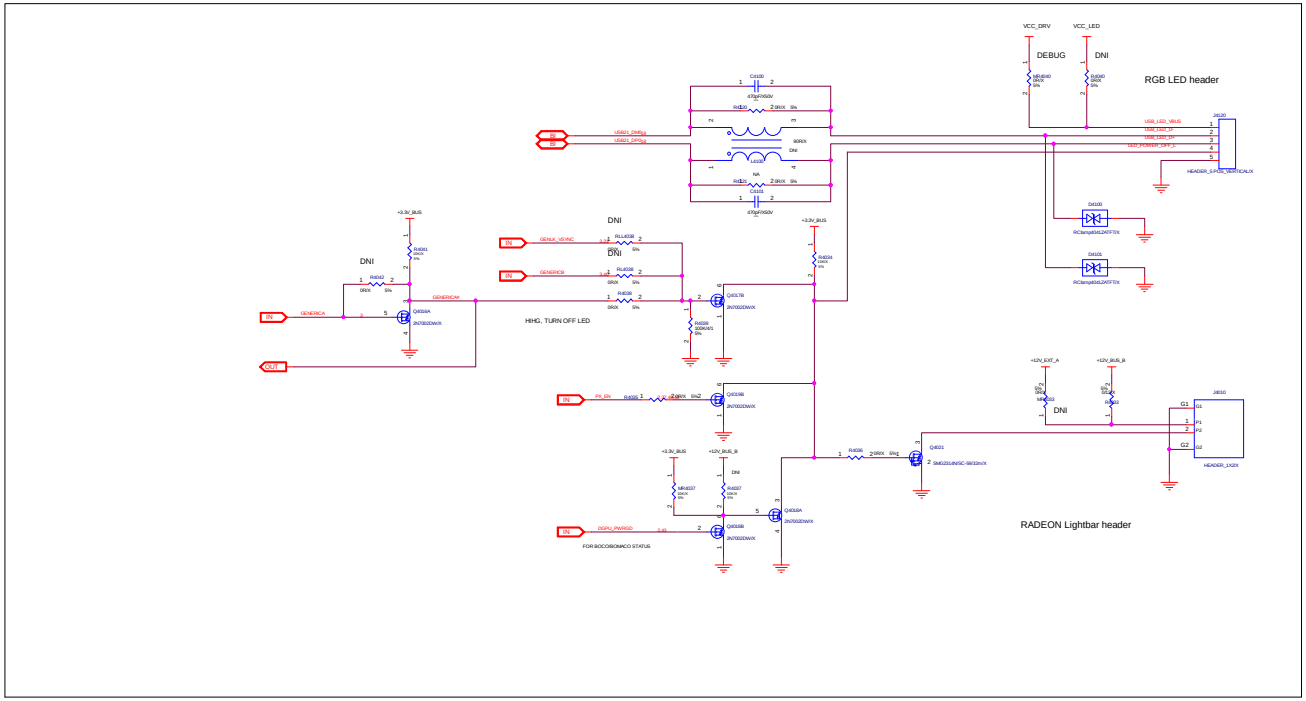

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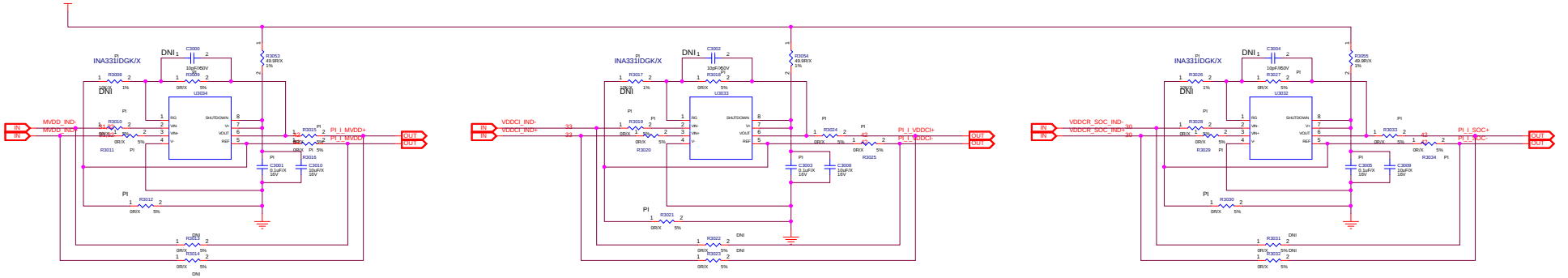
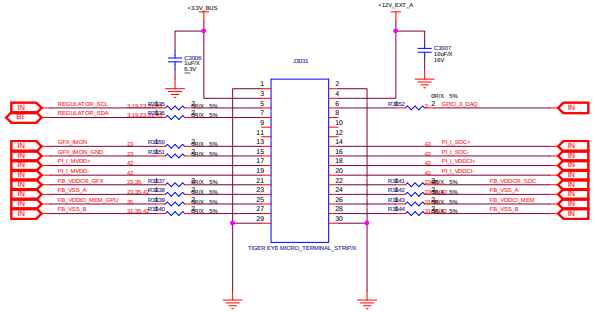
+3.3V_ModS



FOR PI DAUGHTER CARD



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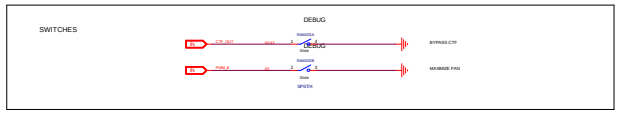
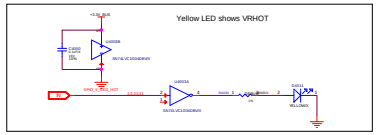
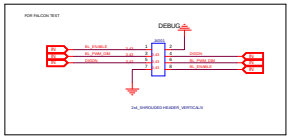
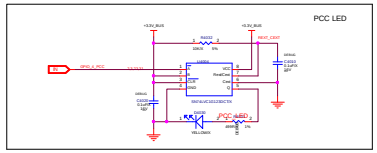
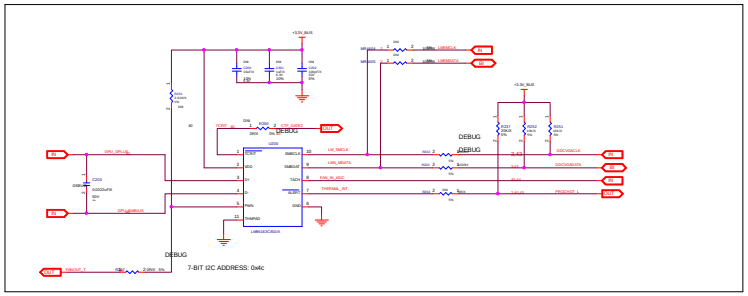
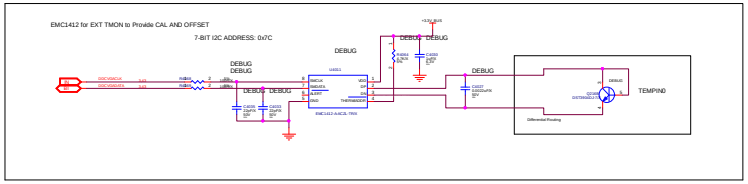


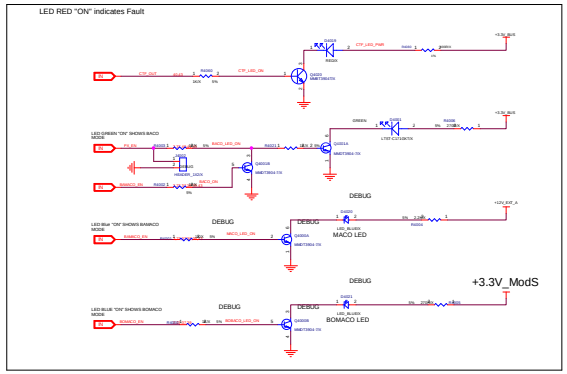


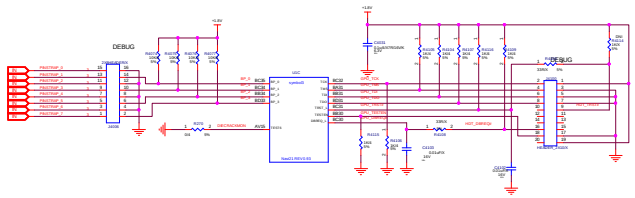












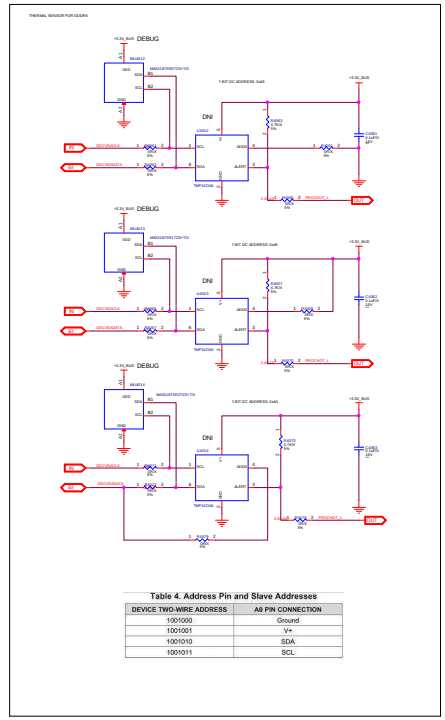
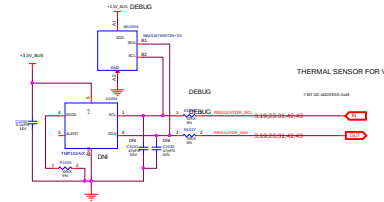
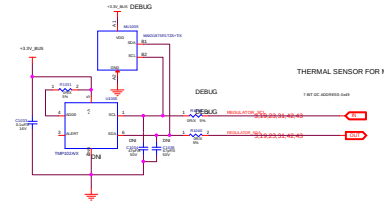
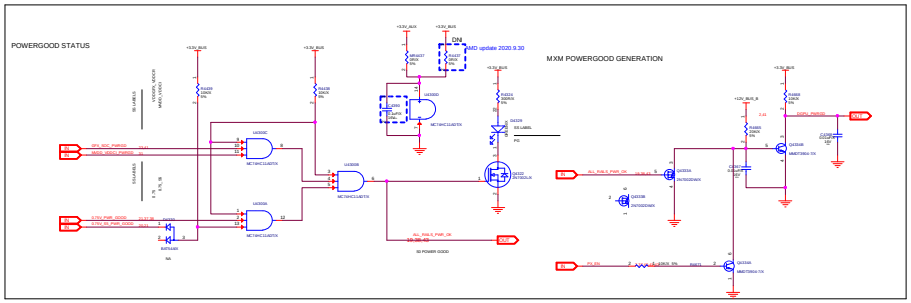


Table 4. Address Pin and Slave Addresses

DEVICE TWO-WIRE ADDRESS	A0 PIN CONNECTION
1001000	Ground
1001001	V+
1001010	SDA
1001011	SCL







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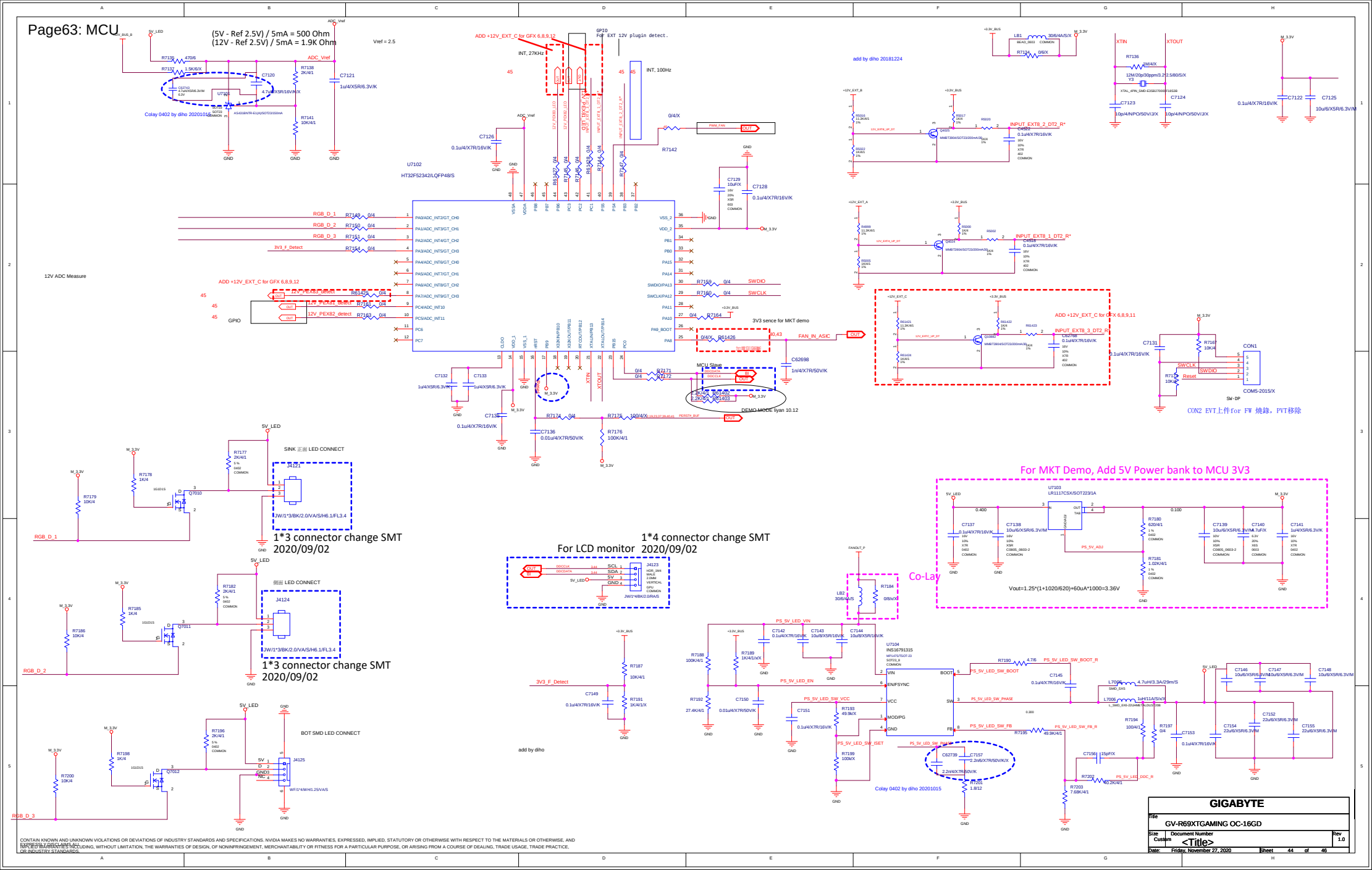

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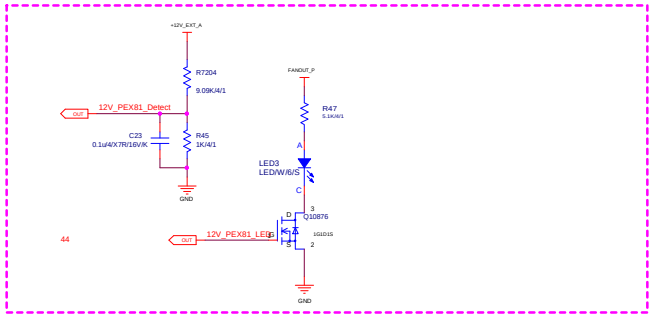
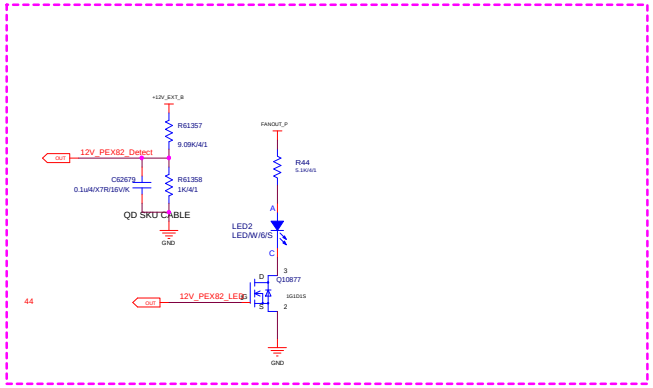
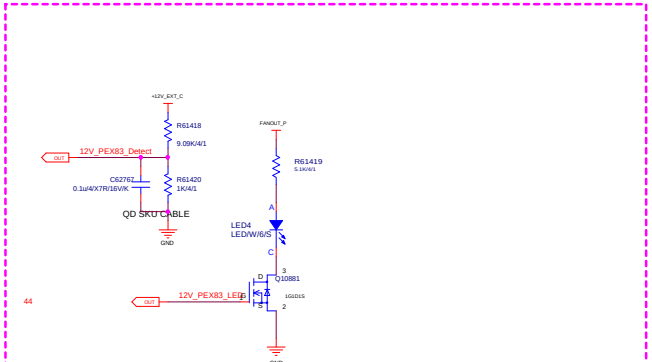
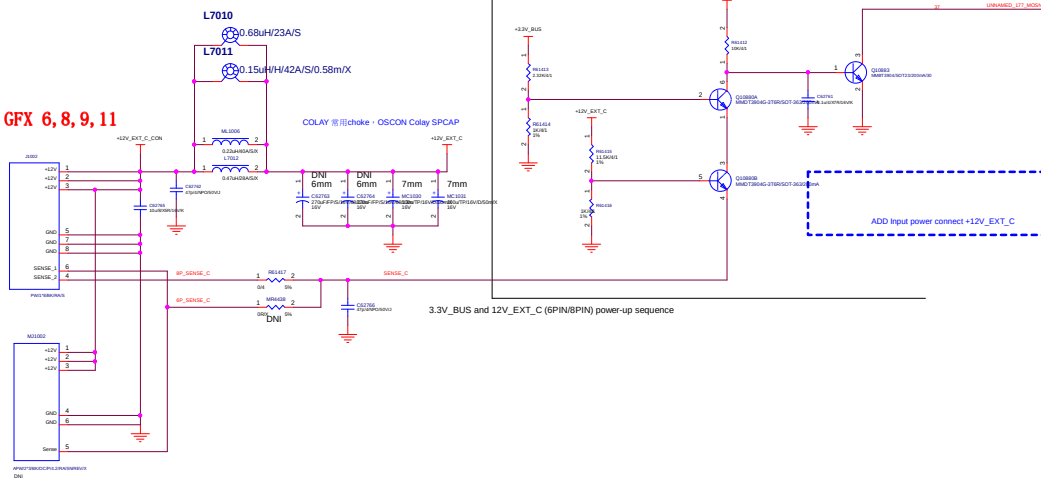






ADD +12V_EXT_C for GFX 6,8,9,11

0805 COLAY 0603 diho 2018.12.02



3.3V_BUS and 12V_EXT_C (6PIN/8PIN) power-up sequence

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1	-00B	Nov 11 2019	Added MODS circuit
1	-00C	Jan 21 2020	Connected +1.8V_SS to OSC_VDD18 Gated +VBUS_PWR_USBC0 by Modified USBC Power protection circuits

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