

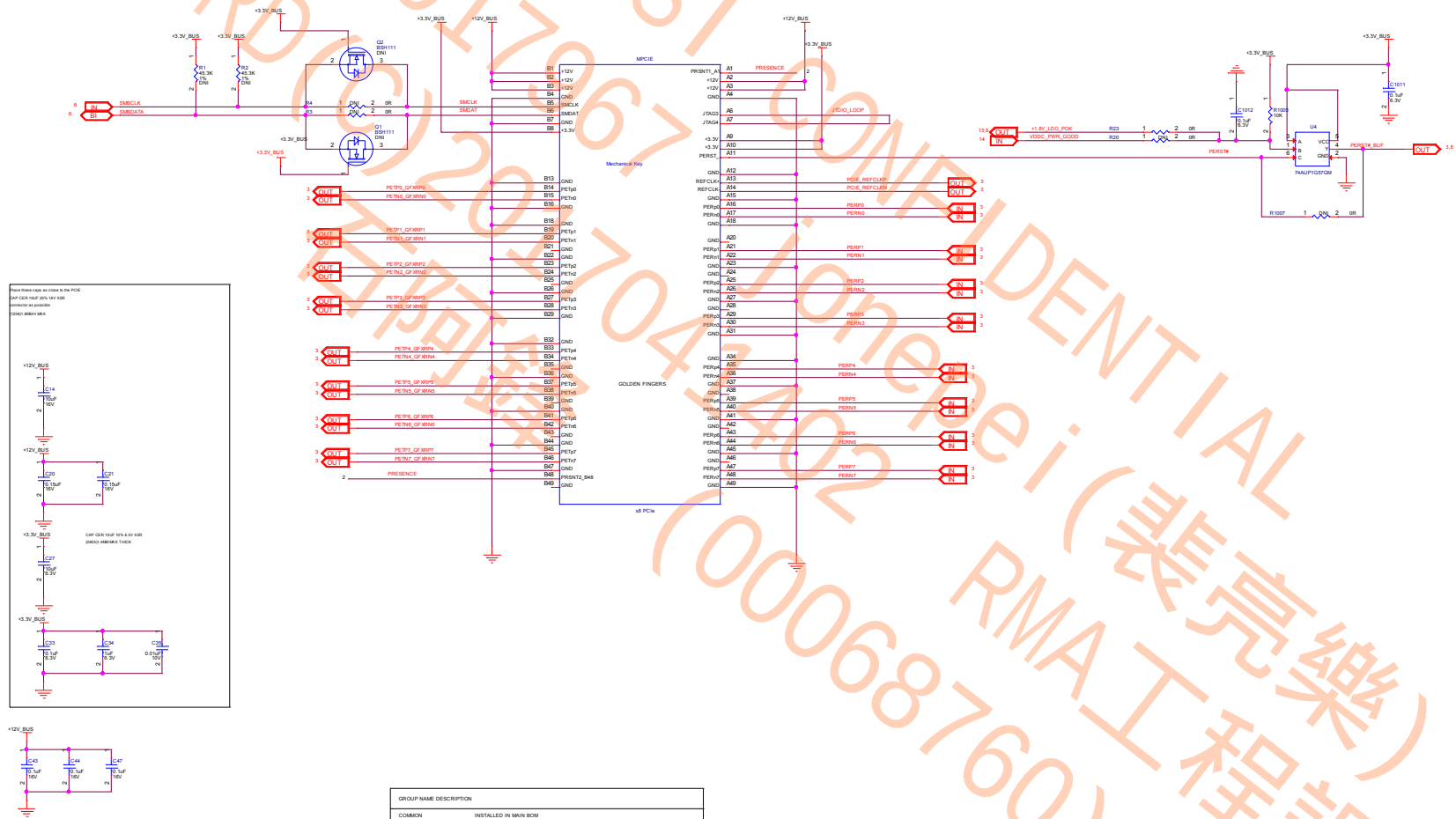
TABLE OF CONTENTS

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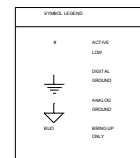
GROUP NAME DESCRIPTION	
COMMON	INSTALLED IN MAIN BOM
NONE	NO P/N/NOT IN BOM
DNI	DON'T INSTALL
INT	INTERNAL, WON'T BE IN PRODUCTION BOM
GPU	GPU P/N
BC	BRACKET
FIS	FAN/HEAT SINK OR FAN/SINK
BACD	BACD CPU/F
SUBBOM	SUBBOM P/N
2ND SOURCE	
ALT	ALTERNATIVE P/N/FORMAT-ALT+ALT1/PN1/PN2...(-)
SUB BOM	
MEM	MEMORY SUB BOM
DRBOM	DRIBOM SUB BOM
POWER SUB BOM	
VDDIC	VDDIC SUB BOM
VDDIC1	VDDIC1 SUB BOM
MAGD	MAGD SUB BOM
OSD	OSD SUB BOM
TVS	1.5V SUB BOM

AMD - PLATFORM HARDWARE ENG #48: NO.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203		COMPONENTS: MICROPROCESSOR ADVANCED MICRODEVICES INC. ④ REV. 1 AMC0000000000000000 This information represents the design for the customer product only, and is provided only to facilitate a non-disclosure agreement with AMD for the customer's purposes. Further distribution or disclosure is strictly prohibited. This information represents the design for the customer's product only, and is provided only to facilitate a non-disclosure agreement with AMD for the customer's purposes. Further distribution or disclosure is strictly prohibited.
SHEET: TOC AND BOM GROUP	DATE: Thu Feb 04 04:22:45 2016	
SHEET NUMBER: 1 OF 17	REV: 1.0	
DOCUMENT NUMBER: 105_003400_00A	TITLE: BANKS DT	
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PCI-EXPRESS EDGE CONNECTOR

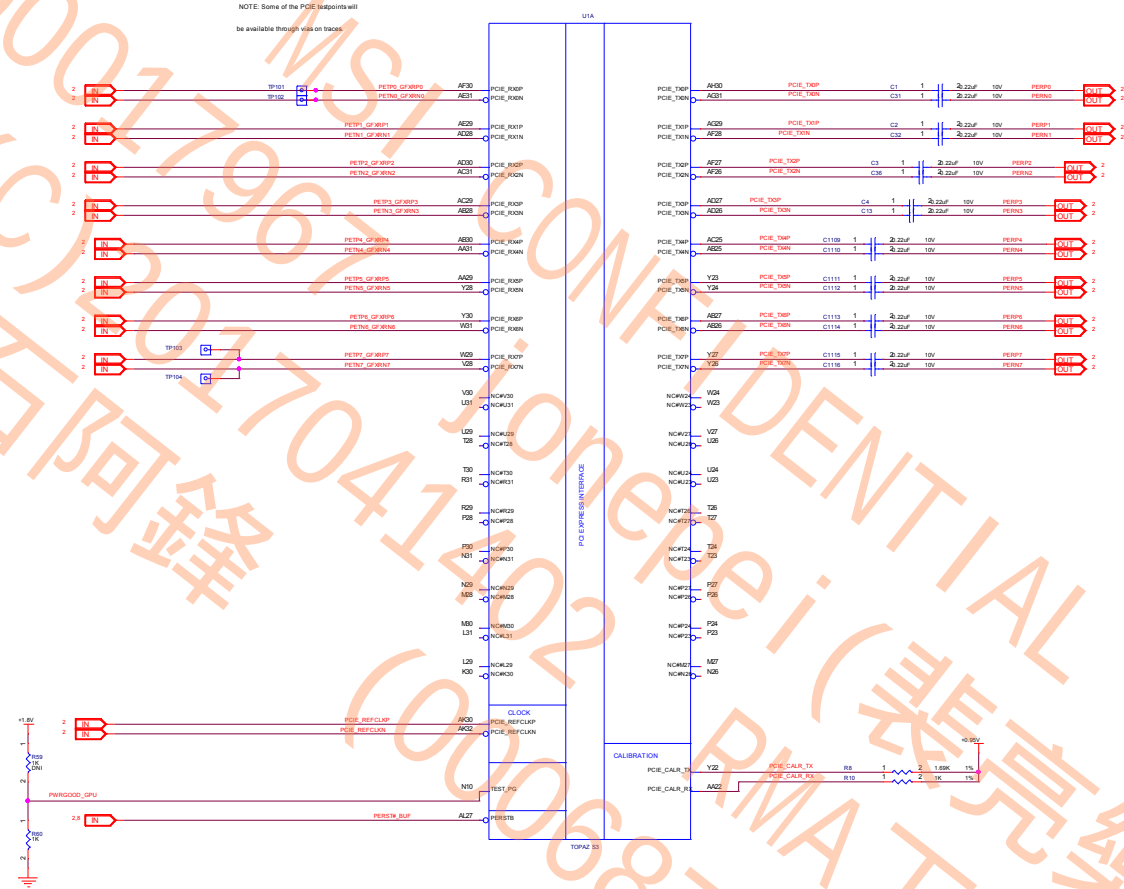


GROUP NAME DESCRIPTION	
COMMON	INSTALLED IN MAIN ROM
ROM1	NO PIN, WON'T BE IN ROM
DN1	DON'T INSTALL
INT	INTERNAL ROM, WON'T BE IN PRODUCTION ROM
GPU	GPU PIN
SUBROM	SUBROM PIN
2ND SOURCE	ALTERNATIVE PINFORMAT ALTH1/PIN1/PIN2...)
ALT	
POWER SUB ROM	
VIDEO	VIDEO SUB ROM
MIMO	MIMO SUB ROM
ISS	0.8V SUB ROM
1VB	1.8V SUB ROM
DEBUG	DEBUG SUB ROM



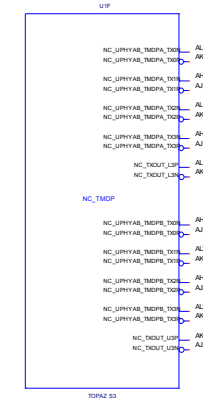
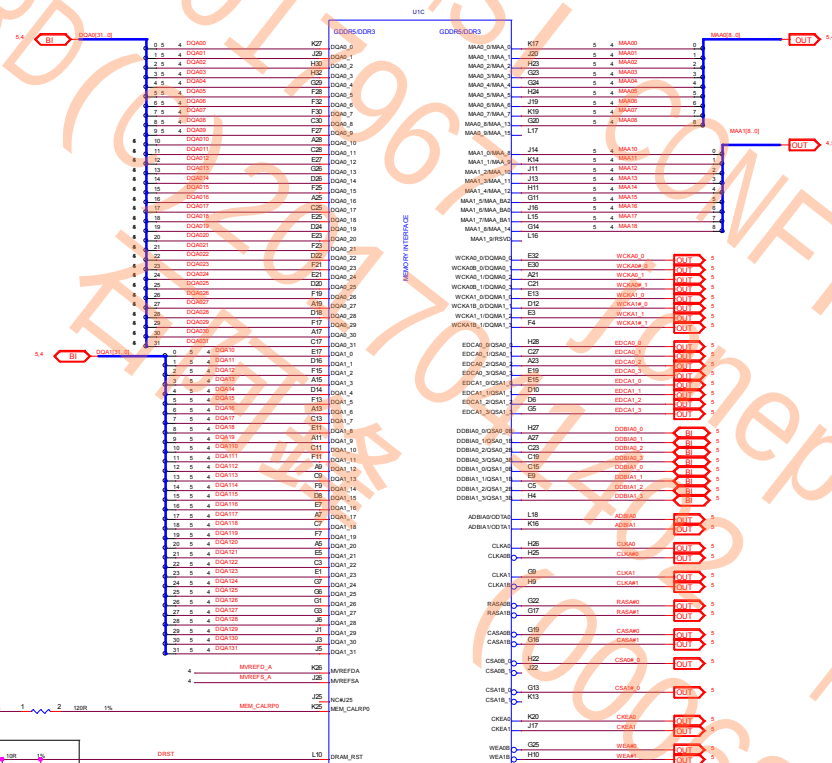
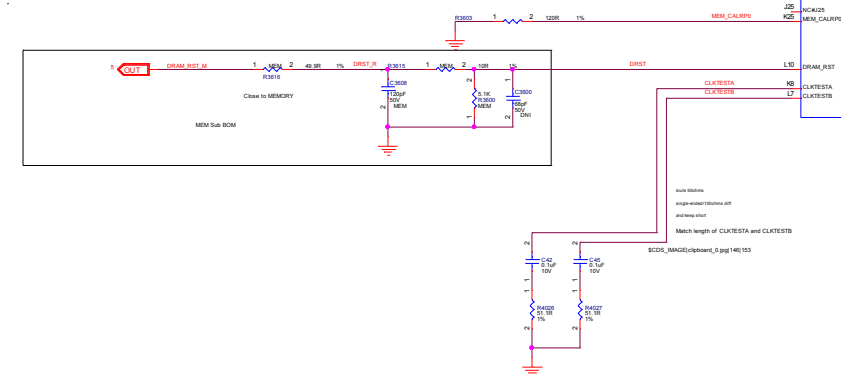
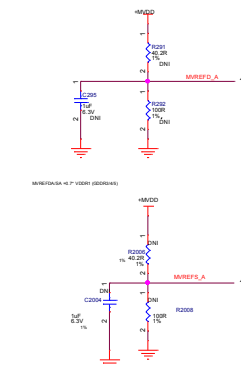
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SHEET: PCH-E Edge Connector		REV: 1.0		TITLE:	
DATE: Thu Feb 04 02:22:45 2016				BANKS DT	
SHEET NUMBER: 2 OF 17					
DOCUMENT NUMBER: 105_D03400_00A					

PCIe Interface



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SHEET: PCIe8 Interface		REV: 1.0		TITLE: BANKS DT	
DATE: Thu Feb 04 02:22:46 2016		SHEET NUMBER: 3 OF 17			
DOCUMENT NUMBER: 105_D03400_00A					

MEM Interface Ch A



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SHEET: MEMInterface		
DATE:	Thu Feb 04 02:22:46 2016	REV: 1.0
SHEET NUMBER:	4	OF 17
DOCUMENT NUMBER:	105_D03400_00A	

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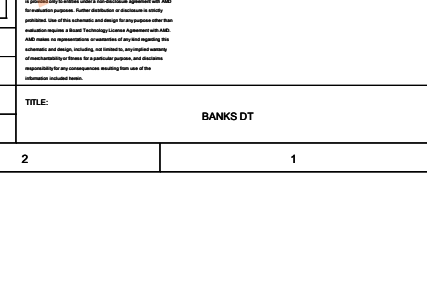
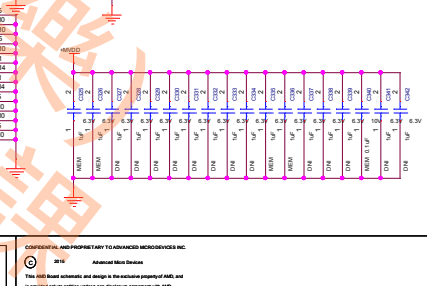
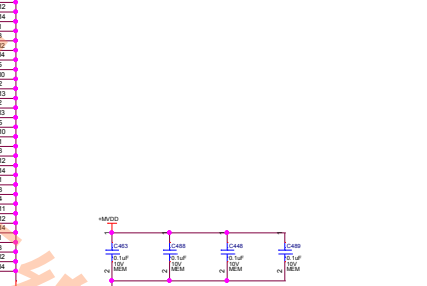
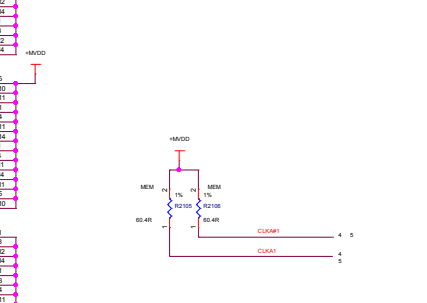
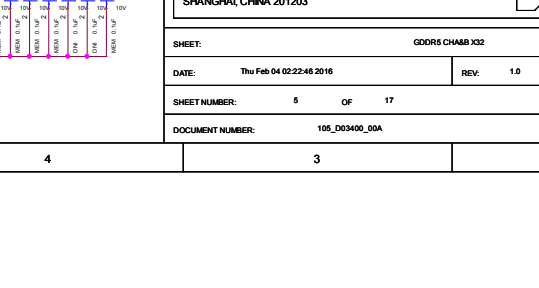
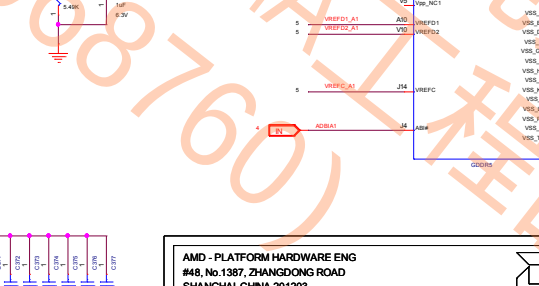
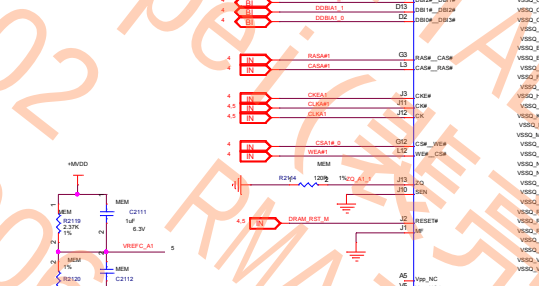
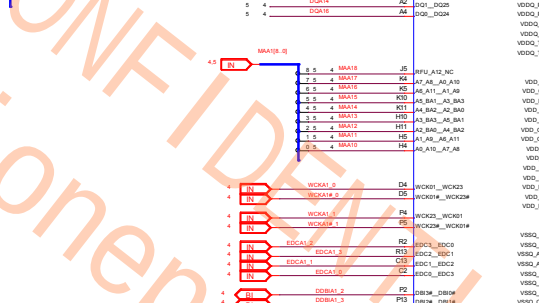
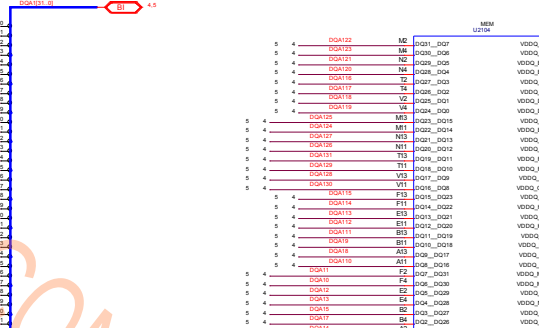
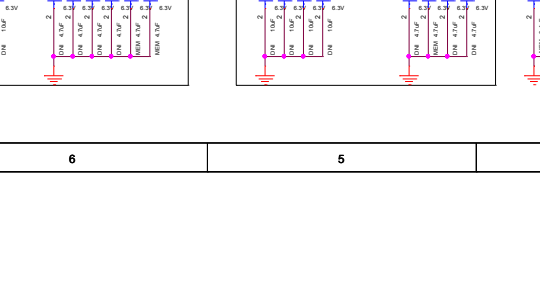
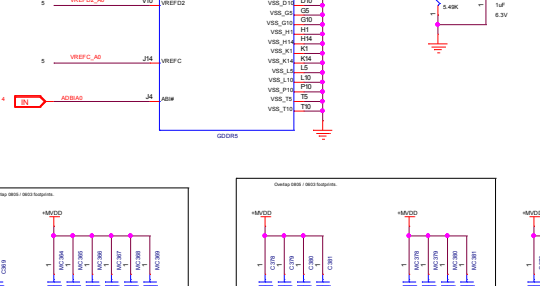
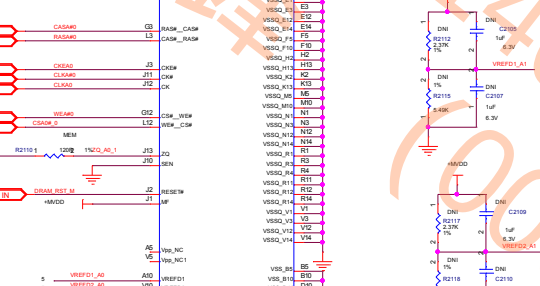
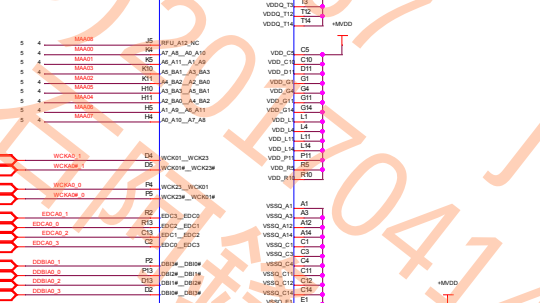
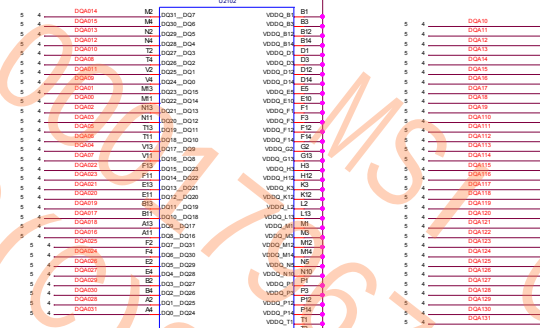
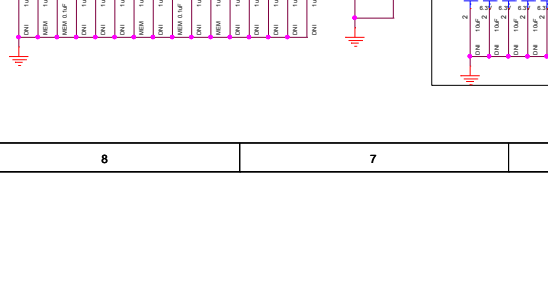
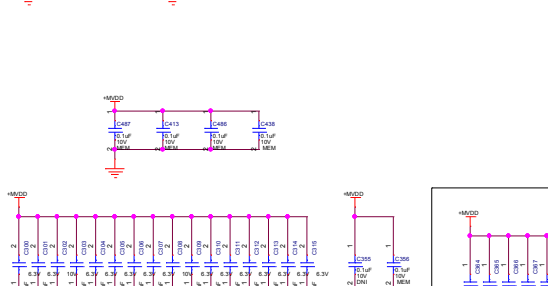
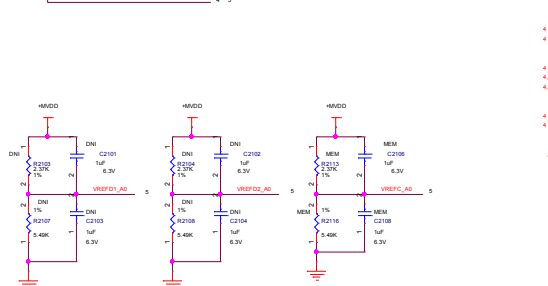
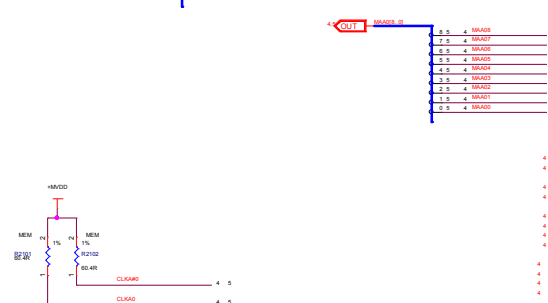
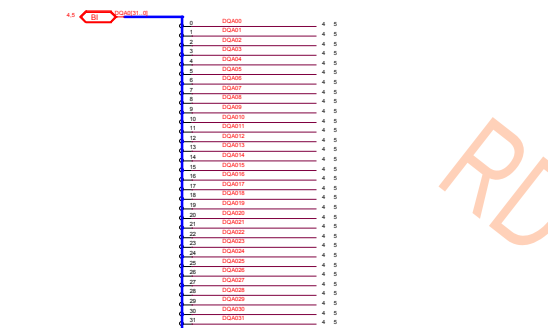
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CHANNEL A: 1GB/512MB GDDR5

(5) GDDR5 Memory Channel A&B

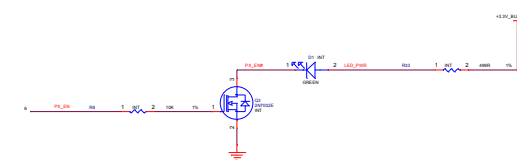
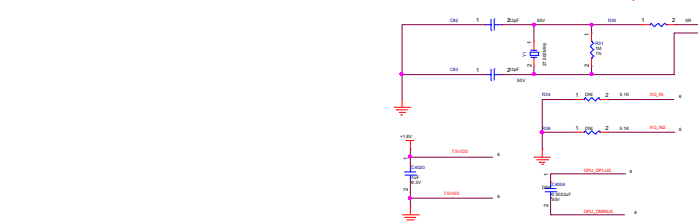
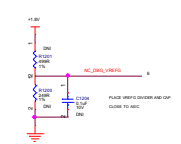
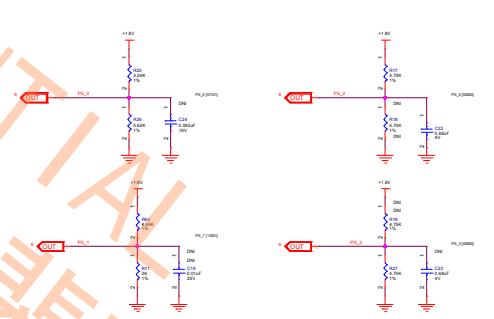
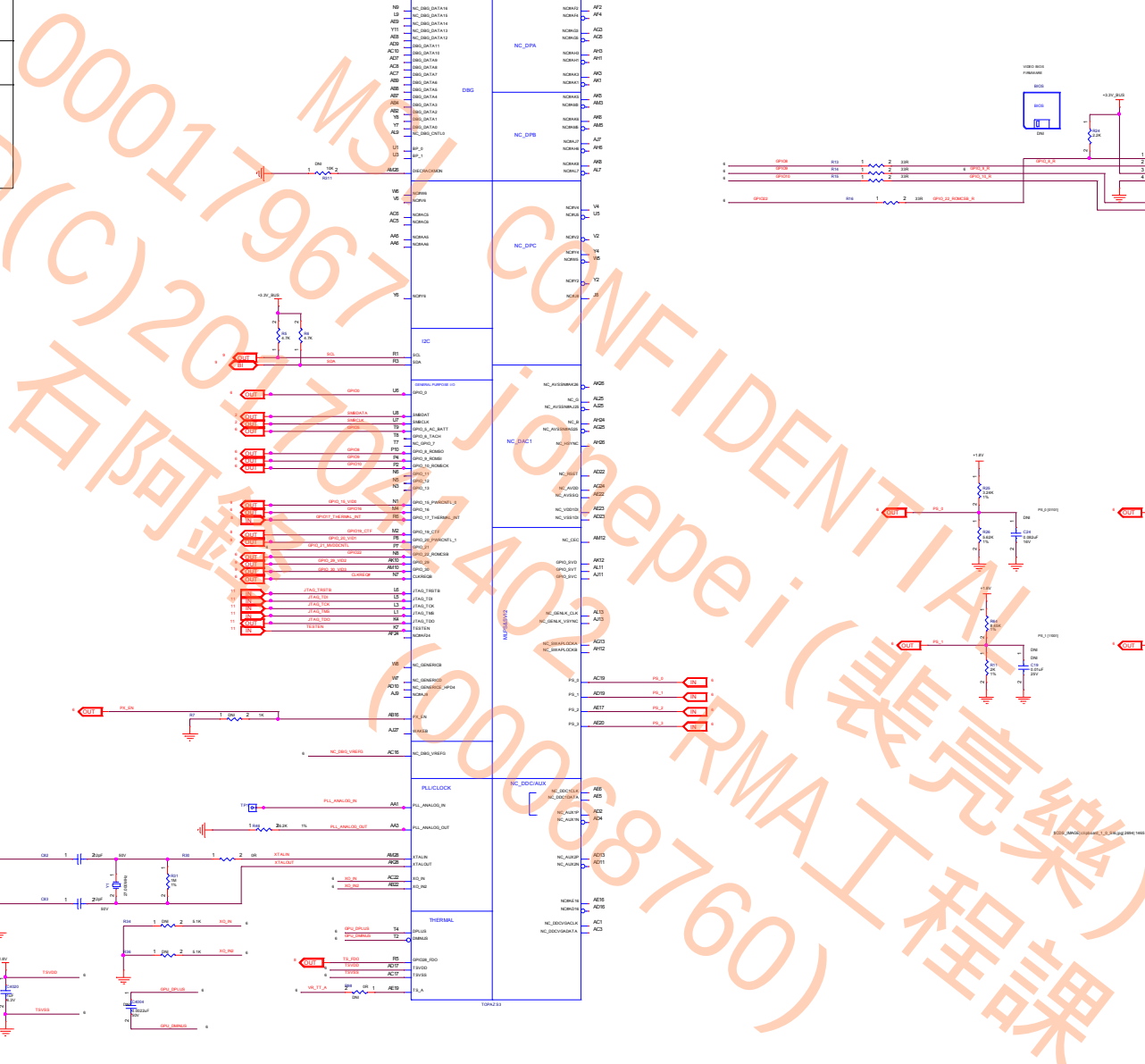


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SHANGHAI, CHINA 201203

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SHEET:		GDORS CHAM6 X32	
DATE:	Thu Feb 04 02:22:46 2016	REV:	1.0
SHEET NUMBER:		5	OF 17
DRAWING NUMBER:		105-003400-00A	

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SHEET: Main		 Intel Confidential	
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SHEET NUMBER: 6 OF 34 17		TITLE:	
DOCUMENT NUMBER: 10S_003400_00A		BANKS DT	
NOTES: NONE			

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SHEET: Power/GND			
DATE: Thu Feb 04 02:22:47 2016		REV: 1.0	
SHEET NUMBER: 7		OF 17	
DOCUMENT NUMBER: 105_003400_00A			

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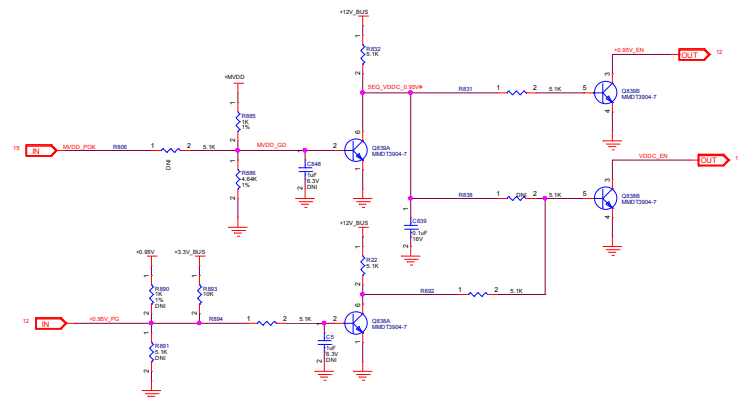
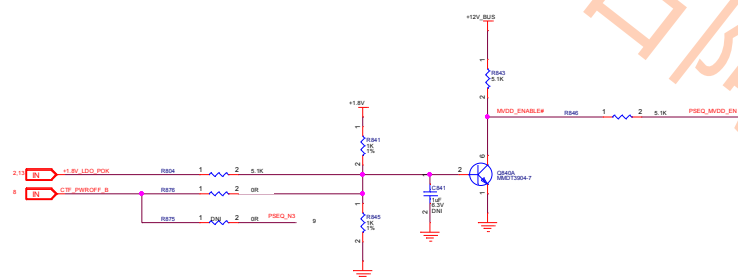
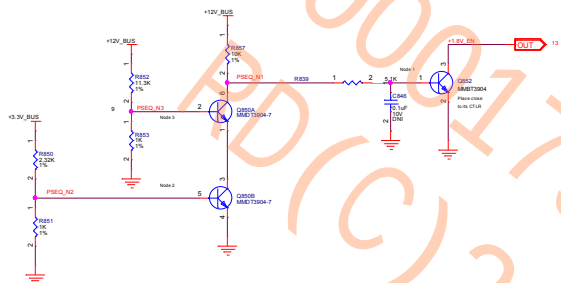
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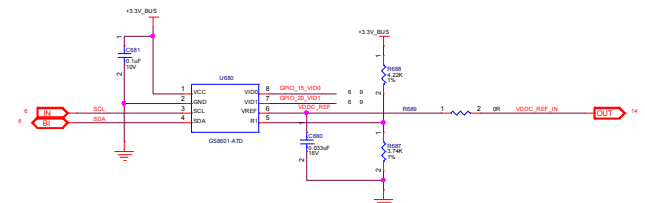
BANKS DT

POWER SEQUENCE
+1.8V → MVDD → +0.9V → VDDC
0.9V must ramp up before VDDC

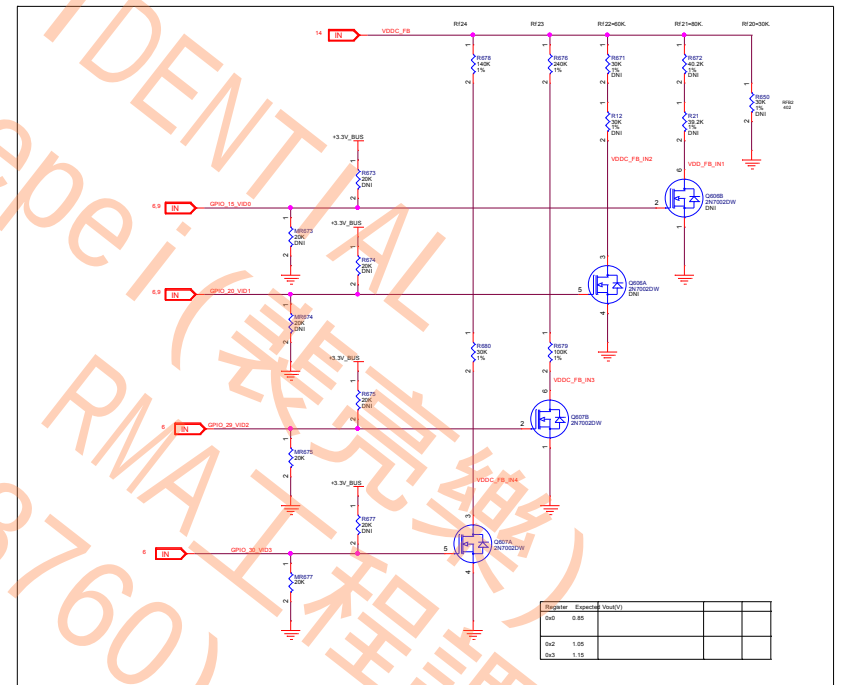
Don't support BACO
Support CTP (internal)



VDDC Low Side Divider



R088=3.24K, R087=4.48K, BOOT UP VDDC=0.9V, VR1/VCC=4.48K/3.24K 40±0.5%
R088=4.22K, R087=5.74K, BOOT UP VDDC=0.9V, VR1/VCC=5.74K/4.22K 40±0.5%



Register	Expected Value(V)		
0x0	0.85		
0x2	1.05		
0x3	1.15		

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DATE: Thu Feb 04 02:22:48 2016
REV: 1.0
SHEET NUMBER: 9 OF 17
DOCUMENT NUMBER: 105_D03400_00A

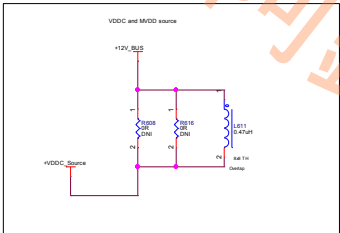
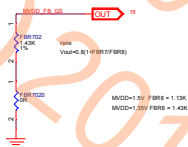
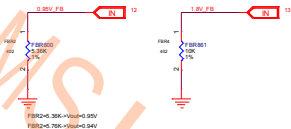
TITLE: BANKS DT

MSI
SUB BOM
SUBBOM(13A-01000)
SUBBOM(13A-01000)
TOL: +/-3%

VDDC
SUB BOM
SUBBOM(13A-01000)
TOL: +/-3%

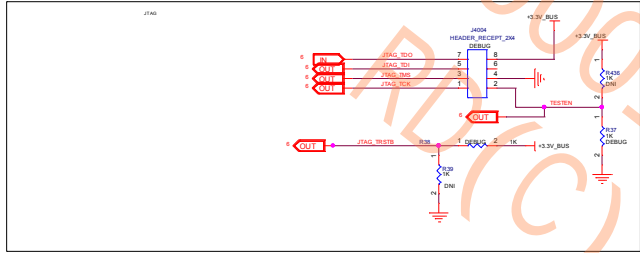
MGD
SUB BOM
SUBBOM(13A-01000)
TOL: +/-3%

LDG
SUB BOM
SUBBOM(13A-01000)
TOL: +/-3%



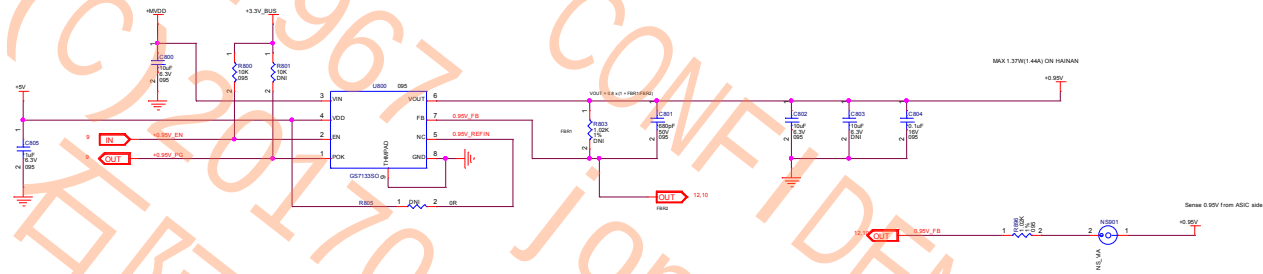
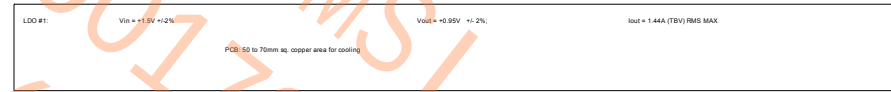
AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: Sub BOM	
DATE: Thu Feb 04 02:22:48 2016	REV: 1.0
SHEET NUMBER: 10 OF 17	
DOCUMENT NUMBER: 105_D03400_00A	
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SHEET: Debug		REV: 1.0		TITLE: BANKS DT	
DATE: Thu Feb 04 02:22:48 2016					
SHEET NUMBER: 11 OF 17					
DOCUMENT NUMBER: 105_D03400_00A					

Linear Regulators

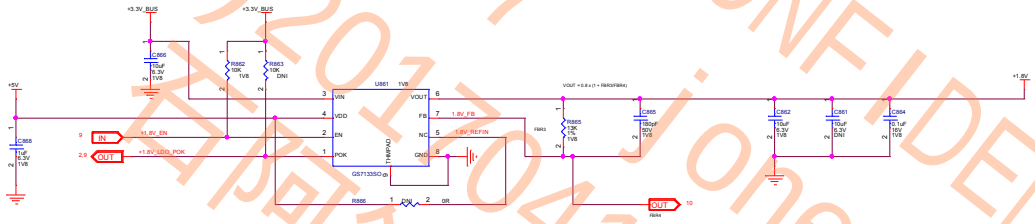
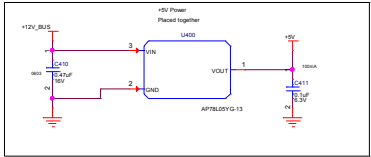


Sense 0.25V from ASIC side

COMPRESSED IMAGE

Linear Regulators

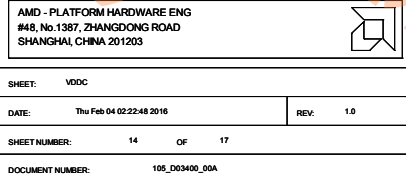
1.00 #2: Vin = 3.00V to 3.60V (0.3V $\pm$ 9%) Vout = +1.8V $\pm$ 2% Iout = 1.6A (TYP) RMS MAX
PDB: 50 to 70mm sq. copper area for cooling



COMPRESSED
IMAGE

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SHEET: 1.8V	
DATE: Thu Feb 04 02:22:48 2016	REV: 1.0
SHEET NUMBER: 13 OF 17	
DOCUMENT NUMBER: 105_D03400_00A	

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8		7		6		5		4		3		2		1	
AMD				TITLE: BANKS DT		DOCUMENT NUMBER: 106_D03400_00A		DATE: Thu Feb 04 02:22:49 2016		SHEET NUMBER: 17 OF 17		REV: 1.0			
REVISION HISTORY				ENGINEER: BILLYDENG		NOTES: NOTE		CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRODEVICES INC. This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representation or warranty of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of this schematic without notice.		C 004 Advanced Micro-Devices		AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203			
SCH Rev		PCB Rev		Date		REVISION DESCRIPTION									
1.00		00A		20170306		1 Initial release									
						17ci203									

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