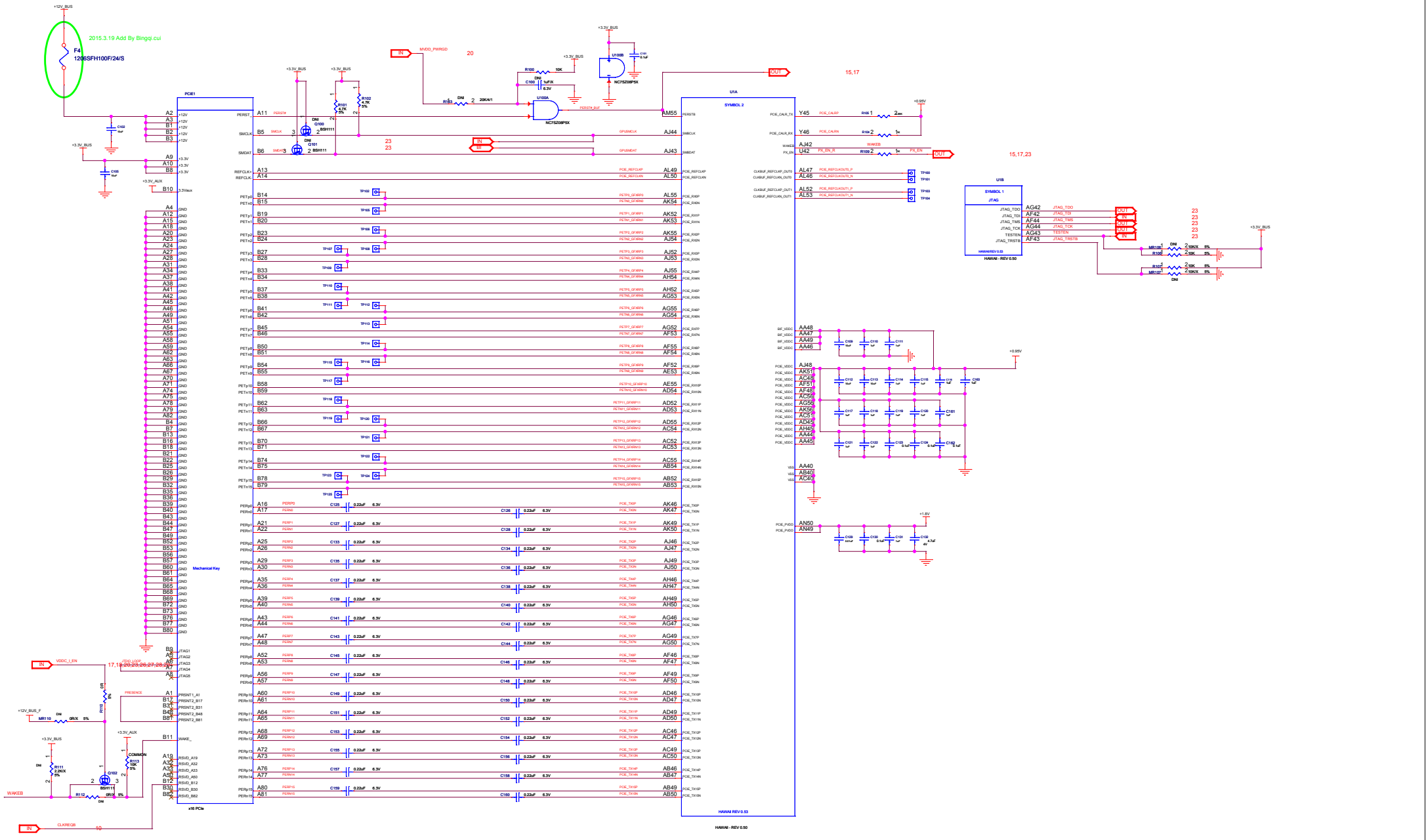

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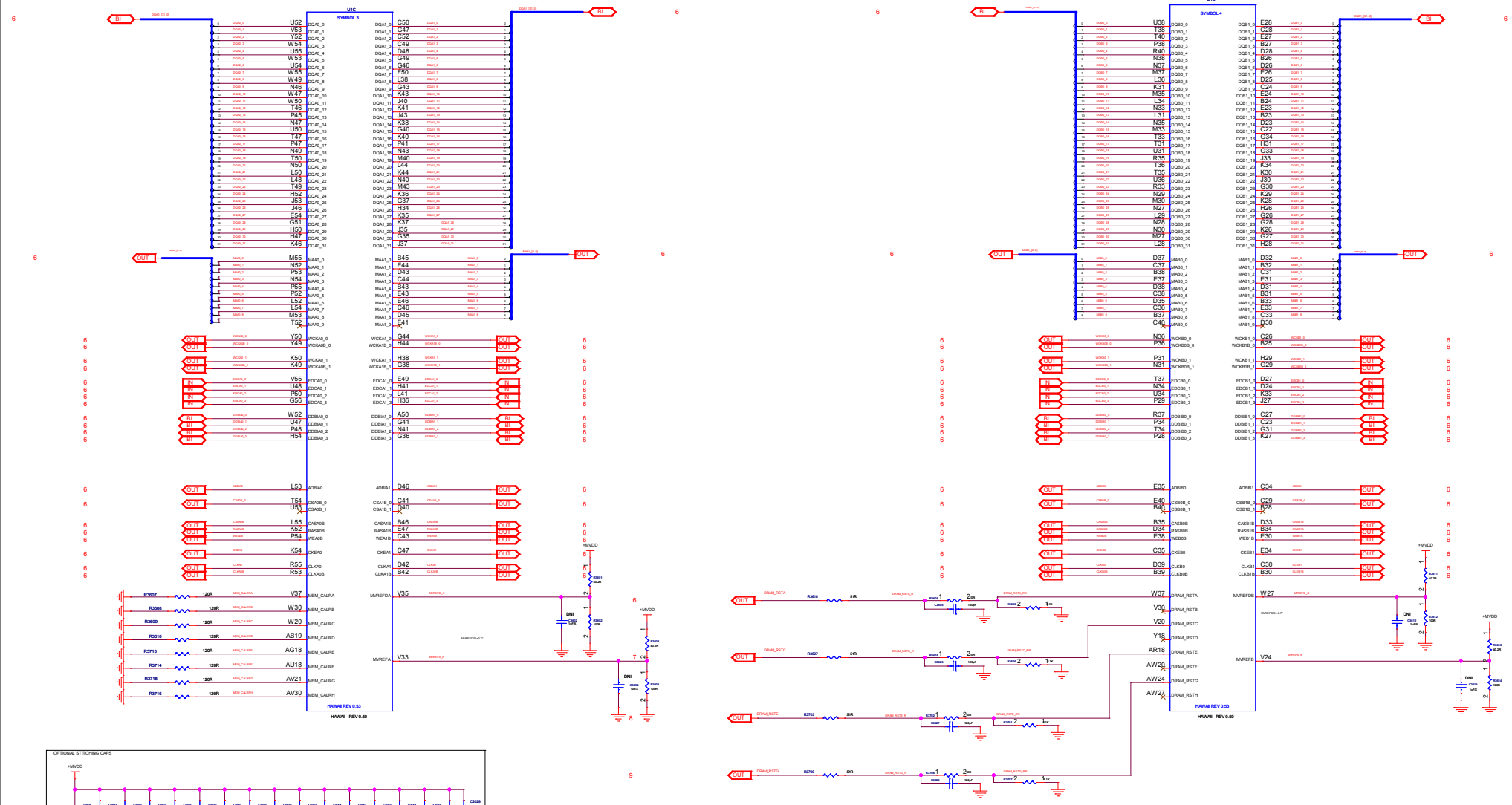

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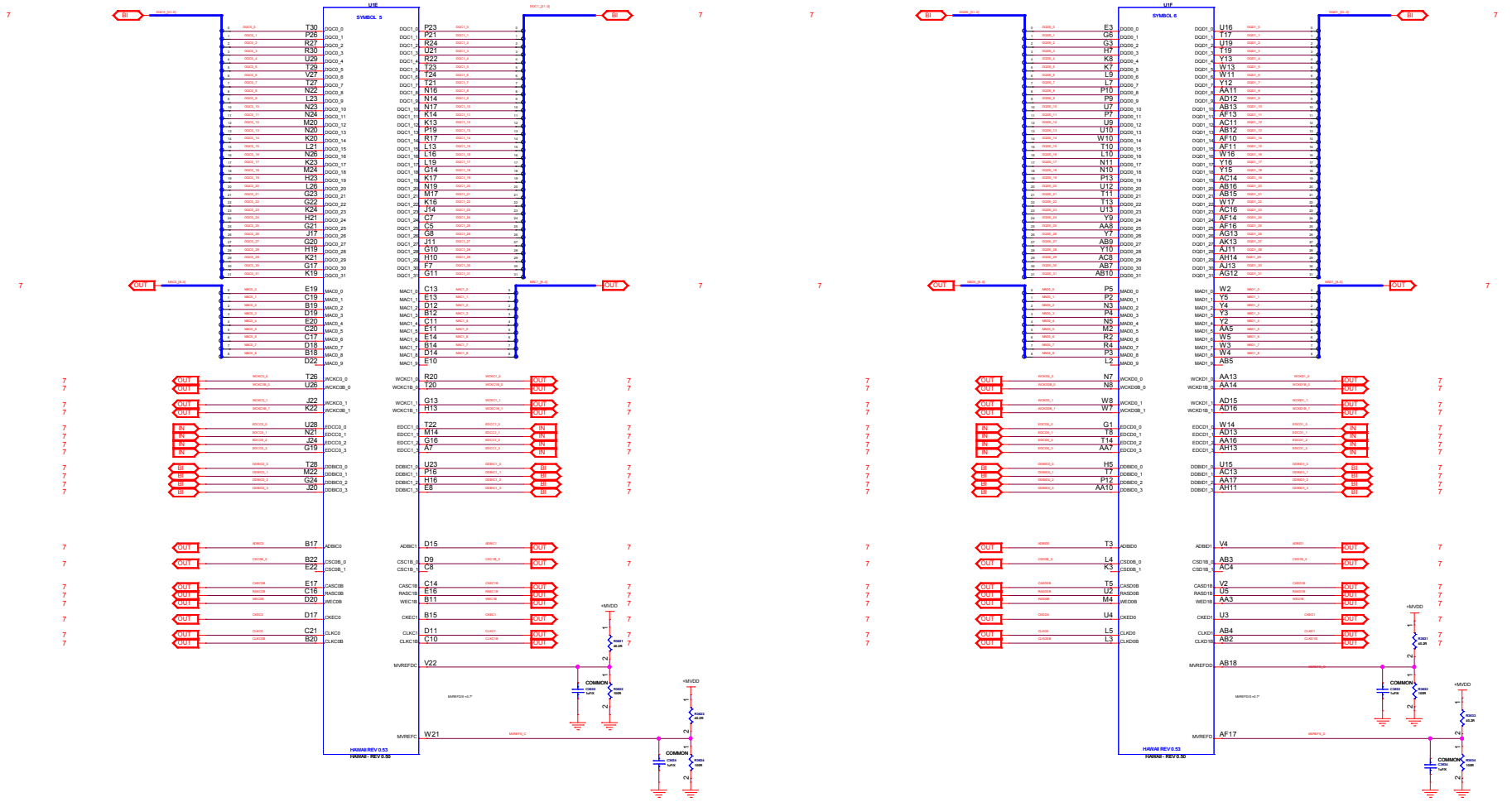

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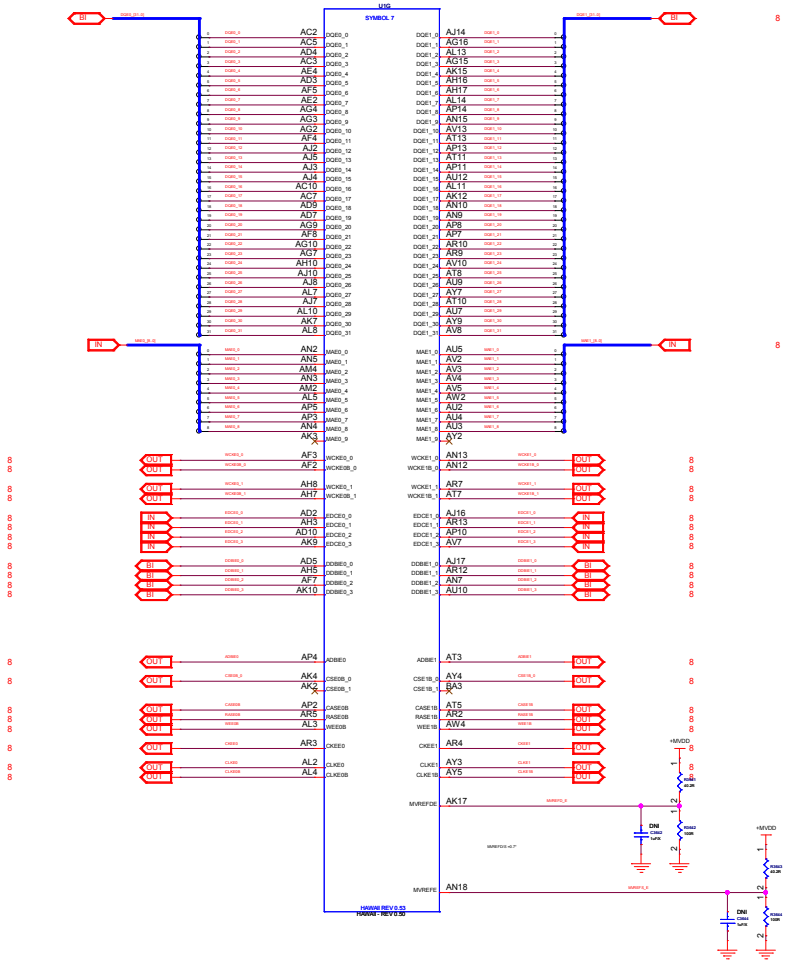

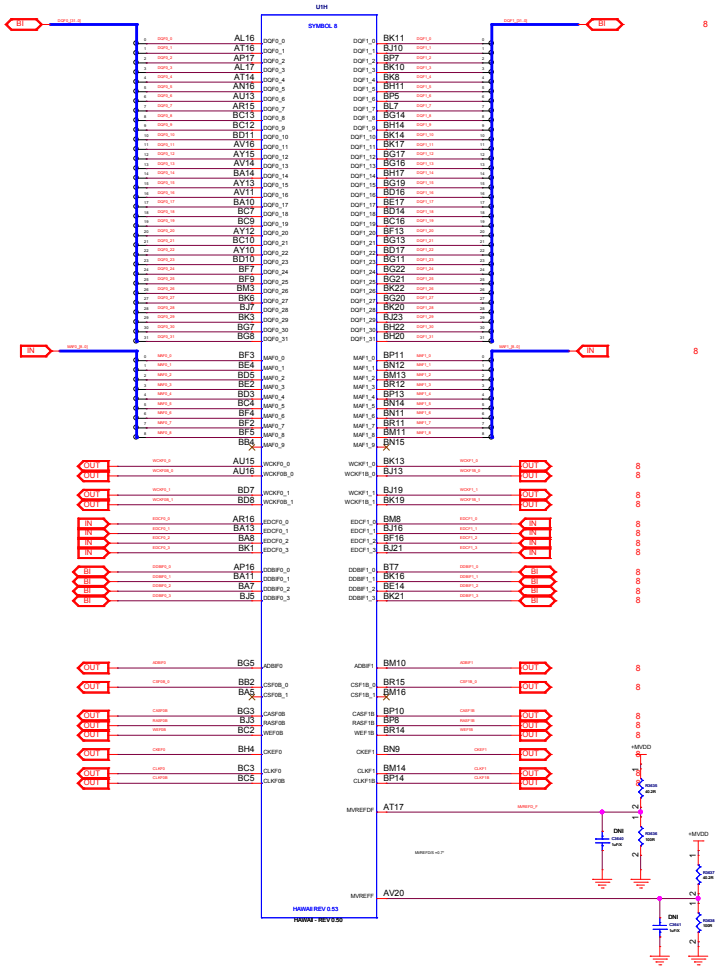

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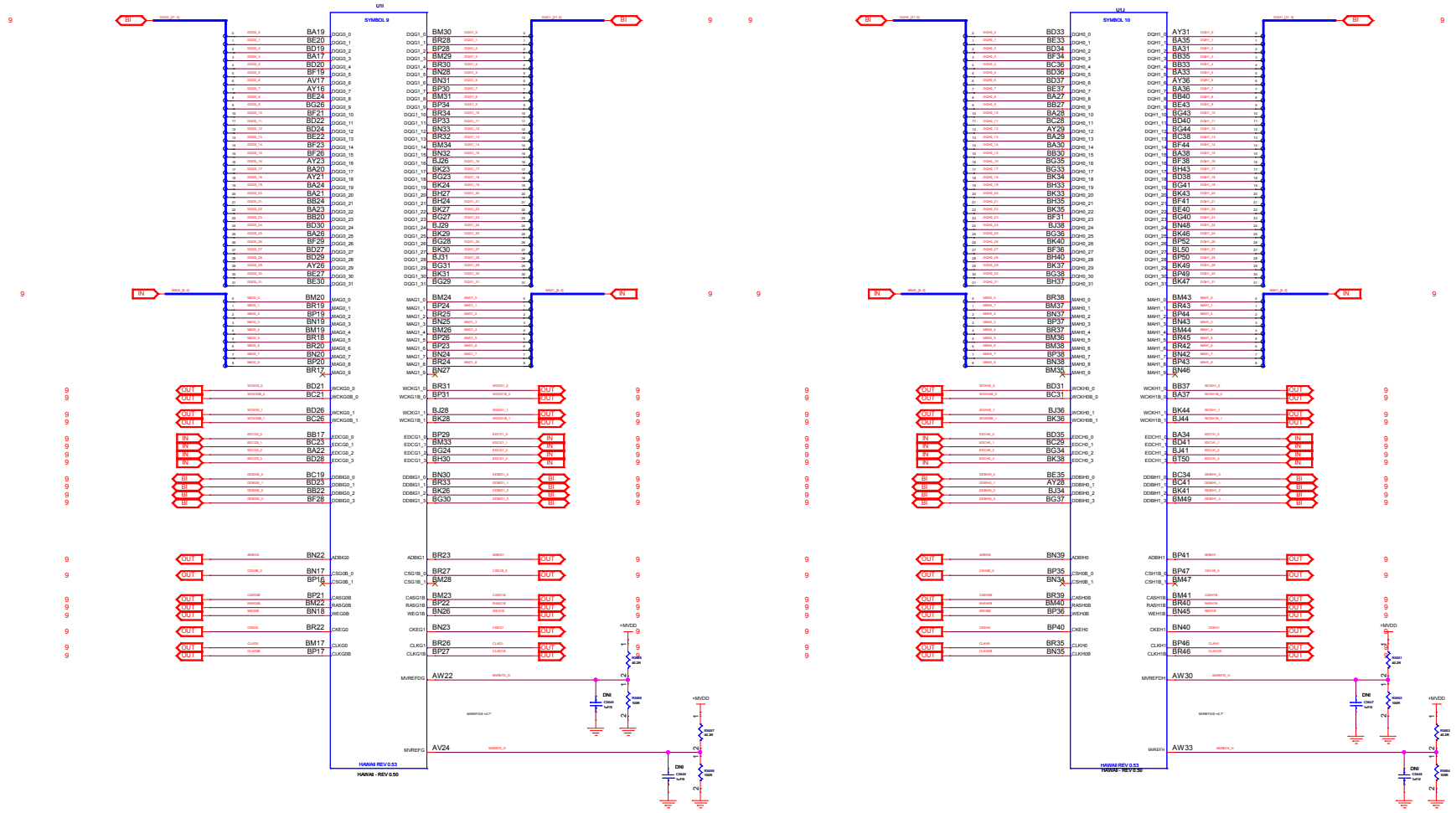

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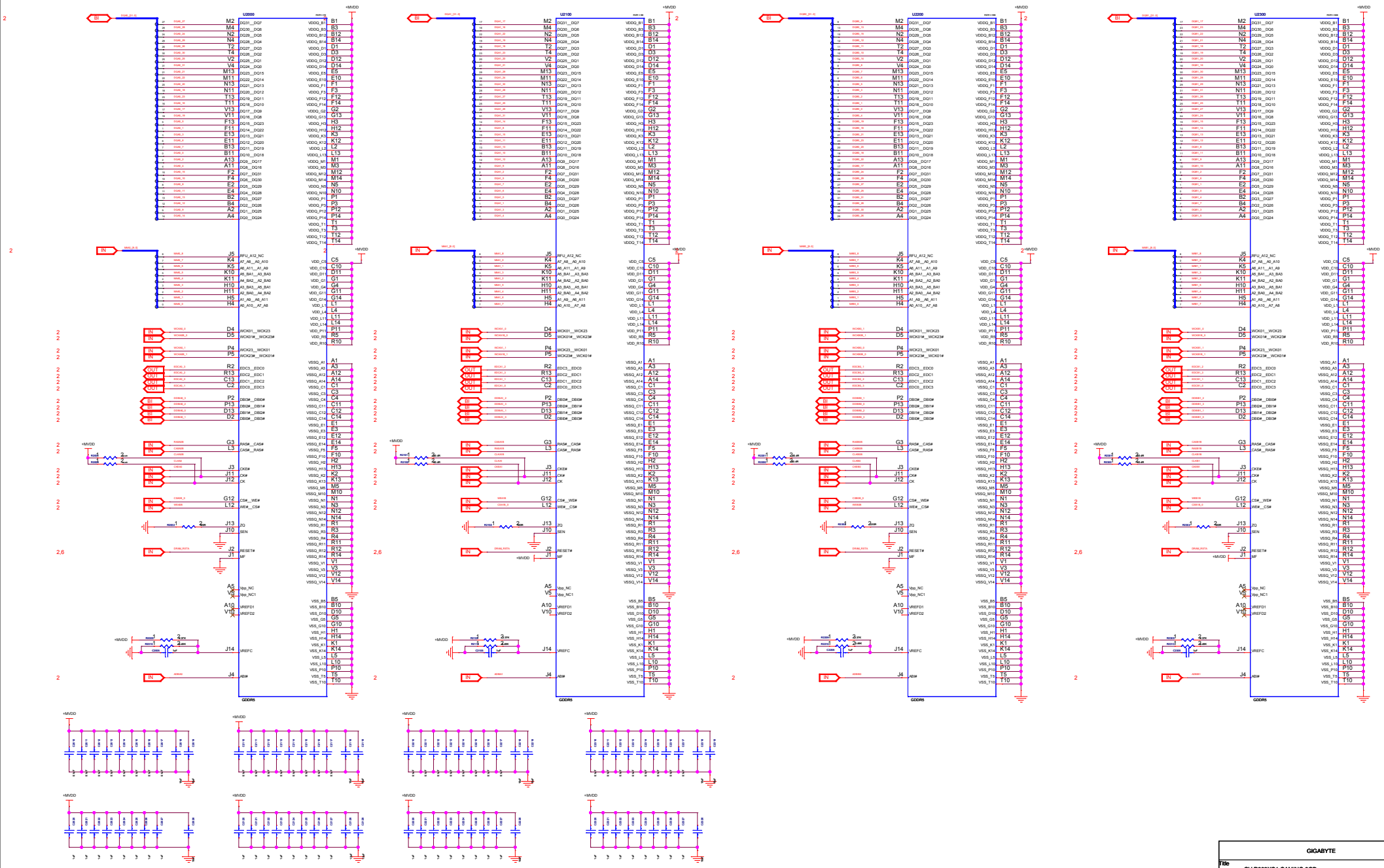

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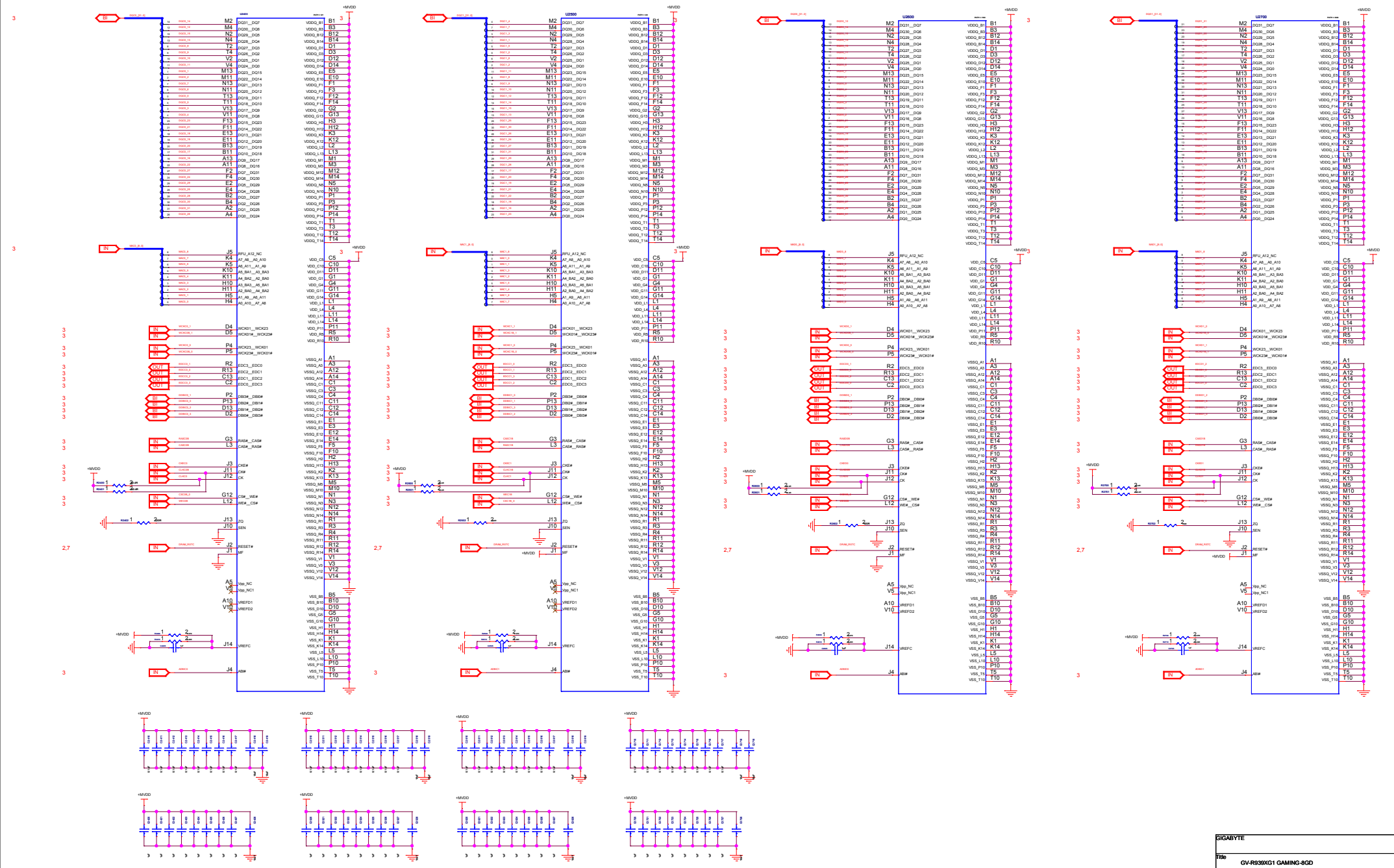

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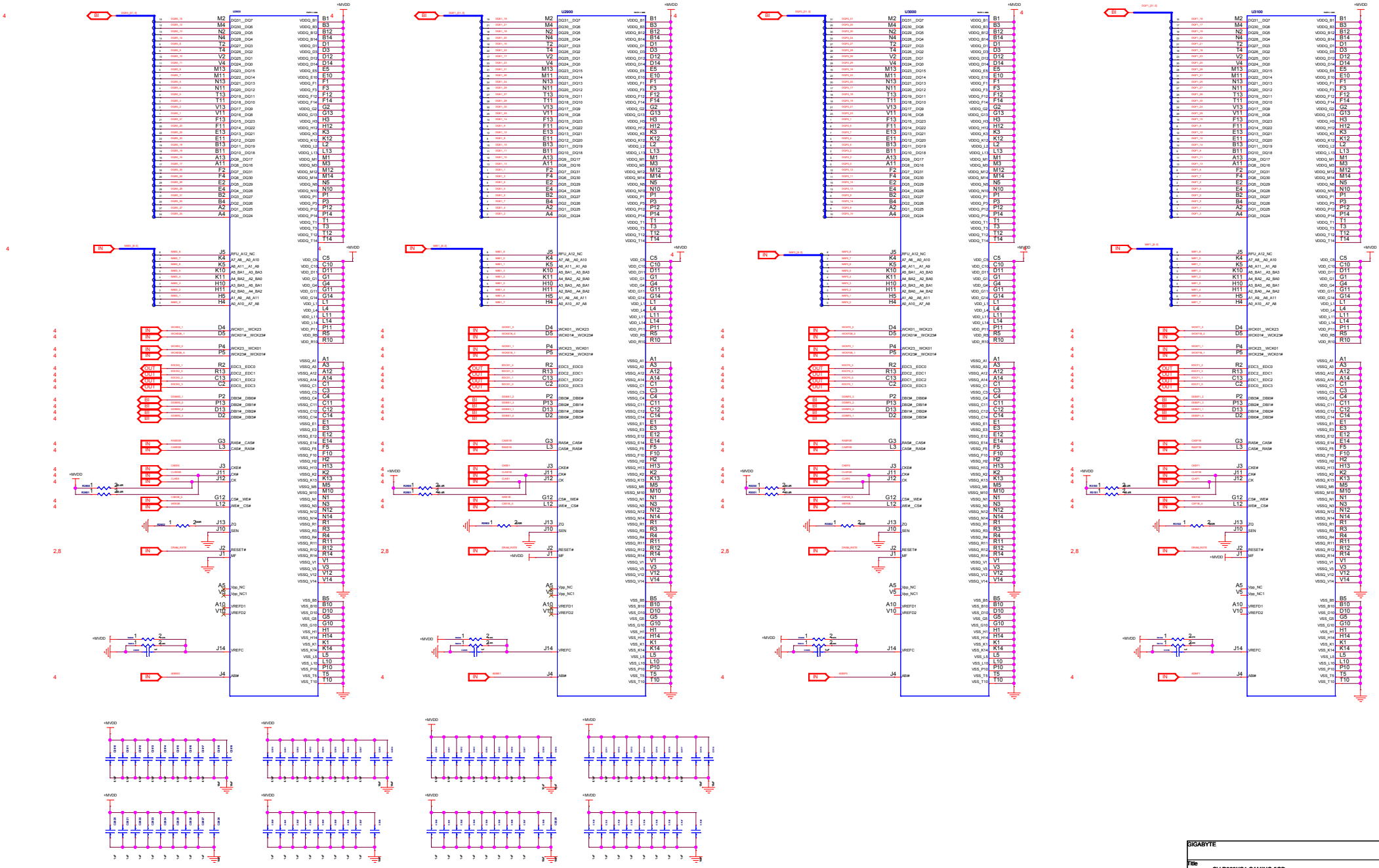

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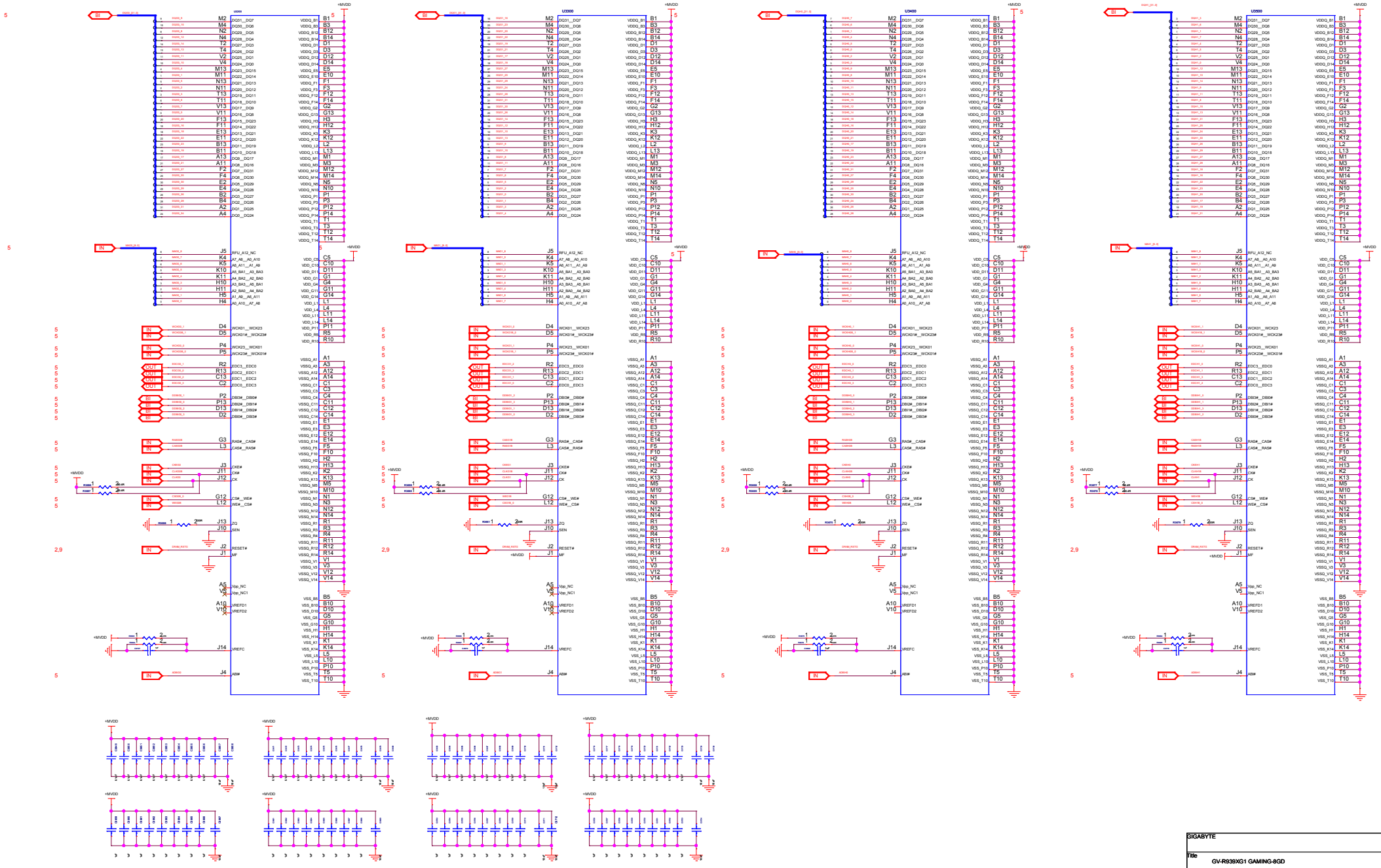

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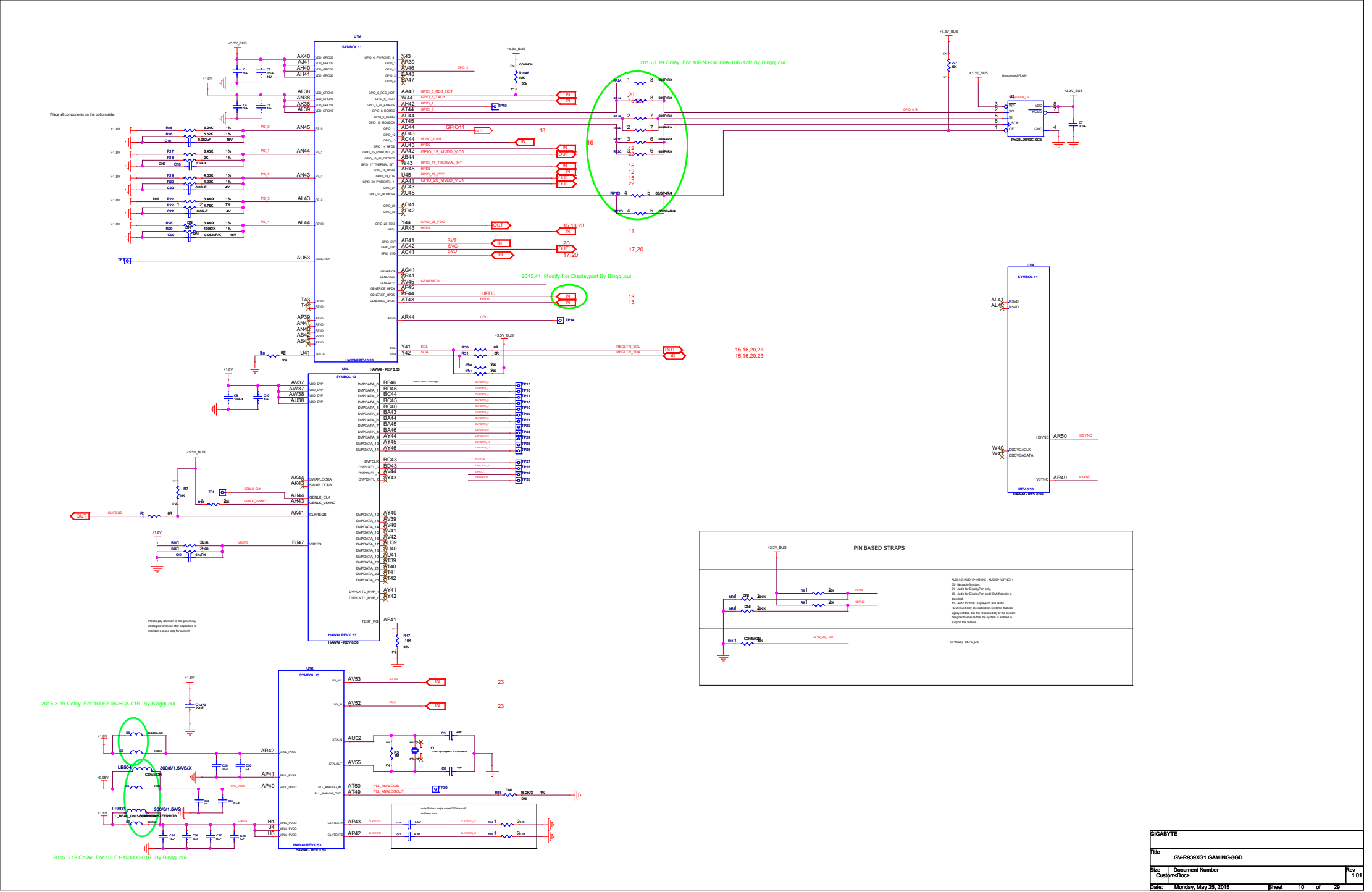

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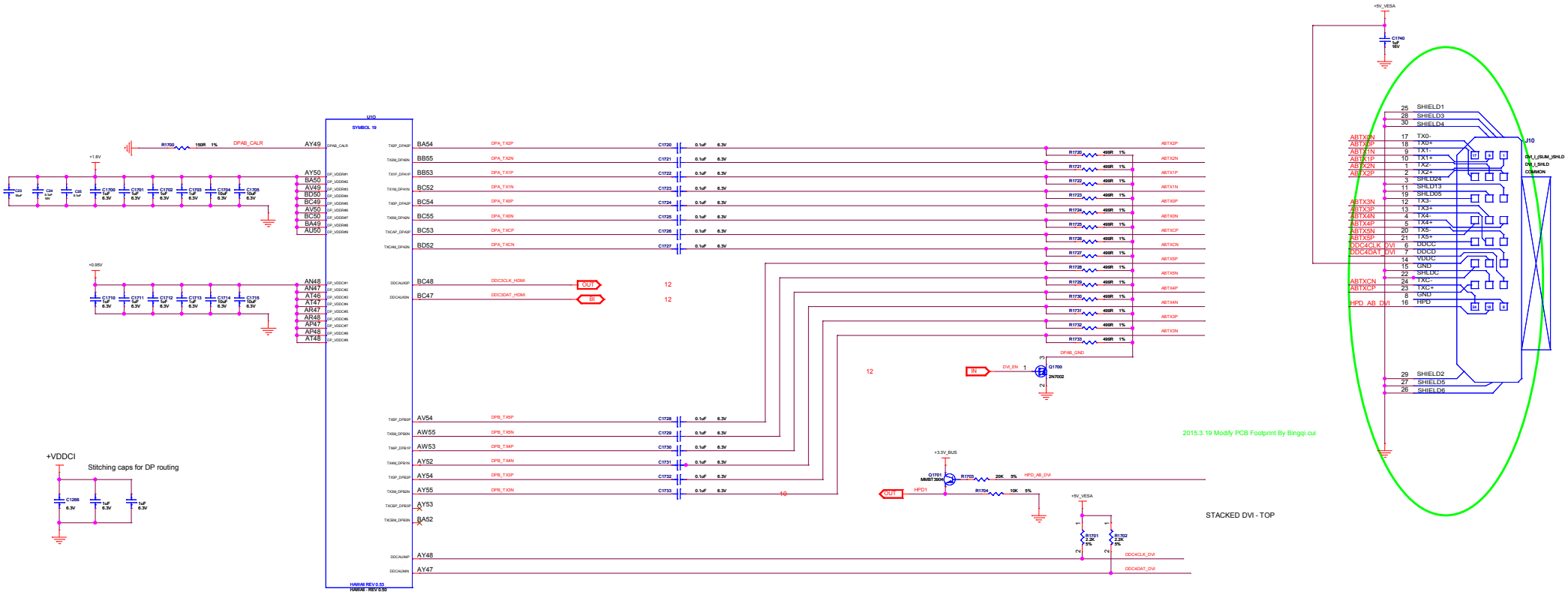

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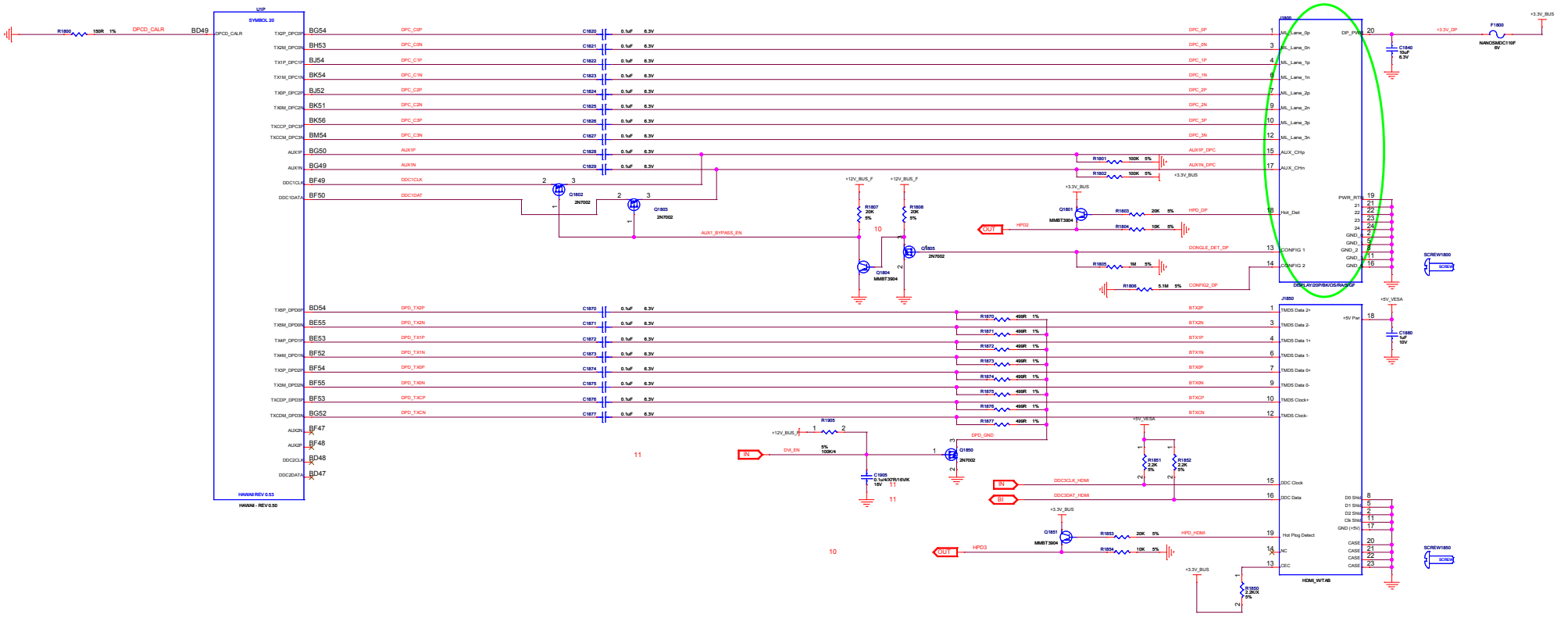

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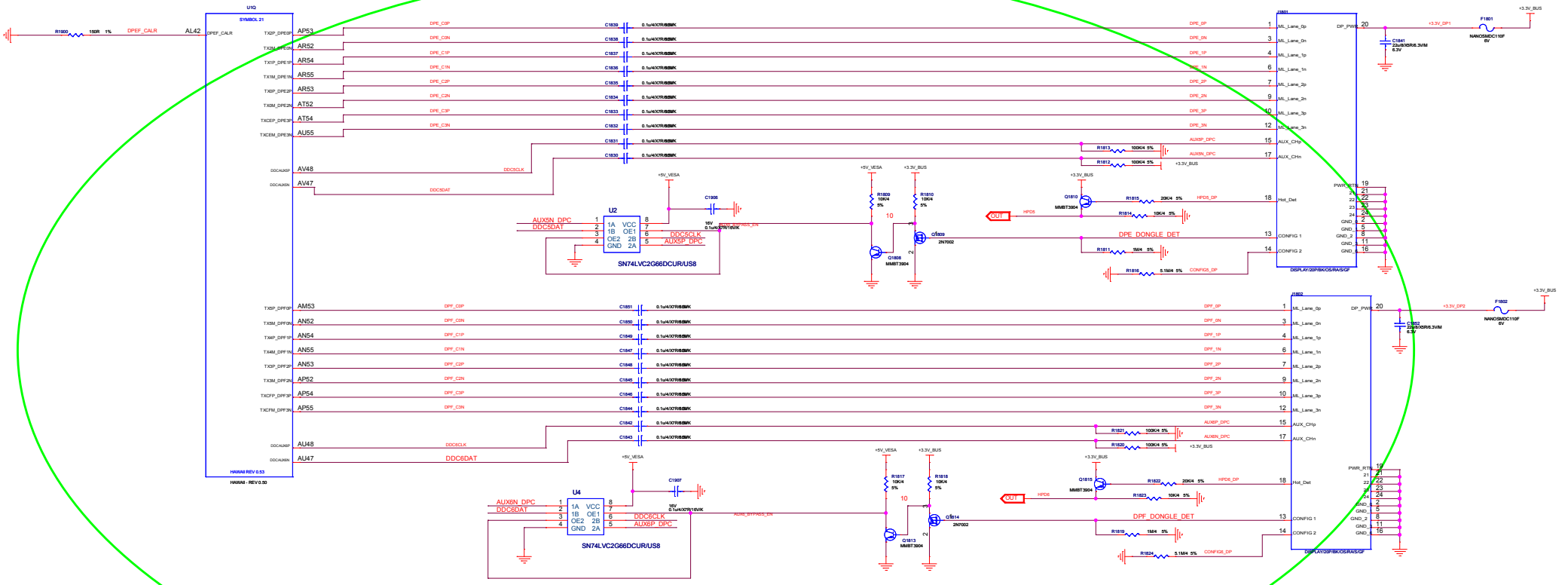
2015.41. Modify For Displayport *3 By Bingqi.cui



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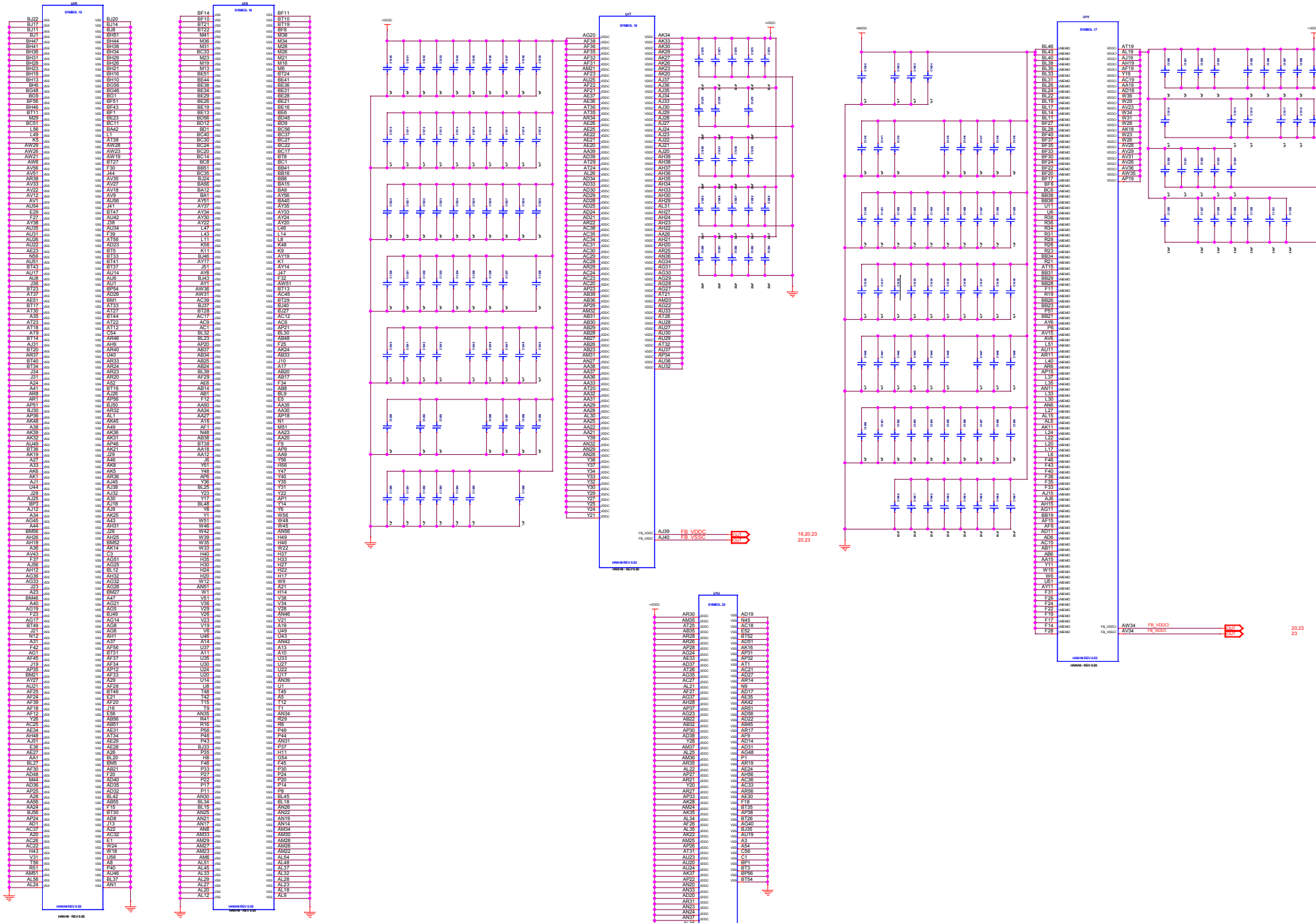

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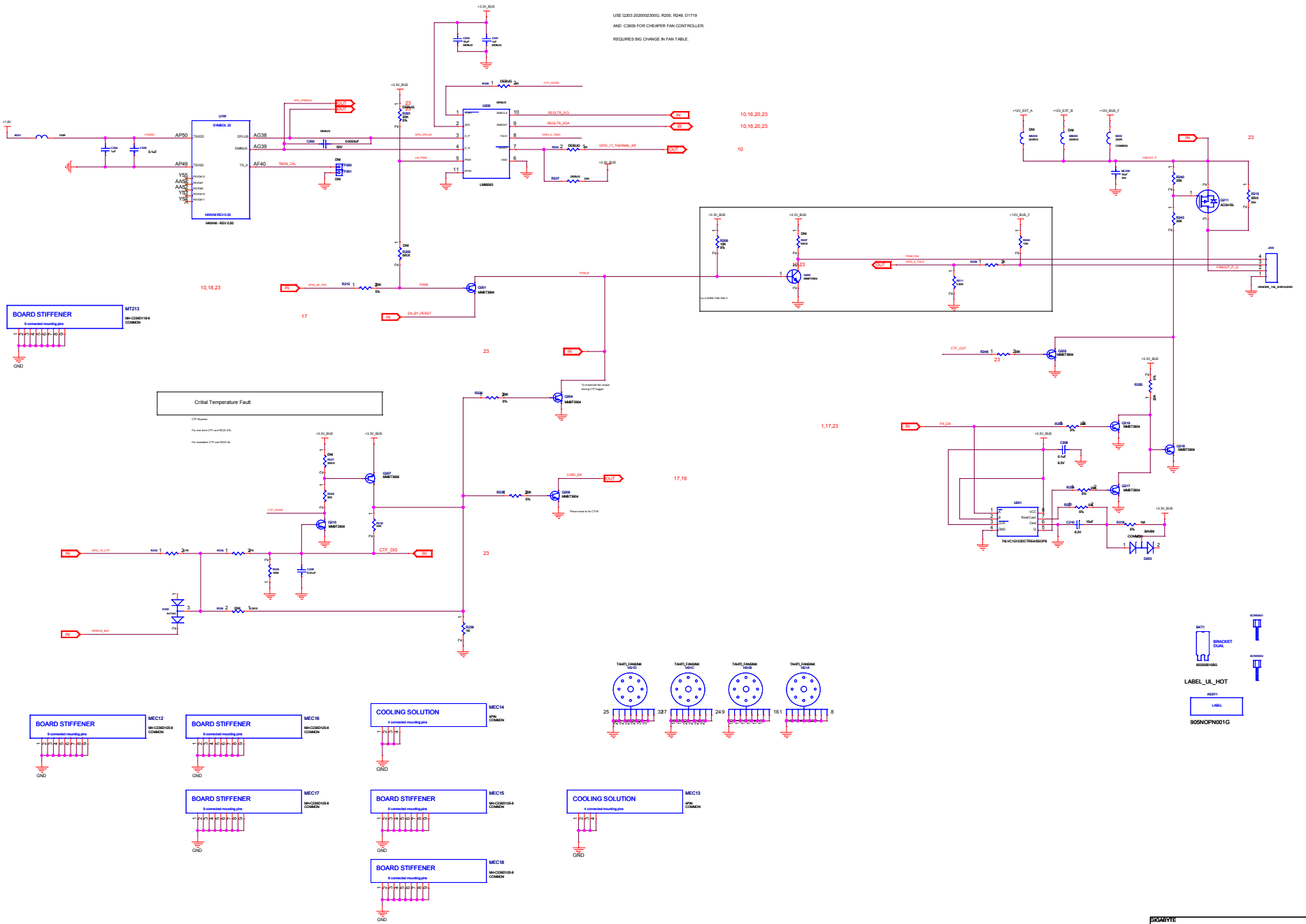

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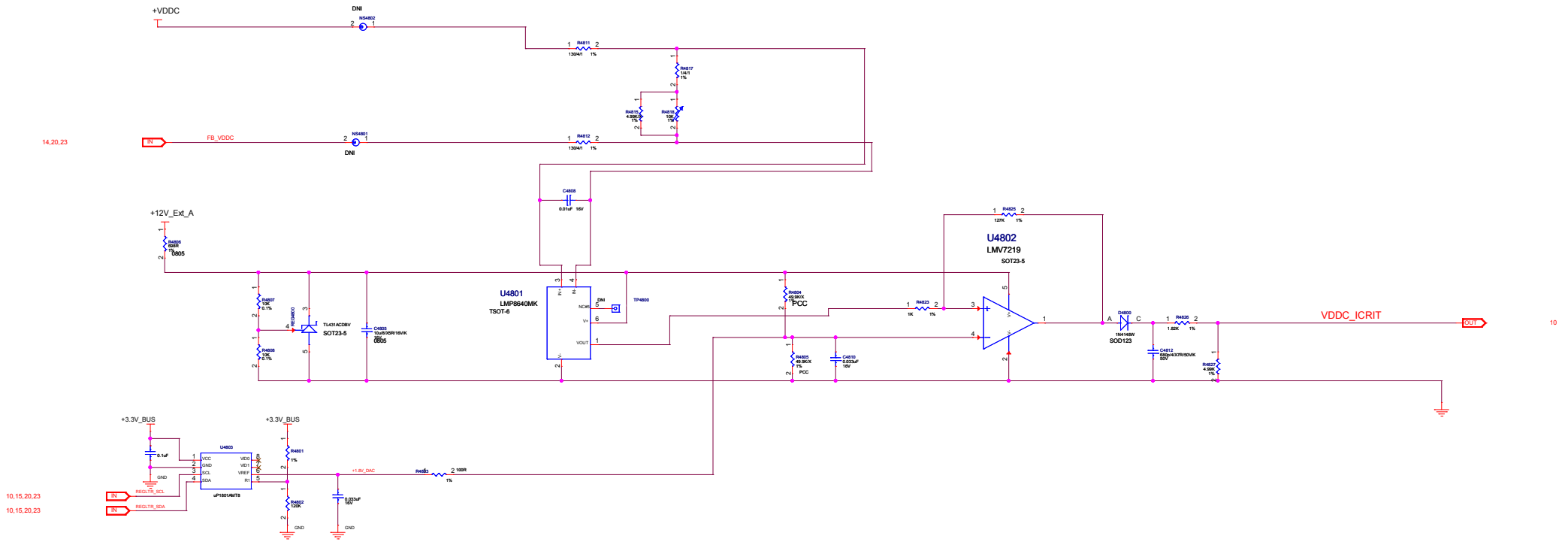

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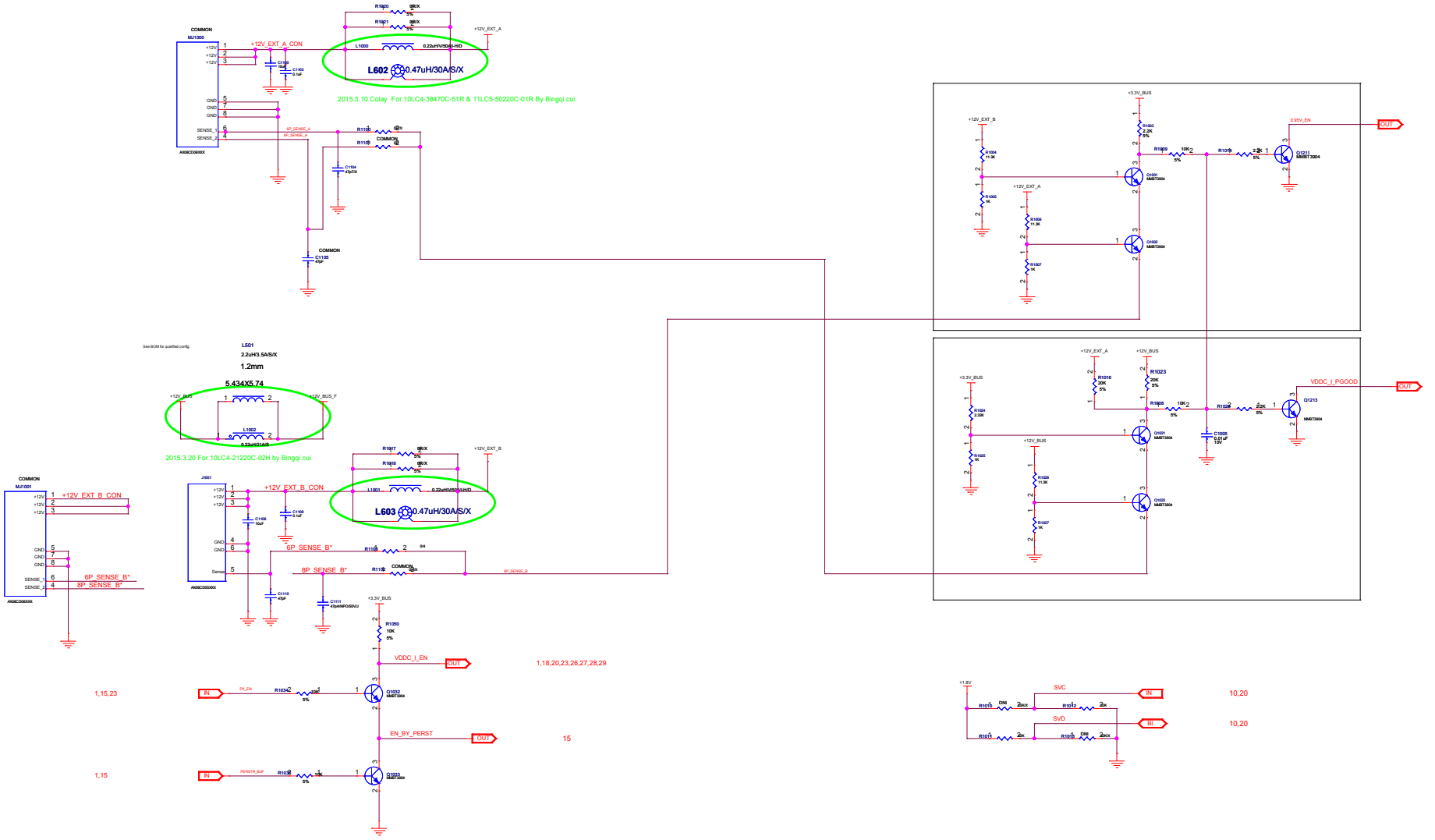

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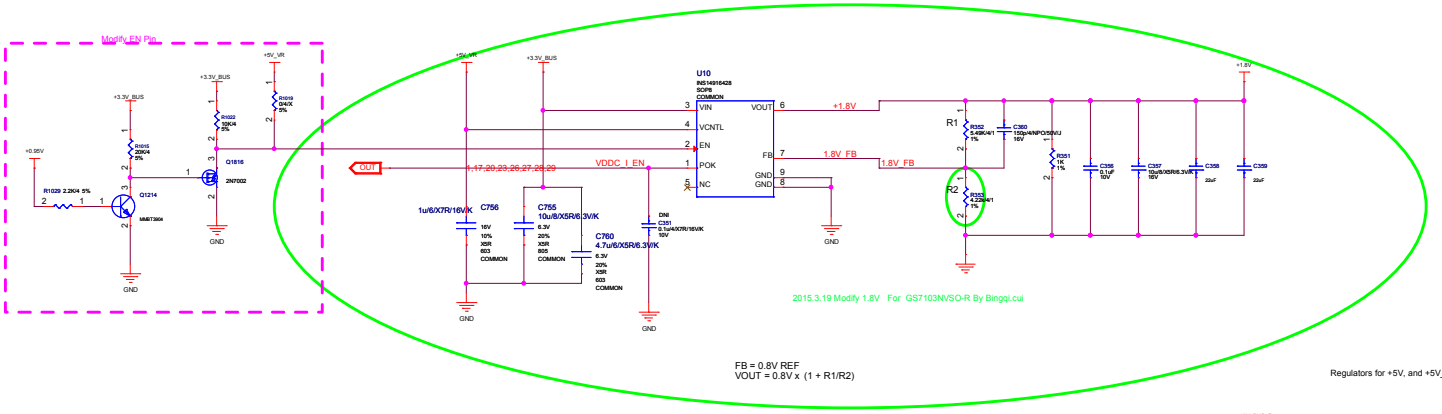
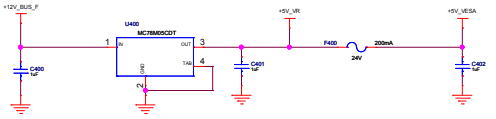
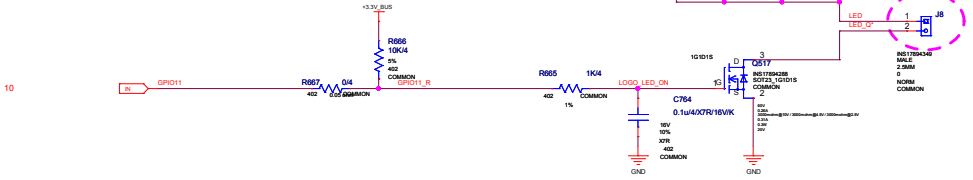


FB = 0.8V REF
VOUT = 0.8V x (1 + R1/R2)

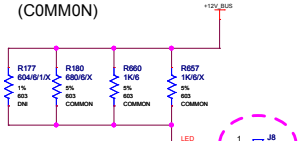
Regulators for +5V, and +5V_VESA



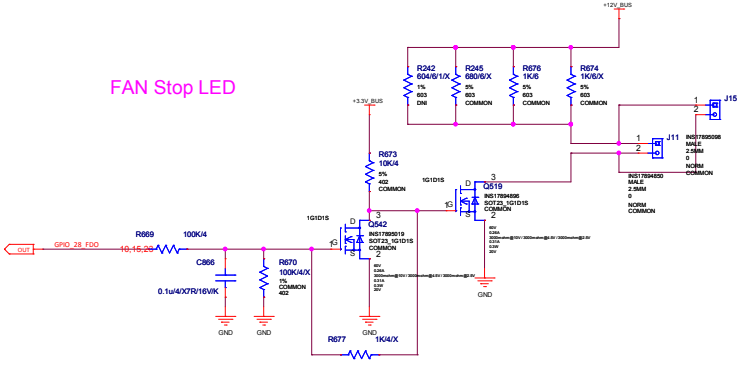
GeForce Logo LED



LED HEADER
(C0MM0N)



FAN Stop LED



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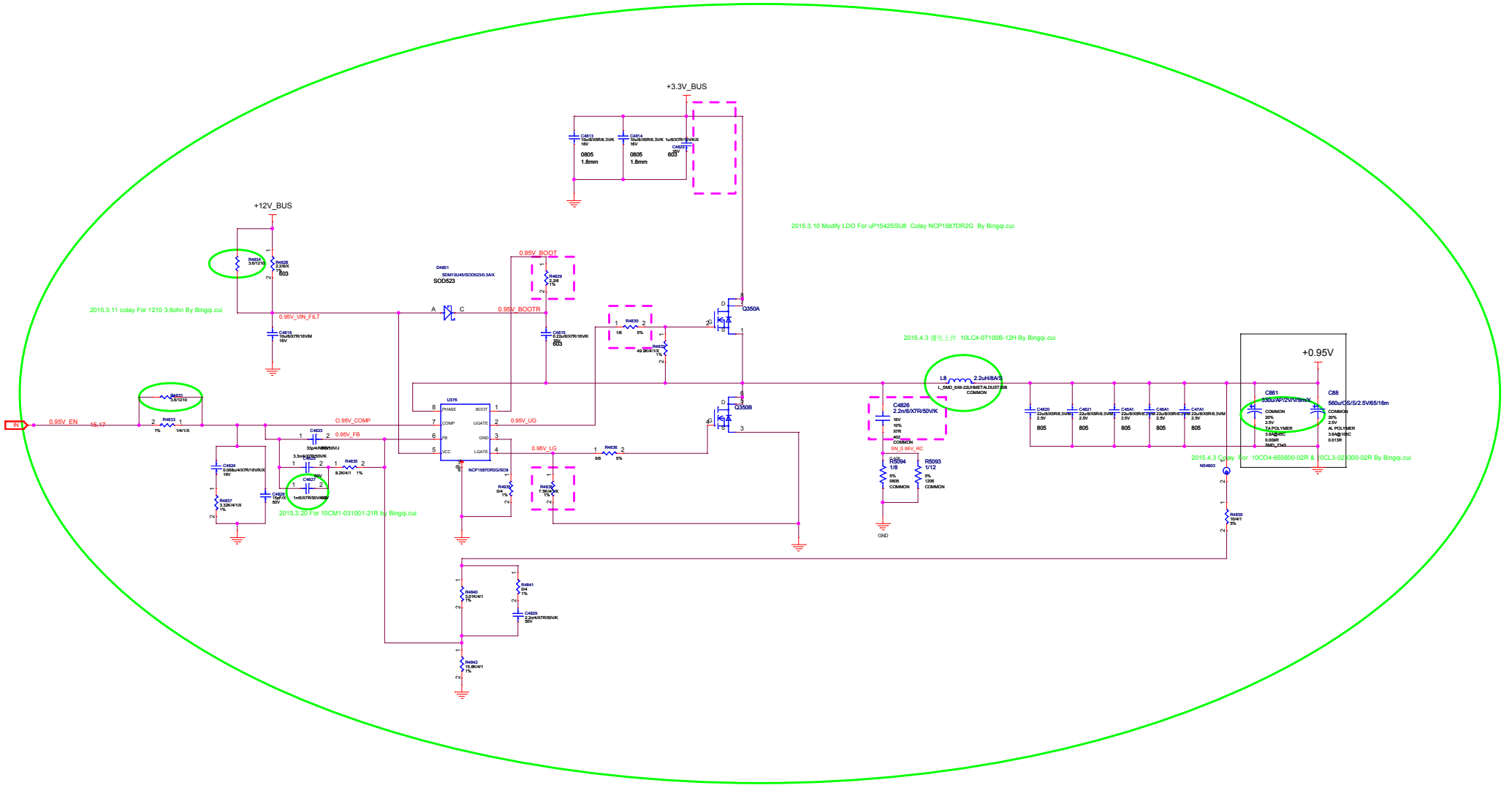

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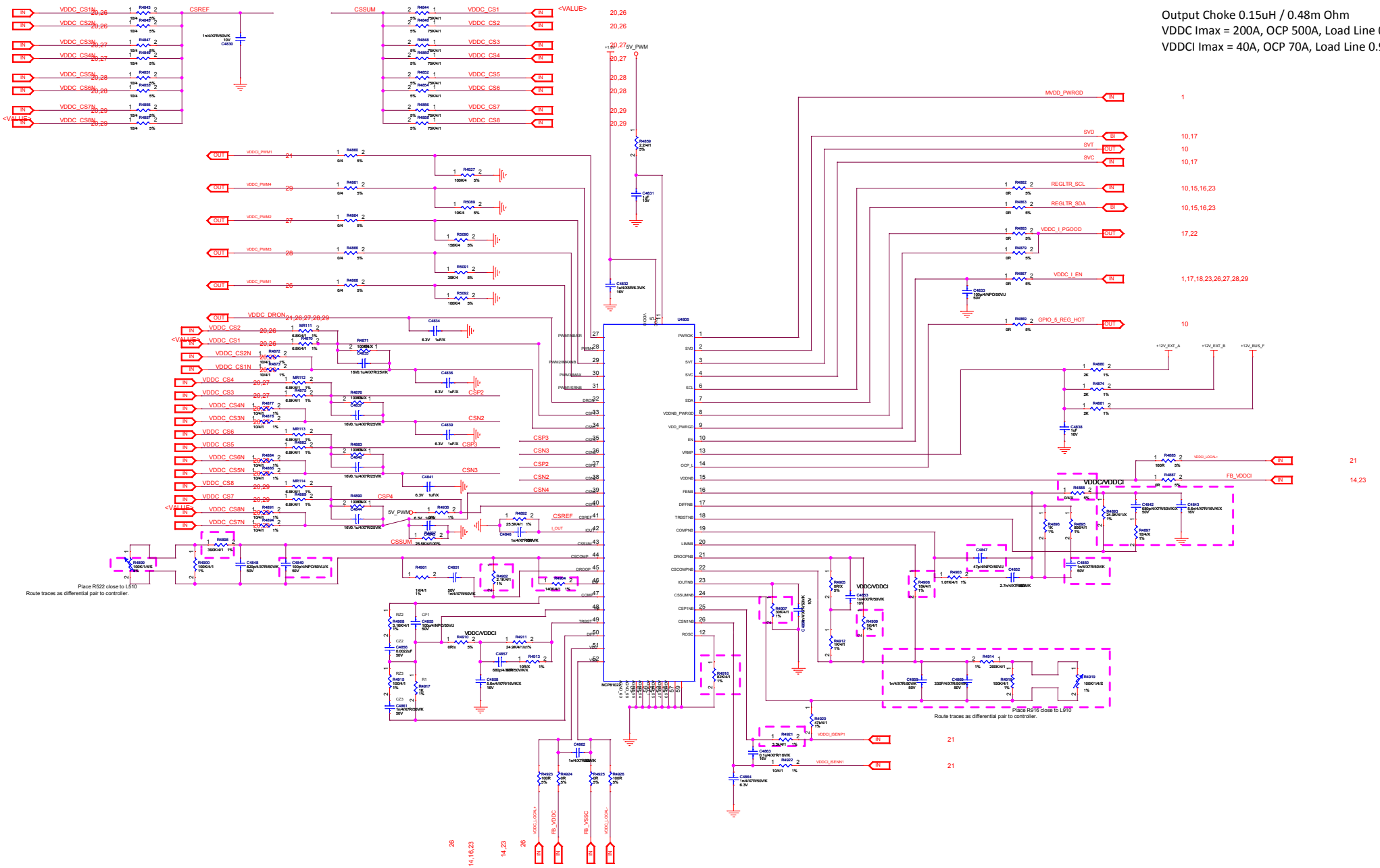
Output Choke 0.15uH / 0.48m Ohm
VDDC Imax = 200A, OCP 500A, Load Line 0.9mOhm
VDDCI Imax = 40A, OCP 70A, Load Line 0.9mOhm



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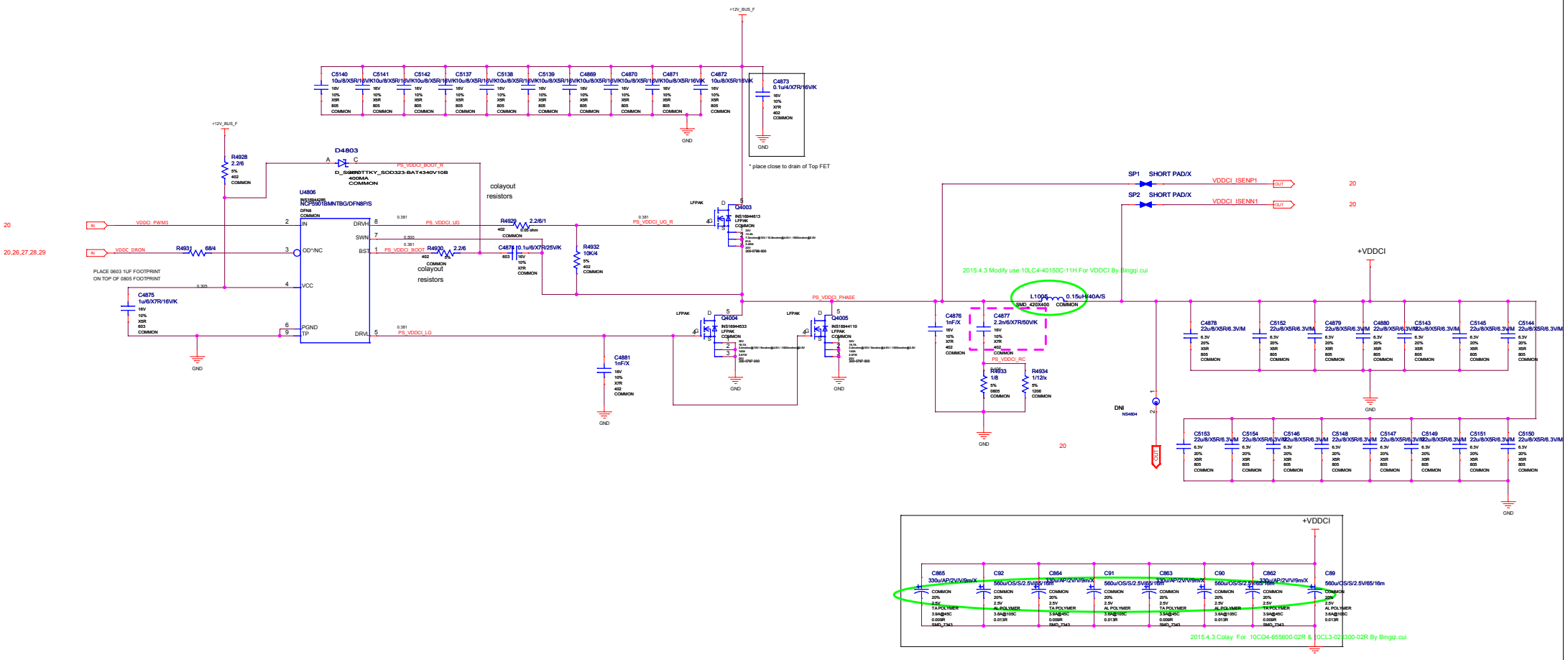

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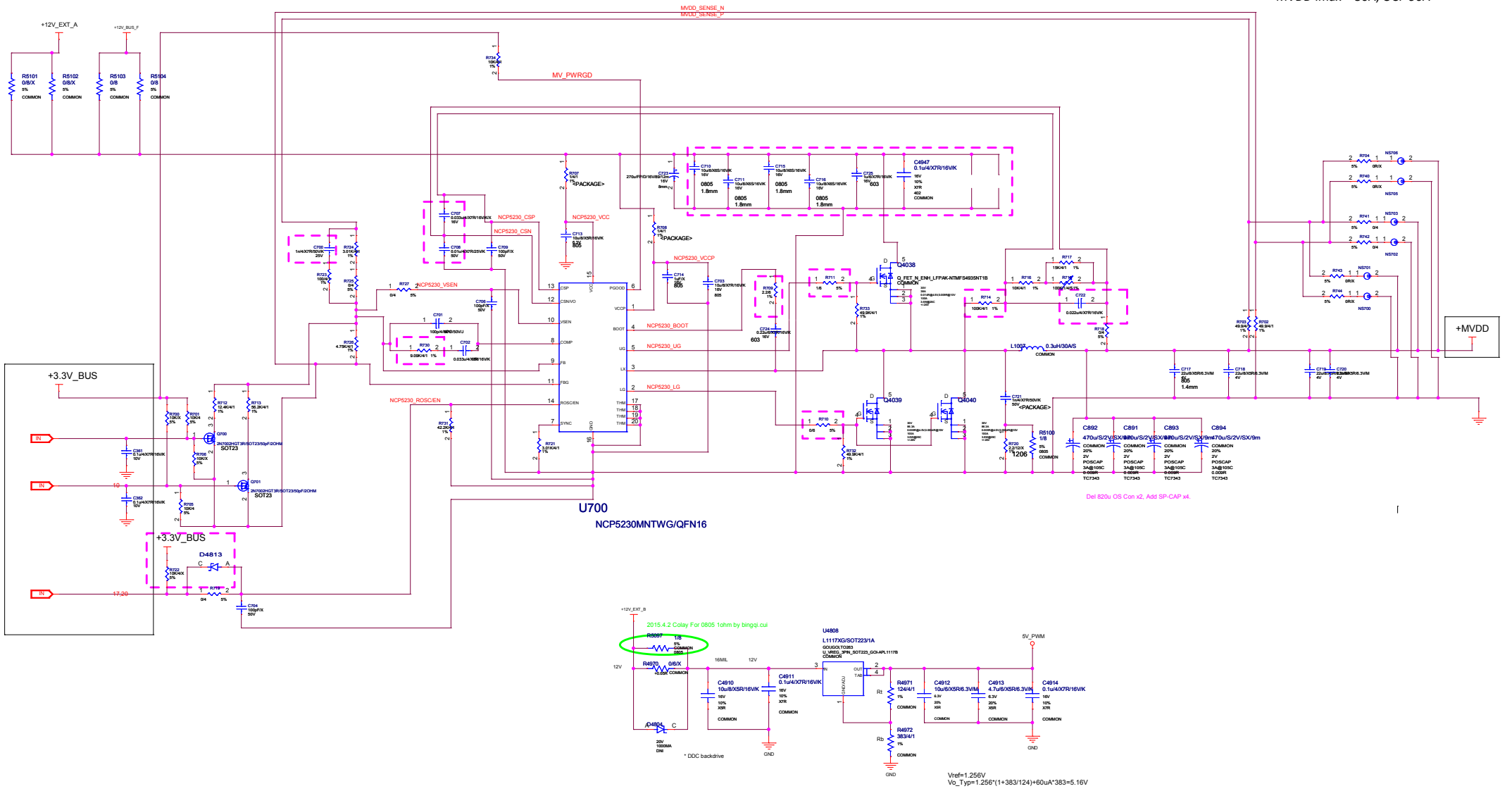
Output Choke 0.3uH / 1.2m Ohm
MVDD Imax = 30A, OCP 90A



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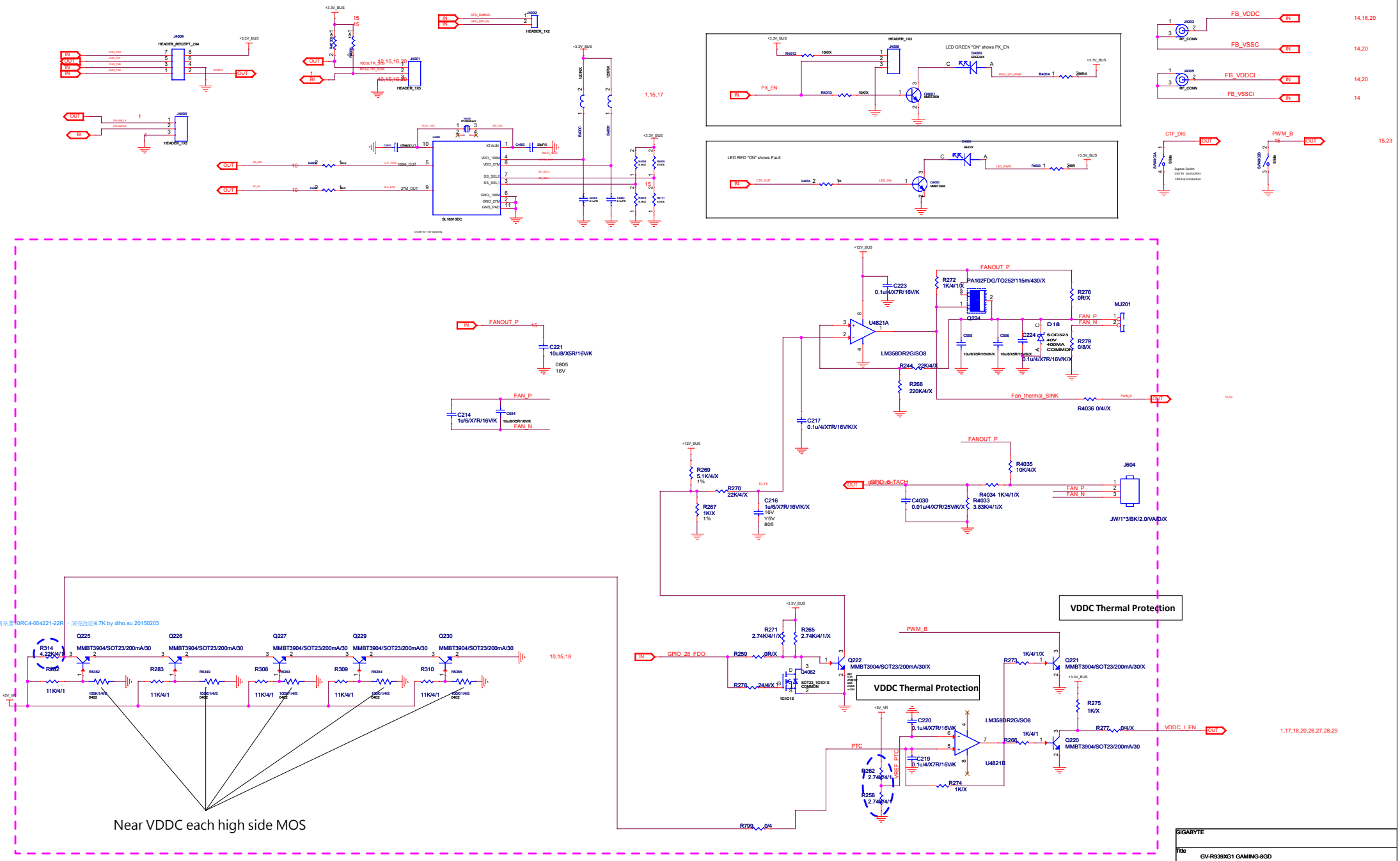

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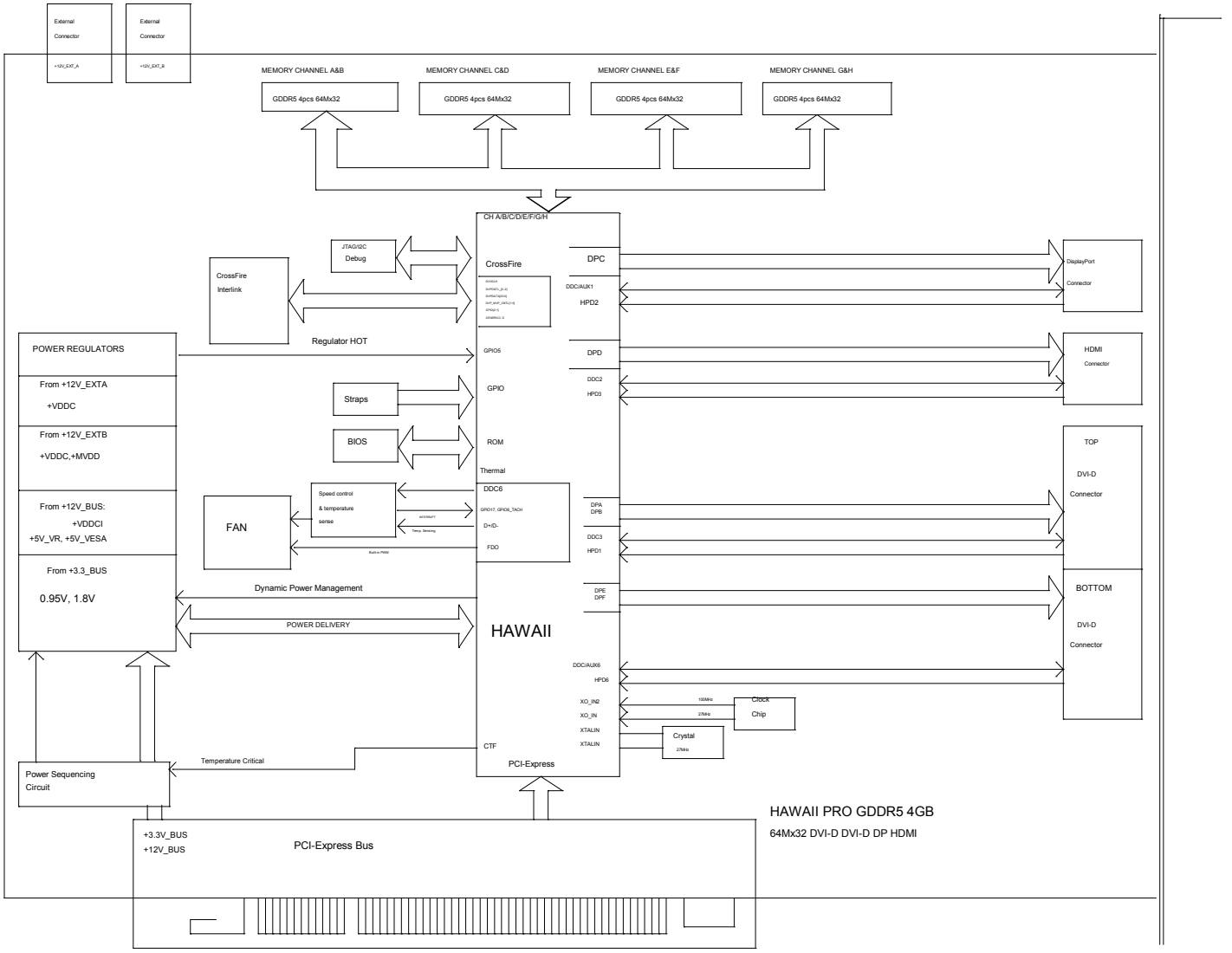

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AMD	TITLE: Hawaii XT CR	DOCUMENT NUMBER: 105-C67900-00B	DATE: Mon Jan 13 03:07:00 2014	SHEET NUMBER: 26 OF 26	REV: 1.0

REVISION HISTORY

ENGINEER: Anatoly FRidman

NOTES: NOTE

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AMD - GRAPHICS
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MARKHAM, ONTARIO, L3T 7X6

SCH Rev	PCB Rev	Date	REVISION DESCRIPTON
1	00A	Oct 03 2013	1) Based on C672. 2) VDDC/VDDCI regulator changed to C671 solution. 3) VR_HOT circuitry deleted and used C671 solution.

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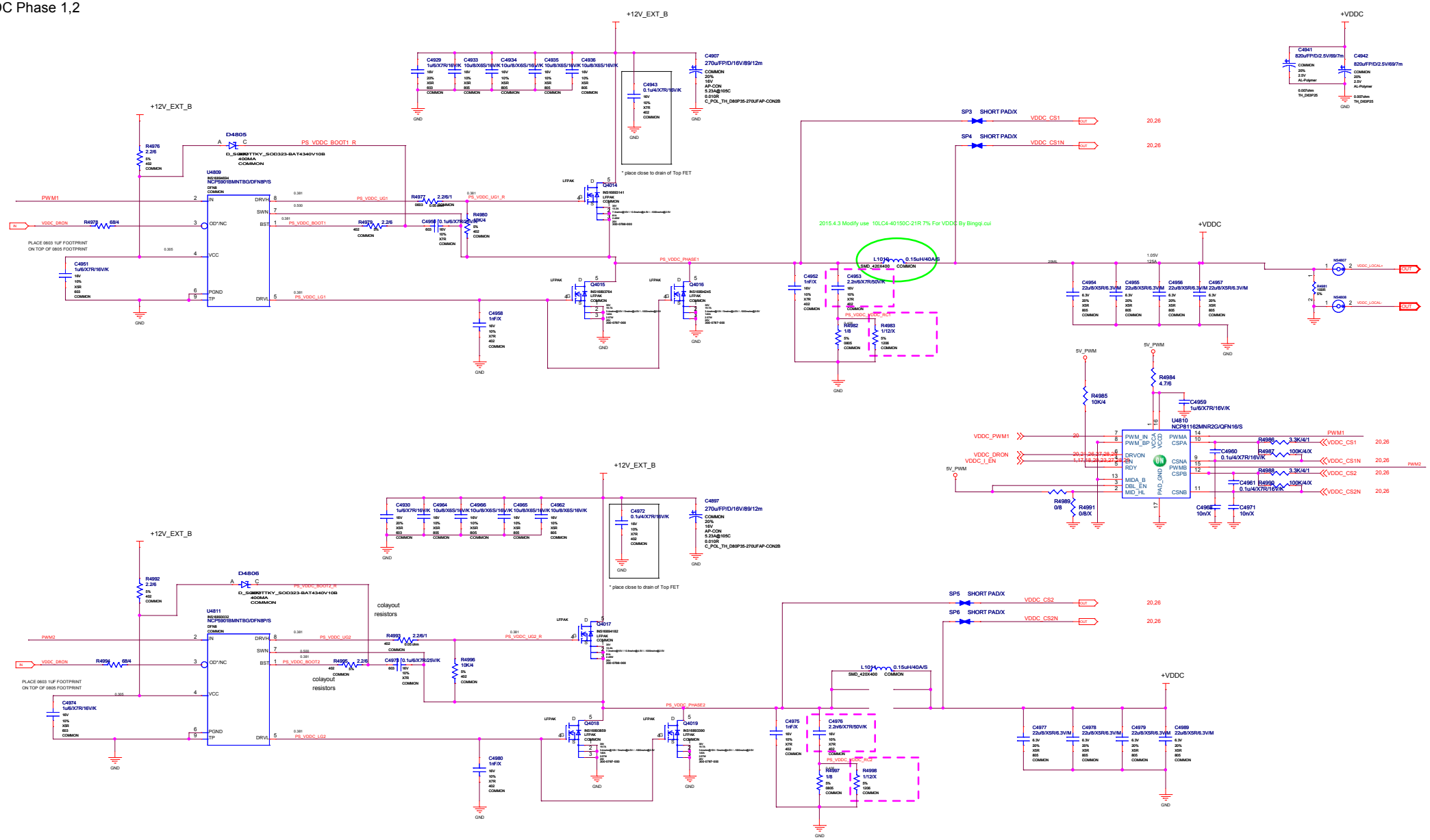
VDDC Phase 1,2



ASSEMBLY
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PS: NVVDD Phase 1,2

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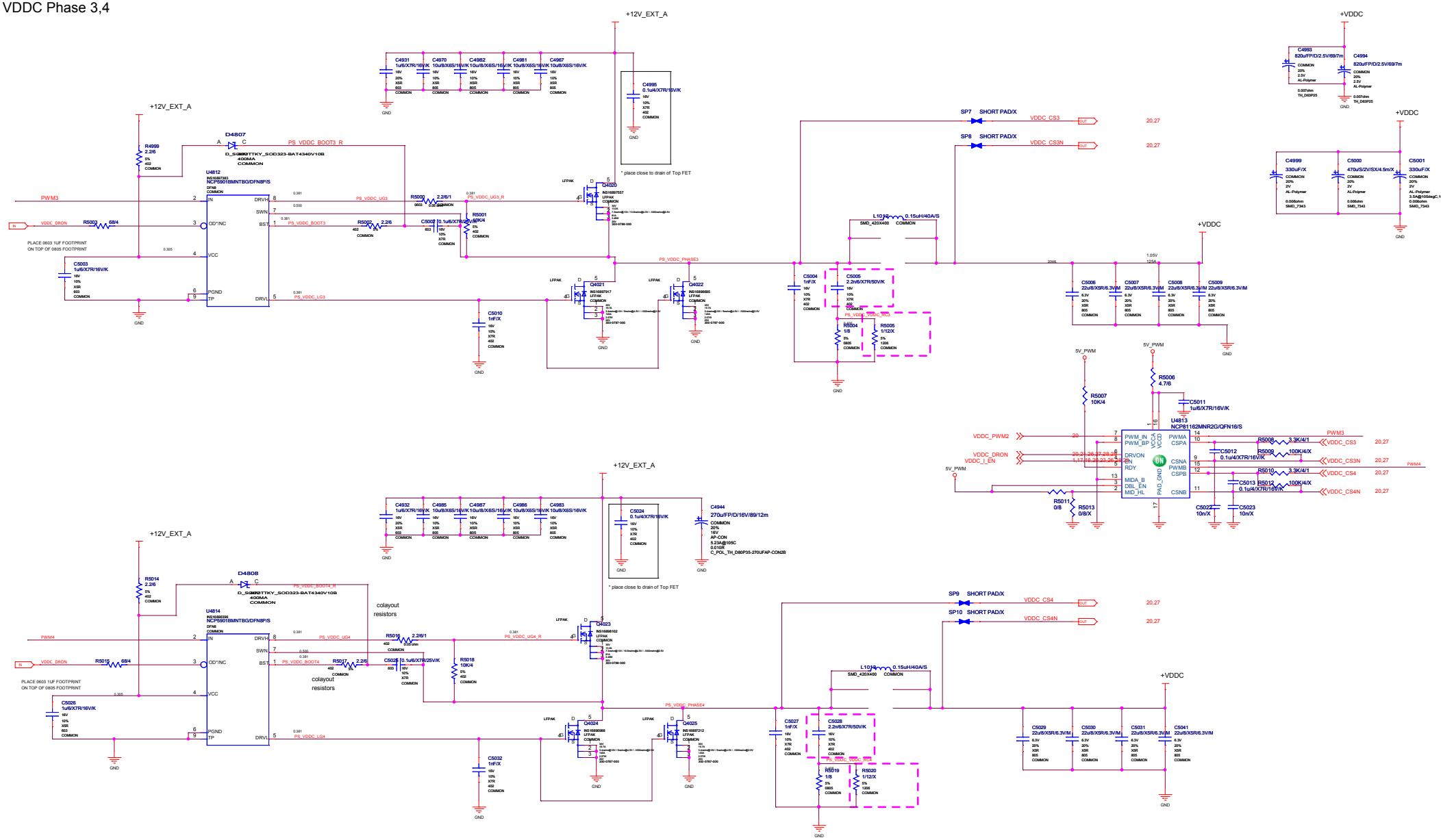
PS_ VDDC Phase 3,4



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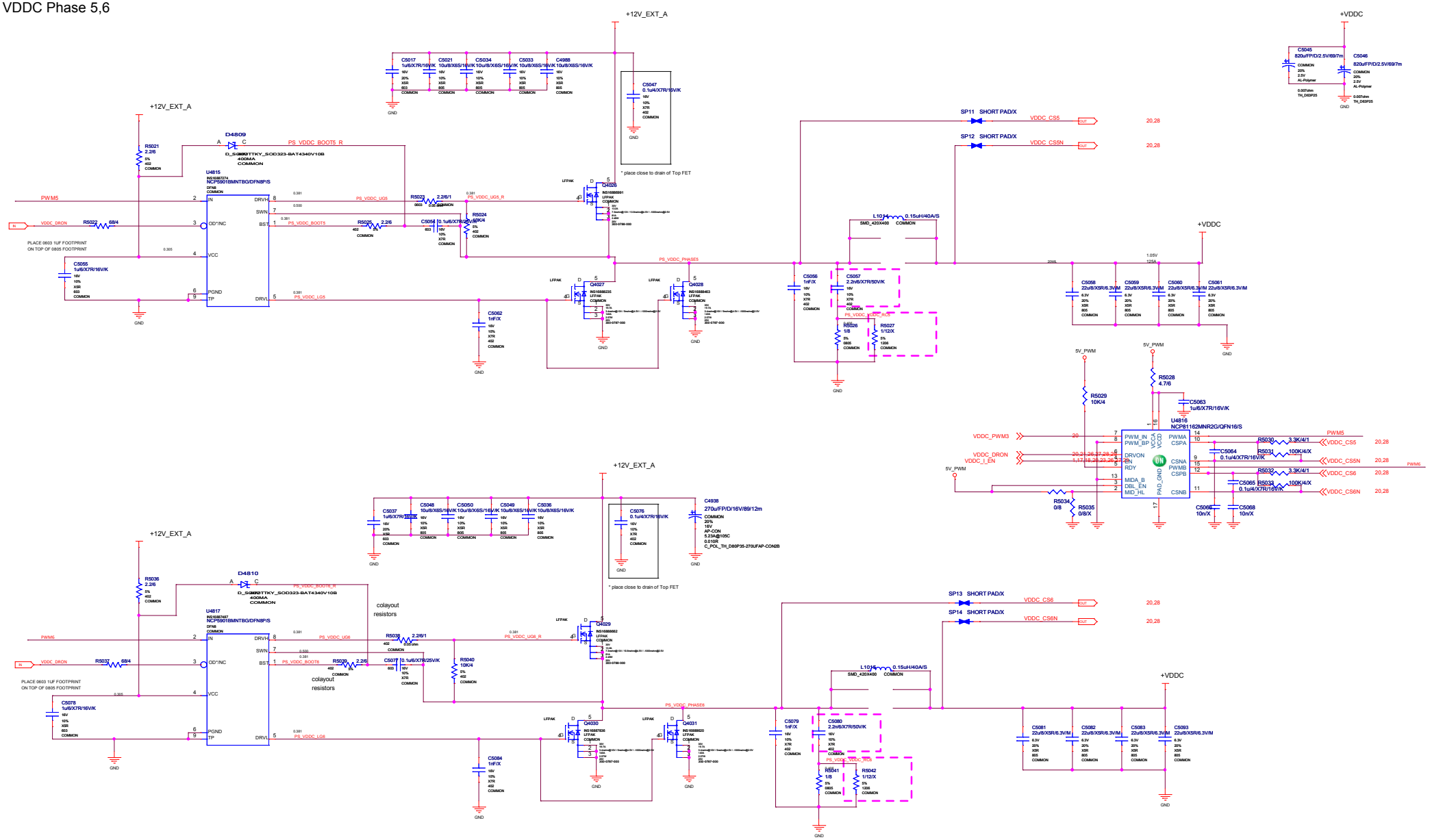
PS_ VDDC Phase 5,6



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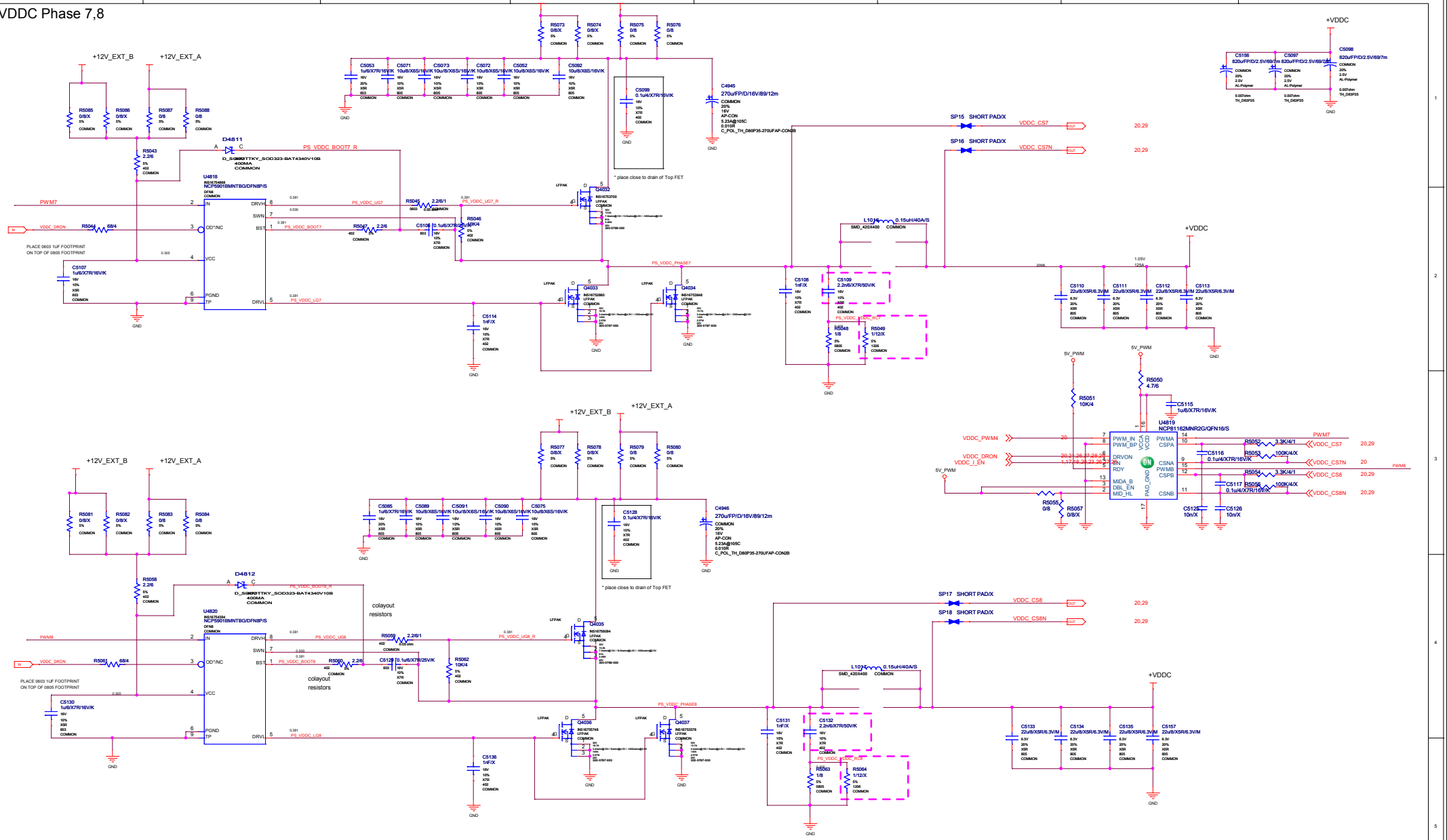
PS_VDDC Phase 7,8



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