

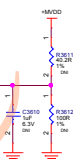
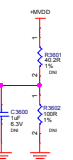
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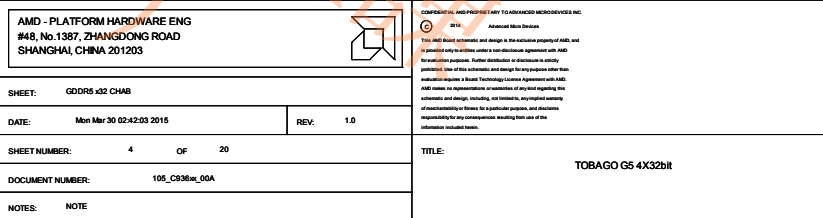
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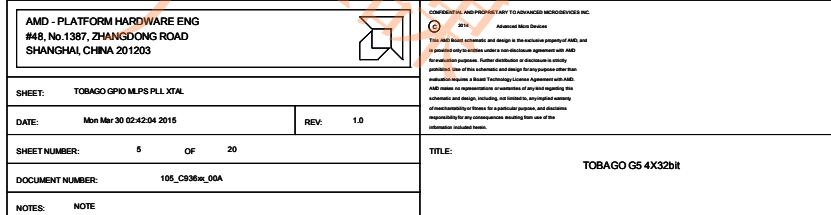
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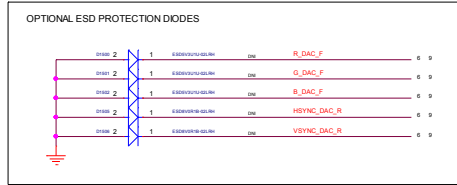
TITLE:

TOBAGO G5 4X32bit



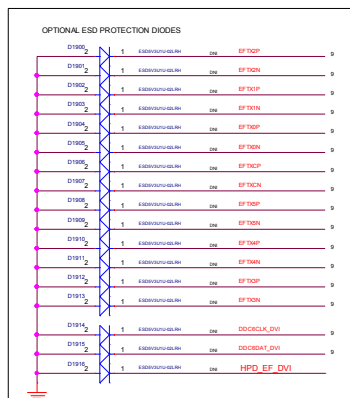
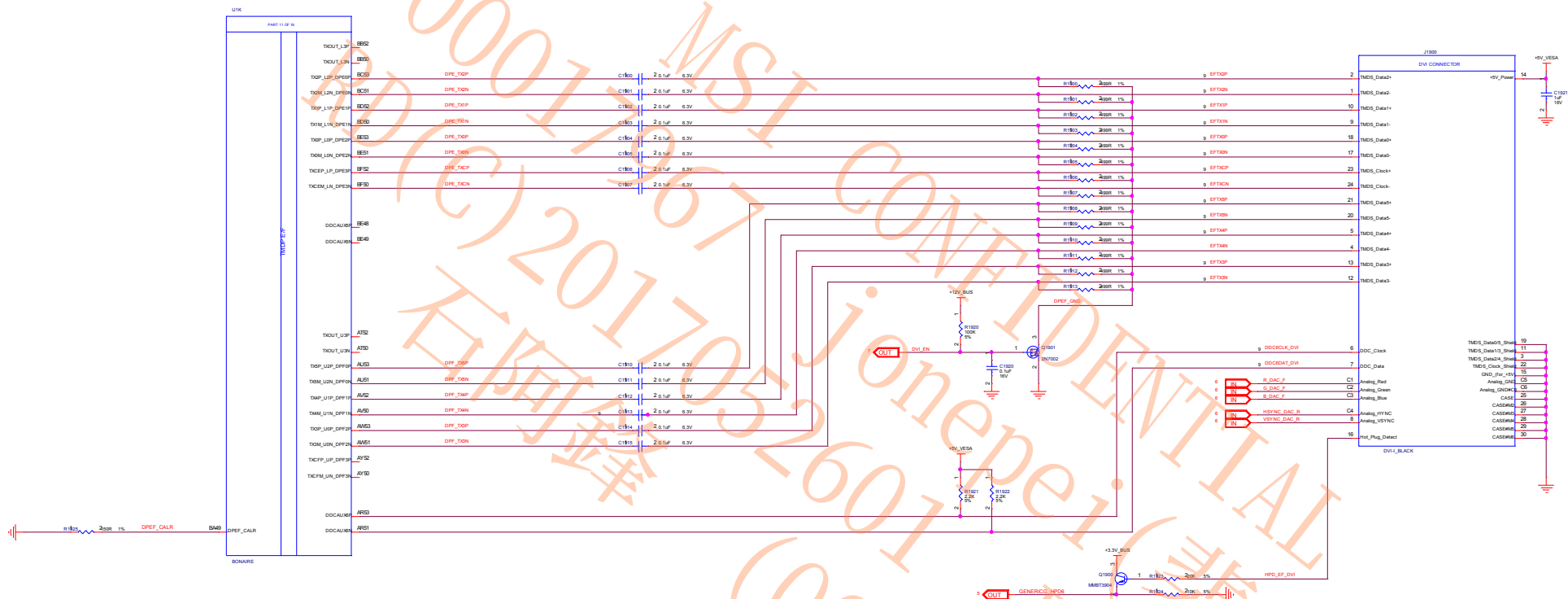




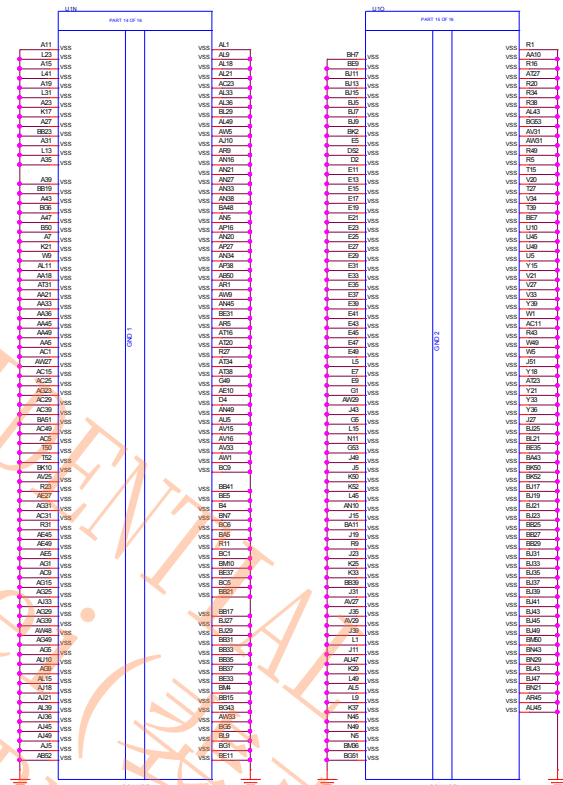
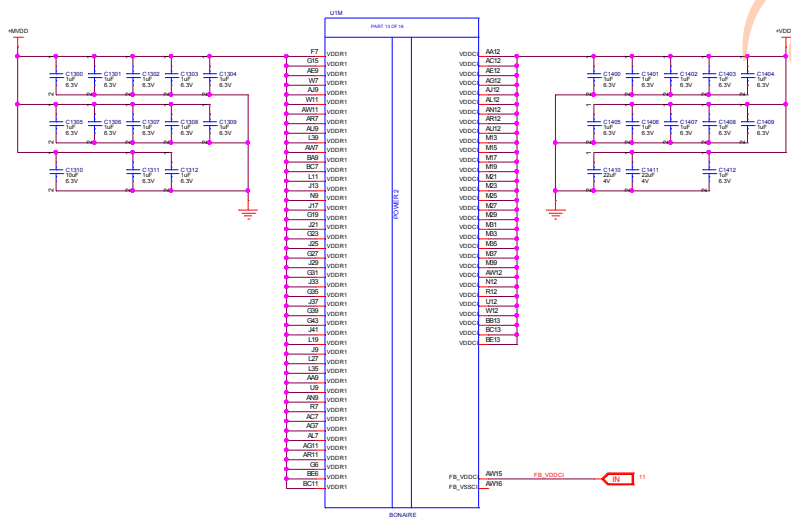
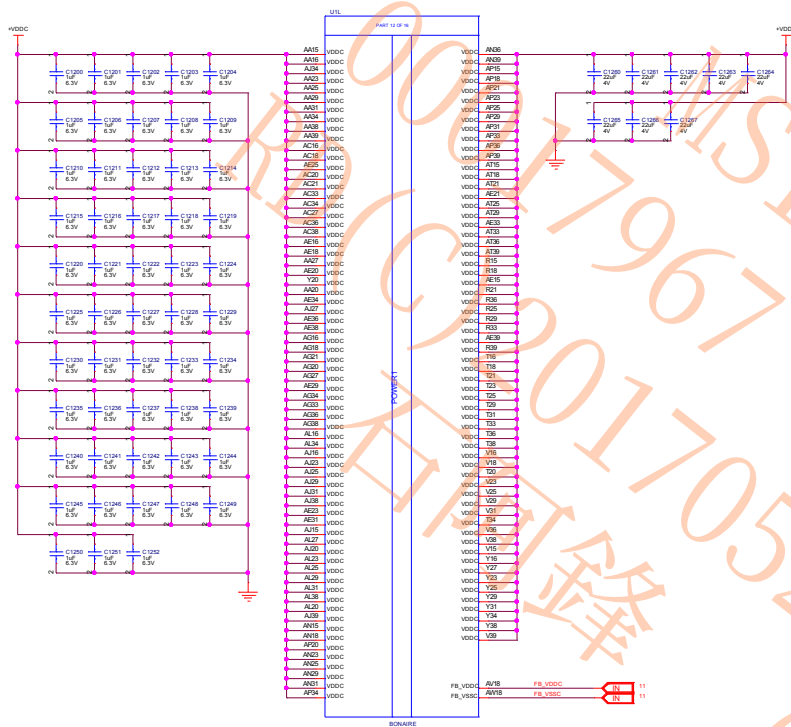


AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203	
SHEET: TOBAGO DAC	
DATE: Mon Mar 30 02:42:05 2015	REV: 1.0
SHEET NUMBER: 6 OF 20	
DOCUMENT NUMBER: 105_C936w_00A	
NOTES: NOTE	

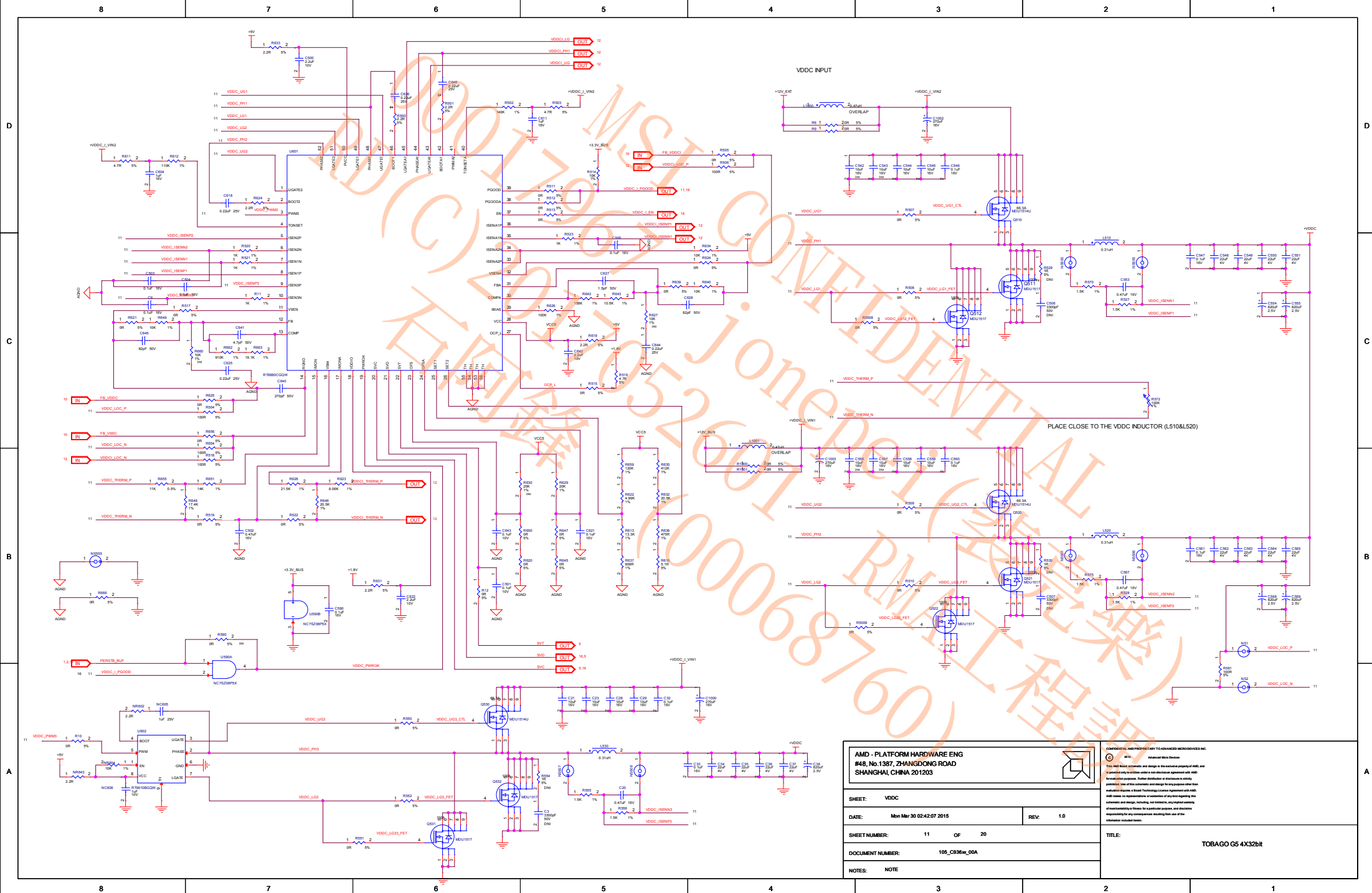
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SHEET: T0BAGO TMDPEF					
DATE: Mon Mar 30 02:42:06 2015		REV: 1.0			
SHEET NUMBER: 9 OF 20				TITLE: T0BAGO G5 4X32bit	
DOCUMENT NUMBER: 105_C936w_00A					
NOTES: NOTE					



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SHEET: TOBAGO POWER GND		REV: 1.0		TITLE: TOBAGO GS 4X32bit	
DATE: Mon Mar 30 02:42:06 2015					
SHEET NUMBER: 10 OF 20					
DOCUMENT NUMBER: 105_C936w_00A					
NOTES: NOTE					



INPUT POWER SEQUENCE

ENABLE THRESHOLD

+1.8V >+1.4V
+0.95V FLOAT
+VDDC+VDDC >+1.8V
+MVDD FLOAT

POWER UP SEQUENCE

BUS RAILS (0.3V/12V UP) -> +1.8V >+0.95V	-> VDDC+VDDC -> MVDD
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INTERNAL CTF LATCH - 1.8V VDDC REQUIRED

VOLTAGE CONTROL

SVD POWER UP VOLTAGE (VDDC+VDDC)

SVC	SVD	VOLTAGE
0	0	1.7V
0	1	1.0V
1	0	0.9V
1	1	0.9V

+MVDD OUTPUT VOLTAGE

$V_{OUT} = V_{REF} * (1 + R_{FB}/R_{F2})$
 $R_{F2} = (R_{FB} * V_{REF}) / (V_{OUT} - V_{REF})$
 $V_{REF} = 0.8V$

AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
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SHEET: POWER MANAGEMENT

DATE: Mon Mar 30 02:42:09 2015

REV: 1.0

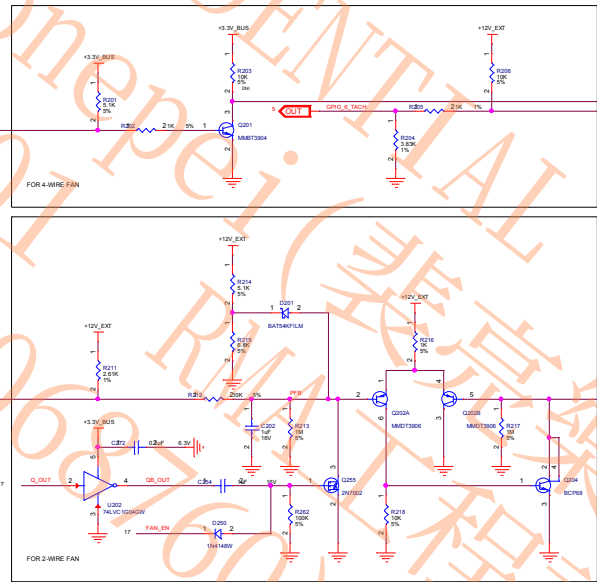
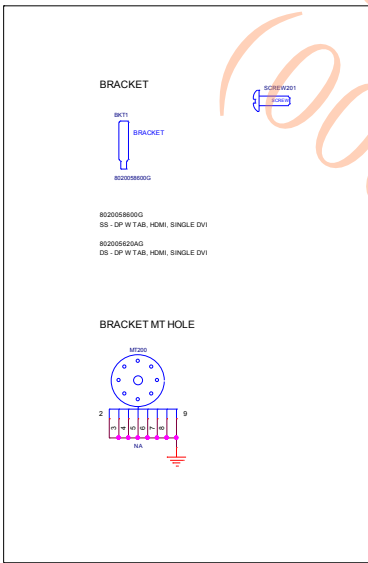
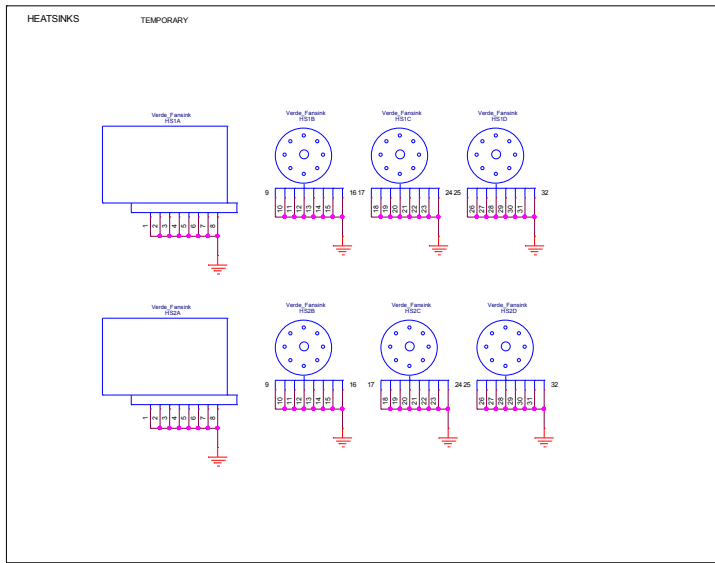
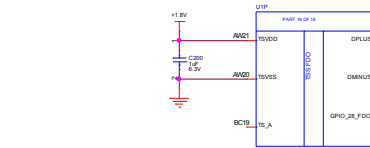
SHEET NUMBER: 16 OF 20

DOCUMENT NUMBER: 105_C936w_00A

NOTES: NOTE

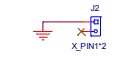
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TITLE: TOBAGO G5 4X32bit

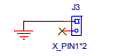


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SHEET: MECH AND THERMAMGMT	
DATE: Mon Mar 30 02:42:09 2015	REV: 1.0
SHEET NUMBER: 17 OF 20	
DOCUMENT NUMBER: 105_C936w_00A	
NOTES: NOTE	

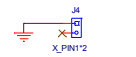
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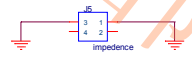
TOP
Single end
RGB
50 ohm +/- 10%
0.102mm
4.02 mils



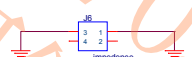
L3
Single end
Memory
48 ohm +/- 5 ohm
0.11mm
4.33 mils



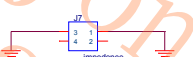
Bottom
Single end
Memory
48 ohm +/- 5 ohm
0.11mm
4.33 mils



TOP
Different
TMDS
80 ohm +/- 10 %
0.11 mm / 0.16 mm
4.33 mils / 6.3 mils

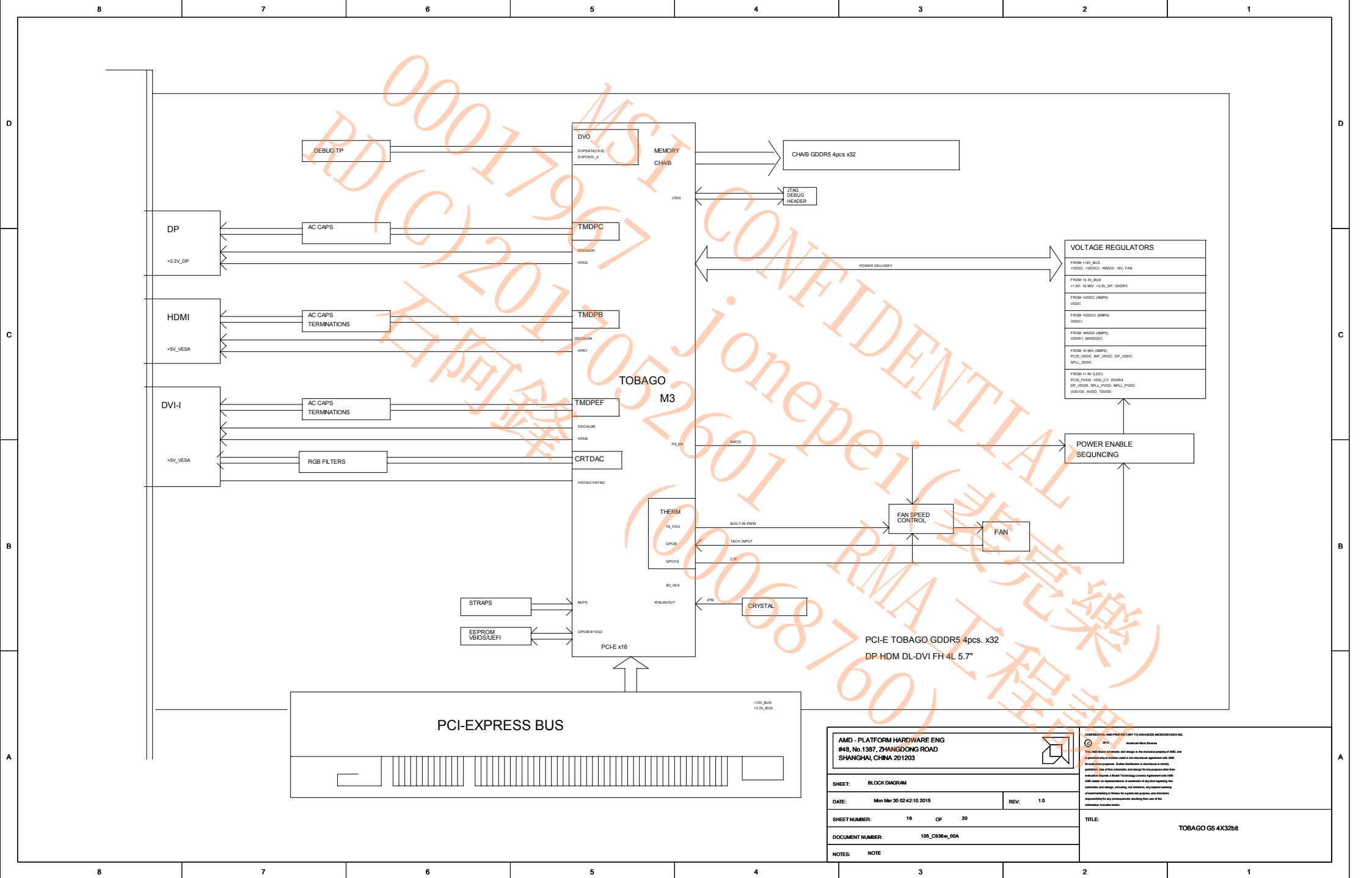


L3
Different
Memory clock
80 ohm +/- 10 %
0.11 mm / 0.16 mm
4.33 mils / 6.3 mils



Bottom
Different
PCIE
85 ohm +/- 10 %
0.112 mm / 0.188 mm
4.41 mils / 7.04 mils

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SHEET: DEBUG CIRCUITS			TITLE: TOBAGO G5 4X32bit
DATE: Mon Mar 30 02:42:10 2015	REV: 1.0		
SHEET NUMBER: 18 OF 20			
DOCUMENT NUMBER: 105_C936w_00A			
NOTES: NOTE			



8		7		6		5		4		3		2		1	
AMD				TITLE: TORAGO G5 4X32bit		DOCUMENT NUMBER: 105_C93bex_00A		DATE: Wed Feb 11 05:56:21 2015		SHEET NUMBER: 20 OF 20		REV: 1.0			
REVISION HISTORY				ENGINEER: PEAK, DONG		NOTES: NOTE		CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRODEVICES INC. This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure to other parties, even if this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representation or warranty of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of this schematic without notice.		C 944 Advanced MicroDevices		AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203			
SCH Rev		PCB Rev		Date		REVISION DESCRIPTION									
0		00A		02/10/2015		INITIAL DESIGN									

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