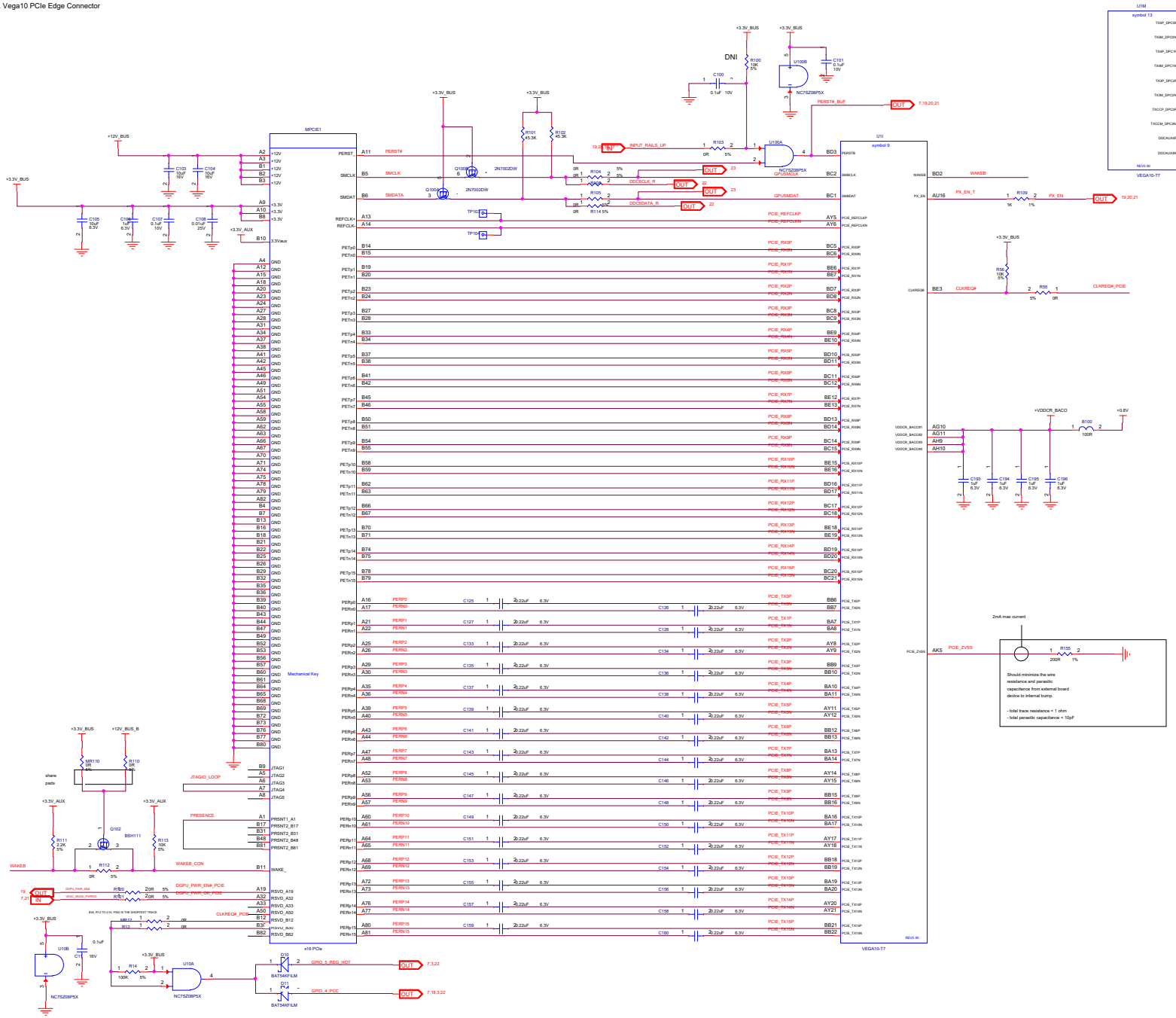
1. Vega10 PCIe Edge Connector



SYMBOL LEGEND

DNI	DO NOT INSTALL
b or #/	ACTIVE LOW
BUO	BRING UP ONLY
	DIGITAL GROUND
	ANALOG GROUND

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6	Vega10 - TMDPEF 2xDP
7	Control - VDDC / MVDD
8	Reg - VDDCR_SOC PHASES I and VII
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11	Reg - VDDCR_SOC PHASES IV and X
12	Reg - VDDCR_SOC PHASES II and VIII
13	Reg - VDDCR_SOC PHASES VI and XII
14	Reg - VDDCR_IO
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21	GPUTACH & BACO LEDs
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MICRO-STAR INT'L CO.,LTD

MS-V368

Size	Document Description	Rev
Custom	Vega10 - PCIe Interface	1.1

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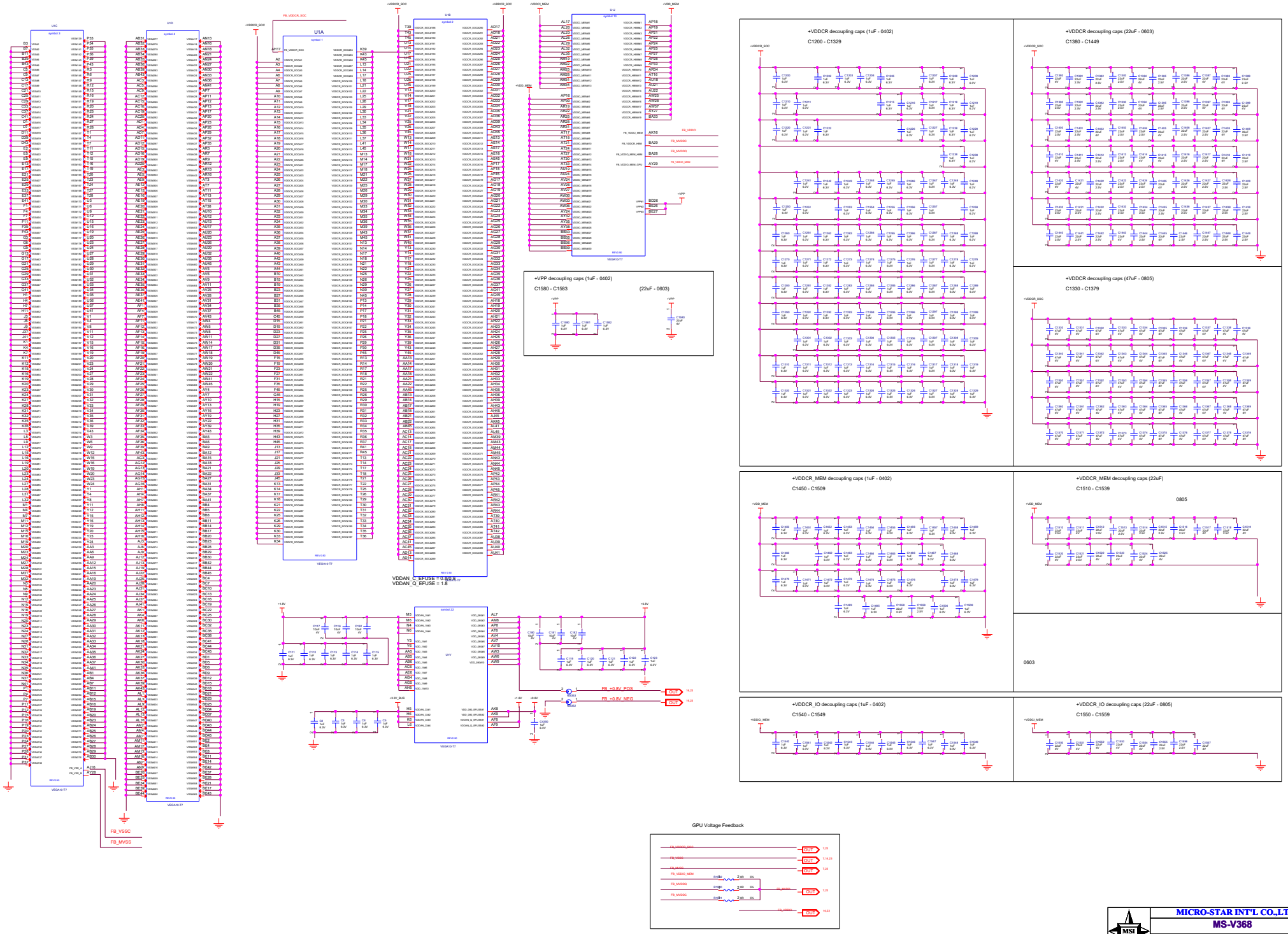
+VDDCR decoupling caps (1uF - 0402)
C1200 - C1329
+VDDCR decoupling caps (22uF - 0603)
C1380 - C1449
+VDDCR decoupling caps (47uF - 0805)
C1330 - C1379
+VPP decoupling caps (1uF - 0402)
C1580 - C1583
(22uF - 0603)
+VDDCR_MEM decoupling caps (1uF - 0402)
C1450 - C1509
+VDDCR_MEM decoupling caps (22uF)
C1510 - C1539
0805
0603
+VDDCR_IO decoupling caps (1uF - 0402)
C1540 - C1549
+VDDCR_IO decoupling caps (22uF - 0805)
C1550 - C1559
GPU Voltage Feedback
VDDAN_C_EFUSE = 0.9-1.8
VDDAN_Q_EFUSE = 1.8
FB_VSSC
FB_MVSS
FB_+0.8V_POS
FB_+0.8V_NEG
MICRO-STAR INT'L CO.,LTD
MS-V368
Size Custom
Document Description
Vega10 - Power / GND
Rev 1.1
Date: 2017-08-15
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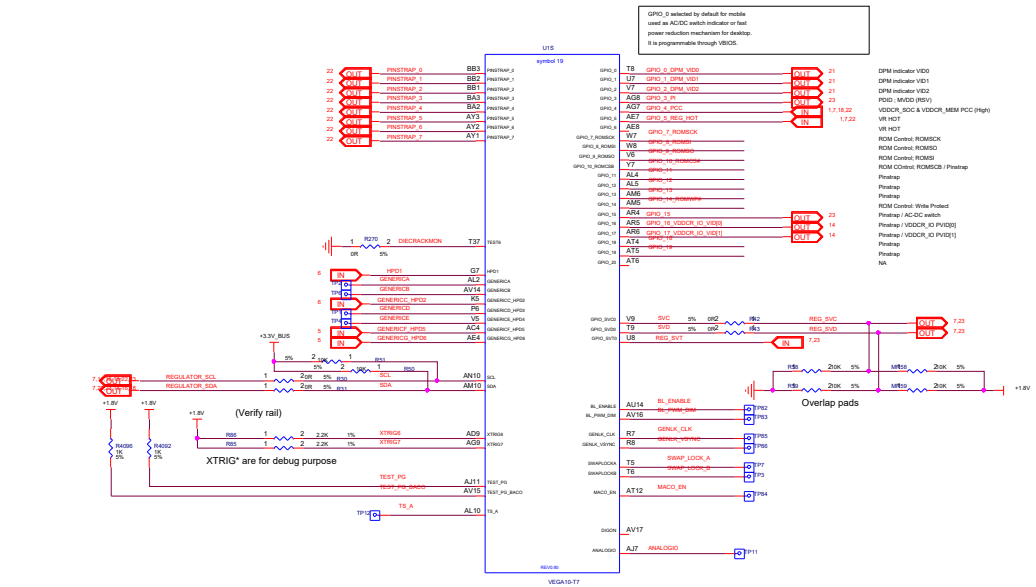

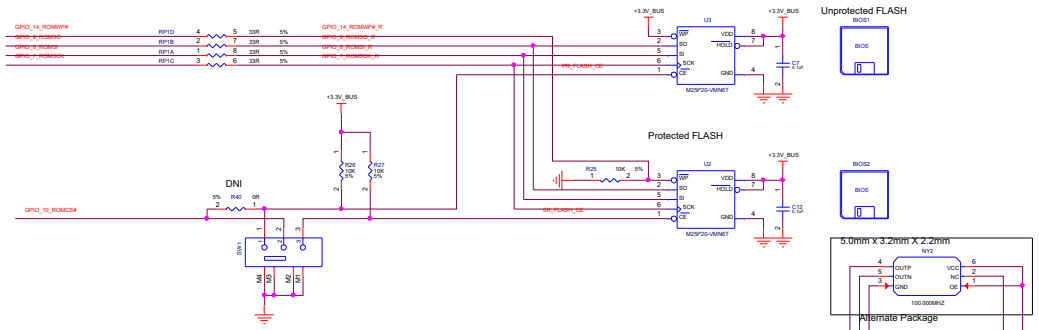

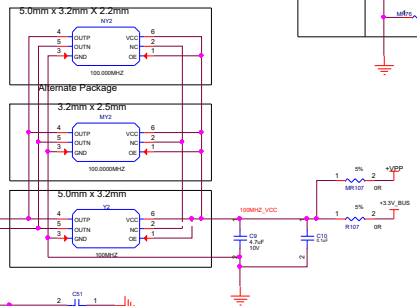

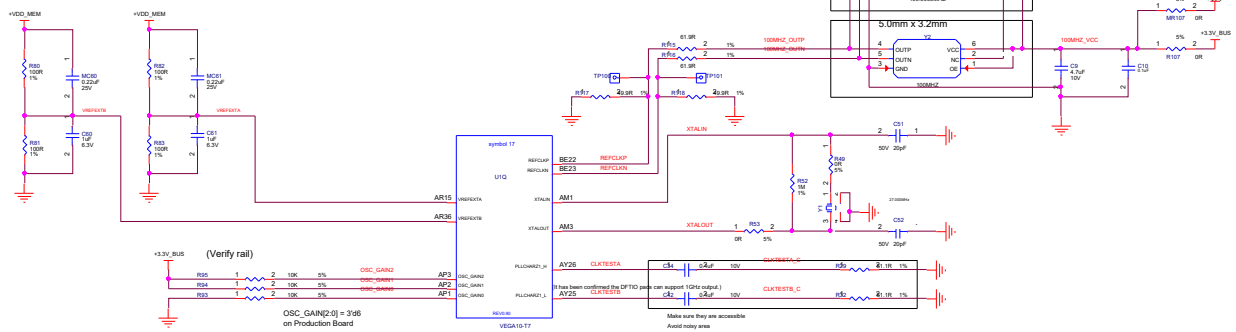

Note: Internal PU/PD at GPIO pad is strength in 14nm design spec

User		Internal Default Value	Definition
BIF	MR50 2.0K 5% / R1 2.0K 5% PINSTRAP_6	0	STRAP_BIF_GEN3_DIS_A 0: PCIe GEN 3 supported 1: PCIe GEN 3 not supported
	MR51 2.0K 5% / R51 2.0K 5% PINSTRAP_7	0	PINSTRAP_BIF_CLK_PM_EN 0: CLKREQ# power management capability is disabled 1: CLKREQ# power management capability is enabled
	MR52 2.0K 5% / R52 2.0K 5% GPIO_13	0	PINSTRAP_BIF_LC_TX_SWING
	MR53 2.0K 5% / R53 2.0K 5% GPIO_15	0	PINSTRAP_BIF_VGA_DIS 0: VGA controller capacity enabled 1: The device won't be recognised as the system's VGA controller
DCE	MR54 2.0K 5% / R54 2.0K 5% PINSTRAP_5	0	PINSTRAP_AUD_PORT_CONN[2:0] Number of audio-capable display outputs 0: All endpoints connected 1: 6 endpoints connected 2: 5 endpoints connected 3: 4 endpoints connected 4: 3 endpoints connected 5: 2 endpoints connected 6: 1 endpoint connected 7: 0 endpoints connected
	MR55 2.0K 5% / R55 2.0K 5% PINSTRAP_4	0	
	MR56 2.0K 5% / R56 2.0K 5% PINSTRAP_3	0	
	MR57 2.0K 5% / R57 2.0K 5% GPIO_12	0	PINSTRAP_AUD[1:0] 1: Audio for DisplayPort only 2: Audio for DisplayPort and HDMI if dongle is detected 3: Audio for DisplayPort and native HDMI
	MR58 2.0K 5% / R58 2.0K 5% GPIO_11	0	
Platform	MR69 2.0K 5% / R69 2.0K 5% GPIO_18	0	PINSTRAP_BOARD_CONFIG[2:0]
	MR70 2.0K 5% / R70 2.0K 5% GPIO_17_VDDCR_IO_VID[1]	0	TBD
	MR71 2.0K 5% / R71 2.0K 5% GPIO_16_VDDCR_IO_VID[0]	0	
SMU	MR72 2.0K 5% / R72 2.0K 5% PINSTRAP_2	1	PINSTRAP_ROM_CONFIG[2:0] 100 - 512KBIT (ST) M25P05A 101 - 1MBIT (ST) (M25P10A) 101 - 2MBIT (ST) M25P20 101 - 4MBIT (ST) M25P40 101 - 8MBIT (ST) M25P80 100 - 512KBIT (CHINGIS) PM25LV512 101 - 1MBIT (CHINGIS) PM25LV010
	MR73 2.0K 5% / R73 2.0K 5% PINSTRAP_1	0	
	MR74 2.0K 5% / R74 2.0K 5% PINSTRAP_0	1	
	MR75 2.0K 5% / R75 2.0K 5% GPIO_19	0	PINSTRAP_SMBUS_ADDR 0: 0x41h 1: 0x40h
	MR76 2.0K 5% / R76 2.0K 5% GPIO_10_ROMCS#	1	PINSTRAP_BIOS_ROM_EN 0: Disable the external BIOS ROM device 1: Enable the external BIOS ROM device

//gpuE/doc/design/chip/padring/AI_dGPU/PinStrap_Plan.pptx

18ci203

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V368	
Size Custom	Document Description: Vega10 - GPIO, EXTRA	Rev 1.1
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DFTIO

U1E

symbol 5

J7	DFTIO_0	DFTIO_96	C18
L11	DFTIO_1	DFTIO_97	B16
E4	DFTIO_2	DFTIO_98	G20
L8	DFTIO_3	DFTIO_99	J20
M10	DFTIO_4	DFTIO_100	J19
E3	DFTIO_5	DFTIO_101	D17
M9	DFTIO_6	DFTIO_102	C19
L7	DFTIO_7	DFTIO_103	F18
N8	DFTIO_8	DFTIO_104	C20
C2	DFTIO_9	DFTIO_105	D18
N10	DFTIO_10	DFTIO_106	E22
M8	DFTIO_11	DFTIO_107	B17
E6	DFTIO_12	DFTIO_108	D20
D4	DFTIO_13	DFTIO_109	B18
K9	DFTIO_14	DFTIO_110	D21
P9	DFTIO_15	DFTIO_111	E19
E7	DFTIO_16	DFTIO_112	B20
C1	DFTIO_17	DFTIO_113	H26
D2	DFTIO_18	DFTIO_114	G23
K10	DFTIO_19	DFTIO_115	C22
H8	DFTIO_20	DFTIO_116	D22
C3	DFTIO_21	DFTIO_117	E20
C4	DFTIO_22	DFTIO_118	C26
K8	DFTIO_23	DFTIO_119	C23
L10	DFTIO_24	DFTIO_120	B21
F8	DFTIO_25	DFTIO_121	B22
J8	DFTIO_26	DFTIO_122	F22
D3	DFTIO_27	DFTIO_123	G26
G8	DFTIO_28	DFTIO_124	J26
B2	DFTIO_29	DFTIO_125	J22
H10	DFTIO_30	DFTIO_126	E23
B5	DFTIO_31	DFTIO_127	F20
C6	DFTIO_32	DFTIO_128	D24
D5	DFTIO_33	DFTIO_129	C24
E8	DFTIO_34	DFTIO_130	G28
J10	DFTIO_35	DFTIO_131	C27
D8	DFTIO_36	DFTIO_132	D25
J11	DFTIO_37	DFTIO_133	C31
F10	DFTIO_38	DFTIO_134	F25
D6	DFTIO_39	DFTIO_135	B24
J14	DFTIO_40	DFTIO_136	B25
J12	DFTIO_41	DFTIO_137	D28
G10	DFTIO_42	DFTIO_138	F21
H9	DFTIO_43	DFTIO_139	C28
B4	DFTIO_44	DFTIO_140	J27
G12	DFTIO_45	DFTIO_141	E24
F12	DFTIO_46	DFTIO_142	D29
D9	DFTIO_47	DFTIO_143	B26
B6	DFTIO_48	DFTIO_144	G27
C7	DFTIO_49	DFTIO_145	F24
F13	DFTIO_50	DFTIO_146	D26
J16	DFTIO_51	DFTIO_147	C32
C8	DFTIO_52	DFTIO_148	E30
F9	DFTIO_53	DFTIO_149	D36
J15	DFTIO_54	DFTIO_150	J23
E12	DFTIO_55	DFTIO_151	C34
E11	DFTIO_56	DFTIO_152	B28
G11	DFTIO_57	DFTIO_153	C30
B8	DFTIO_58	DFTIO_154	D30
H12	DFTIO_59	DFTIO_155	H24
H16	DFTIO_60	DFTIO_156	G31
F14	DFTIO_61	DFTIO_157	E28
E14	DFTIO_62	DFTIO_158	B29
G14	DFTIO_63	DFTIO_159	F26
E10	DFTIO_64	DFTIO_160	J24
D13	DFTIO_65	DFTIO_161	B30
H20	DFTIO_66	DFTIO_162	D32
H18	DFTIO_67	DFTIO_163	E31
B9	DFTIO_68	DFTIO_164	D38
H13	DFTIO_69	DFTIO_165	B32
D10	DFTIO_70	DFTIO_166	B33
H17	DFTIO_71	DFTIO_167	C35
H21	DFTIO_72	DFTIO_168	F28
H14	DFTIO_73	DFTIO_169	C38
C14	DFTIO_74	DFTIO_170	H25
C10	DFTIO_75	DFTIO_171	G30
G18	DFTIO_76	DFTIO_172	D40
D14	DFTIO_77	DFTIO_173	E32
H22	DFTIO_78	DFTIO_174	B34
E15	DFTIO_79	DFTIO_175	C36
G16	DFTIO_80	DFTIO_176	E26
G22	DFTIO_81	DFTIO_177	E27
C15	DFTIO_82	DFTIO_178	H28
G15	DFTIO_83	DFTIO_179	D33
E16	DFTIO_84	DFTIO_180	D42
C16	DFTIO_85	DFTIO_181	D37
B13	DFTIO_86	DFTIO_182	C43
C11	DFTIO_87	DFTIO_183	F29
G19	DFTIO_88	DFTIO_184	J28
F16	DFTIO_89	DFTIO_185	F32
J18	DFTIO_90	DFTIO_186	D44
B14	DFTIO_91	DFTIO_187	B44
D16	DFTIO_92	DFTIO_188	E44
G24	DFTIO_93	DFTIO_189	C44
E18	DFTIO_94	DFTIO_190	D34
F17	DFTIO_95	DFTIO_191	H29

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U1F

symbol 6

D41	DFTIO_192	DFTIO_288	P41
J35	DFTIO_193	DFTIO_289	L39
E42	DFTIO_194	DFTIO_290	H32
F42	DFTIO_195	DFTIO_291	W38
F30	DFTIO_196	DFTIO_292	W39
J30	DFTIO_197	DFTIO_293	W40
H30	DFTIO_198	DFTIO_294	Y38
E43	DFTIO_199	DFTIO_295	P37
F40	DFTIO_200	DFTIO_296	U44
B40	DFTIO_201	DFTIO_297	W44
B41	DFTIO_202	DFTIO_298	U43
B38	DFTIO_203	DFTIO_299	V40
C42	DFTIO_204	DFTIO_300	N39
G44	DFTIO_205	DFTIO_301	P40
F34	DFTIO_206	DFTIO_302	Y44
H37	DFTIO_207	DFTIO_303	T40
E34	DFTIO_208	DFTIO_304	W42
B42	DFTIO_209	DFTIO_305	Y42
B36	DFTIO_210	DFTIO_306	W43
B37	DFTIO_211	DFTIO_307	AA44
G32	DFTIO_212	DFTIO_308	U40
J31	DFTIO_213	DFTIO_309	R40
E35	DFTIO_214	DFTIO_310	M38
F44	DFTIO_215	DFTIO_311	AB44
E39	DFTIO_216	DFTIO_312	AA42
C40	DFTIO_217	DFTIO_313	AA43
H36	DFTIO_218	DFTIO_314	AB41
E38	DFTIO_219	DFTIO_315	R38
F33	DFTIO_220	DFTIO_316	Y40
E36	DFTIO_221	DFTIO_317	AB40
C39	DFTIO_222	DFTIO_318	AA39
G42	DFTIO_223	DFTIO_319	AC40
G43	DFTIO_224	DFTIO_320	N38
H44	DFTIO_225	DFTIO_321	AA40
H42	DFTIO_226	DFTIO_322	T38
G36	DFTIO_227	DFTIO_323	Y41
E40	DFTIO_228	DFTIO_324	P38
F41	DFTIO_229	DFTIO_325	AB42
J43	DFTIO_230	DFTIO_326	AC39
J44	DFTIO_231	DFTIO_327	AD41
J32	DFTIO_232	DFTIO_328	AC44
K44	DFTIO_233	DFTIO_329	AA38
G35	DFTIO_234	DFTIO_330	AC43
F38	DFTIO_235	DFTIO_331	AD42
M44	DFTIO_236	DFTIO_332	AB37
L44	DFTIO_237	DFTIO_333	AC42
H34	DFTIO_238	DFTIO_334	AC38
K41	DFTIO_239	DFTIO_335	AB38
L43	DFTIO_240	DFTIO_336	AM40
K42	DFTIO_241	DFTIO_337	AM42
J42	DFTIO_242	DFTIO_338	AT45
F37	DFTIO_243	DFTIO_339	AN42
G40	DFTIO_244	DFTIO_340	AT44
G39	DFTIO_245	DFTIO_341	AR45
K40	DFTIO_246	DFTIO_342	AJ40
J34	DFTIO_247	DFTIO_343	AY45
L42	DFTIO_248	DFTIO_344	AV40
H41	DFTIO_249	DFTIO_345	AW43
N43	DFTIO_250	DFTIO_346	AY42
N44	DFTIO_251	DFTIO_347	AW42
G34	DFTIO_252	DFTIO_348	BA43
M42	DFTIO_253	DFTIO_349	AW44
F36	DFTIO_254	DFTIO_350	BA44
J36	DFTIO_255	DFTIO_351	AY41
J39	DFTIO_256	DFTIO_352	AW40
G38	DFTIO_257	DFTIO_353	AY44
P44	DFTIO_258	DFTIO_354	BA40
J40	DFTIO_259	DFTIO_355	AT43
N42	DFTIO_260	DFTIO_356	AV44
M41	DFTIO_261	DFTIO_357	AU42
R43	DFTIO_262	DFTIO_358	AU43
R44	DFTIO_263	DFTIO_359	AY40
J38	DFTIO_264	DFTIO_360	AK42
K37	DFTIO_265	DFTIO_361	BA42
V44	DFTIO_266	DFTIO_362	AK44
P42	DFTIO_267	DFTIO_363	AN39
T42	DFTIO_268	DFTIO_364	AR39
H38	DFTIO_269	DFTIO_365	AR40
R39	DFTIO_270	DFTIO_366	AV41
U42	DFTIO_271	DFTIO_367	AV42
H40	DFTIO_272	DFTIO_368	AN40
V41	DFTIO_273	DFTIO_369	AL42
V42	DFTIO_274	DFTIO_370	AH37
M37	DFTIO_275	DFTIO_371	AL40
L40	DFTIO_276	DFTIO_372	AM41
T41	DFTIO_277	DFTIO_373	AL43
U38	DFTIO_278	DFTIO_374	AP40
U39	DFTIO_279	DFTIO_375	AP41
L38	DFTIO_280	DFTIO_376	AU44
H33	DFTIO_281	DFTIO_377	AK41
M40	DFTIO_282	DFTIO_378	AJ39
V38	DFTIO_283	DFTIO_379	AP39
R42	DFTIO_284	DFTIO_380	AL44
T44	DFTIO_285	DFTIO_381	AJ43
K38	DFTIO_286	DFTIO_382	AL39
N40	DFTIO_287	DFTIO_383	AJ38

REV0.90

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FREE

U1H

symbol 8

B1	RSVD81	RSVD813	AU27
B12	RSVD82	RSVD814	AV1
C12	RSVD83	RSVD815	AV2
D12	RSVD84	RSVD816	AV3
L4	RSVD85	RSVD817	AV8
N7	RSVD86	RSVD818	AV12
N11	RSVD87	RSVD819	AV13
P8	RSVD88	RSVD820	AV18
P10	RSVD89	RSVD821	AV19
R10	RSVD810	RSVD822	AV20
R11	RSVD811	RSVD823	AV21
T10	RSVD812	RSVD824	AV22
U4	RSVD813	RSVD825	AV23
U5	RSVD814	RSVD826	AV36
U10	RSVD815	RSVD827	AV38
U11	RSVD816	RSVD828	AV39
W10	RSVD817	RSVD829	AV45
W11	RSVD818	RSVD830	AW1
Y9	RSVD819	RSVD831	AW2
AA4	RSVD820	RSVD832	AW7
AA7	RSVD821	RSVD833	AW10
AA10	RSVD822	RSVD834	AW12
AA11	RSVD823	RSVD835	AW13
AB10	RSVD824	RSVD836	AW15
AC10	RSVD825	RSVD837	AW16
AC11	RSVD826	RSVD838	AW23
AD10	RSVD827	RSVD839	AW24
AD37	RSVD828	RSVD840	AW26
AD38	RSVD829	RSVD841	AW27
AD40	RSVD830	RSVD842	AW29
AD44	RSVD831	RSVD843	AW38
AE11	RSVD832	RSVD844	AW39
AE38	RSVD833	RSVD845	AY23
AE39	RSVD834	RSVD846	AY30
AE40	RSVD835	RSVD847	AY31
AE42	RSVD836	RSVD848	AY33
AE43	RSVD837	RSVD849	AY34
AE44	RSVD838	RSVD850	AY36
AF10	RSVD839	RSVD851	AY37
AF37	RSVD840	RSVD852	BA4
AF38	RSVD841	RSVD853	BA23
AF40	RSVD842	RSVD854	BA24
AF41	RSVD843	RSVD855	BA25
AF42	RSVD844	RSVD856	BA26
AF44	RSVD845	RSVD857	BA30
AG38	RSVD846	RSVD858	BA32
AG39	RSVD847	RSVD859	BA35
AG40	RSVD848	RSVD860	BA36
AG42	RSVD849	RSVD861	BA38
AG43	RSVD850	RSVD862	BA39
AG44	RSVD851	RSVD863	BB24
AH38	RSVD852	RSVD864	BB25
AH40	RSVD853	RSVD865	BB26
AH41	RSVD854	RSVD866	BB27
AH42	RSVD855	RSVD867	BB31
AH44	RSVD856	RSVD868	BB32
AJ4	RSVD857	RSVD869	BB37
AJ5	RSVD858	RSVD870	BB38
AJ8	RSVD859	RSVD871	BB40
AJ10	RSVD860	RSVD872	BB41
AJ14	RSVD861	RSVD873	BB43
AJ42	RSVD862	RSVD874	BC3
AJ44	RSVD863	RSVD875	BC23
AK7	RSVD864	RSVD876	BC24
AK10	RSVD865	RSVD877	BC26
AK38	RSVD866	RSVD878	BC27
AK40	RSVD867	RSVD879	BC28
AL6	RSVD868	RSVD880	BC31
AL8	RSVD869	RSVD881	BC33
AL11	RSVD870	RSVD882	BC36
AL15	RSVD871	RSVD883	BC37
AL38	RSVD872	RSVD884	BC39
AM14	RSVD873	RSVD885	BC40
AM37	RSVD874	RSVD886	BD4
AM38	RSVD875	RSVD887	BD22
AN1	RSVD876	RSVD888	BD24
AN2	RSVD877	RSVD889	BD27
AN3	RSVD878	RSVD890	BD28
AN4	RSVD879	RSVD891	BD32
AN5	RSVD880	RSVD892	BD35
AN6	RSVD881	RSVD893	BD36
AN8	RSVD882	RSVD894	BD38
AN11	RSVD883	RSVD895	BD39
AN12	RSVD884	RSVD896	BD41
AN14	RSVD885	RSVD897	BD42
AN38	RSVD886	RSVD898	BE24
AP4	RSVD887	RSVD899	BE32
AP5	RSVD888	RSVD9000	BE35
AP6	RSVD889	RSVD9001	BE36
AP9	RSVD890	RSVD9002	BE38
AP10	RSVD891	RSVD9003	BE40
AP38	RSVD892		
AR6	RSVD893		
AR10	RSVD894		
AR11	RSVD895		
AR37	RSVD896		
AR38	RSVD897		
AT9	RSVD898		
AT10	RSVD899		
AT36	RSVD9100		
AU1	RSVD9101		
AU2	RSVD9102		
AU3	RSVD9103		
AU4	RSVD9104		
AU5	RSVD9105		
AU6	RSVD9106		
AU7	RSVD9107		
AU8	RSVD9108		
AU9	RSVD9109		
AU11	RSVD9110		
AU15	RSVD9111		
AU25	RSVD9112		

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HBM_DAP

U1G

symbol 7

AJ27	HBM8_DAP_0	HBM8_DAP_0	AL37
AK26	HBM8_DAP_1	HBM8_DAP_1	AJ36
AR27	HBM8_DAP_2	HBM8_DAP_2	AP36
AM27	HBM8_DAP_3	HBM8_DAP_3	AM36
AM26	HBM8_DAP_4	HBM8_DAP_4	AW35
AL27	HBM8_DAP_5	HBM8_DAP_5	AP37
AJ26	HBM8_DAP_6	HBM8_DAP_6	AN35
AJ21	HBM8_DAP_7	HBM8_DAP_7	AL36
AJ24	HBM8_DAP_8	HBM8_DAP_8	AT35
AK25	HBM8_DAP_9	HBM8_DAP_9	AR35
AN26	HBM8_DAP_10	HBM8_DAP_10	AK35
AL22	HBM8_DAP_11	HBM8_DAP_11	AJ35
AJ20	HBM8_DAP_12	HBM8_DAP_12	AU34
AL21	HBM8_DAP_13	HBM8_DAP_13	AM35
AK22	HBM8_DAP_14	HBM8_DAP_14	AK34
AN22	HBM8_DAP_15	HBM8_DAP_15	AV35
AL25	HBM8_DAP_16	HBM8_DAP_16	AN34
AJ23	HBM8_DAP_17	HBM8_DAP_17	AL34
AN25	HBM8_DAP_18	HBM8_DAP_18	AT34
AK23	HBM8_DAP_19	HBM8_DAP_19	AV33
AL24	HBM8_DAP_20	HBM8_DAP_20	AW34
AK20	HBM8_DAP_21	HBM8_DAP_21	AL33
AM21	HBM8_DAP_22	HBM8_DAP_22	AP34
AK19	HBM8_DAP_23	HBM8_DAP_23	AM33
AT26	HBM8_DAP_24	HBM8_DAP_24	AJ33
AR26	HBM8_DAP_25	HBM8_DAP_25	AU33
AL18	HBM8_DAP_26	HBM8_DAP_26	AT32
AM20	HBM8_DAP_27	HBM8_DAP_27	AM32
AJ18	HBM8_DAP_28	HBM8_DAP_28	AR33
AM24	HBM8_DAP_29	HBM8_DAP_29	AW32
AR24	HBM8_DAP_30	HBM8_DAP_30	AJ32
AR20	HBM8_DAP_31	HBM8_DAP_31	AK32
AJ17	HBM8_DAP_32	HBM8_DAP_32	AR32
AT25	HBM8_DAP_33	HBM8_DAP_33	AN32
AN20	HBM8_DAP_34	HBM8_DAP_34	AV32
AM23	HBM8_DAP_35	HBM8_DAP_35	AW31
AR23	HBM8_DAP_36	HBM8_DAP_36	AU31
AT23	HBM8_DAP_37	HBM8_DAP_37	AP31
AK17	HBM8_DAP_38	HBM8_DAP_38	AN31
AM17	HBM8_DAP_39	HBM8_DAP_39	AL31
AM18	HBM8_DAP_40	HBM8_DAP_40	AV30
AL19	HBM8_DAP_41	HBM8_DAP_41	AJ30
AN23	HBM8_DAP_42	HBM8_DAP_42	AR30
AR17	HBM8_DAP_43	HBM8_DAP_43	AT31
AR21	HBM8_DAP_44	HBM8_DAP_44	AK31
AT22	HBM8_DAP_45	HBM8_DAP_45	AM30
AK15	HBM8_DAP_46	HBM8_DAP_46	AU30
AT20	HBM8_DAP_47	HBM8_DAP_47	AJ29
AT19	HBM8_DAP_48	HBM8_DAP_48	AM29
AJ15	HBM8_DAP_49	HBM8_DAP_49	AR29
AN19	HBM8_DAP_50	HBM8_DAP_50	AL30
AN17	HBM8_DAP_51	HBM8_DAP_51	AV29
AN15	HBM8_DAP_52	HBM8_DAP_52	AT29
AP14	HBM8_DAP_53	HBM8_DAP_53	AN29
AR18	HBM8_DAP_54	HBM8_DAP_54	AN28
AT14	HBM8_DAP_55	HBM8_DAP_55	AK29
AP15	HBM8_DAP_56	HBM8_DAP_56	AU28
AR14	HBM8_DAP_57	HBM8_DAP_57	AT28
AL14	HBM8_DAP_58	HBM8_DAP_58	AL28
AK14	HBM8_DAP_59	HBM8_DAP_59	AK28

REV0.90

VEGA10-T7

CRACKMON

U1T

symbol 20

AE10	INTCRACKMONDA
AU36	INTCRACKMONDB
V10	INTCRACKMONGLL
Y10	INTCRACKMONGLR
V37	INTCRACKMONGUL
Y37	INTCRACKMONGUR
BC43	INTCRACKMONP
BC42	INTCRACKMONPDG

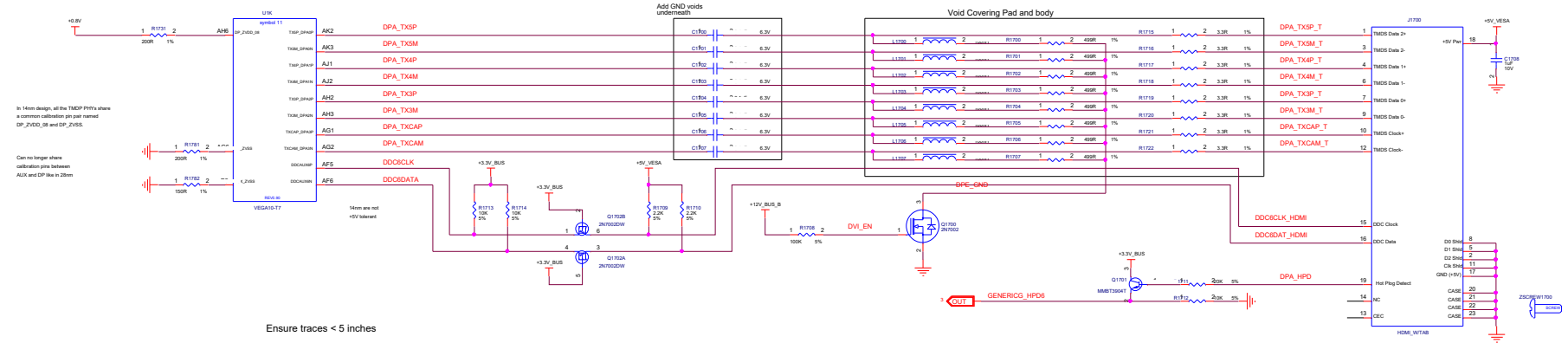
REV0.90

VEGA10-T7

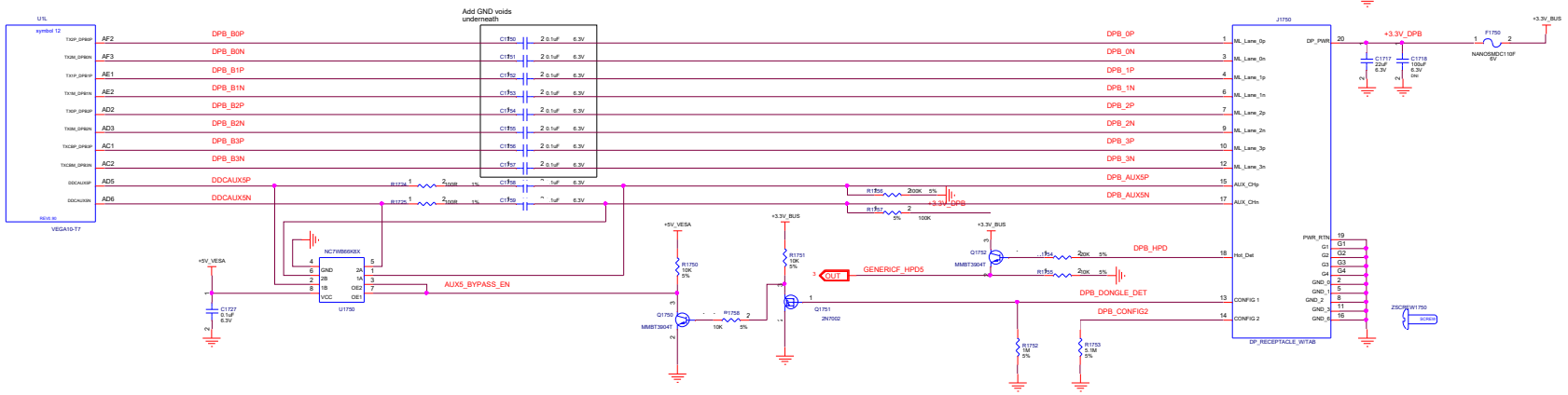
MSI	MICRO-STAR INT'L CO.,LTD		
	MS-V368		
Size Custom	Document Description: Vega10 - DFTIO, FREE, HPM_DAP, CRACKMON		Rev 1.1
Date: 2017-08-15	Sheet 4 of 25		

Ensure traces < 5 inches MAX (if routed on same layer)

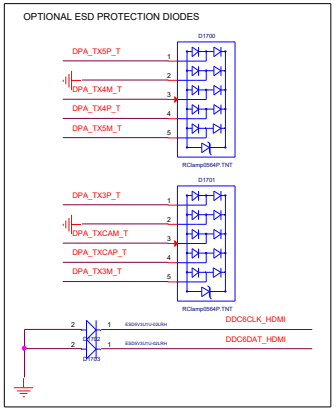
For differential routing on HDMI 2.0 connection, use dogbone shape antipads for the transitional vias of the same differential pair, and the distance from the via edge to the shape boundary should be



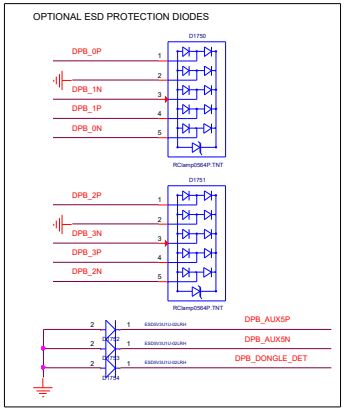
Ensure traces < 5 inches

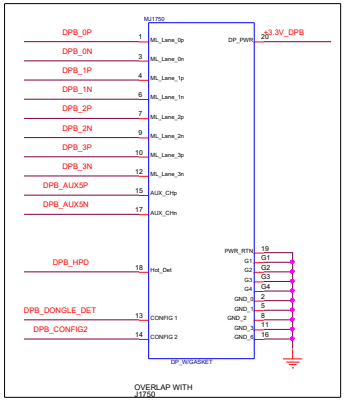


OPTIONAL ESD PROTECTION DIODES

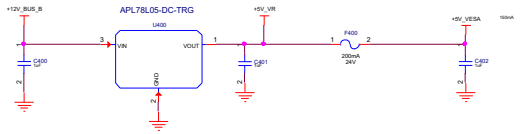


OPTIONAL ESD PROTECTION DIODES





Regulators for +5V and +5V_VESA



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MICRO-STAR INT'L CO.,LTD		
MS-V368		
Size Custom	Document Description: Vega10 - TMDPAB 1xDP, 1xHDMI & +5V VESA	Rev 1.1
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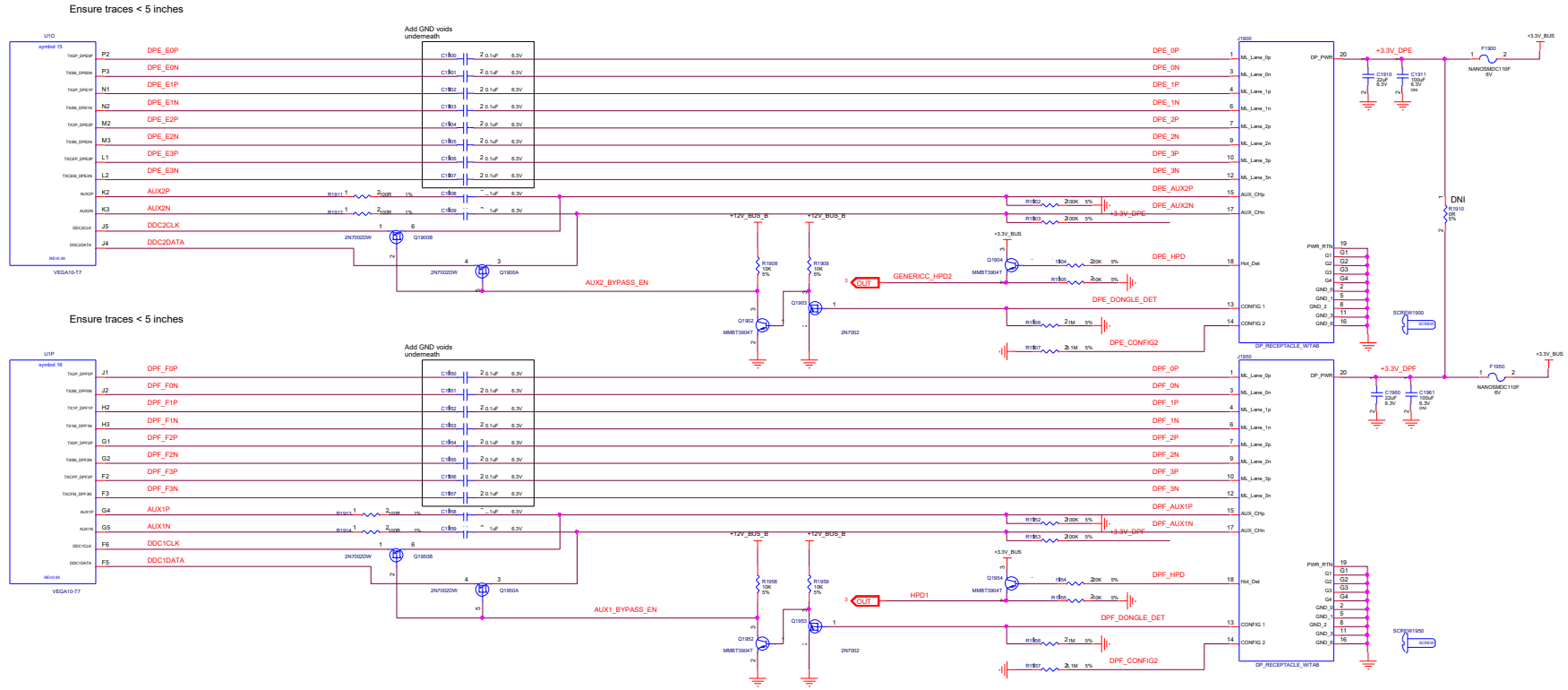

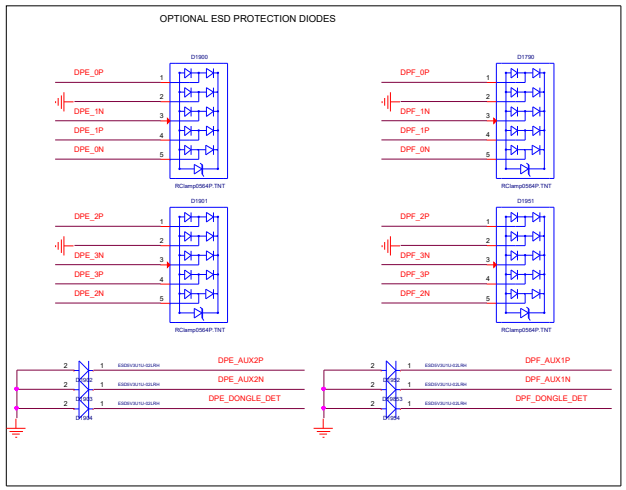

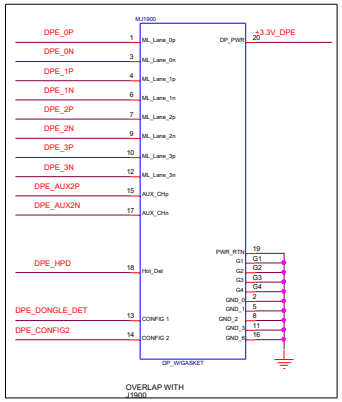

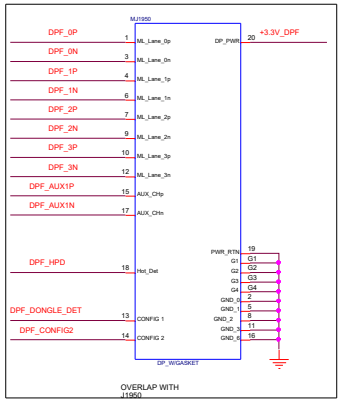

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V368	
Size Custom	Document Description Vega10 - TMDPEF 2xDP	Rev 1.1
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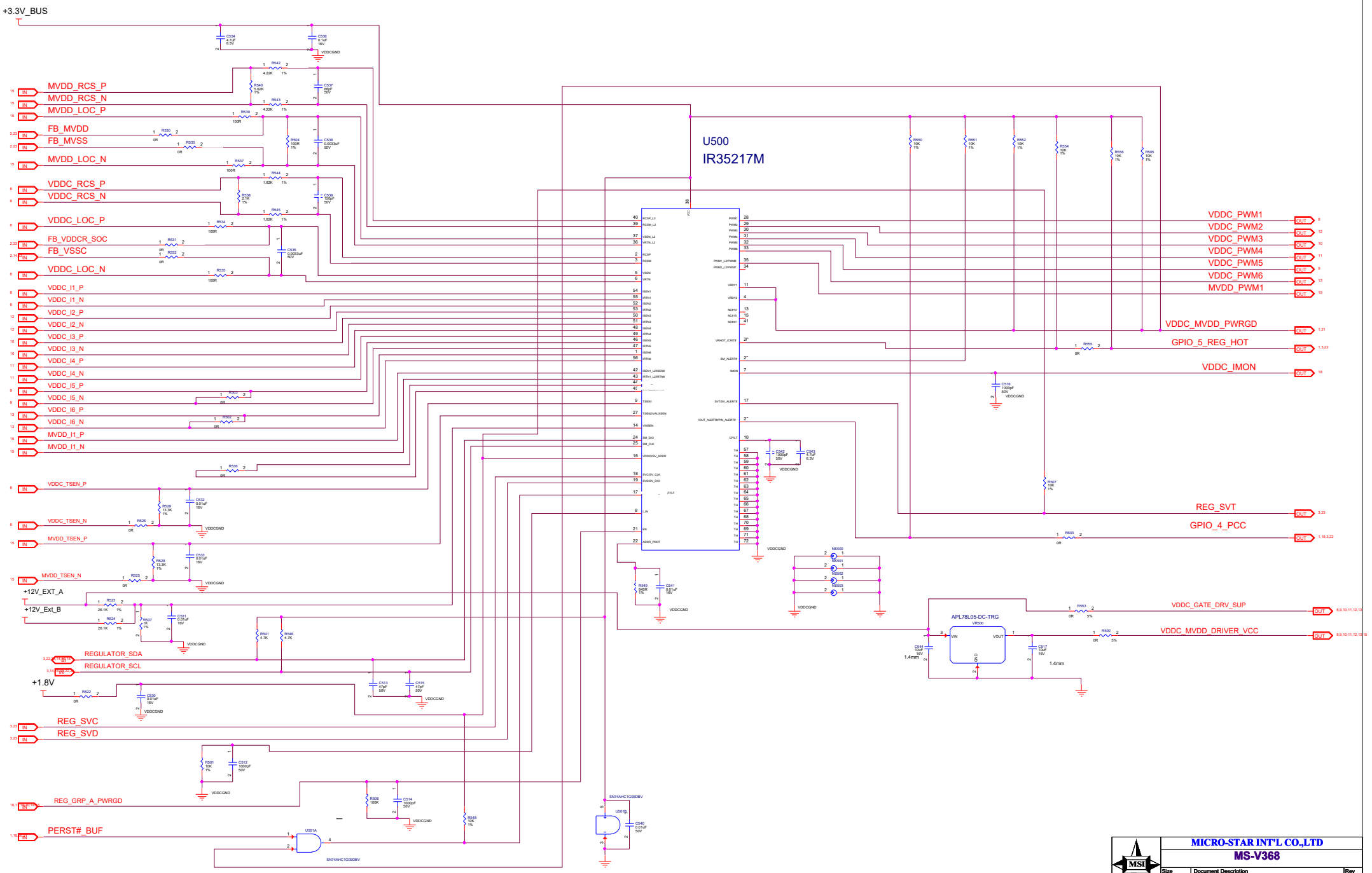
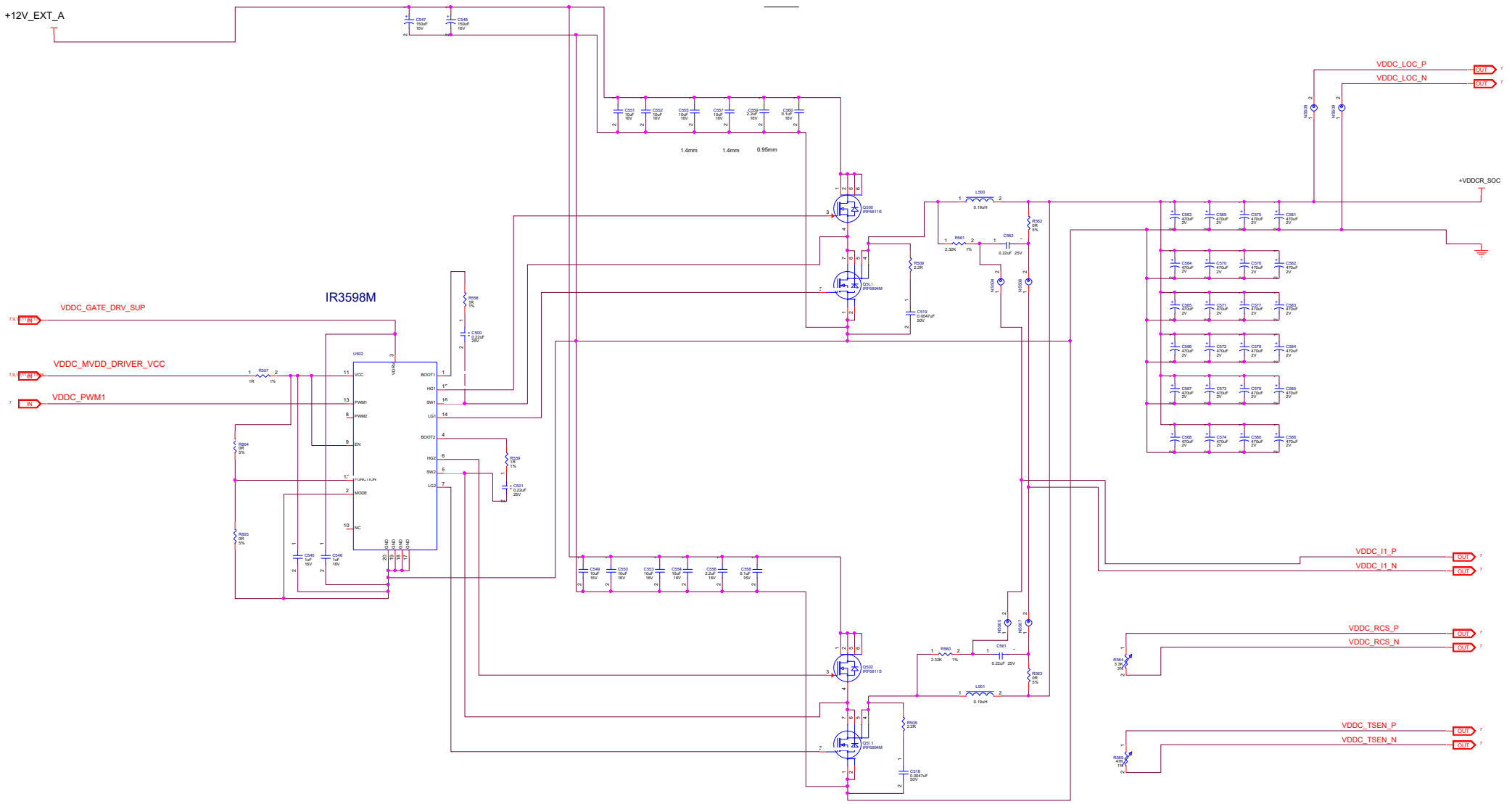
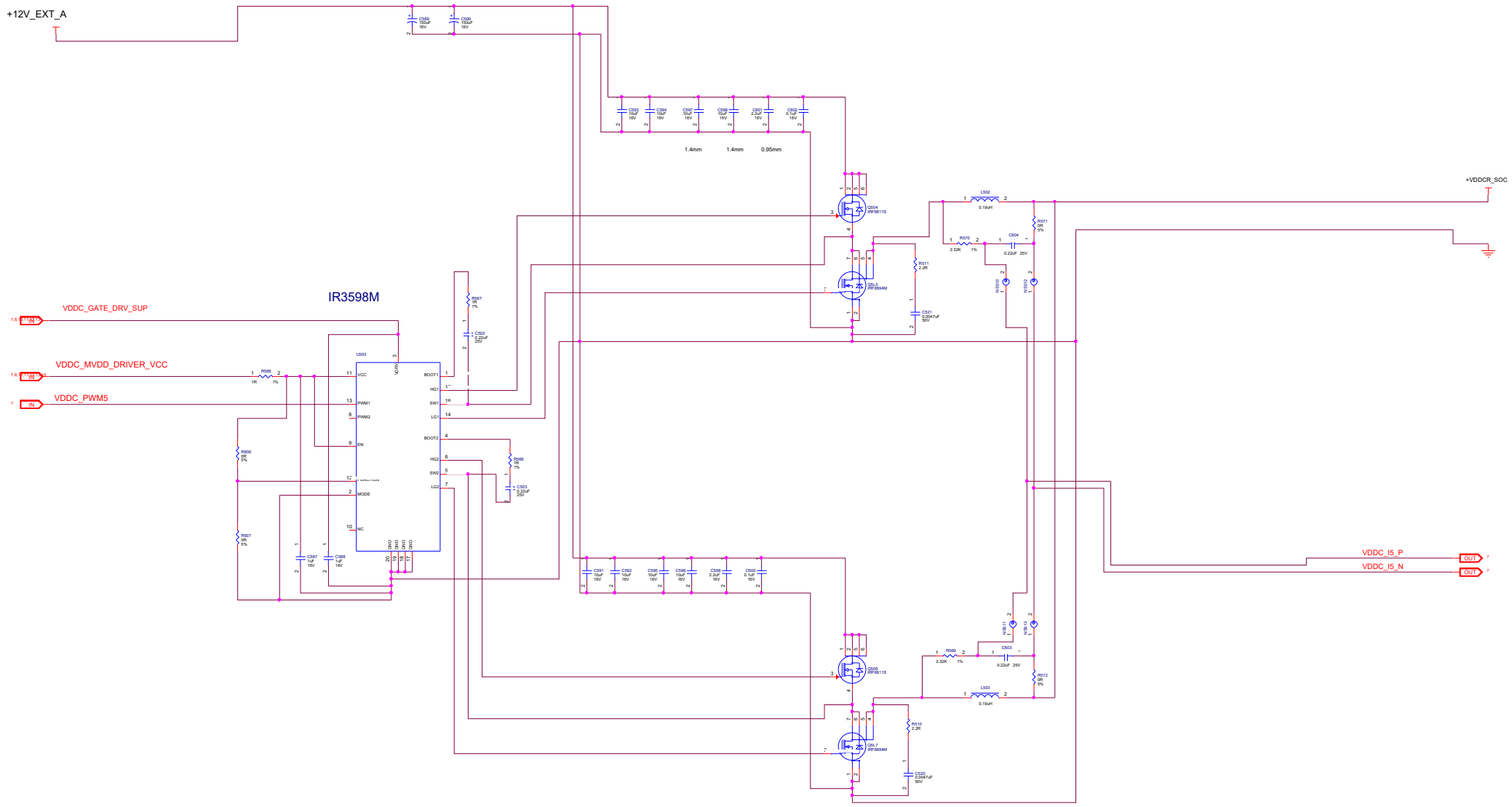


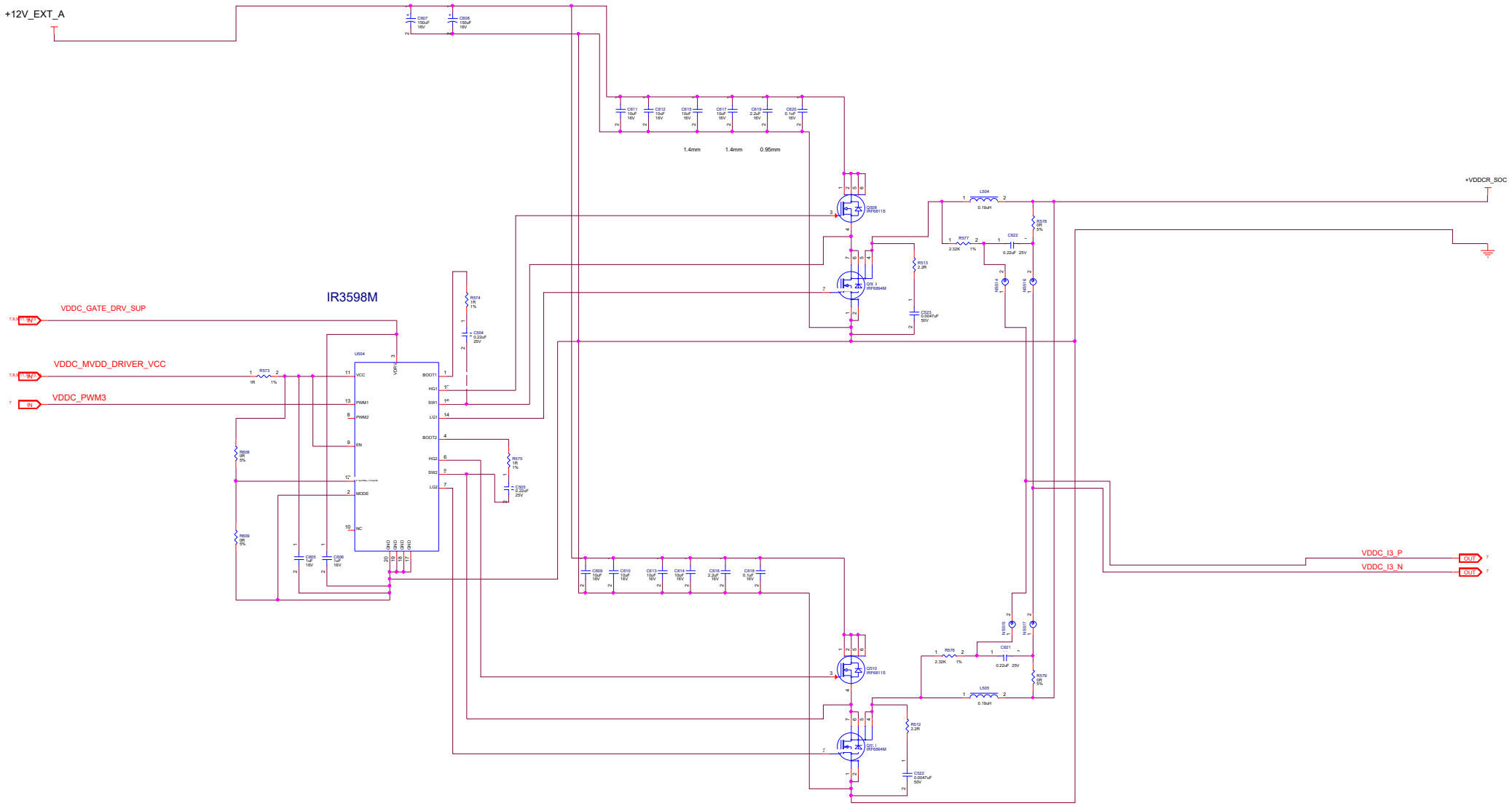
MICRO-STAR INT'L CO.,LTD	
MS-V368	
Size: Custom	Document Description: Control - VDDC / MVDD
Rev: 1.1	
Date: 2017-08-15	Sheet 7 of 25



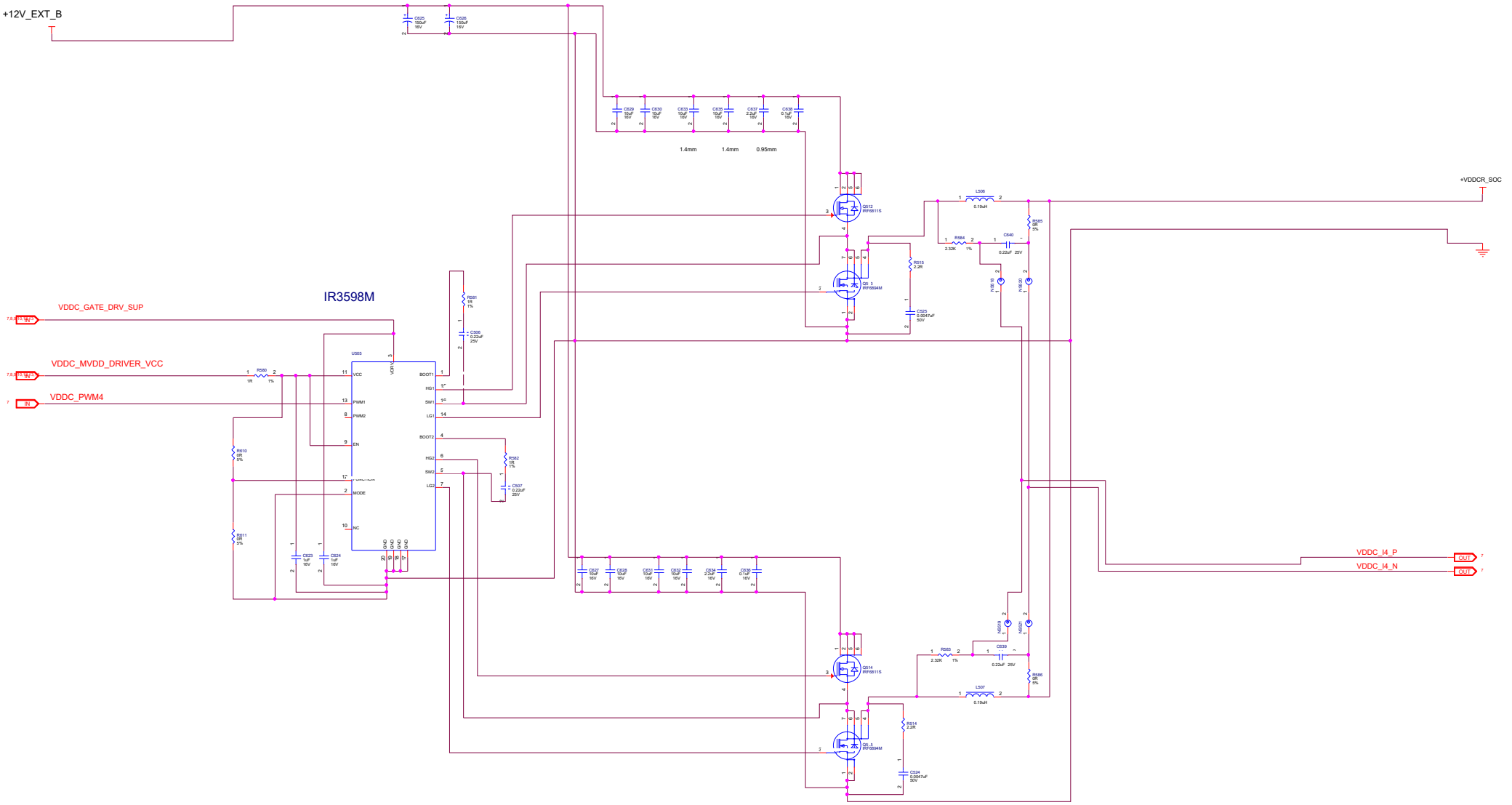
MICRO-STAR INT'L CO.,LTD		
MS-V368		
Size Custom	Document Description: Reg - VDDCR_SOC PHASES I and VII	Rev 1.1
Date: 2017-08-15	Sheet 8 of 25	



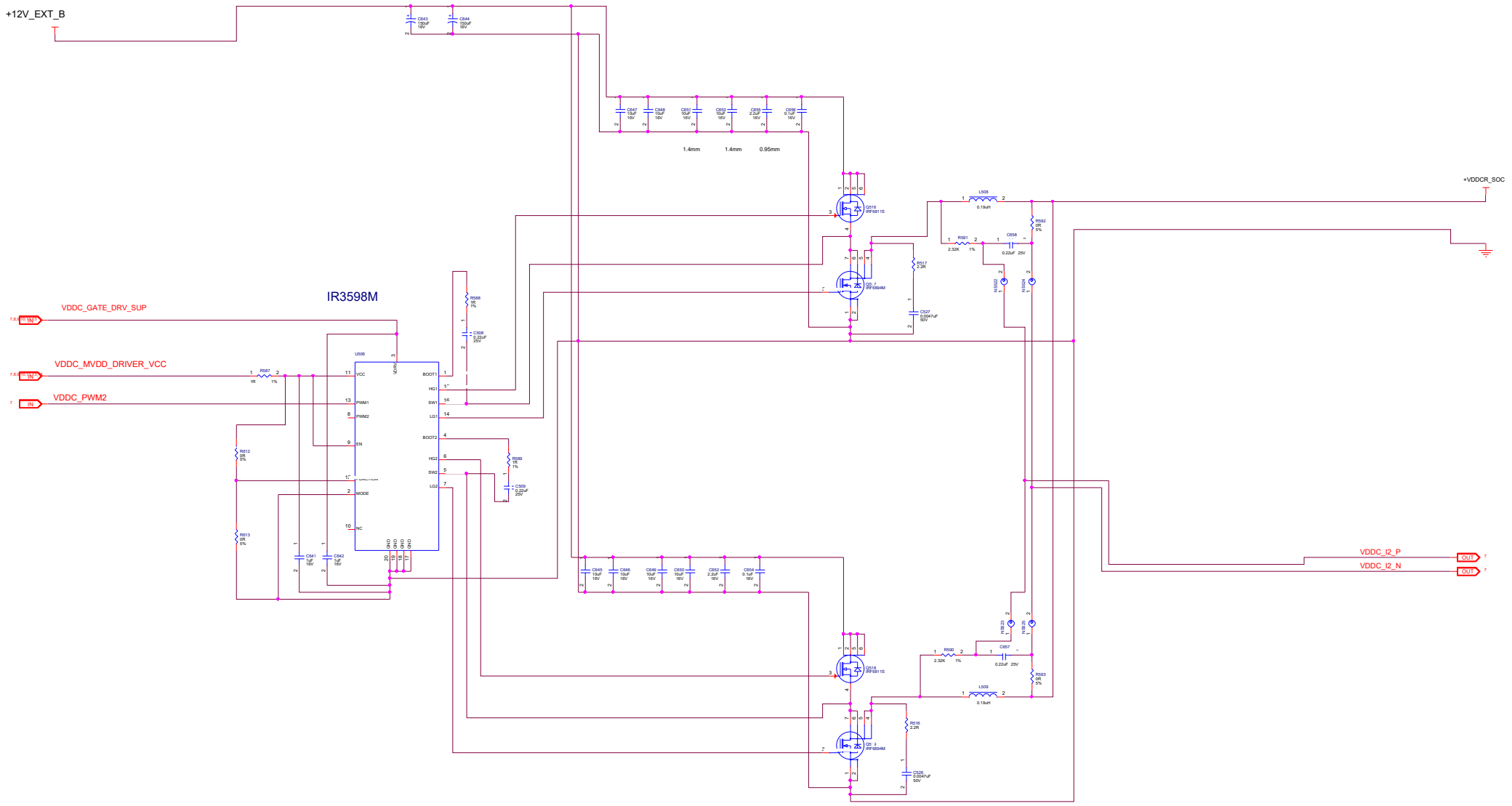
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V368	
Size Custom	Document Description: Reg - VDDCR_SOC PHASES V and XI	Rev 1.1
Date: 2017-08-15	Sheet 9 of 25	



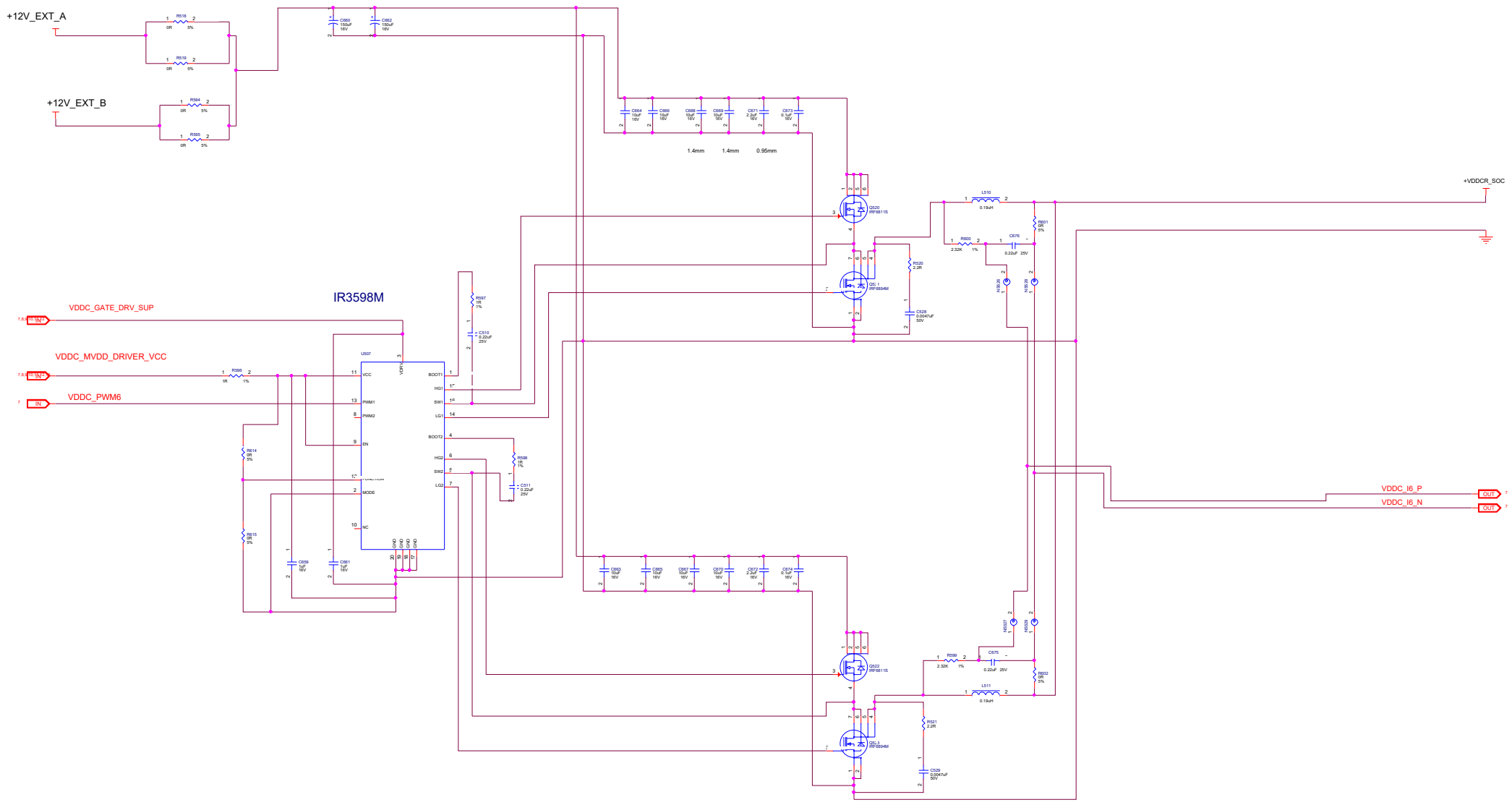
MICRO-STAR INT'L CO.,LTD		
MS-V368		
Size Custom	Document Description: Reg - VDDCR_SOC PHASES III and IX	Rev 1.1
Date: 2017-08-15	Sheet 10 of 25	



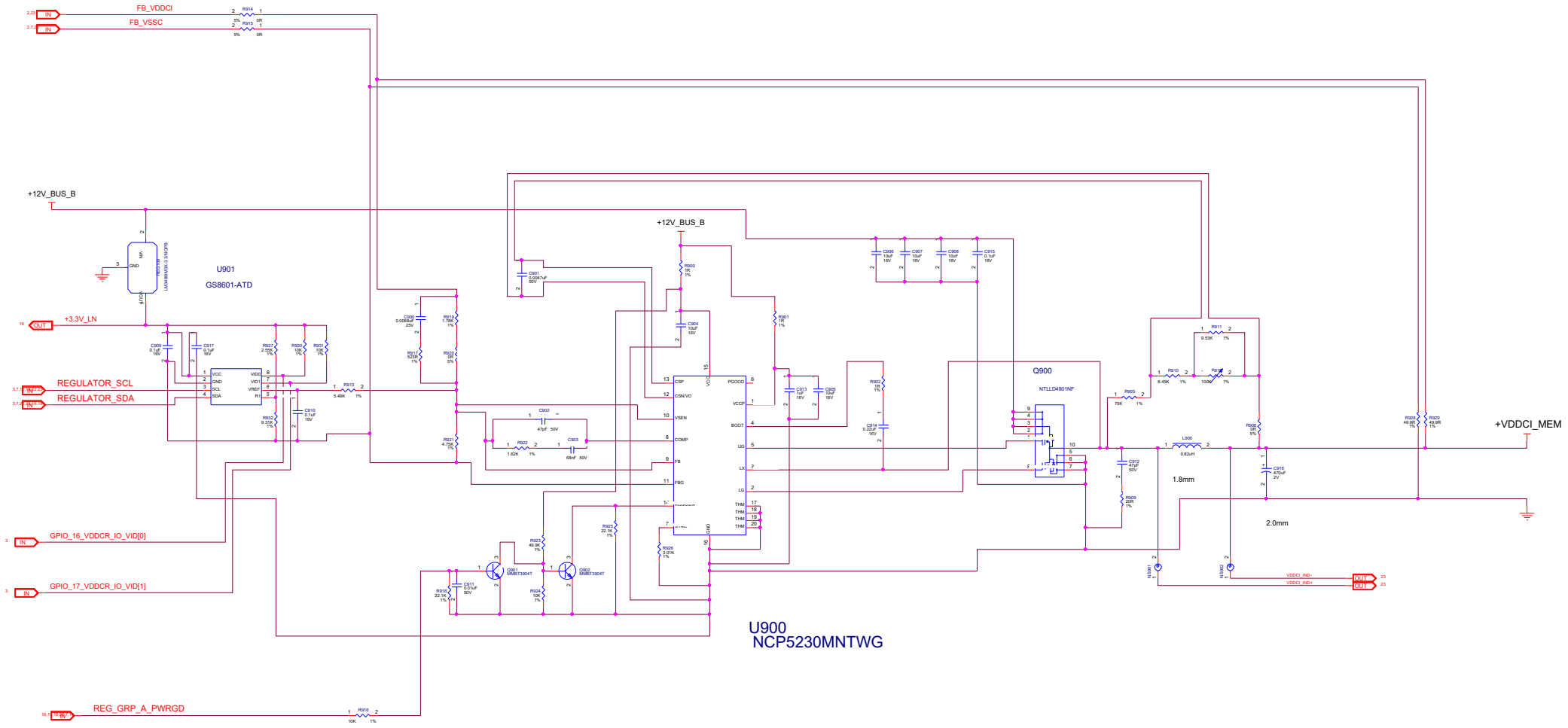
MICRO-STAR INT'L CO.,LTD		
MS-V368		
Size Custom	Document Description: Reg - VDDCR_SOC PHASES IV and X	Rev 1.1
Date: 2017-08-15	Sheet 11 of 25	



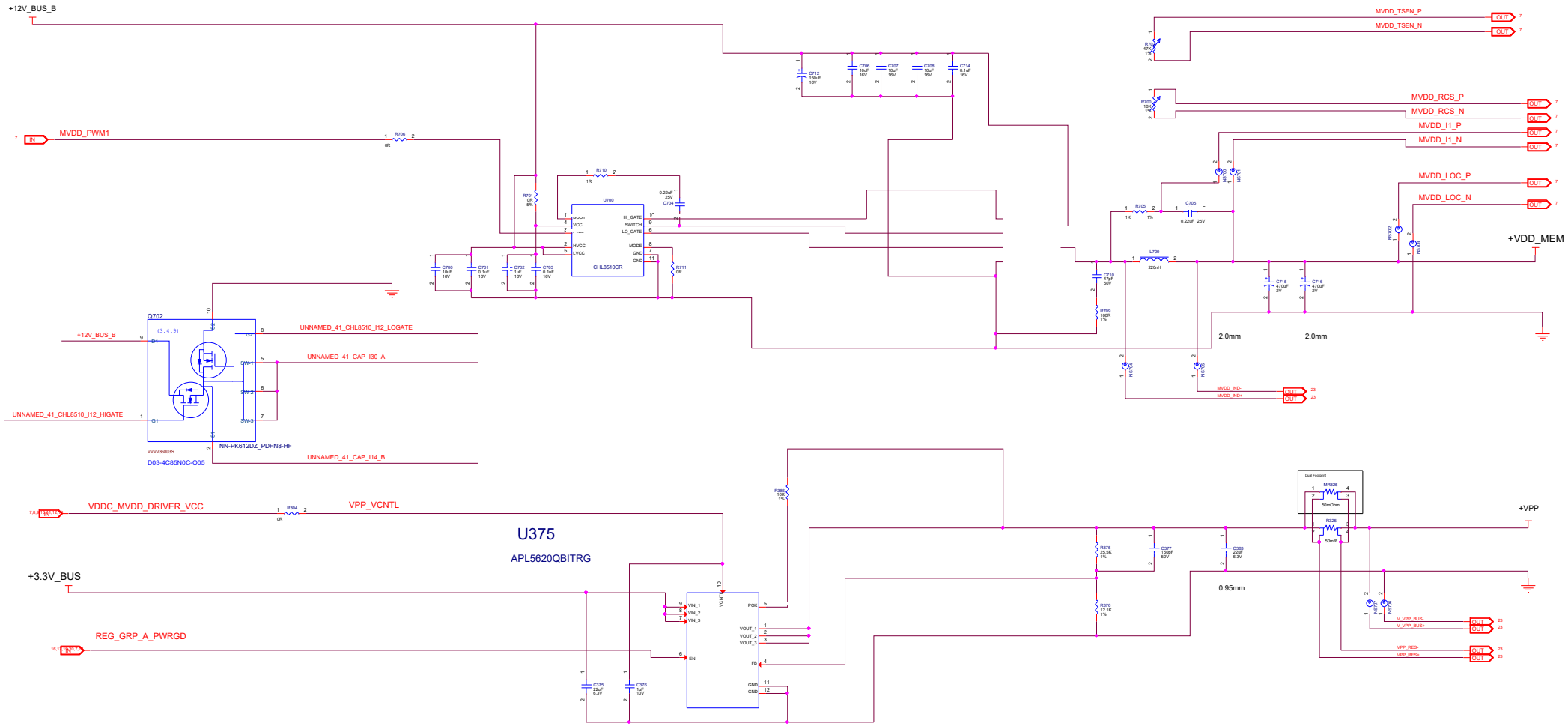
MICRO-STAR INT'L CO.,LTD		
MS-V368		
Size Custom	Document Description: Reg - VDDCR_SOC PHASES II and VIII	Rev 1.1
Date: 2017-08-15	Sheet 12 of 25	



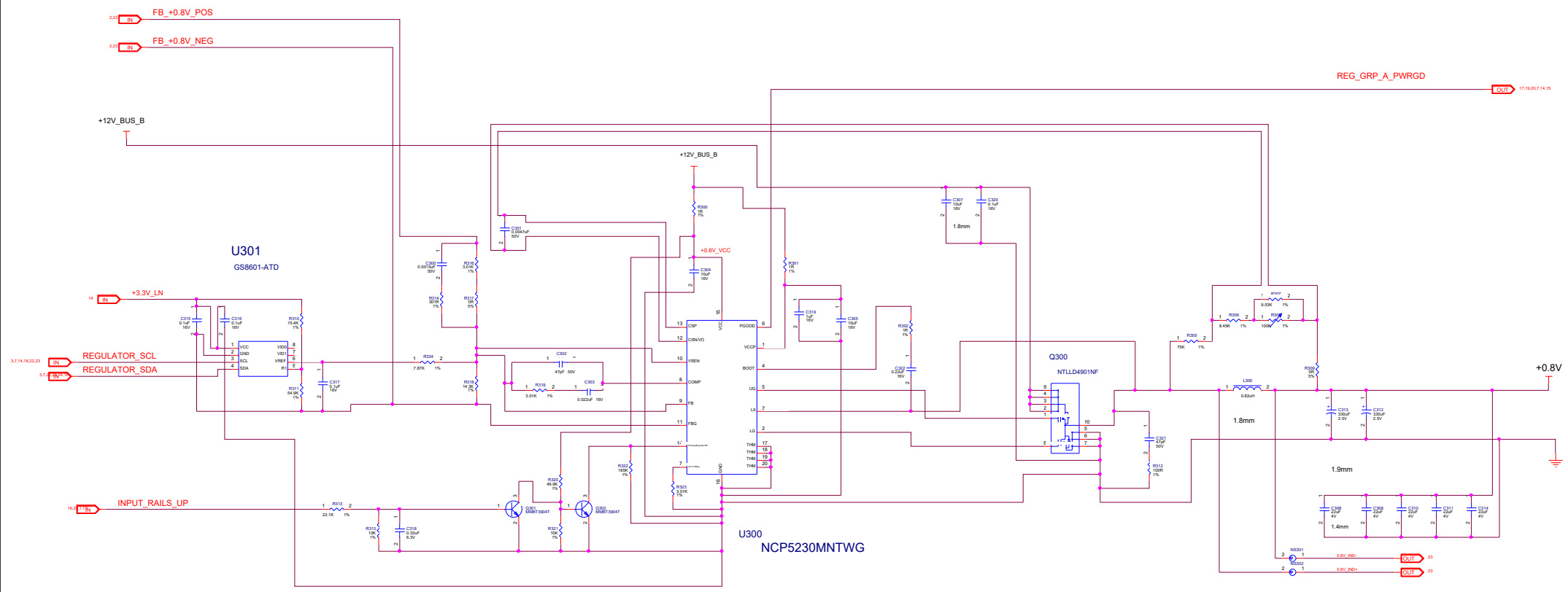
MICRO-STAR INT'L CO.,LTD		
MS-V368		
Size Custom	Document Description: Reg - VDDCR_SOC PHASES VI and XII	Rev 1.1
Date: 2017-08-15	Sheet 13 of 25	



MICRO-STAR INT'L CO.,LTD		
MS-V368		
Size Custom	Document Description Reg - VDDCR_IO	Rev 1.1
Date: 2017-08-15	Sheet 14 of 25	



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V368	
Size Custom	Document Description: Reg - VDDCR_MEM and VPP	Rev 1.1
Date: 2017-08-15	Sheet 15 of 25	



MICRO-STAR INT'L CO.,LTD

MS-V368

Size	Document Description	Rev
Custom	Reg - 0V8	1.1

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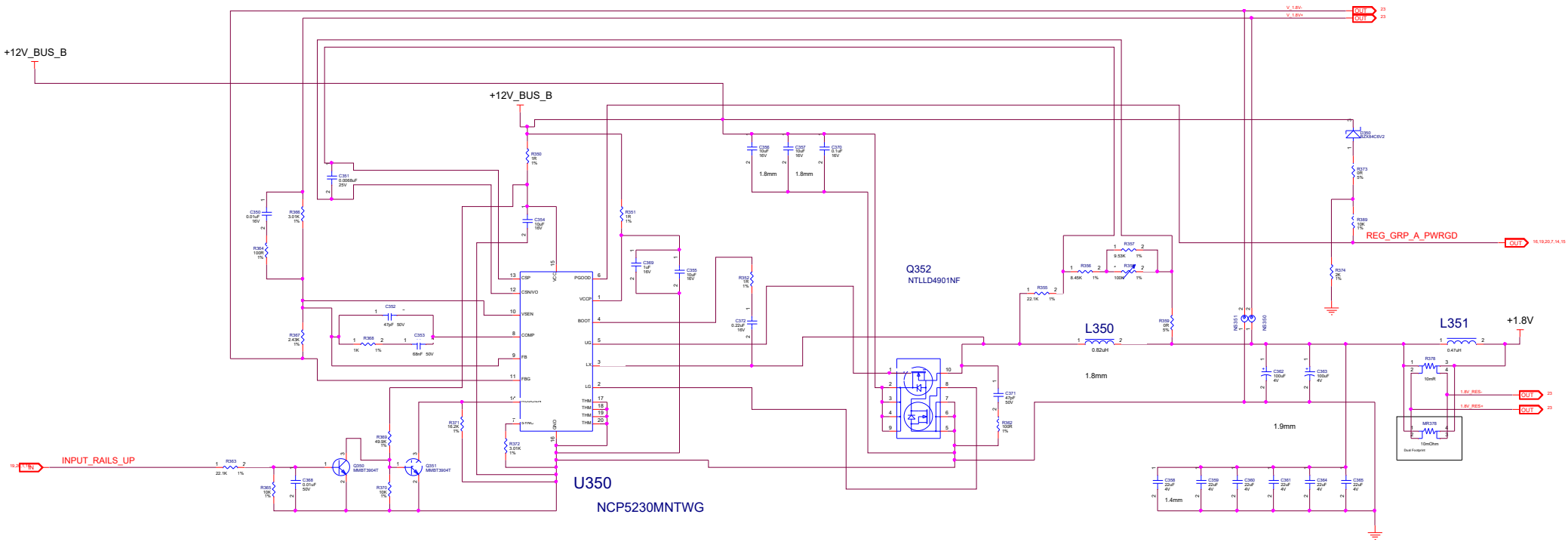
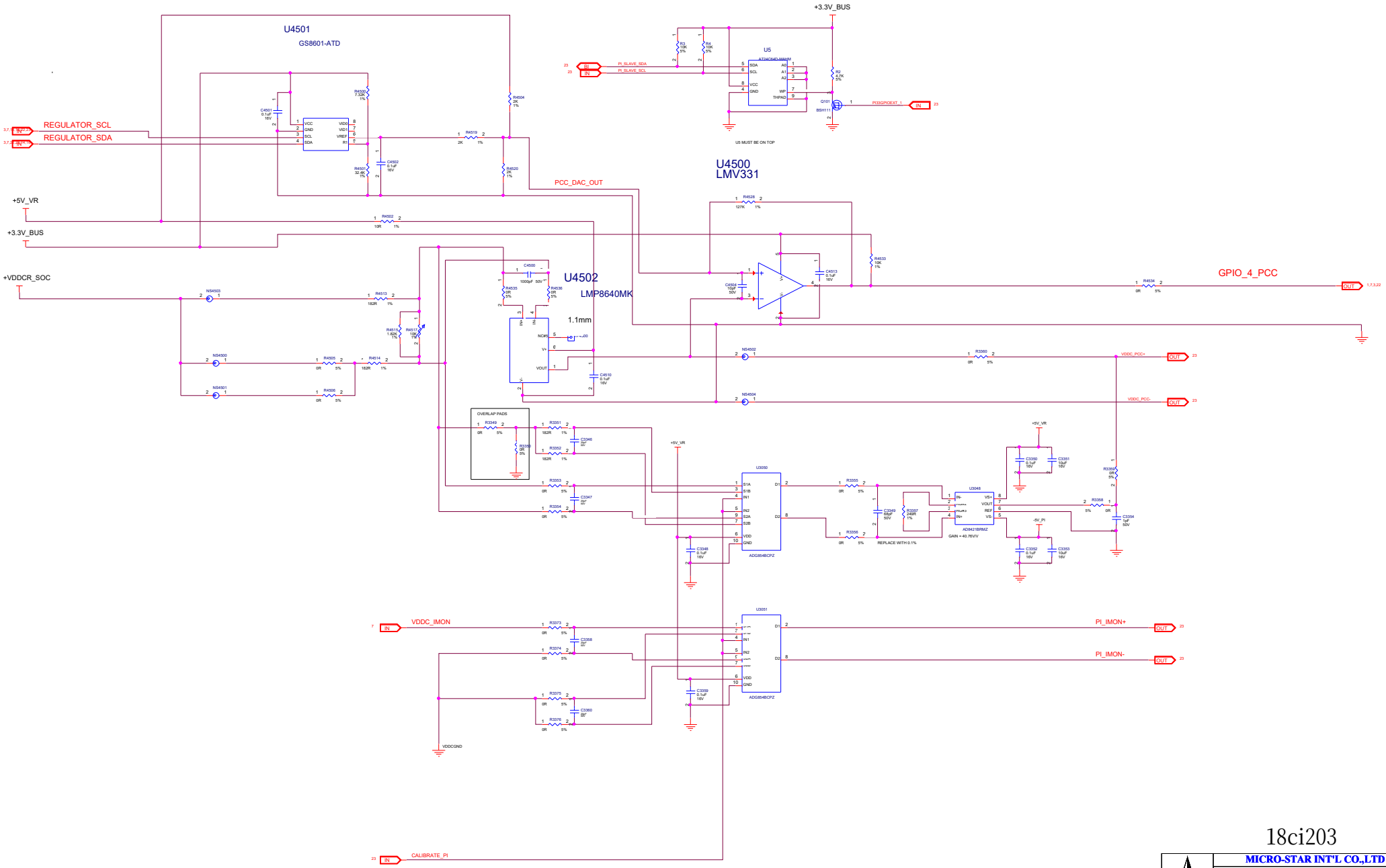


MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V368	
Size Custom	Document Description: Reg - 1V8 / VDDCR_BACO	Rev 1.1
Date: 2017-08-15	Sheet 17 of 25	



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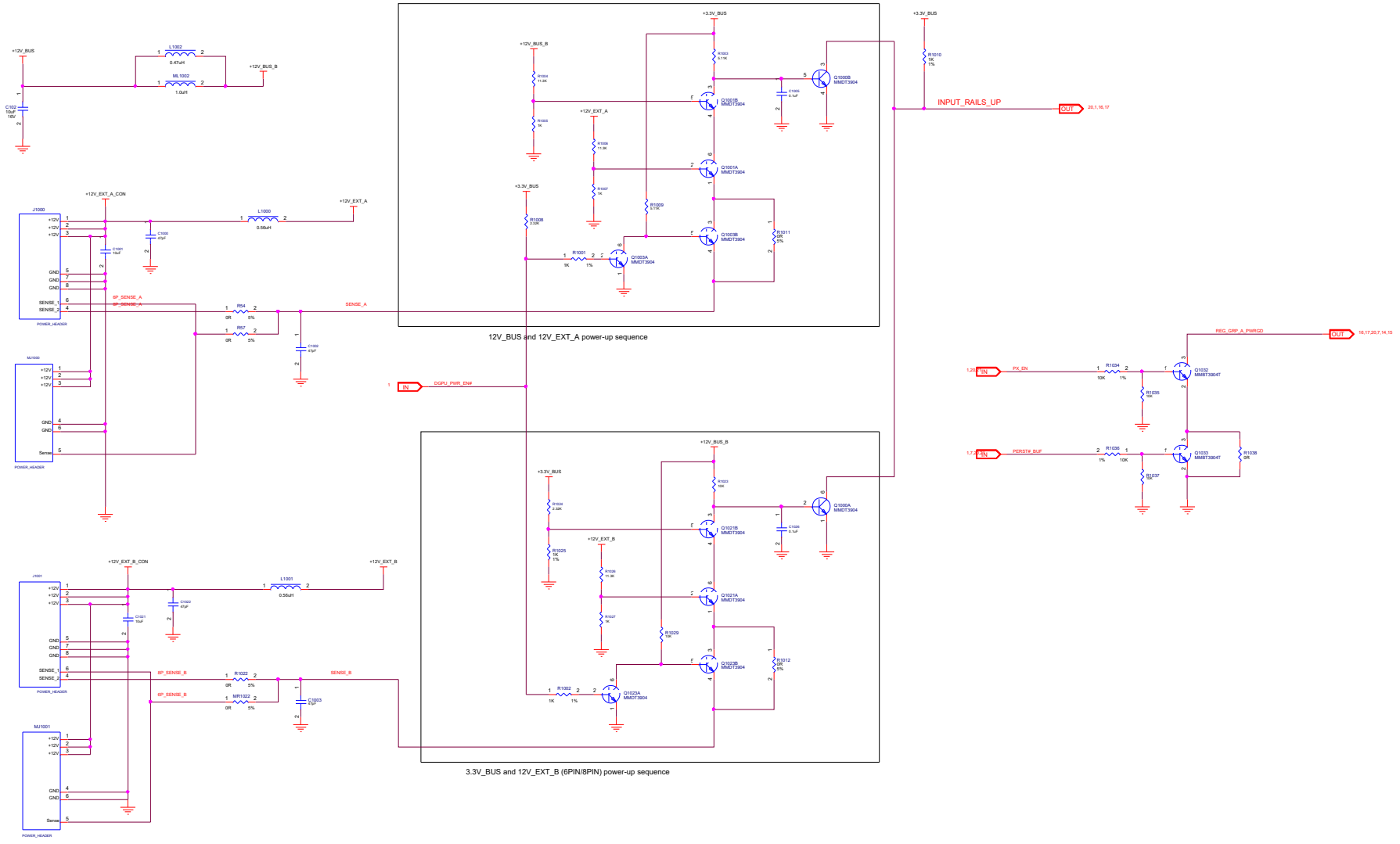
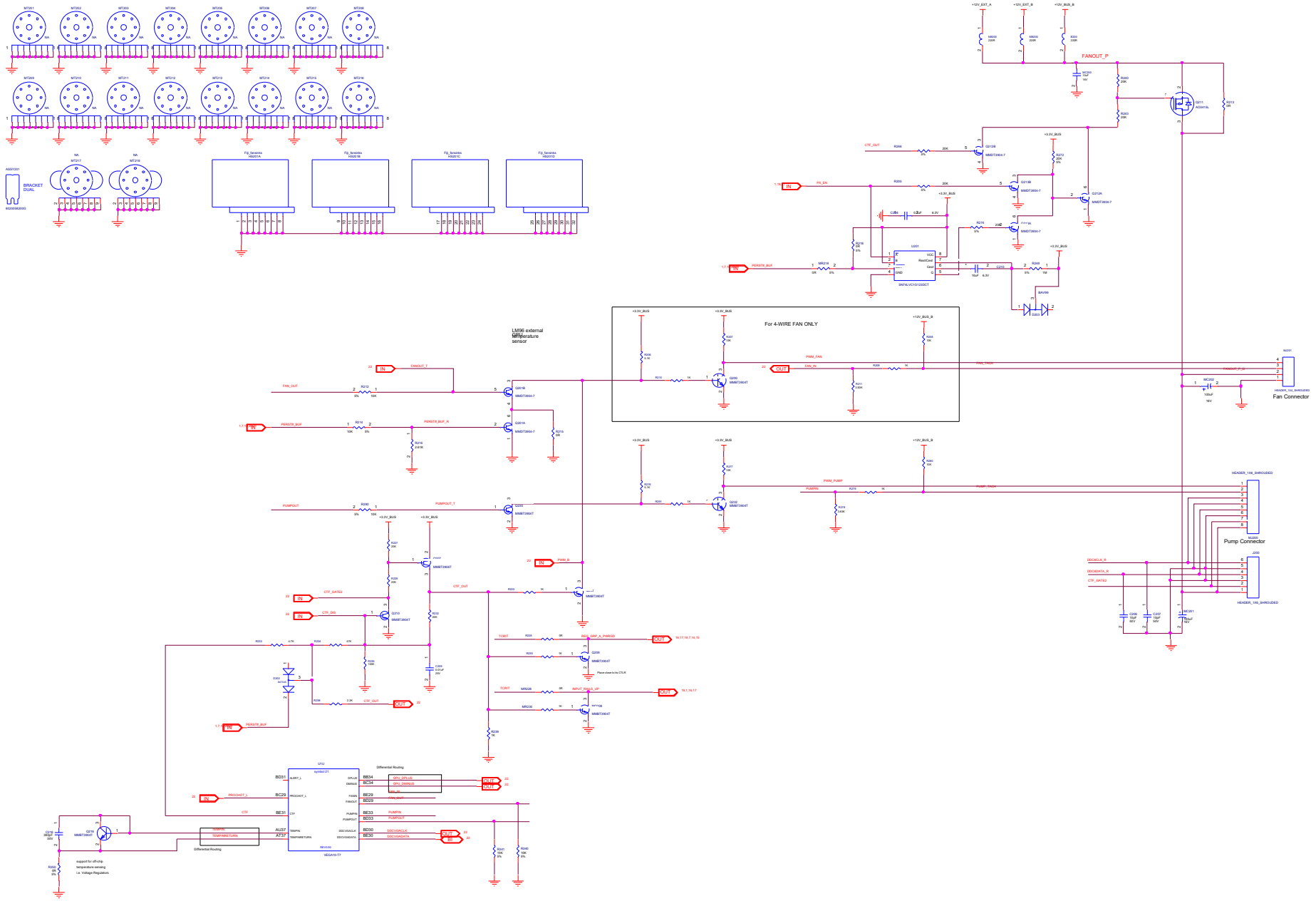
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V368	
Size Custom	Document Description PCC - VDDC	Rev 1.1
Date: 2017-08-15	Sheet 18 of 25	



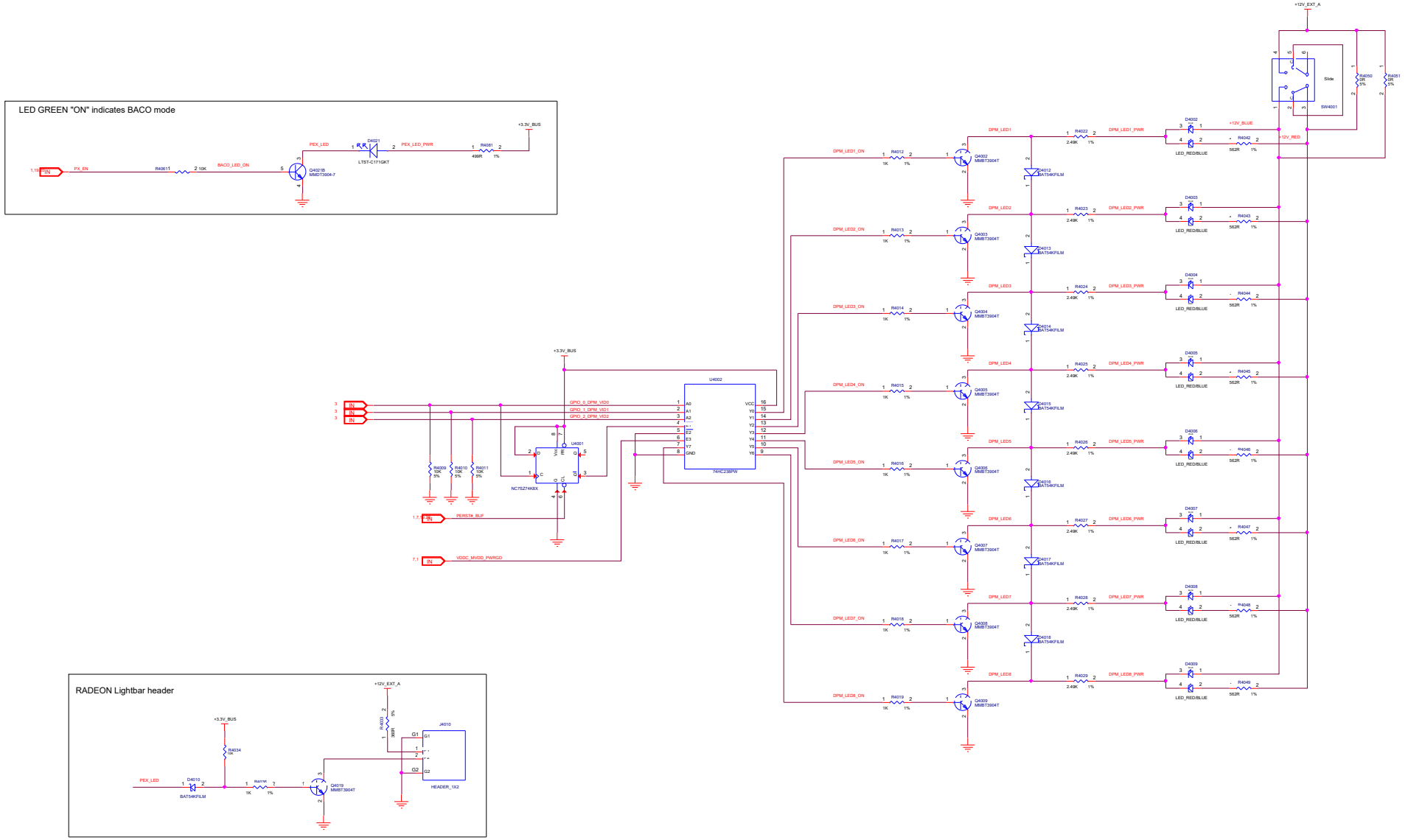
12V_BUS and 12V_EXT_A power-up sequence

3.3V_BUS and 12V_EXT_B (6PIN/8PIN) power-up sequence

MICRO-STAR INT'L CO.,LTD			
MS-V368			
Size Custom	Document Description POWER MANAGEMENT		Rev 1.1
Date: 2017-08-15	Sheet 19 of 25		



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V368	
Size: Custom	Document Description: THERMAL	Rev: 1.1
Date: 2017-08-15	Sheet 20 of 25	



MICRO-STAR INT'L CO.,LTD		
MS-V368		
Size: Custom	Document Description: GPUTACH & BACO LEDs	Rev: 1.1
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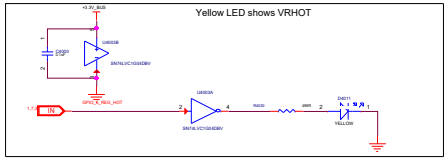
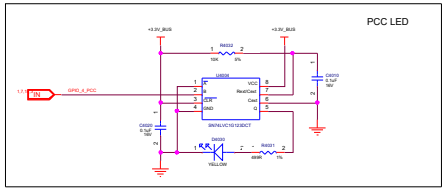
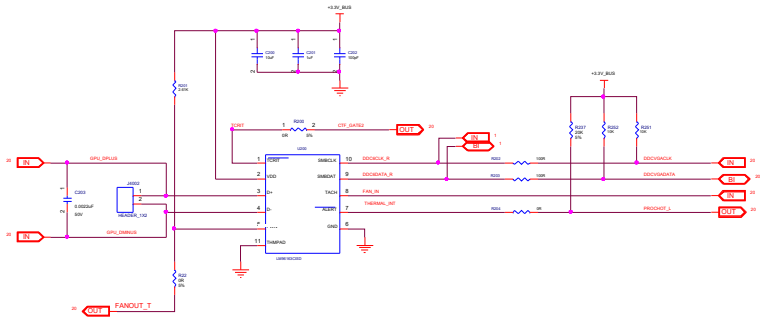
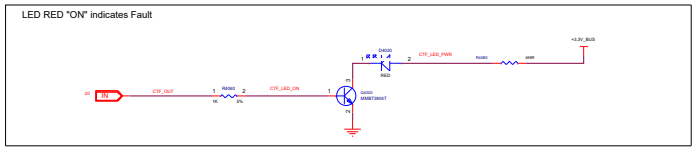
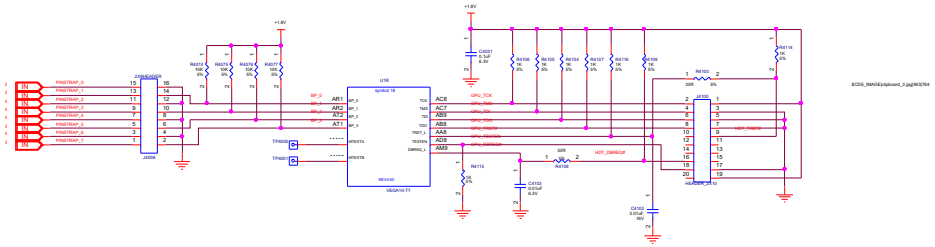




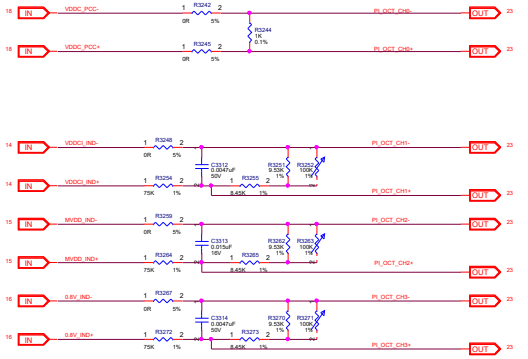


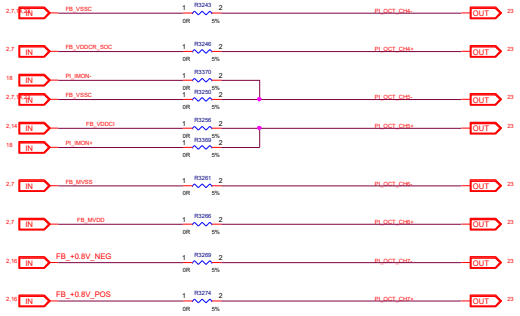


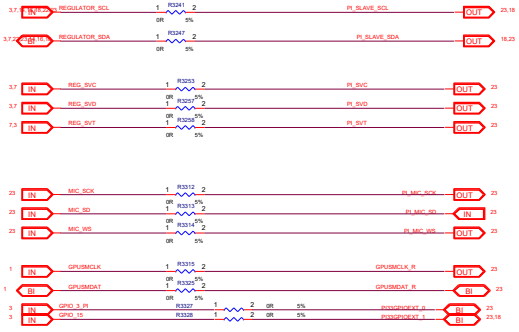


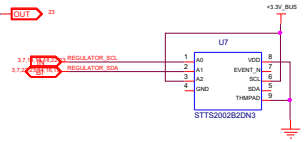
MICRO-STAR INT'L CO.,LTD		
MS-V368		
Size: Custom	Document Description: DEBUG	Rev: 1.1
Date: 2017-08-15	Sheet 22 of 25	

ALL COMPONENTS TO BE LOCATED NEXT TO SENSING ELEMENT (ON MAIN BOARD)
NETS IN GREEN SHOULD BE RE-NAMED





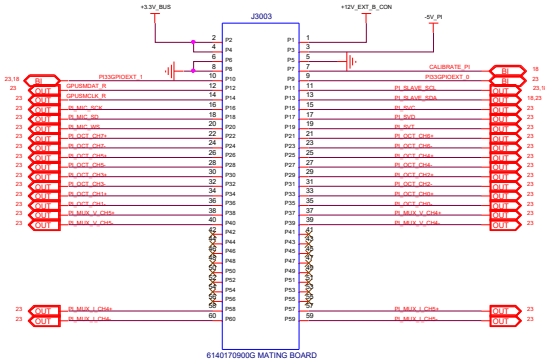




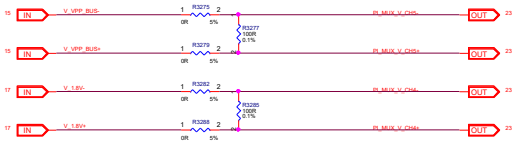
PLACE HOLDER FOR DS28C22

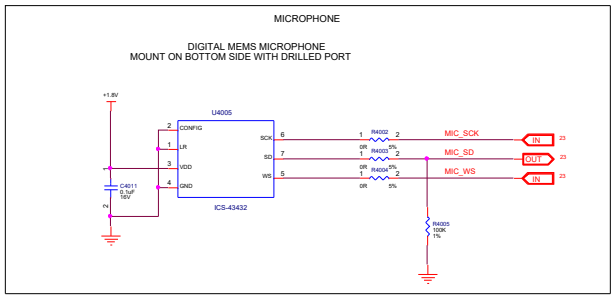
U7 MUST BE ON TOP

RESERVED FOR I2C_MASTER PINS



6140170900G MATING BOARD





MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V368	
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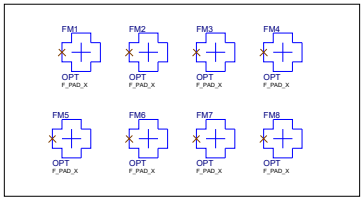

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A	10/9/15	Initial schematic creation
B	6/30/16	Many Changes on PI circuit , Minor Chnages on SMPS
C	9/30/16	Many Changes on PI circuit , ASIC SYMBOL UPDATED FOR FLASH ROM INTERFACE , flash ROM SI/SO swapped , RP1 added
D	11/29/16	Changes on PI circuit , 100MHz HCSL clock source replced (contact AMD for detailes)
E	01/05/17	PI circuit removed , 200R added to DP AUX (6 resistors)
F	02/02/17	1.8V/VPP Kelvin resistors dual footprinted , DP AUX (6 resistors changed to 100R) , Changed R4033 to 360R 1206 and moved to 12V_AUX , SMBUS Address note swap , J4001 removed , R115/R116 changed to 61.9R , R205 added
G	06/29/17	Re-Name to MSI Lable
H	08/15/17	Remove R1013,R1014,R1015,R106 and V_12V_BUS,V_12V_EXTA,V_12V_EXTB,V_3.3V_BUS, 12V_BUS_RES,12V_EXTA_RES,12V_EXTB_RES,3.3V_BUS_RES
I	08/16/17	Change J3003 footprint name from con_mating_samtec_fsi-130-03-x-d-m-ad to con_mating_samtec
I	08/17/17	Remove TP102/105/126/127/106/108/107/106/128/129/110/111/112/113/130/131/114/116/115/117/132/133/118/119/120/121/134/135/122/124/123/125. Change Q702 Footprint , Rename Page 24 to MECH and add 8 + light Point