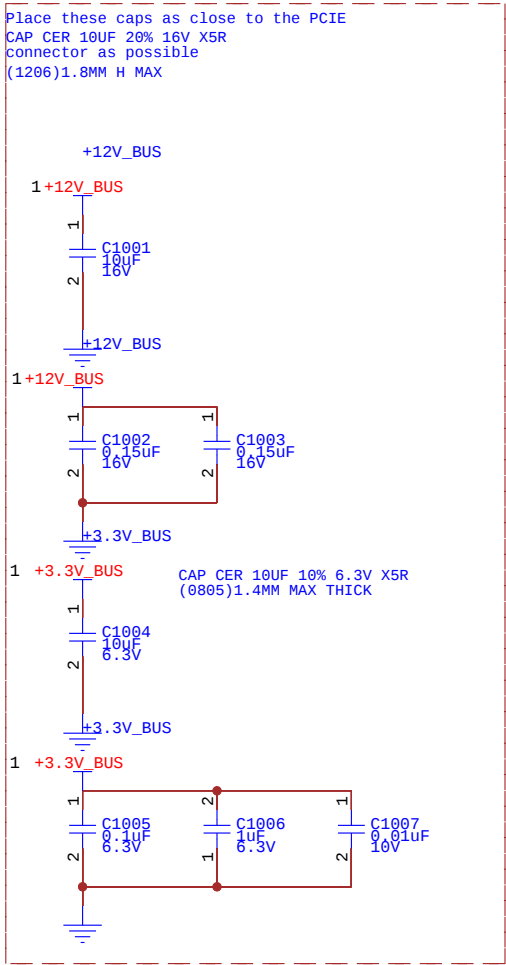


The diagram illustrates the electrical connections for the PCI-Express Edge Connector. It shows two main sections: the connector pins on the left and the corresponding pins on the MPCIE1 module on the right.

- Connector Pins (Left):**
 - SMBCLK:** Pin 1, connected to the SMBCLK pin of the MPCIE1 module.
 - SMBDATA:** Pin 2, connected to the SMBDATA pin of the MPCIE1 module.
 - +3.3V_BUS:** Pins 3 and 4, connected to the +3.3V_BUS pin of the MPCIE1 module.
 - +12V_BUS:** Pins 5 and 6, connected to the +12V_BUS pin of the MPCIE1 module.
- MPCIE1 Module Pins (Right):**
 - B1:** +12V
 - B2:** +12V
 - B3:** +12V
 - B4:** GND
 - B5:** SMBCLK
 - B6:** SMBDATA
 - B7:** GND
 - B8:** +3.3V



SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY



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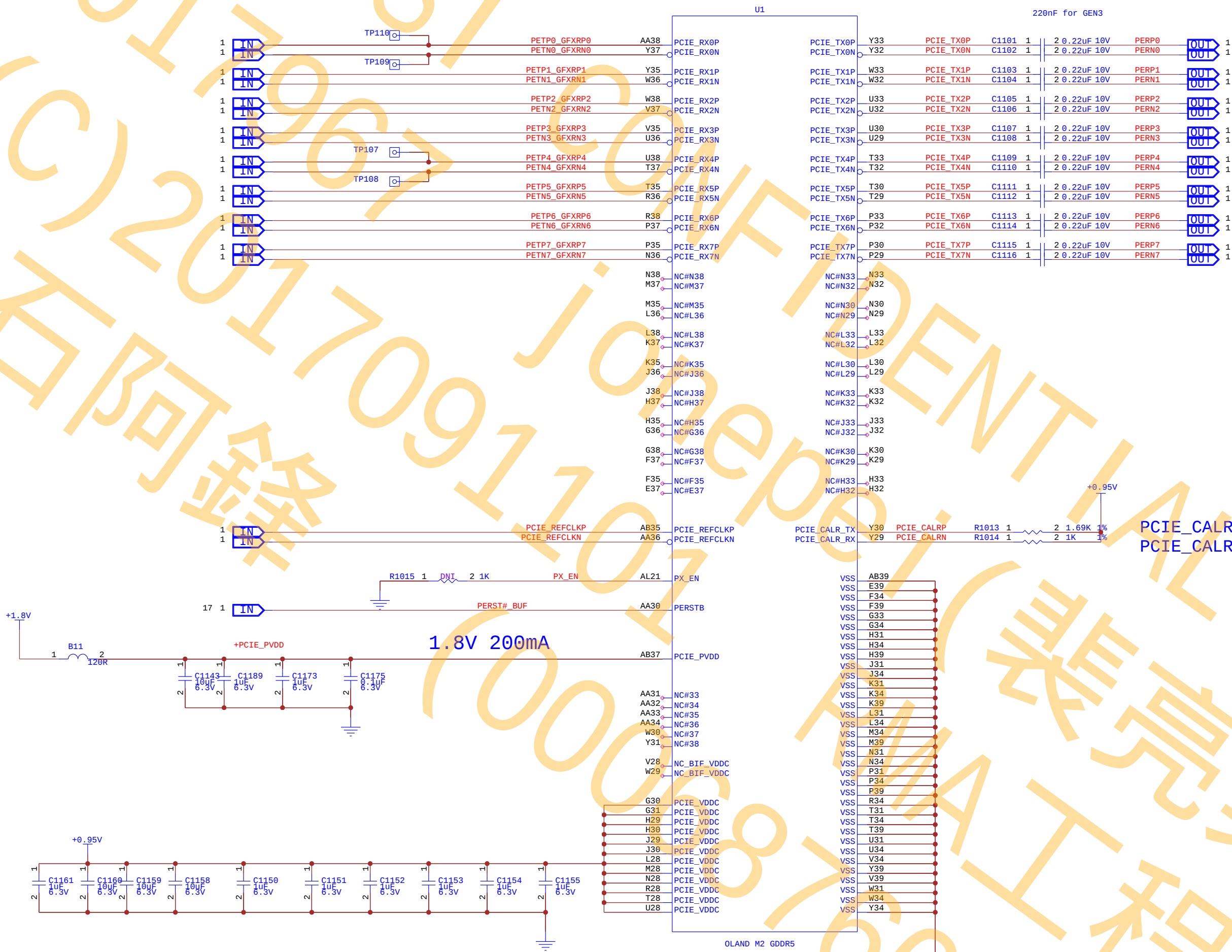
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SHEET: PCI-E Edge Connector		AMD makes no representations or warranties of any schematic and design, including, not limited to, a of merchantability or fitness for a particular purpose responsibility for any consequences resulting from information included herein.	
DATE: Fri Oct 28 17:09:42 2016	REV: 1.0		
SHEET NUMBER: 1 OF 21		TITLE:	
DOCUMENT NUMBER: 105_CXXX00_00A		TITLE	

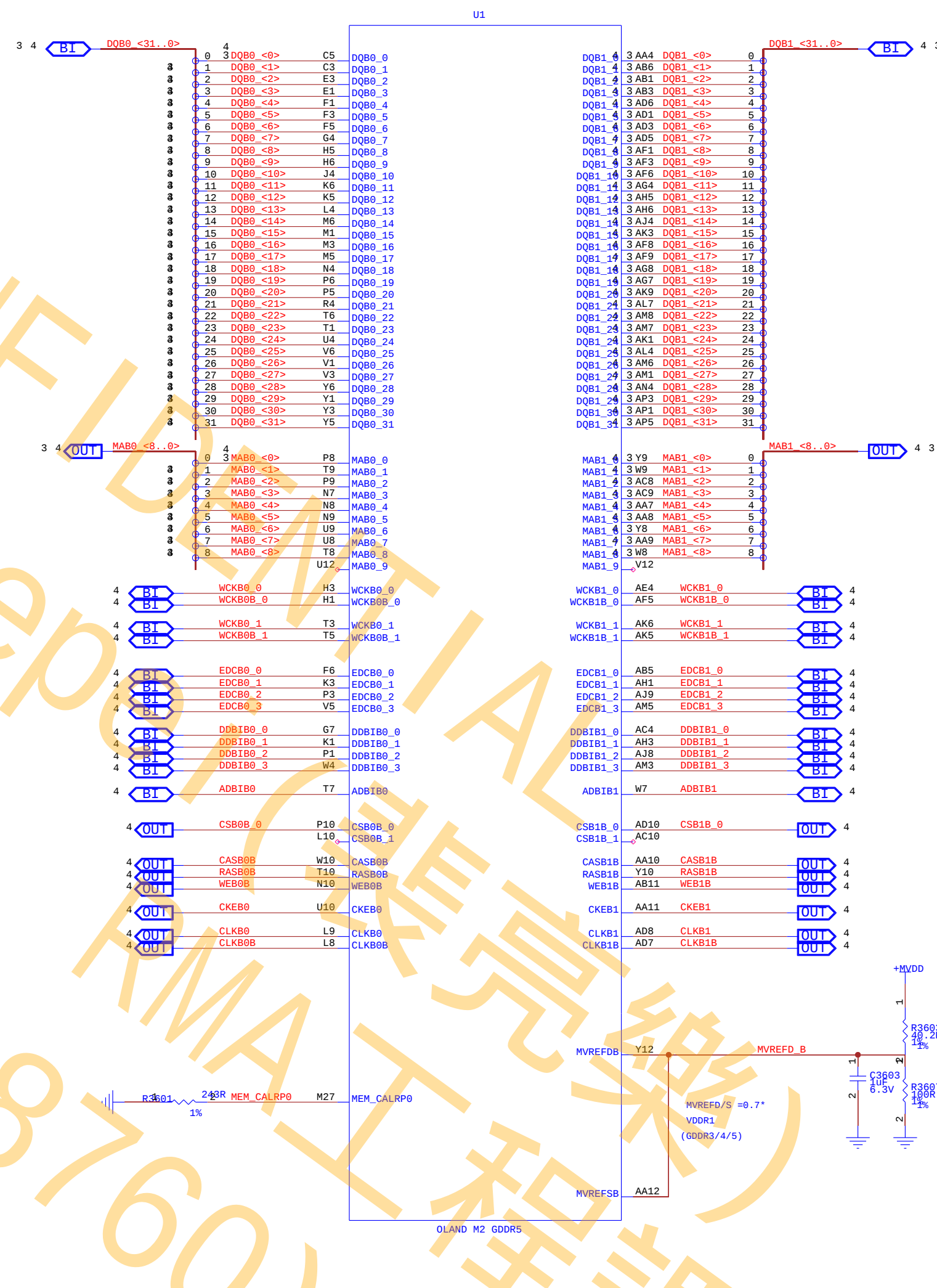
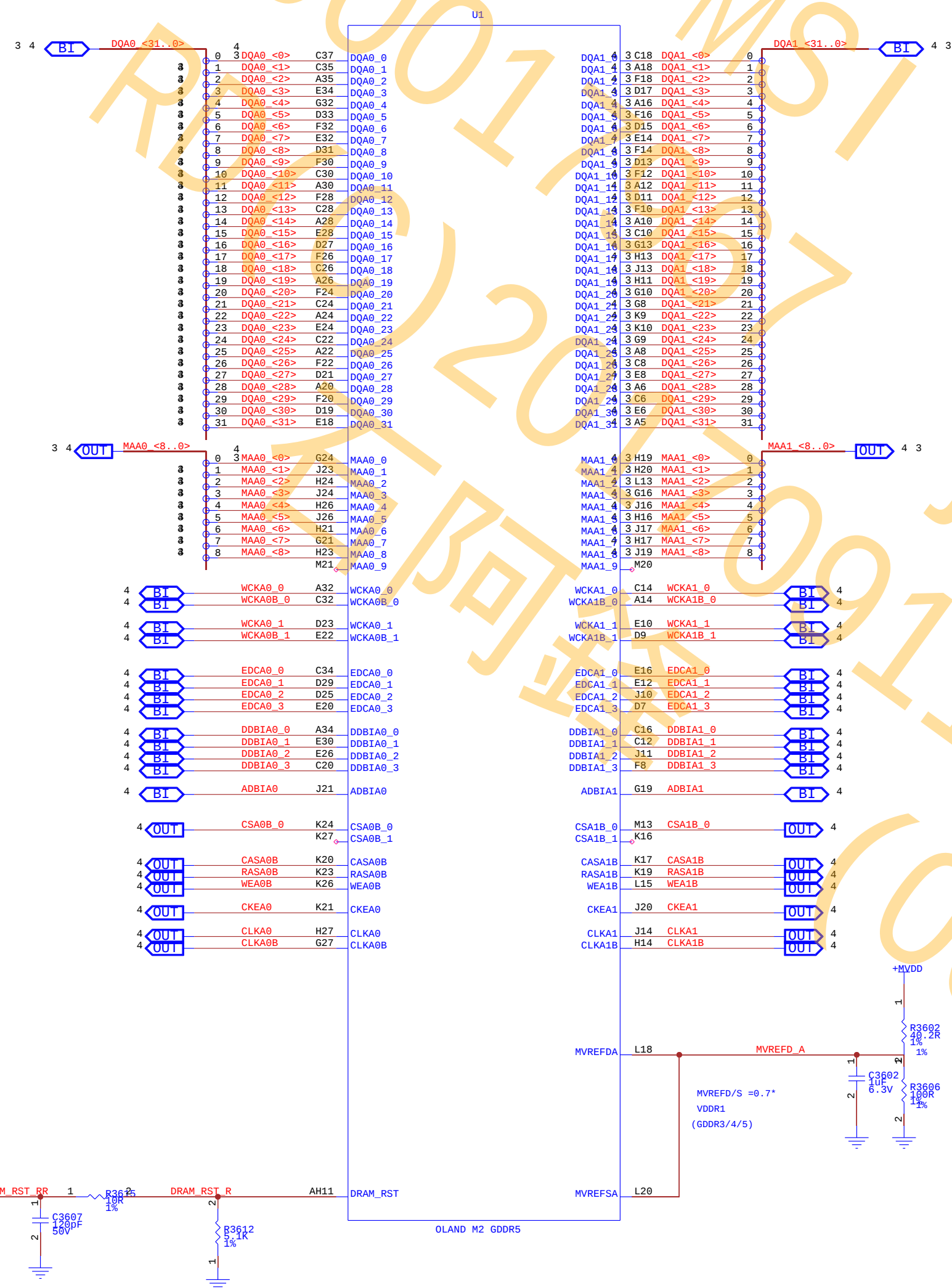
Oland PCIe Interface

NOTE: Some of the PCIe testpoints will be available through vias on traces.



PCIe_CALR_TX 1.69k pull up for Oland
PCIe_CALR_RX 1k pull up for Oland

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SHEET: Oland PCIe Interface		TITLE:	
DATE: Fri Oct 28 17:09:40 2016	REV: 1.0	TITLE	
SHEET NUMBER: 2 OF 21			
DOCUMENT NUMBER: 105_CXX00_00A			



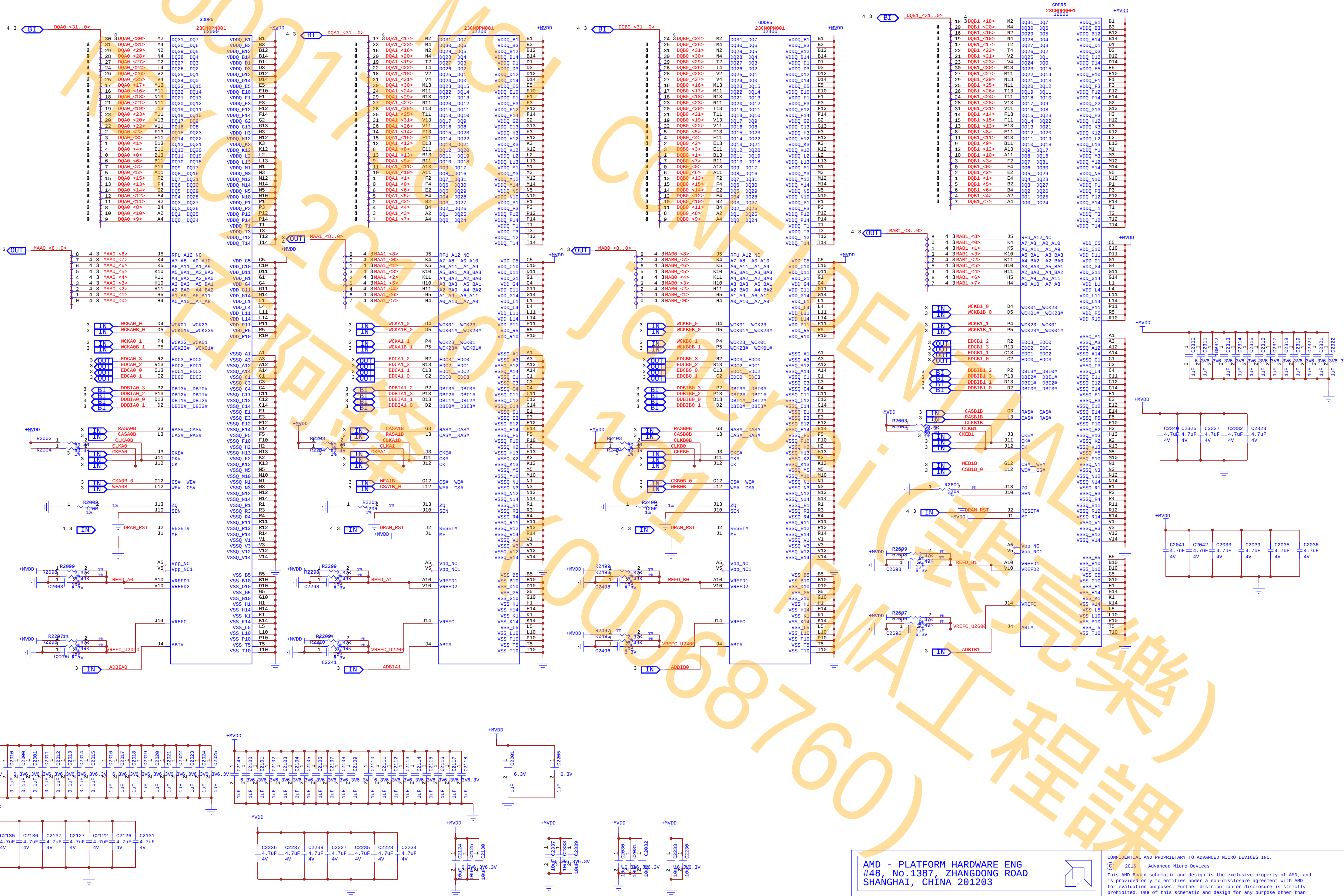
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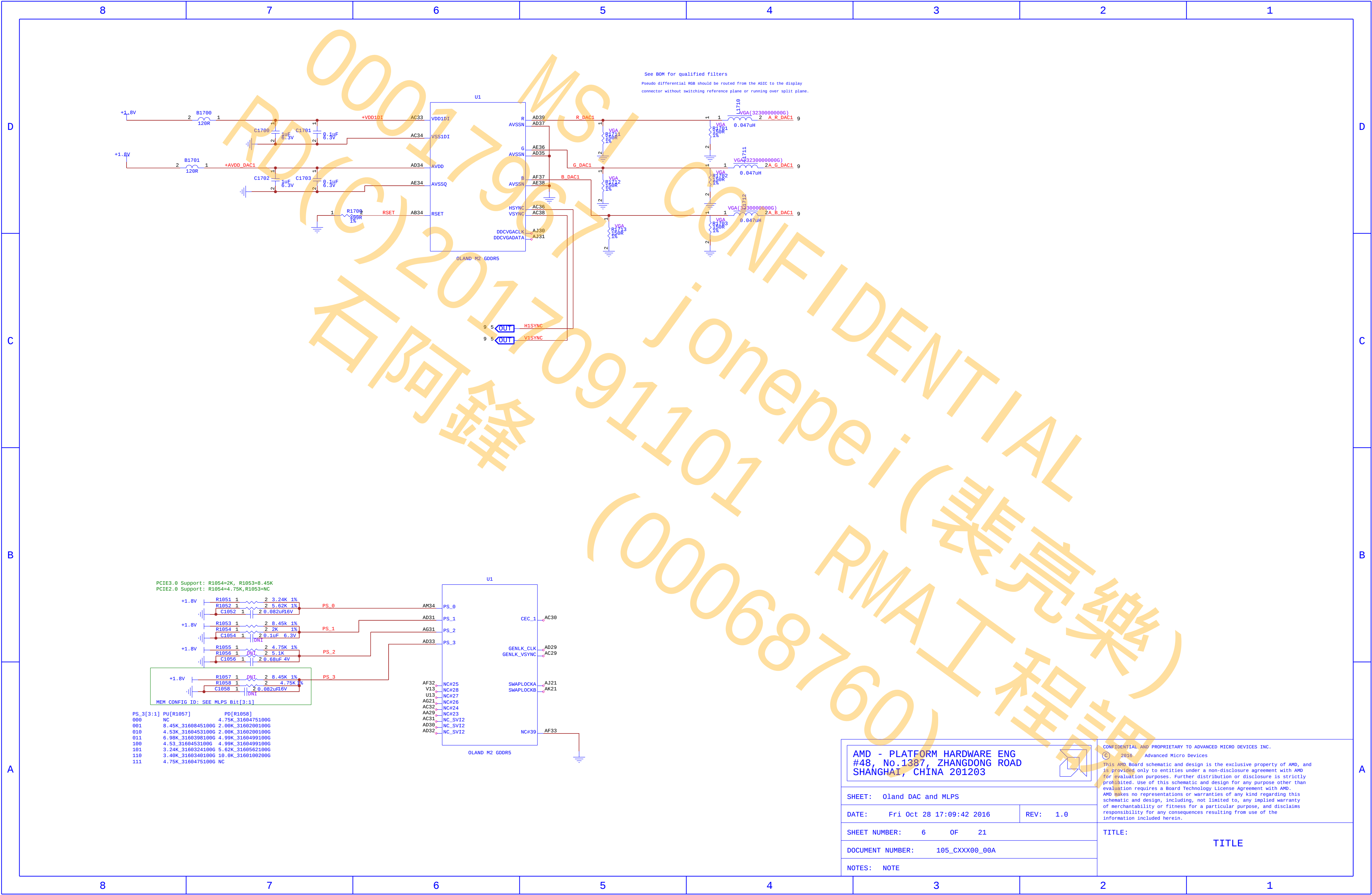
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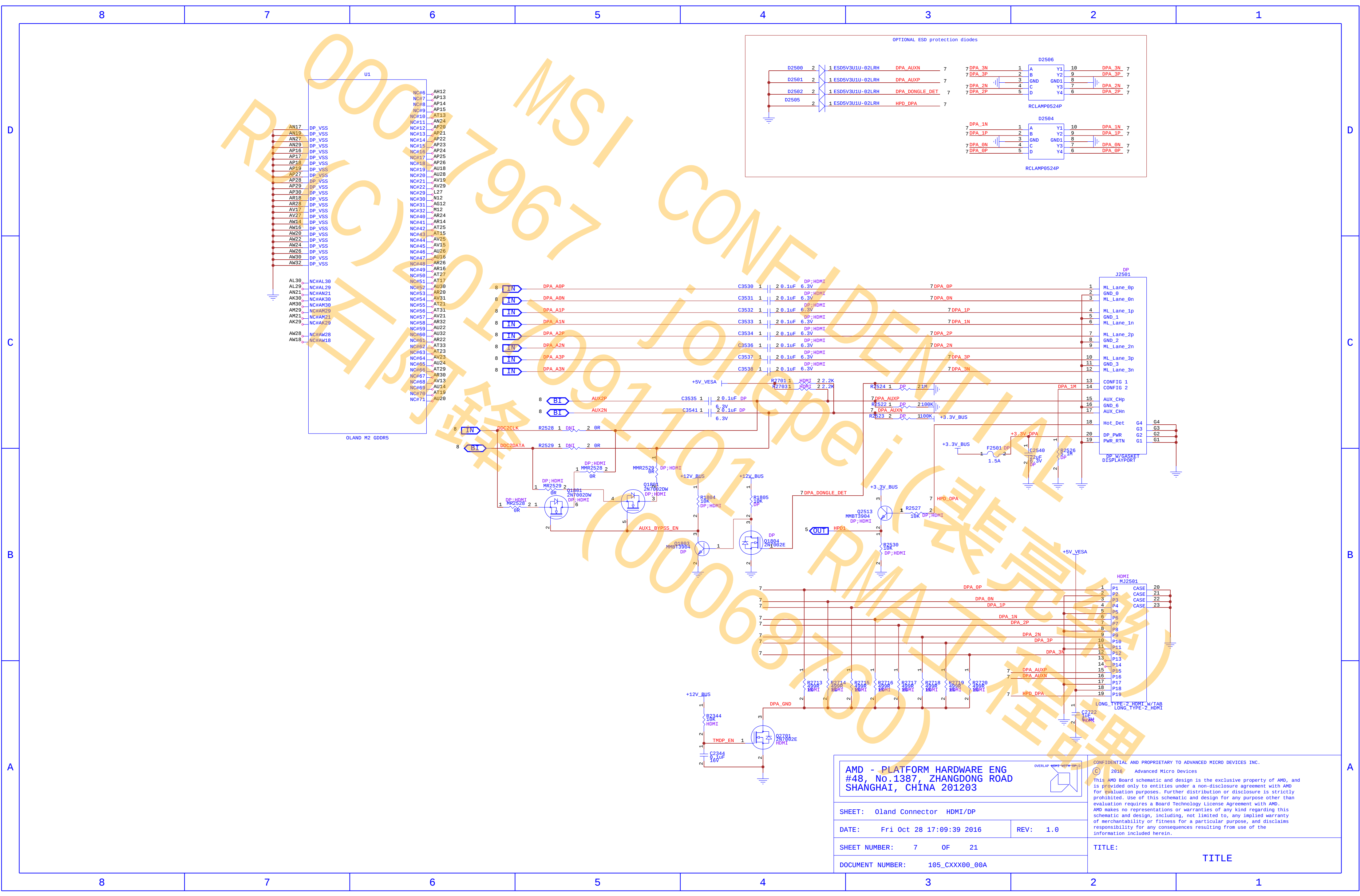
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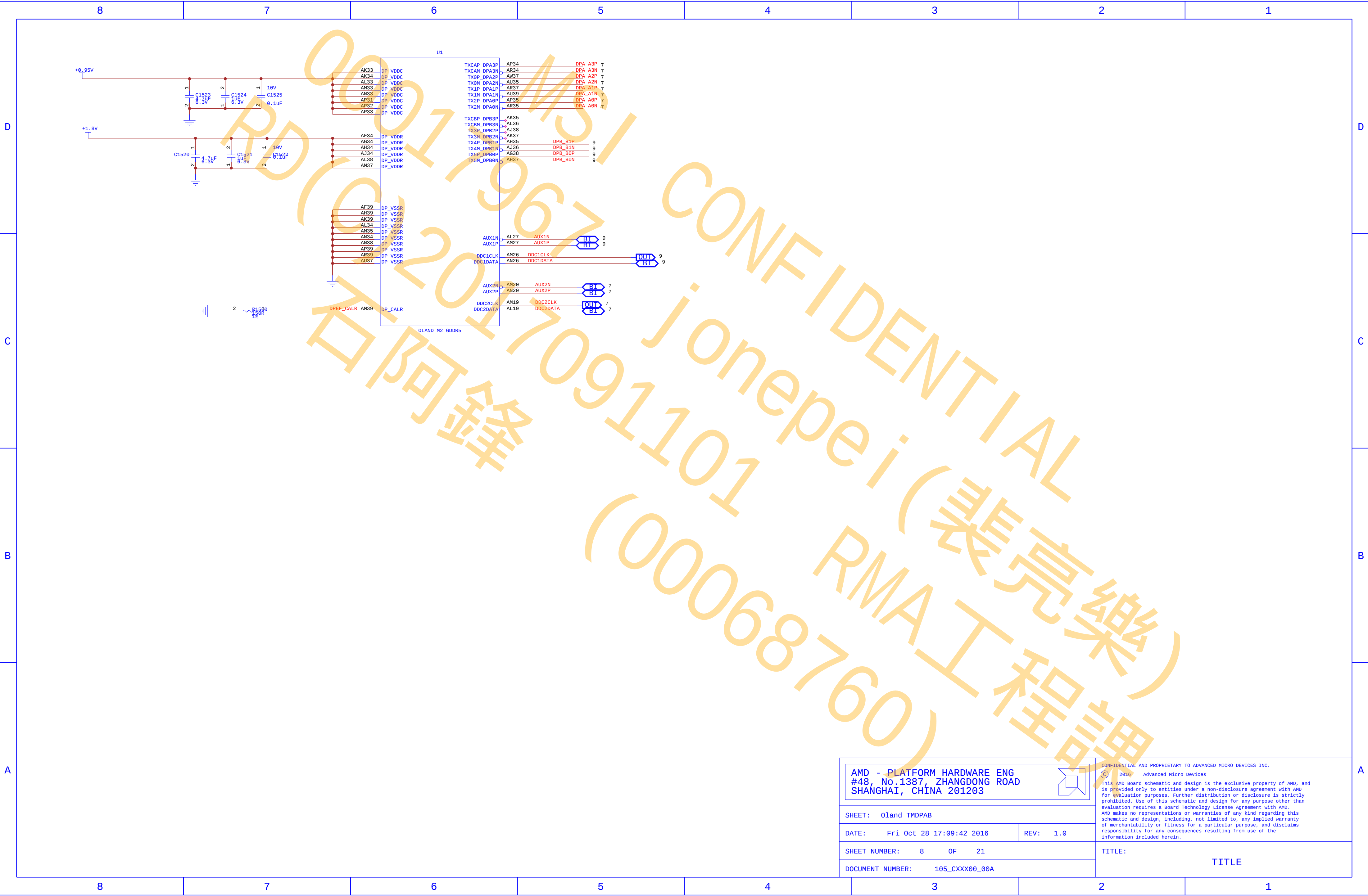
(4) GDDR5 Memory Channel A&B



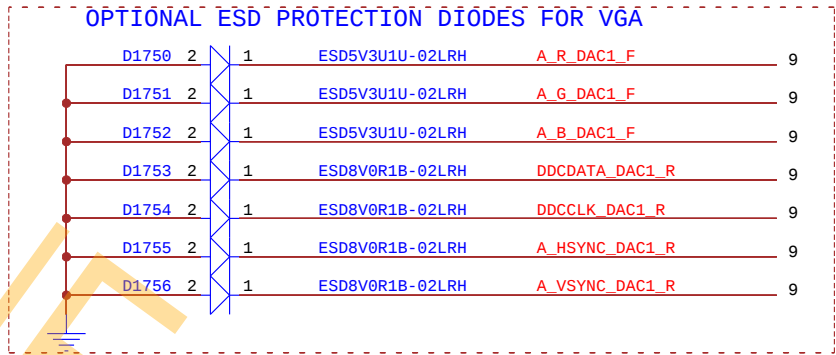


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SHEET: 0land DAC and MLPS			TITLE: TITLE		
DATE: Fri Oct 28 17:09:42 2016		REV: 1.0			
SHEET NUMBER: 6 OF 21					
DOCUMENT NUMBER: 105_CXXX00_00A					
NOTES: NOTE					



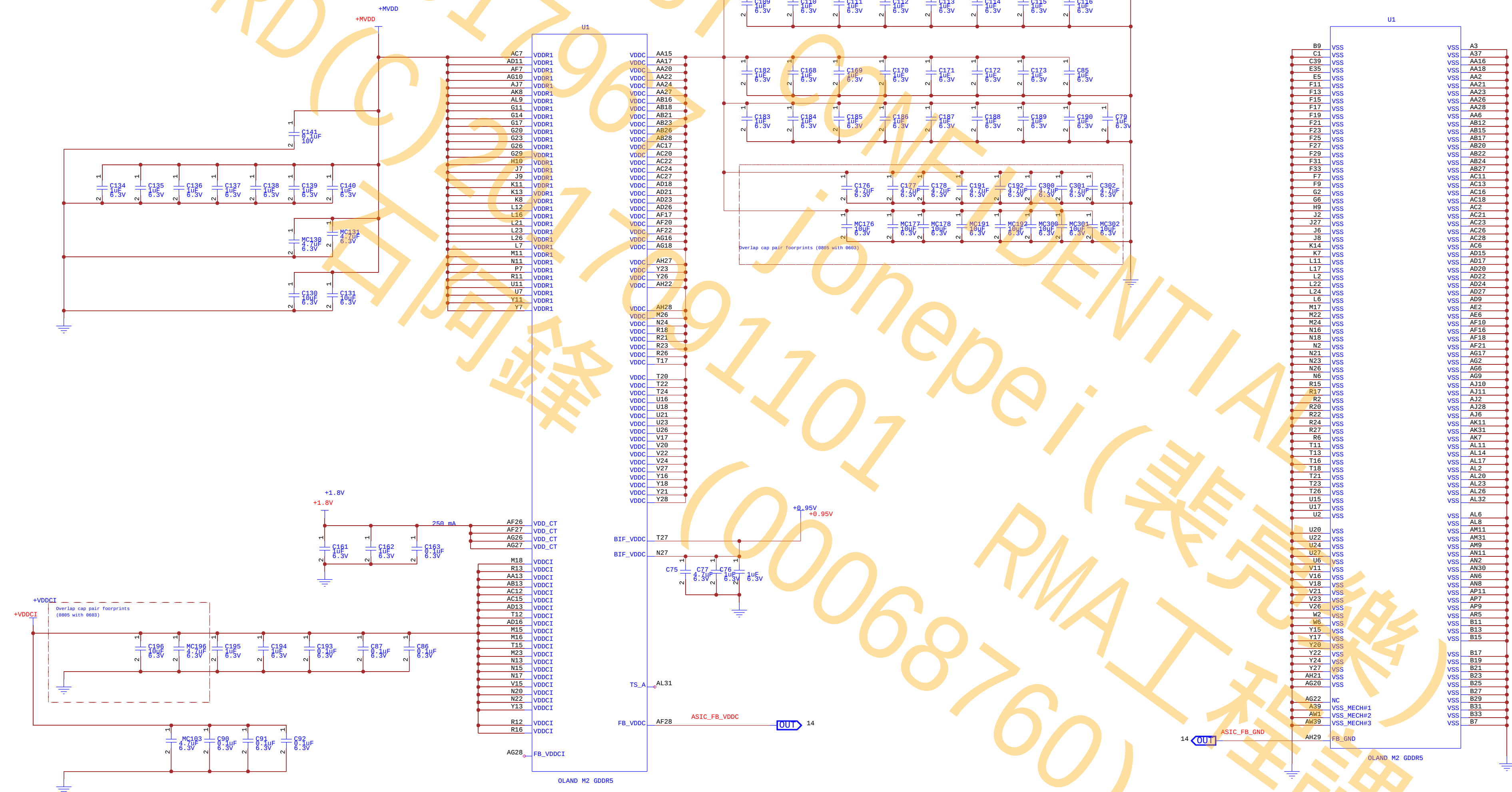


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SHEET: 0land TMDPAB			TITLE: TITLE		
DATE: Fri Oct 28 17:09:42 2016		REV: 1.0			
SHEET NUMBER: 8 OF 21					
DOCUMENT NUMBER: 105_CXXX00_00A					



TITLE

OLAND Power & GND



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SHEET: 01and Power&GND

DATE: Fri Oct 28 17:09:41 2016

SHEET NUMBER: 10 OF 21

DOCUMENT NUMBER: 105_CXXX00_00A

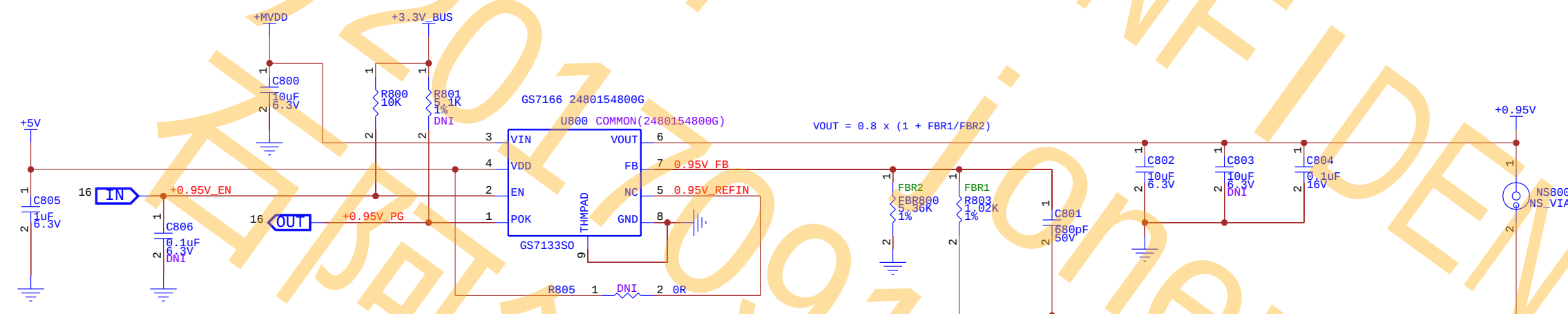
TITLE:

TITLE

Linear Regulators

LDO #1: Vin = +1.5V +/-2% Vout = +0.95V +/- 2% Iout = 1.44A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling



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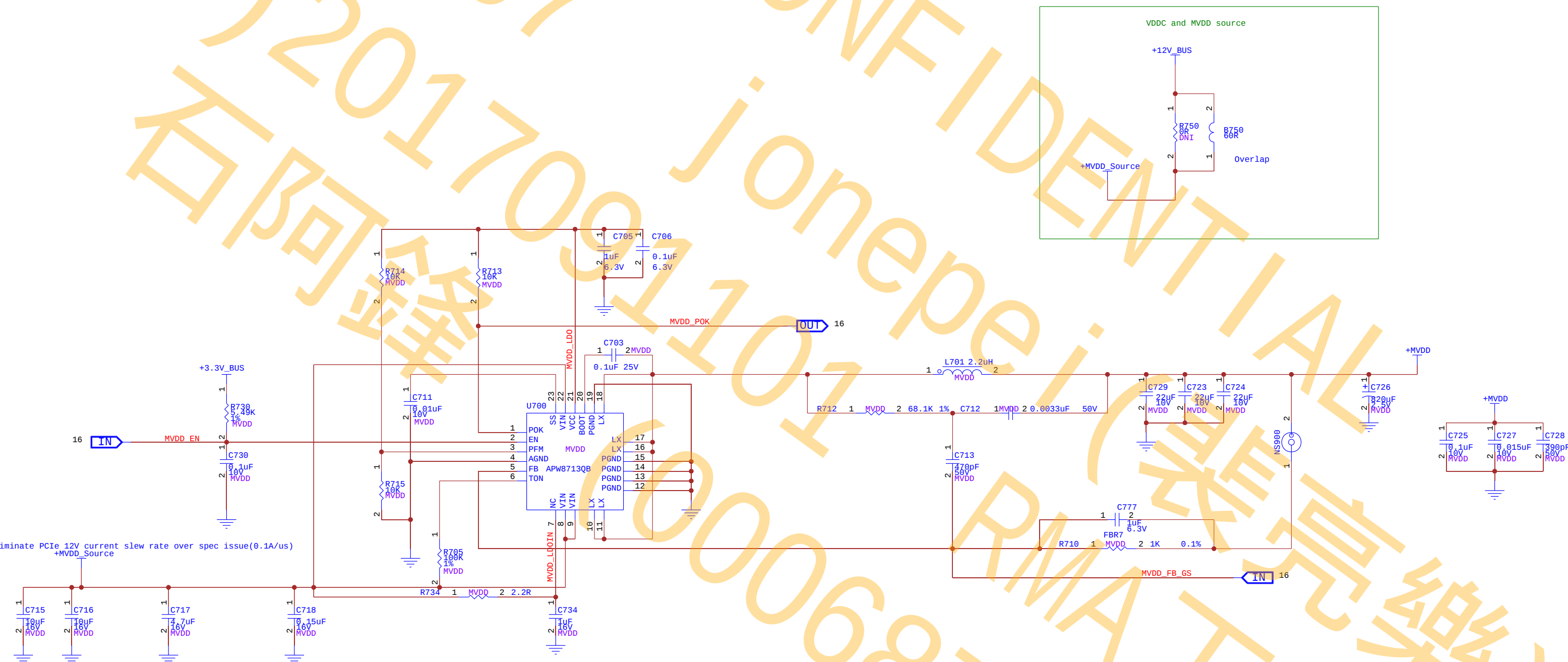
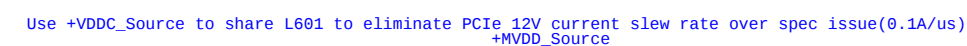
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REV: 1.0

SHEET NUMBER: 11 OF 21

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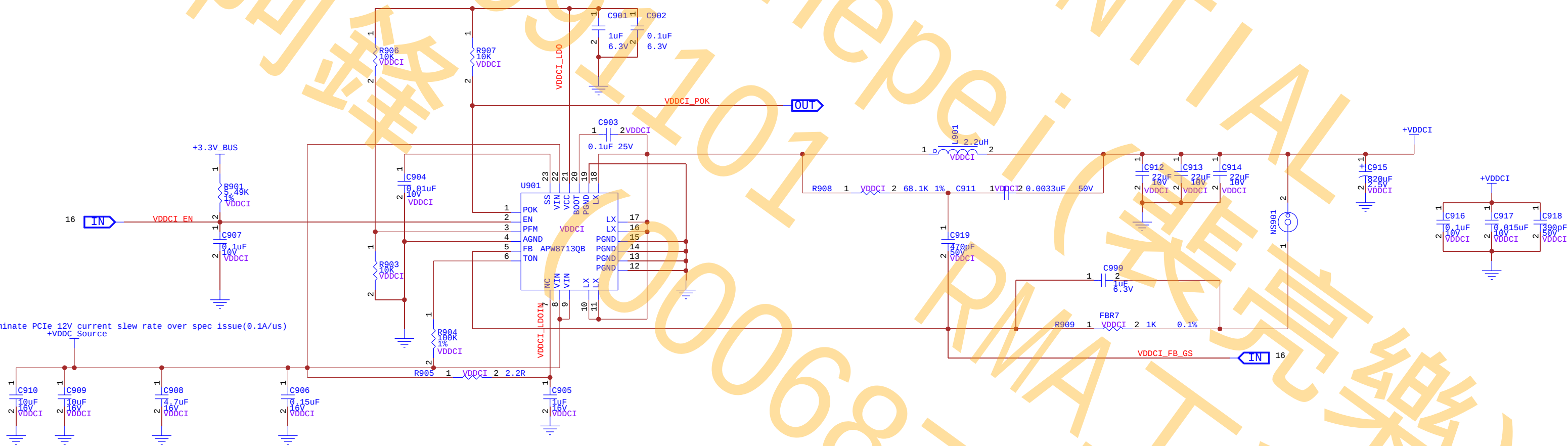


TITLE 17ci203

TITLE 17ci203

Regulator for MVDD

Use +VDDC_Source to share L601 to eliminate PCIe 12V current slew rate over spec issue(0.1A/us)
+VDDC_Source



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SHEET: VDDCI

DATE: Fri Oct 28 17:09:39 2016

REV: 1.0

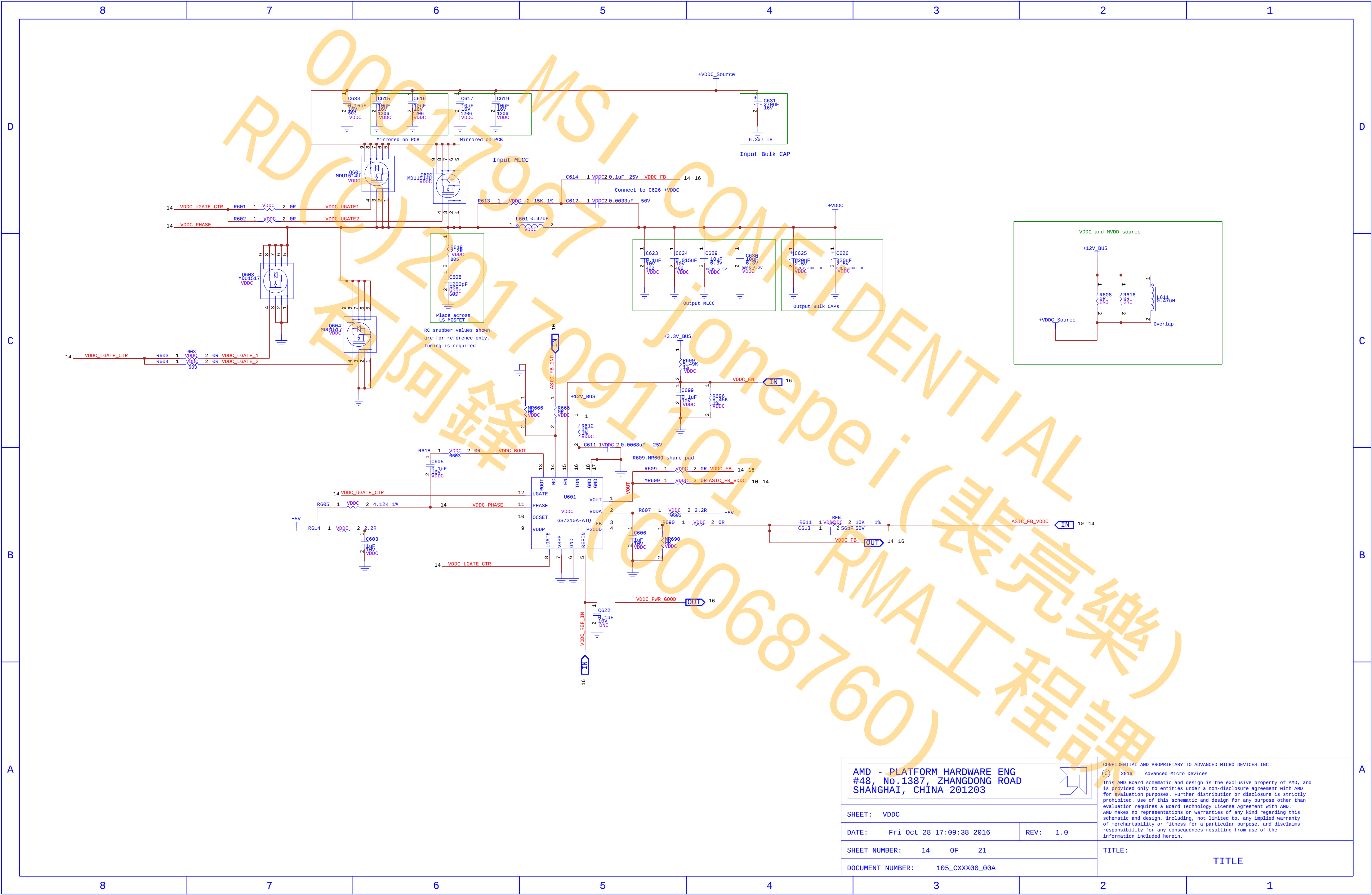
SHEET NUMBER: 13 OF 21

DOCUMENT NUMBER: 105_CXX00_00A

NOTES: NOTE

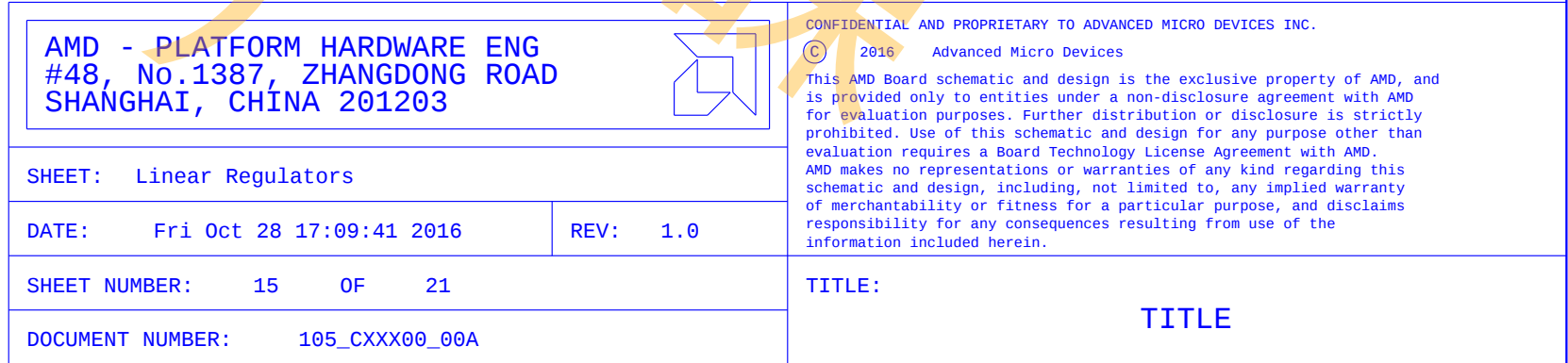
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TITLE 17ci203

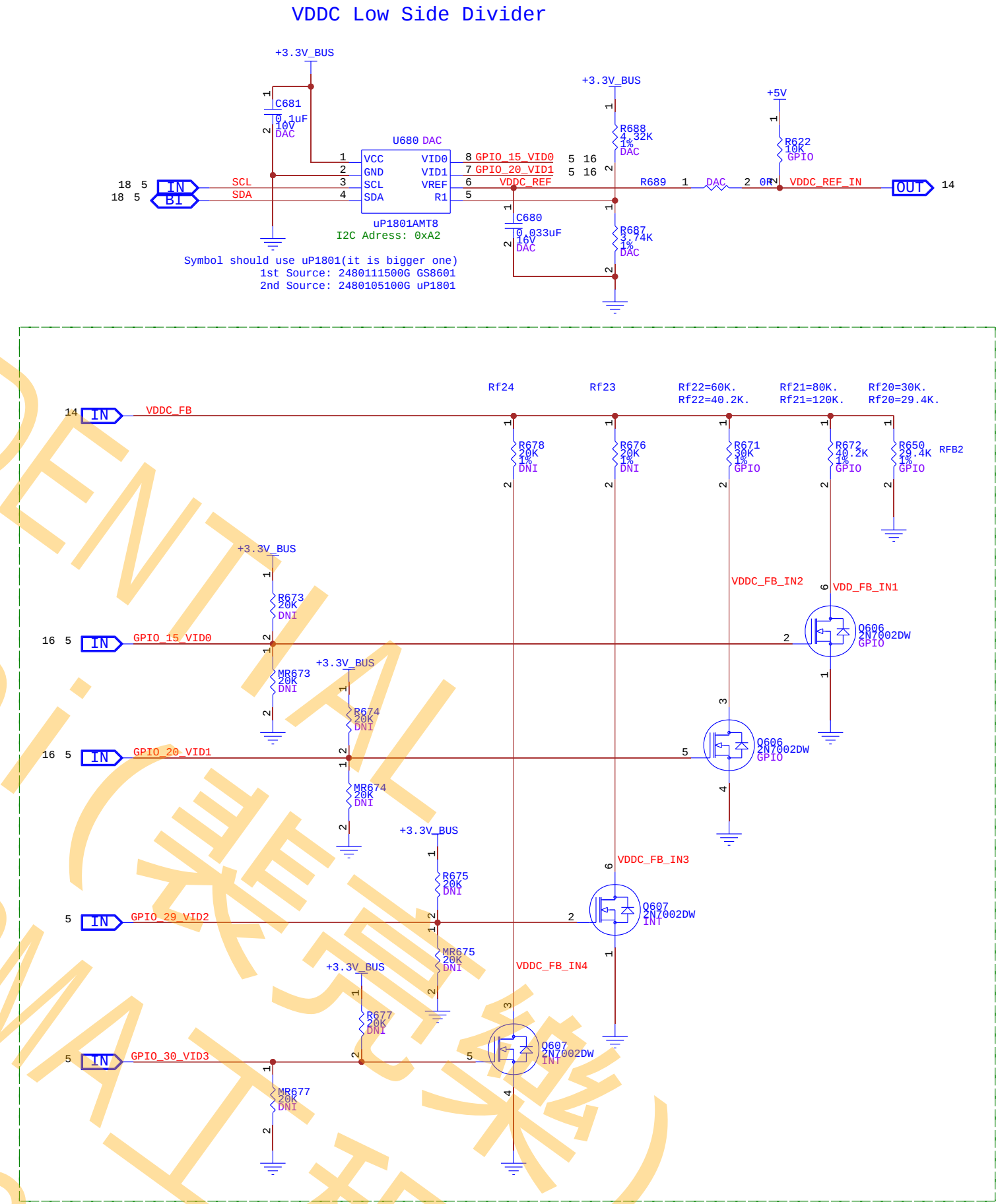


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SHEET: VDDC		TITLE:	
DATE: Fri Oct 28 17:09:38 2016	REV: 1.0	TITLE	
SHEET NUMBER: 14 OF 21	DOCUMENT NUMBER: 105_CXX00_00A		

LDO #2: Vin = 3.00V to 3.60V (3.3V +/- 9%) Vout = +1.8V +/- 2%; Iout = 1.6A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



Don't support BACO
Support CTF(Internal)



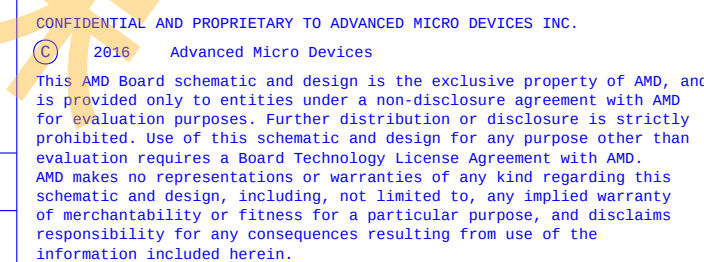
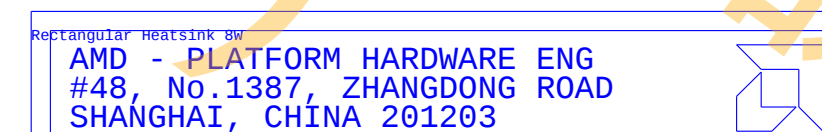
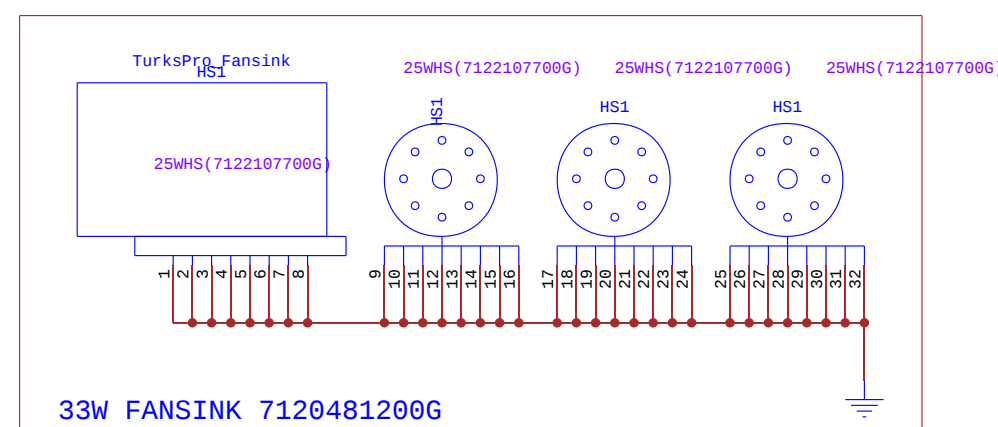
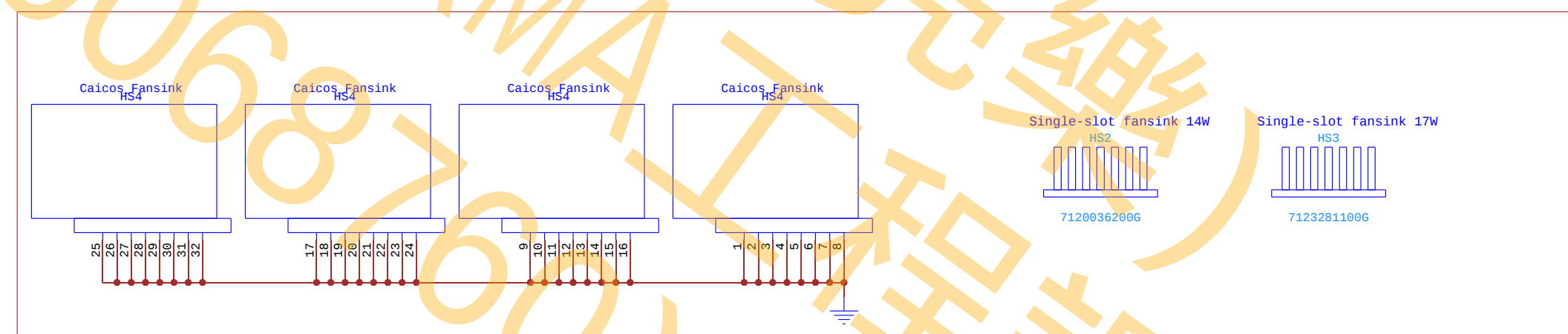
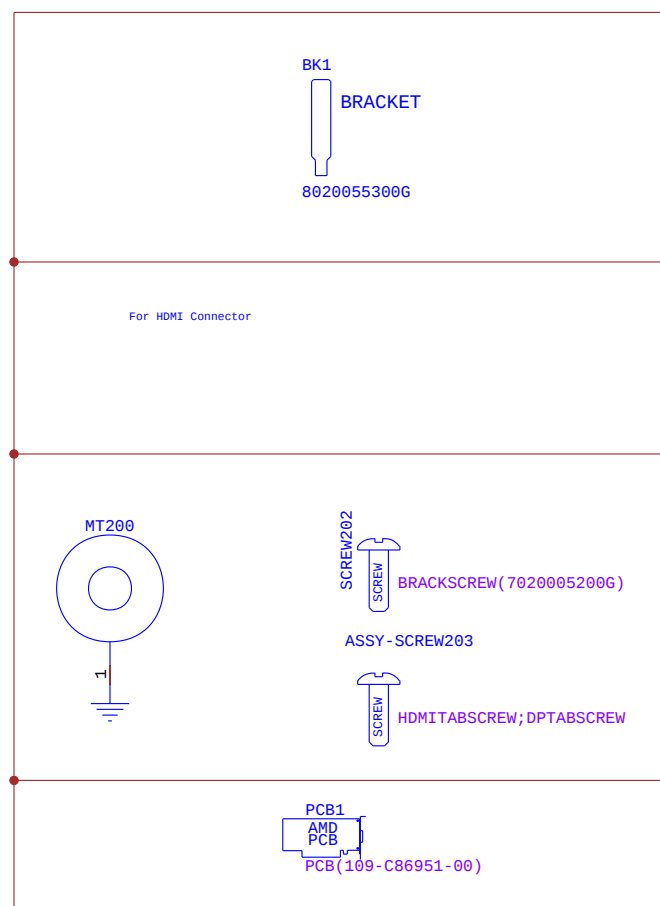
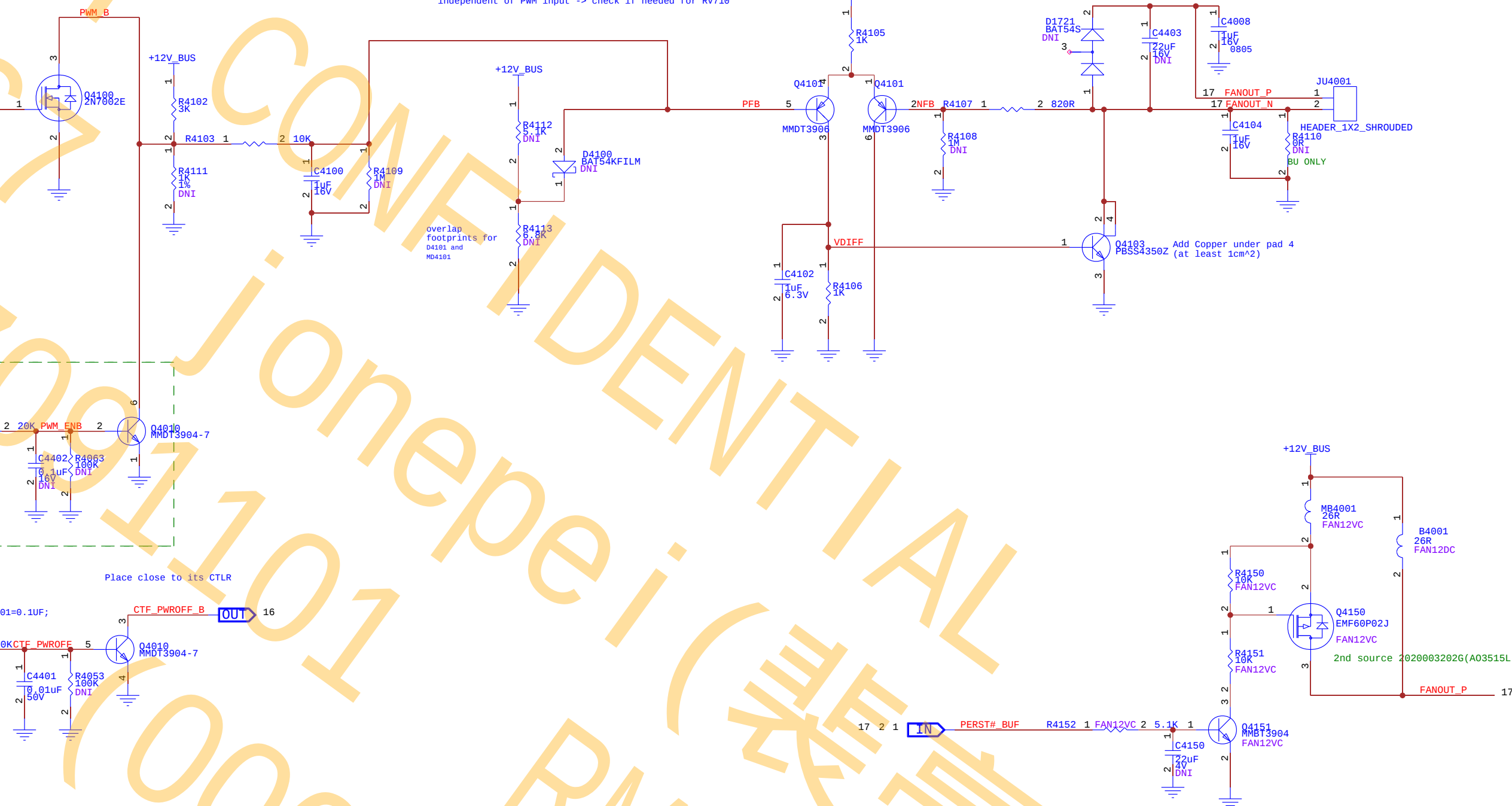
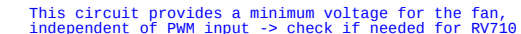
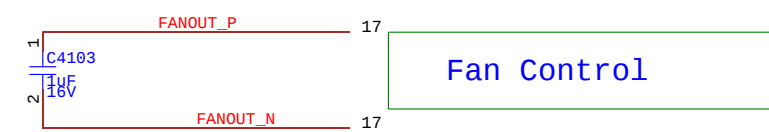
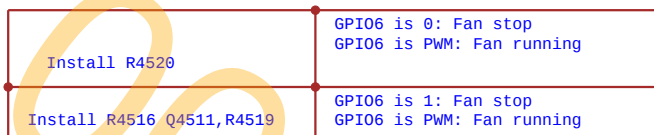
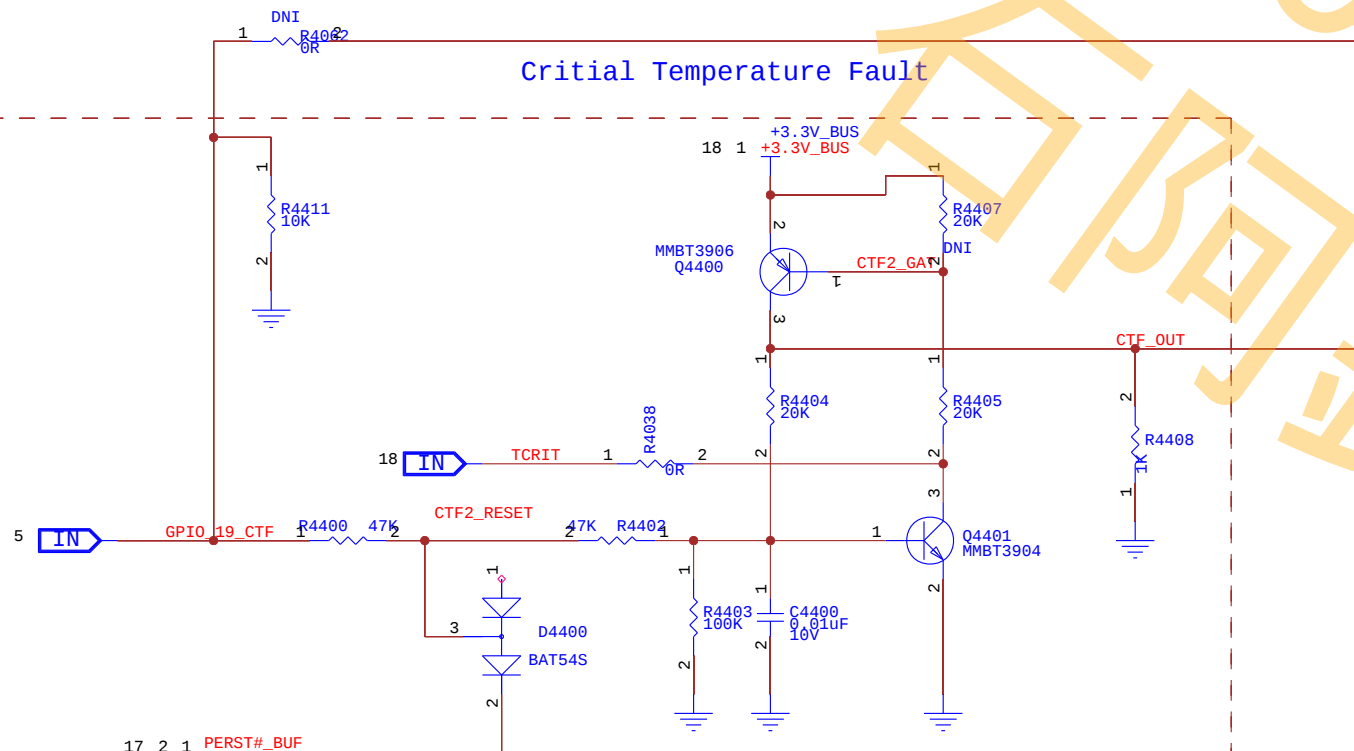
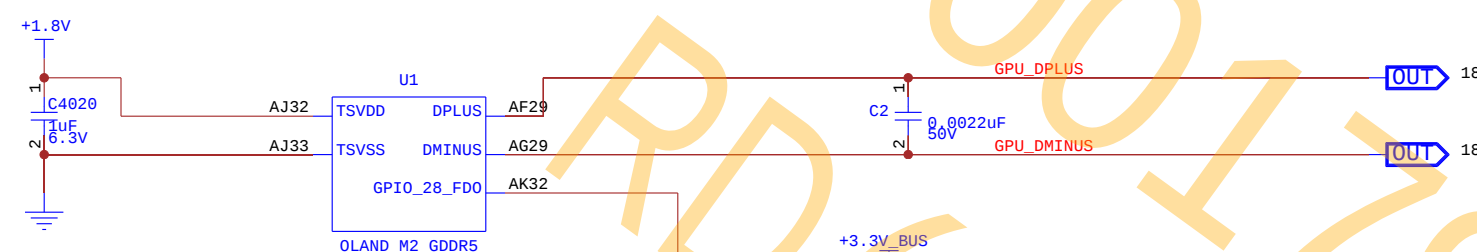
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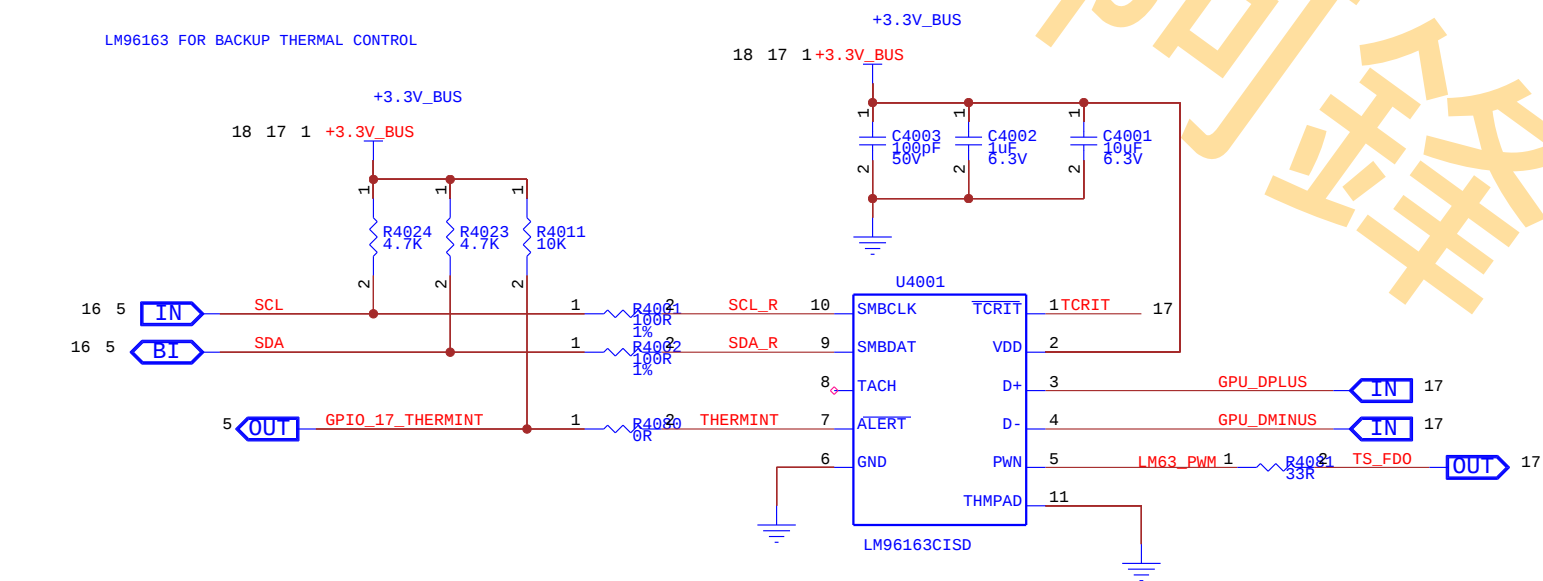
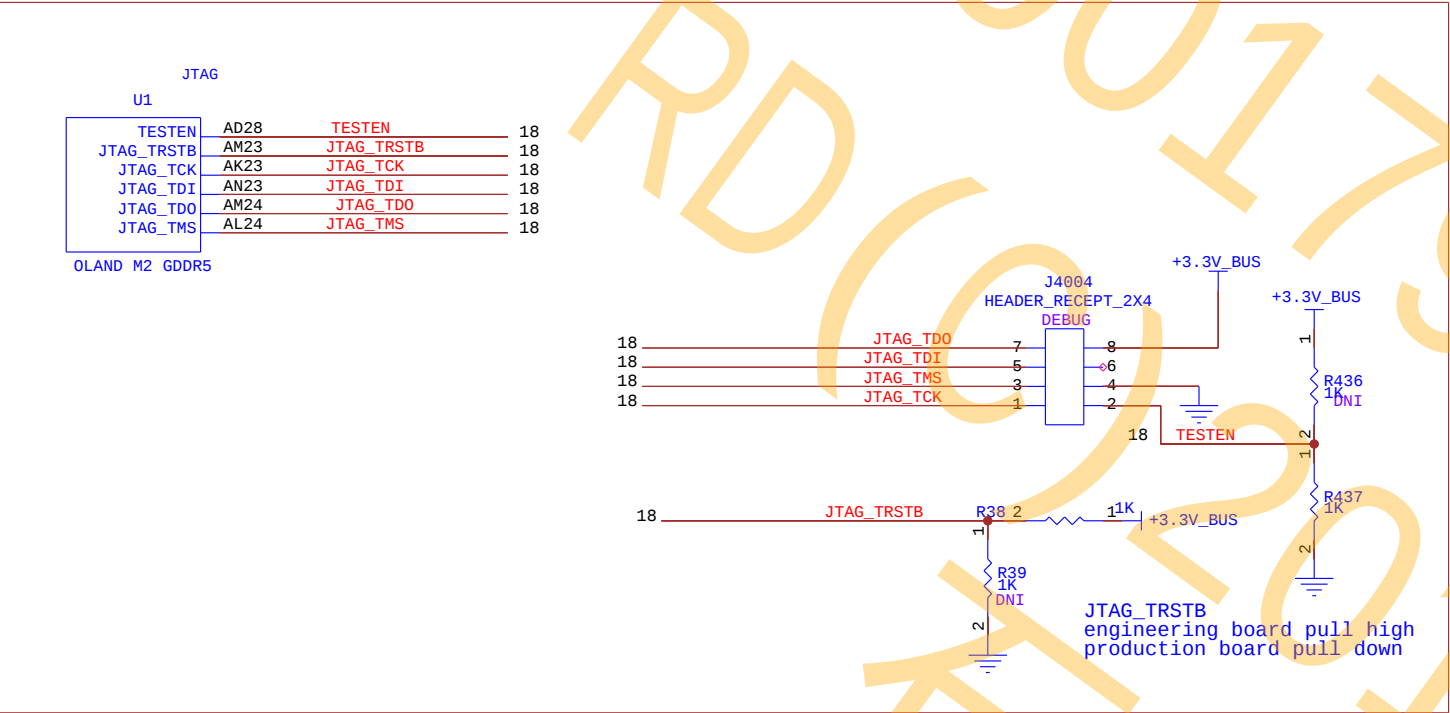
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(19) Debug Circuits



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DATE: Fri Oct 28 17:09:42 2016	REV: 1.0	TITLE	
SHEET NUMBER: 18 OF 21			
DOCUMENT NUMBER: 105_CXX00_00A			

