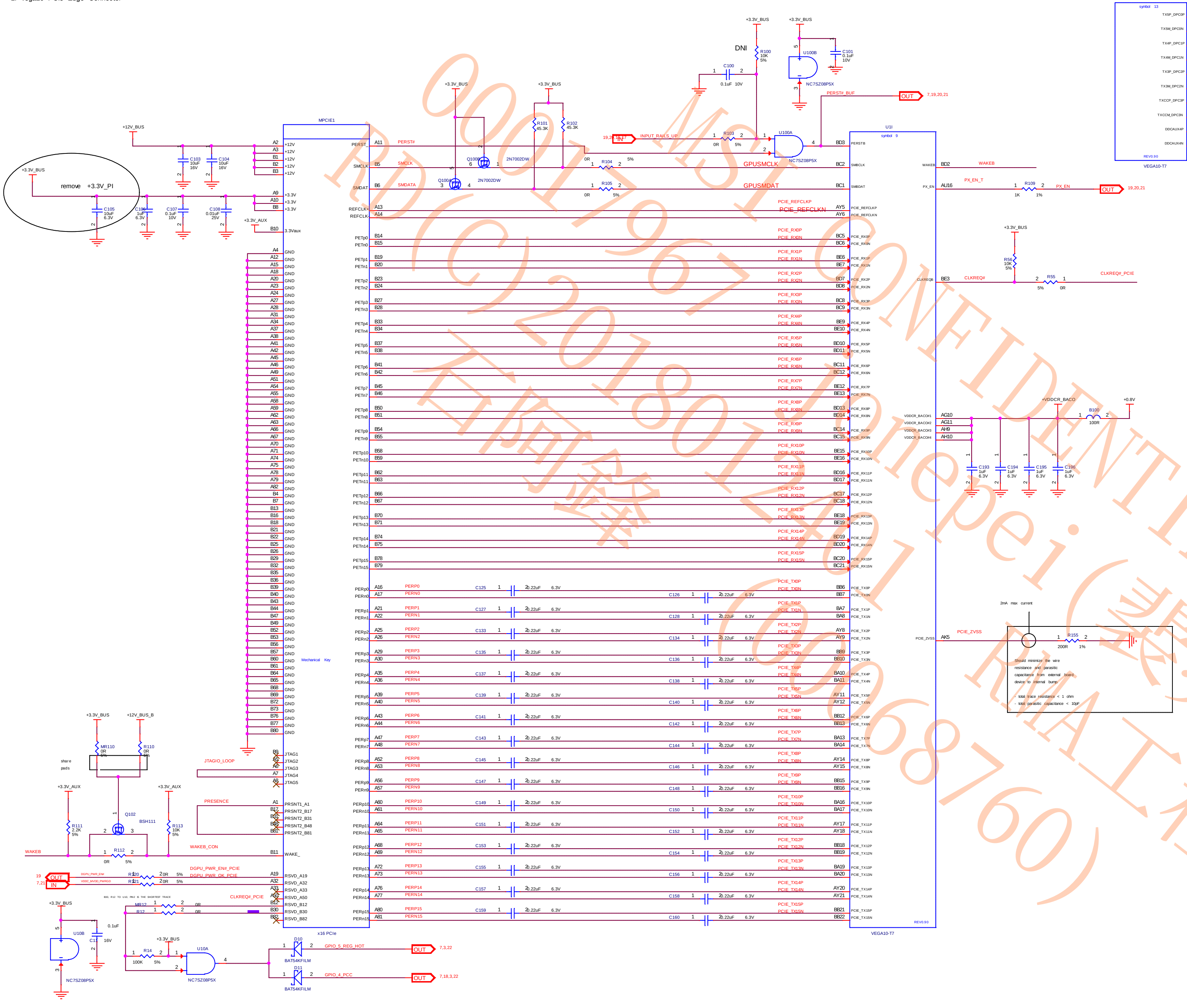
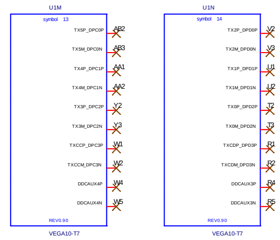
1. Vega10 PCIe Edge Connector





SYMBOL LEGEND

DNI	DO NOT INSTALL
b or #	ACTIVE LOW
BUD	BRING UP ONLY
(symbol)	DIGITAL GROUND
(symbol)	ANALOG GROUND

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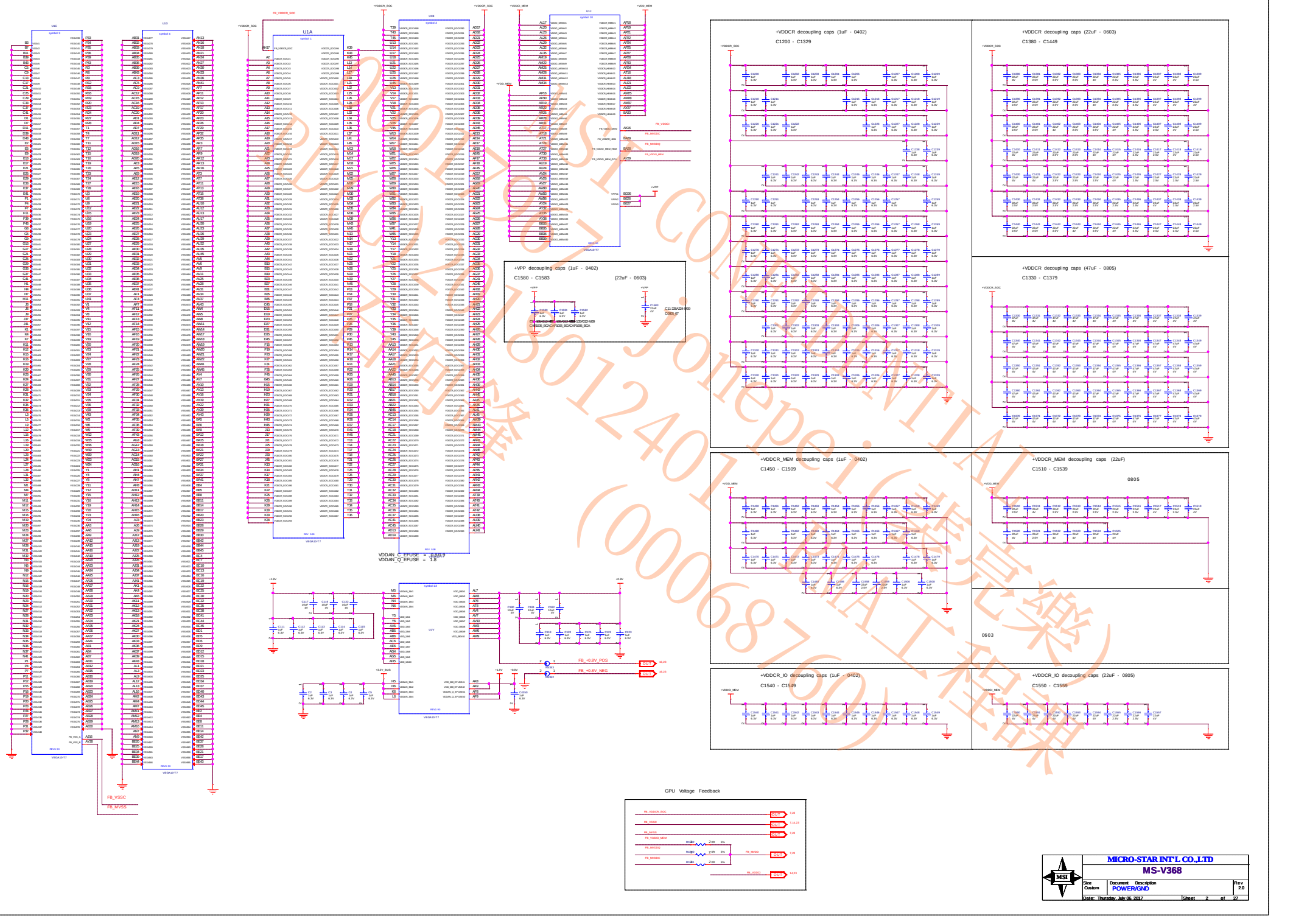
+VDDCR decoupling caps (1uF - 0402)
C1200 - C1329
+VDDCR decoupling caps (22uF - 0603)
C1380 - C1449
+VDDCR decoupling caps (47uF - 0805)
C1330 - C1379
+VPP decoupling caps (1uF - 0402)
C1580 - C1583
(22uF - 0603)
+VDDCR_MEM decoupling caps (1uF - 0402)
C1450 - C1509
+VDDCR_MEM decoupling caps (22uF)
C1510 - C1539
0805
0603
+VDDCR_IO decoupling caps (1uF - 0402)
C1540 - C1549
+VDDCR_IO decoupling caps (22uF - 0805)
C1550 - C1559
GPU Voltage Feedback
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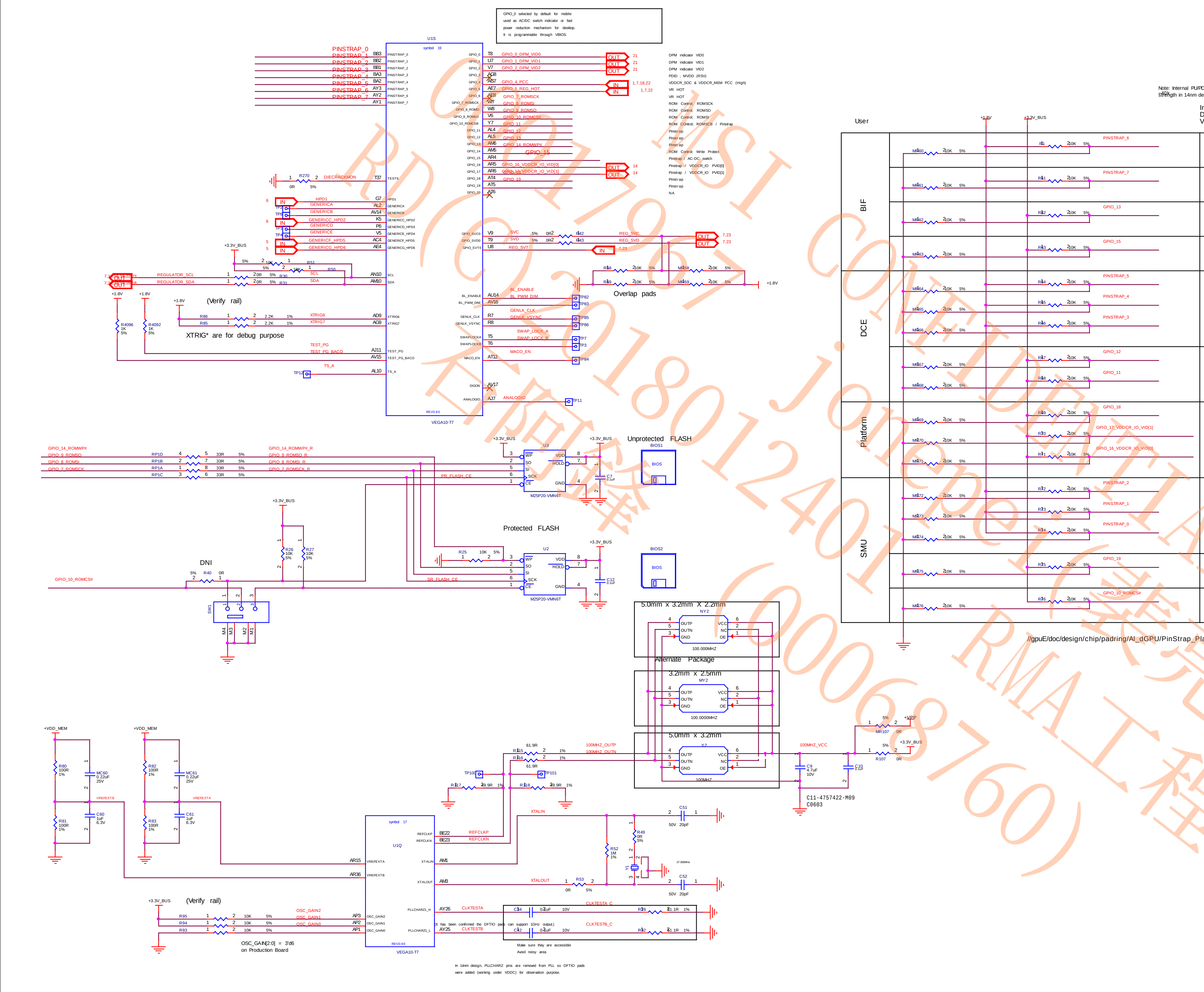

Note: Internal PU/PD at GPIO pad is ~40k strength in 14nm design spec

User		Internal Default Value	Definition
BIF		0	STRAP_BIF_GEN3_DIS_A 0: PCIe GEN 3 supported 1: PCIe GEN 3 not supported
		0	PINSTRAP_BIF_CLK_PM_EN 0: CLKREQ# power management capability is disabled 1: CLKREQ# power management capability is enabled
		0	PINSTRAP_BIF_LC_TX_SWING
		0	PINSTRAP_BIF_VGA_DIS 0: VGA controller capacity enabled 1: The device won't be recognised as the system's VGA controller
DCE		0 0 0	PINSTRAP_AUD_PORT_CONN[2:0] Number of audio-capable display outputs 0: All endpoints connected 1: 6 endpoints connected 2: 5 endpoints connected 3: 4 endpoints connected 4: 3 endpoints connected 5: 2 endpoints connected 6: 1 endpoint connected 7: 0 endpoints connected
		0 0	PINSTRAP_AUD[1:0] 1: Audio for DisplayPort only 2: Audio for DisplayPort and HDMI if dongle is detected 3: Audio for DisplayPort and native HDMI
Platform		0 0 0	PINSTRAP_BOARD_CONFIG[2:0] TBD
SMU		1 0 1	PINSTRAP_ROM_CONFIG[2:0] 100 - 512KBIT (ST) M25P05A 101 - 1MBIT (ST) (M25P10A) 101 - 2MBIT (ST) M25P20 101 - 4MBIT (ST) M25P40 101 - 8MBIT (ST) M25P80 100 - 512KBIT (CHINGIS) PM25LV512 101 - 1MBIT (CHINGIS) PM25LV010
		0	PINSTRAP_SMBUS_ADDR 0: 0x41h 1: 0x40h
		1	PINSTRAP_BIOS_ROM_EN 0: Disable the external BIOS ROM device 1: Enable the external BIOS ROM device

//gpuE/doc/design/chip/padring/AI_dGPU/PinStrap_Plan.pptx

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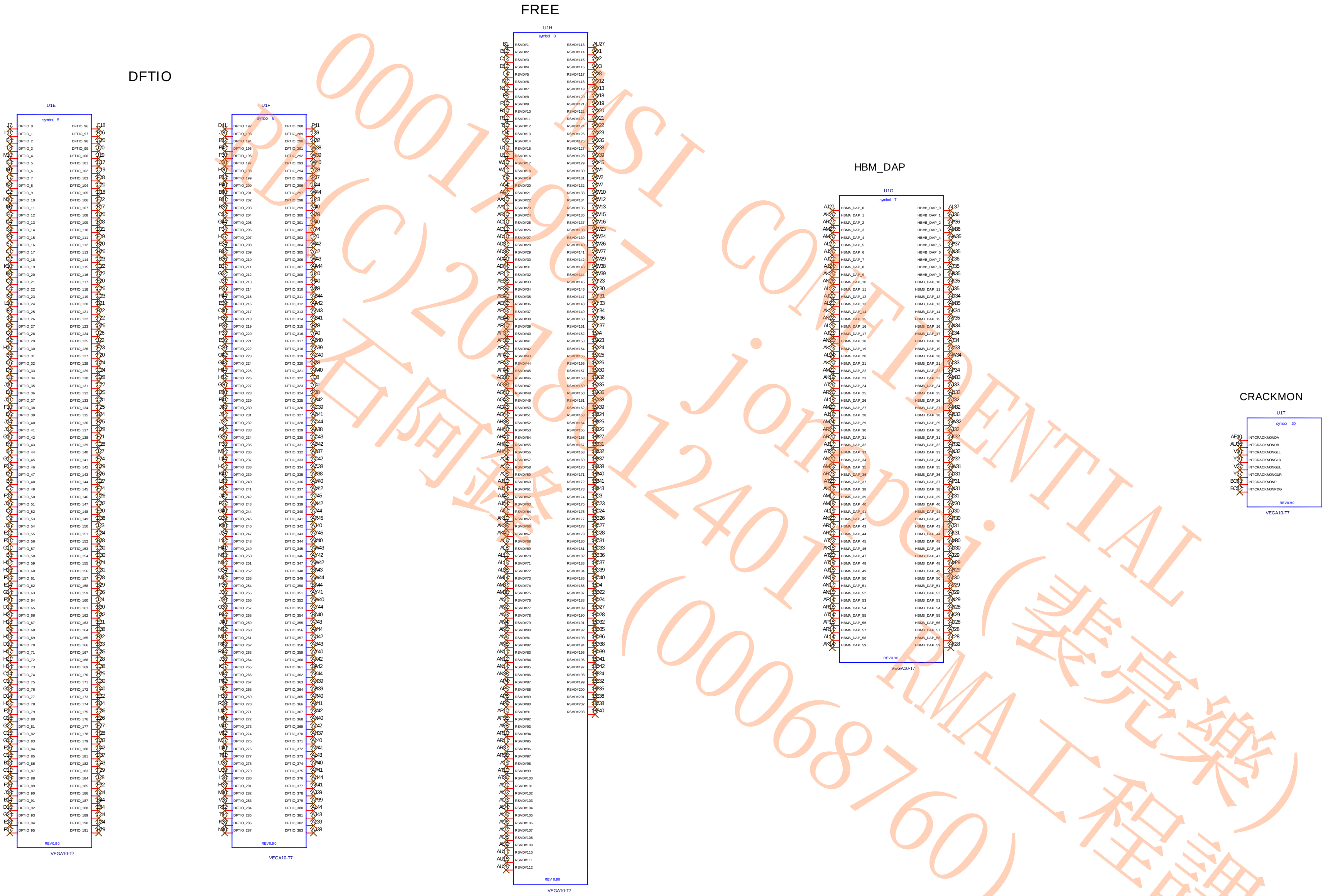

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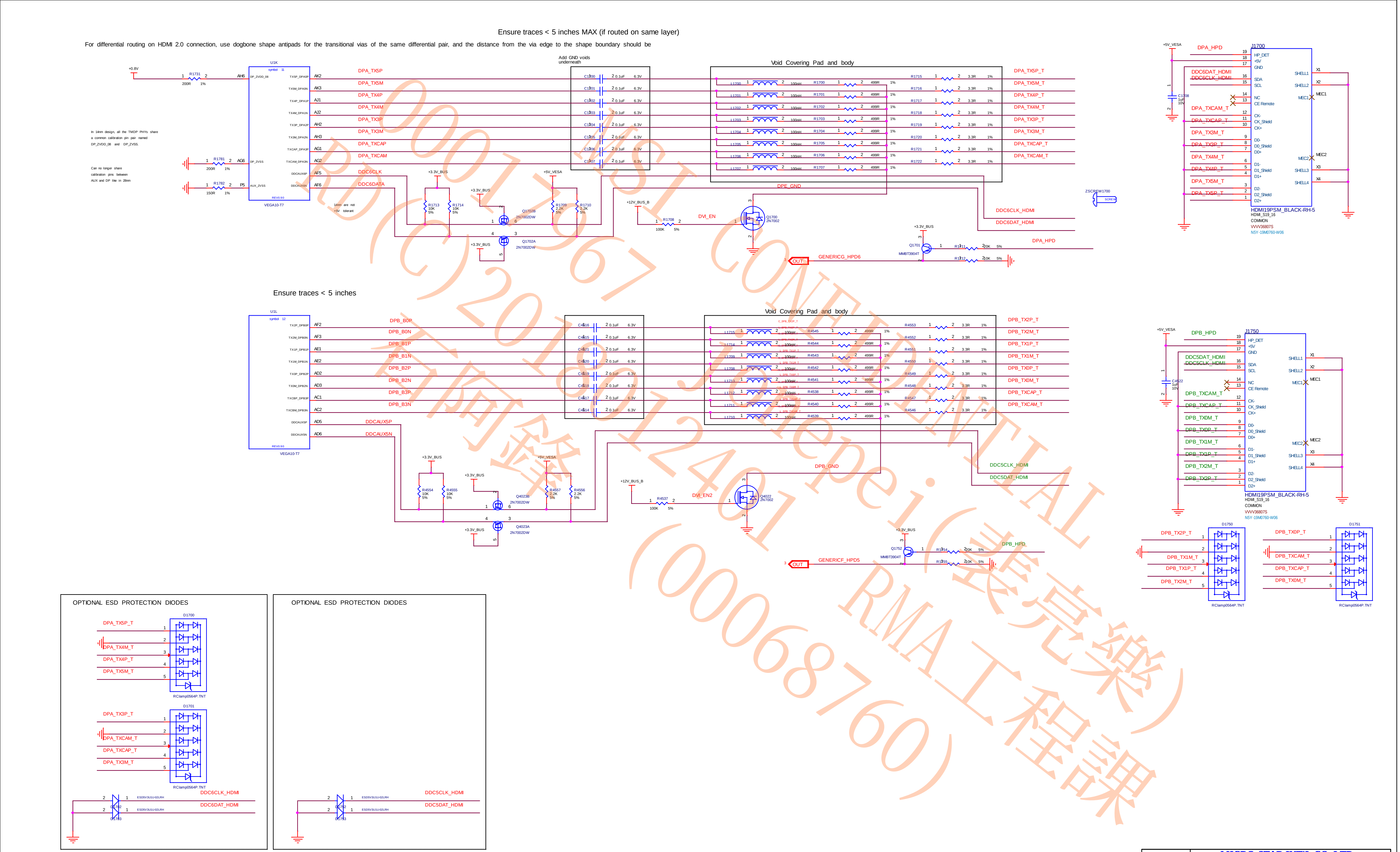

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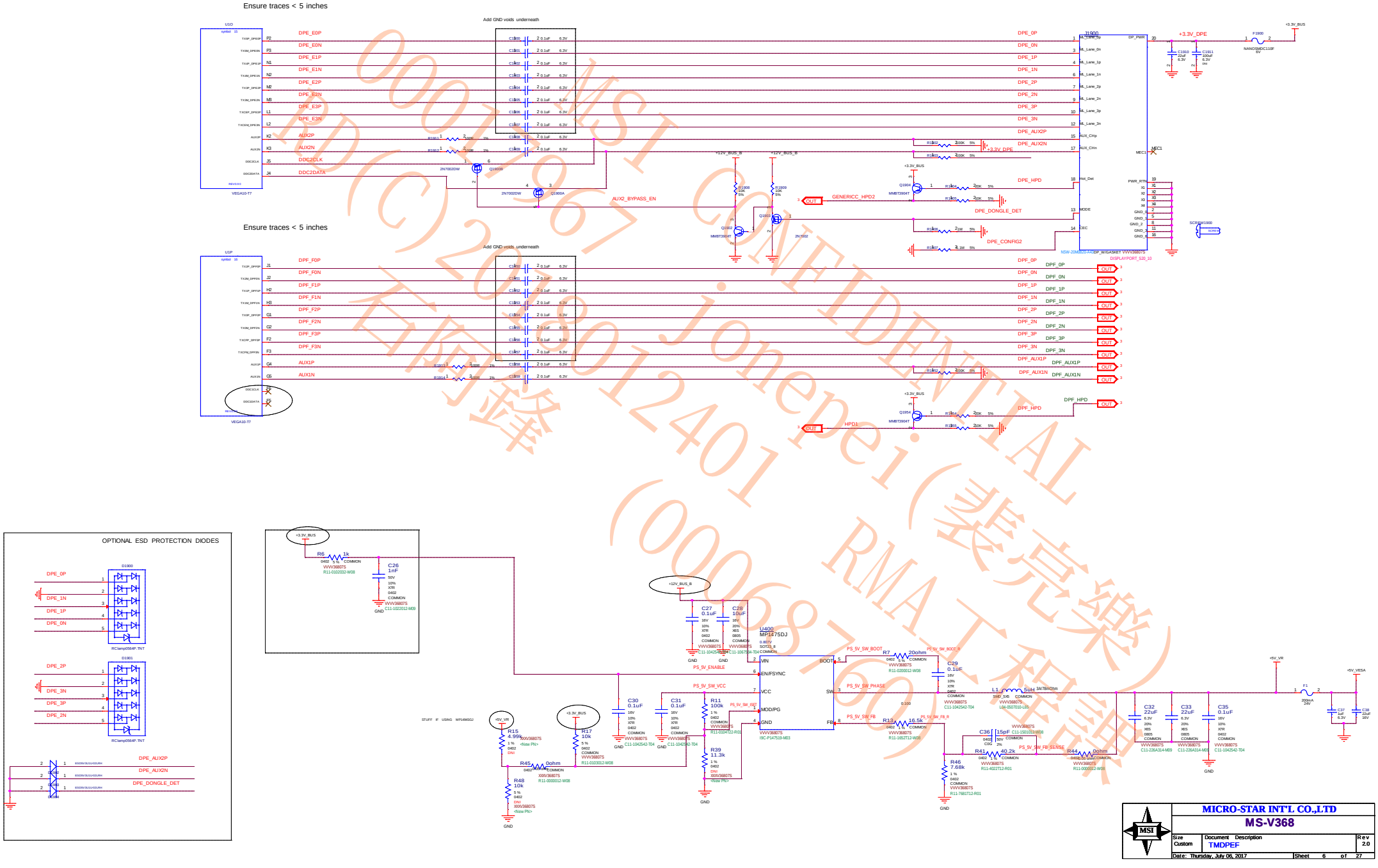
Ensure traces < 5 inches
Add GND voids underneath
DPE_E0P
DPE_E0N
DPE_E1P
DPE_E1N
DPE_E2P
DPE_E2N
DPE_E3P
DPE_E3N
AUX2P
AUX2N
DDC2CLK
DDC2DATA
AUX2_BYPASS_EN
GENERICC_HPD2
DPE_DONGLE_DET
DPE_CONFIG2
DPE_HPD
+3.3V_DPE
+12V_BUS_B
Ensure traces < 5 inches
Add GND voids underneath
DPF_F0P
DPF_F0N
DPF_F1P
DPF_F1N
DPF_F2P
DPF_F2N
DPF_F3P
DPF_F3N
AUX1P
AUX1N
HPD1
OPTIONAL ESD PROTECTION DIODES
DPE_0P
DPE_1N
DPE_1P
DPE_0N
DPE_2P
DPE_3N
DPE_3P
DPE_2N
DPE_AUX2P
DPE_AUX2N
DPE_DONGLE_DET
U400
MP1475DJ
PS_5V_ENABLE
PS_5V_SW_VCC
PS_5V_SW_BST
PS_5V_SW_BOOT
PS_5V_SW_PHASE
PS_5V_SW_FB
PS_5V_SW_FB_SENSE
+5V_VR
+5V_VESA
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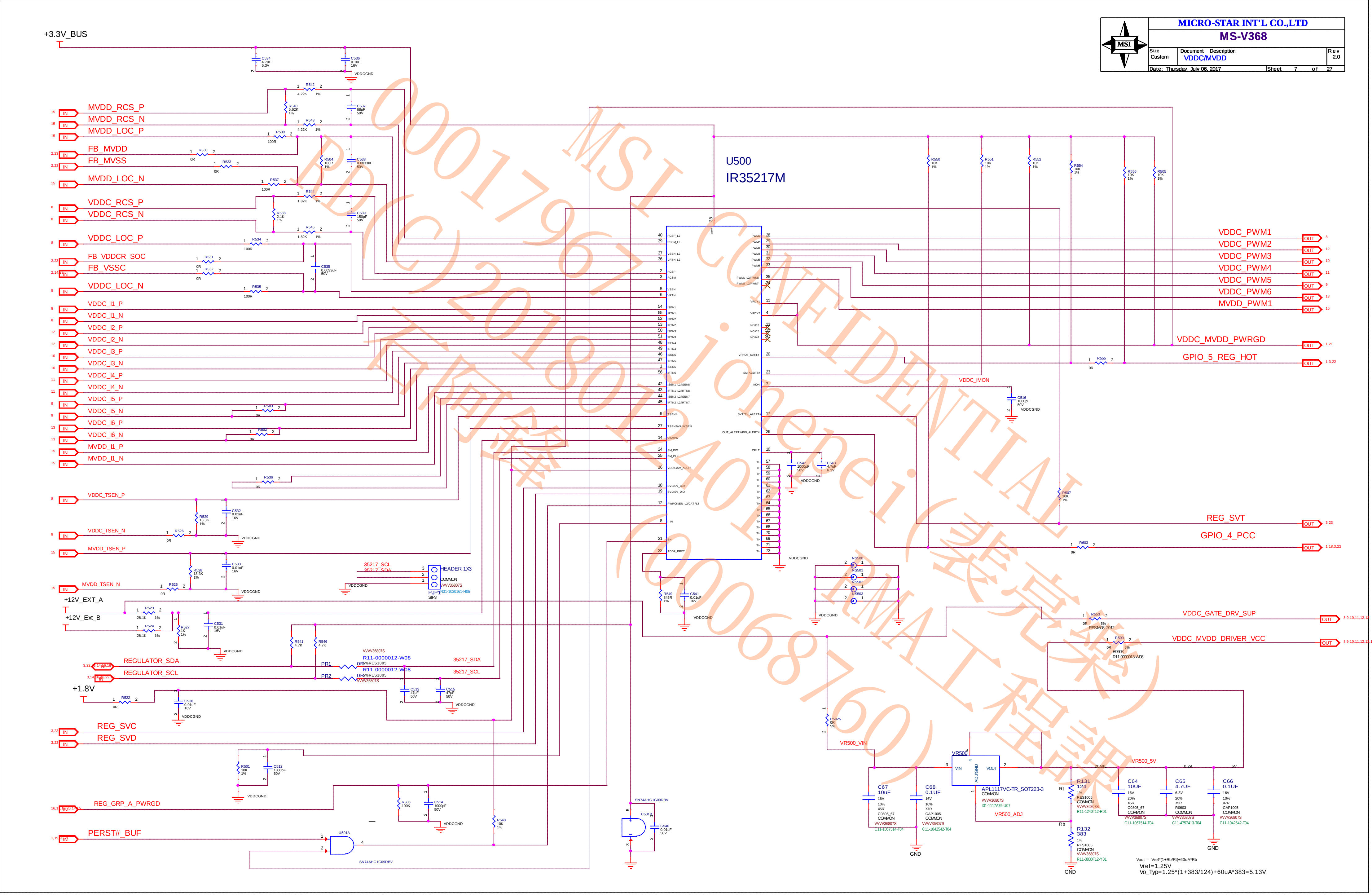

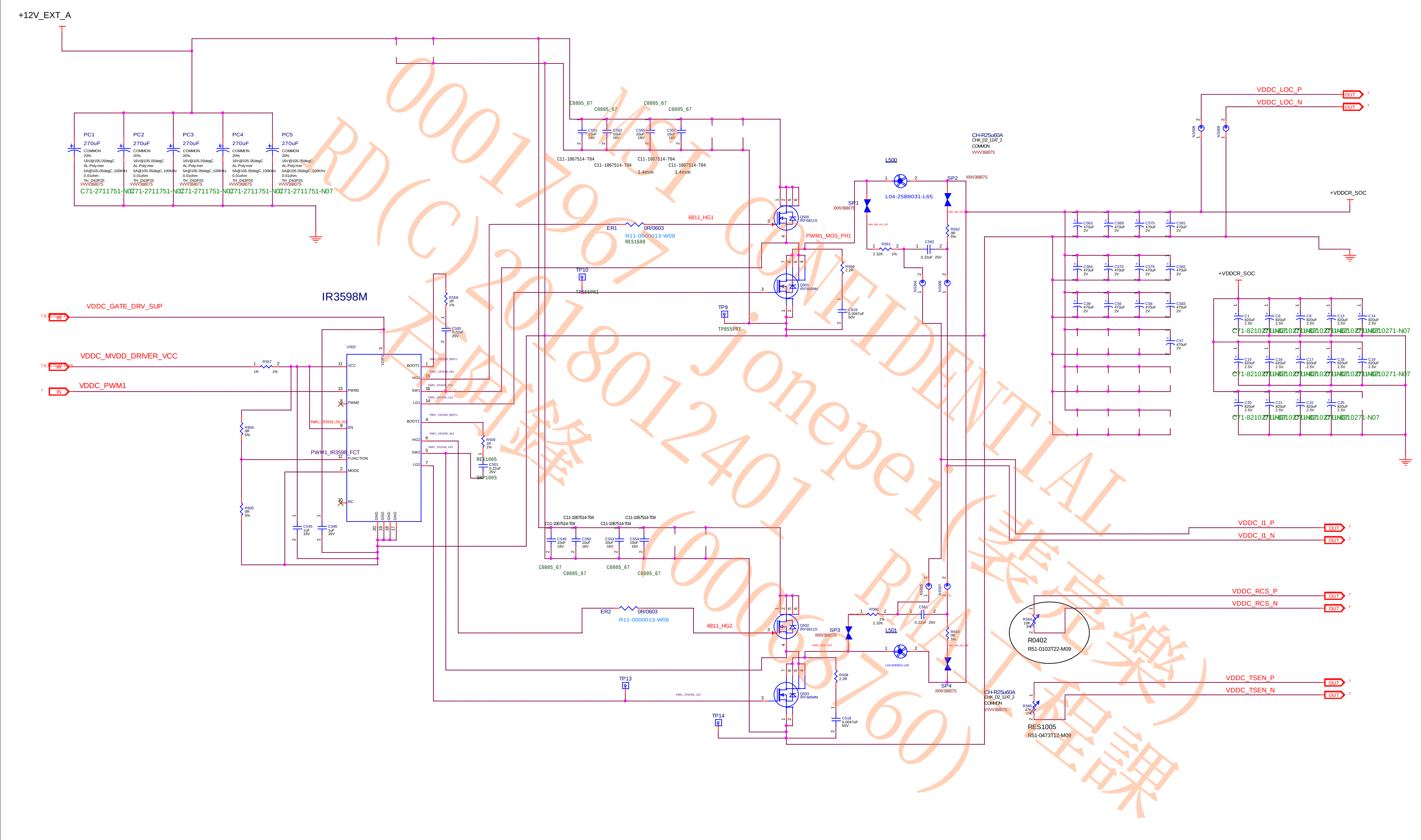

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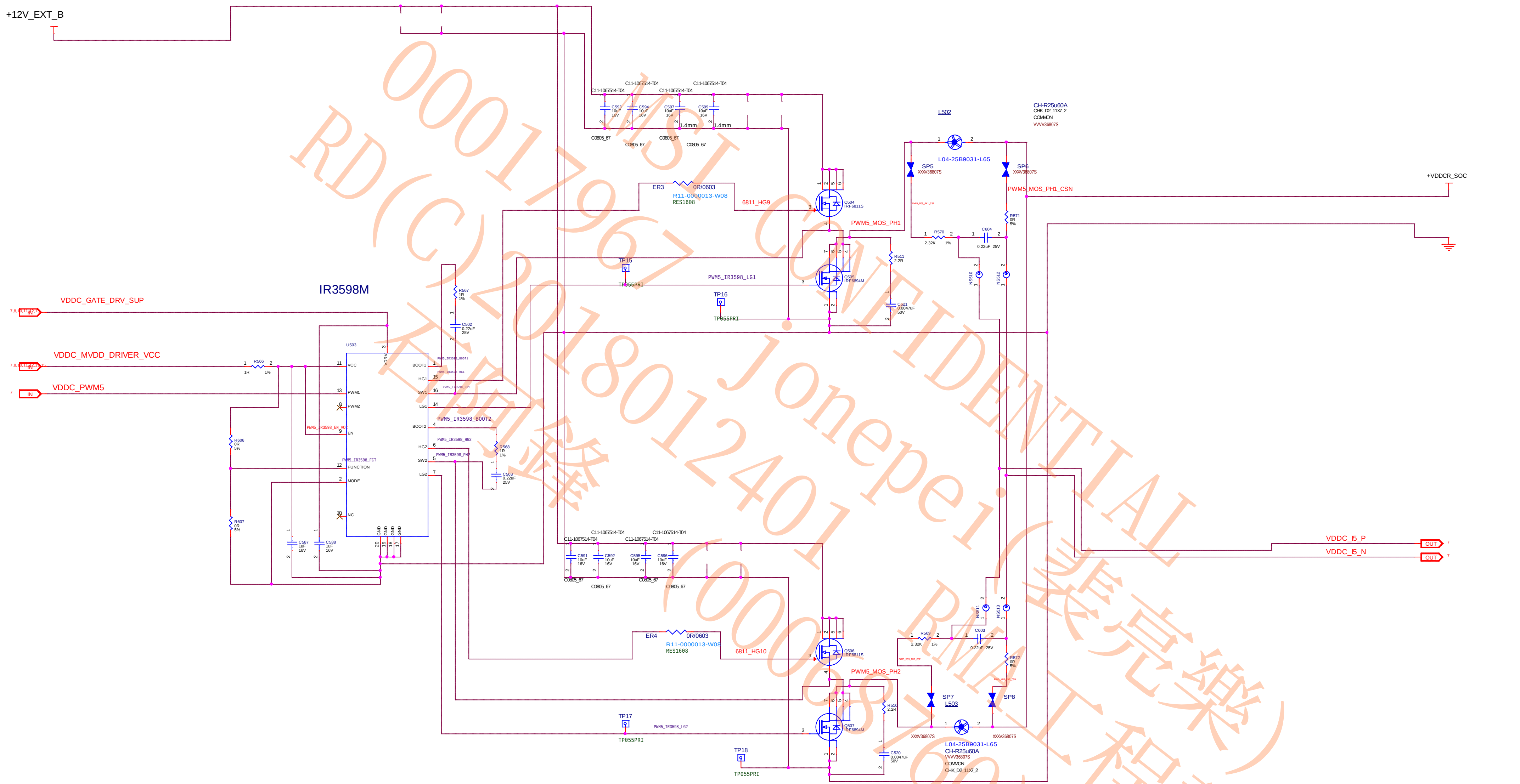

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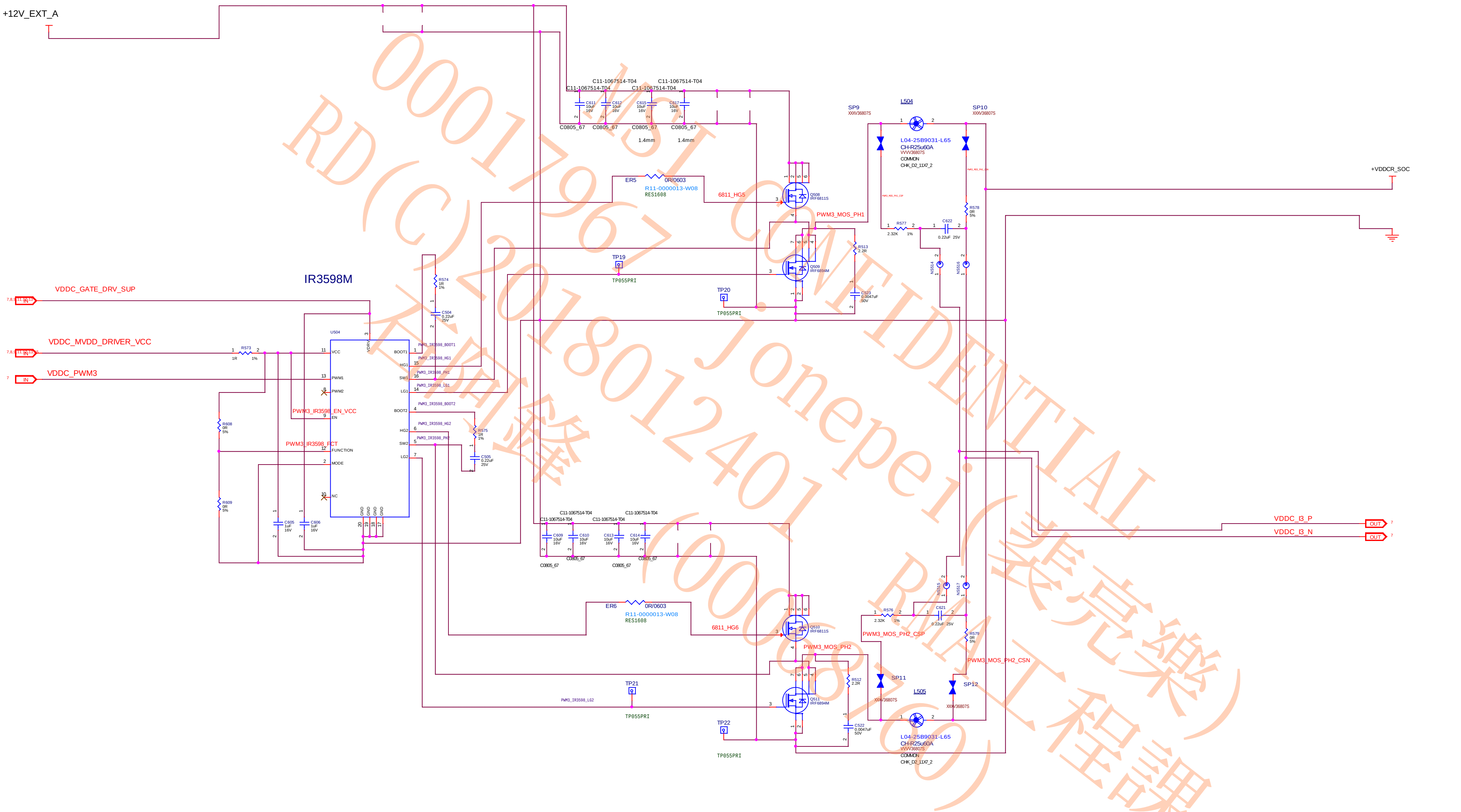

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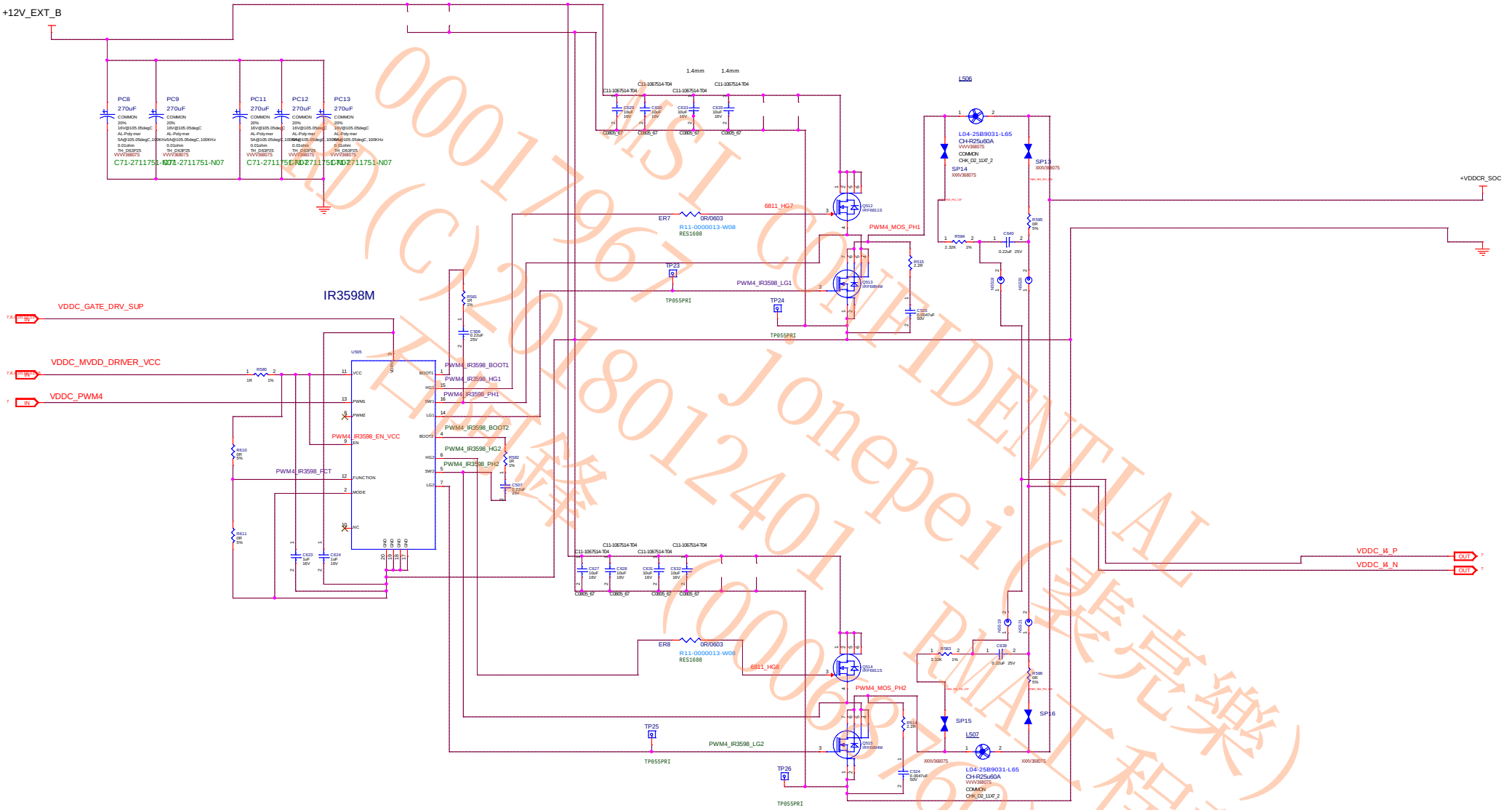
+12V_EXT_B
PC8 270uF
PC9 270uF
PC11 270uF
PC12 270uF
PC13 270uF
C71-2711751-N07
IR3598M
VDDC_GATE_DRV_SUP
VDDC_MVDD_DRIVER_VCC
VDDC_PWM4
PWM4_IR3598_EN_VCC
PWM4_IR3598_FCT
PWM4_IR3598_BOOT1
PWM4_IR3598_HG1
PWM4_IR3598_PH1
PWM4_IR3598_BOOT2
PWM4_IR3598_HG2
PWM4_IR3598_PH2
PWM4_IR3598_LG1
PWM4_IR3598_LG2
PWM4_MOS_PH1
PWM4_MOS_PH2
6811_HG7
6811_HG8
ER7
ER8
R11-0000013-W08
RES1608
L506
L507
L04-25B9031-L65
CH-R25u60A
+VDDCR_SOC
VDDC_I4_P
VDDC_I4_N
TP23
TP24
TP25
TP26
TP055PRI
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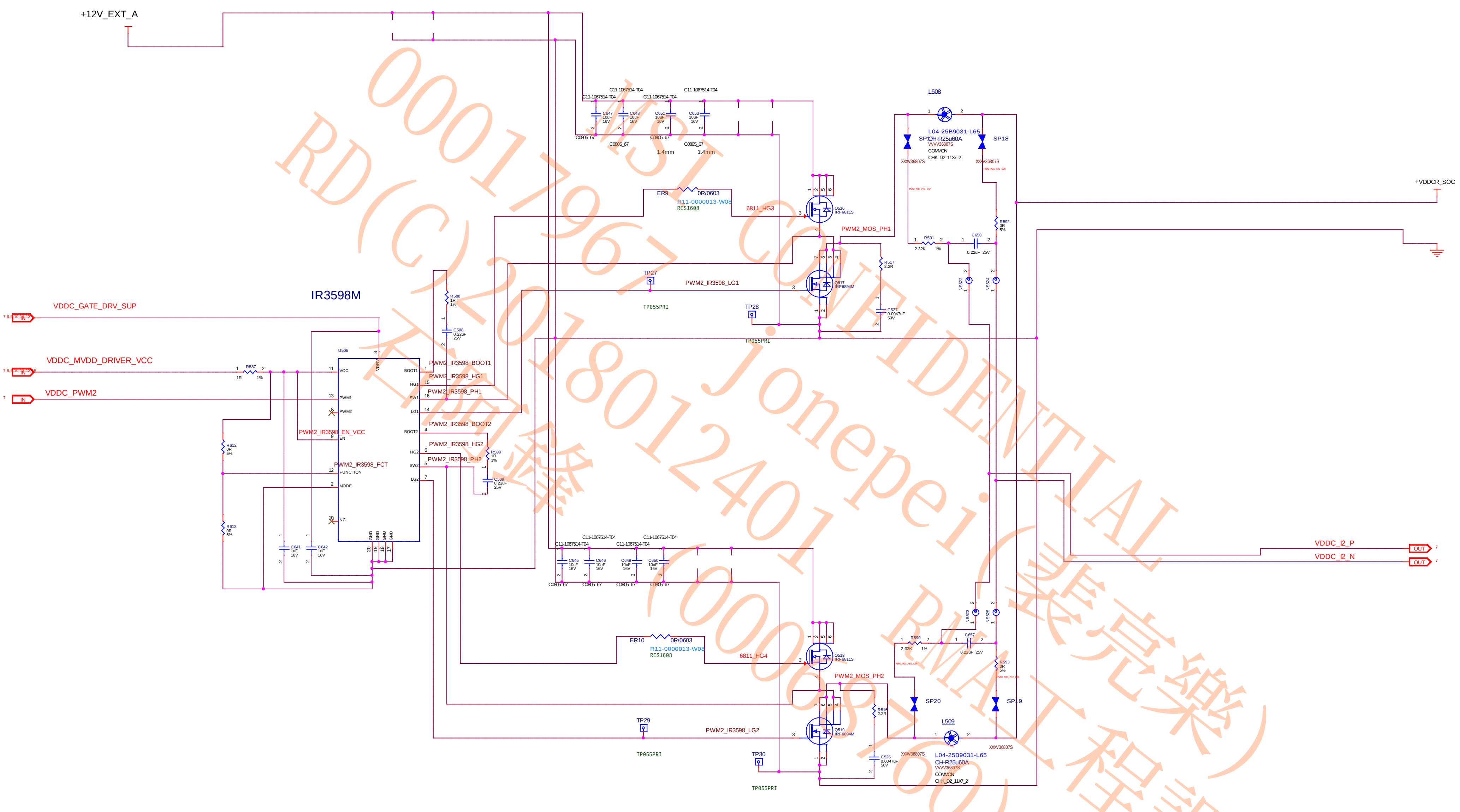

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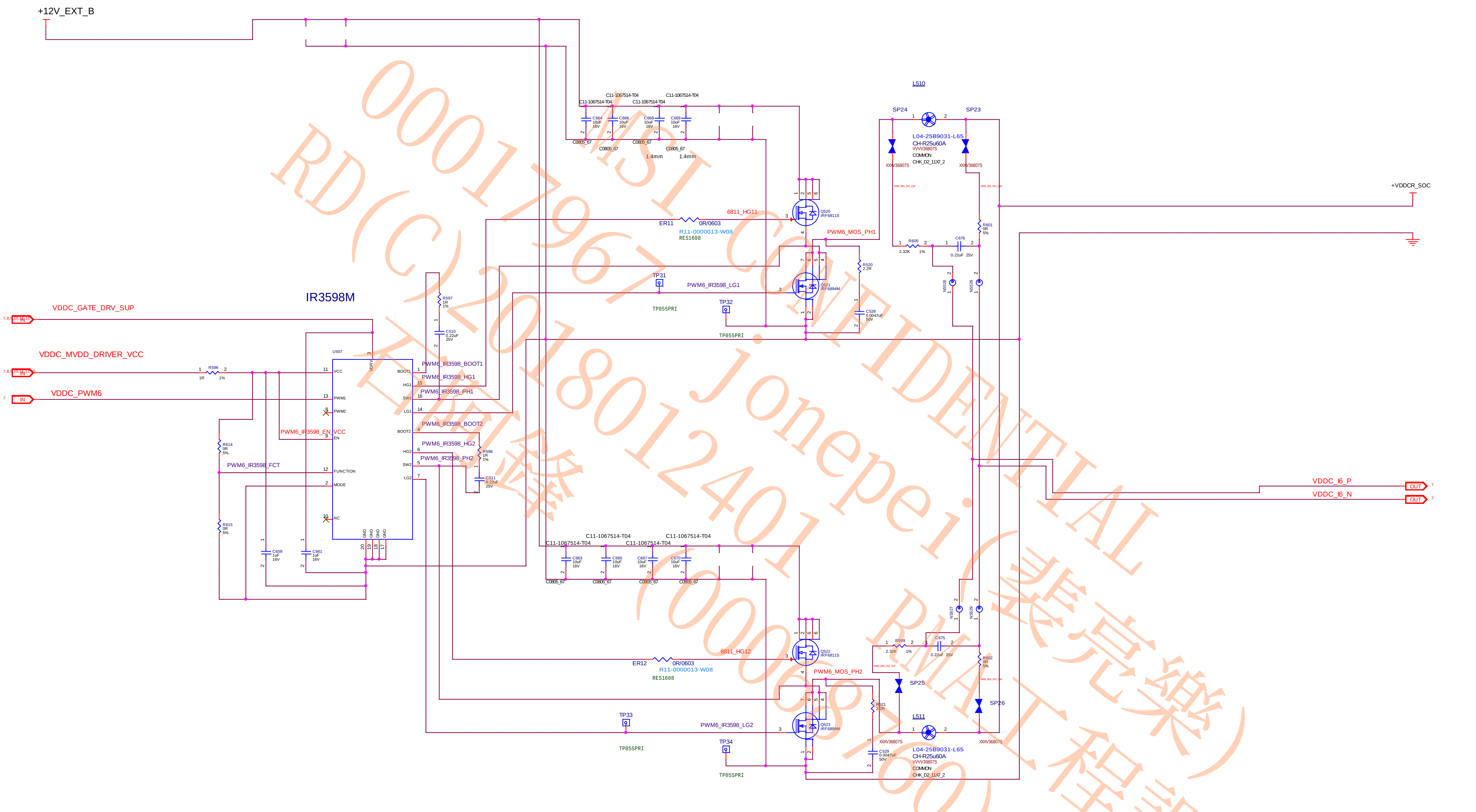

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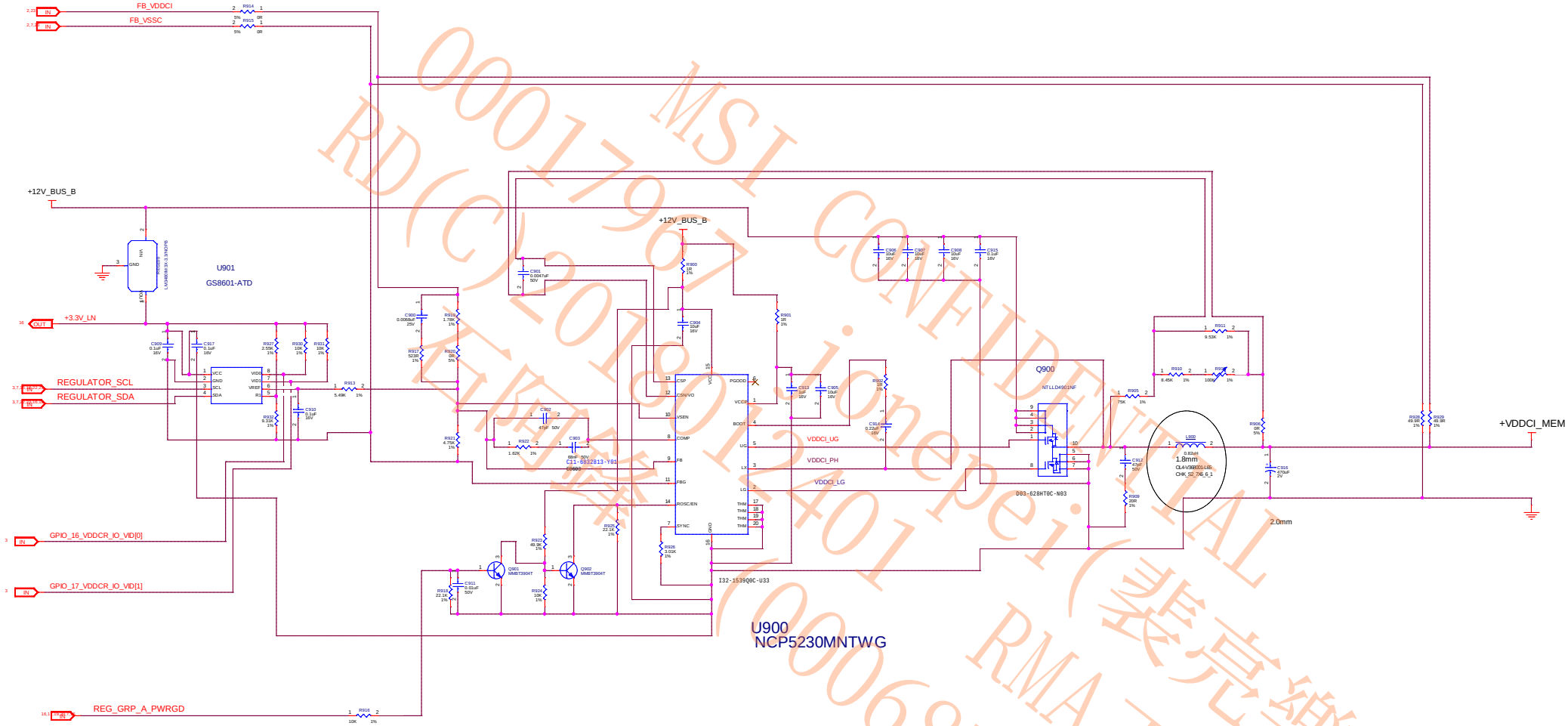

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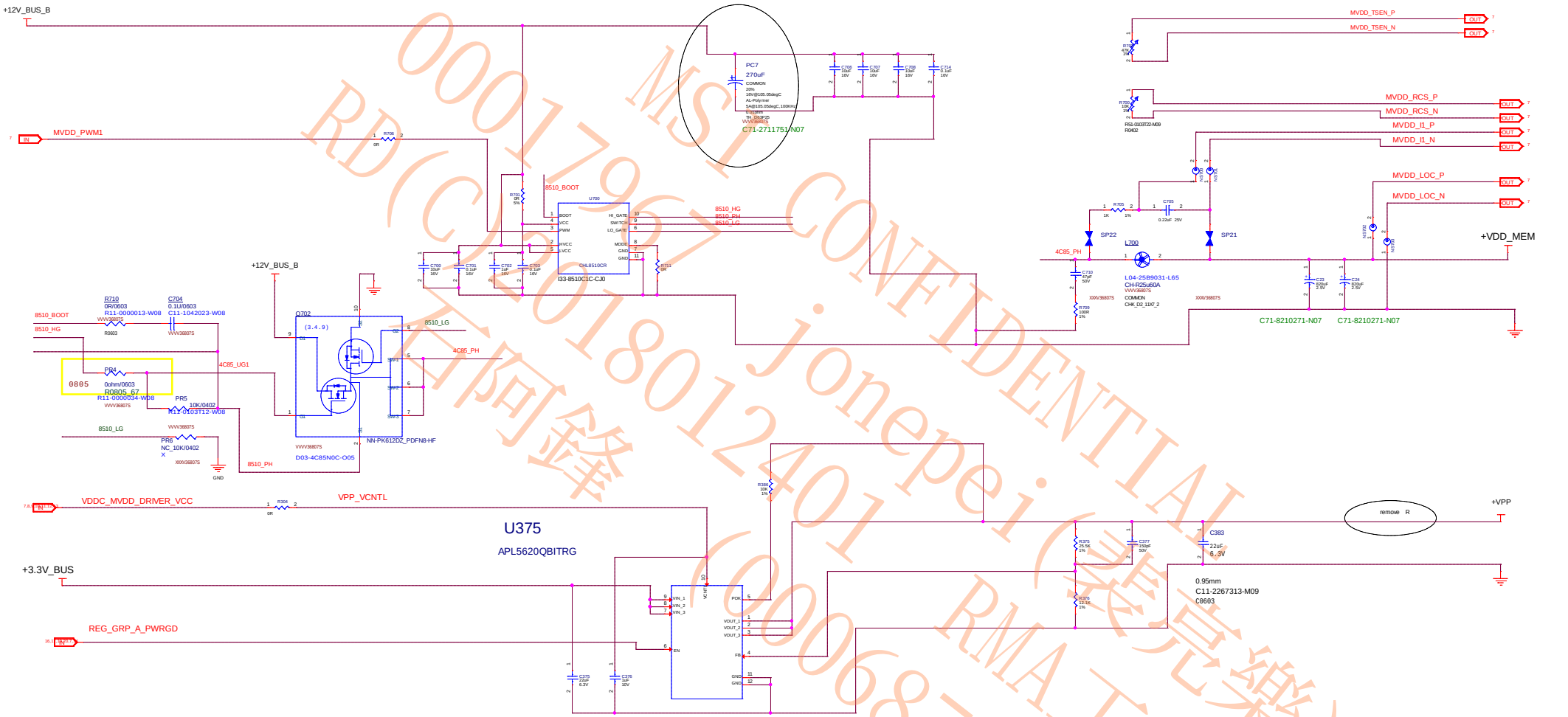

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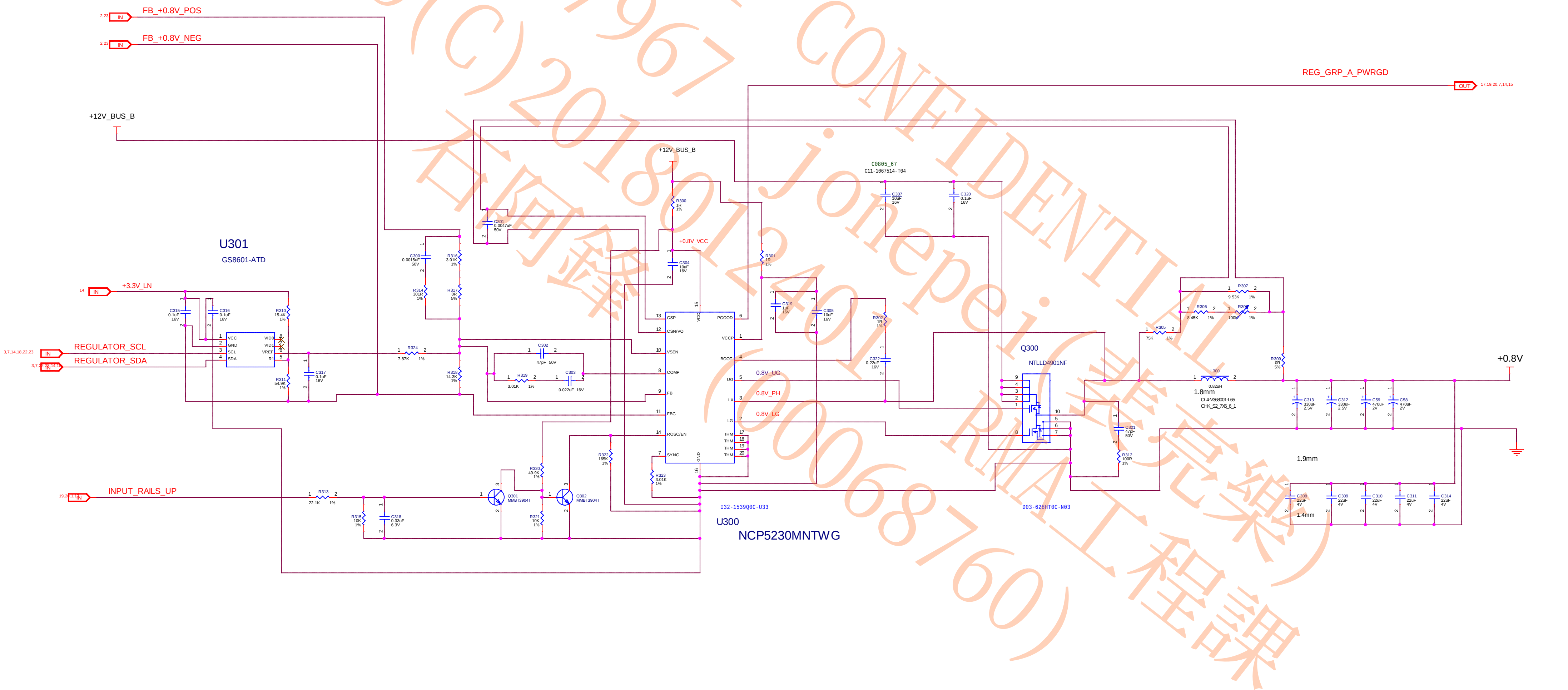

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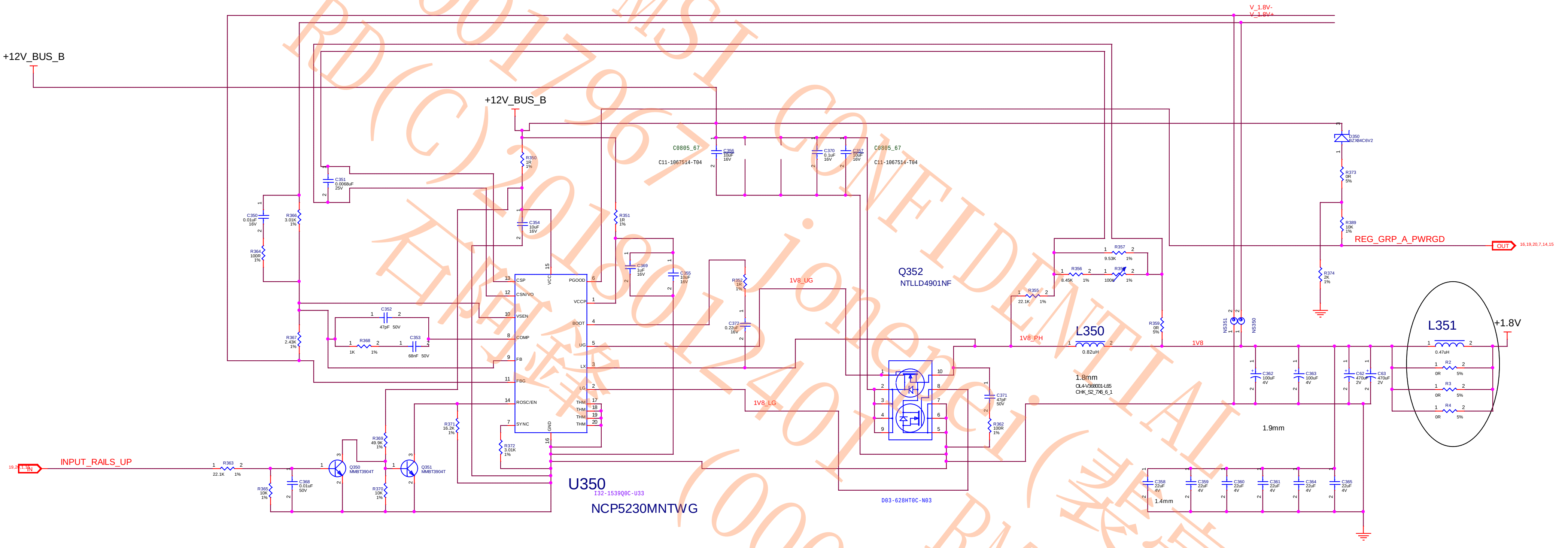

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remove PCC

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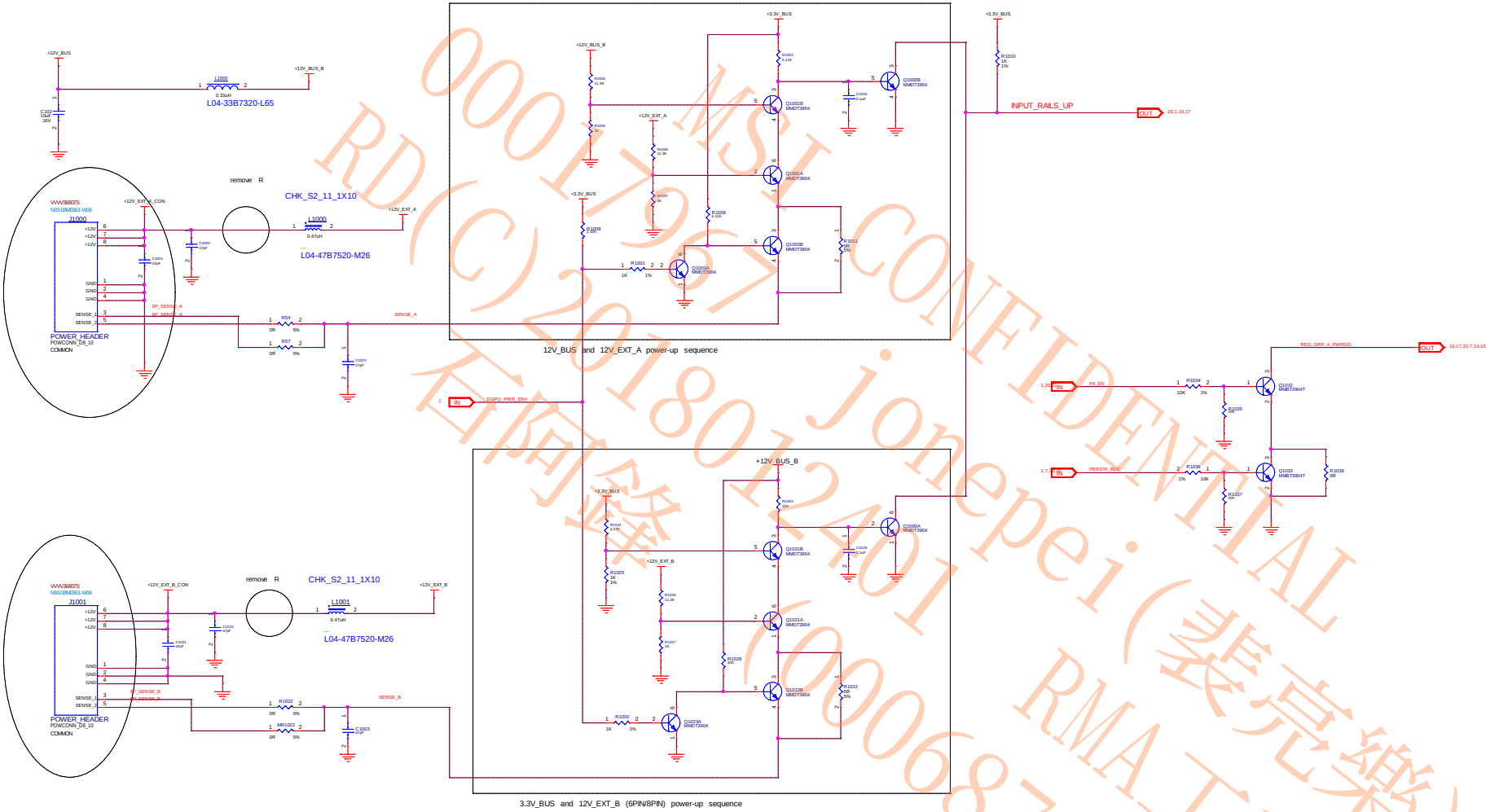

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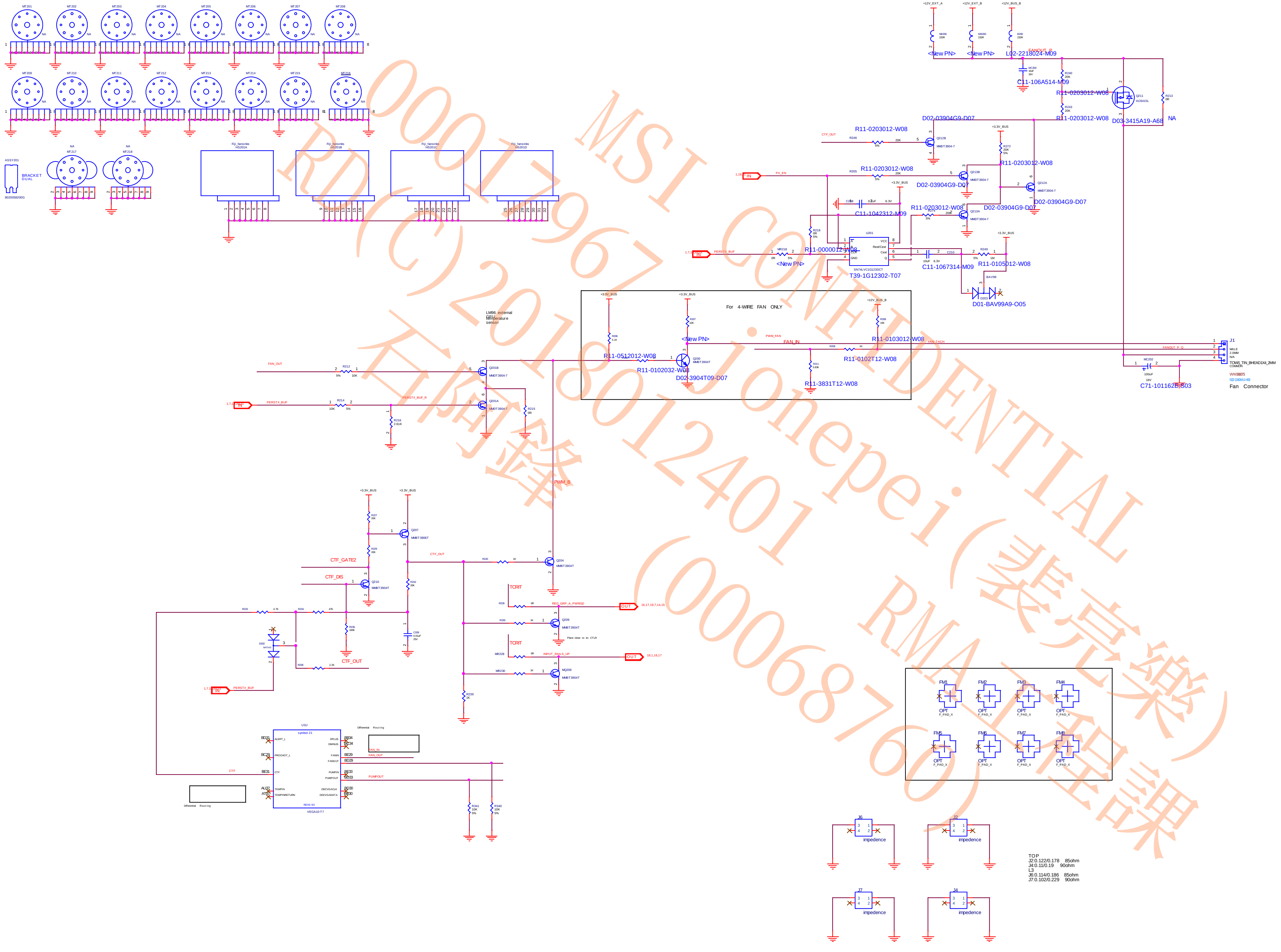

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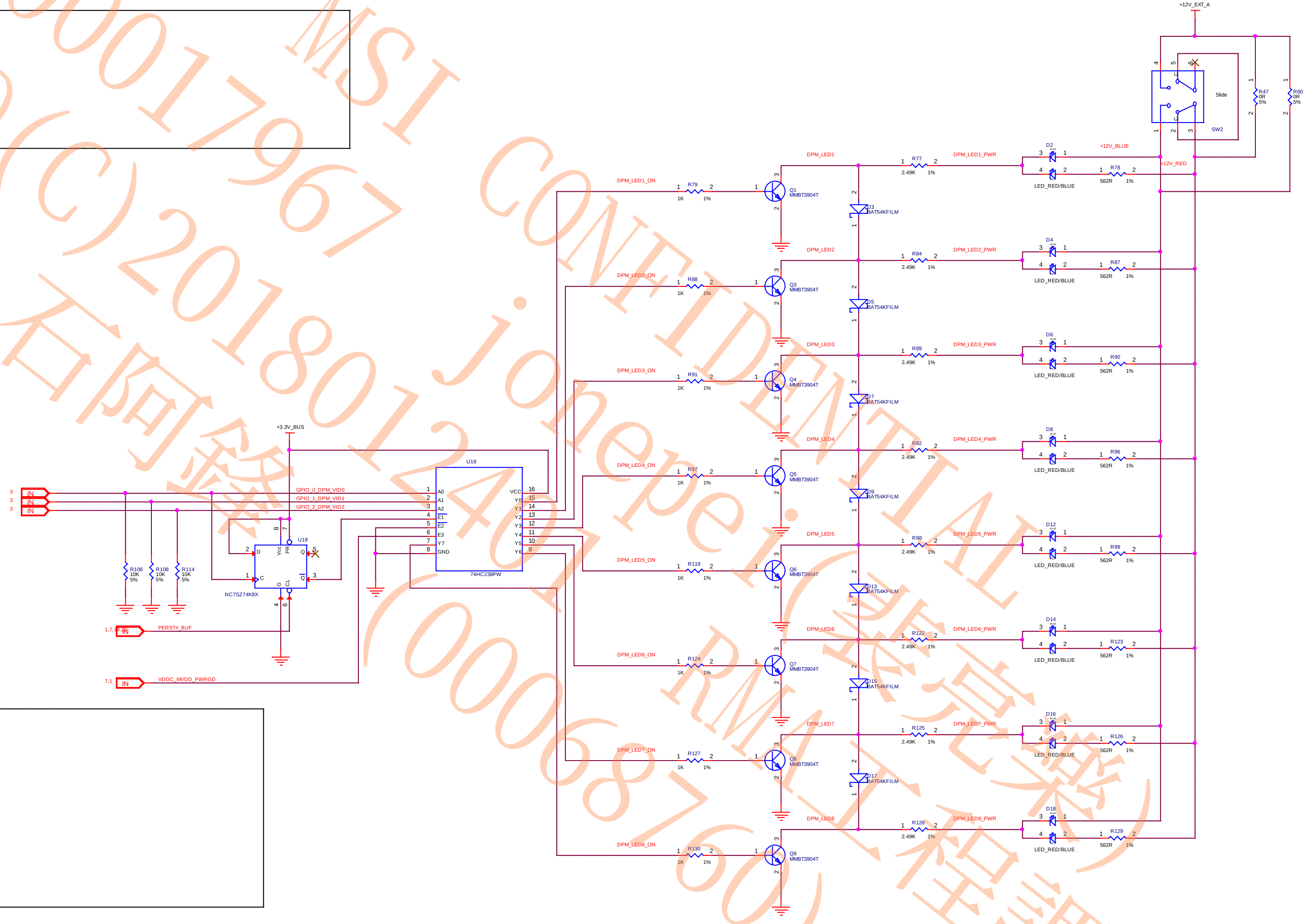
LED GREEN "ON" indicates BACO mode



RADEON Lightbar header

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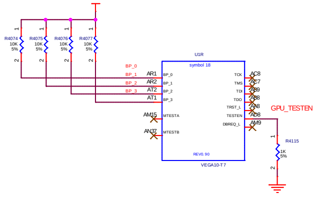

REMOVE

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Size: Custom	Document Description: PI GLUE	Rev: 2.0
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0	A	10/9/15	Initial schematic creation
	B	6/30/16	Many Changes on PI circuit , Minor Chnages on SMPS
	C	9/30/16	Many Changes on PI circuit , ASIC SYMBOL UPDATED FOR FLASH ROM INTERFACE , flash ROM SI/SO swapped , RP1 added
	D	11/29/16	Changes on PI circuit , 100MHz HCSL clock source replced (contact AMD for detailes)
	E	01/05/17	PI circuit removed , 200R added to DP AUX (6 resistors)
	-00	02/02/17	1.8V/VPP Kelvin resistors dual footprinted , DP AUX (6 resistors changed to 100R) , Changed R4033 to 360R 1206 and moved to 12V_AUX , SMBUS Address note swap , J4001 removed , R115/R116 changed to 61.9R , R205 added

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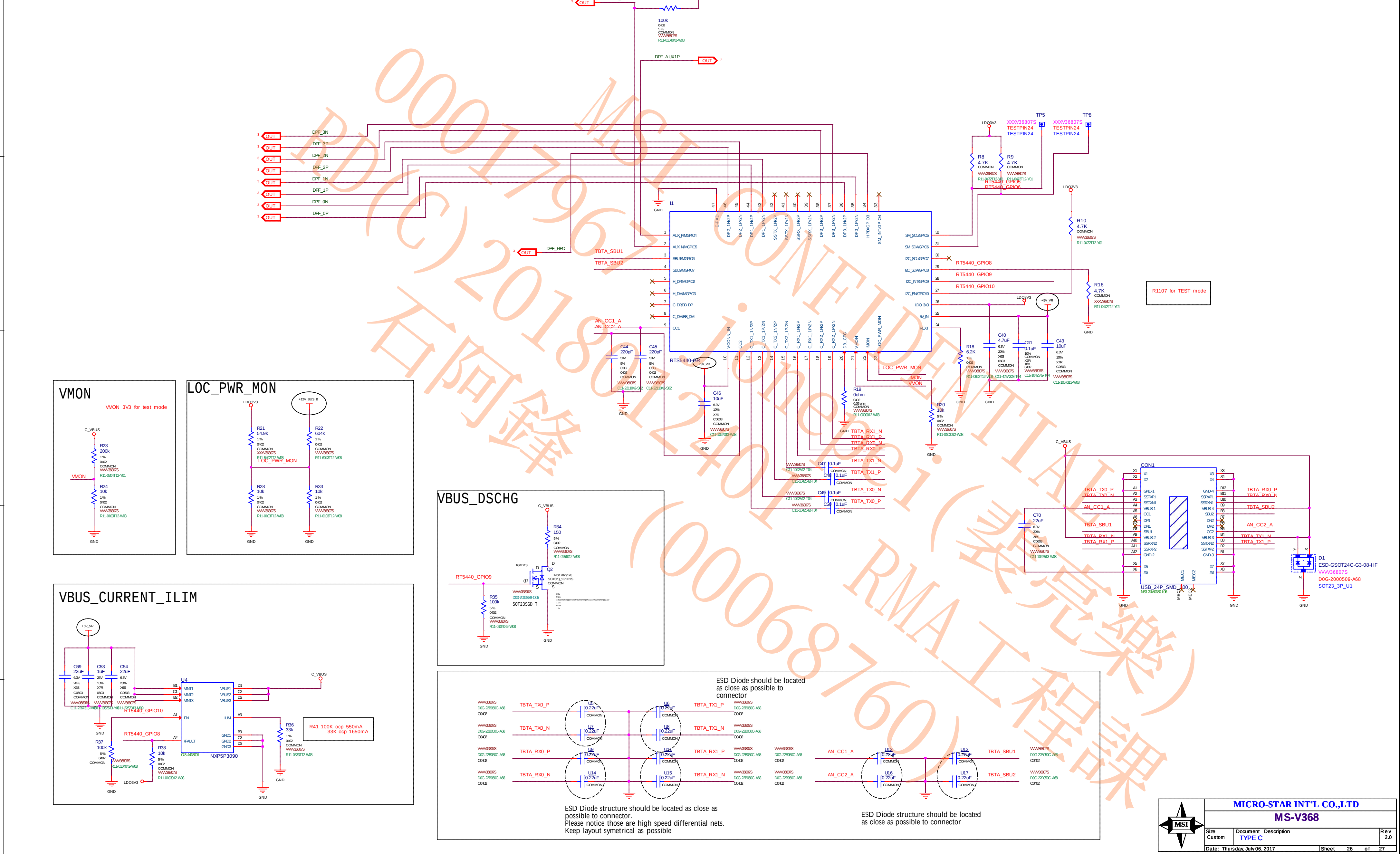

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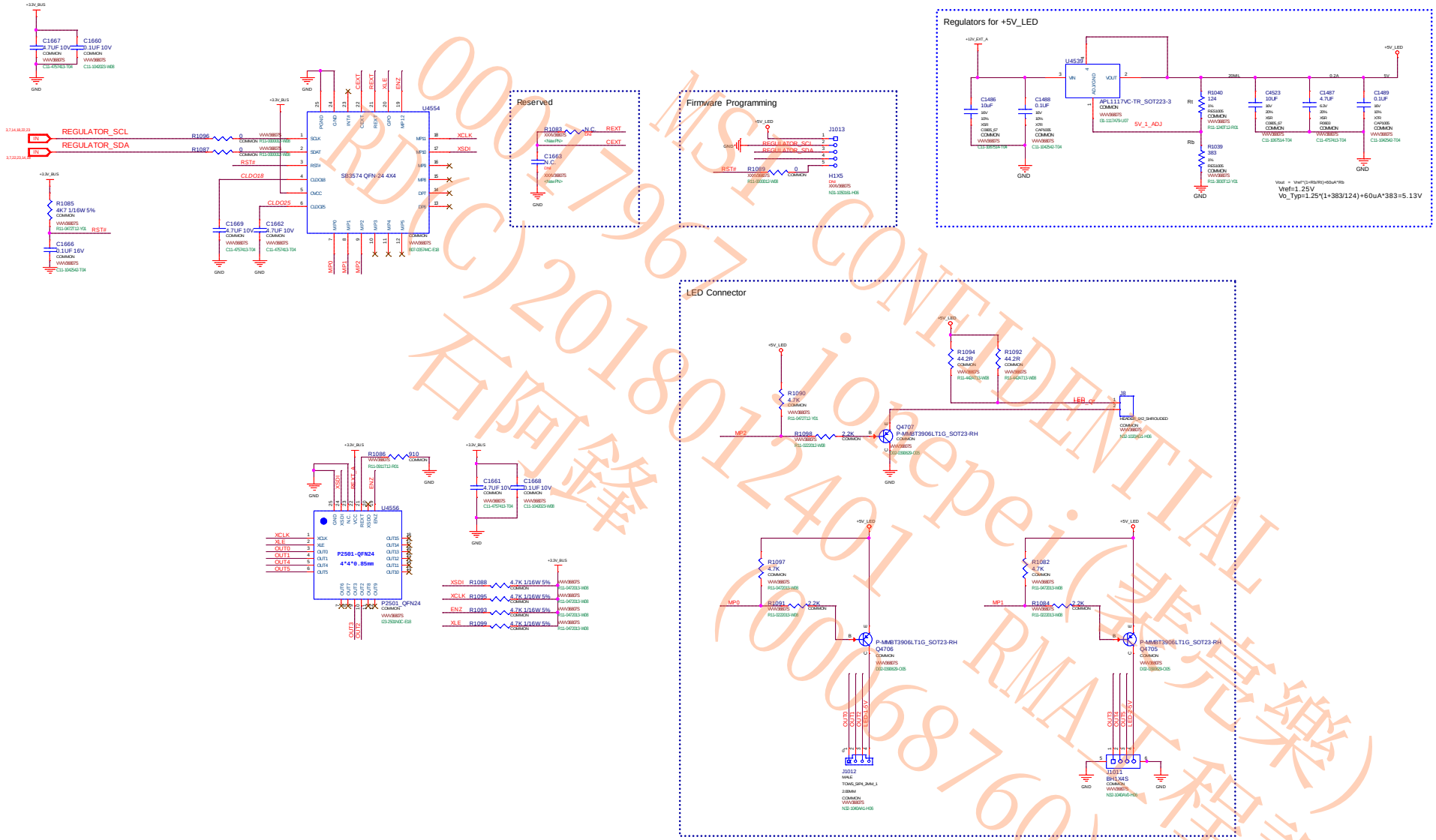
Page39: LED_CONTROLLER_ENE3574



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