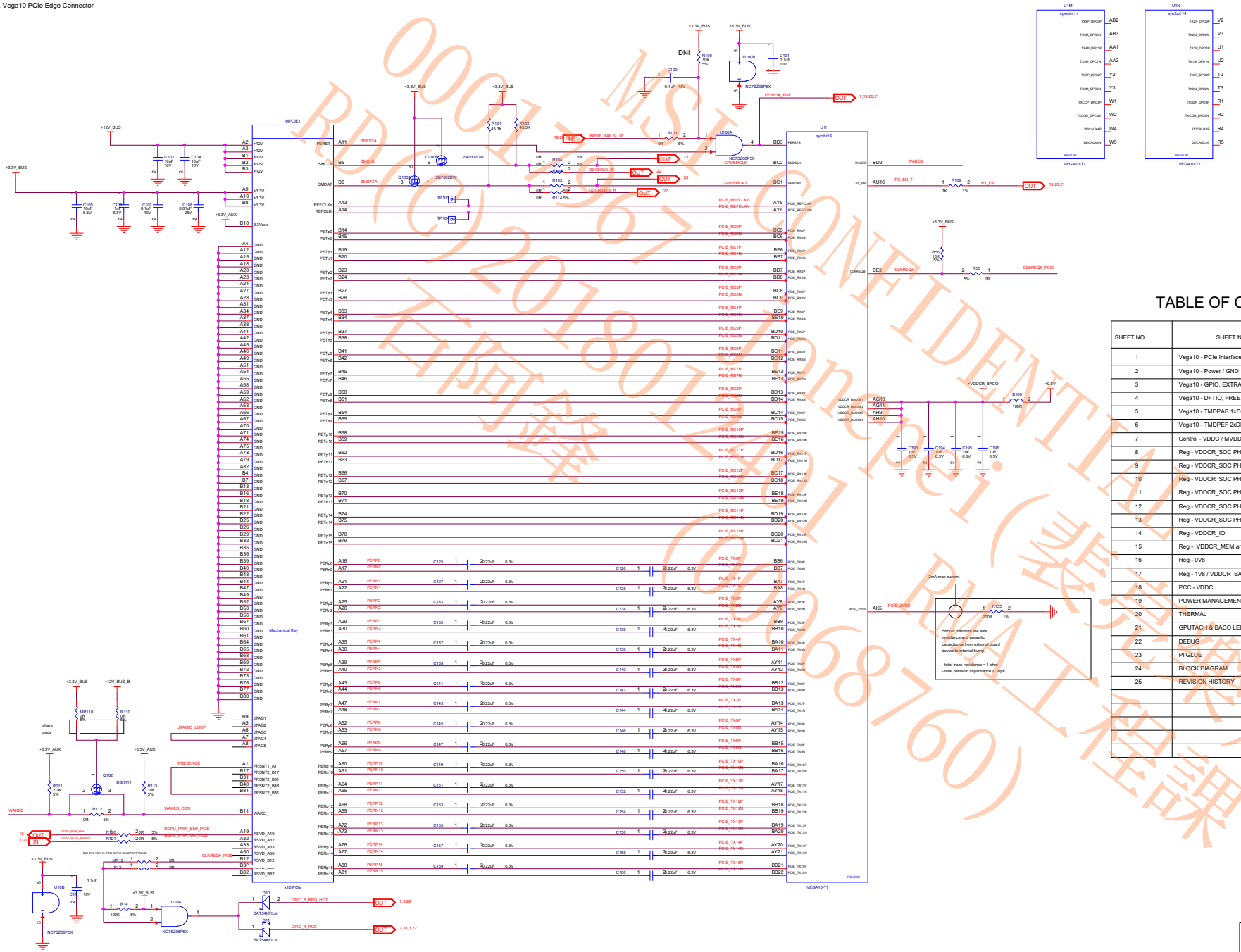
1. Vega10 PCIe Edge Connector



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RD(C)2018/1/1 (0068760) 石陶鋒

SYMBOL LEGEND

DNI	DO NOT INSTALL
o or #	ACTIVE LOW
BUD	BRING UP ONLY
	DIGITAL GROUND
	ANALOG GROUND

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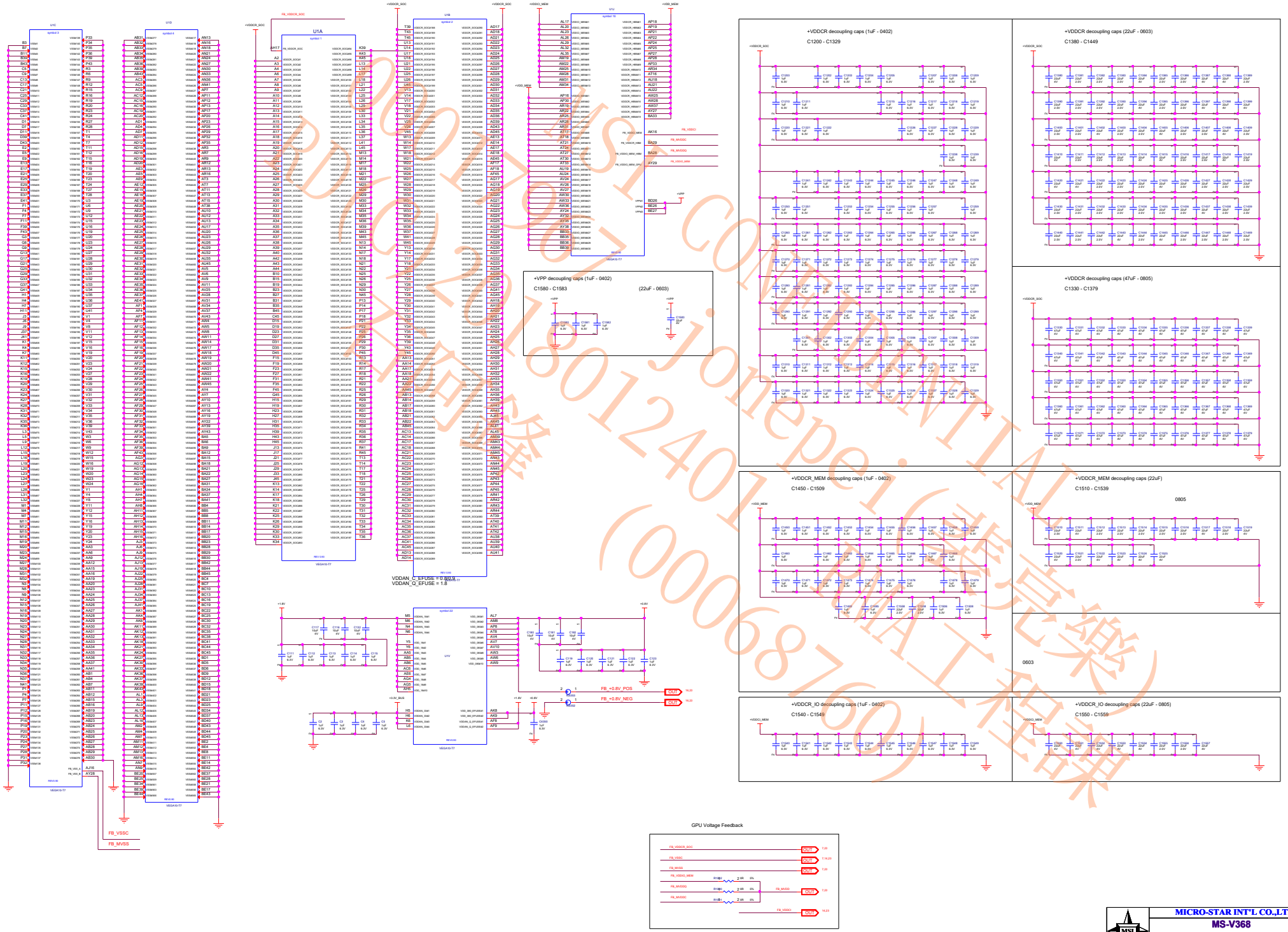

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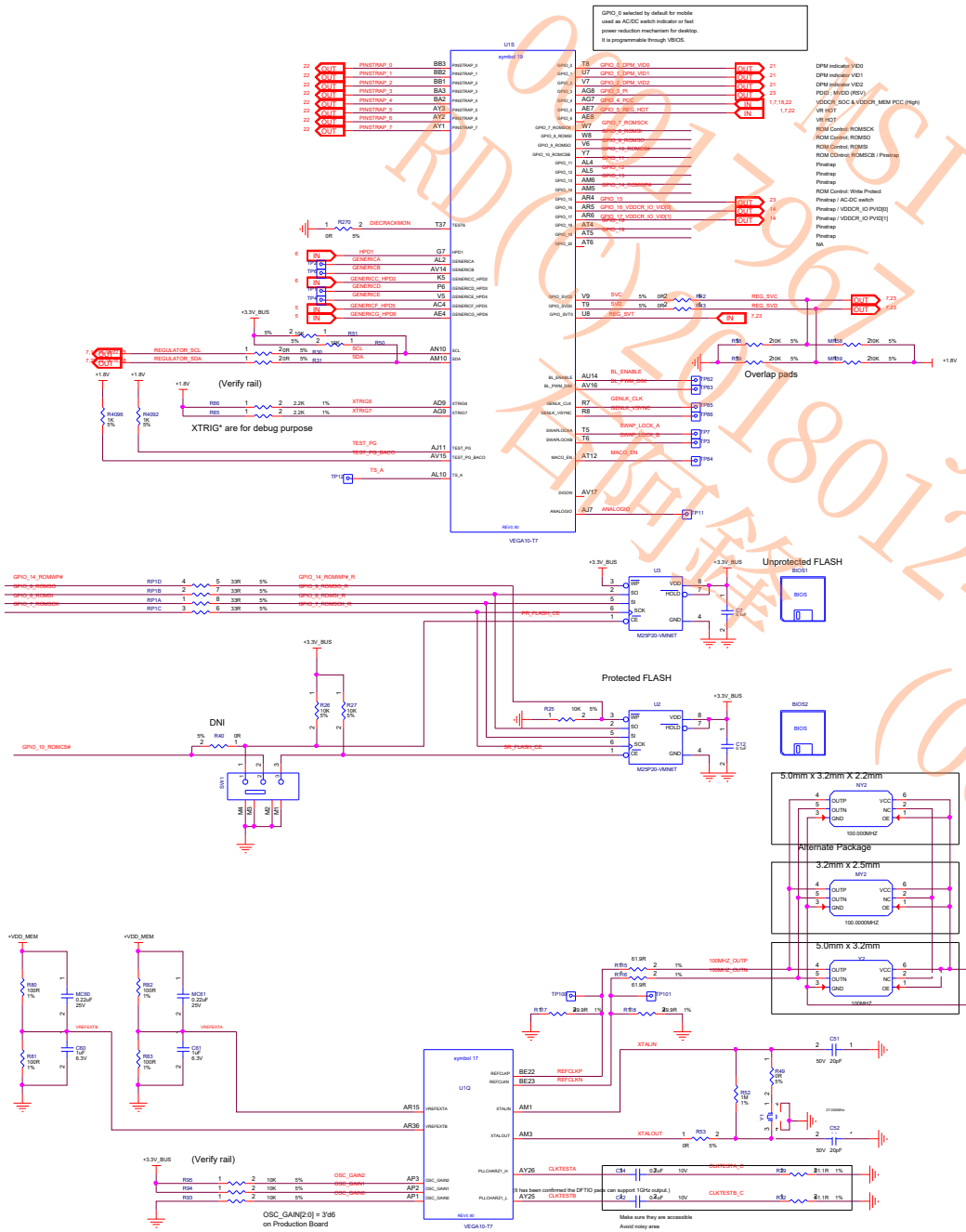

Note: Internal PU/PD at GPIO pad is strength in 14nm design spec

User		Internal Default Value	Definition
BIF		0	STRAP_BIF_GEN3_DIS_A 0: PCIe GEN 3 supported 1: PCIe GEN 3 not supported
		0	PINSTRAP_BIF_CLK_PM_EN 0: CLKREQ# power management capability is disabled 1: CLKREQ# power management capability is enabled
		0	PINSTRAP_BIF_LC_TX_SWING
		0	PINSTRAP_BIF_VGA_DIS 0: VGA controller capacity enabled 1: The device won't be recognised as the system's VGA controller
DCE		0 0 0	PINSTRAP_AUD_PORT_CONN[2:0] Number of audio-capable display outputs 0: All endpoints connected 1: 6 endpoints connected 2: 5 endpoints connected 3: 4 endpoints connected 4: 3 endpoints connected 5: 2 endpoints connected 6: 1 endpoint connected 7: 0 endpoints connected
		0 0	PINSTRAP_AUD[1:0] 1: Audio for DisplayPort only 2: Audio for DisplayPort and HDMI if dongle is detected 3: Audio for DisplayPort and native HDMI
Platform		0 0 0	PINSTRAP_BOARD_CONFIG[2:0] TBD
SMU		1 0 1	PINSTRAP_ROM_CONFIG[2:0] 100 - 512KBIT (ST) M25P05A 101 - 1MBIT (ST) (M25P10A) 101 - 2MBIT (ST) M25P20 101 - 4MBIT (ST) M25P40 101 - 8MBIT (ST) M25P80 100 - 512KBIT (CHINGIS) PM25LV512 101 - 1MBIT (CHINGIS) PM25LV010
		0	PINSTRAP_SMBUS_ADDR 0: 0x41h 1: 0x40h
		1	PINSTRAP_BIOS_ROM_EN 0: Disable the external BIOS ROM device 1: Enable the external BIOS ROM device

//gpuE/doc/design/chip/padring/AI_dGPU/PinStrap_Plan.pptx

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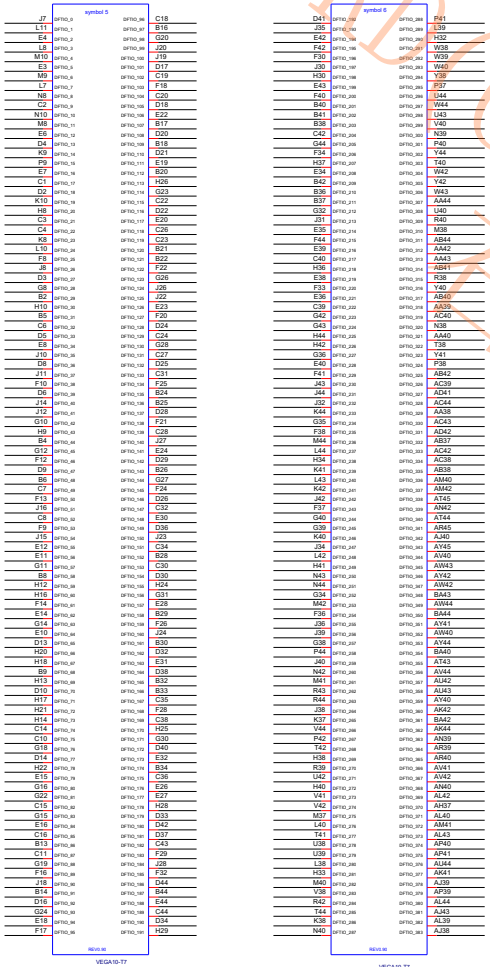
DFTIO



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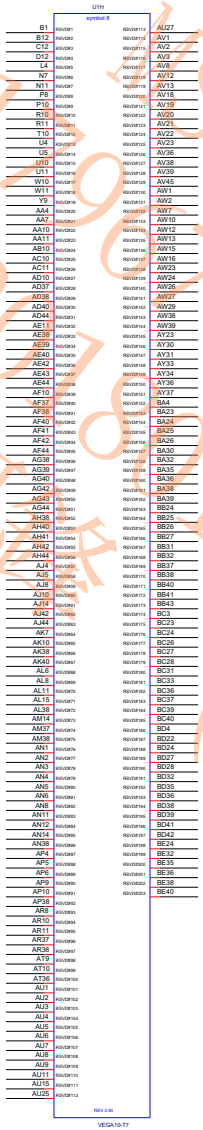
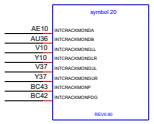


HBM_DAP

CRACKMON



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Ensure traces < 5 inches MAX (if routed on same layer)

For differential routing on HDMI 2.0 connection, use dogbone shape antipads for the transitional vias of the same differential pair, and the distance from the via edge to the shape boundary should be

Add GND voids underneath

Void Covering Pad and body

In 14nm design, all the TMDP PHYs share a common calibration pin pair named DP_ZVDD_08 and DP_ZVSS.

Can no longer share calibration pins between AUX and DP like in 28nm

14nm are not +5V tolerant

Ensure traces < 5 inches

Add GND voids underneath

OPTIONAL ESD PROTECTION DIODES

OPTIONAL ESD PROTECTION DIODES

OVERLAP WITH J1750

Regulators for +5V and +5V_VESA

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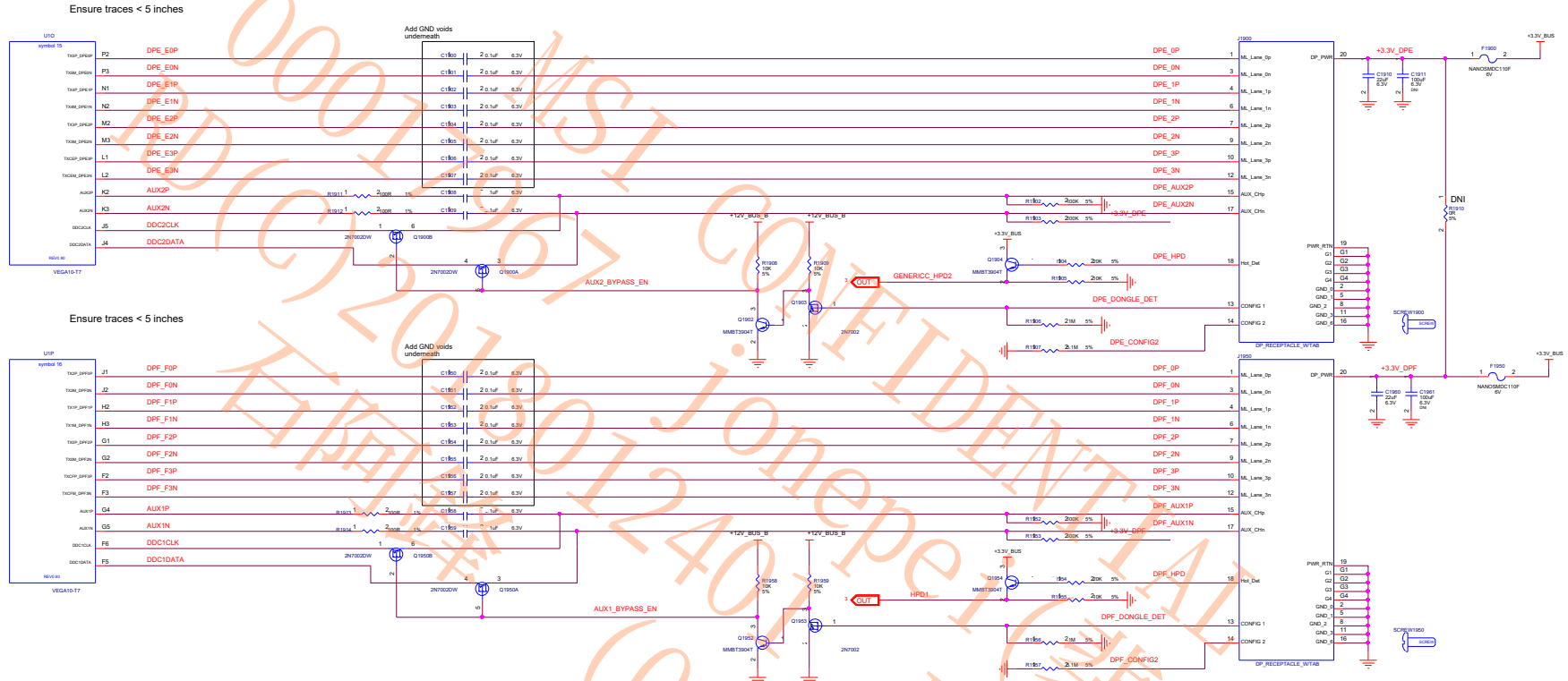

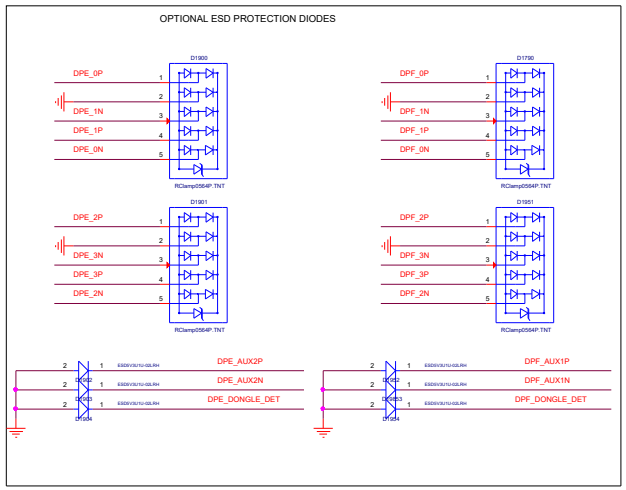

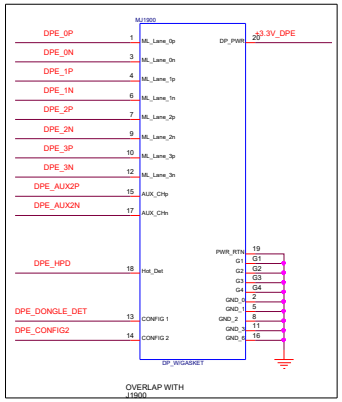

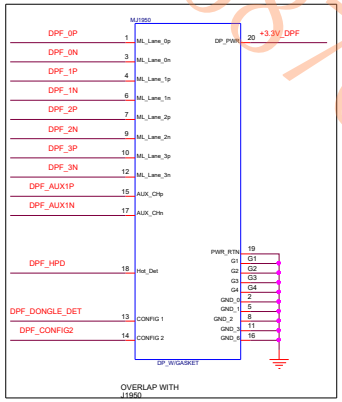

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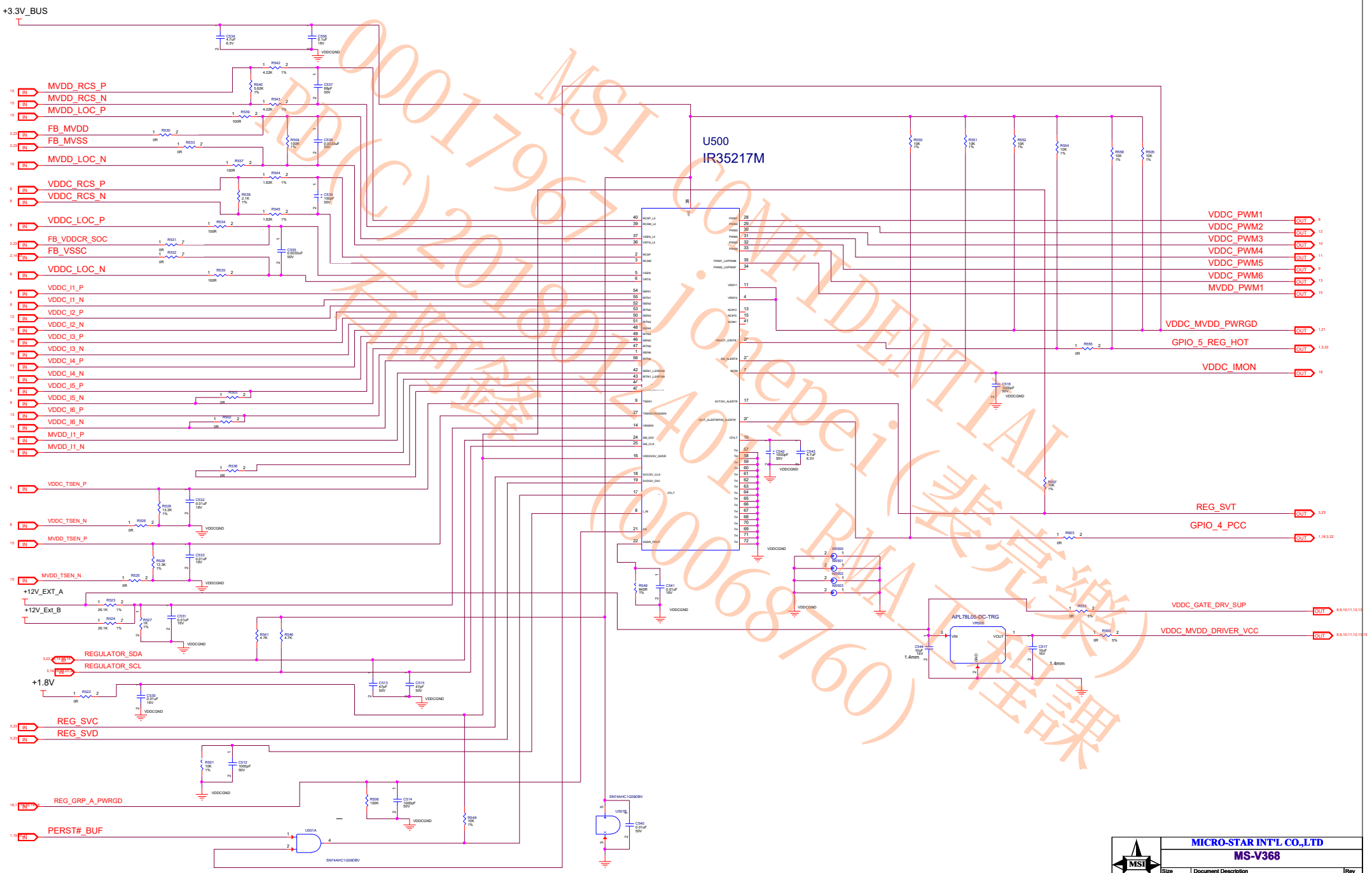

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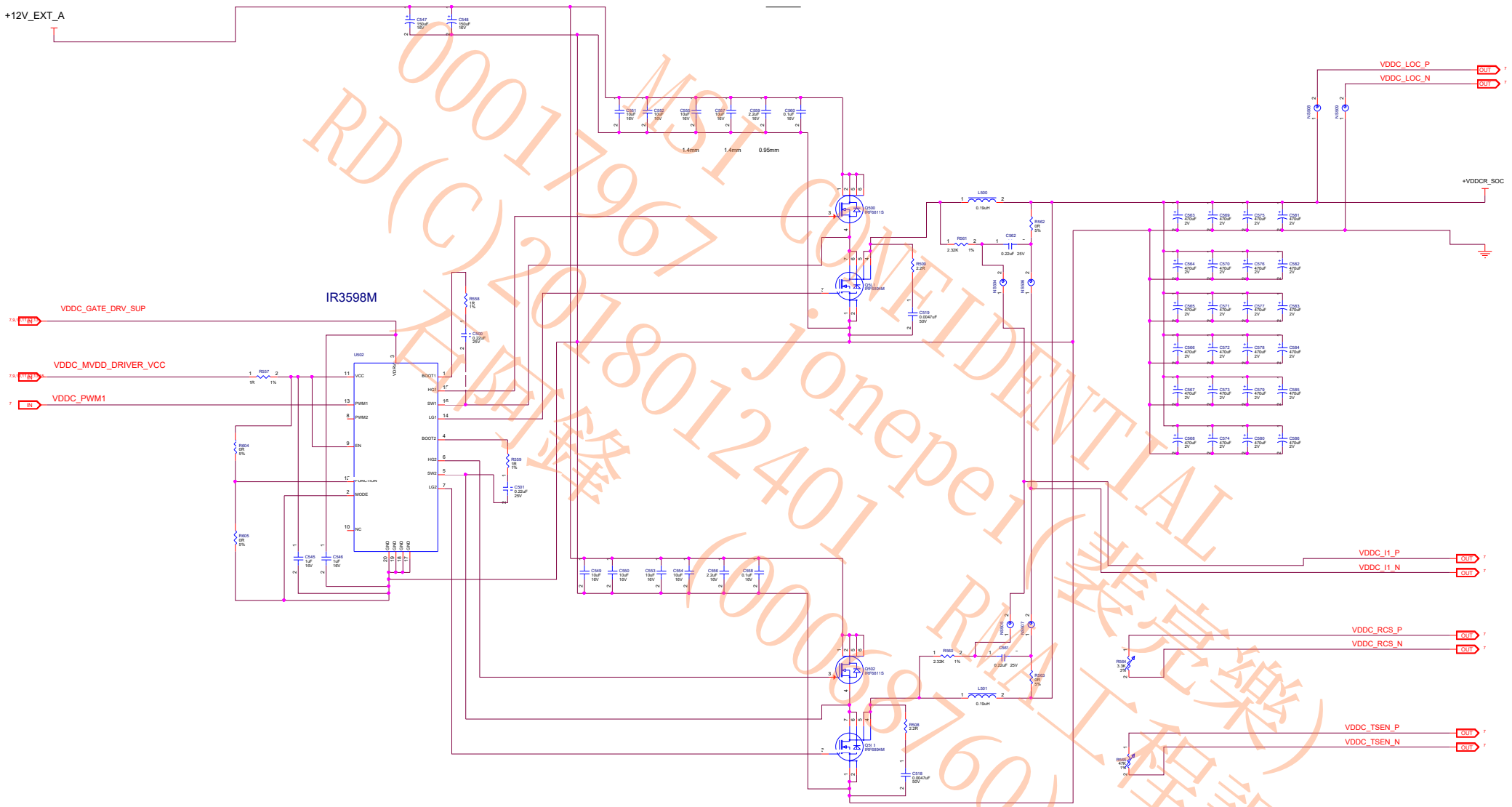

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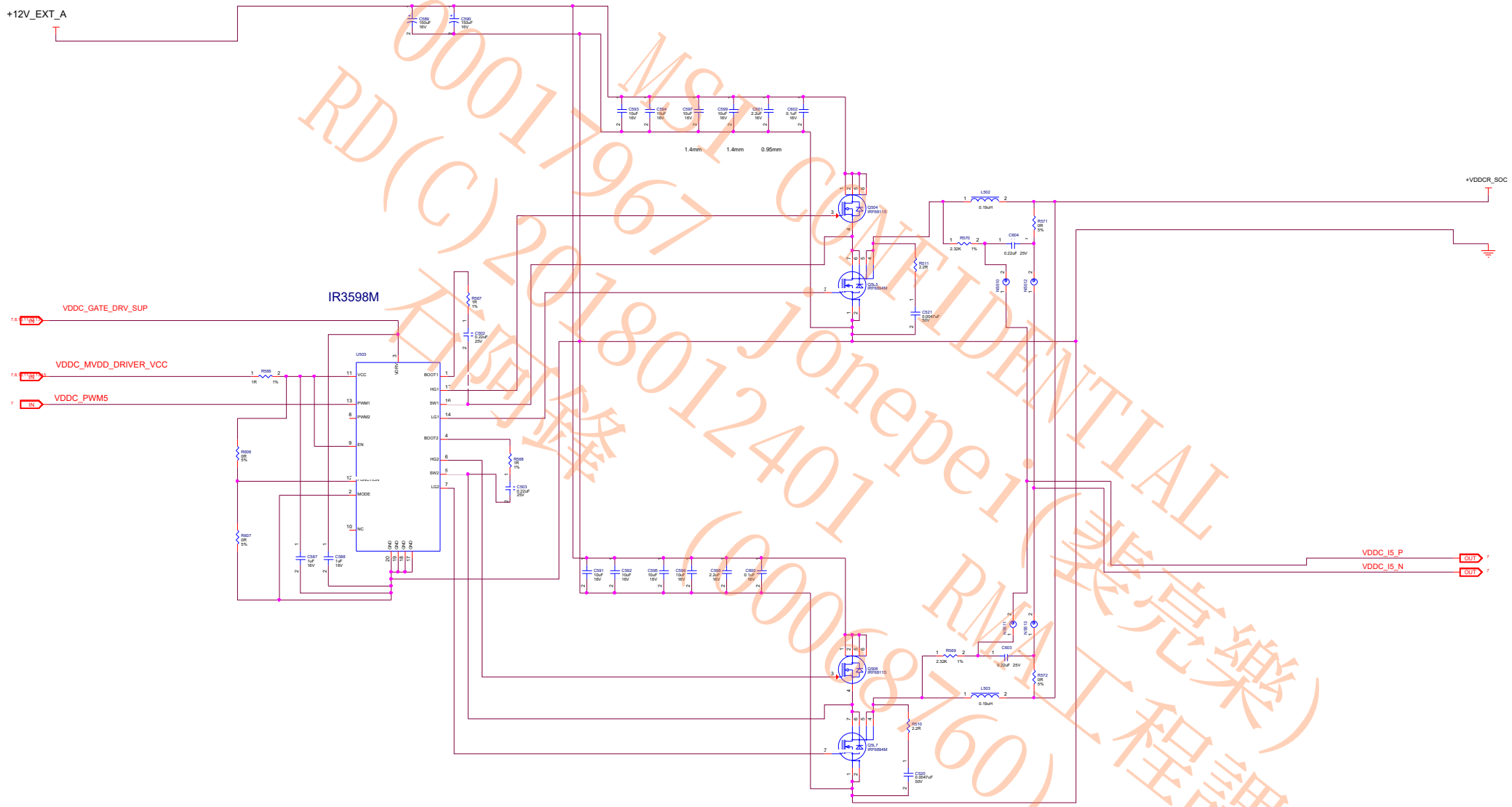

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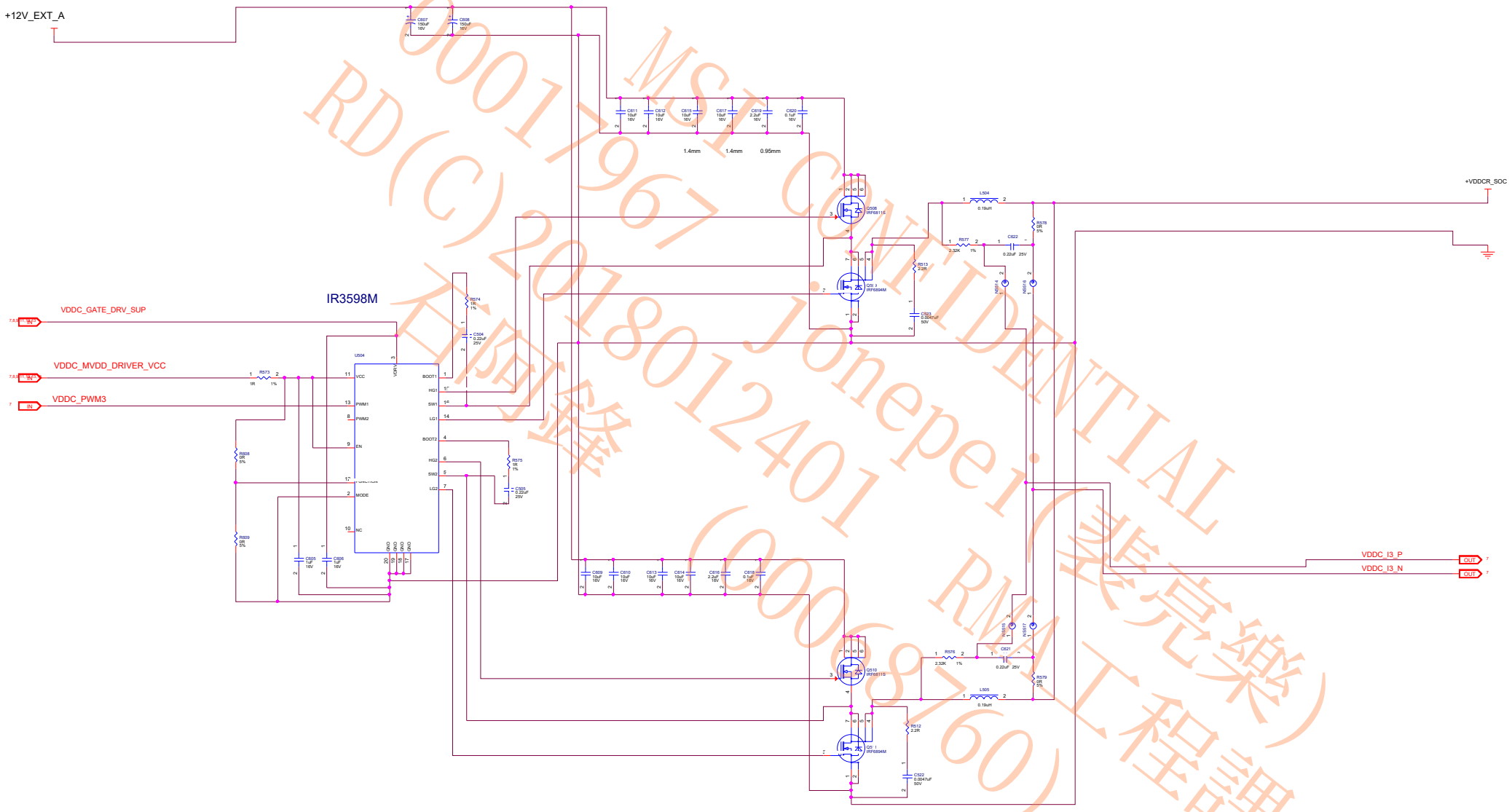

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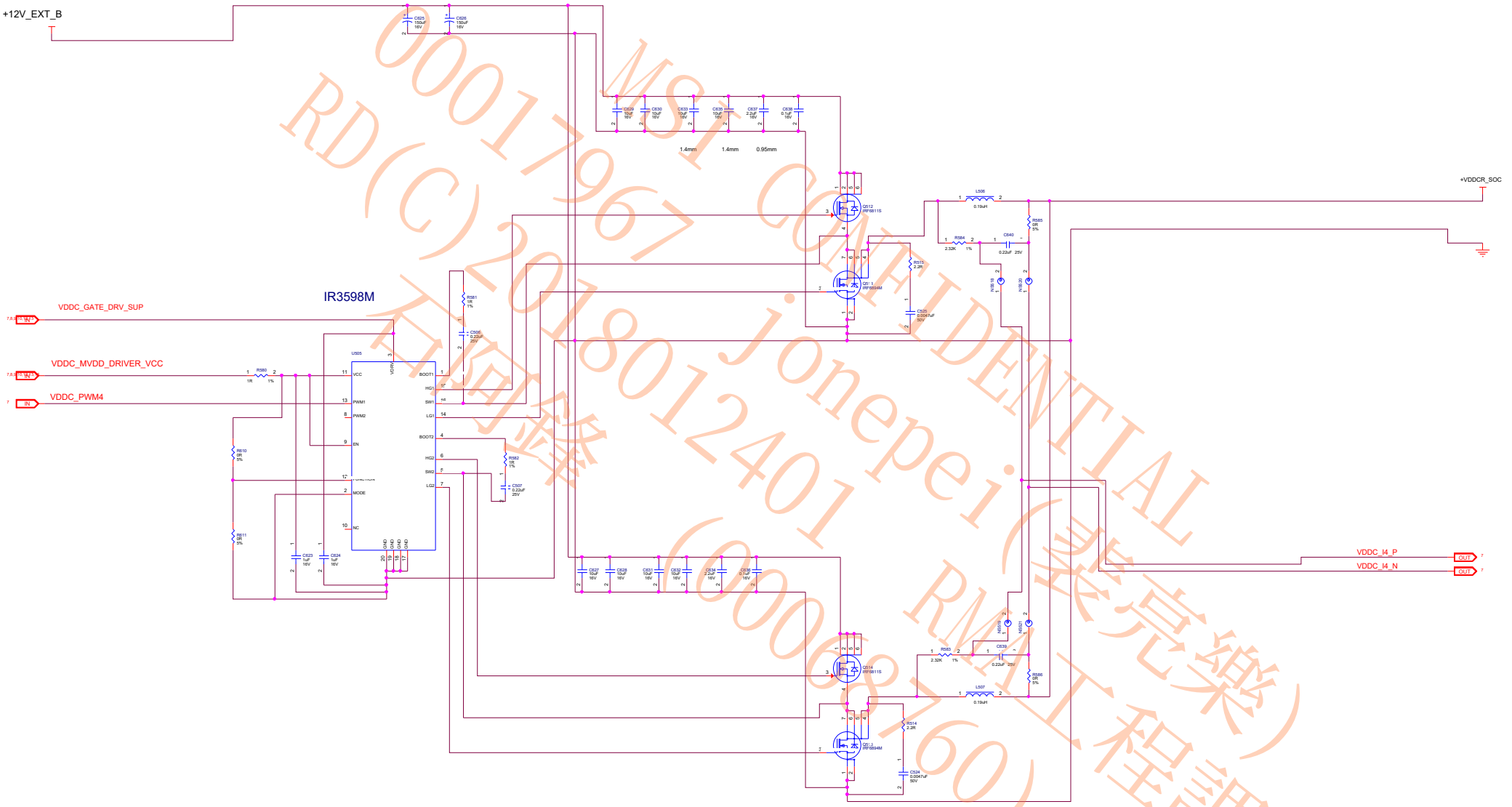

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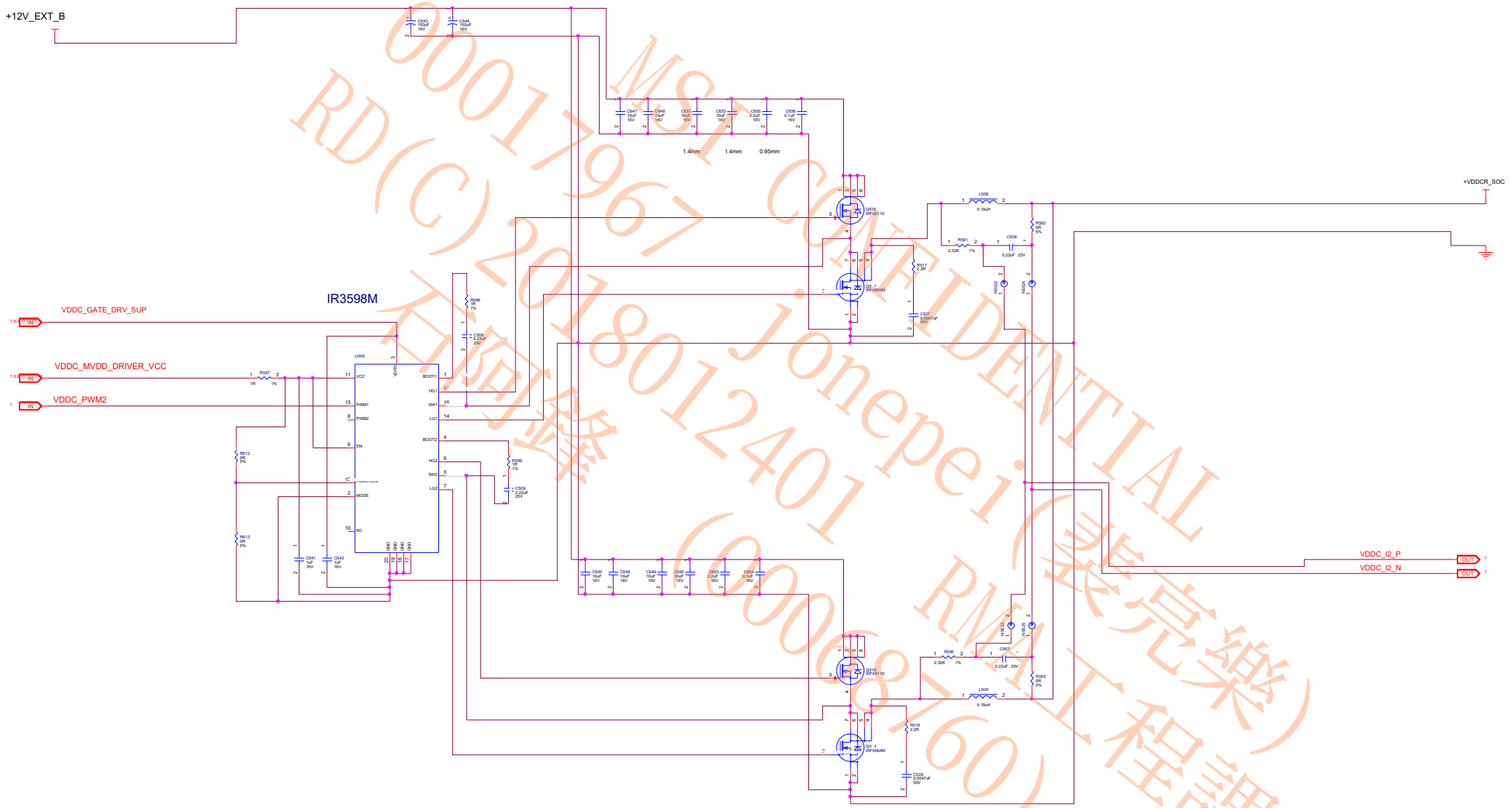

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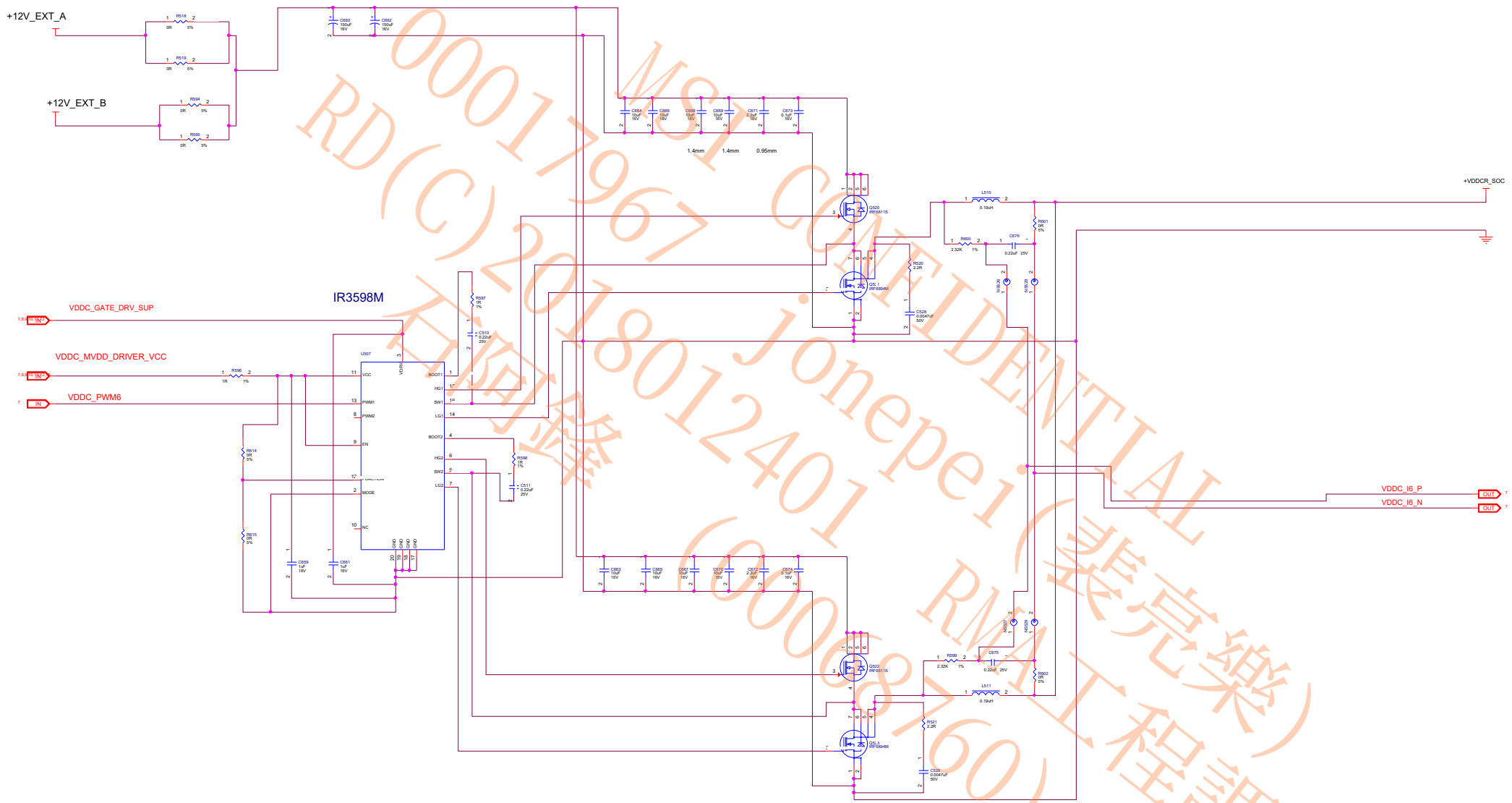

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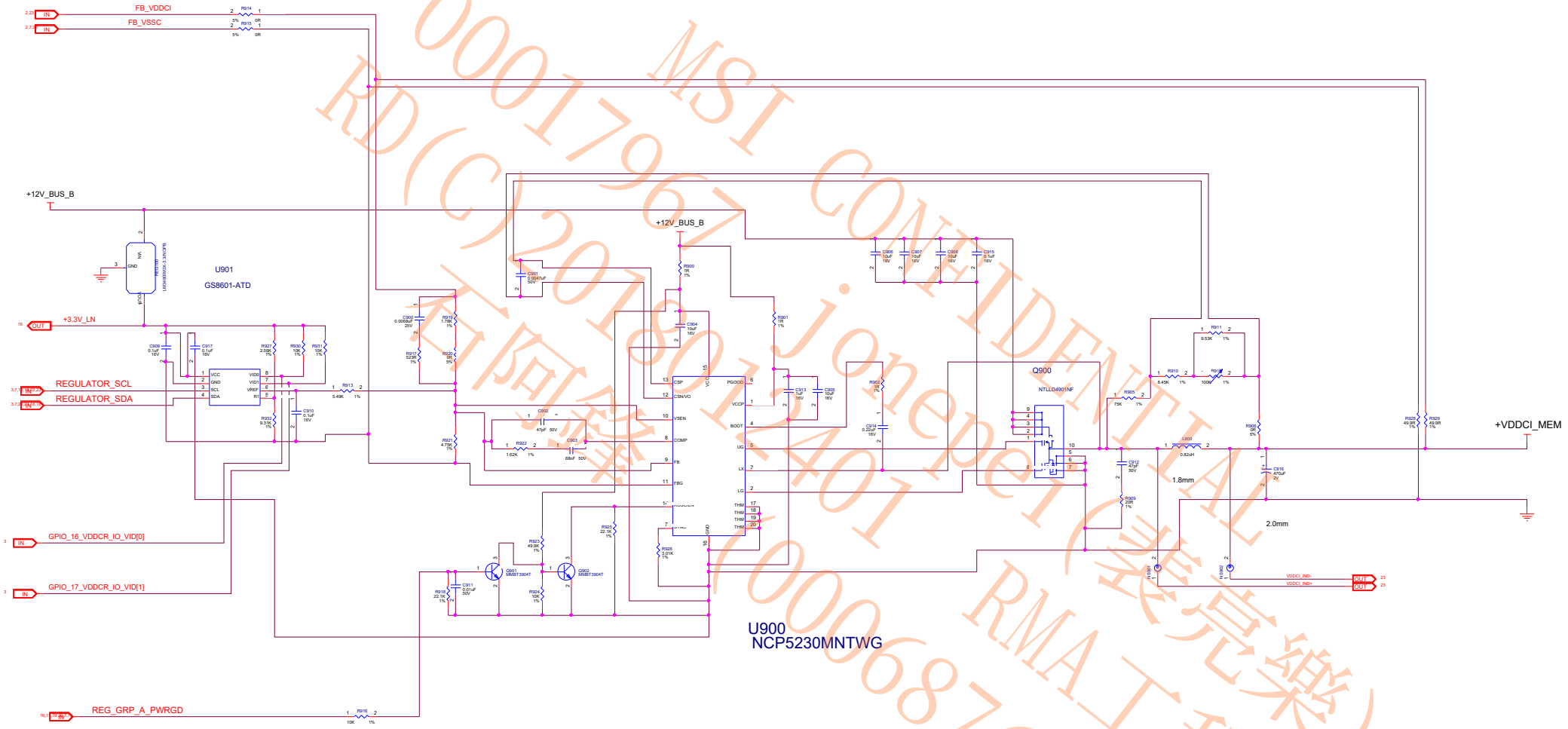

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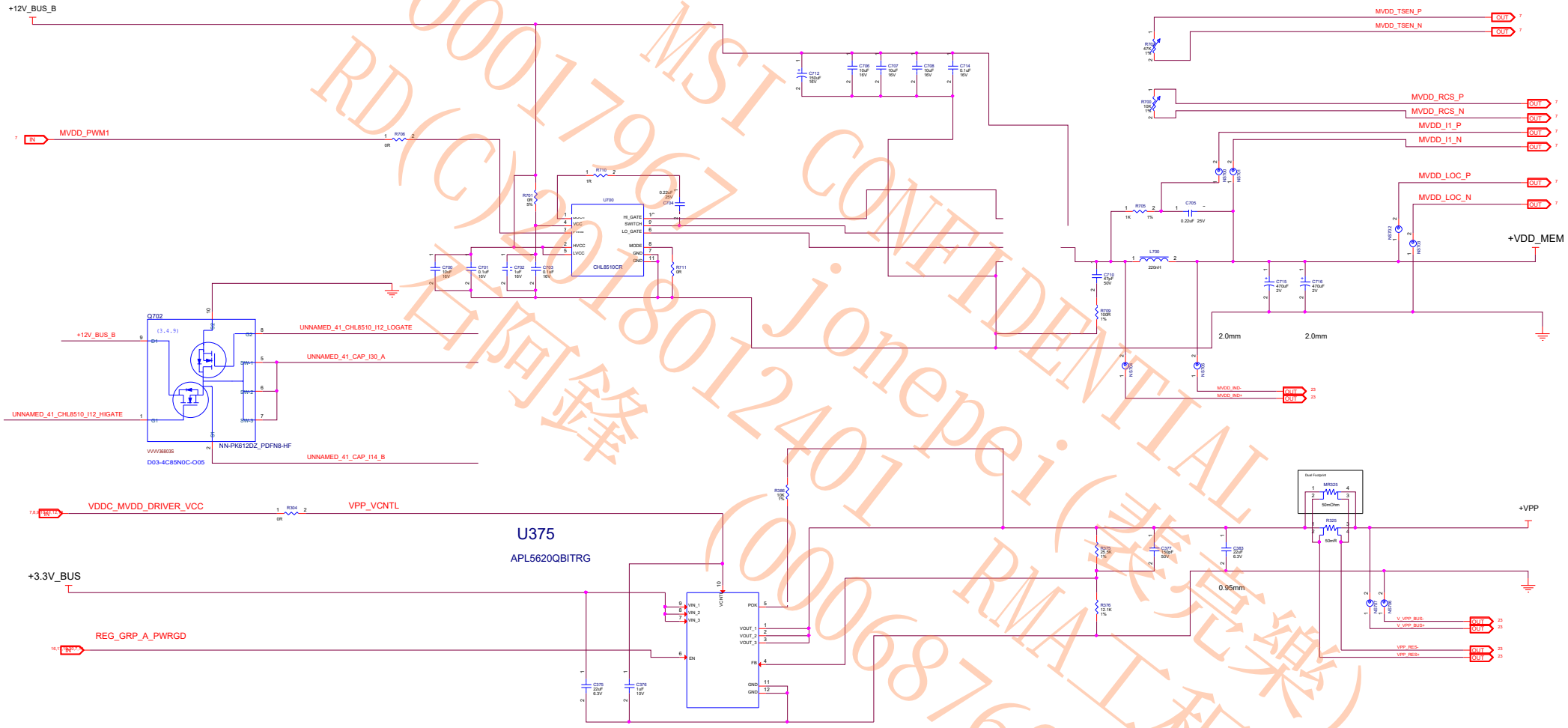

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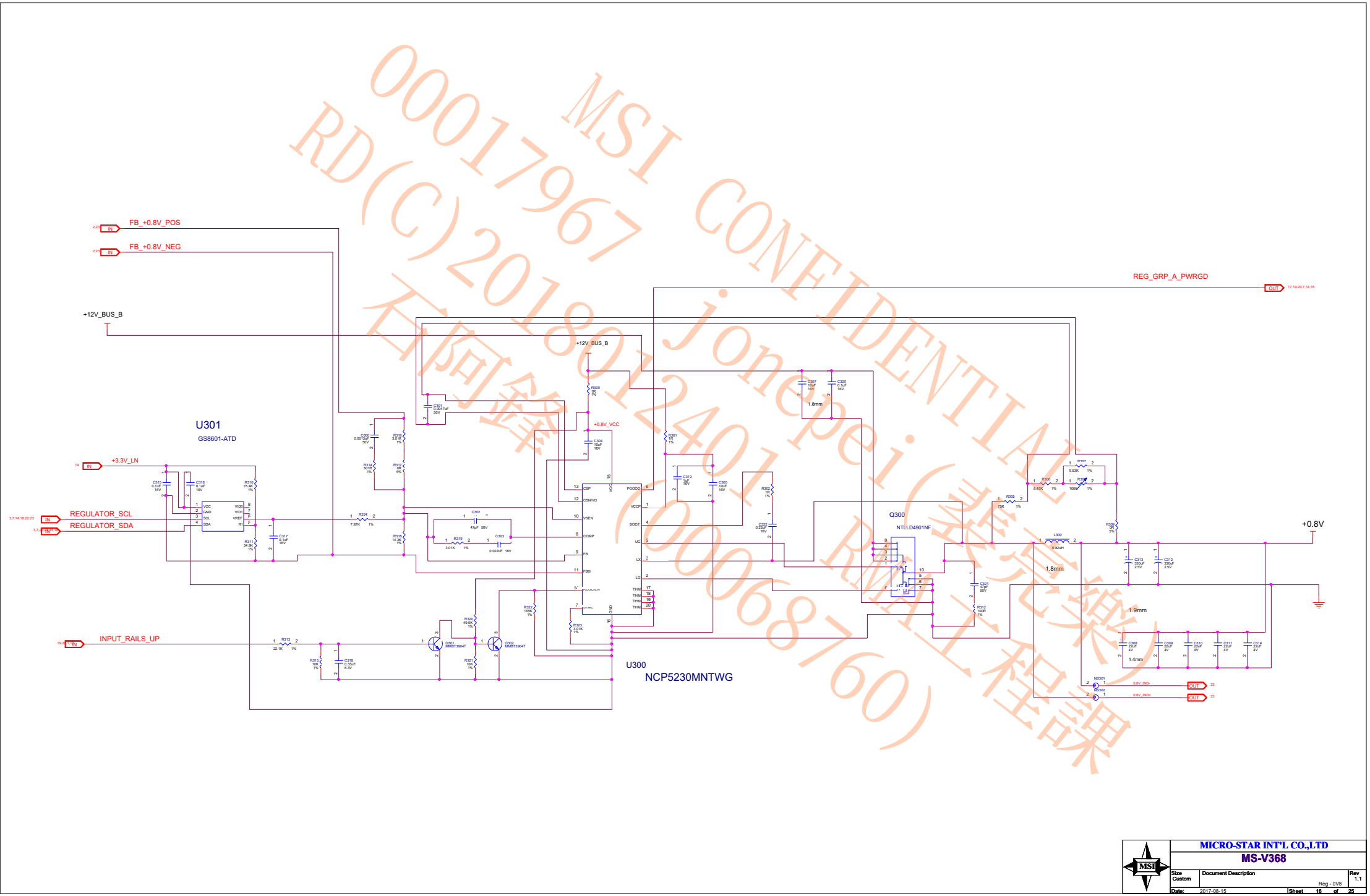

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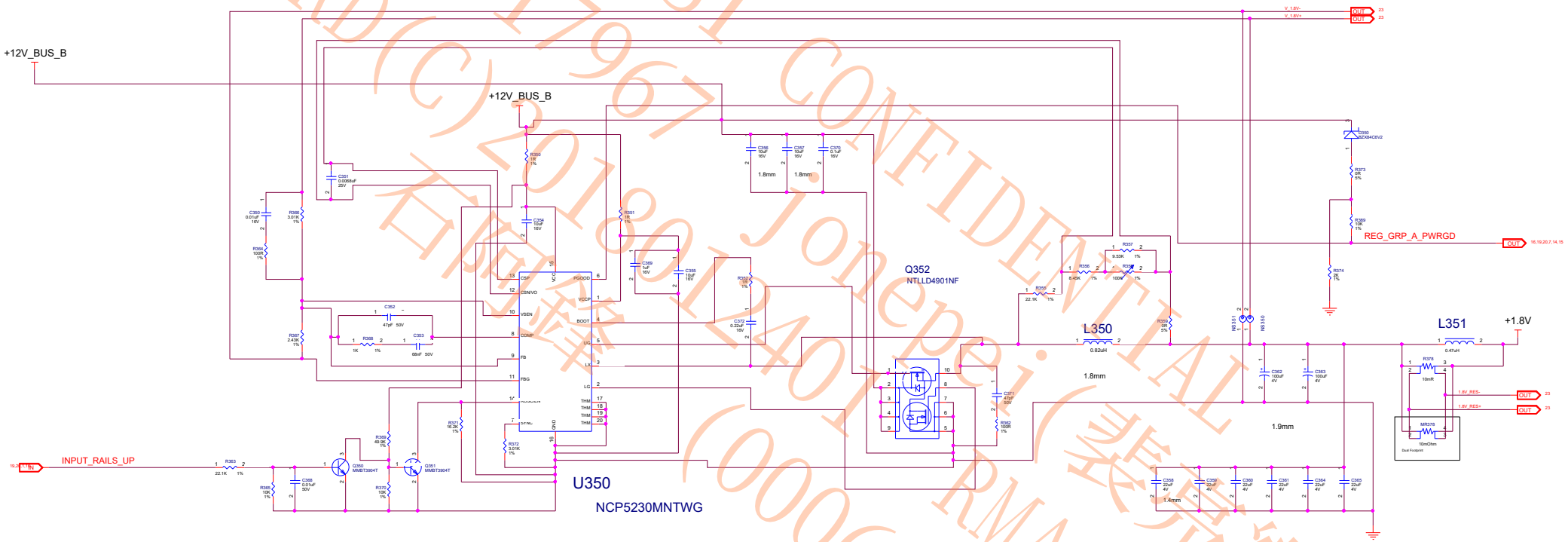

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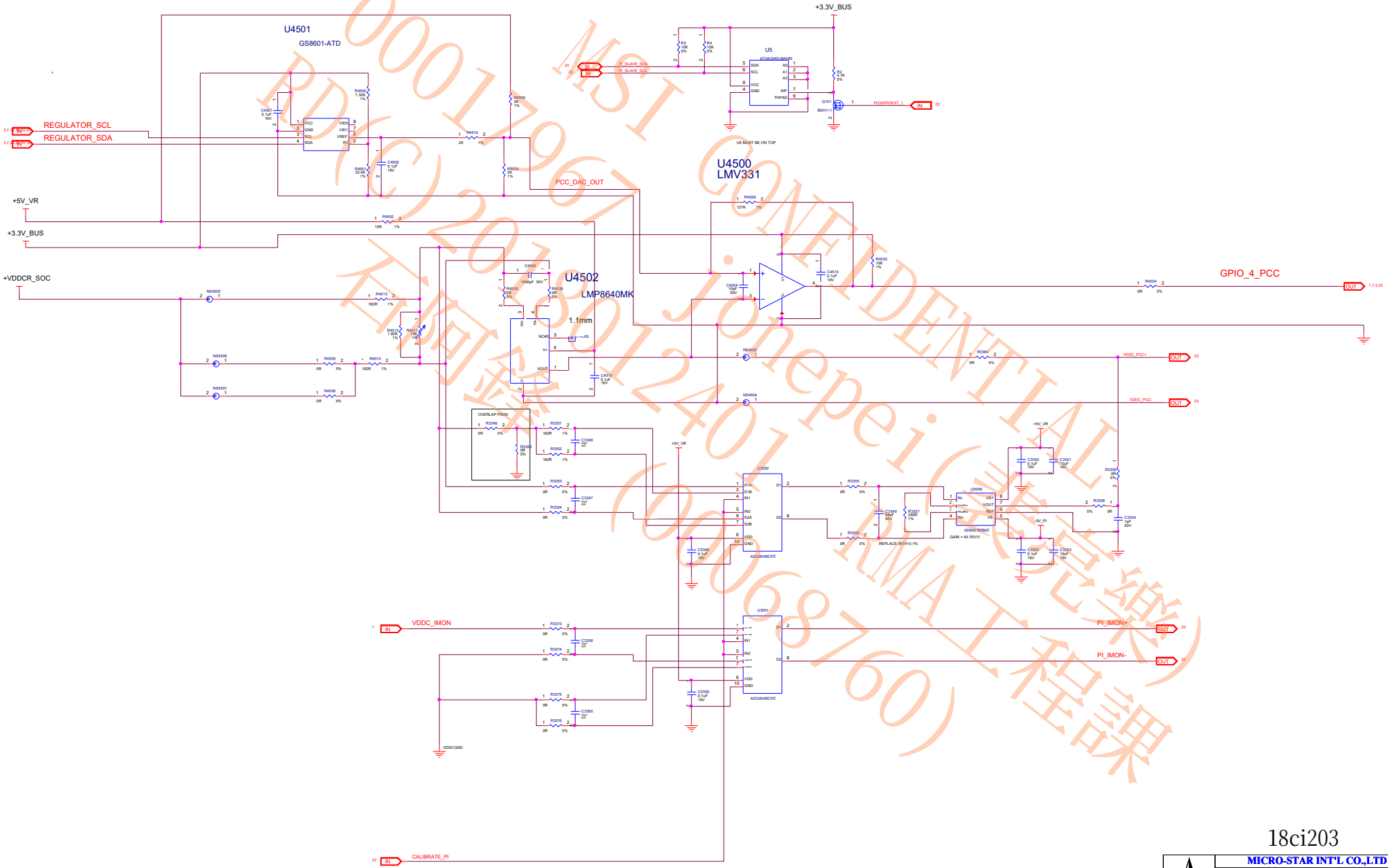

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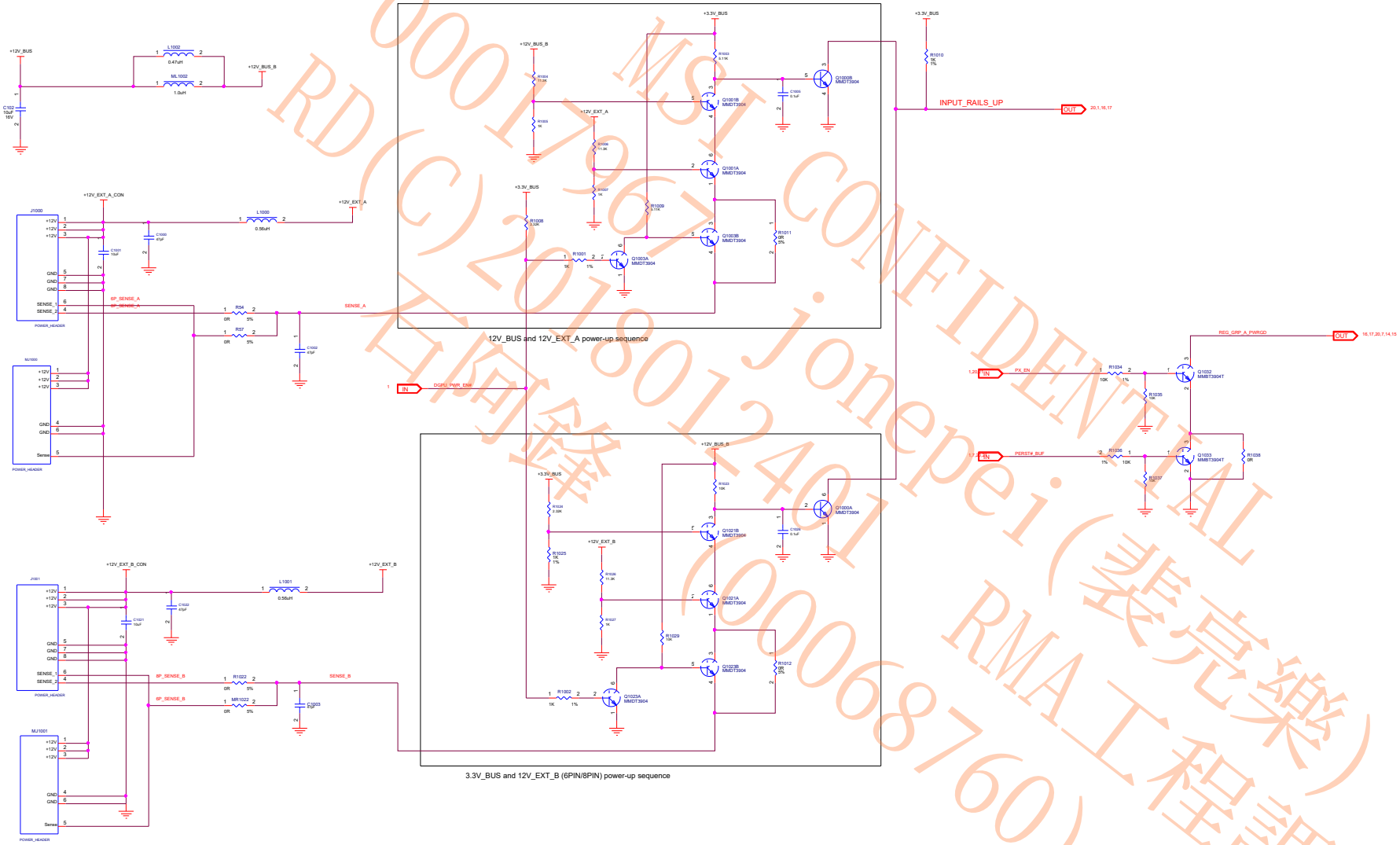

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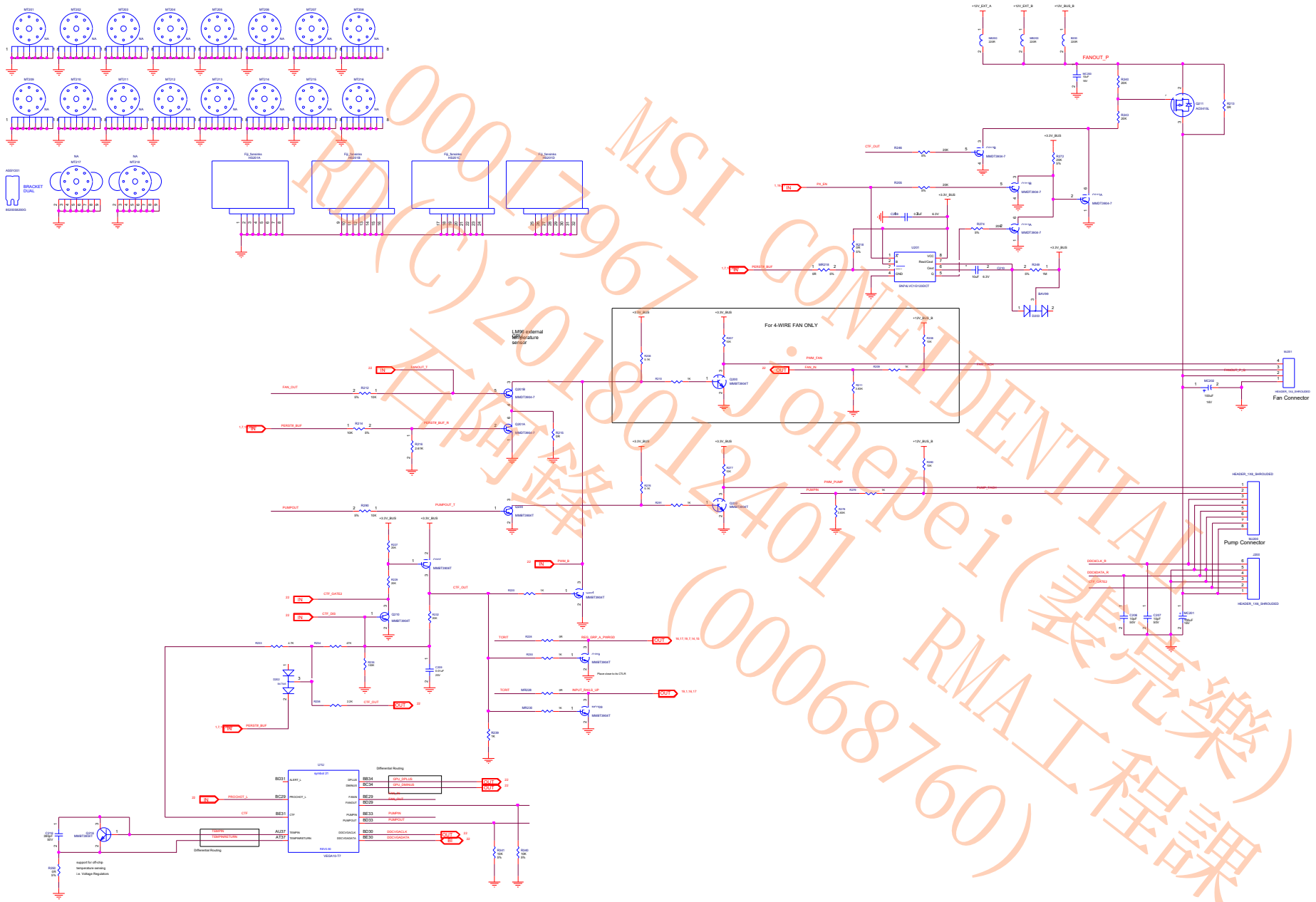

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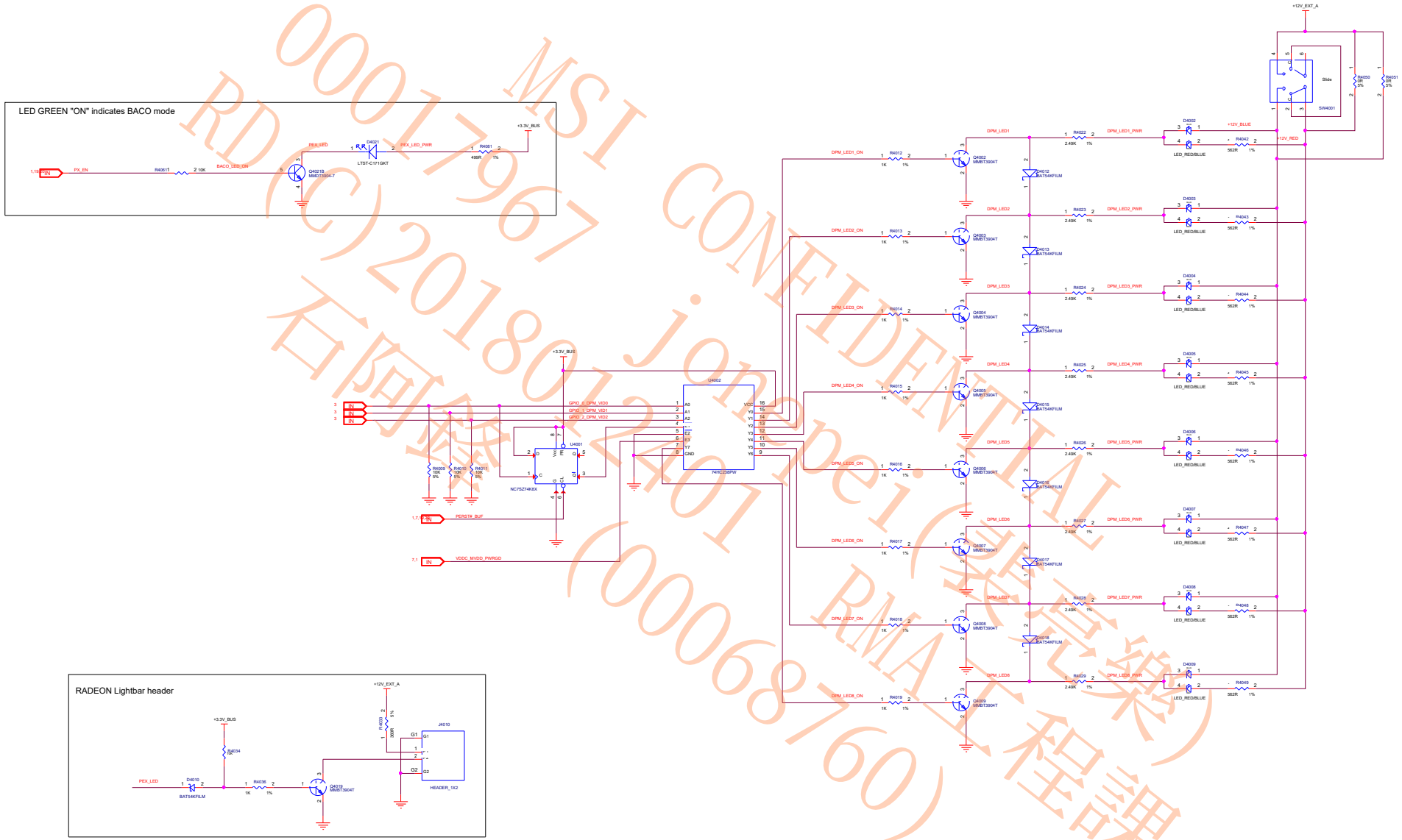

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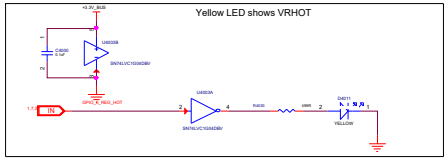

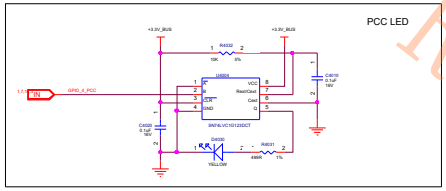

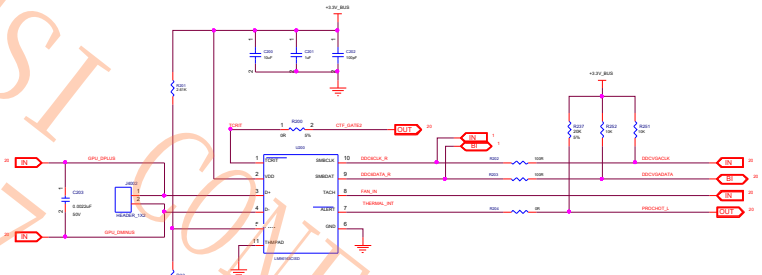

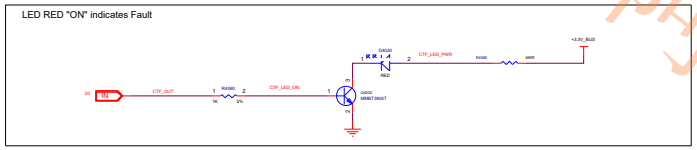

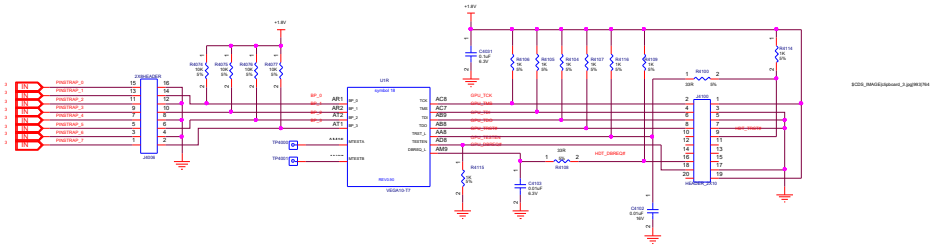

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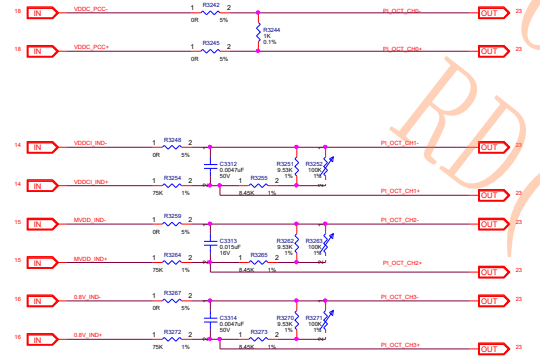
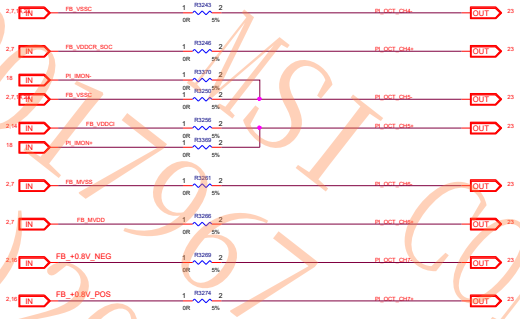
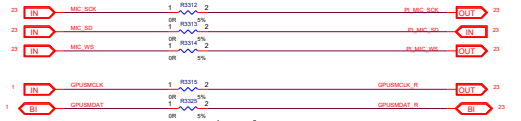
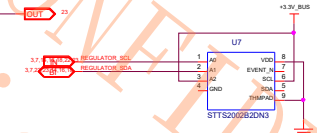
ALL COMPONENTS TO BE LOCATED NEXT TO SENSING ELEMENT (ON MAIN BOARD)
NETS IN GREEN SHOULD BE RE-NAMED



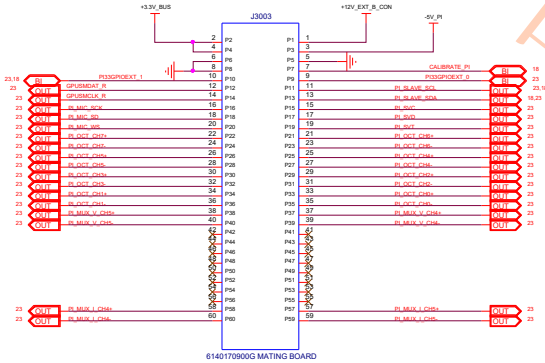


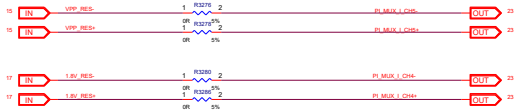


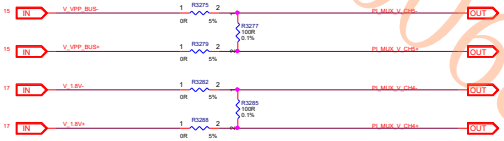


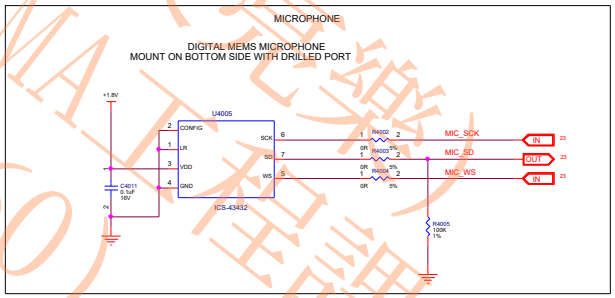
PLACE HOLDER FOR DS28C22
U7 MUST BE ON TOP

RESERVED FOR I2C_MASTER PINS









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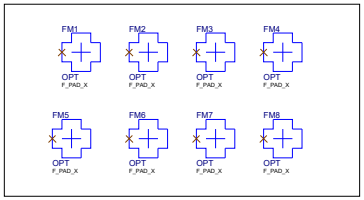

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A	10/9/15	Initial schematic creation
B	6/30/16	Many Changes on PI circuit , Minor Chnages on SMPS
C	9/30/16	Many Changes on PI circuit , ASIC SYMBOL UPDATED FOR FLASH ROM INTERFACE , flash ROM SI/SO swapped , RP1 added
D	11/29/16	Changes on PI circuit , 100MHz HCSL clock source replced (contact AMD for detailes)
E	01/05/17	PI circuit removed , 200R added to DP AUX (6 resistors)
F	02/02/17	1.8V/VPP Kelvin resistors dual footprinted , DP AUX (6 resistors changed to 100R) , Changed R4033 to 360R 1206 and moved to 12V_AUX , SMBUS Address note swap , J4001 removed , R115/R116 changed to 61.9R , R205 added
G	06/29/17	Re-Name to MSI Lable
H	08/15/17	Remove R1013,R1014,R1015,R106 and V_12V_BUS,V_12V_EXTA,V_12V_EXTB,V_3.3V_BUS, 12V_BUS_RES,12V_EXTA_RES,12V_EXTB_RES,3.3V_BUS_RES
I	08/16/17	Change J3003 footprint name from con_mating_samtec_fsi-130-03-x-d-m-ad to con_mating_samtec
I	08/17/17	Remove TP102/105/126/127/106/108/107/106/128/129/110/111/112/113/130/131/114/116/115/117/132/133/118/119/120/121/134/135/122/124/123/125. Change Q702 Footprint , Rename Page 24 to MECH and add 8 + light Point

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