

PG110-A00

GP108 64Bit GDDR5 X32

HDMI/DP + DVI-D/DP

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ASSEMBLY	<ASSEMBLY DESCRIPTION>
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NV_PN

600-1G110-BASE-A00

PCB REV

PG110-A00

BOM REV

A

PAGE

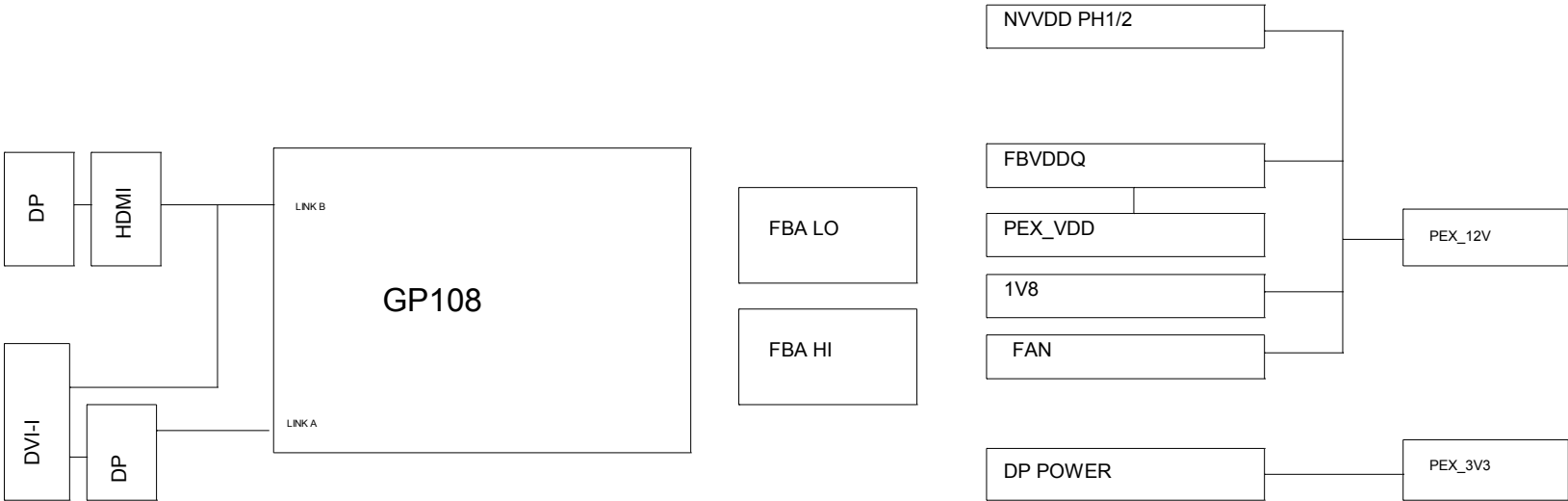
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DATE

19-JUL-2016



Block Diagram



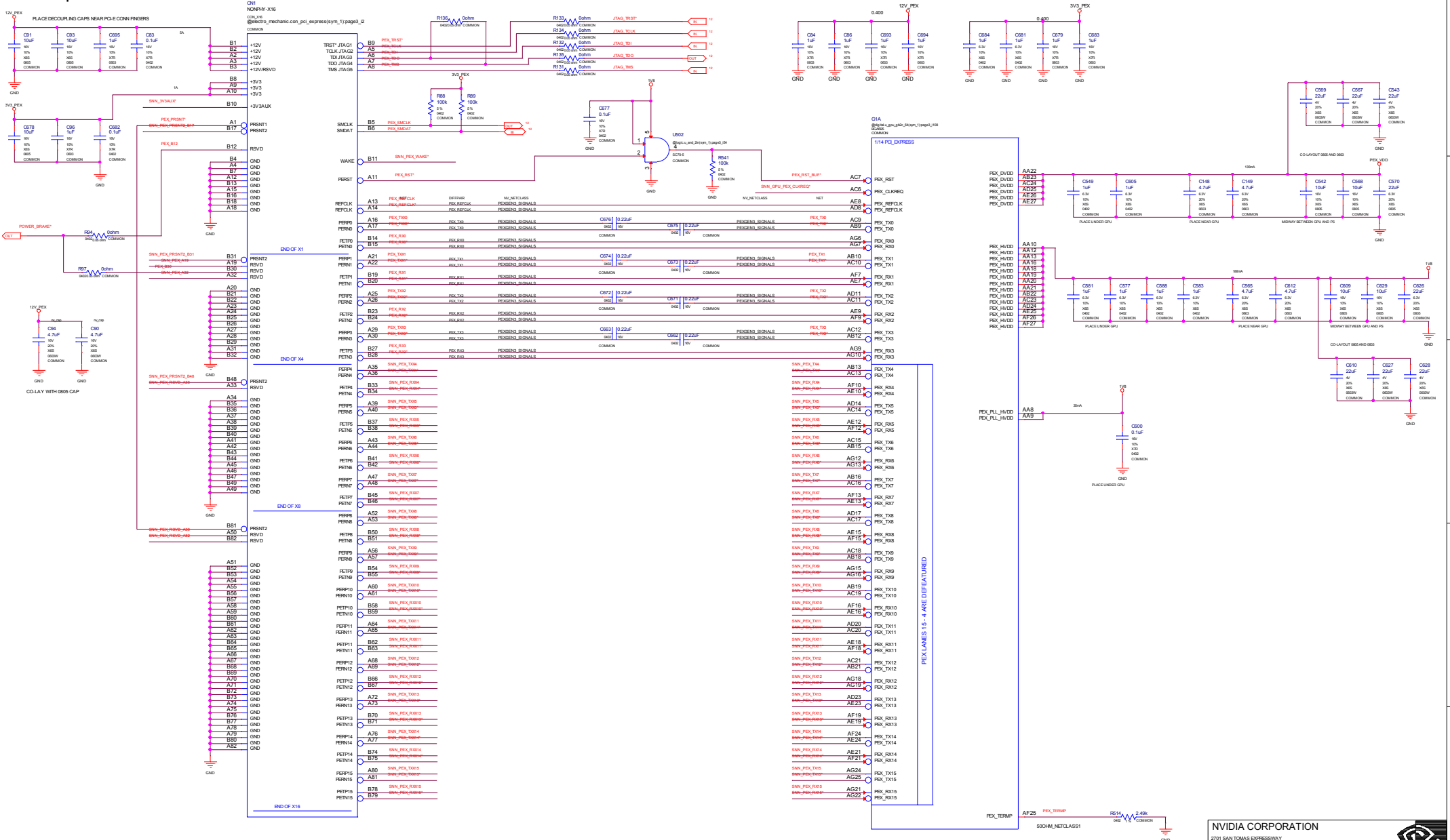
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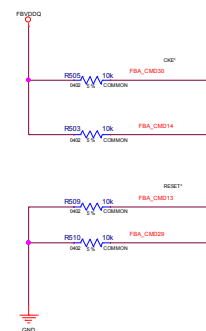
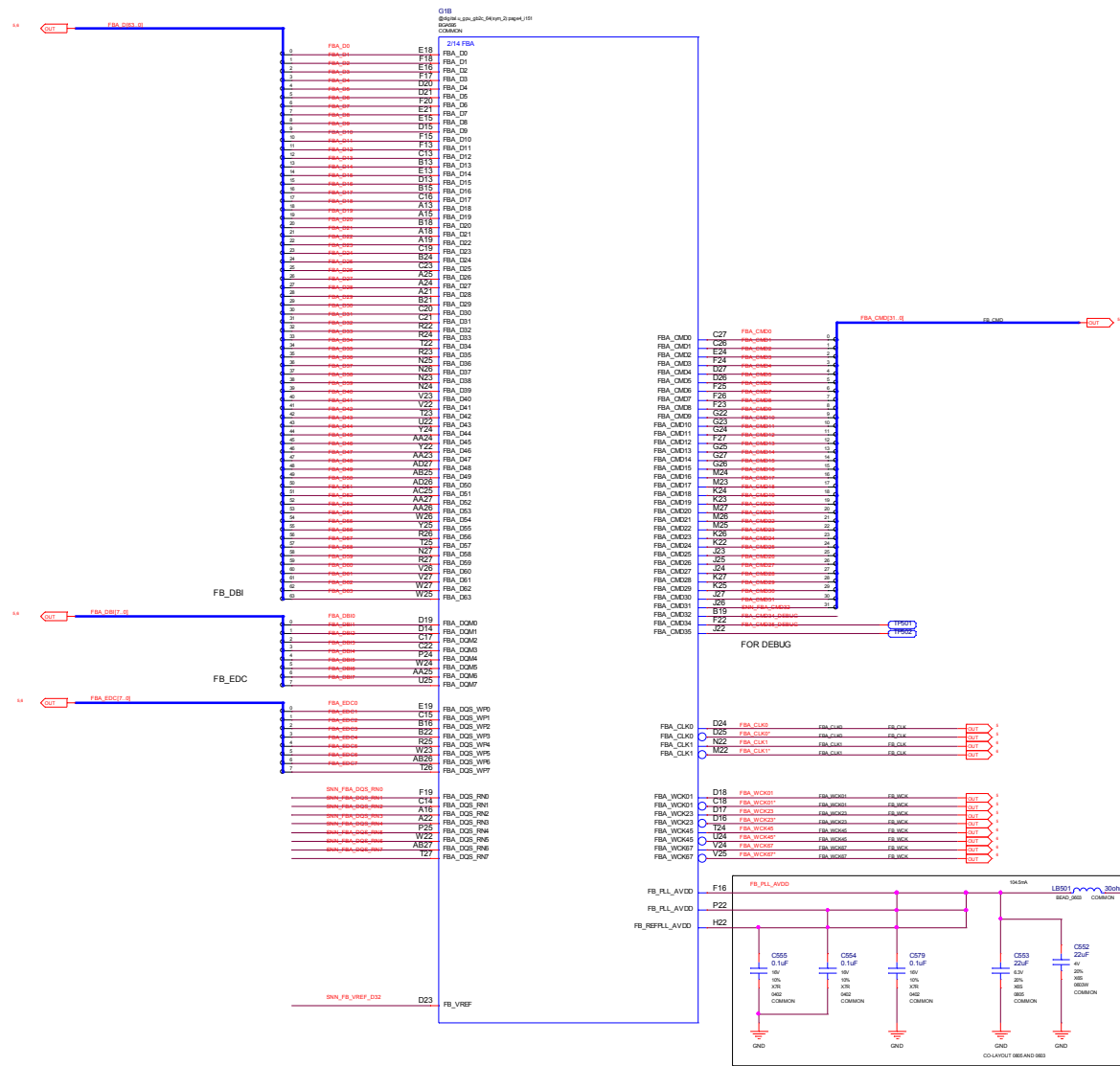
PCI Express



ASSEMBLY	ASSEMBLY DESCRIPTION	SANTA CLARA, CA 95050, USA		
PAGE DETAIL	PG Express			
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GPU Frame Buffer



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU Frame Buffer

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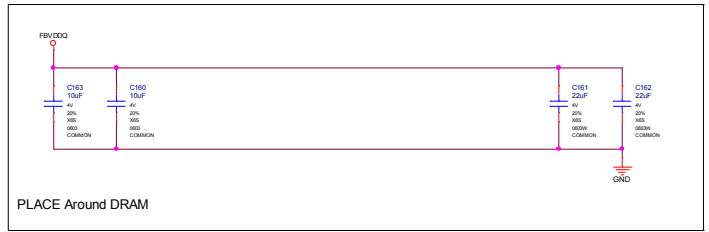
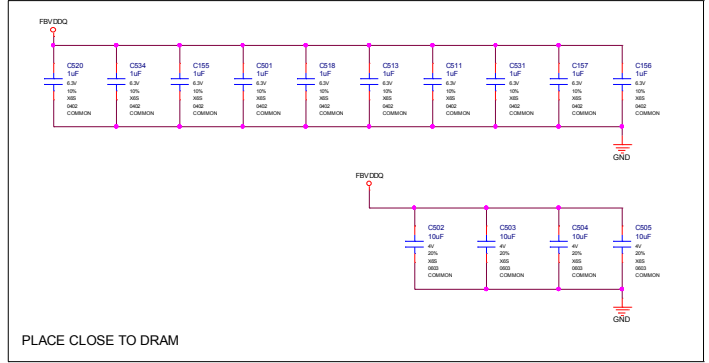
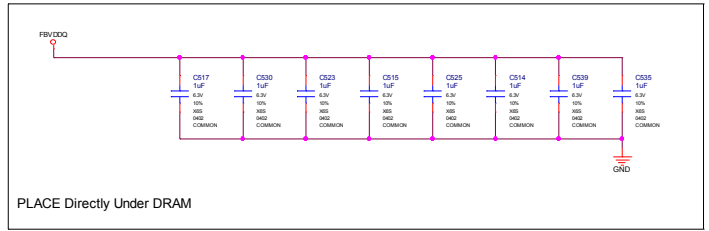
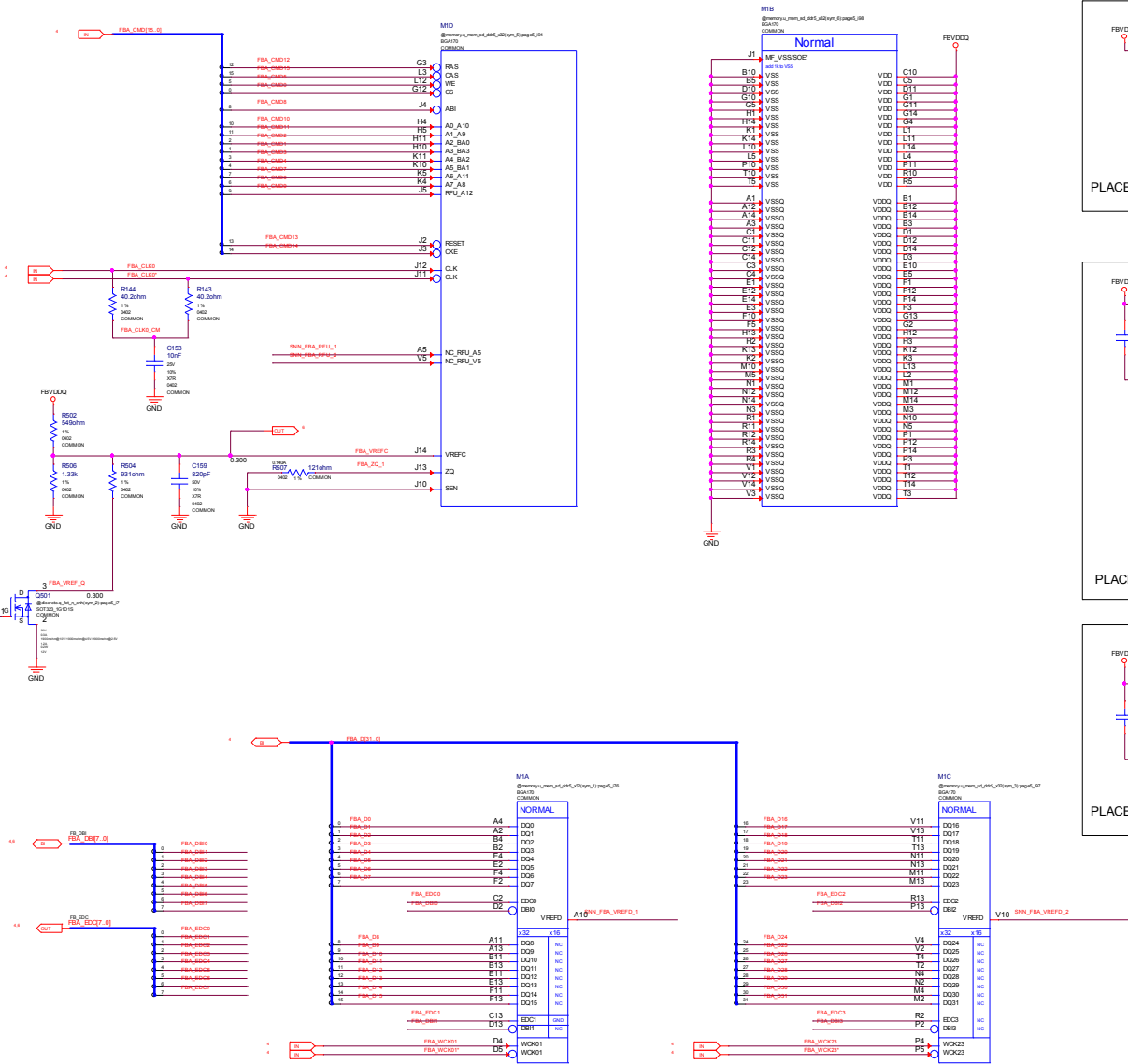


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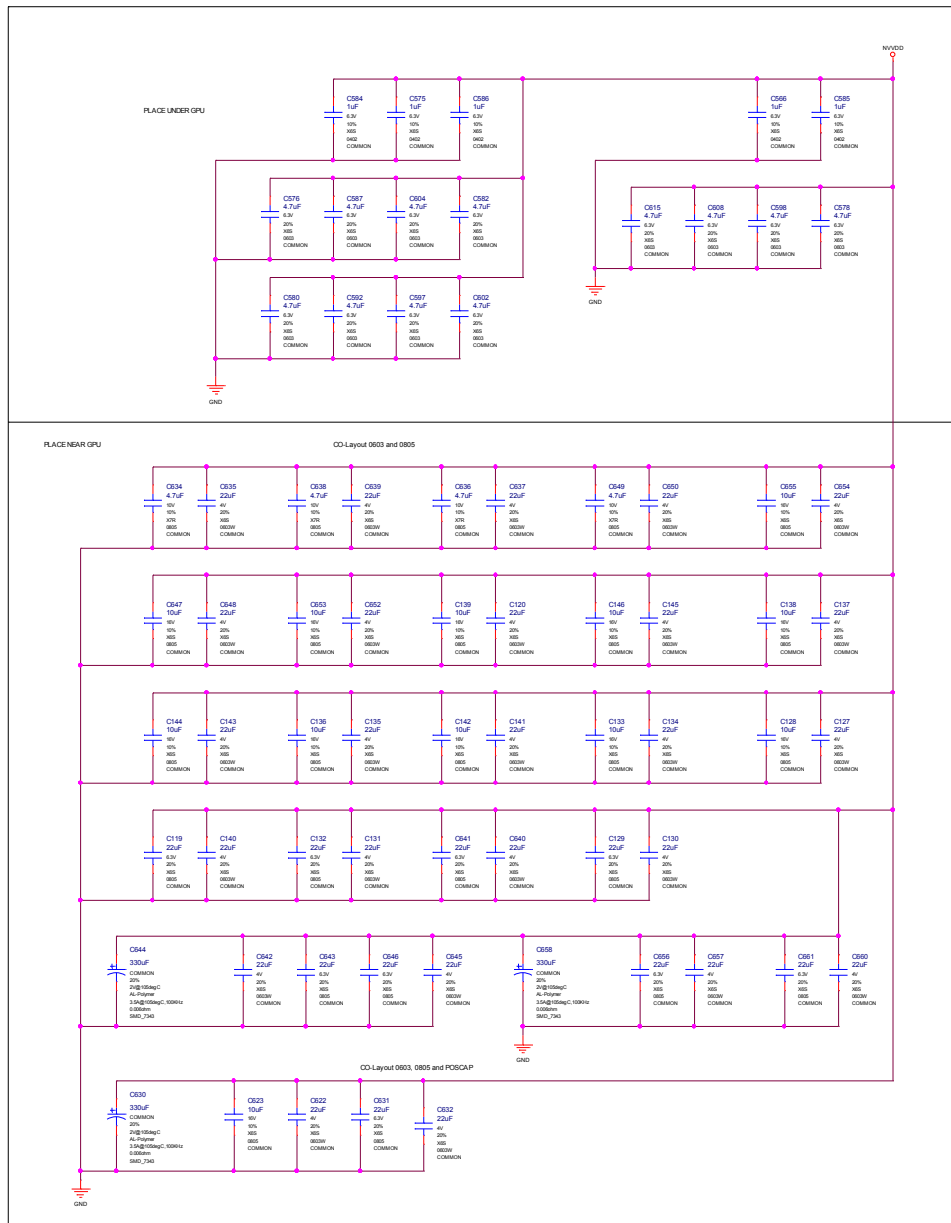
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FBA bits 31..00

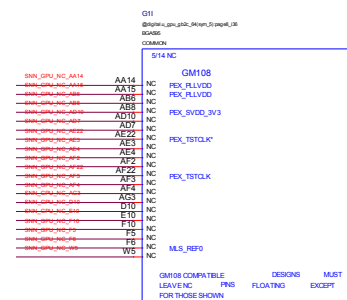
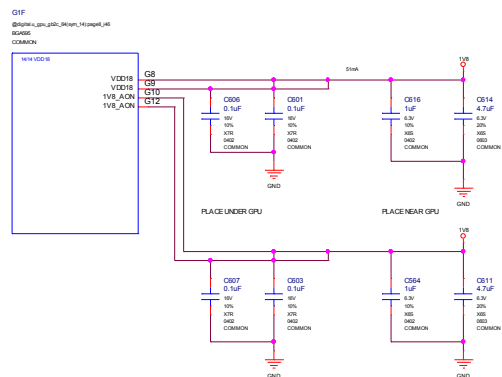
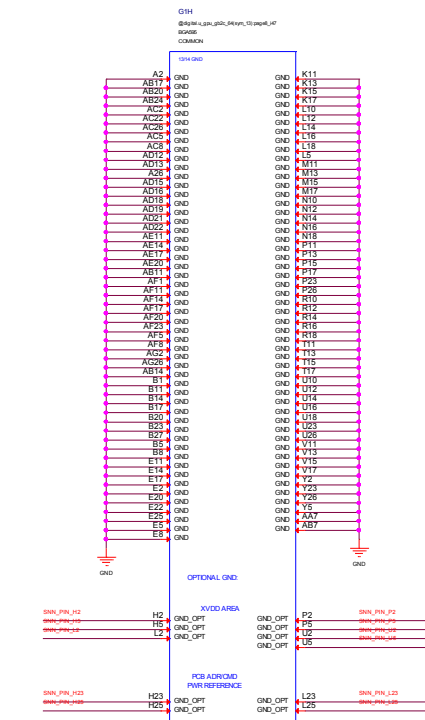
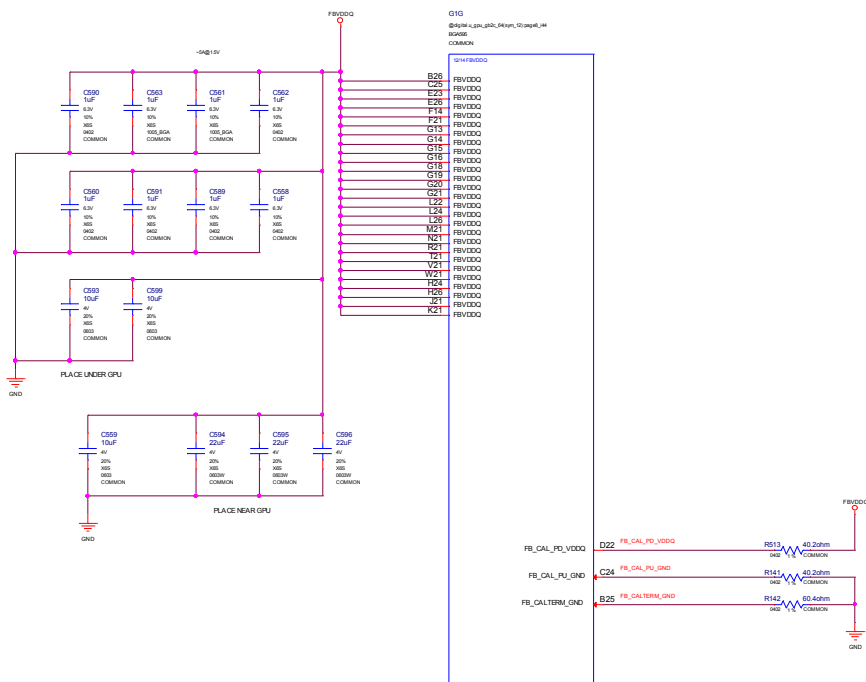
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CM01	A2	
CM02	A2_BA0	
CM03	A4_BA2	
CM04	A5_BA1	
CM05	WE*	
CM06	A7_AB	
CM07	AB*	
CM08	A12_RFU	
CM09	A0_A10	
CM10	A1_AB	
CM11	RA*	
CM12	RS*	
CM13	CS*	
CM14	CS*	
CM15	CS*	
CM16		CS*
CM17		A3_BA3
CM18		A2_BA0
CM19		A4_BA2
CM20		A5_BA1
CM21		WE*
CM22		A7_AB
CM23		A6_A11
CM24		A12_RFU
CM25		A0_A10
CM26		RA*
CM27		RS*
CM28		CS*
CM29		CS*
CM30		CS*
CM31		CS*



NVVVD Decoupling



FBVDDQ and 1V8 Decoupling



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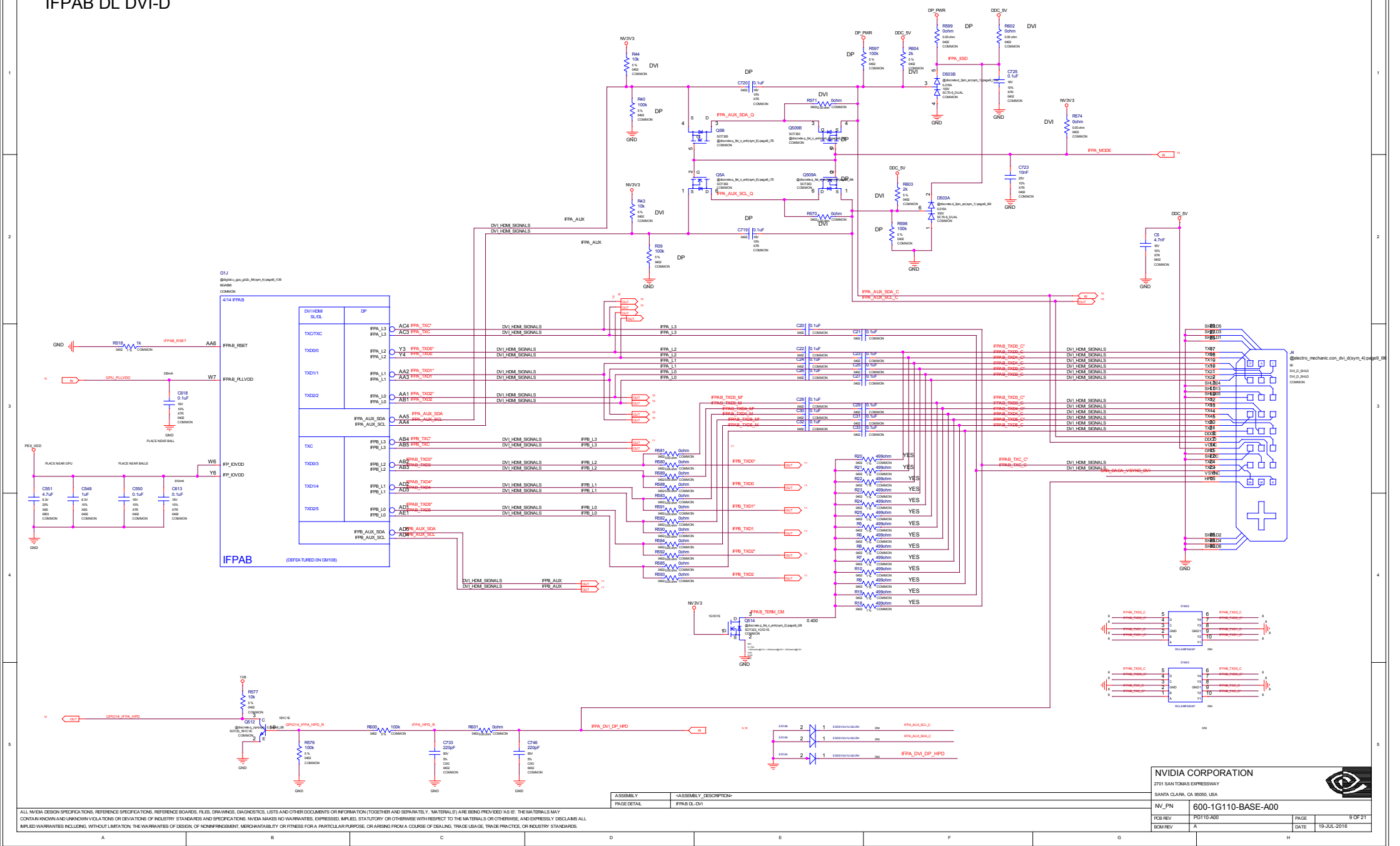
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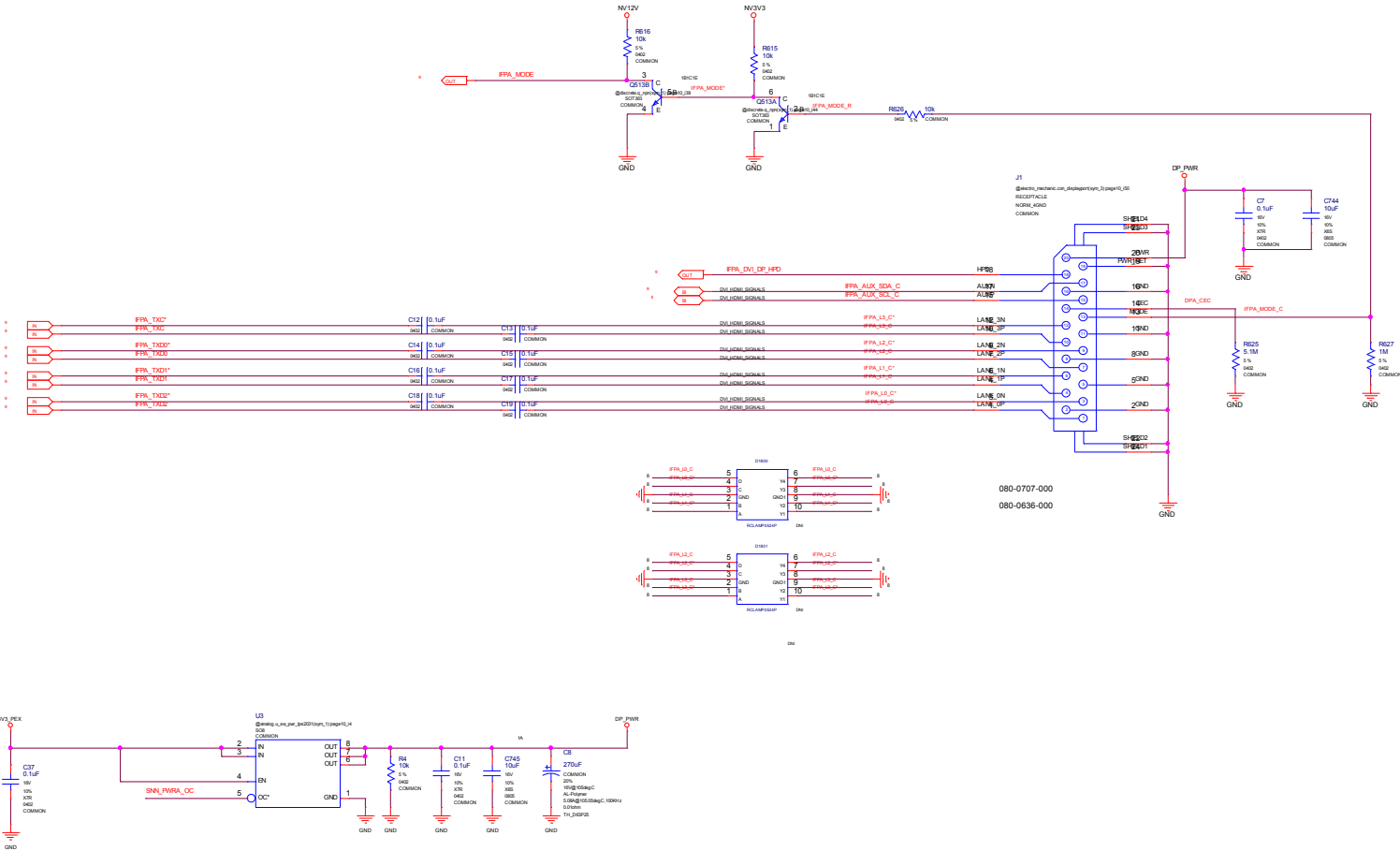
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	FBV/DDQ and 1V8 Decoupling

IFPAB DL DVI-D



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17ci203

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PAGE DETAIL	IFPA DP

IFPB HDMI/DP



Hotplug Detection



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPB DPHDMI

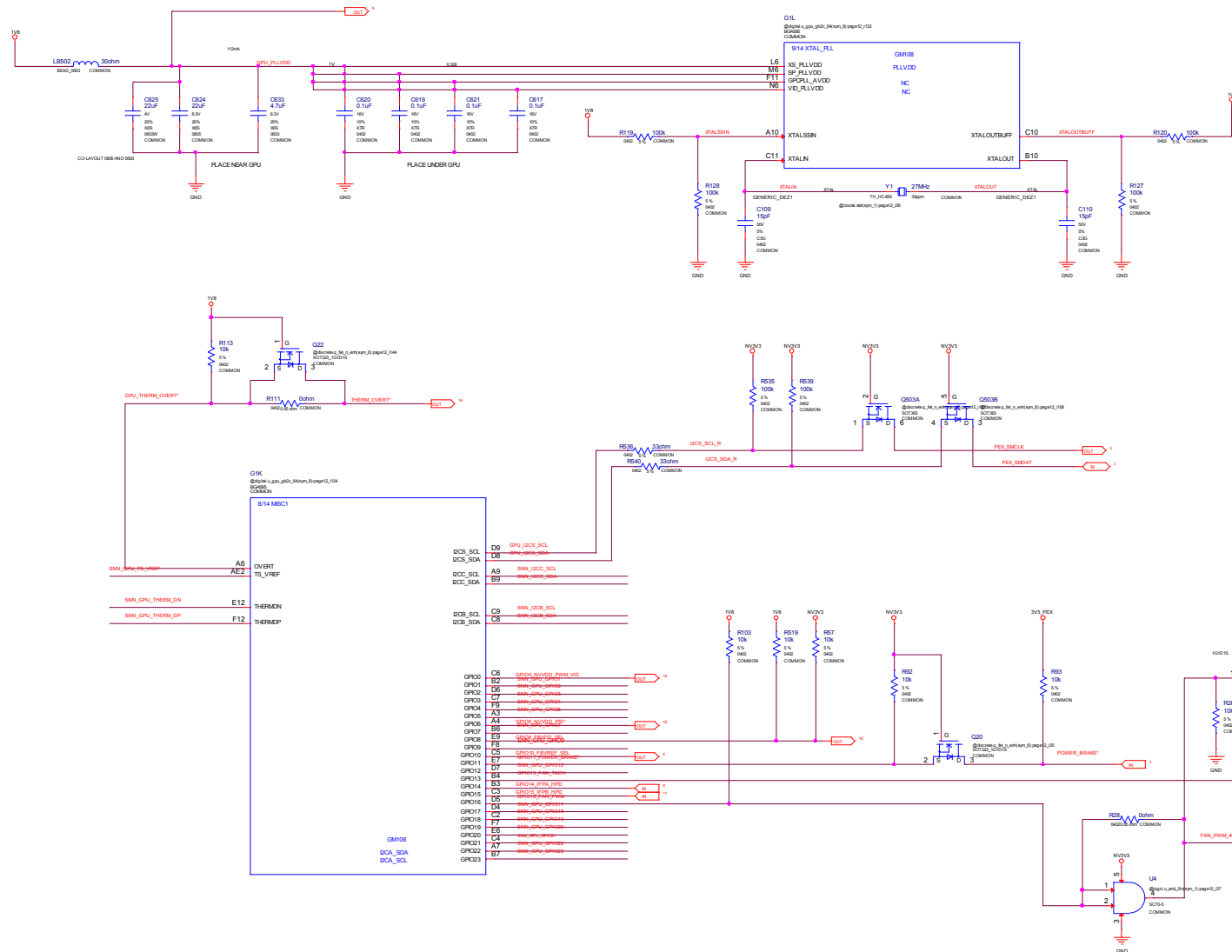
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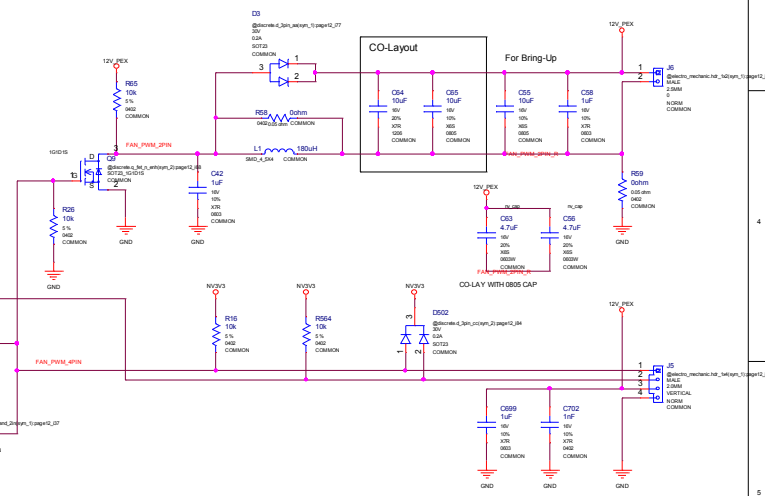
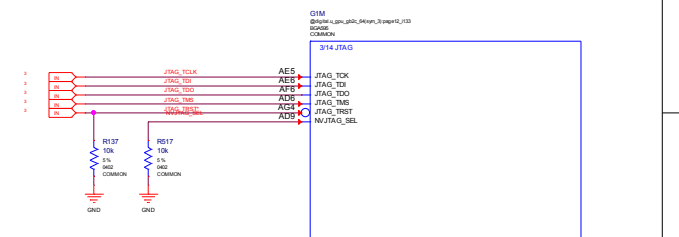
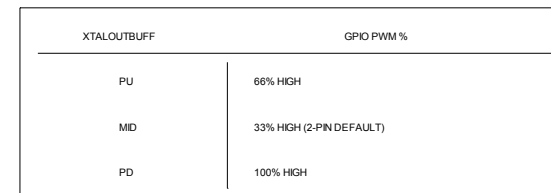
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JTAG,GPIO&XTAL



Smart Fan



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	JTAG,GPIOKXTAL

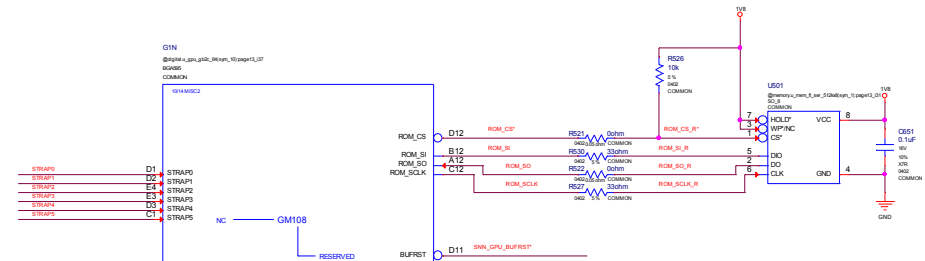
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ROM & STRAPS

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111	DEFAULT
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V



STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	DEFAULT
L	L	H	0001	
L	H	L	0010	
L	H	H	0011	
H	H	L	0110	
H	H	H	0111	
L	L	M	1000	
L	M	L	1001	

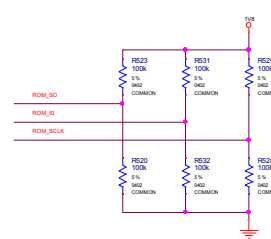
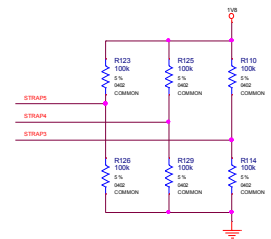
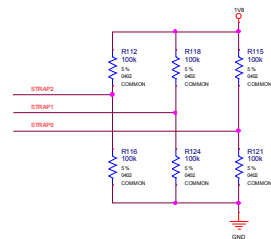
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M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

```
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE
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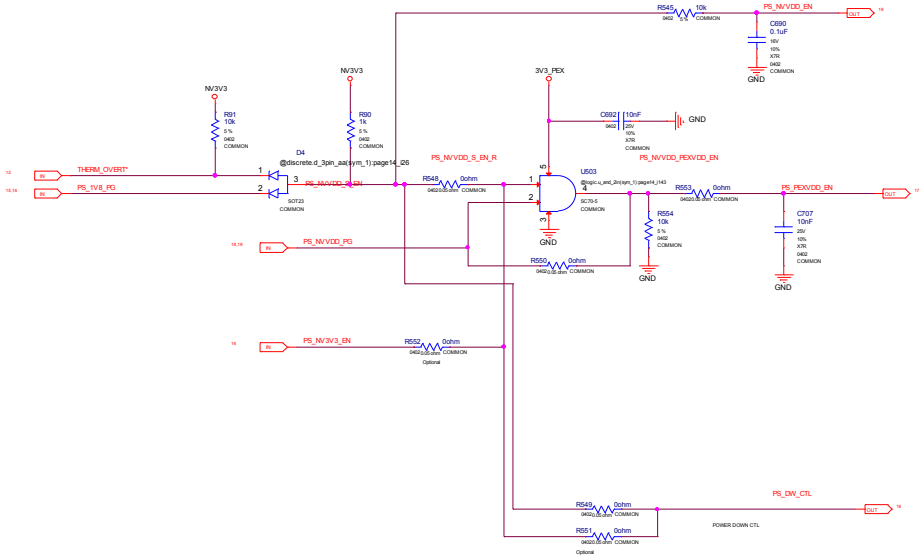
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Power Sequence



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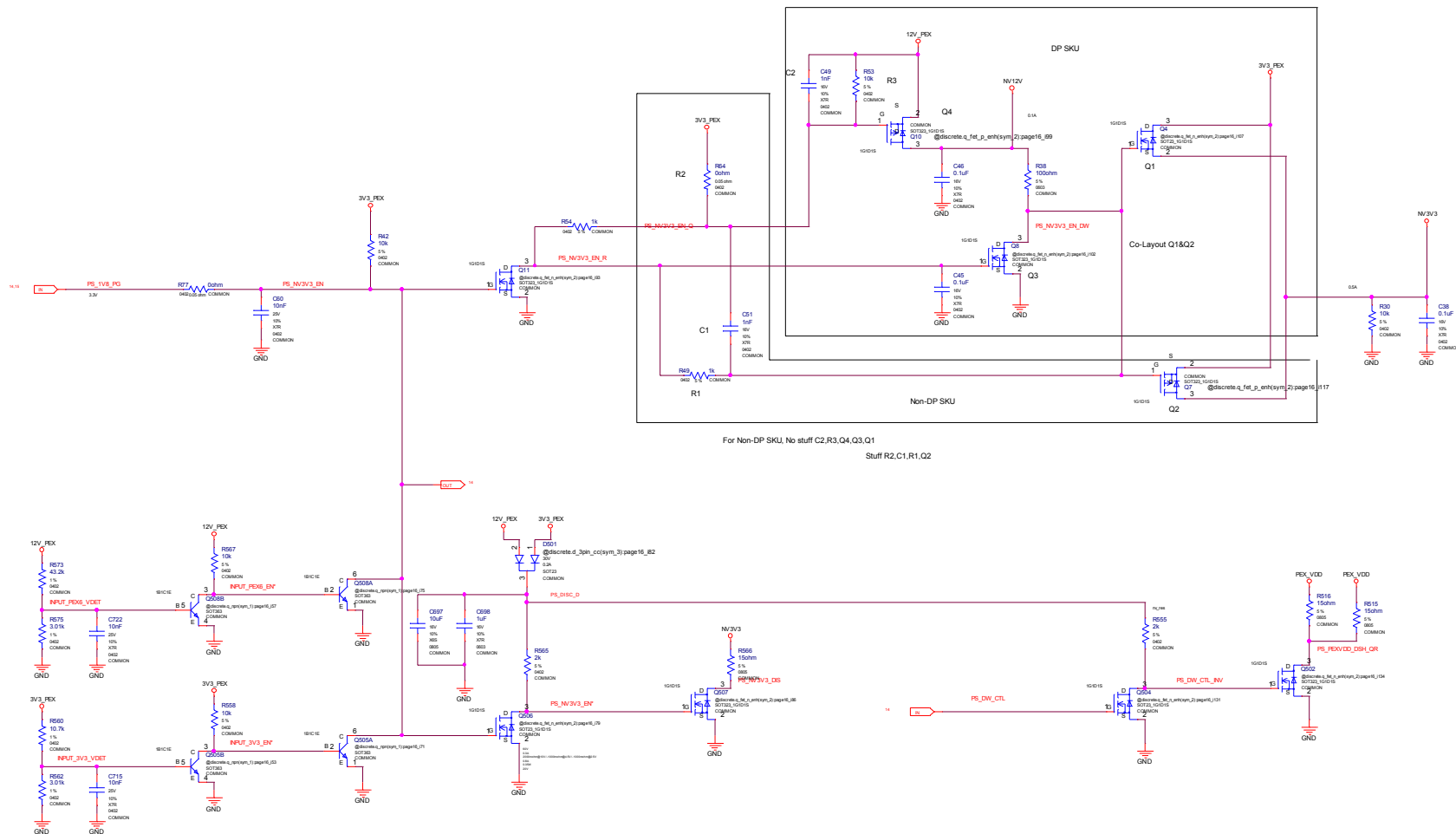
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PAGE DETAIL	Power Sequence

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POWER: NV3V3, NV12V



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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	POWER NV3V3, NV12V

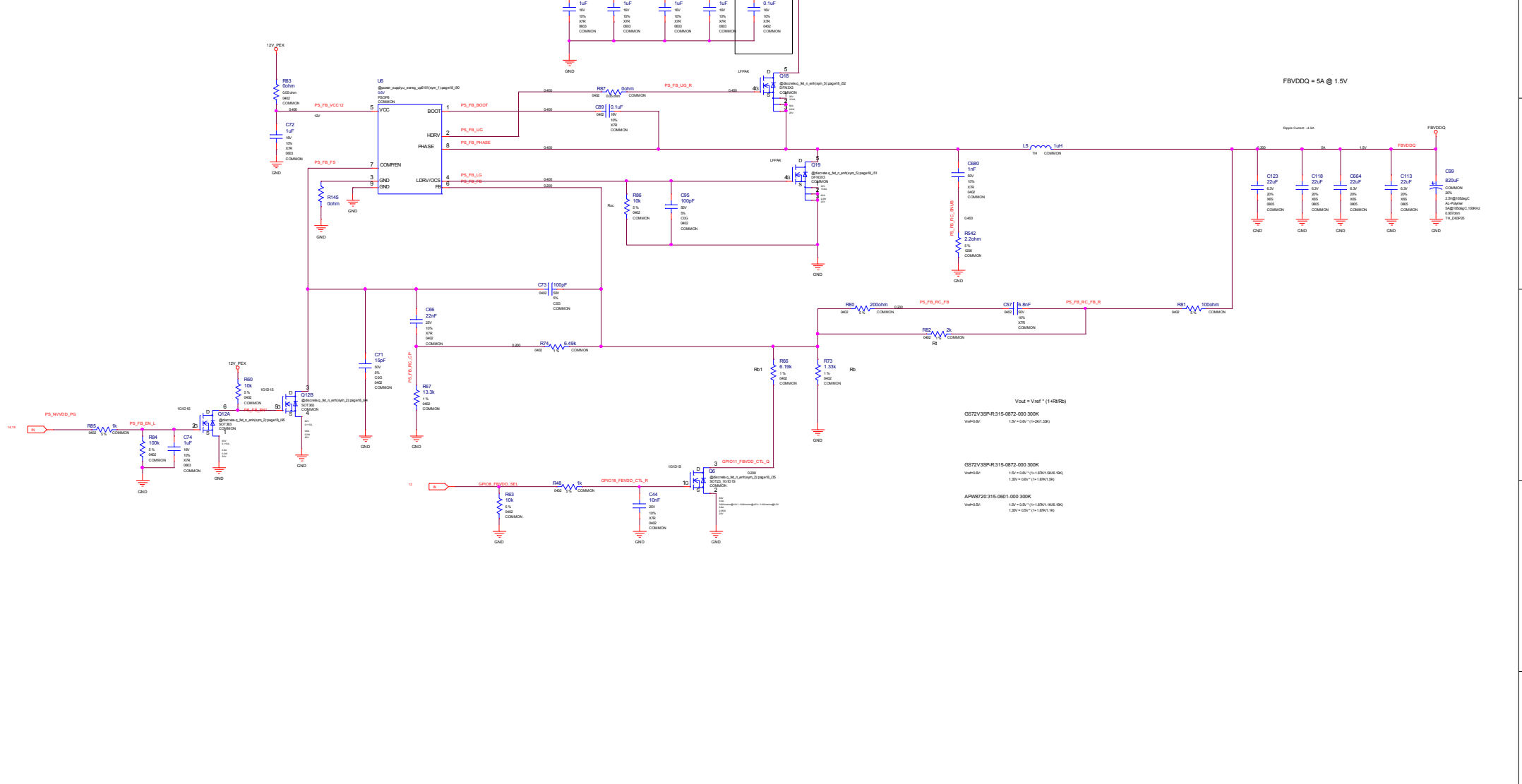


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PAGE DETAIL	POWER_PEX_VDD

NV_PN	600-1G110-BASE-A00
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A	B	C	D	E	F	G	H
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PAGE DETAIL	POWER RIVDDQ		NV PN	600-1G110-BASE-A00

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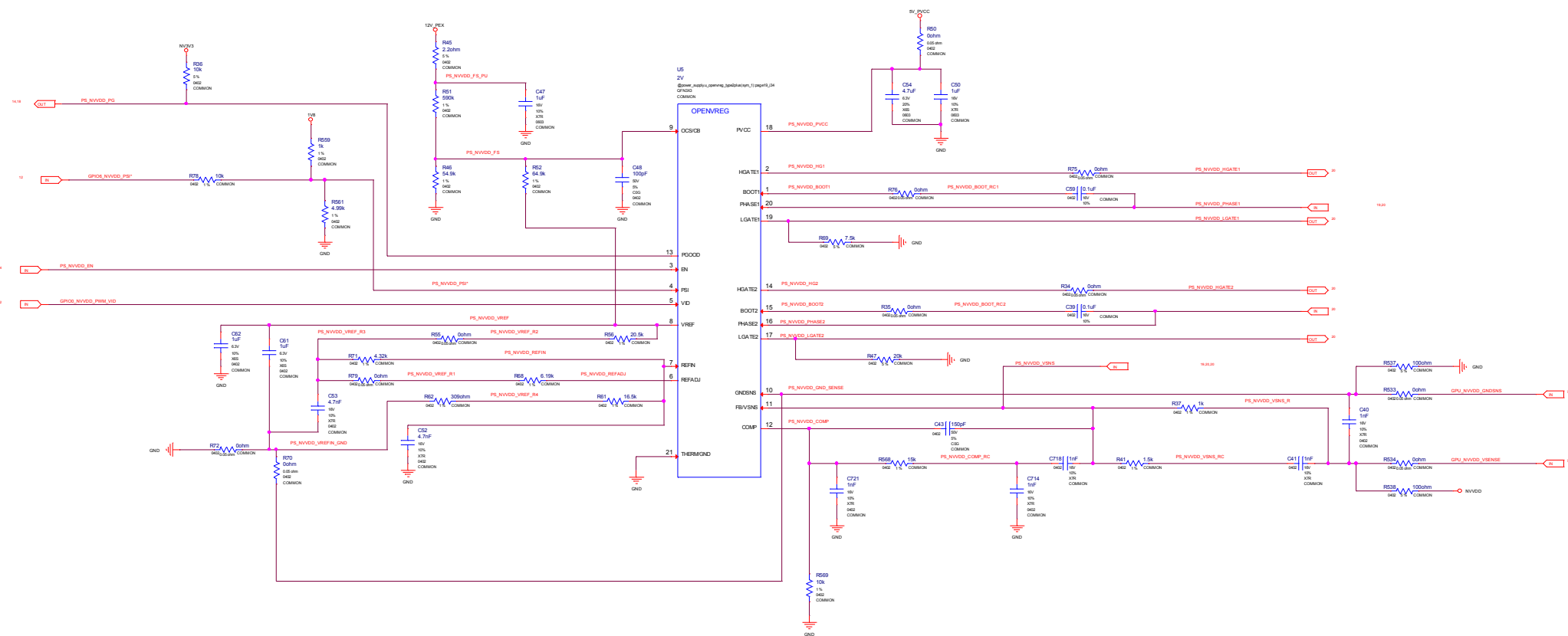


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A horizontal number line with several tick marks. A vertical line segment is drawn from the second tick mark to the right, labeled 'H'.

POWER:NVVDD



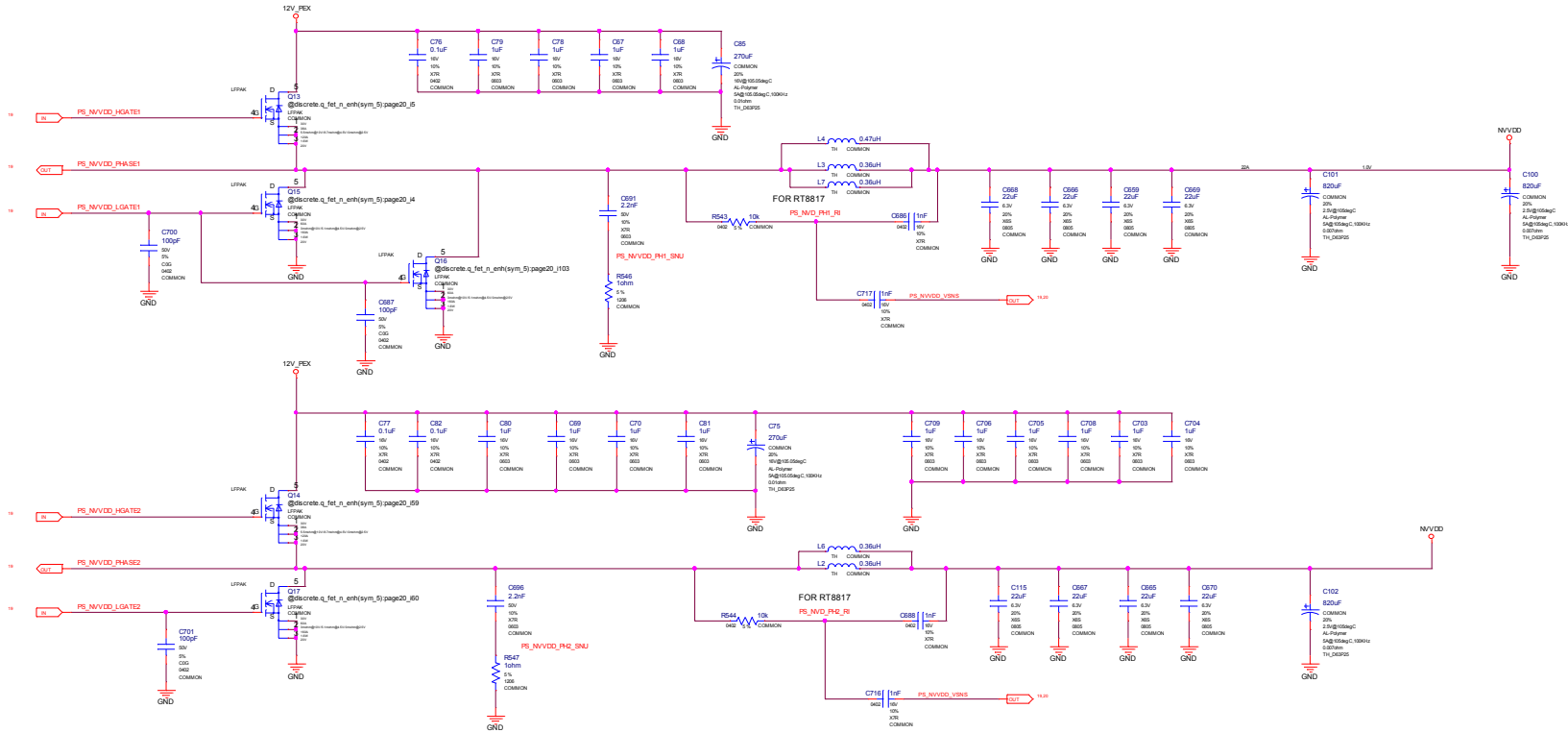
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ASSEMBLY	<ASSEMBLY_DESCRIPTION
PAGE DETAIL	POWER NVDD

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POWER:NVVDD

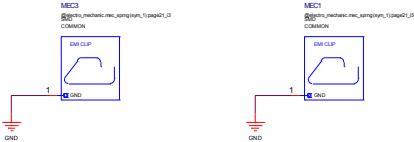
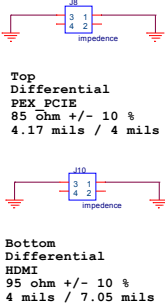
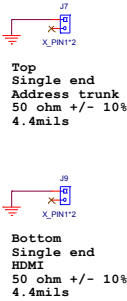
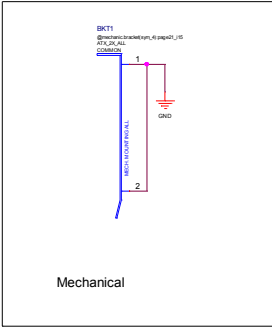
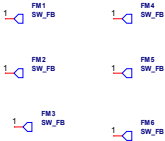


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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	POWER:NVVDD

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NV_PN	600-1G110-BASE-A00		
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