

PG210 B00

GP107 128b GDDR5, 75W , PCB 5.7"
DVI-D_DL (DP + DP) + HDMI (DP) + DP

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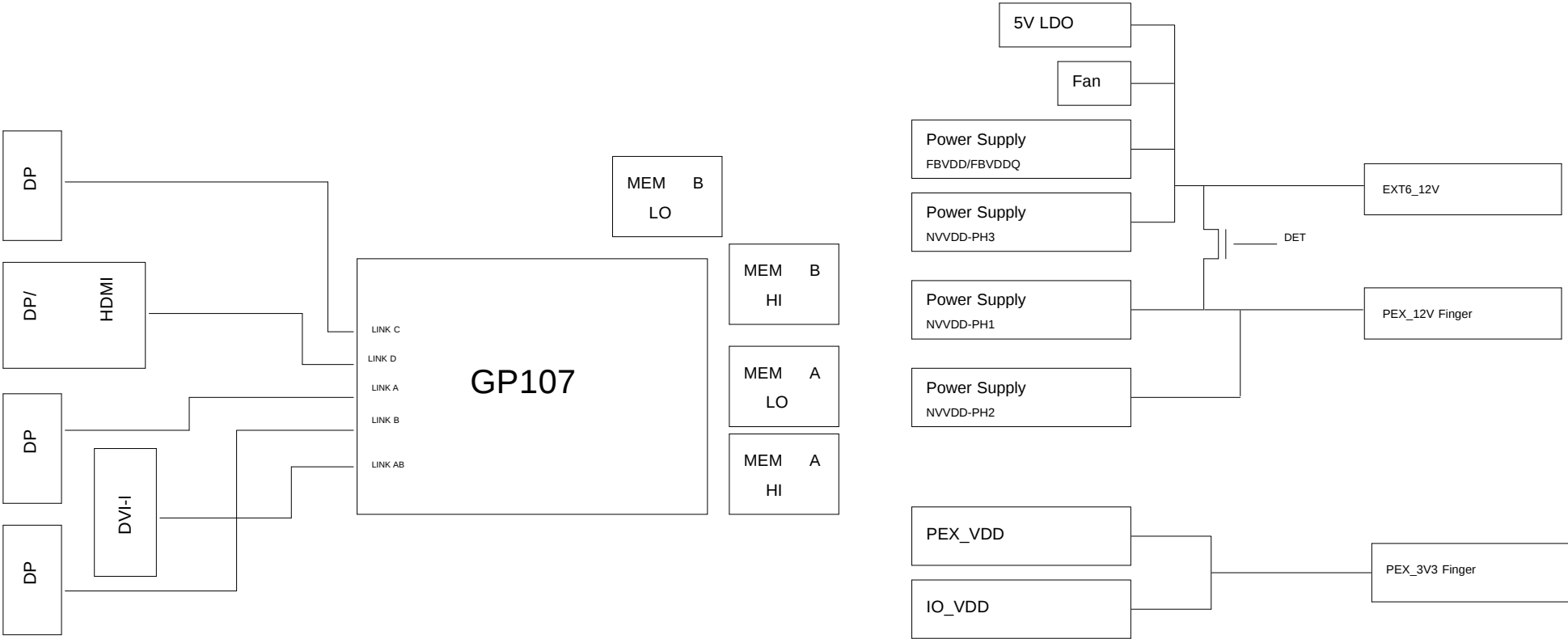
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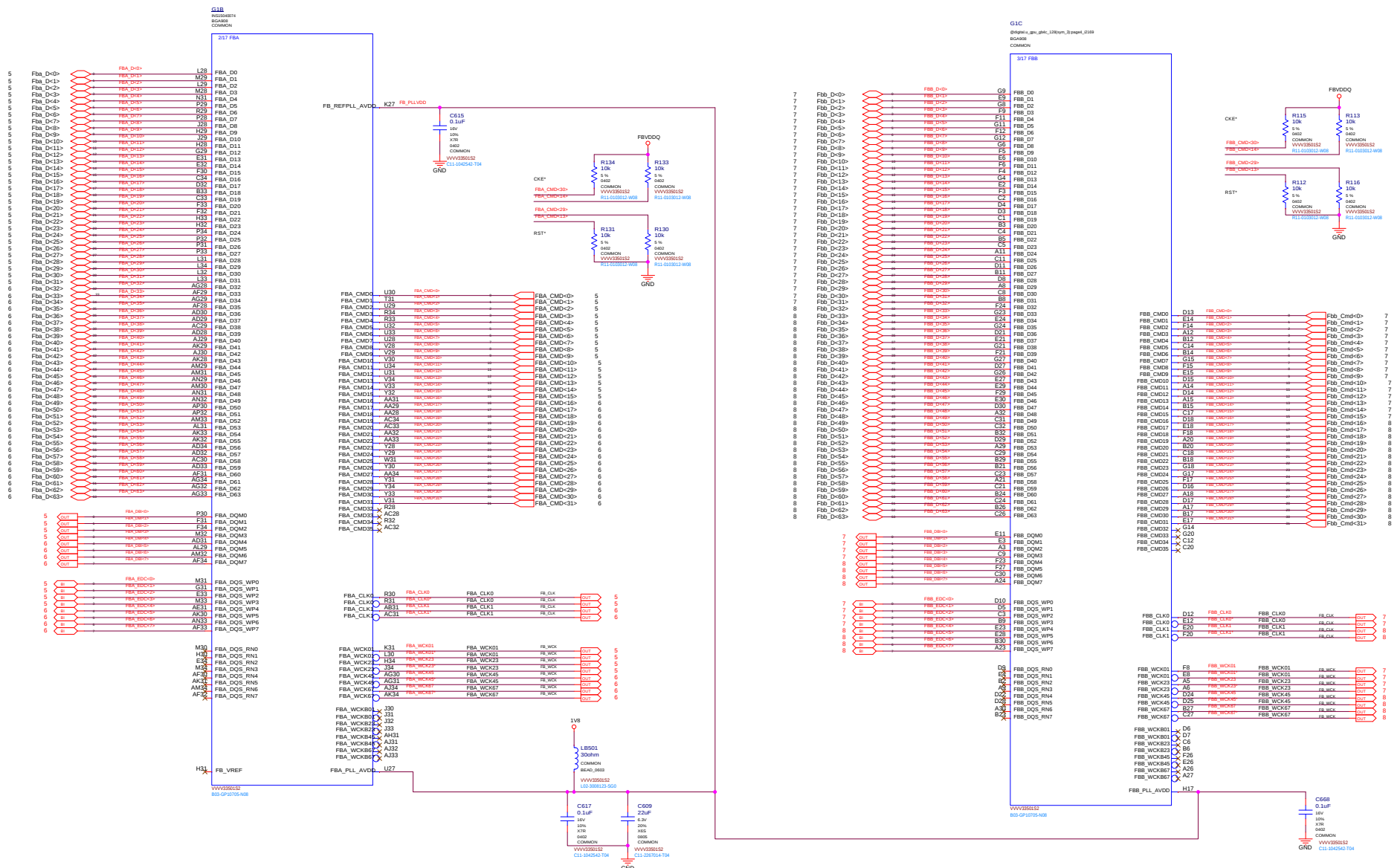
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1	No change

Block Diagram



MEMORY: GPU Partition A/B



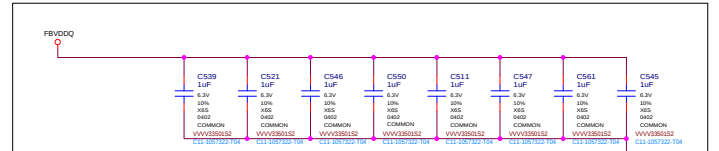
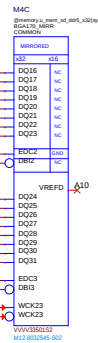
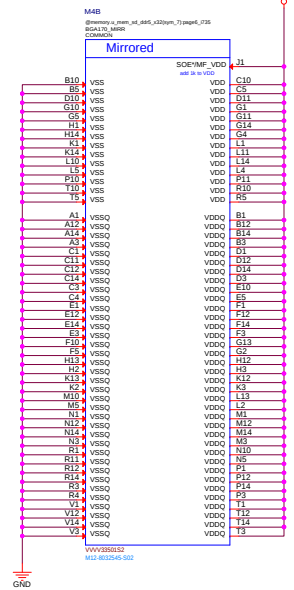
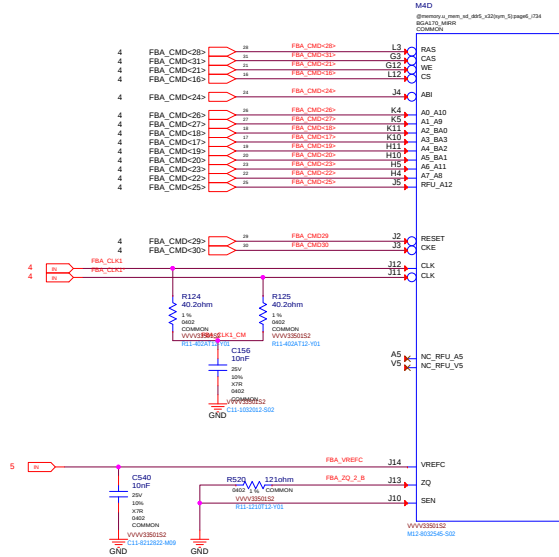
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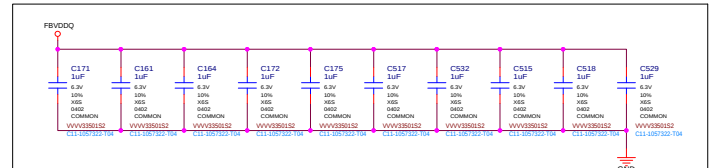
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MEMORY: FBA Partition 63..32

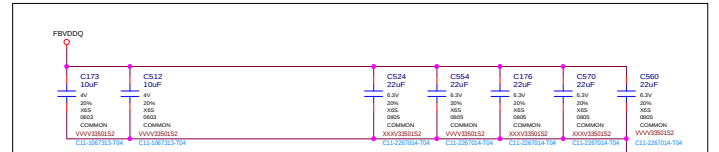
CMD	0..31	32..63
CMD0	CP	CS*
CMD1	A0_BA3	A0_BA3
CMD2	A2_BA0	A2_BA0
CMD3	A0_BA3	A0_BA3
CMD4	A0_BA3	A0_BA3
CMD5	WE*	WE*
CMD6	A7_AB	A7_AB
CMD7	AB_A11	AB_A11
CMD8	AB*	AB*
CMD9	A12_RFU	A12_RFU
CMD10	A0_A10	A0_A10
CMD11	A1_AB	A1_AB
CMD12	RAS*	RAS*
CMD13	RST*	RST*
CMD14	CKE*	CKE*
CMD15	10uF	10uF
CMD16		
CMD17		
CMD18		
CMD19		
CMD20		
CMD21		
CMD22		
CMD23		
CMD24		
CMD25		
CMD26		
CMD27		
CMD28		
CMD29		
CMD30		
CMD31		



PLACE Directly Under DRAM

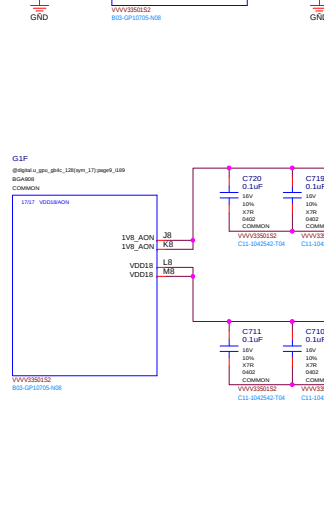
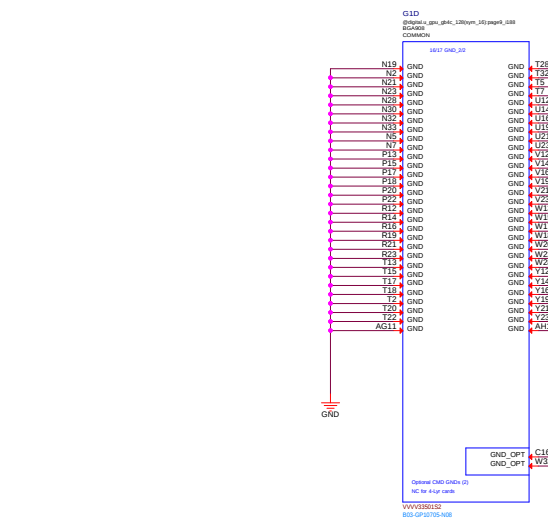
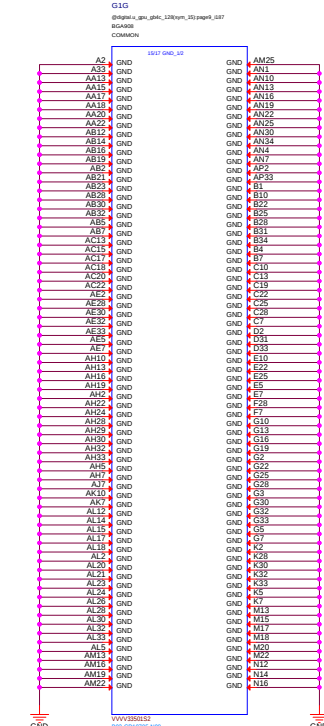
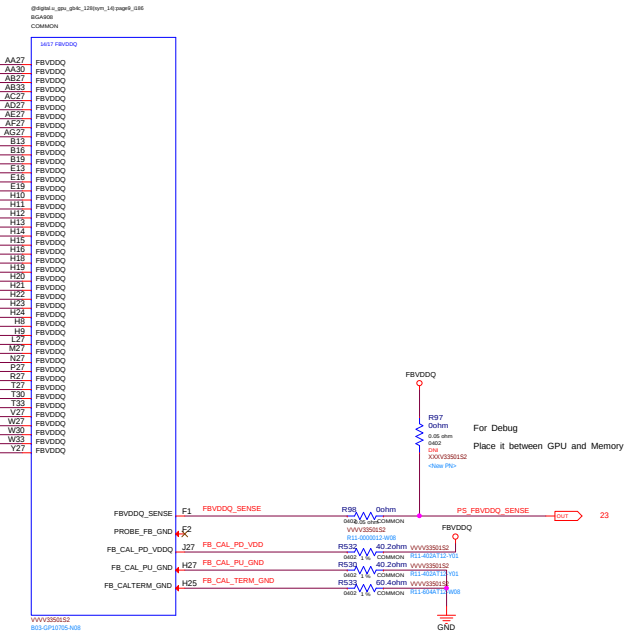
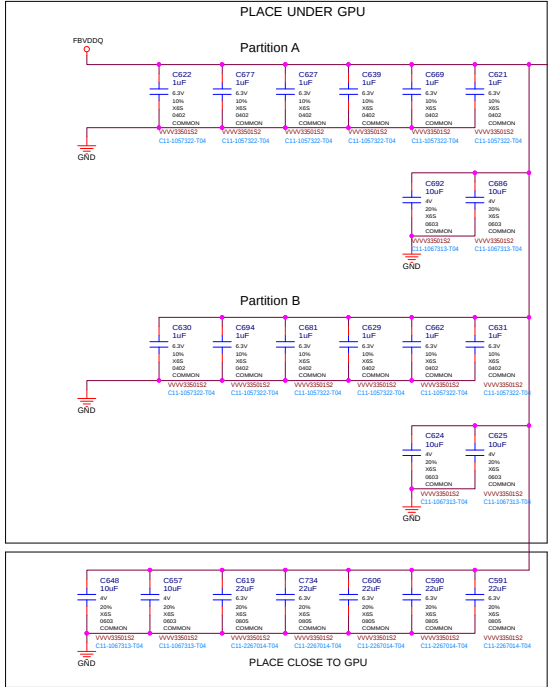


PLACE AT THE PACKAGE KEEPOUT/PERIMETER OF THE DRAM

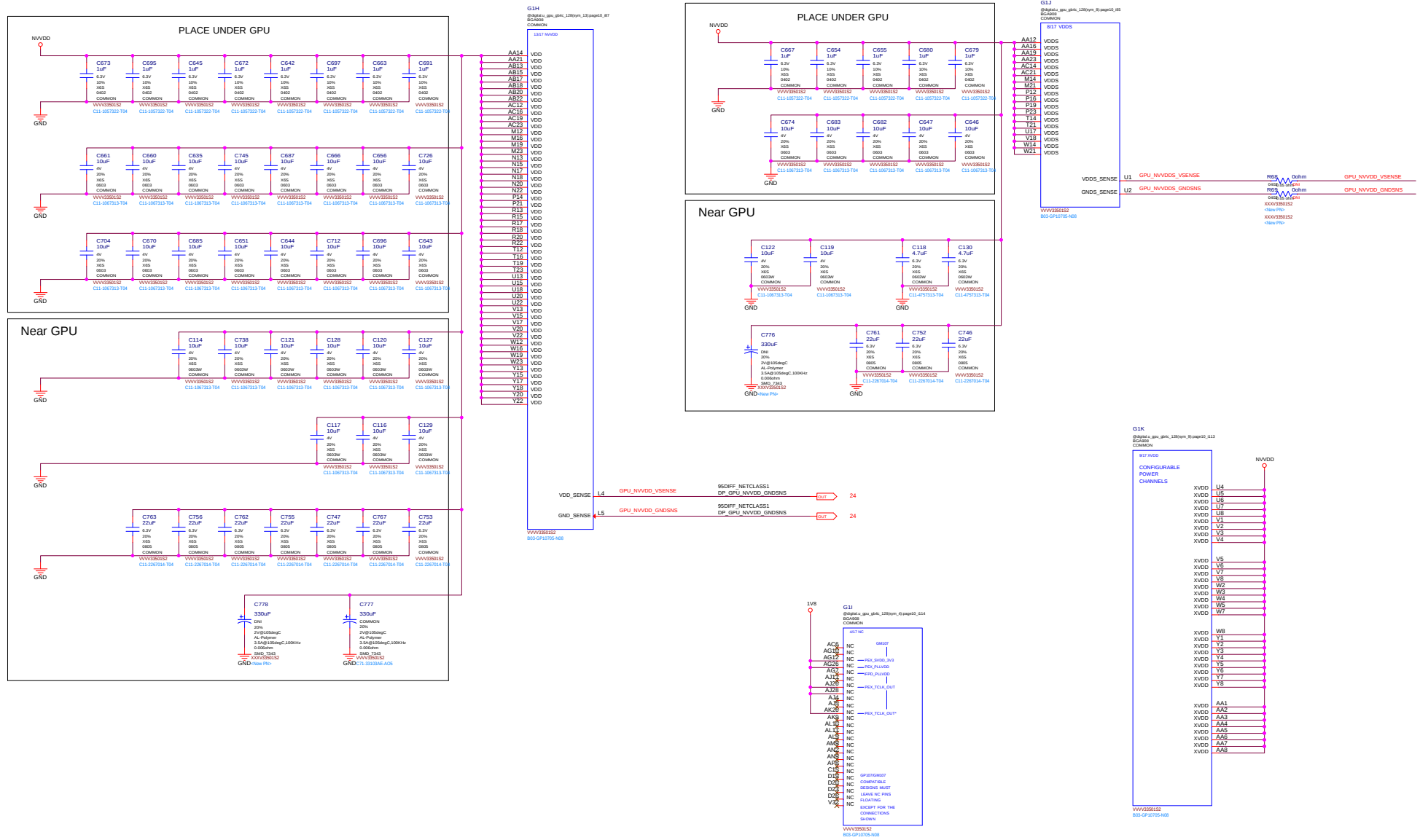


PLACE Around DRAM

GPU FBVDDQ & 1V8 Decoupling



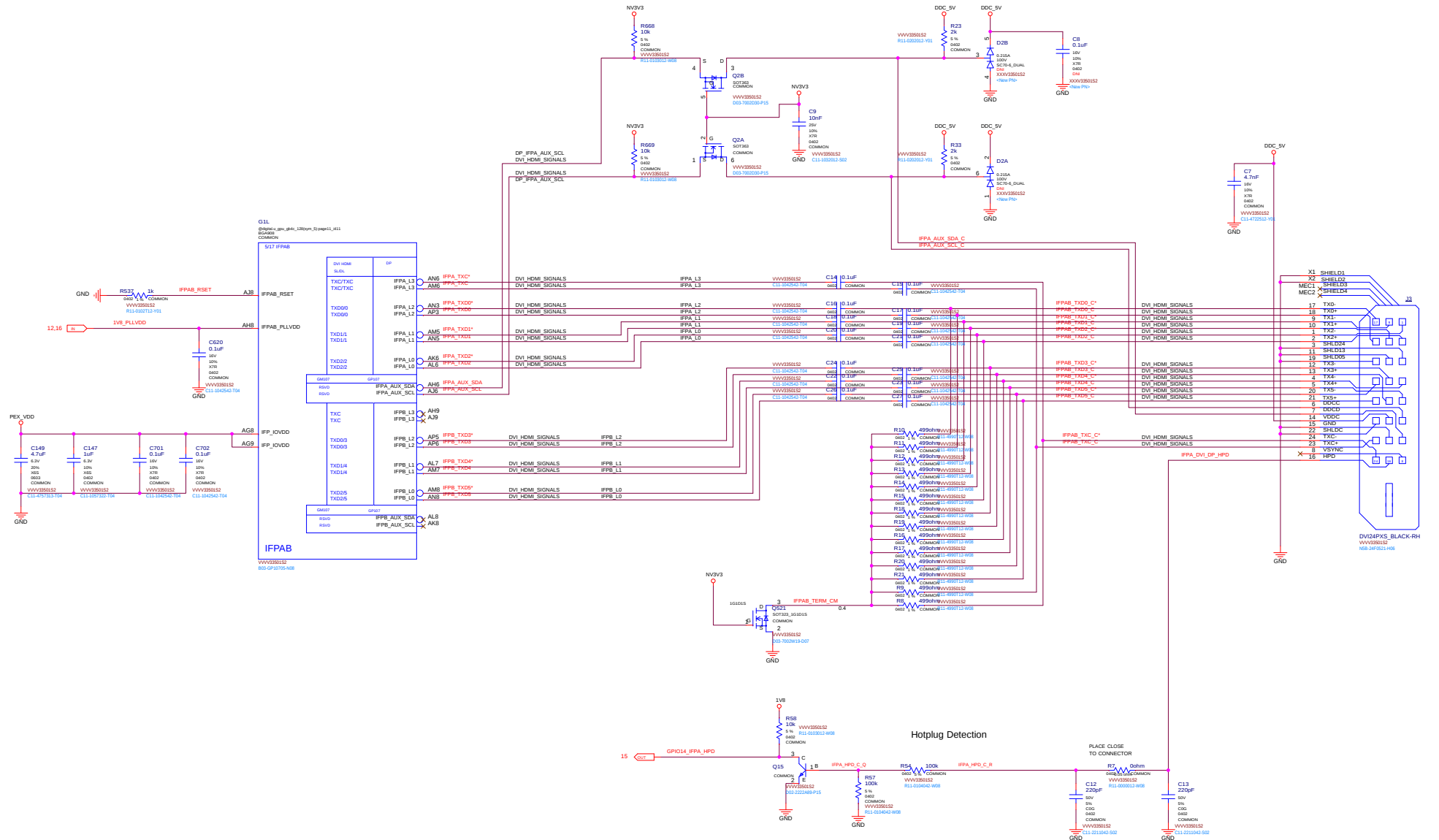
GPU NVVDD & NVVDDS Decoupling



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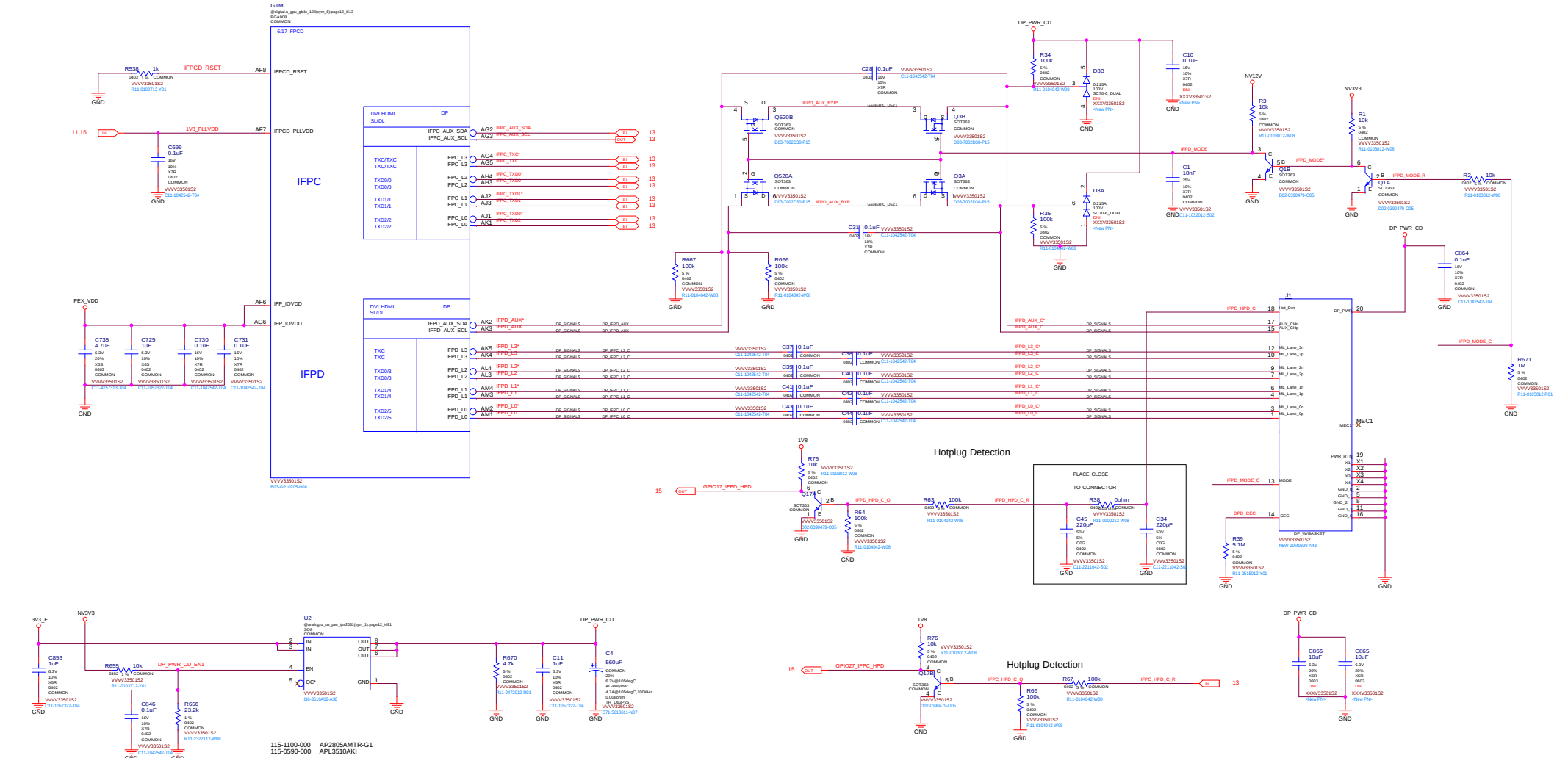
IFPAB DVI-DL



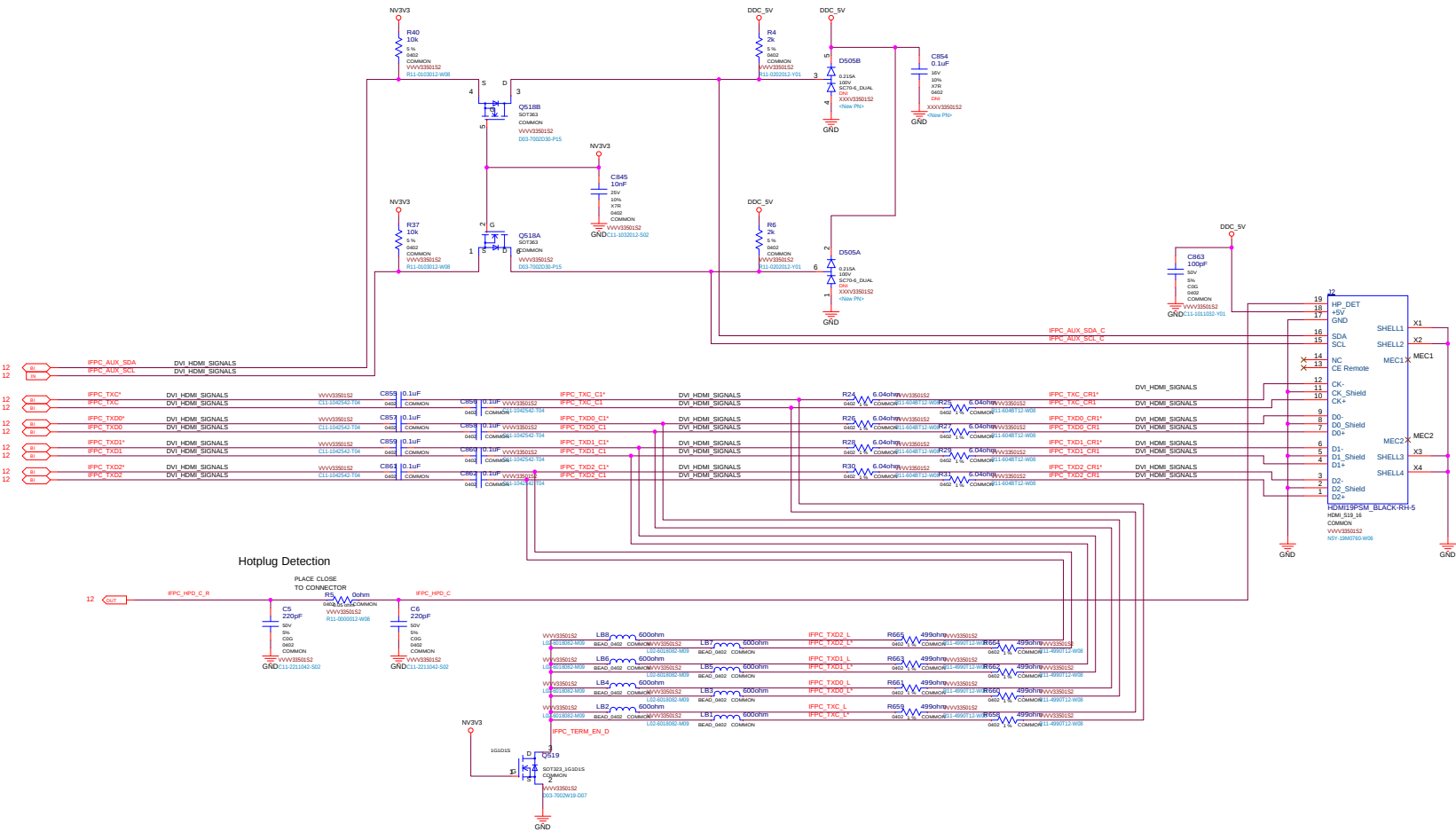
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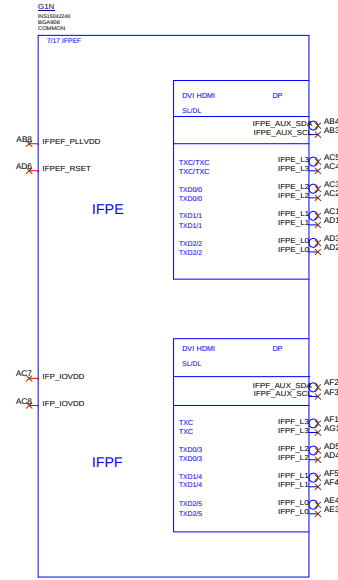
IFPD DP



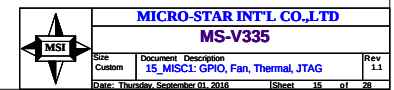
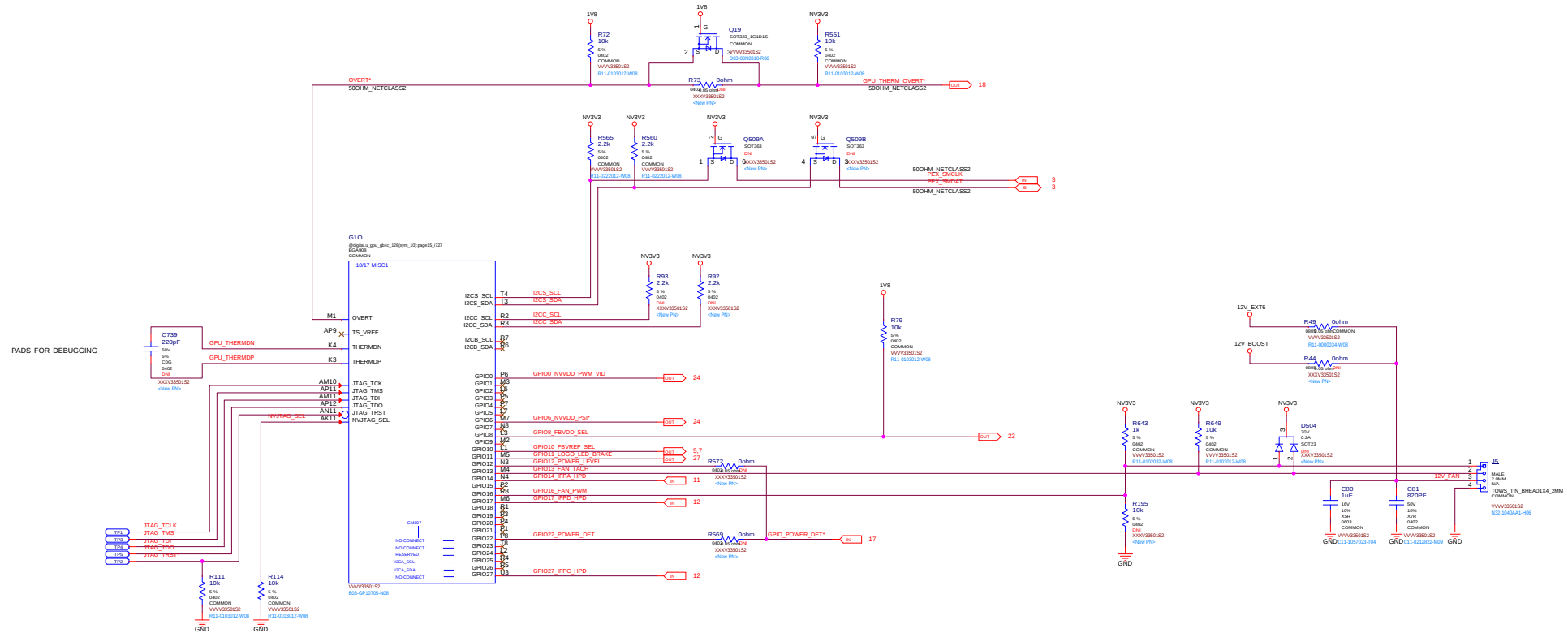
IFPC HDMI



IFPEF UNUSED



MISC1: GPIO, Fan, Thermal, JTAG

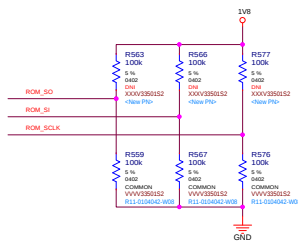


MISC2: ROM, XTAL, Straps

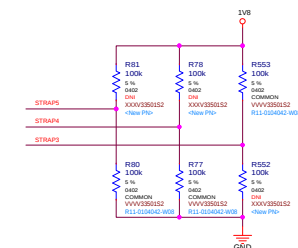
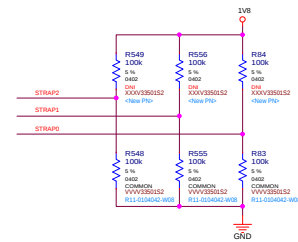
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111	Default
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	Samsung B-Die 8Gb 256Mx32
L	L	H	0001	Micron F-Die 8Gb 256Mx32
L	H	L	0010	Hynix M-Die 8Gb 256Mx32
L	H	H	0011	
H	H	L	0110	Hynix A-Die 4Gb 128Mx32
H	H	H	0111	Samsung E-Die 4Gb 128Mx32
L	L	M	1000	Micron B-Die 4Gb 128Mx32
L	M	L	1001	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0



H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

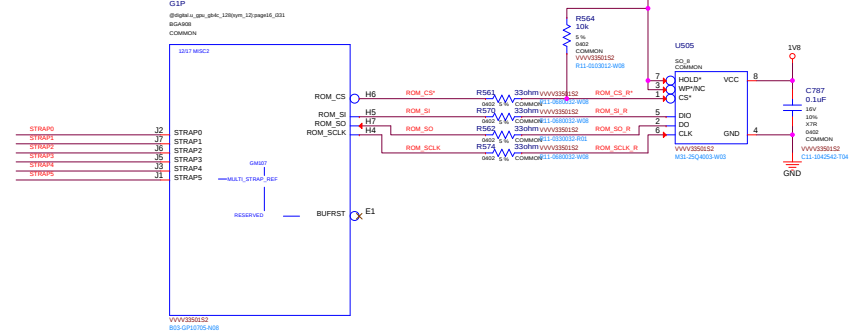


1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

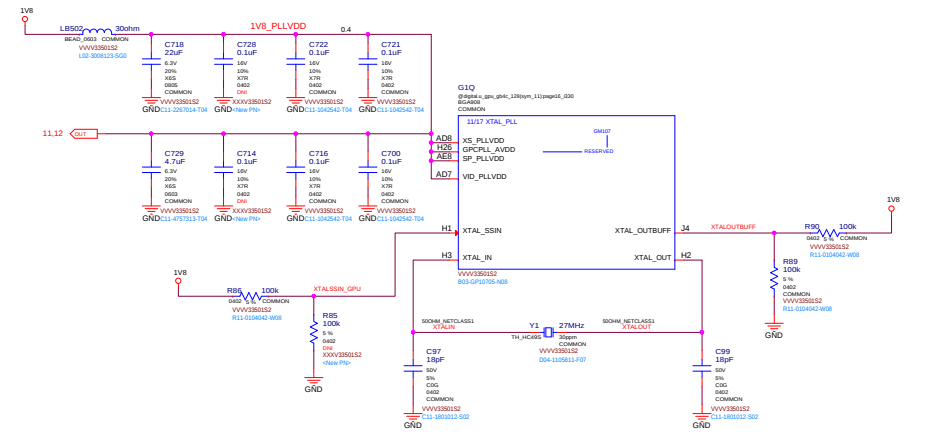
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

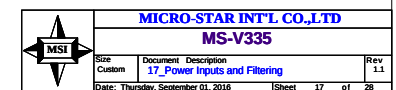
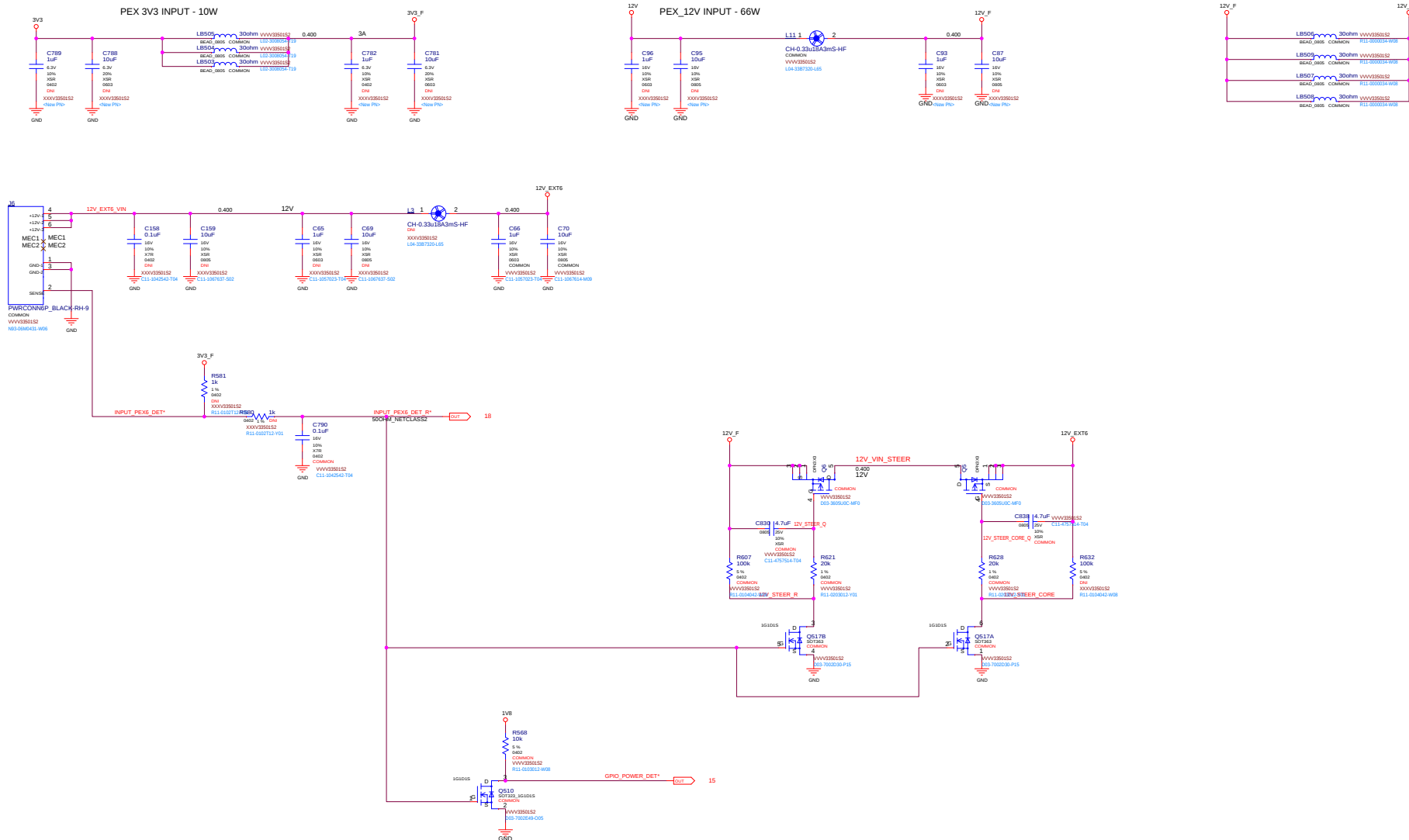


Smart Fan

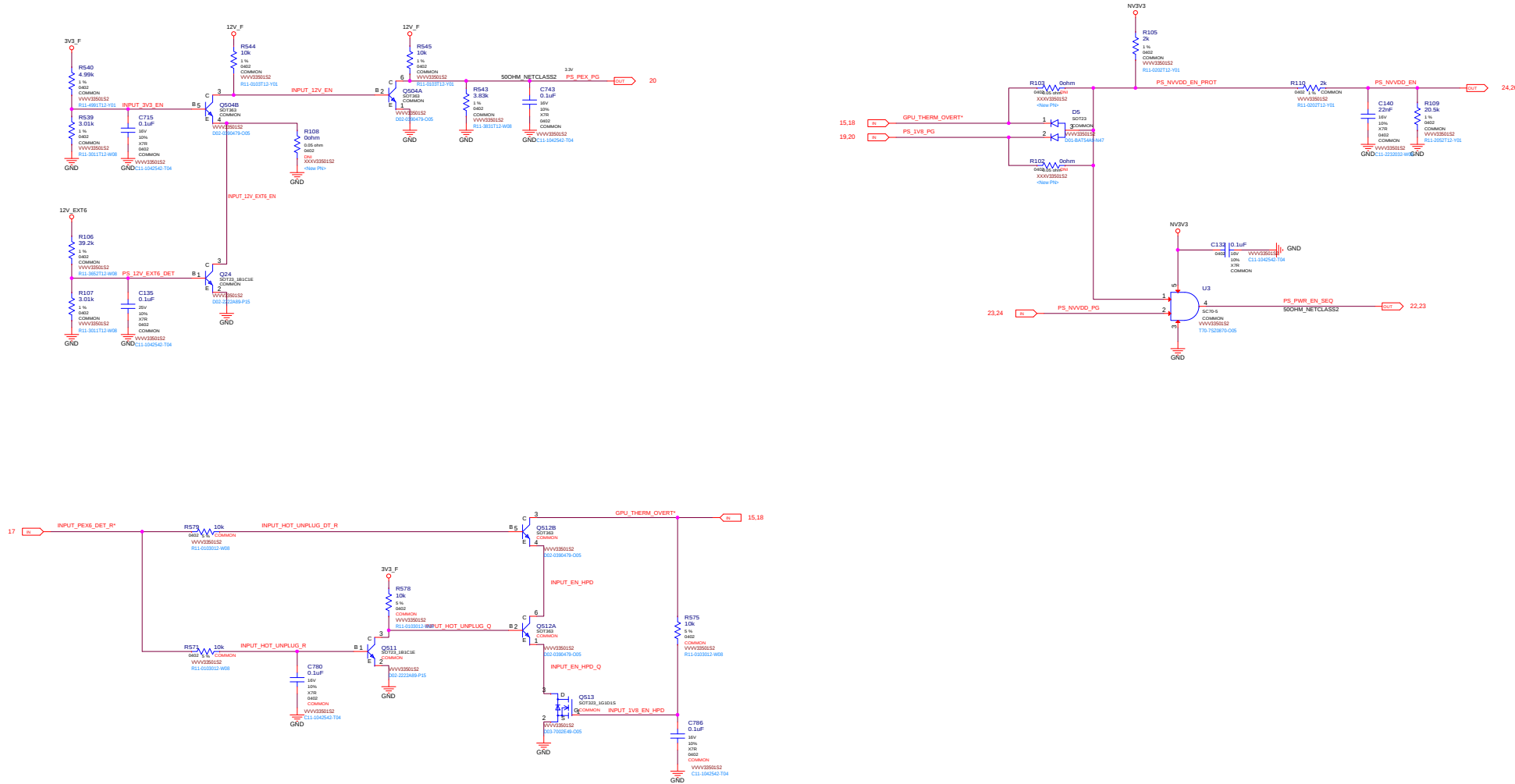
XTALOUTBUFF	Volatge	SmartFan PWM	GPIO/PWM at the FAN
Low	0V	GPIO Disabled	100%
Middle	0.9V	66% PWM	33% PWM (Typical)
High	1.8V	33% PWM	66% PWM



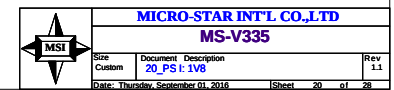
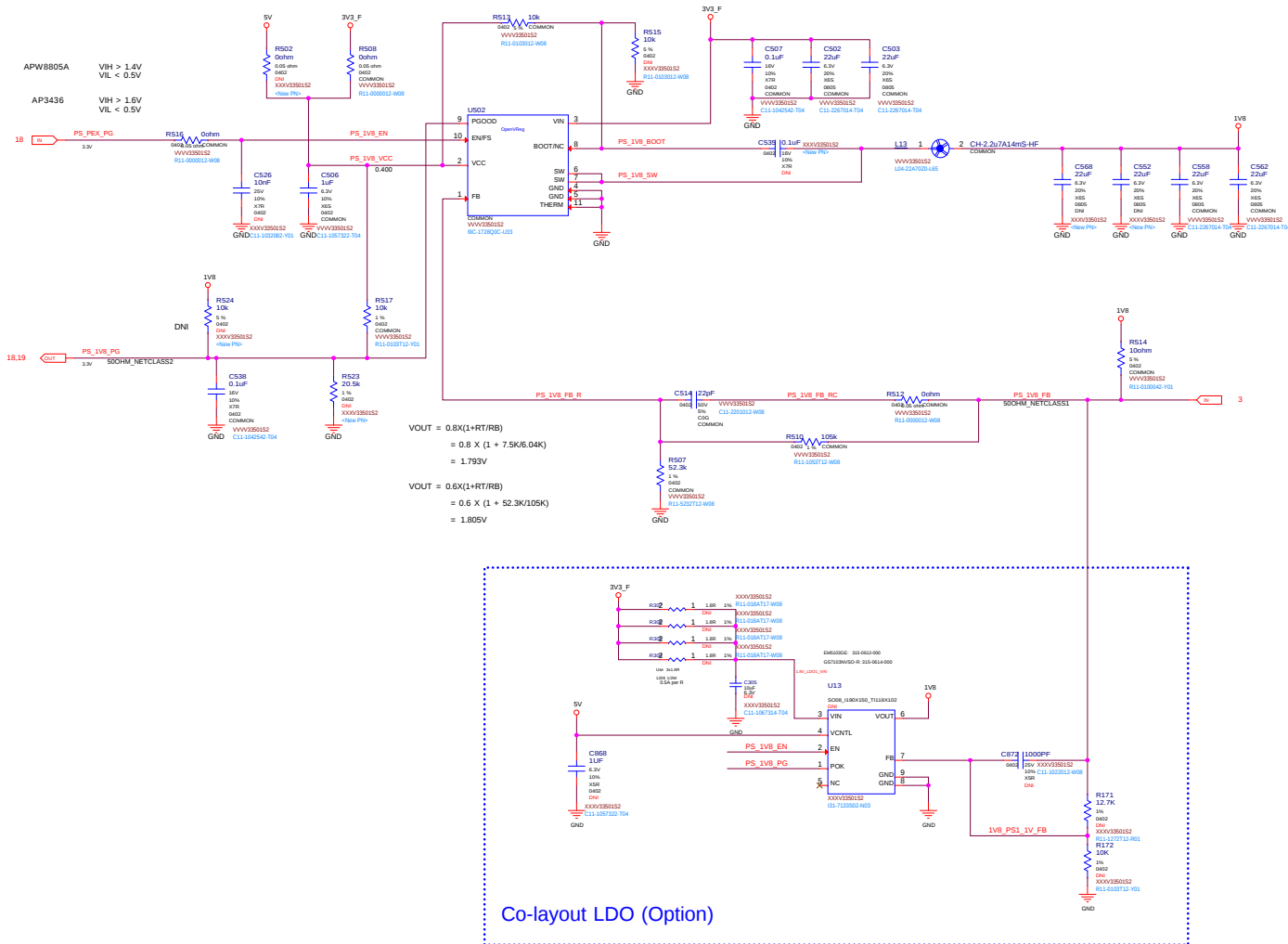
Power Inputs and Filtering



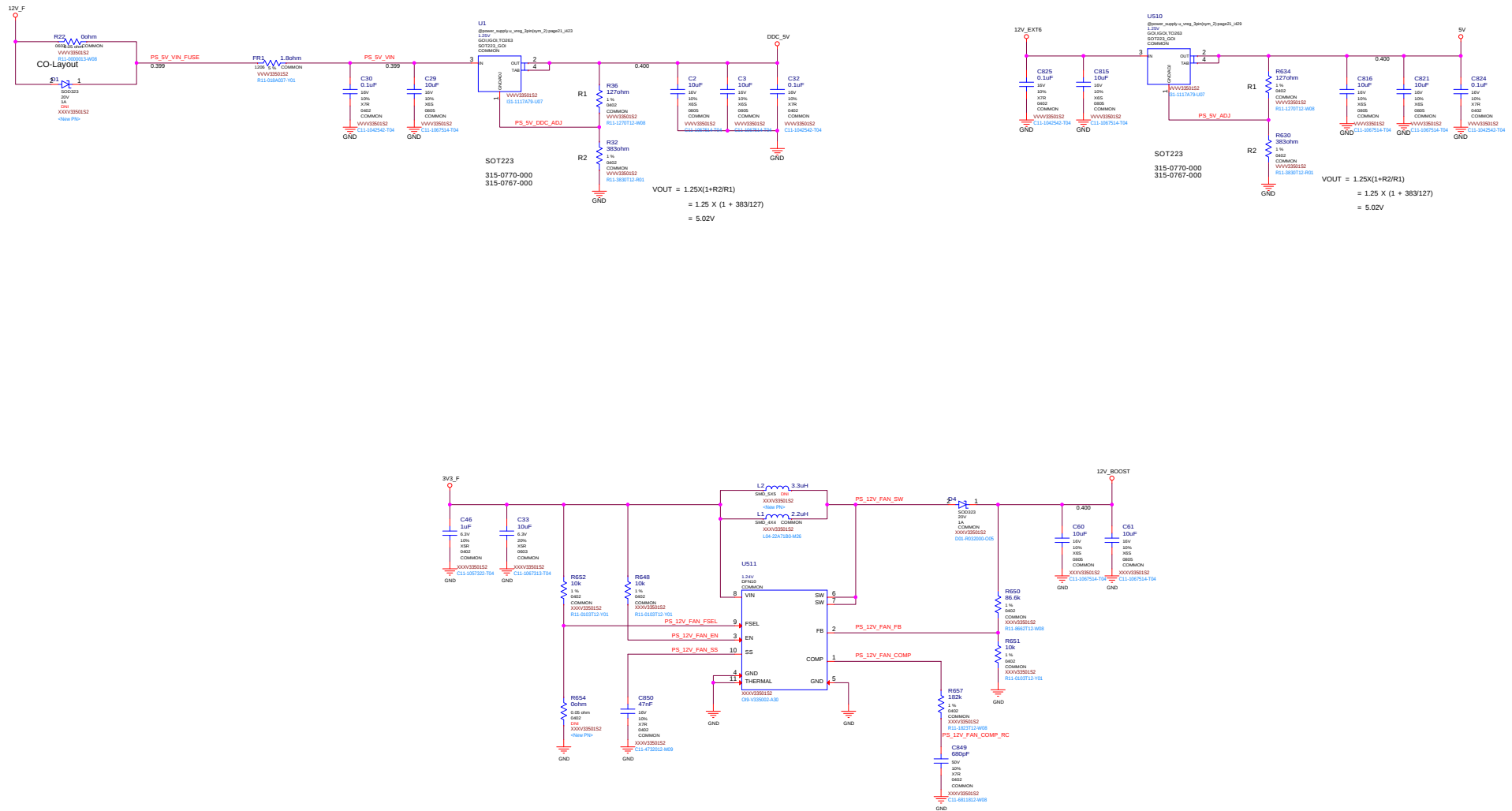
Power sequence



PS I: 1V8



PSII:5V & 12V_FAN



PS IV: FBVDDQ

FBVDDQ_CTL	FBVDDQ	Non-DVS
X	1.5V	<= DEFAULT

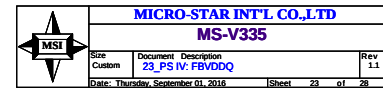
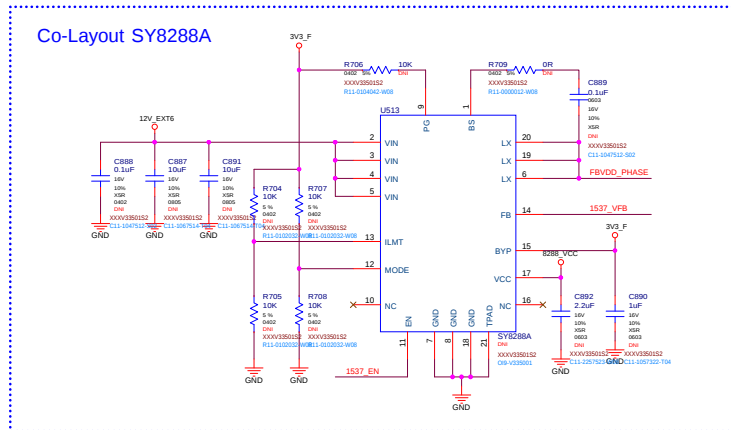
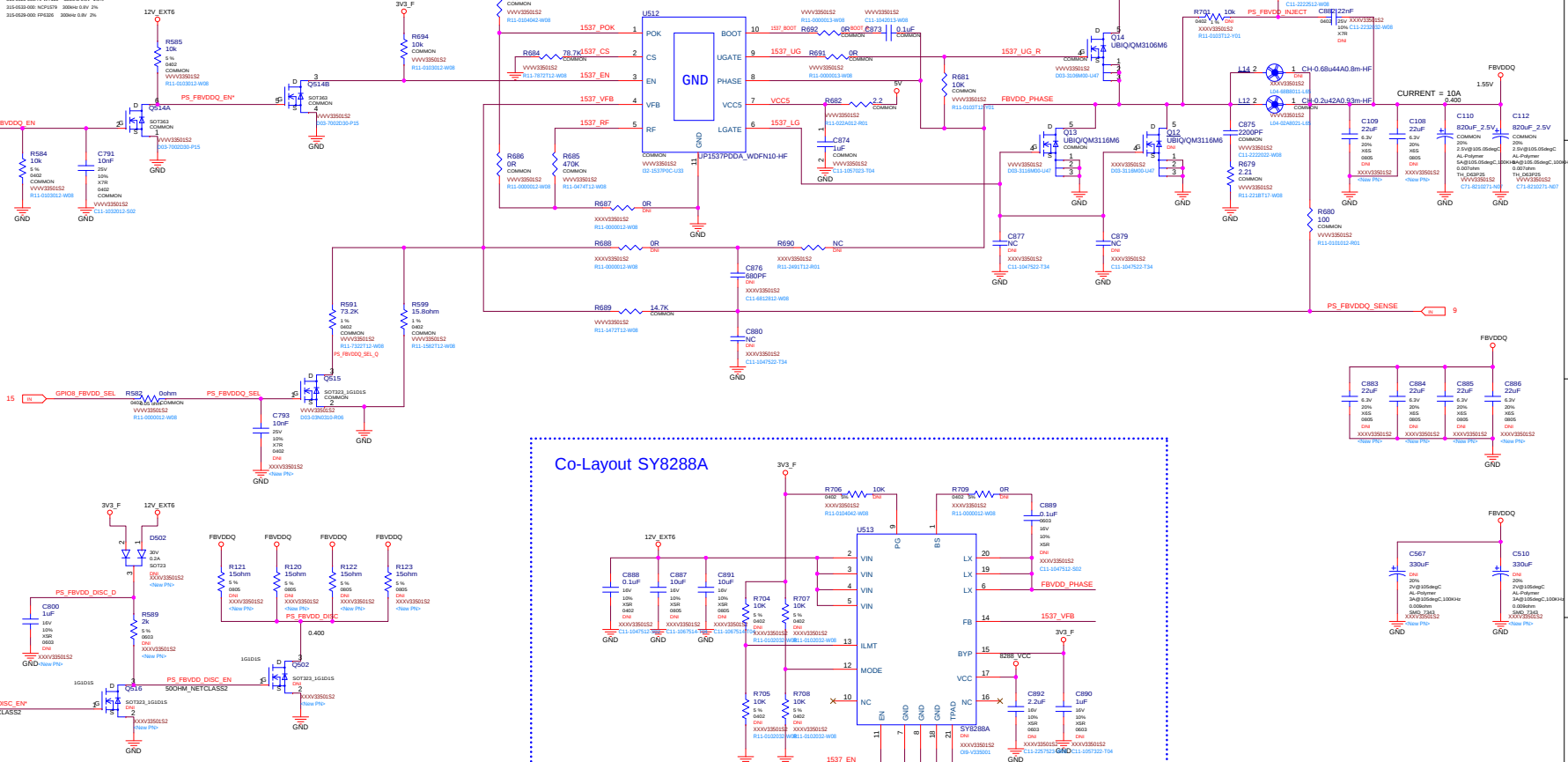
FBVDDQ_CTL	FBVDDQ	For DVS
0	1.35V	
1	1.5V/1.55V	<= DEFAULT

	$V_{out} = V_{ref} \cdot (1 + 0.05R)$
$V_{ref}=0.5V$:	$1.50V = 0.5V \cdot (1 + 30552)$ $1.55V = 0.5V \cdot (1 + 30534)$
$V_{ref}=0.8V$:	$1.50V = 0.8V \cdot (1 + 3K/1.12K)$ $1.55V = 0.8V \cdot (1 + 3K/1.07K)$

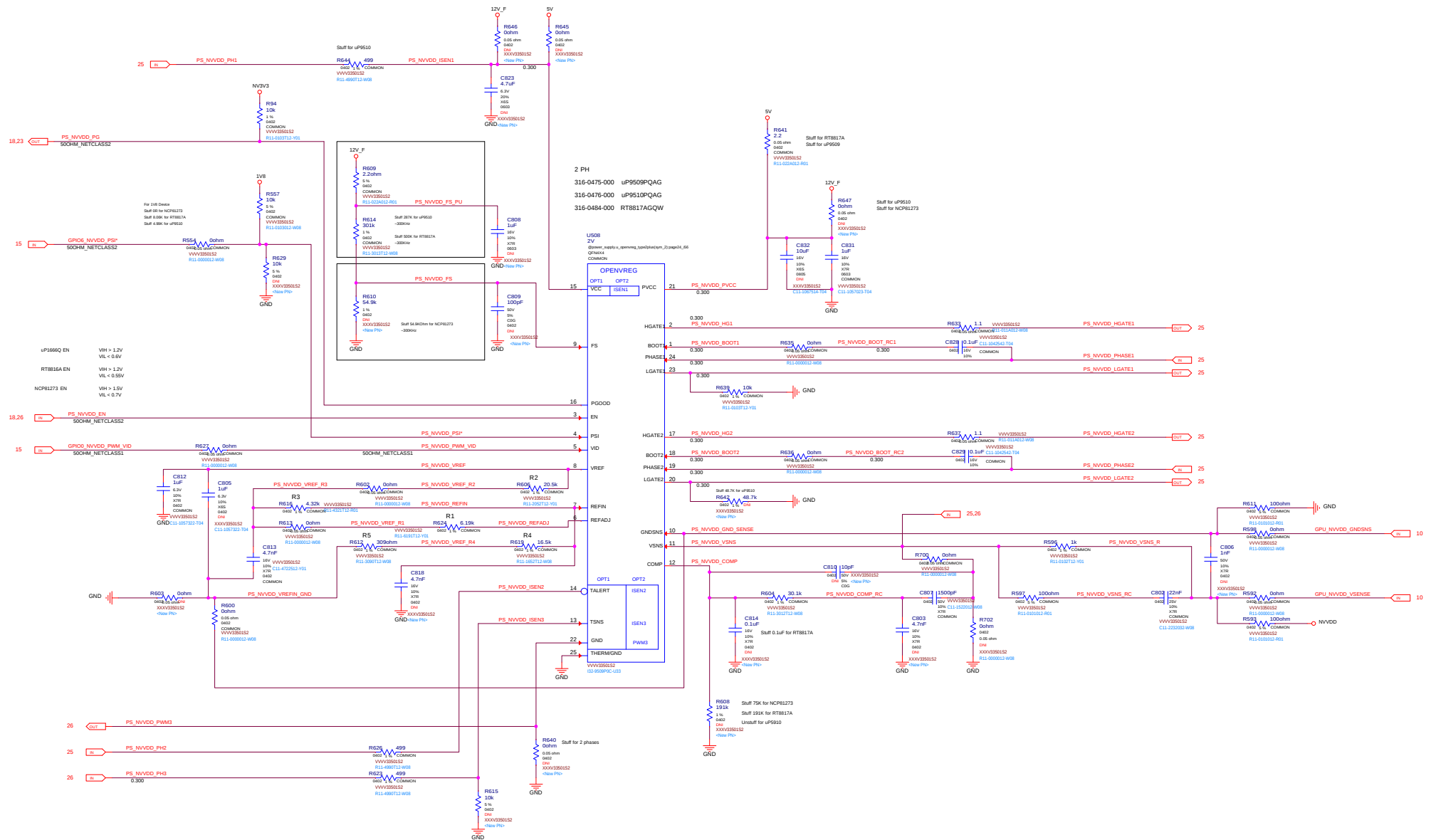
	$V_{out} = V_{ref} \cdot (1+R2/R1)$
$V_{ref}=0.6V$:	$1.50V = 0.6V \cdot (1+3k73/1k12)$ $1.55V = 0.6V \cdot (1+3k73/1k12)$ $1.36V = 0.6V \cdot (1+3k73/1k12)$
$V_{ref}=0.8V$:	$1.50V = 0.8V \cdot (1+3k15/4k3k)$ $1.55V = 0.8V \cdot (1+3k15/4k3k)$ $1.36V = 0.8V \cdot (1+3k15/4k3k)$

	PS	Fanc	Unif	Tot
215-0825-000 APW8722	3006Hz 0.0V 1%			
215-0868-000 EM3301D	3006Hz 0.0V 2%			
216-0096-000 RTE120AGCS	3006Hz 0.0V 1.5%			
216-0096-000 RTE120AGCS	3006Hz 0.0V 1.5%			
215-0638-000 APW8725A	3006Hz 0.0V 2%			
216-0071-000 RTE120GCS	3006Hz 0.0V 1%			
215-0526-000 APW71120	3006Hz 0.0V 1.5%			
215-0523-000 CP15179	3006Hz 0.0V 2%			
215-0529-000 FP832G	3006Hz 0.0V 2%			

12V EXT6



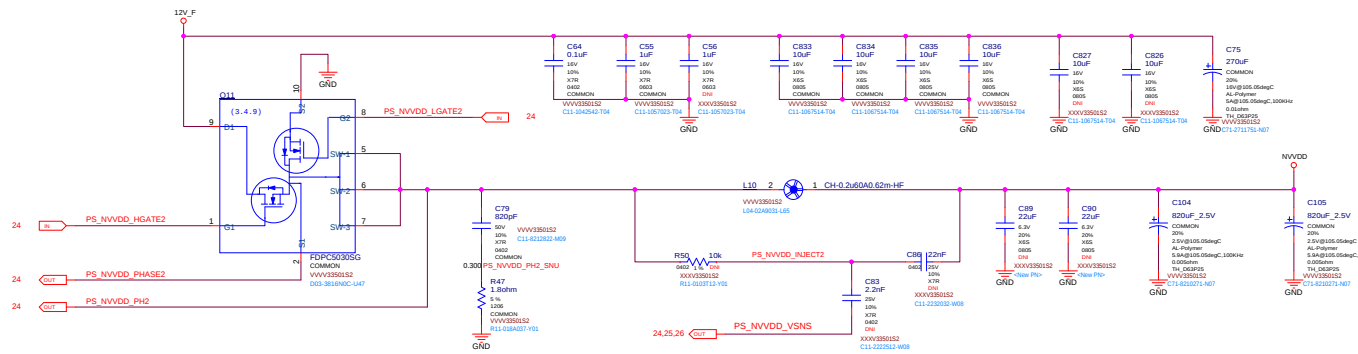
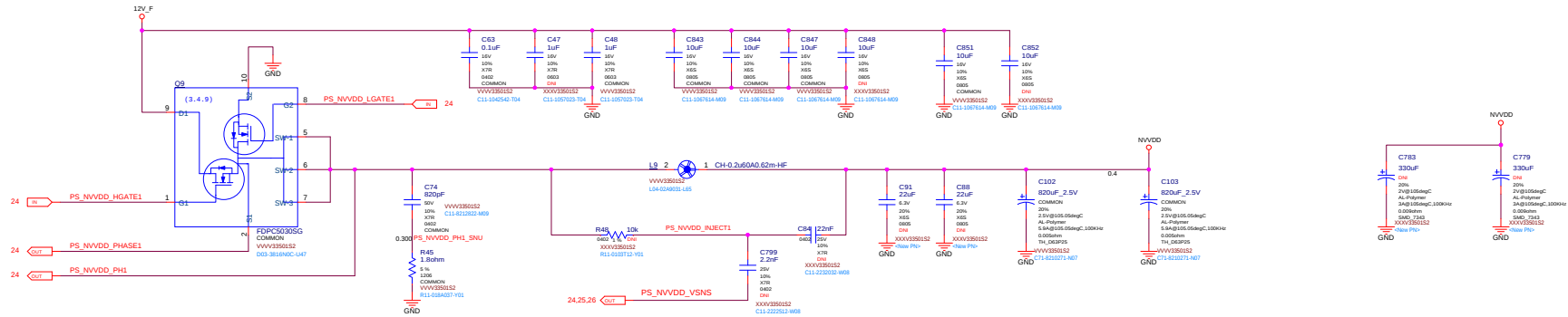
PS V: NVVDD OVR2+1



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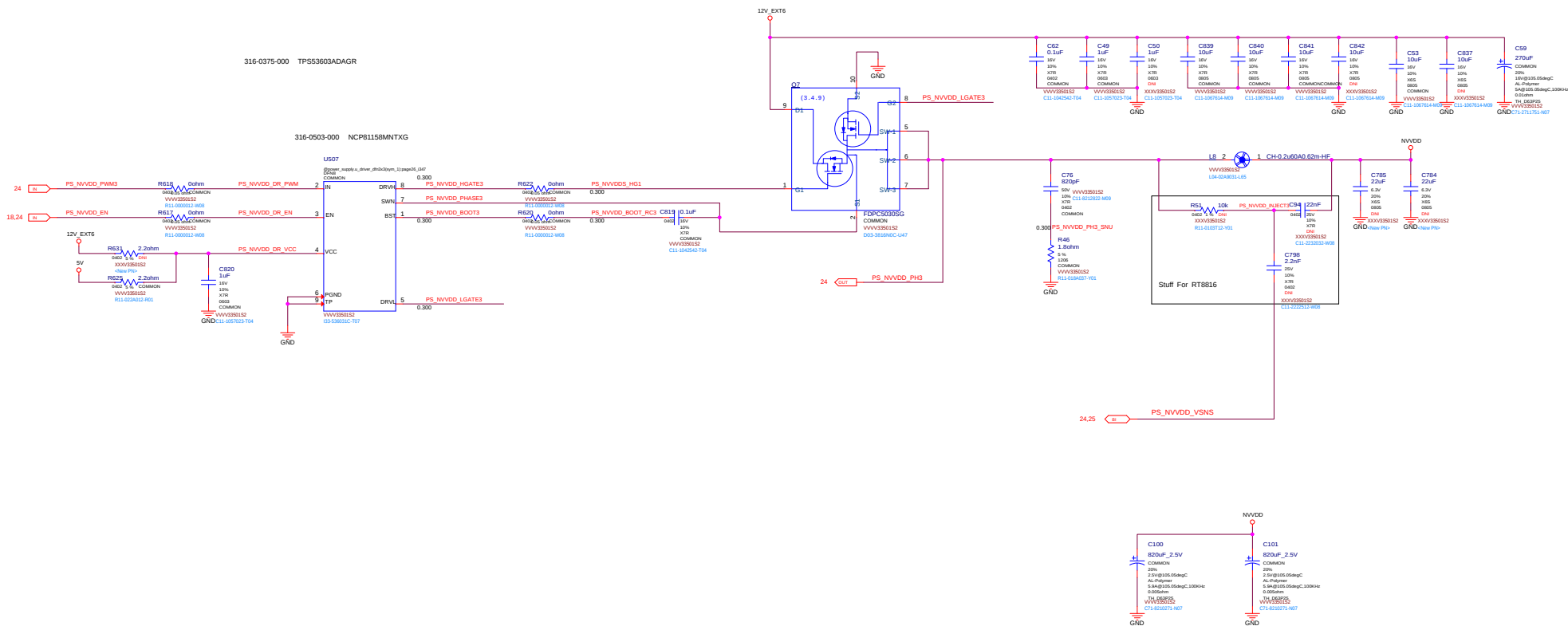
PS V: NVVDD Phase 1,2



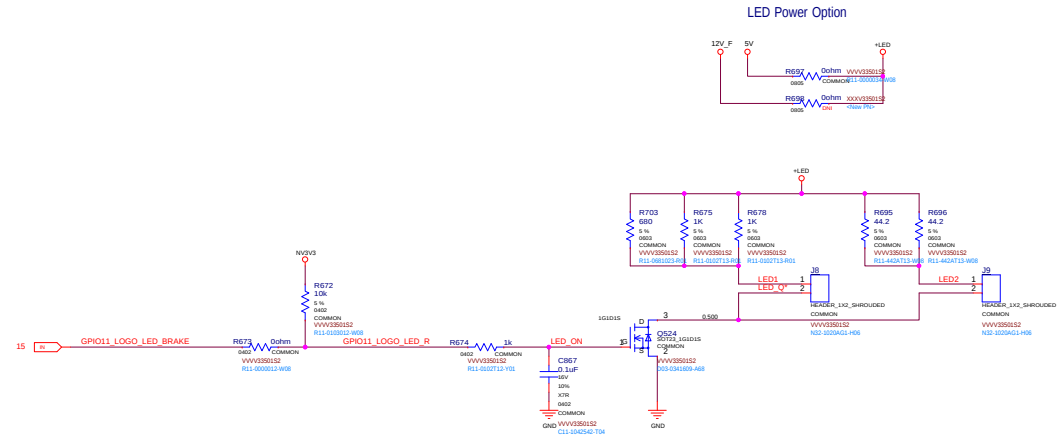
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Size Custom	Document Description 25_PS V: NVDD Phase 1,2	Rev 1.1
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PS V: NVDD Phase 3



Logo LED



Mechanical: Bracket/Thermal Solution

Brackets:

