

PG210 B00

GP107 128b GDDR5, 75W , PCB 5.7"
DVI-D_DL (DP + DP) + HDMI (DP) + DP

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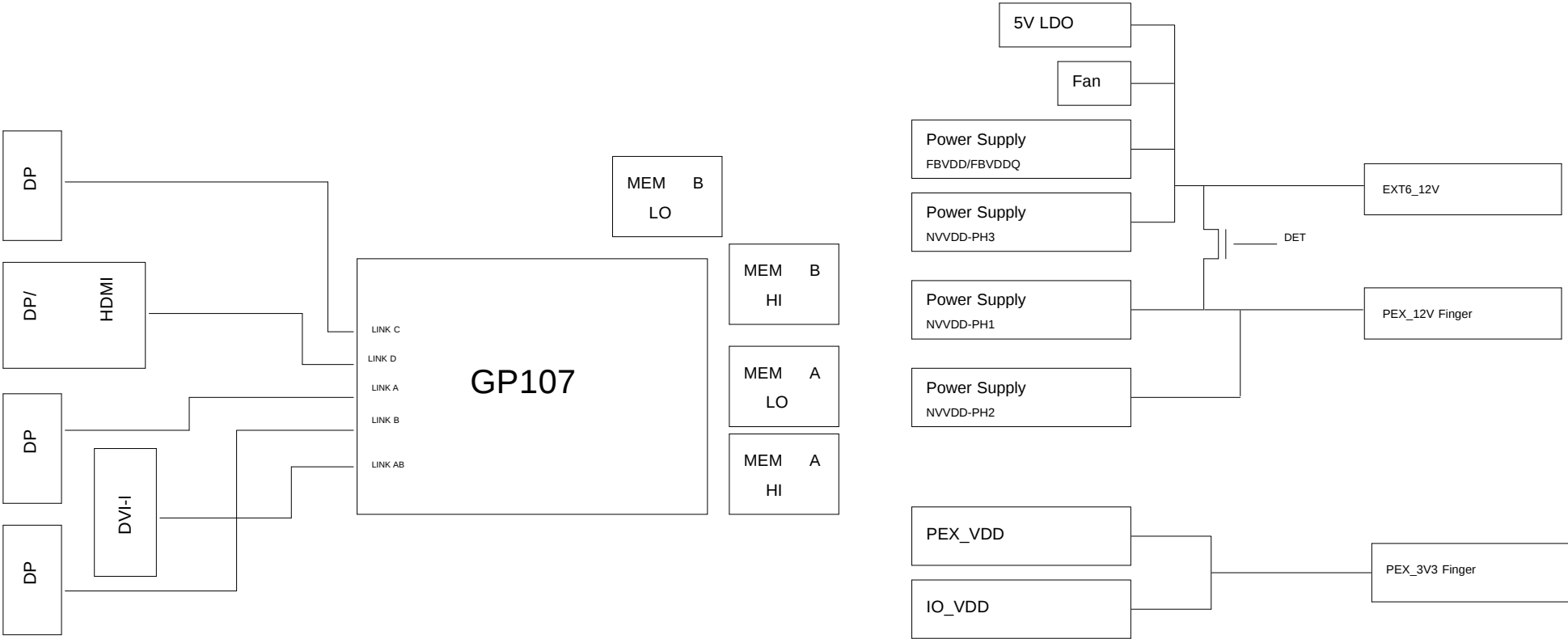
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Page	Description
1	No change

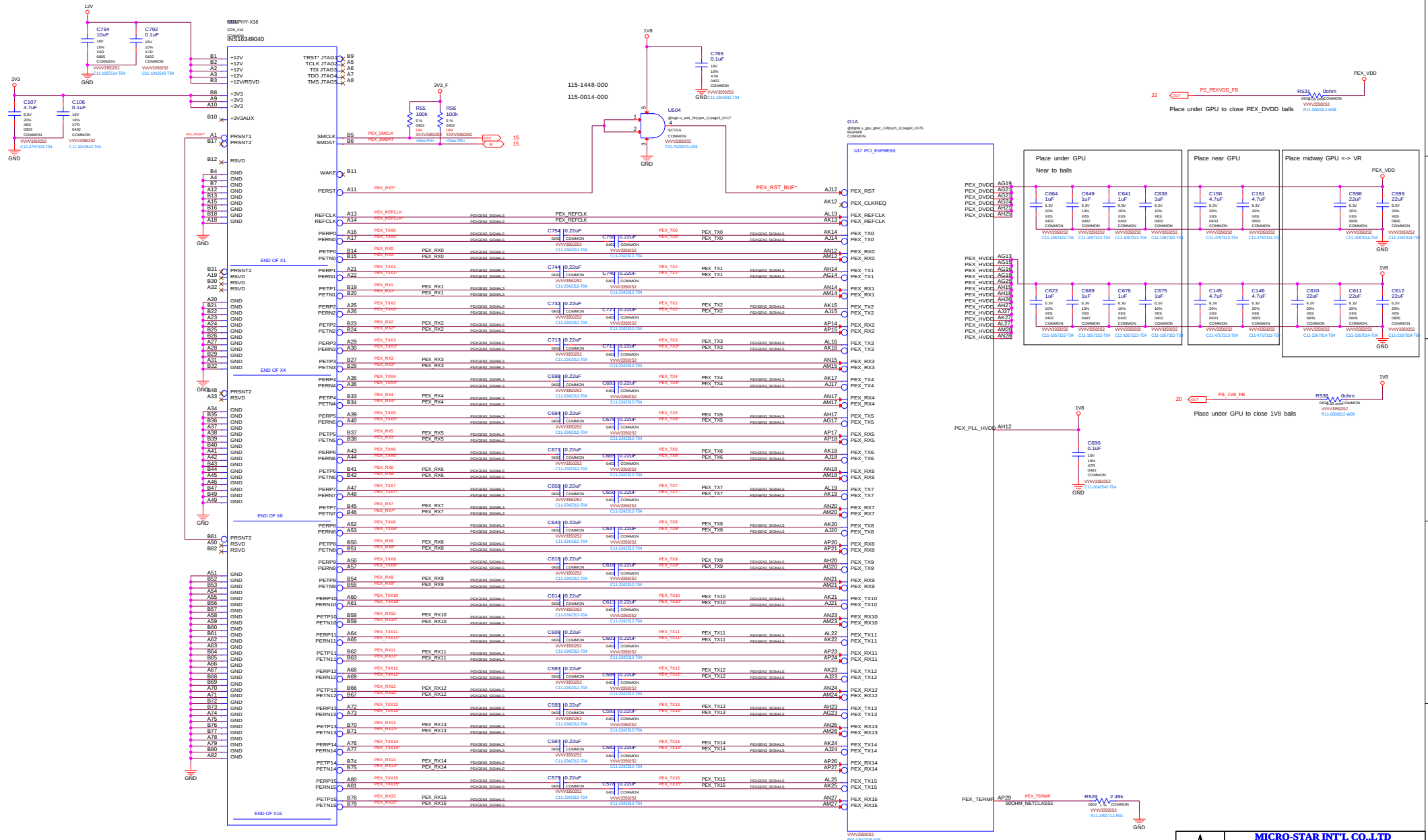
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1	Change PCIE footprint for full pin

Block Diagram



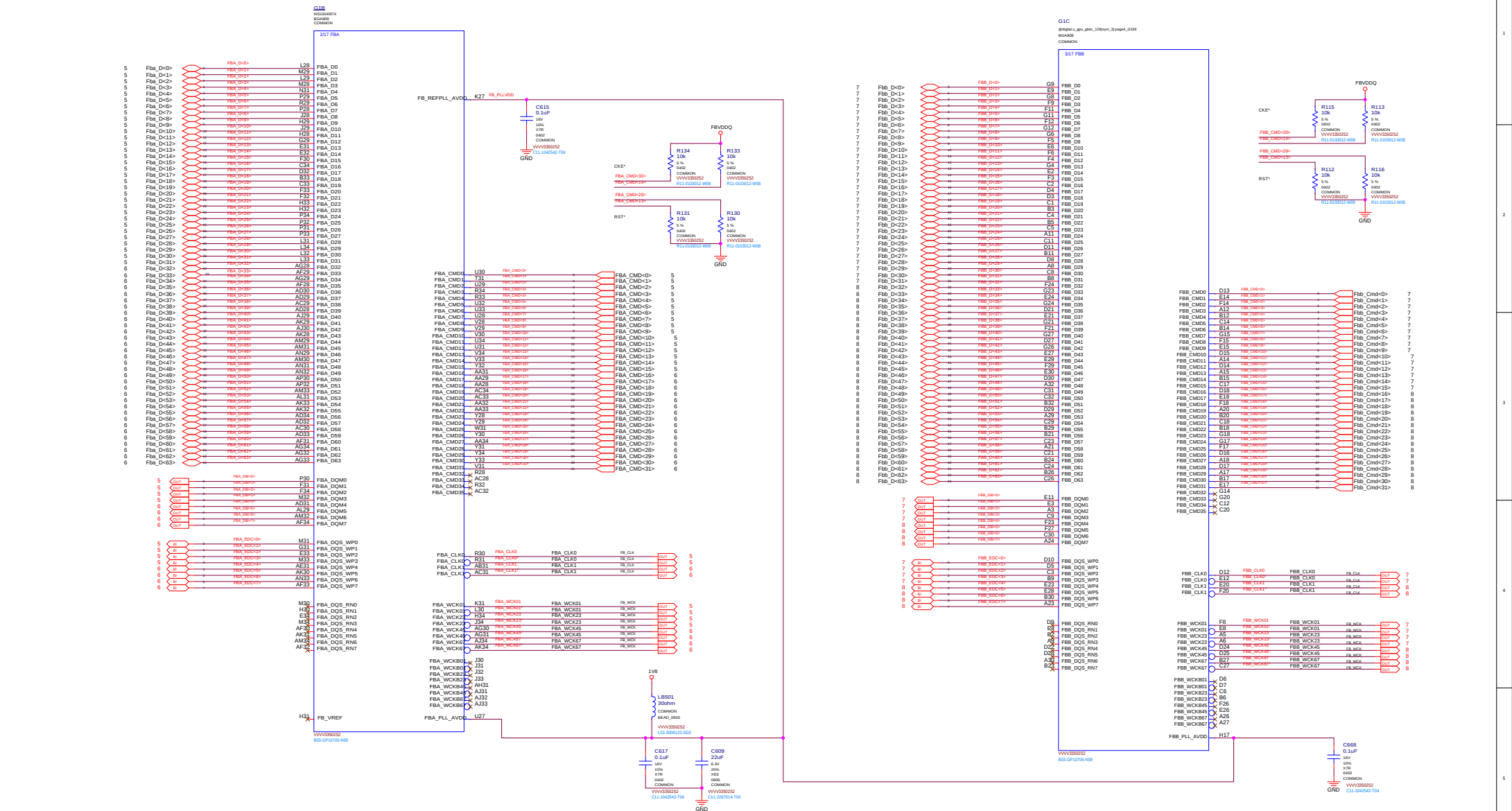
PCI Express



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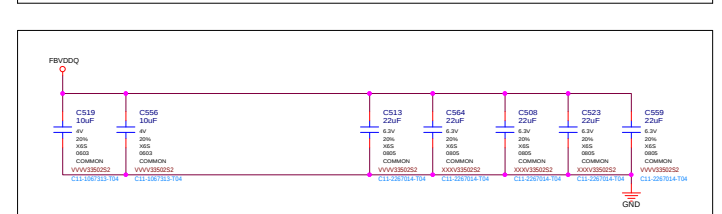
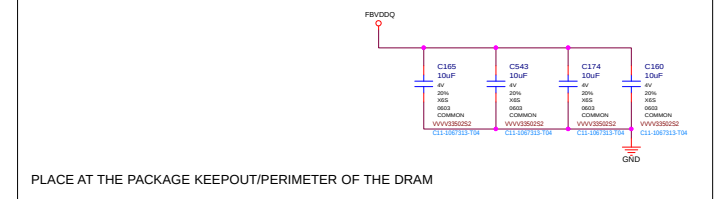
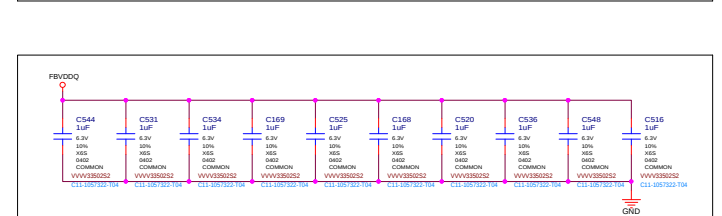
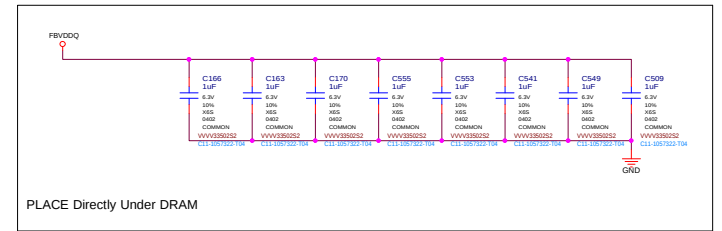
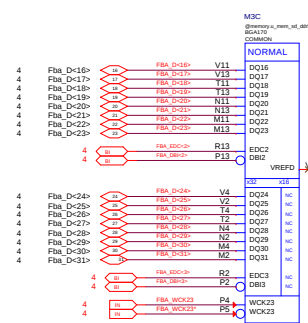
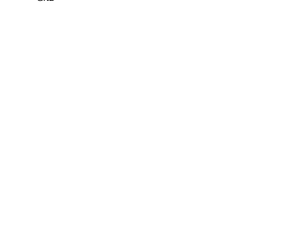
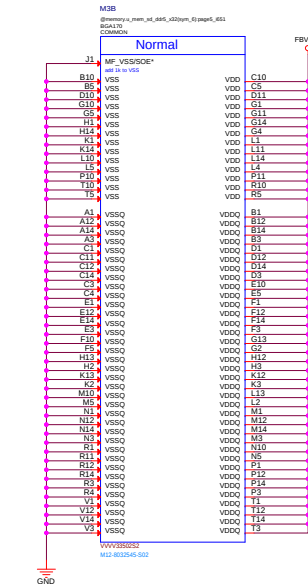
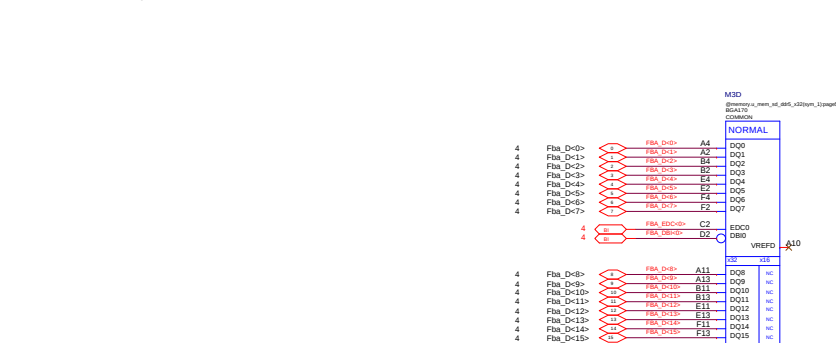
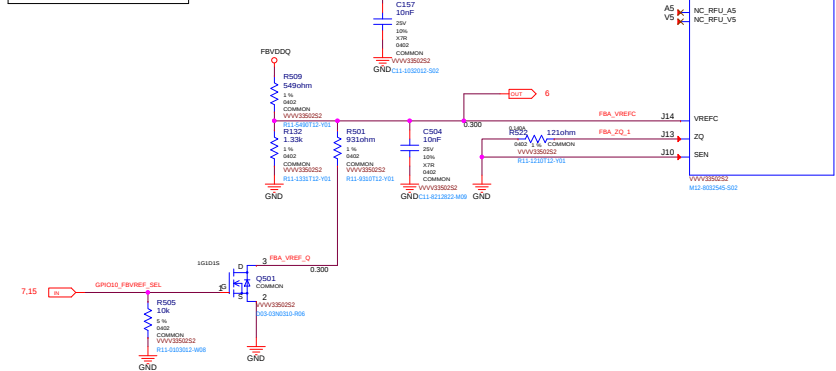
Size Custom	Document Description 03_PCI Express	Rev 1.2
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MEMORY: GPU Partition A/B



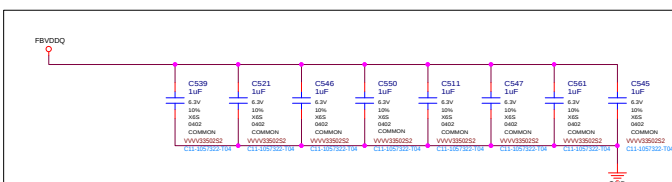
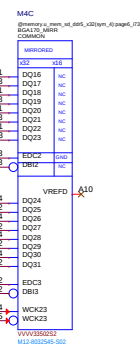
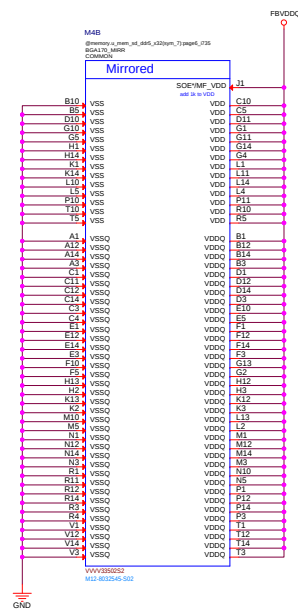
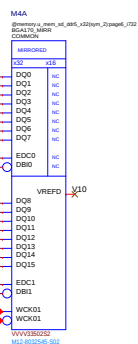
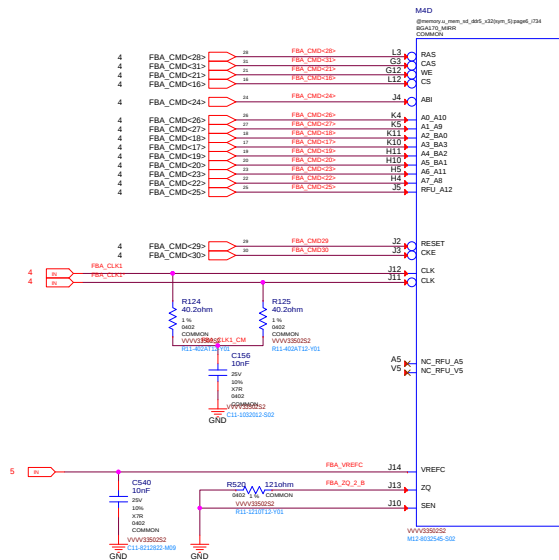
MEMORY: FBA Partition 31..0

CMD	0..31	32..63
CMD0	CS*	
CMD1	A3, BA3	
CMD2	A2, BA2	
CMD3	A4, BA4	
CMD4	A5, BA4	
CMD5	WE*	
CMD6	A7, A8	
CMD7	A6, A11	
CMD8	AB*	
CMD9	A12, RFU	
CMD10	A0, A10	
CMD11	A1, A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17	A3, BA3	
CMD18	A2, BA2	
CMD19	A4, BA4	
CMD20	WE*	
CMD21	A7, A8	
CMD22	A6, A11	
CMD23	AB*	
CMD24	A12, RFU	
CMD25	A0, A10	
CMD26	A1, A9	
CMD27	RAS*	
CMD28	RST*	
CMD29	CKE*	
CMD30	CAS*	
CMD31		CAS*

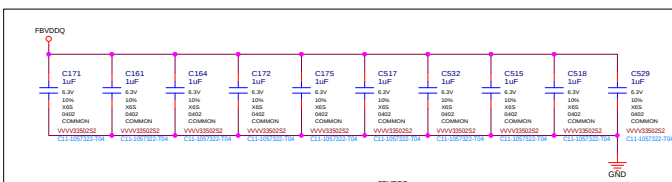


MEMORY: FBA Partition 63..32

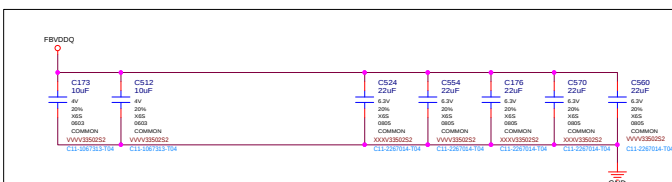
CMD	0..31	32..63
CMD0	CS*	
CMD1	A3, BA3	
CMD2	A2, BA0	
CMD3	A1, BA2	
CMD4	AS, BA1	
CMD5	WE*	
CMD6	A7, AB	
CMD7	AB, A11	
CMD8	ABP	
CMD9	A12, RFU	
CMD10	A0, A10	
CMD11	A1, A0	
CMD12	RA5*	
CMD13	RS1*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3, BA3
CMD18		A2, BA0
CMD19		A1, BA2
CMD20		AS, BA1
CMD21		WE*
CMD22		A7, AB
CMD23		AB, A11
CMD24		ABP
CMD25		A12, RFU
CMD26		A0, A10
CMD27		A1, A0
CMD28		RA5*
CMD29		RS1*
CMD30		CKE*
CMD31		CAS*



PLACE Directly Under DRAM



PLACE AT THE PACKAGE KEEPOUT/PERIMETER OF THE DRAM



PLACE Around DRAM

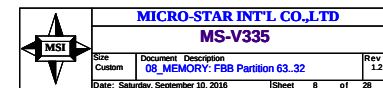
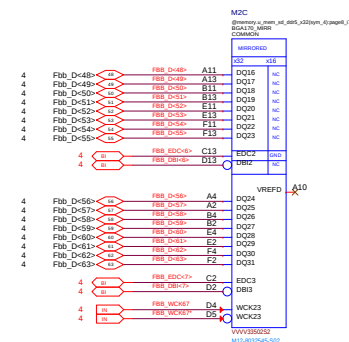
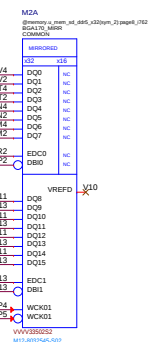
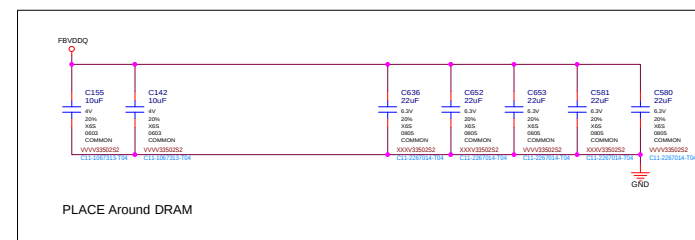
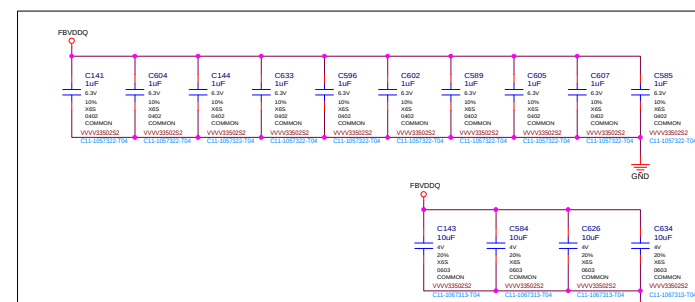
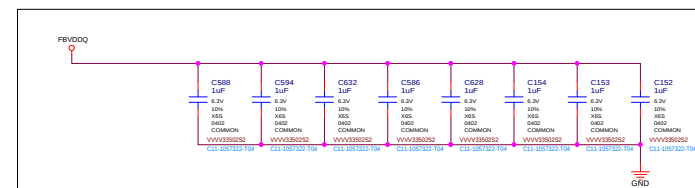
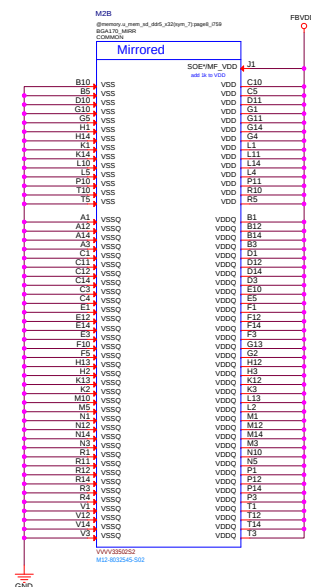
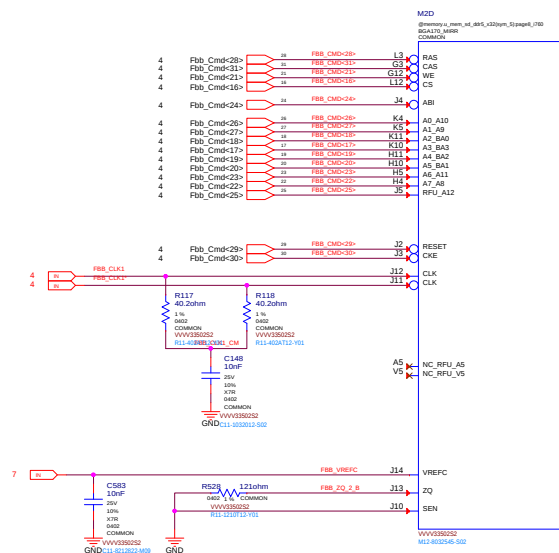


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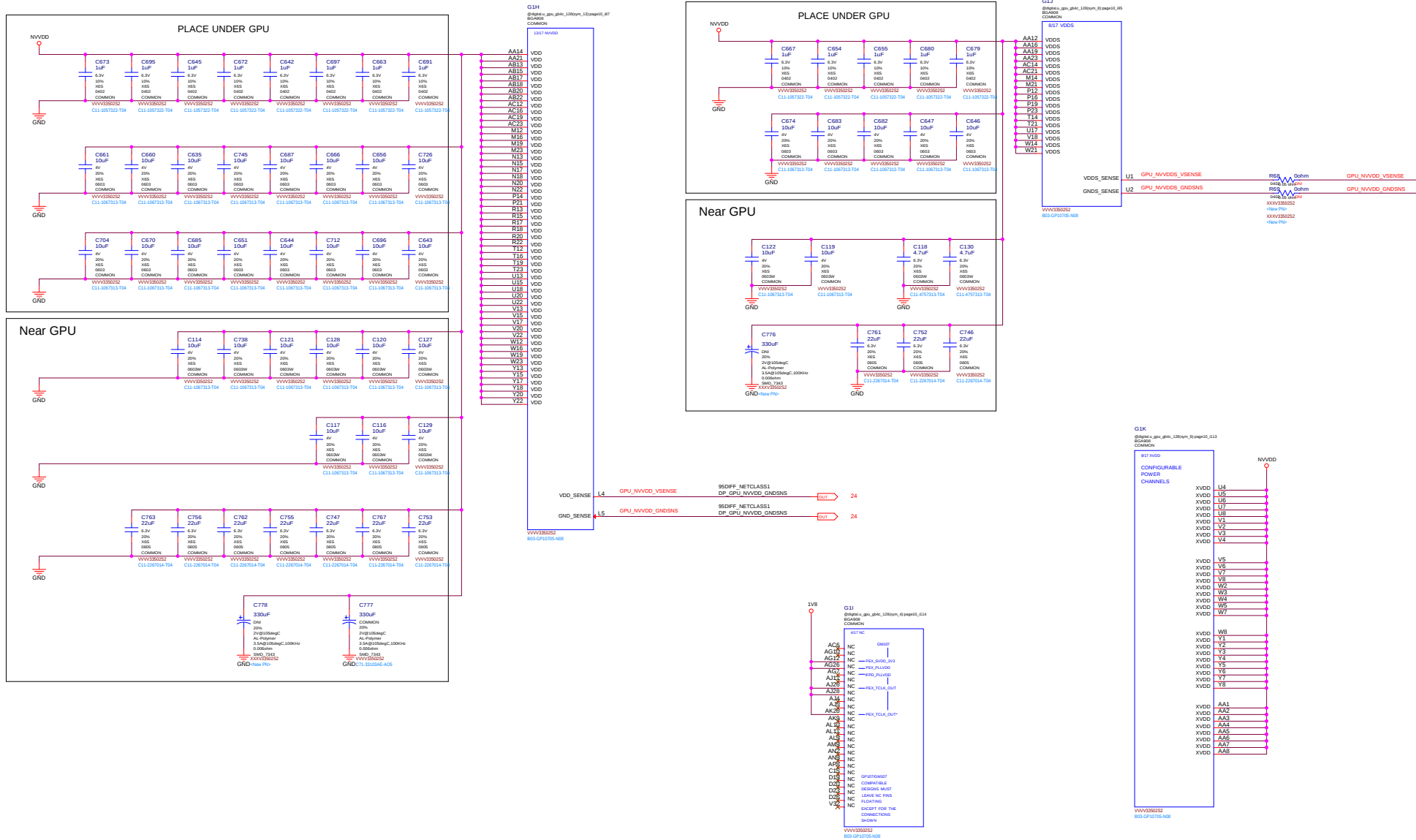
Size Custom	Document Description 06_MEMORY: FBA Partition 63.32	Rev 1.2
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MEMORY: FBB Partition 63..32

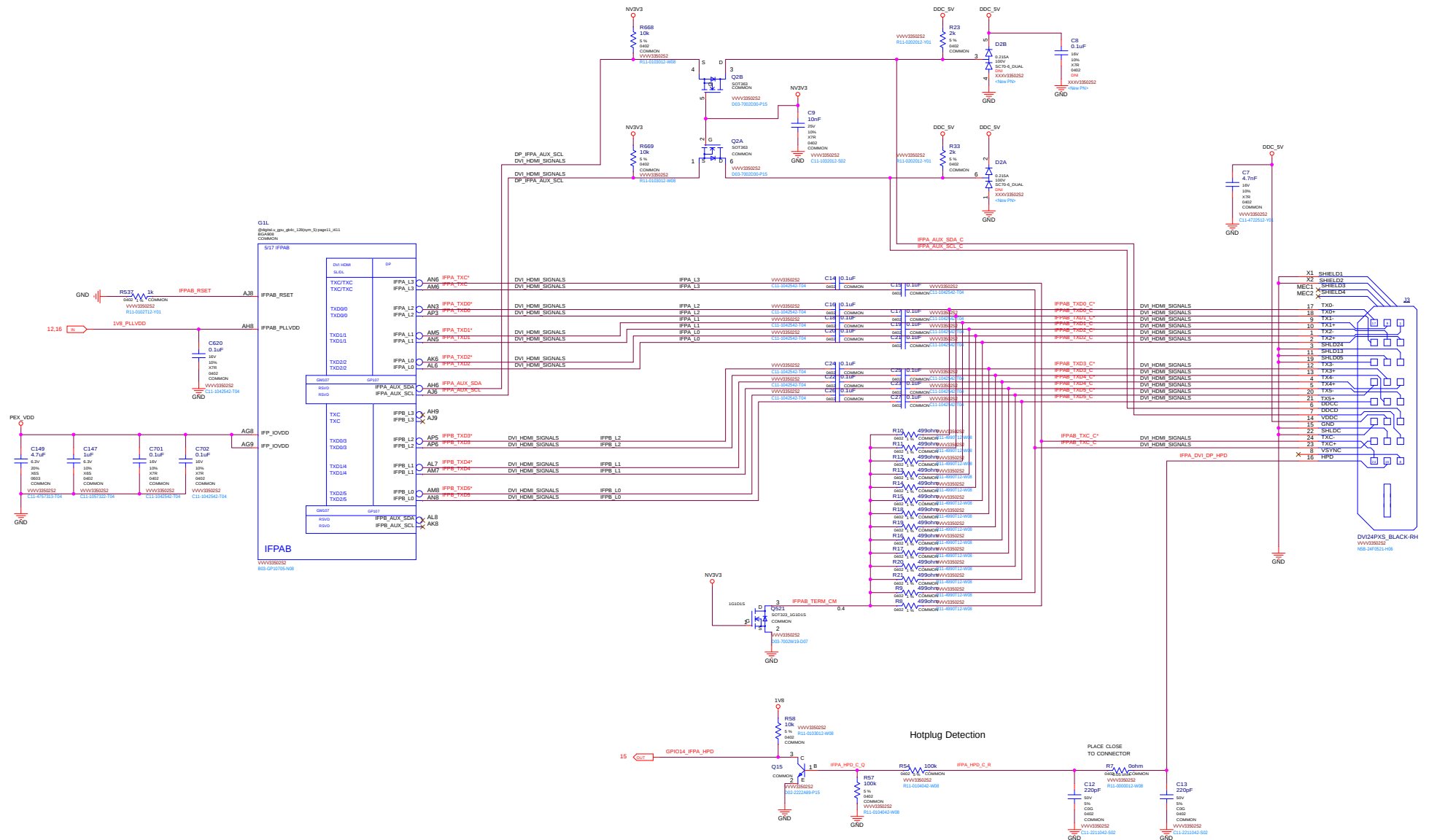
CMD	0..31	32..63
CMD00	C0*	
CMD01	A3, BA3	
CMD02	A2, BA0	
CMD03	A4, BA2	
CMD04	A5, BA1	
CMD05	W6*	
CMD06	A7..A8	
CMD07	AE, A11	
CMD08	W8*	
CMD09	A12..RFU	
CMD10	AE, A10	
CMD11	A1..A8	
CMD12	RA5*	
CMD13	RS1*	
CMD14	CW*	
CMD15	CAS*	
CMD16		C5*
CMD17		A3, BA3
CMD18		A2, BA0
CMD19		A4, BA2
CMD20		AE, BA1
CMD21		W6*
CMD22		AB*
CMD23		AE, A11
CMD24		A7..A8
CMD25		A12..RFU
CMD26		AE, A10
CMD27		A1..A8
CMD28		RA5*
CMD29		RS1*
CMD30		CW*
CMD31		CAS*



GPU NVVDD & NVVDDS Decoupling



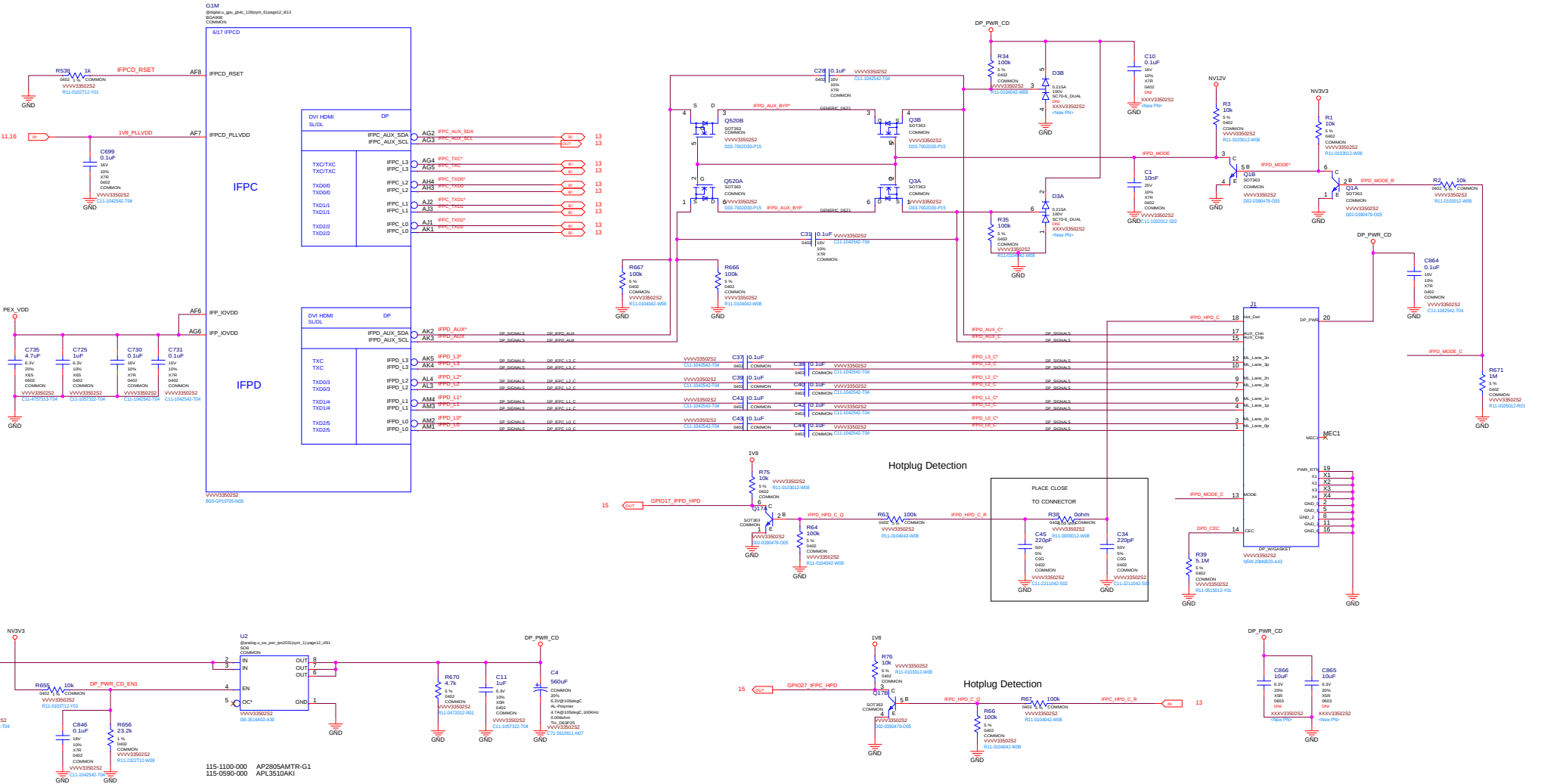
IFPAB DVI-DL



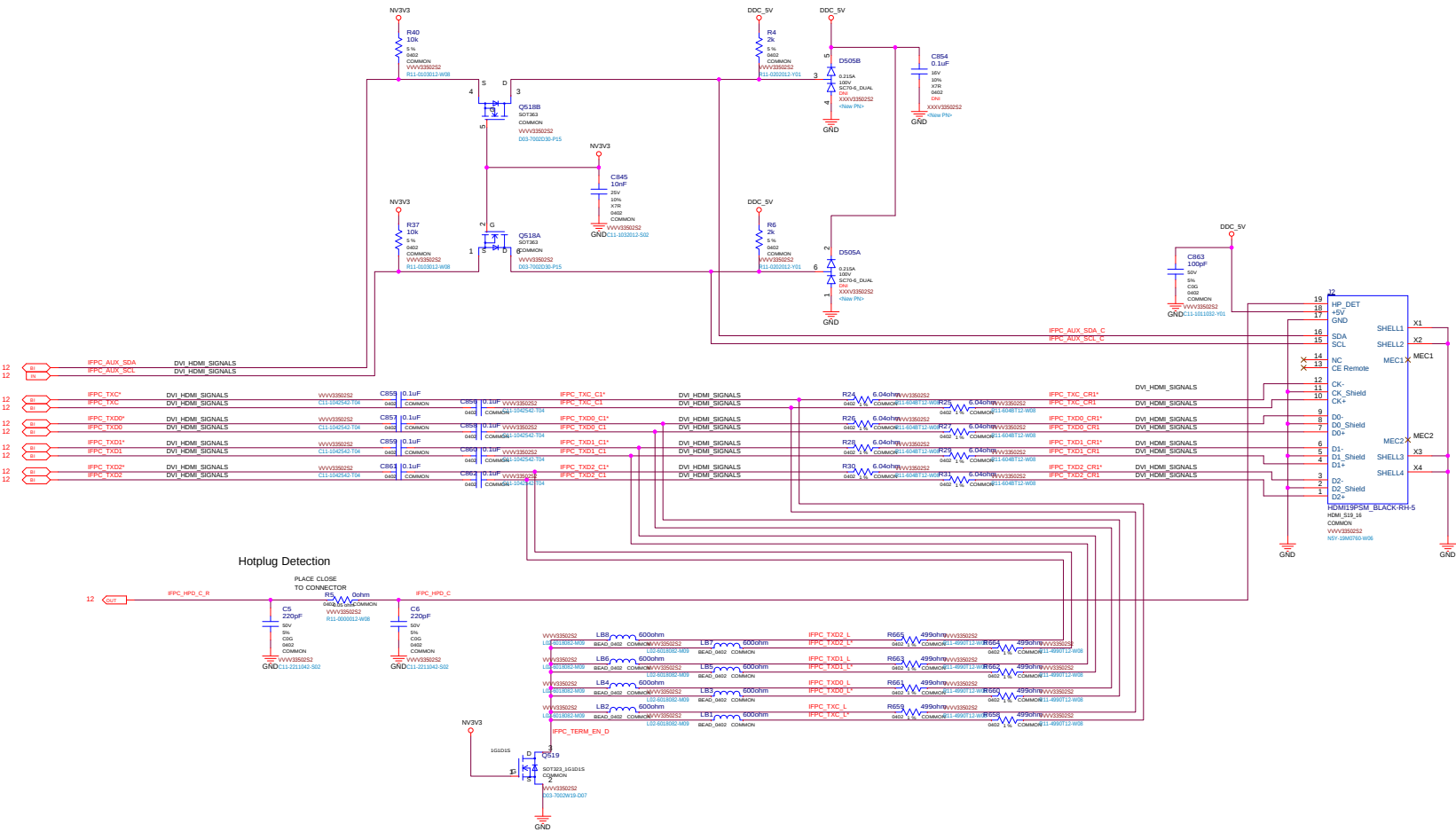
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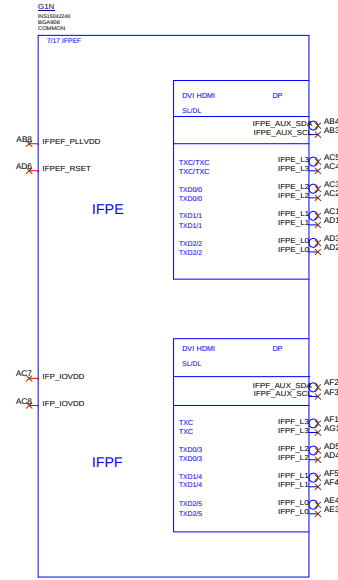
IFPD DP



IFPC HDMI



IFPEF UNUSED

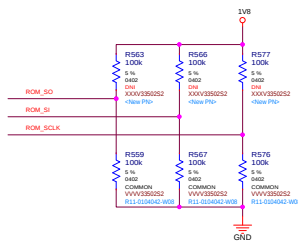


MISC2: ROM, XTAL, Straps

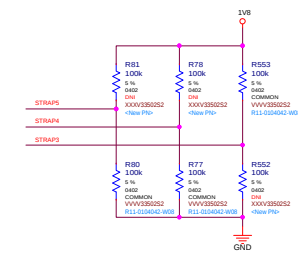
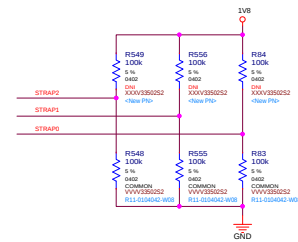
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111	Default
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	Samsung B-Die 8Gb 256Mx32
L	L	H	0001	Micron F-Die 8Gb 256Mx32
L	H	L	0010	Hynix M-Die 8Gb 256Mx32
L	H	H	0011	
H	H	L	0110	Hynix A-Die 4Gb 128Mx32
H	H	H	0111	Samsung E-Die 4Gb 128Mx32
L	L	M	1000	Micron B-Die 4Gb 128Mx32
L	M	L	1001	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0



H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

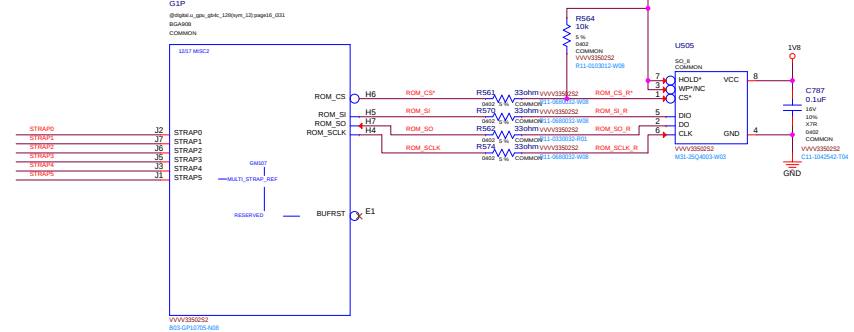


1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

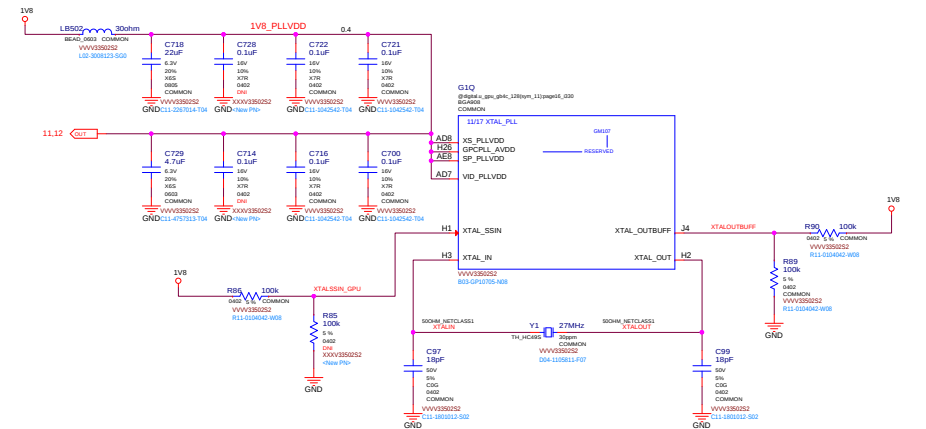
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

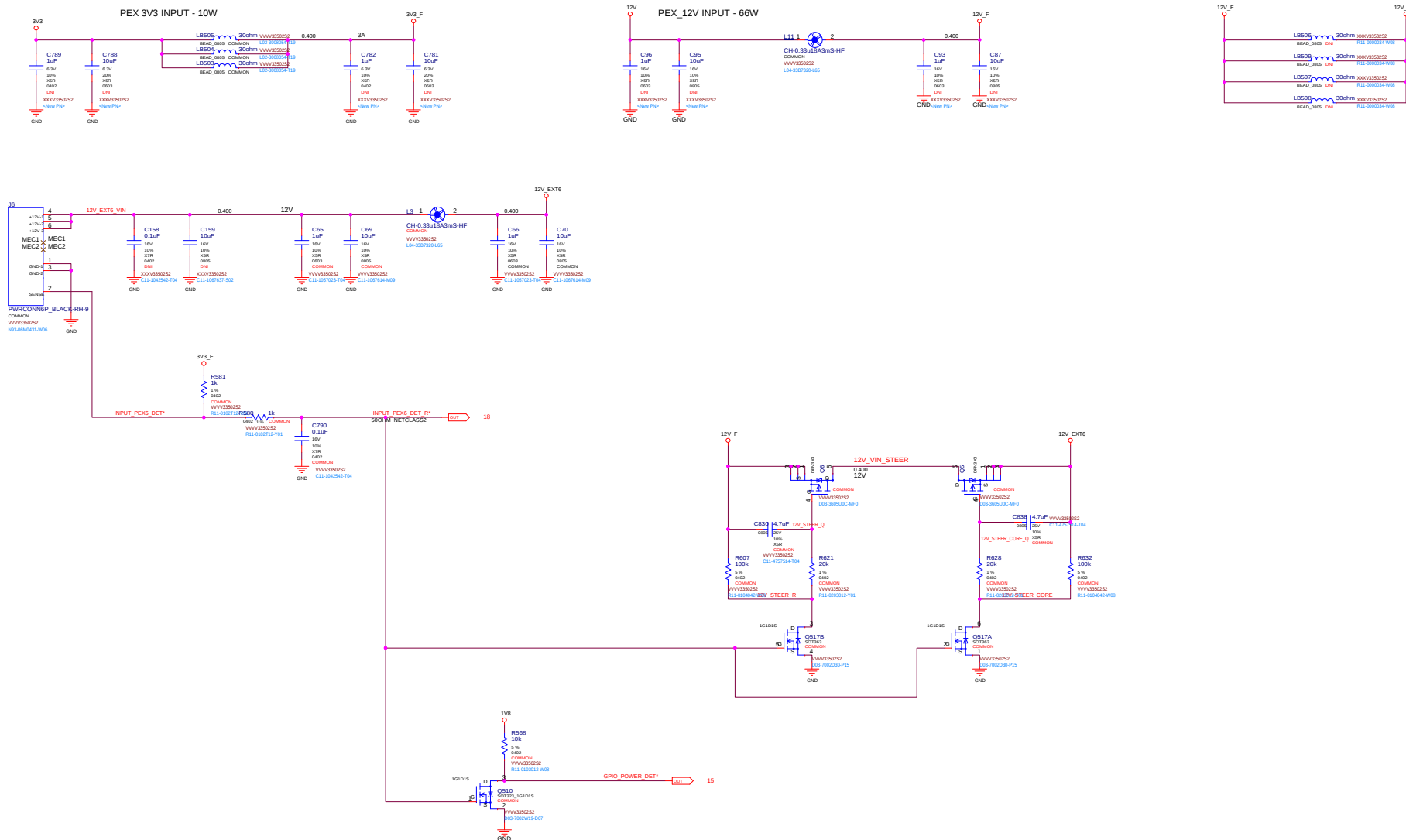


Smart Fan

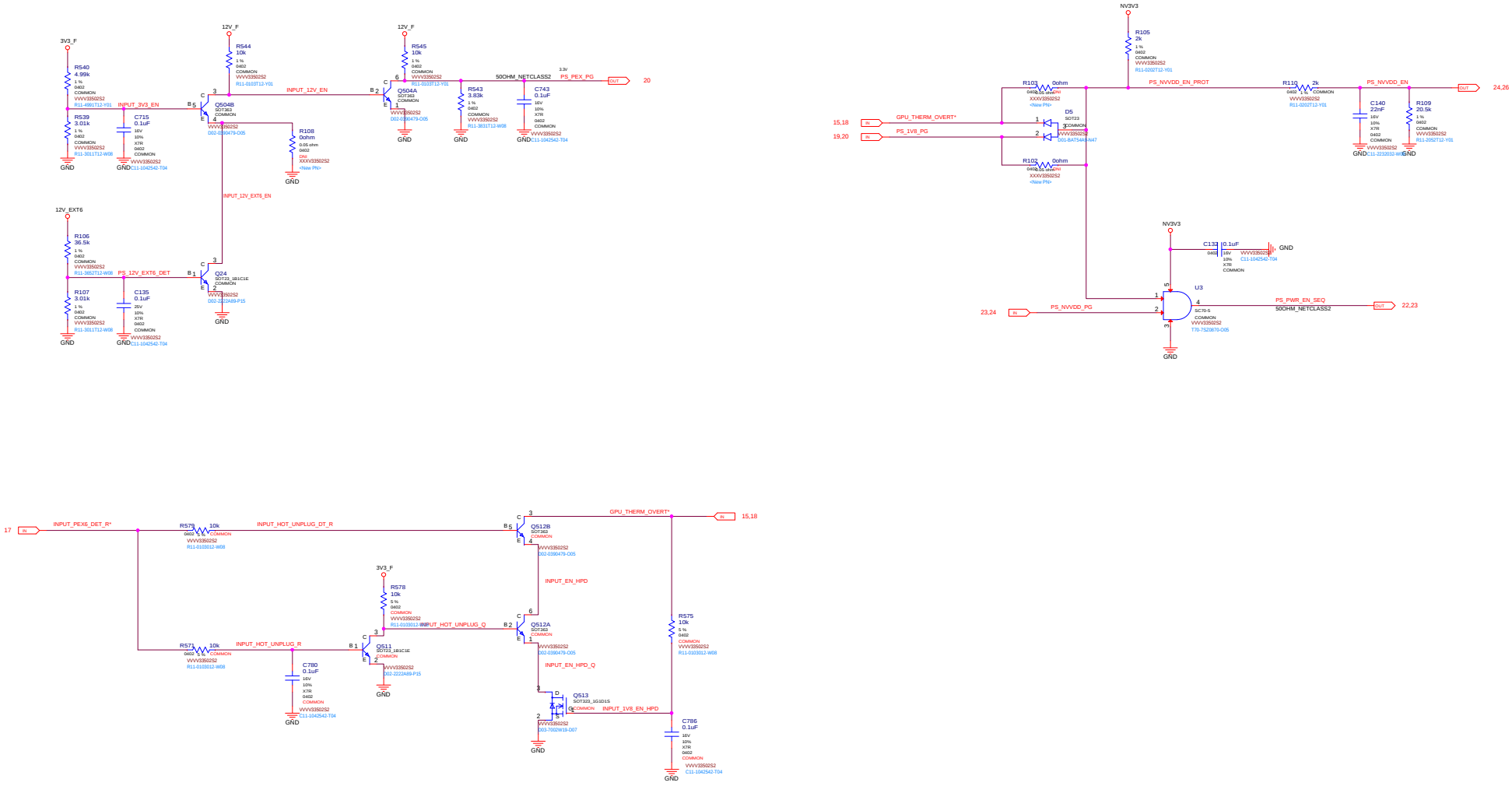
XTALOUTBUFF	Volatge	SmartFan PWM	GPIO/PWM at the FAN
Low	0V	GPIO Disabled	100%
Middle	0.9V	66% PWM	33% PWM (Typical)
High	1.8V	33% PWM	66% PWM



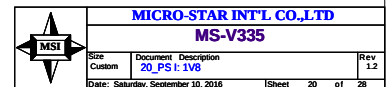
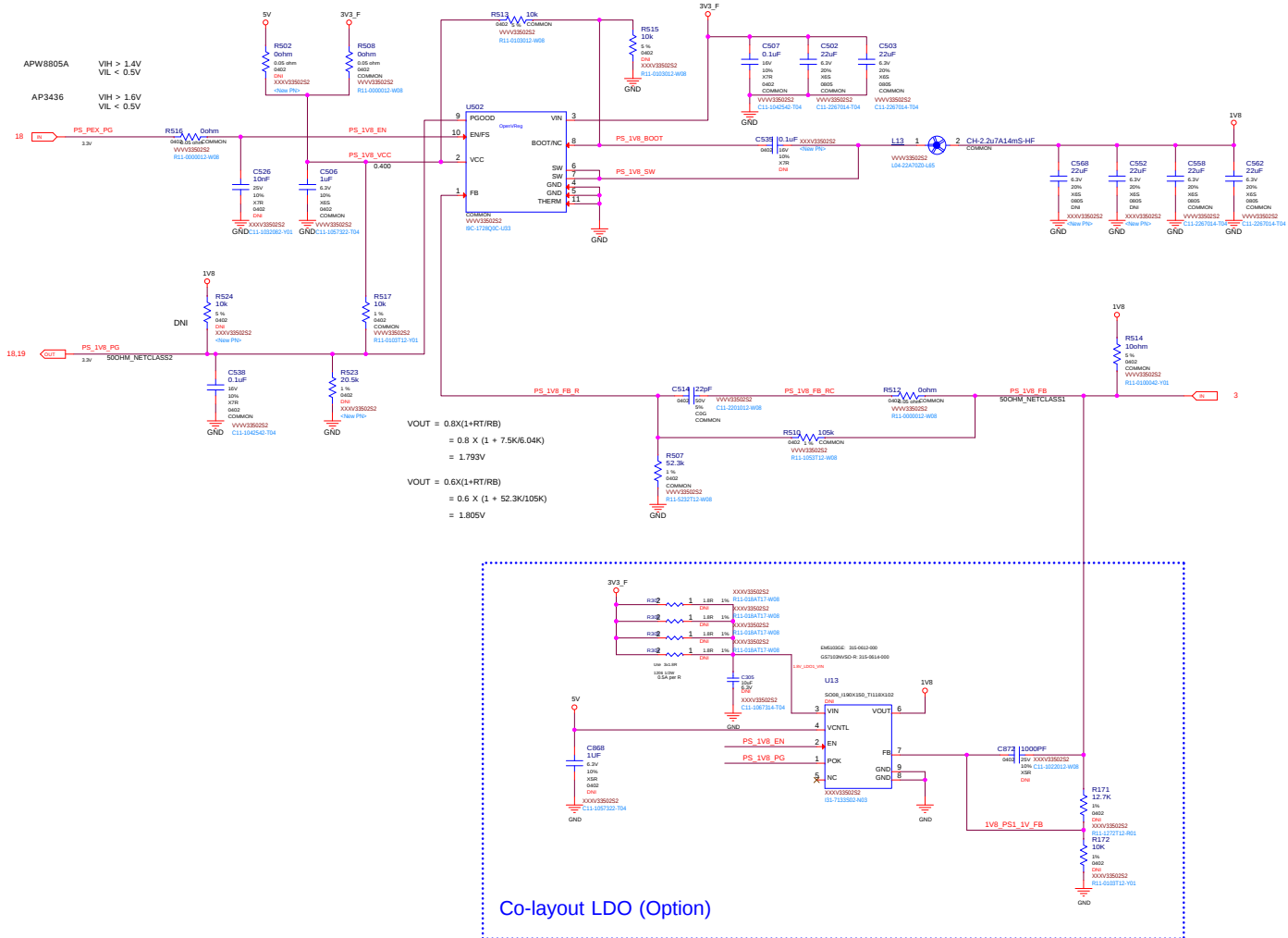
Power Inputs and Filtering



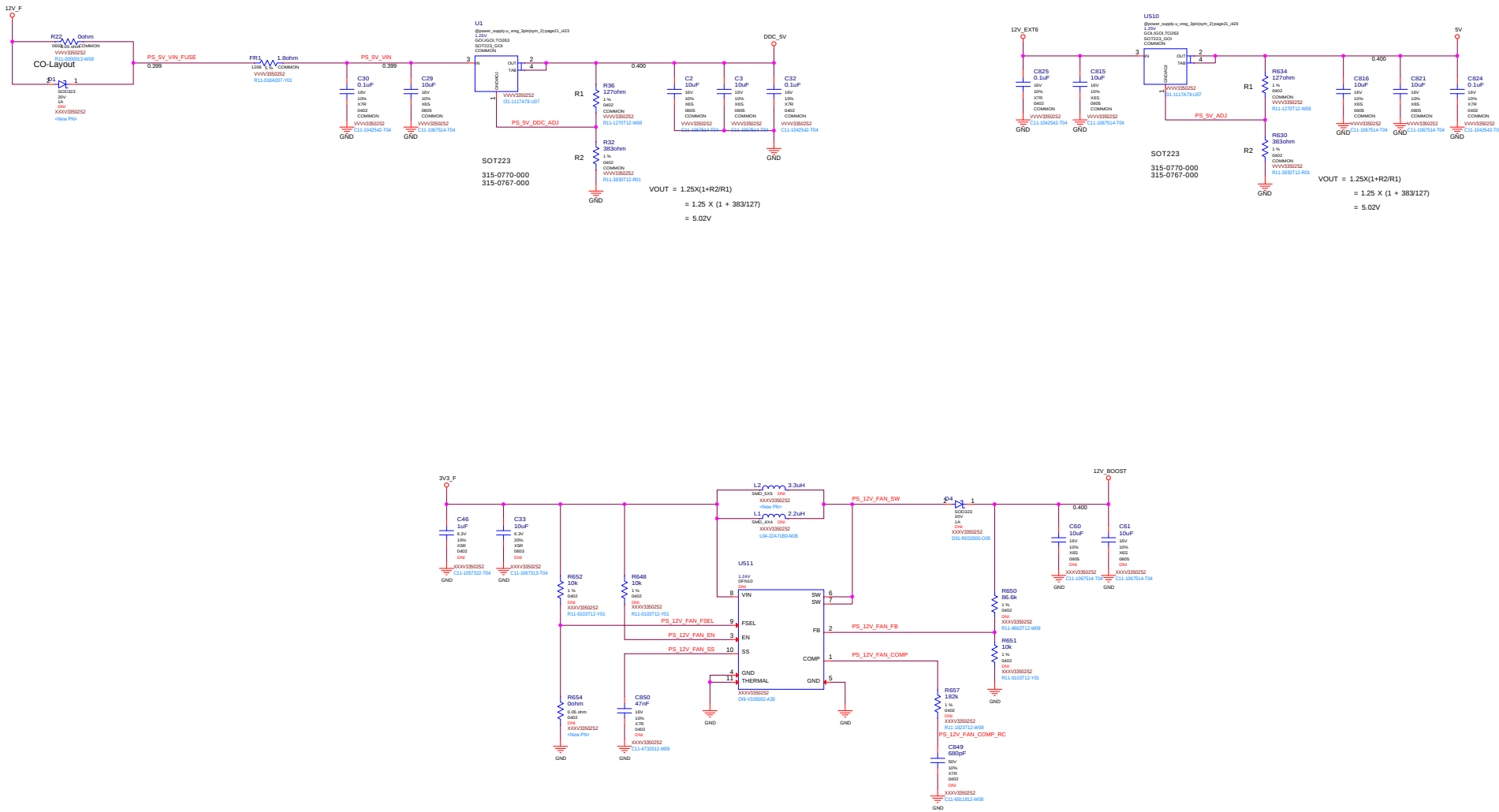
Power sequence



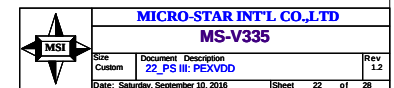
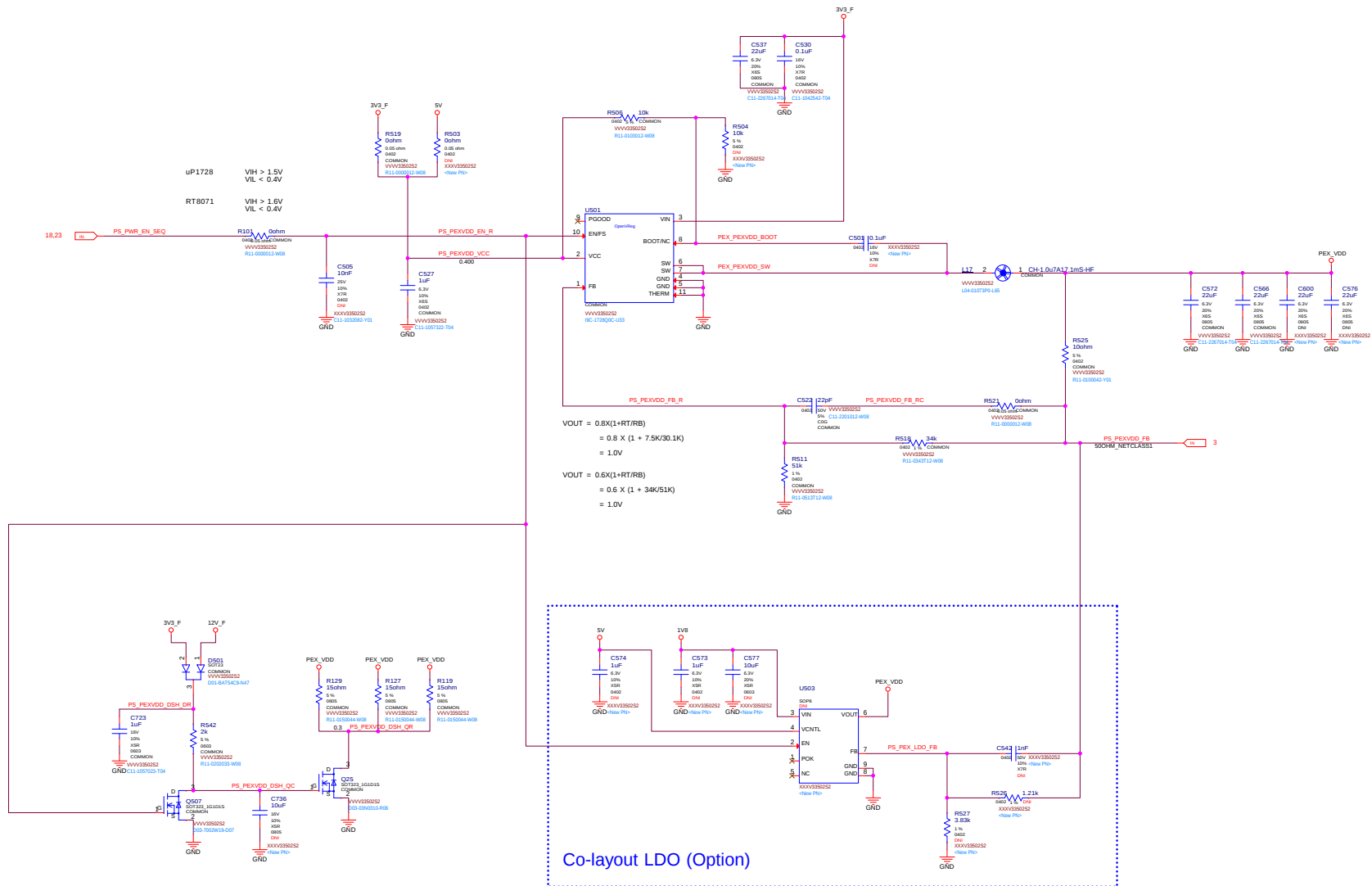
PS I: 1V8



PSII:5V & 12V_FAN



PS III: PEXVDD



PS IV: FBVDDQ

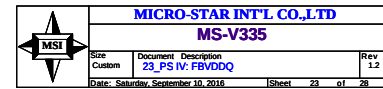
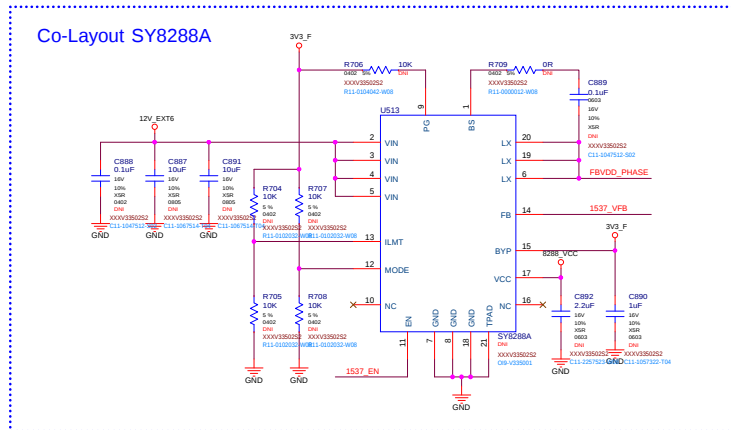
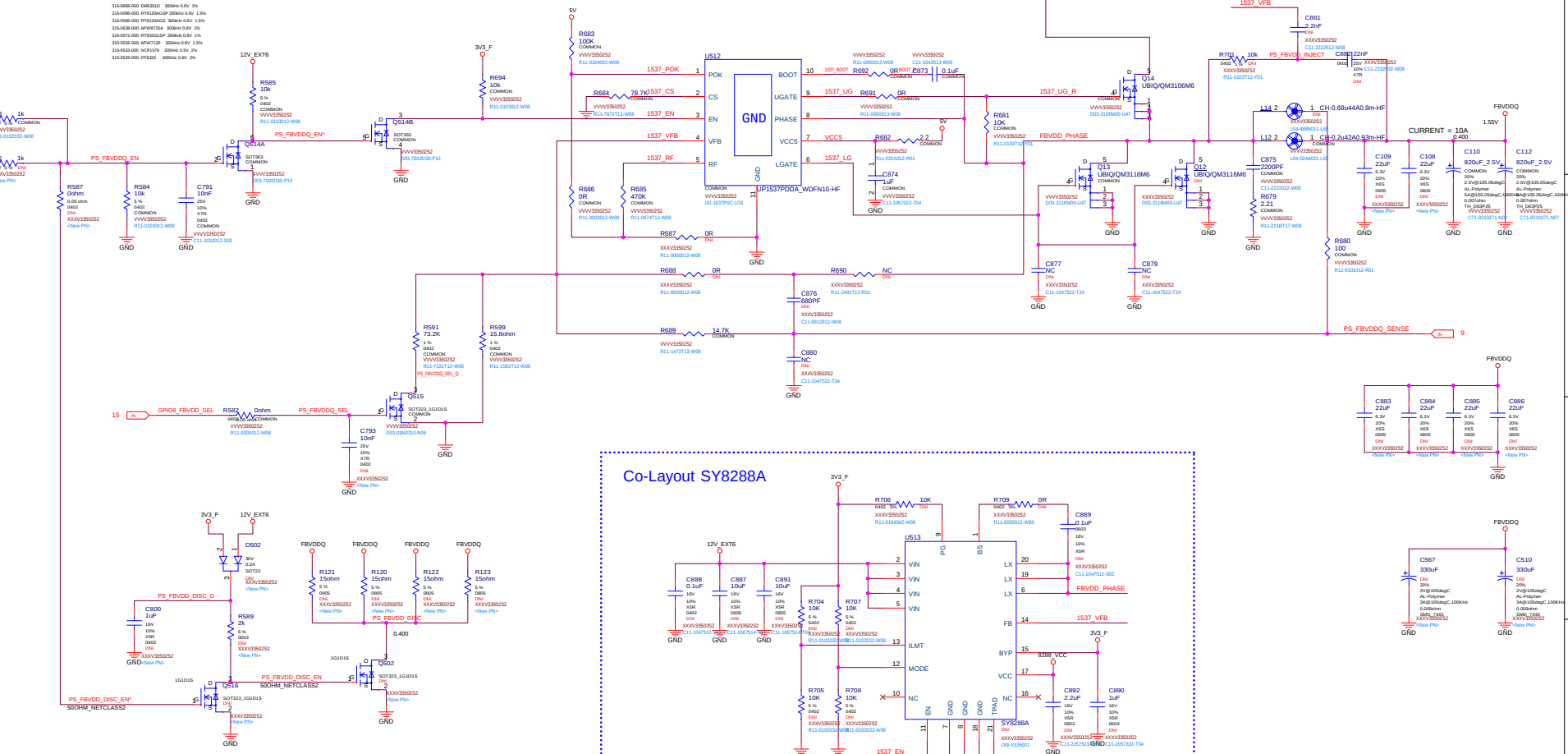
FBVDDQ_CTL	FBVDDQ	Non-DVS
X	1.5V	<= DEFAULT

FBVDDQ_CTL	FBVDDQ	For DVS
0	1.35V	
1	1.5V/1.55V	<= DEFAULT

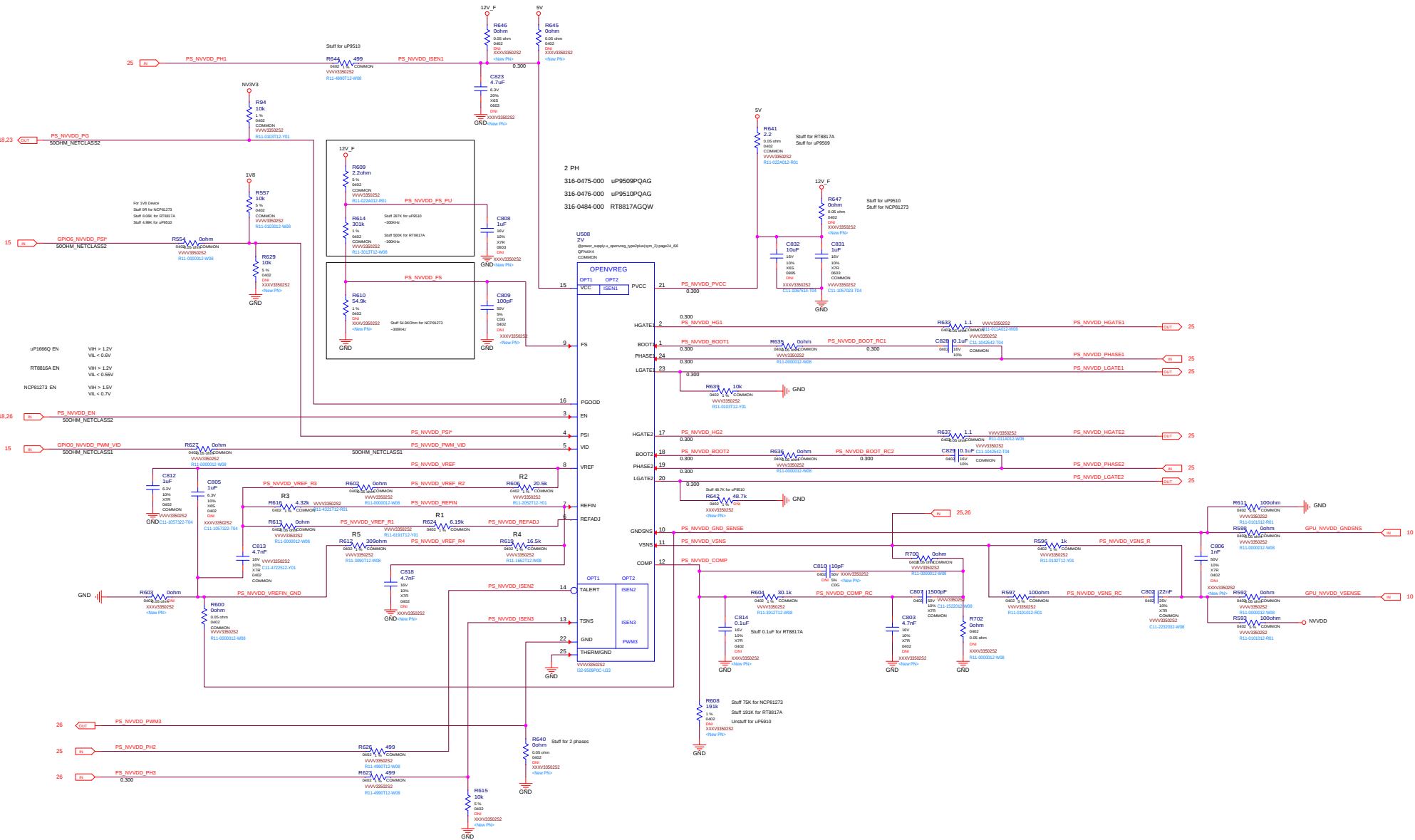
	Vnet = Vnet * (1+0.050)
Vnet=0.0V	1.50V = 0.0V * (1+0.050) 1.55V = 0.0V * (1+0.053)
Vnet=0.1V	1.50V = 0.1V * (1+0.011236) 1.55V = 0.1V * (1+0.01670)
	Vnet = Vnet * (1+0.050)
Vnet=0.0V	1.50V = 0.0V * (1+0.0703220) 1.55V = 0.0V * (1+0.0703288) 1.35V = 0.0V * (1+0.0707)
Vnet=0.1V	1.50V = 0.1V * (1+0.014305496) 1.55V = 0.1V * (1+0.014306126) 1.35V = 0.1V * (1+0.0143)
Vnet=0.700V	1.50V = 0.700V * (1+1.76773265558) 1.55V = 0.700V * (1+1.76753265558)

	PS	Freq	Vref	Tot
215-0625-000	APW8722	300kHz 0.5V	2%	
215-0688-000	EM5301D	300kHz 0.5V	2%	
215-0096-000	RT812DAGSP	300kHz 0.5V	1.5%	
215-0095-000	RT812DAGS	300kHz 0.5V	1.5%	
215-0638-000	APW8725A	300kHz 0.5V	2%	
215-0071-000	RT8021GSP	300kHz 0.5V	2%	
215-0526-000	APW7120	300kHz 0.5V	1.5%	
215-0523-000	NCP1579	300kHz 0.5V	2%	
215-0529-000	FP4526	300kHz 0.5V	2%	

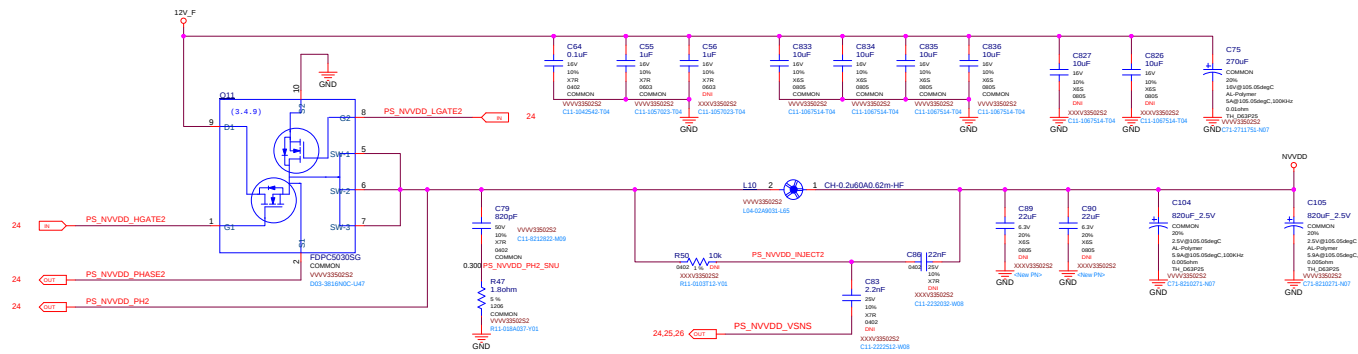
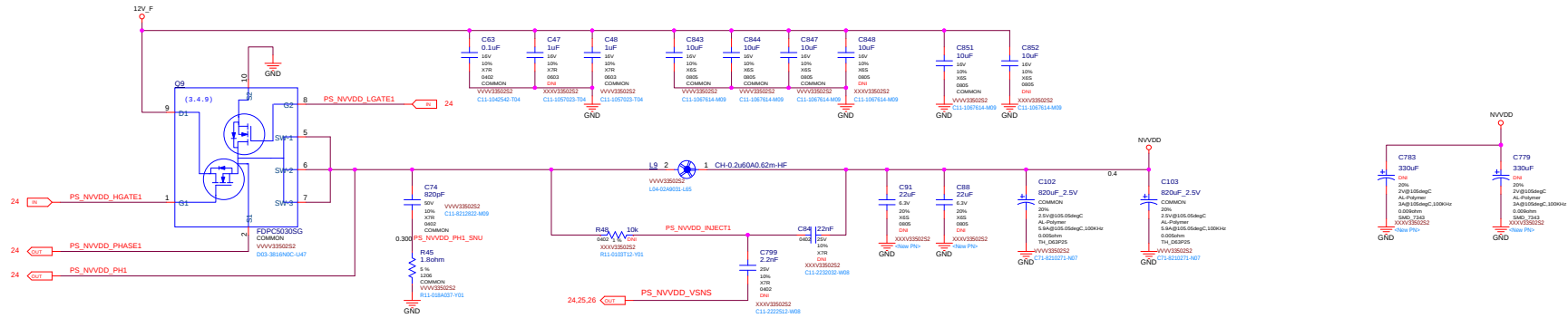
12V_EXT6



PS V: NVVDD OVR2+1



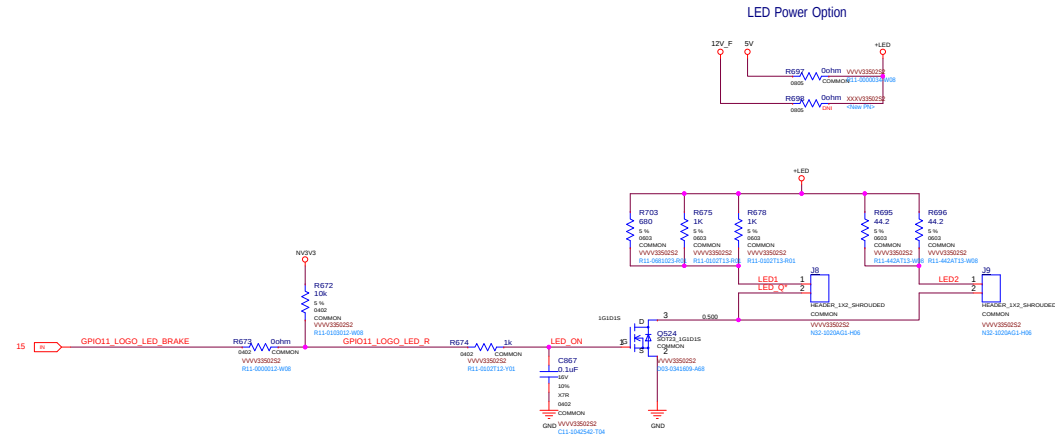
PS V: NVVDD Phase 1,2



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Size Custom	Document Description 25_PS V: NVDD Phase 1,2	Rev 1.2
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Logo LED



Mechanical: Bracket/Thermal Solution

Brackets:

