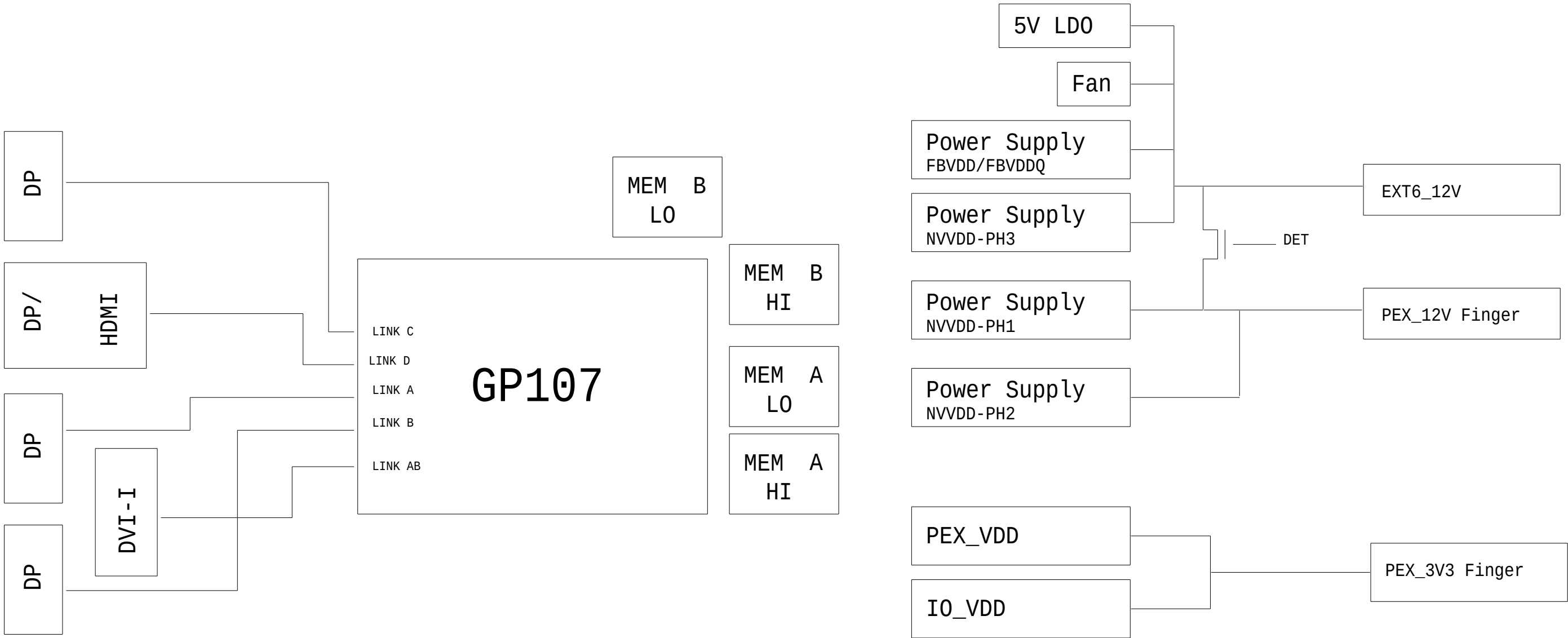


Block Diagram



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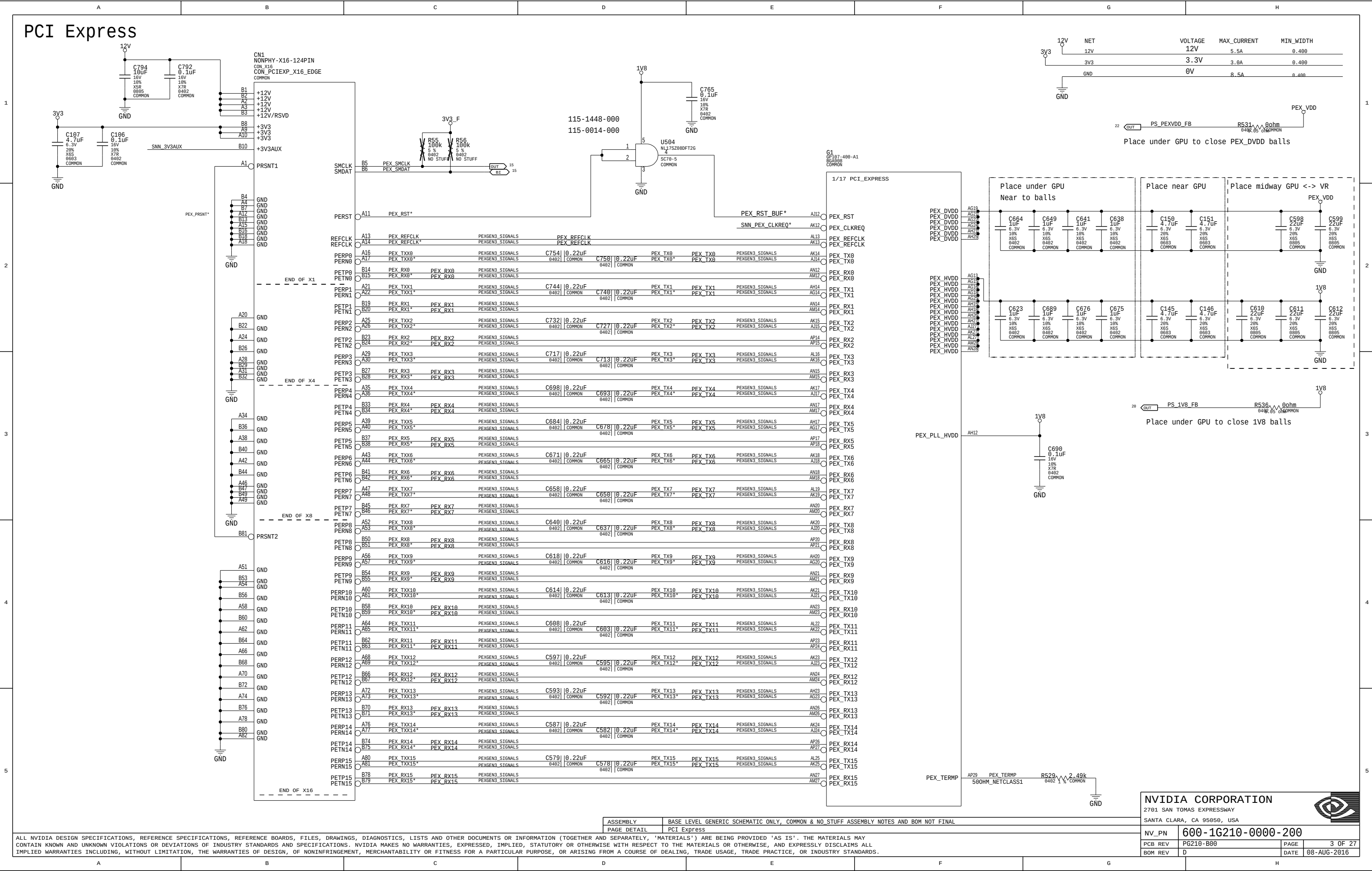
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PCI Express



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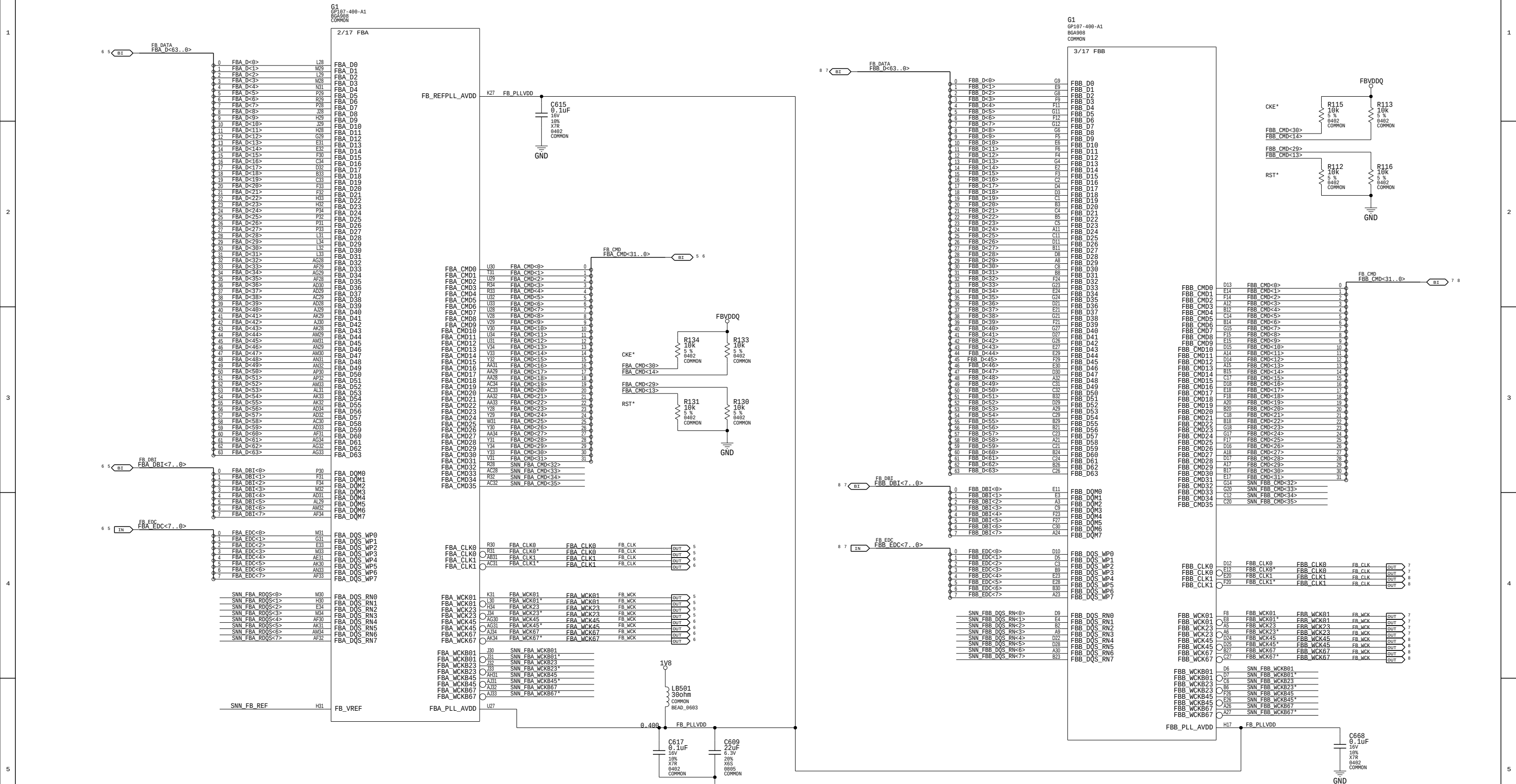
PAGE

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MEMORY: GPU Partition A/B



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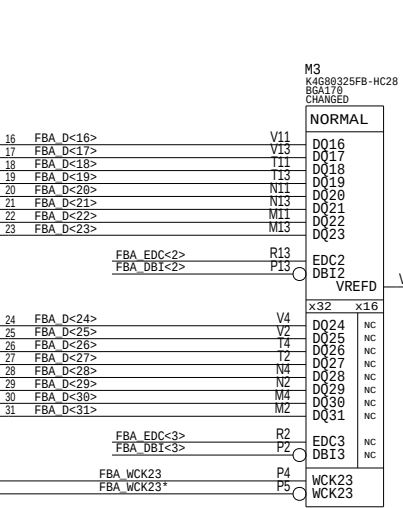
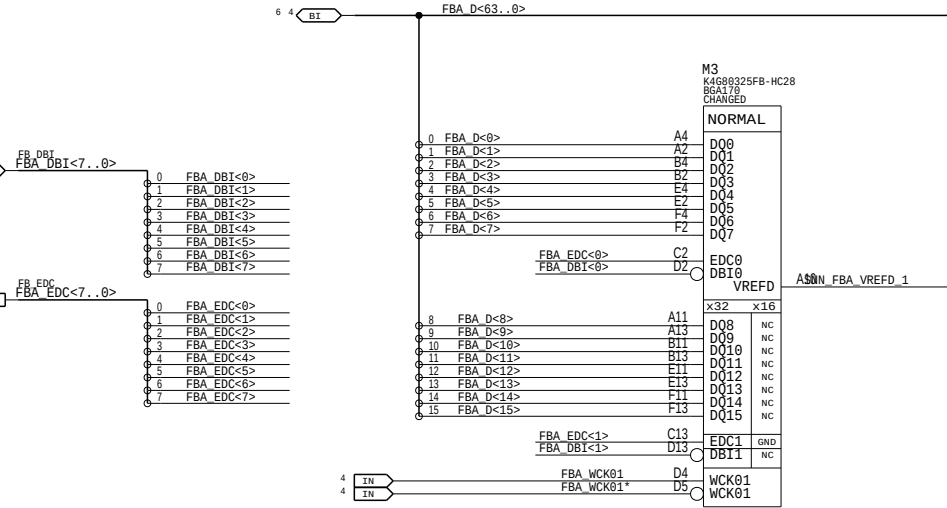
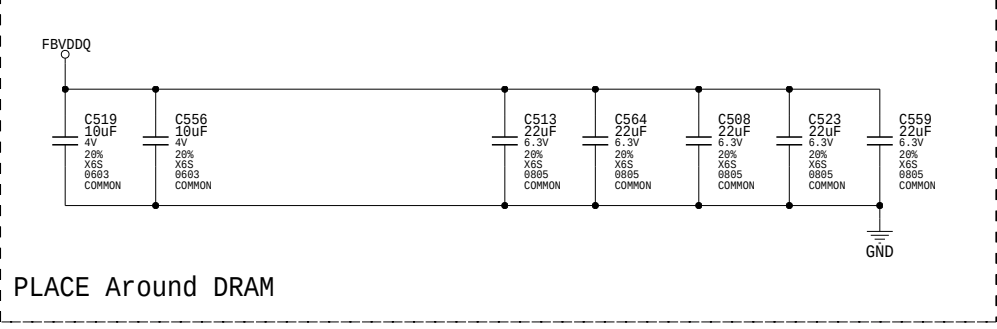
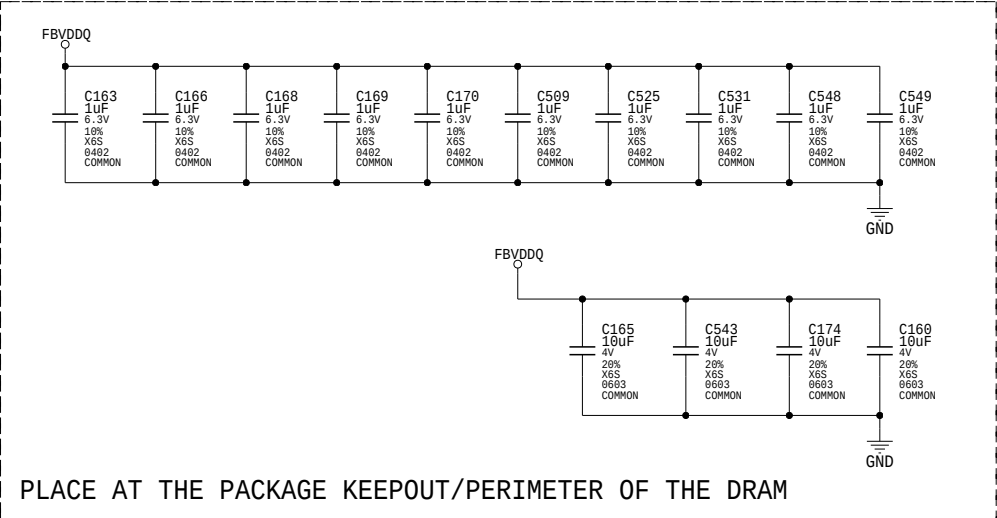
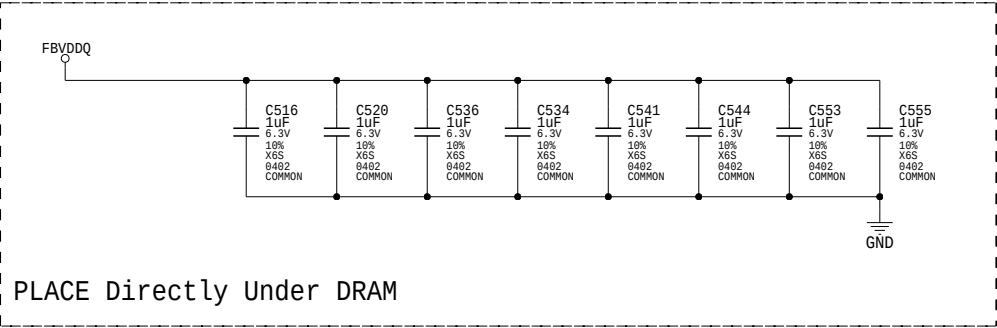
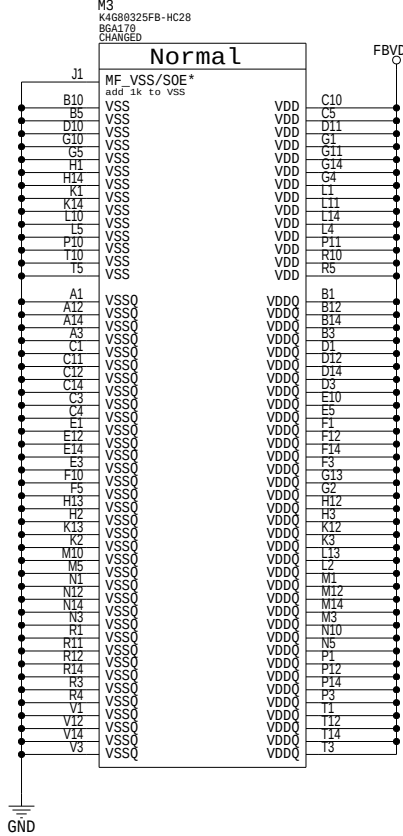
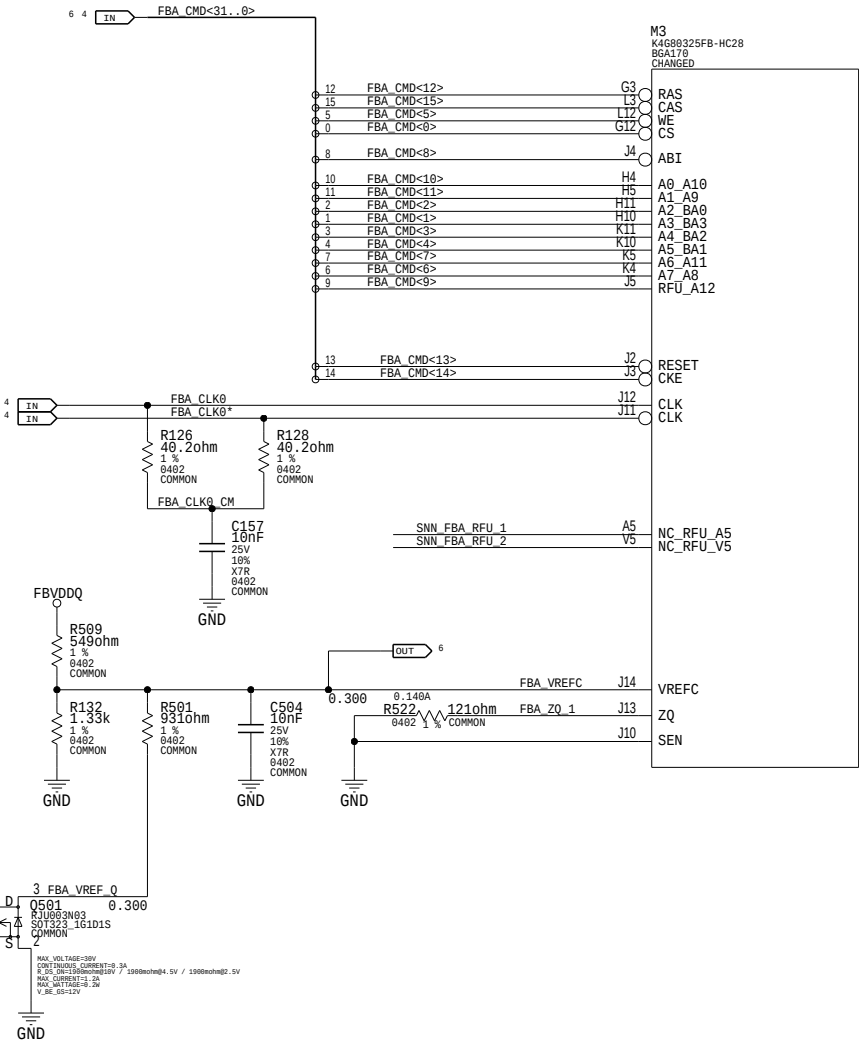
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MEMORY: GPU Partition A/B

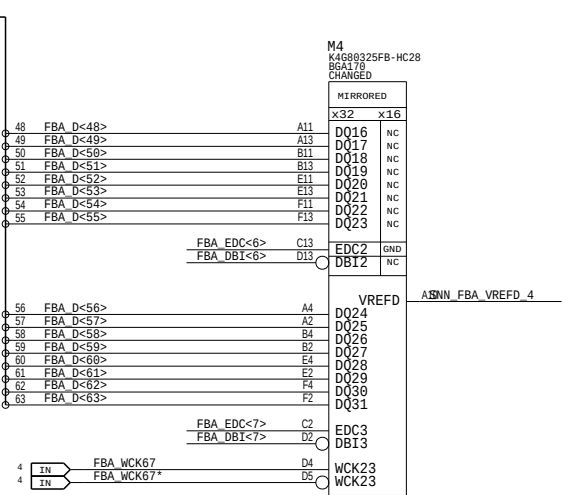
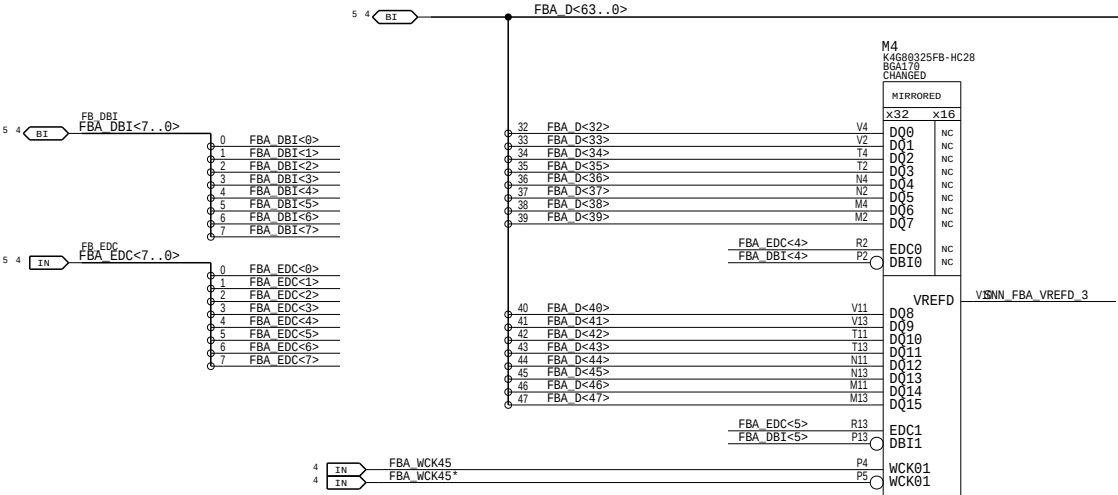
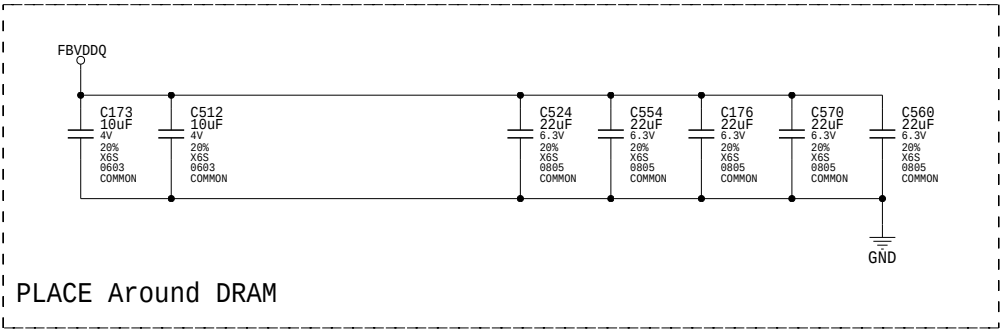
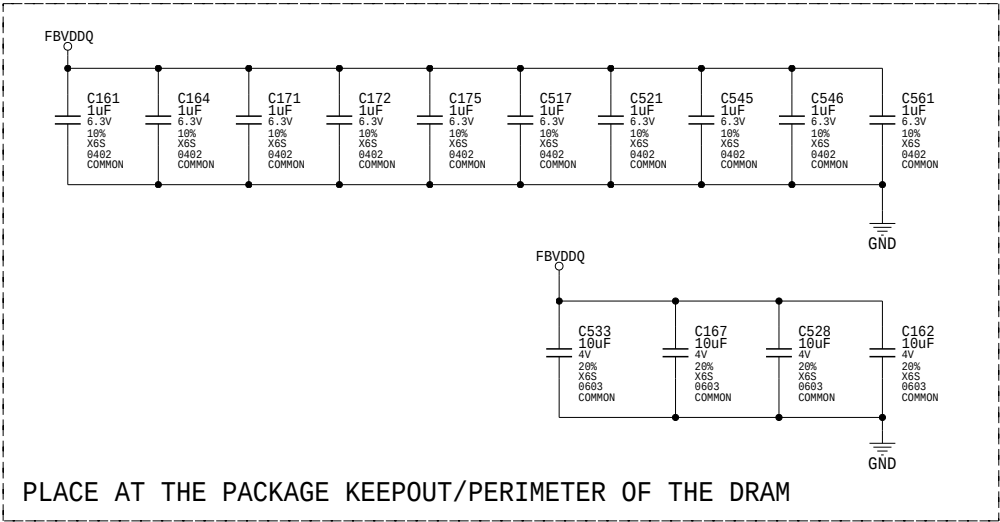
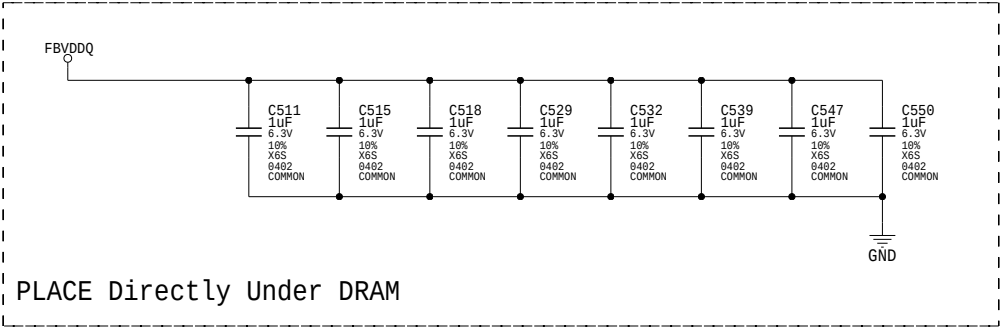
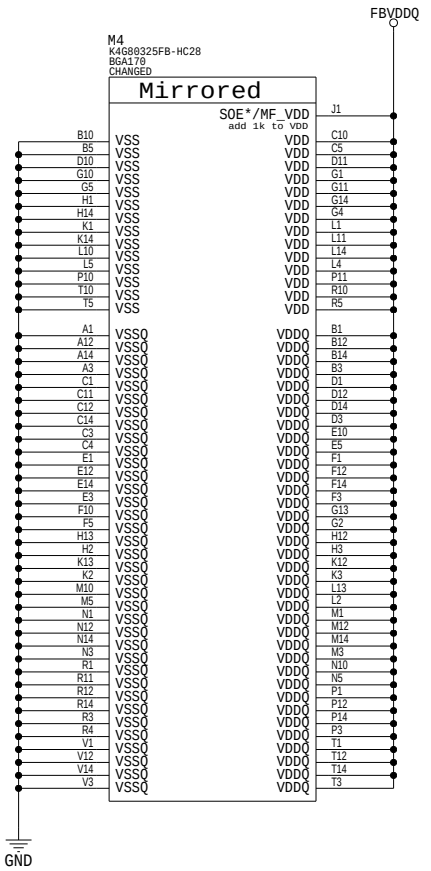
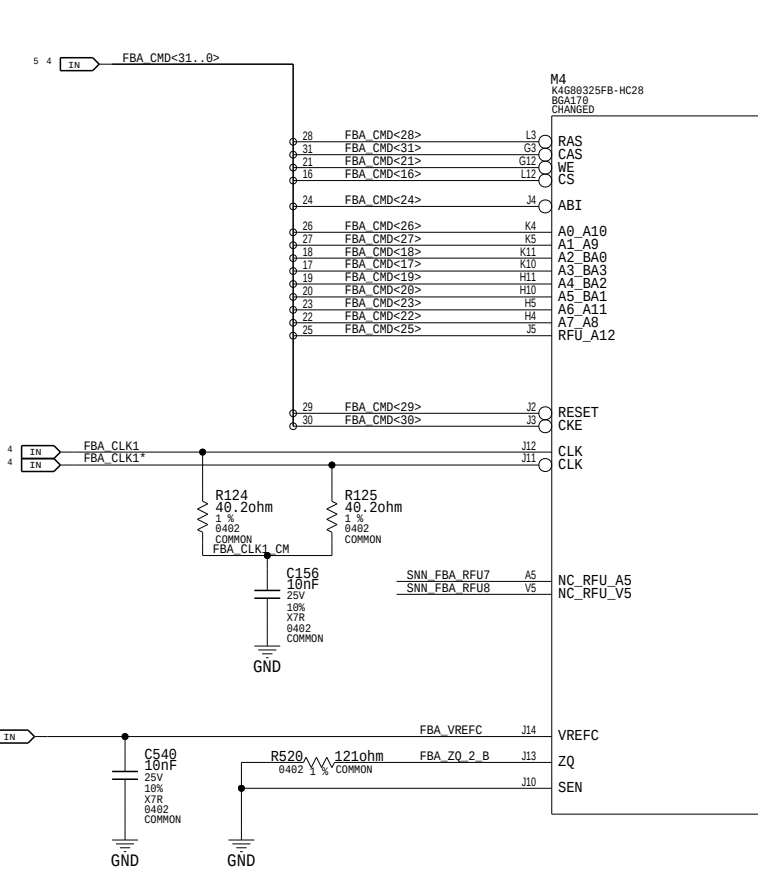
MEMORY: FBA Partition 31..0

CMD	0..31	32..63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABT*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABT*
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*



MEMORY: FBA Partition 63..32

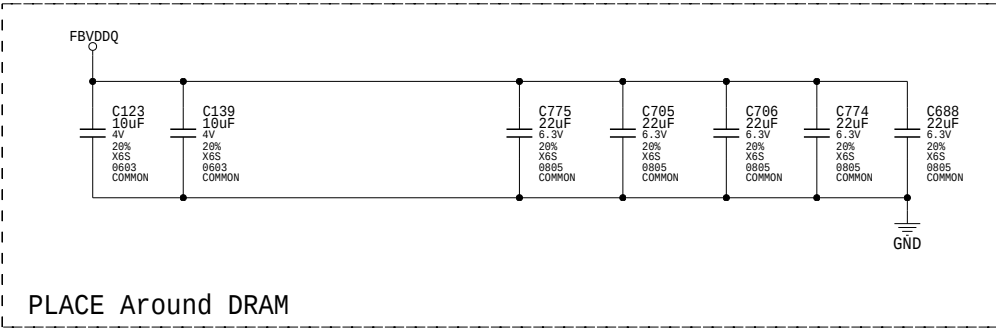
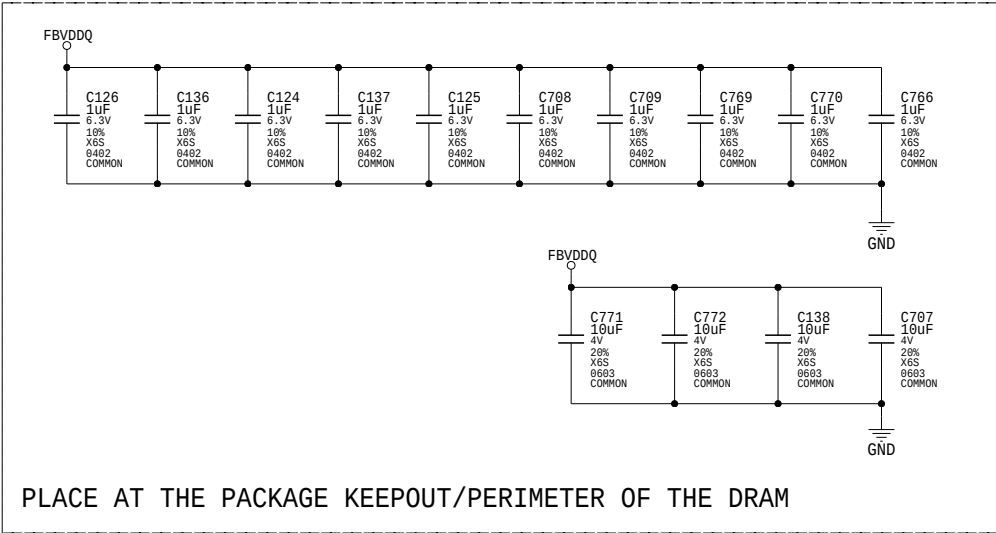
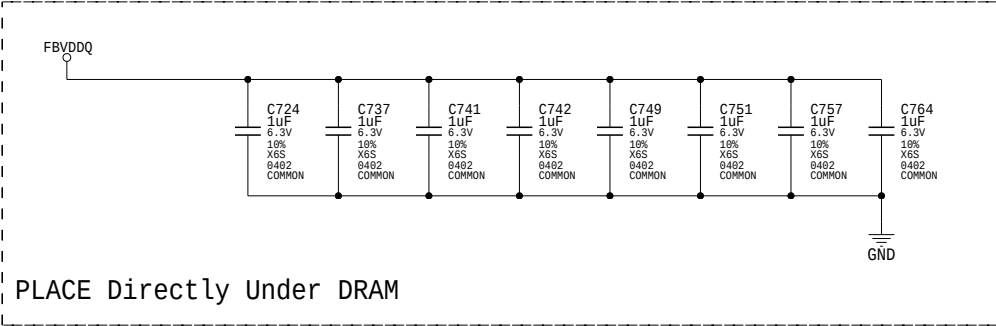
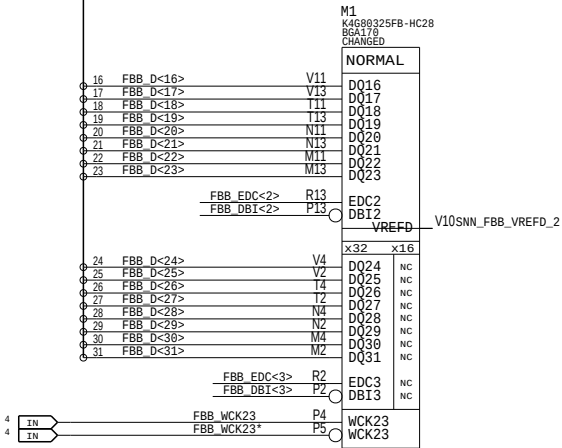
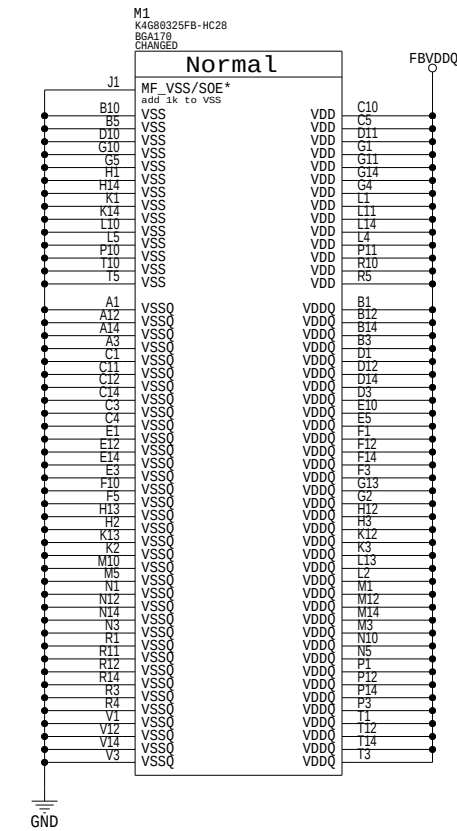
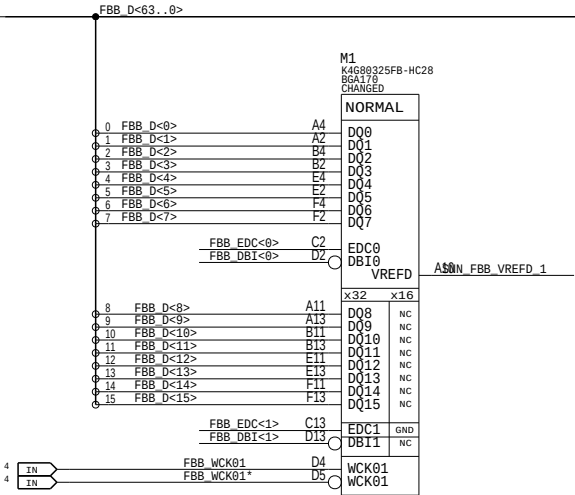
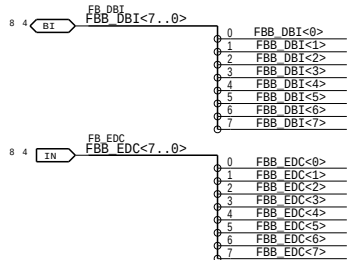
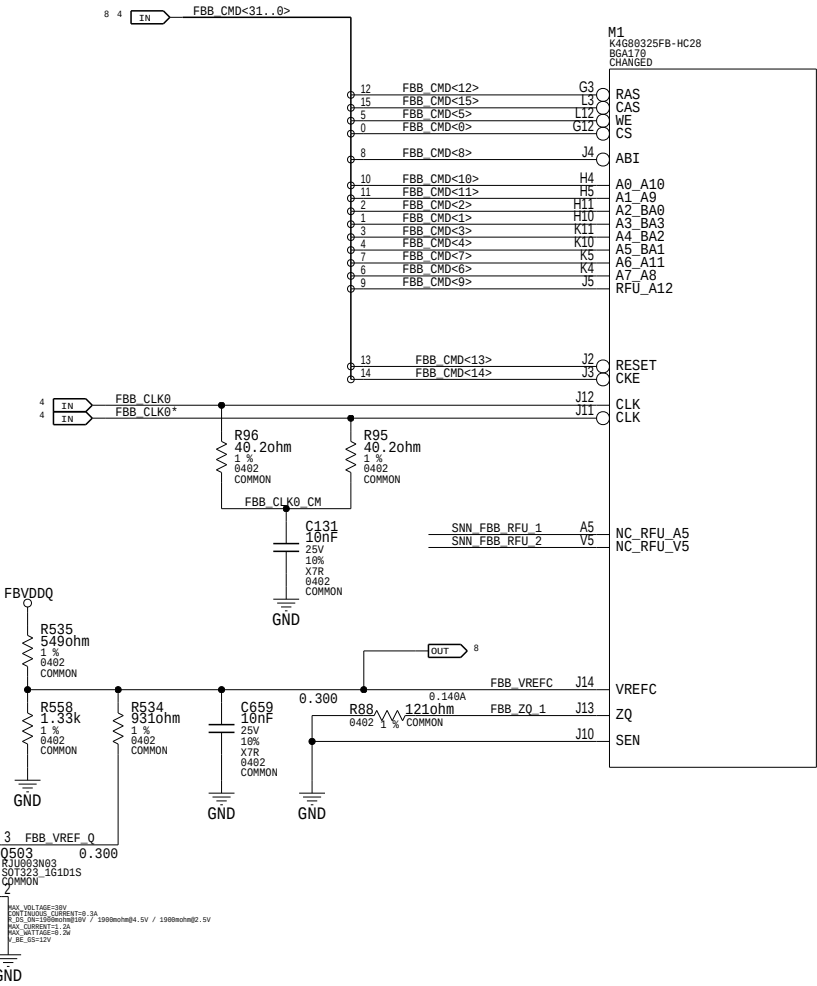
CMD	0..31	32..63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	AB1*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		AB1*
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*



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MEMORY: FBB Partition 31..0

CMD	0..31	32..63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABT*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16	CS*	
CMD17	A3_BA3	
CMD18	A2_BA0	
CMD19	A4_BA2	
CMD20	A5_BA1	
CMD21	WE*	
CMD22	A7_A8	
CMD23	A6_A11	
CMD24	ABT*	
CMD25	A12_RFU	
CMD26	A0_A10	
CMD27	A1_A9	
CMD28	RAS*	
CMD29	RST*	
CMD30	CKE*	
CMD31	CAS*	



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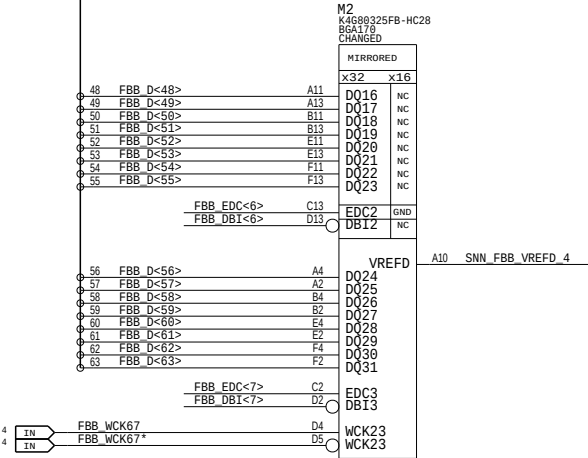
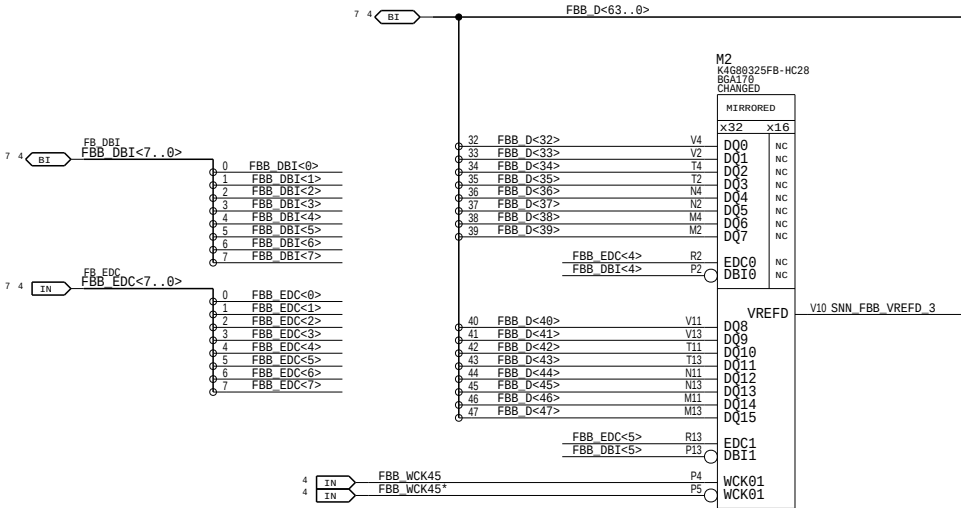
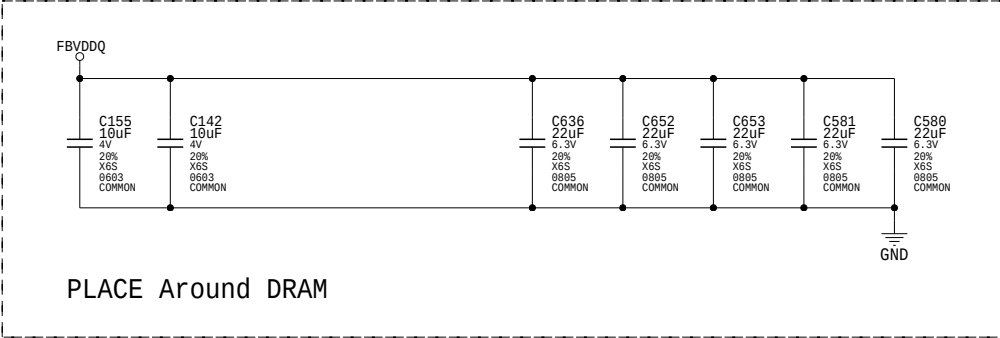
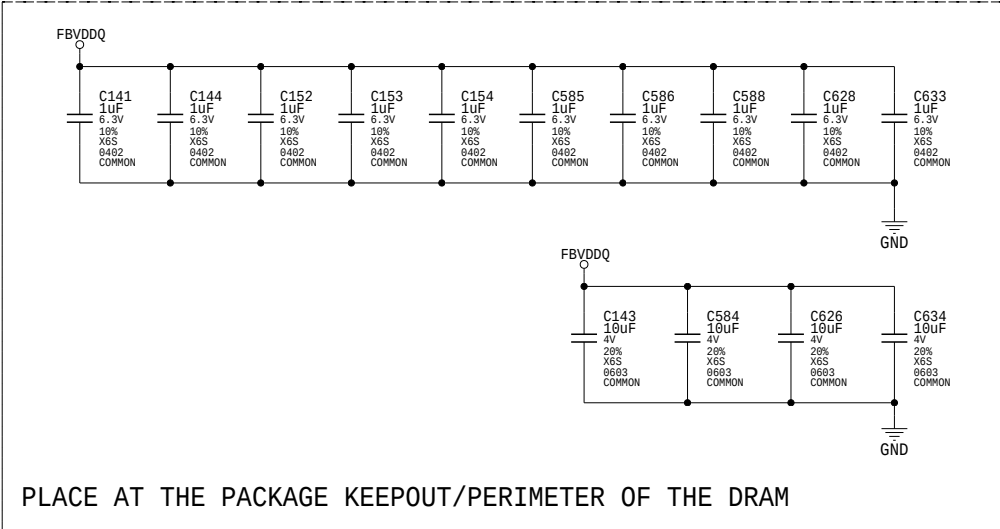
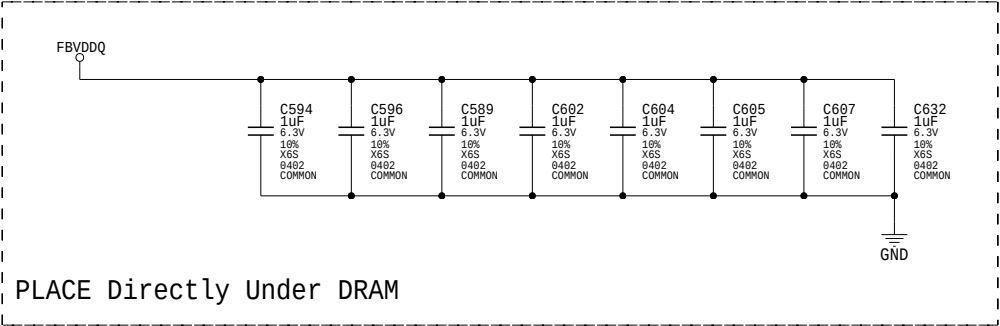
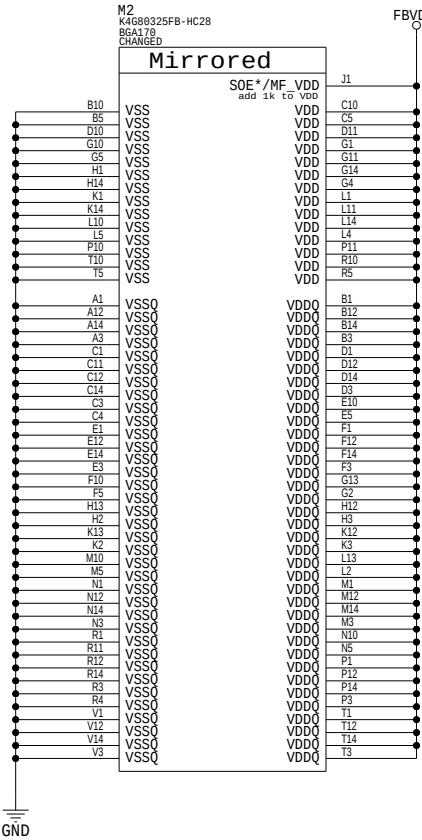
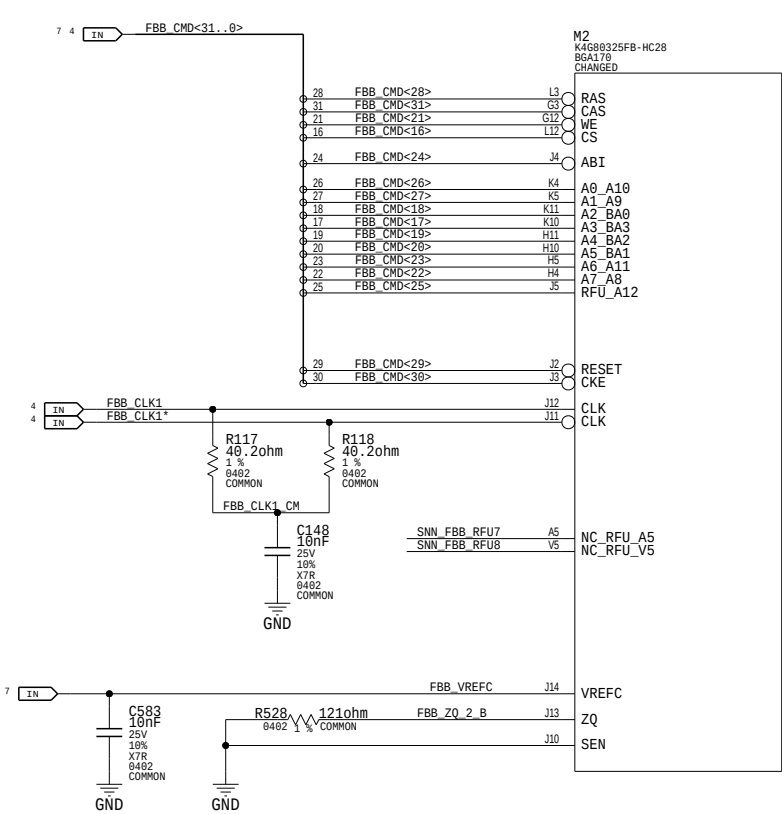
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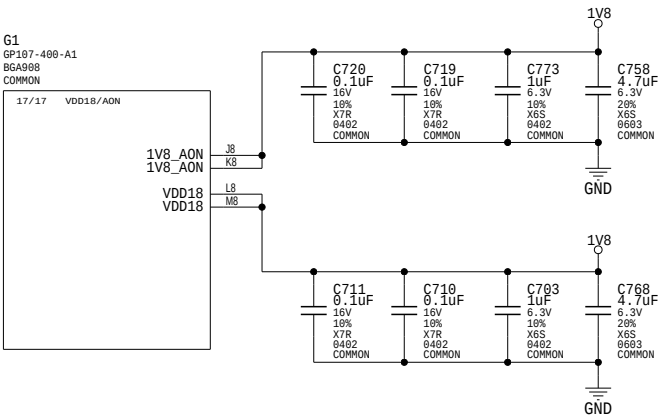
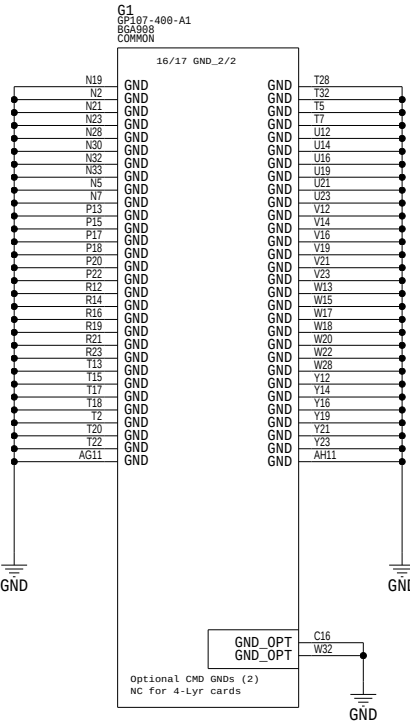
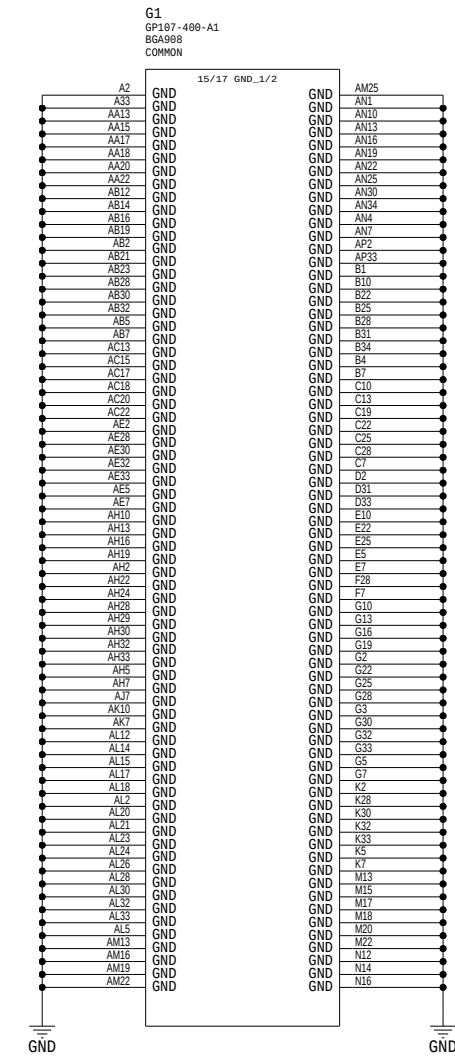
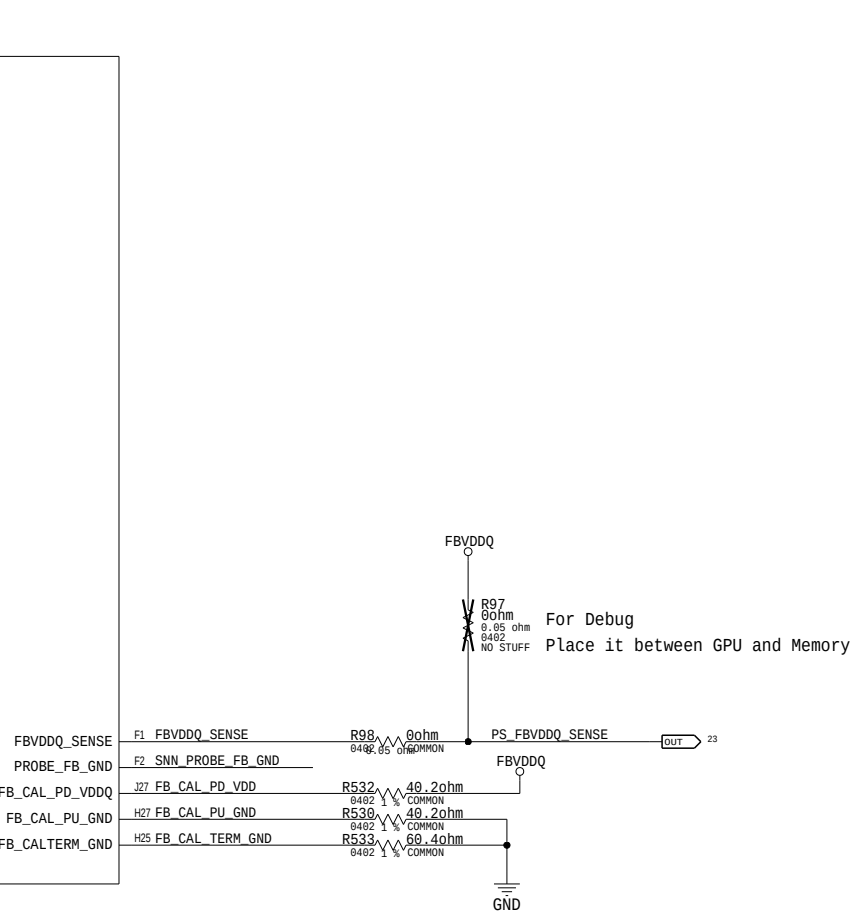
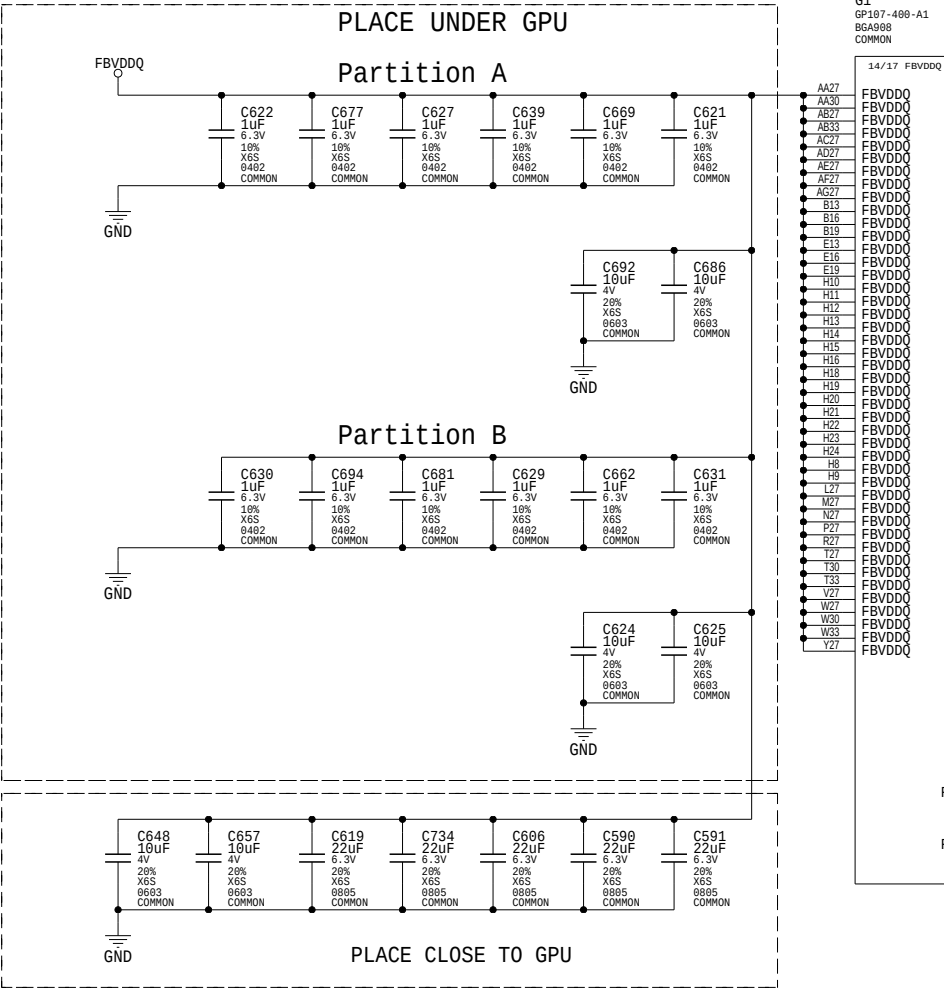
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BOM REV D DATE 08-AUG-2016

MEMORY: FBB Partition 63..32

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CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABT*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABT*
CMD25		A12_RFU
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CMD27		A1_A9
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*

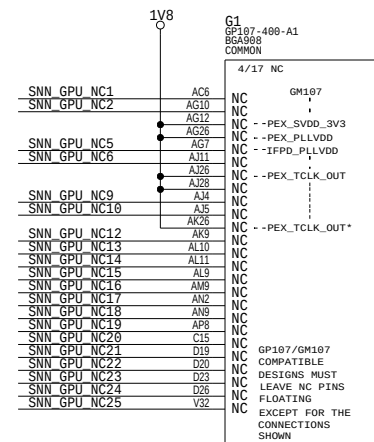
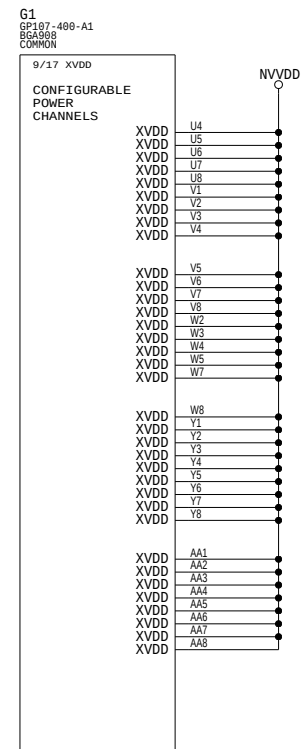
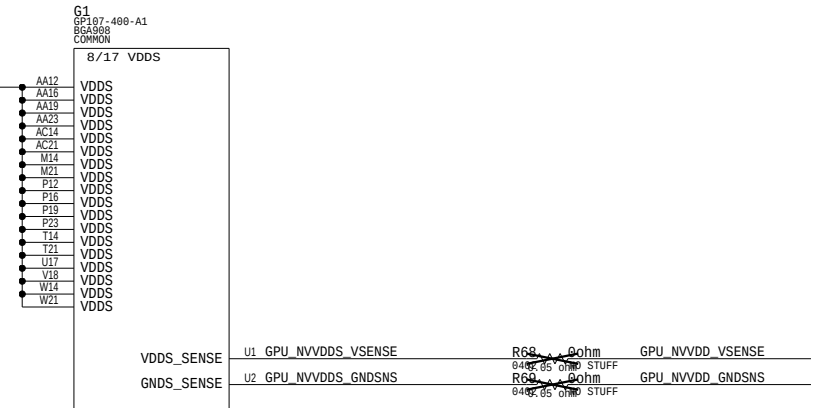
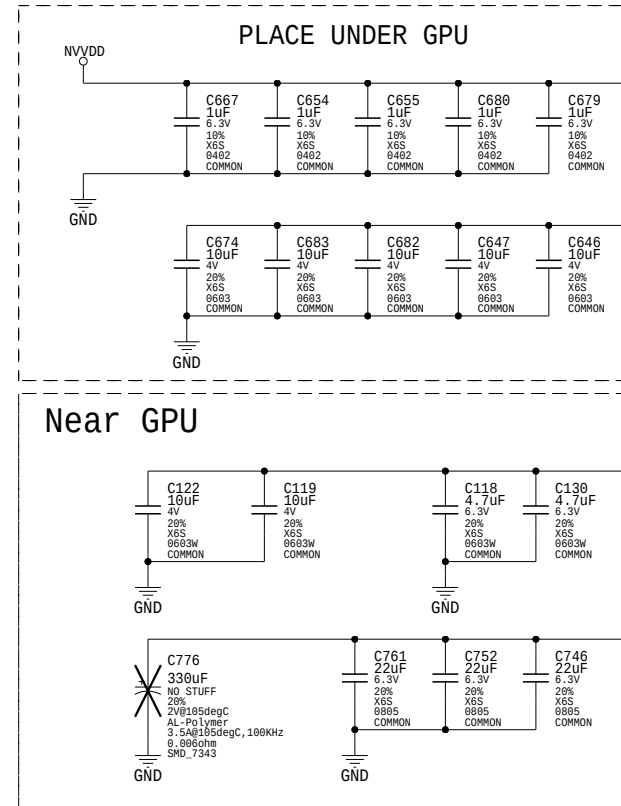
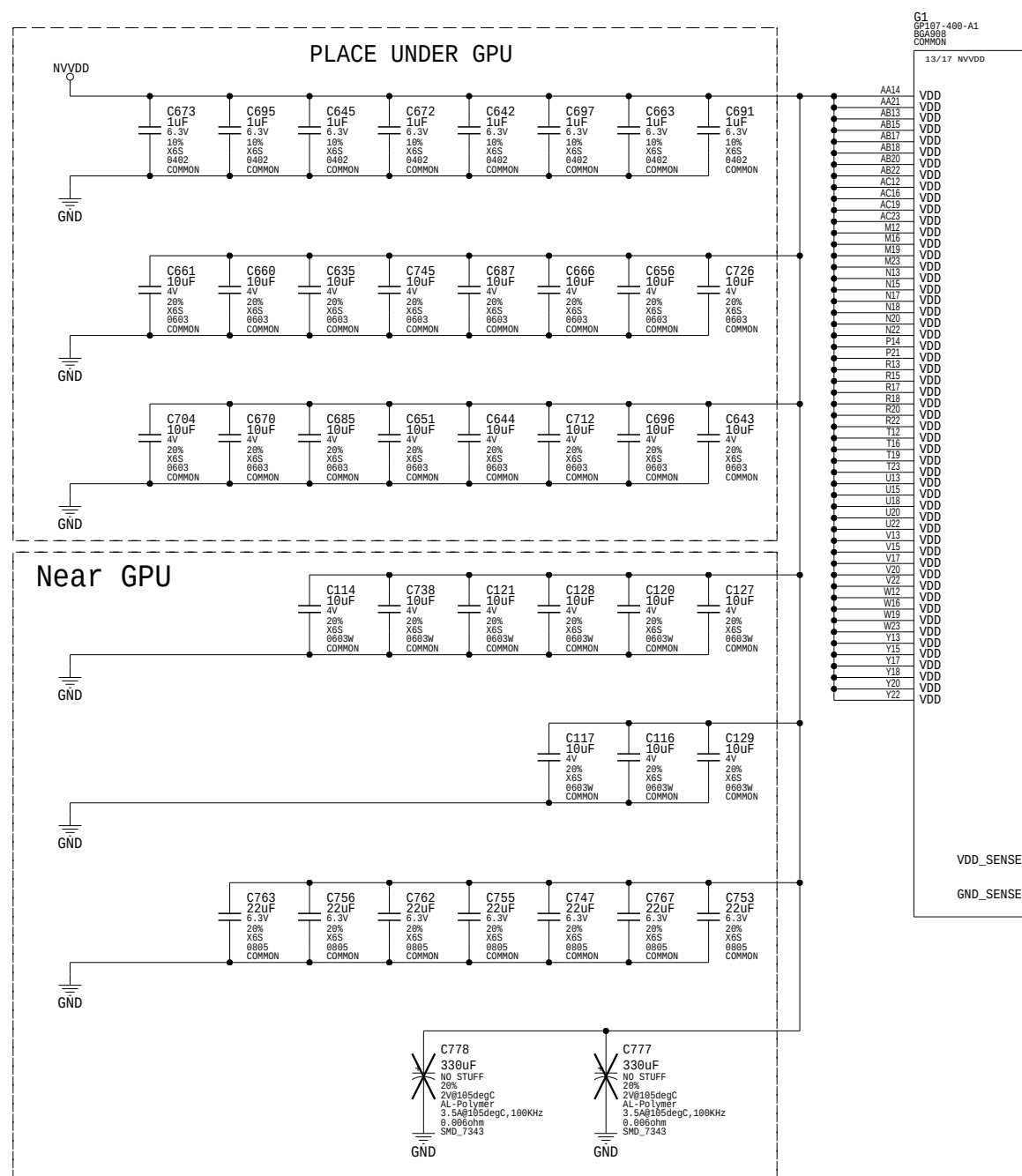


GPU FBVDDQ & 1V8 Decoupling



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GPU NVVDD & NVVDDS Decoupling



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IFPD DP

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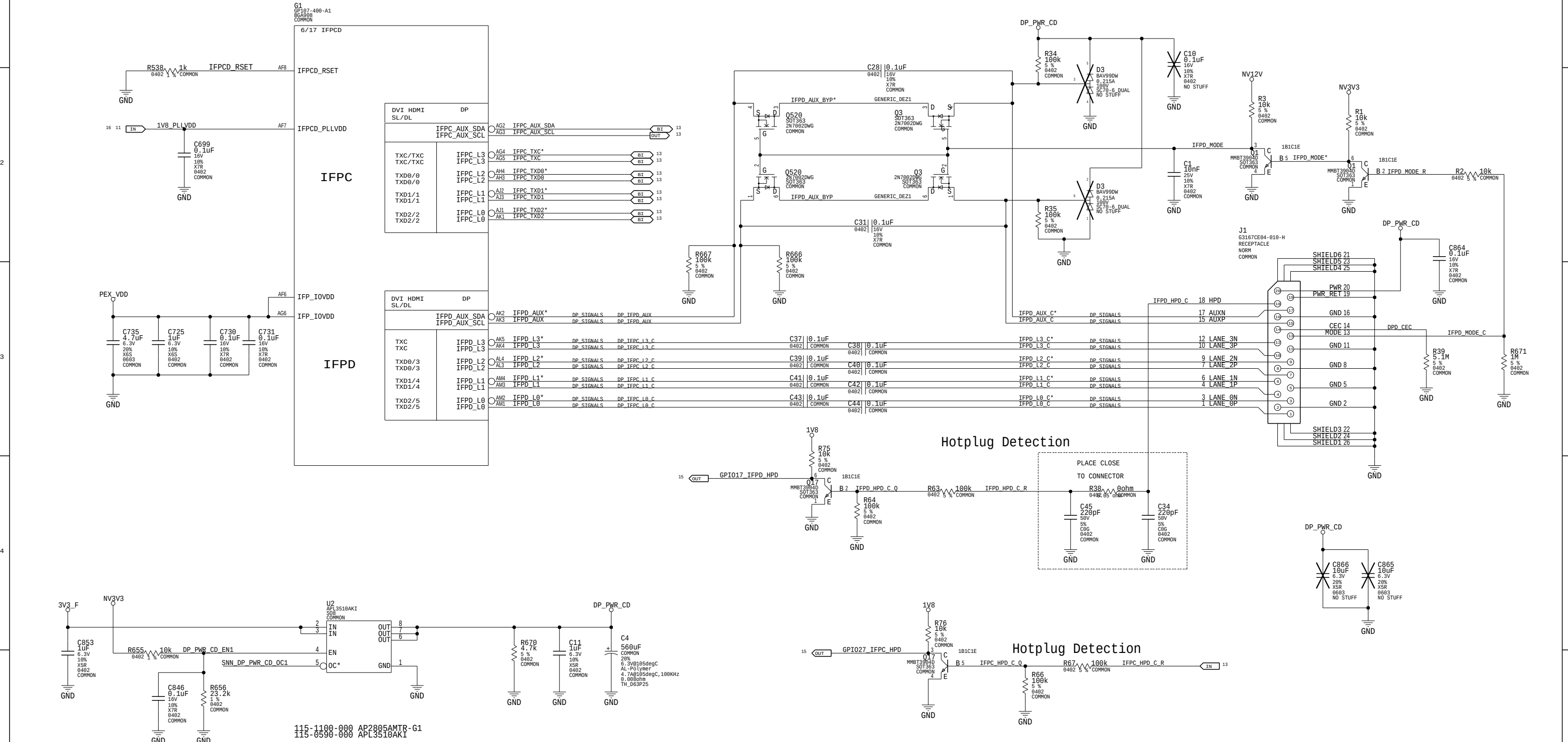
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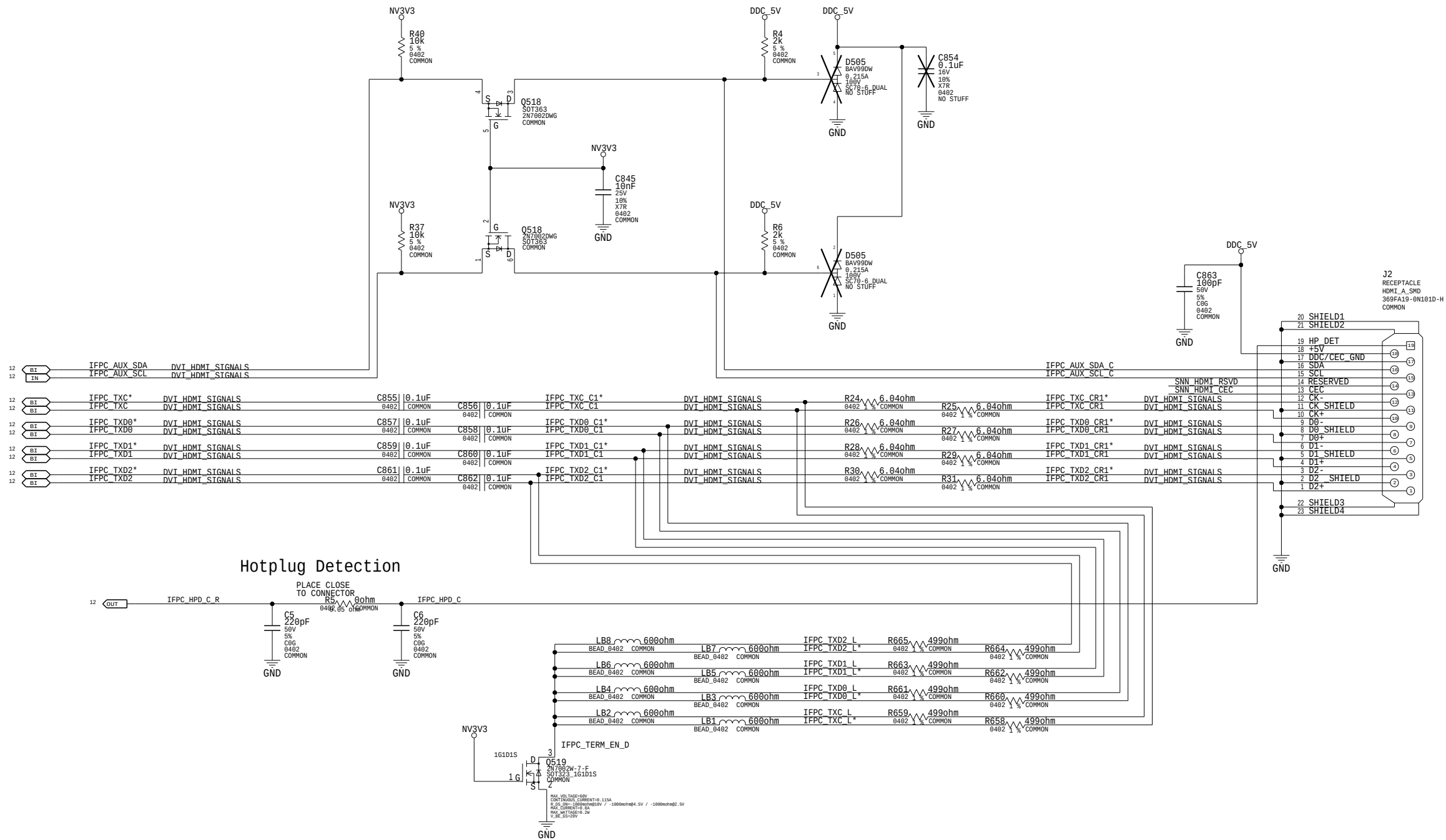
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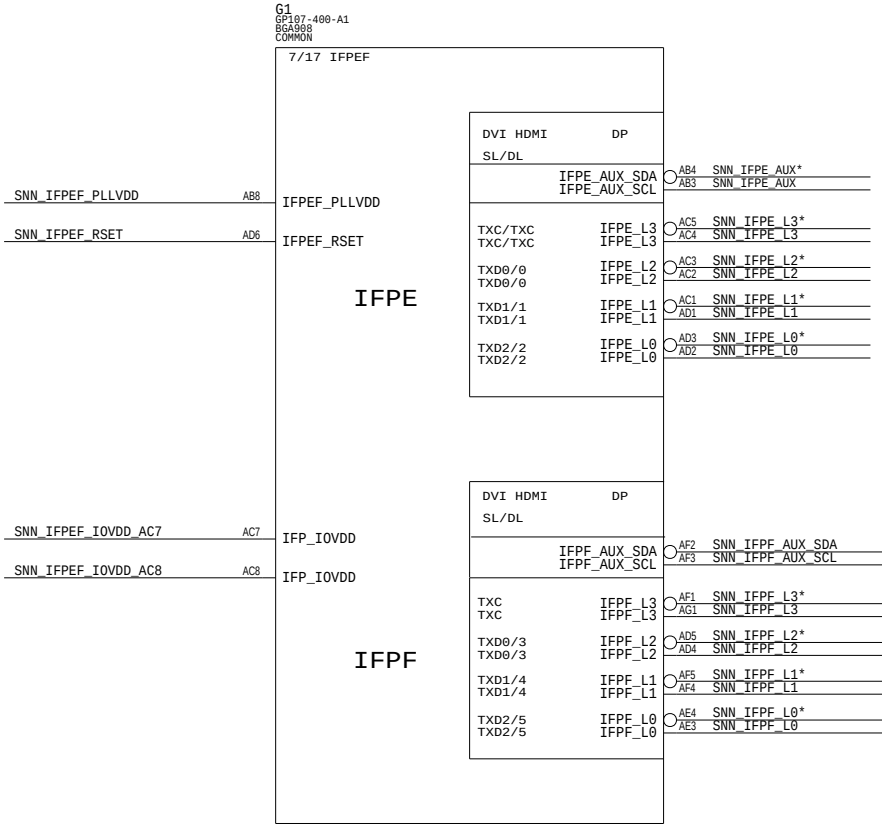
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IFPC HDMI



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFPEF UNUSED

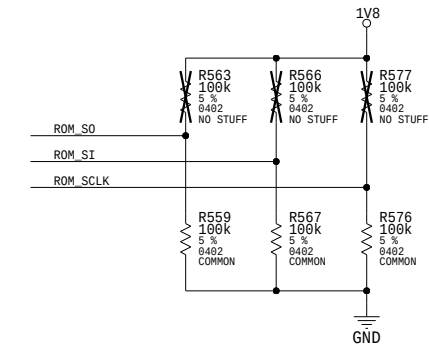
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MISC2: ROM, XTAL, Straps

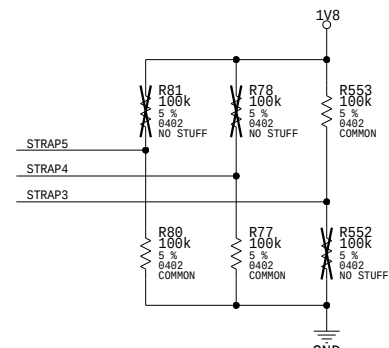
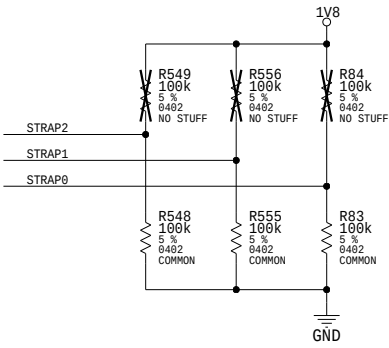
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111	Default
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	Samsung B-Die 8Gb 256Mx32
L	L	H	0001	Micron F-Die 8Gb 256Mx32
L	H	L	0010	Hynix M-Die 8Gb 256Mx32
L	H	H	0011	
H	H	L	0110	Hynix A-Die 4Gb 128Mx32
H	H	H	0111	Samsung E-Die 4Gb 128Mx32
L	L	M	1000	Micron B-Die 4Gb 128Mx32
L	M	L	1001	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0



H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

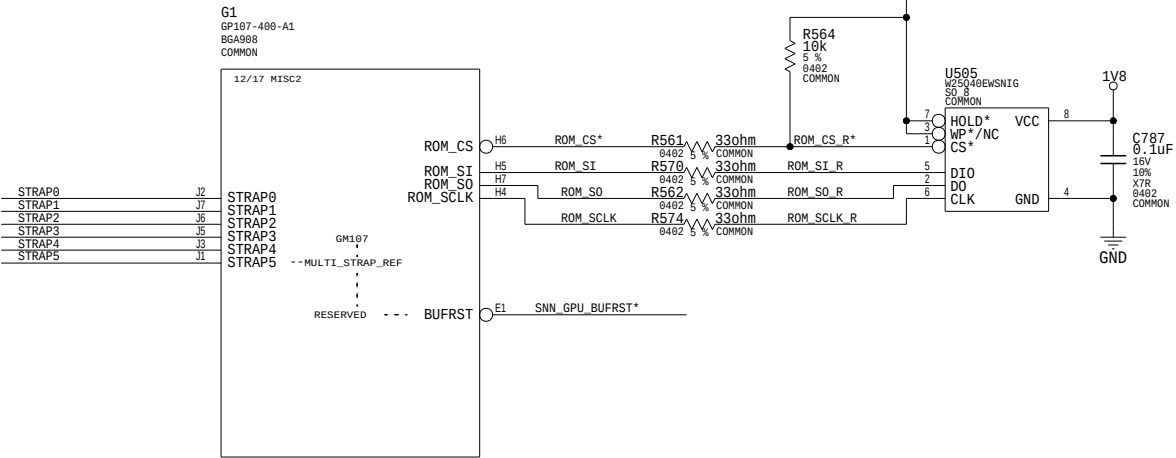


1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

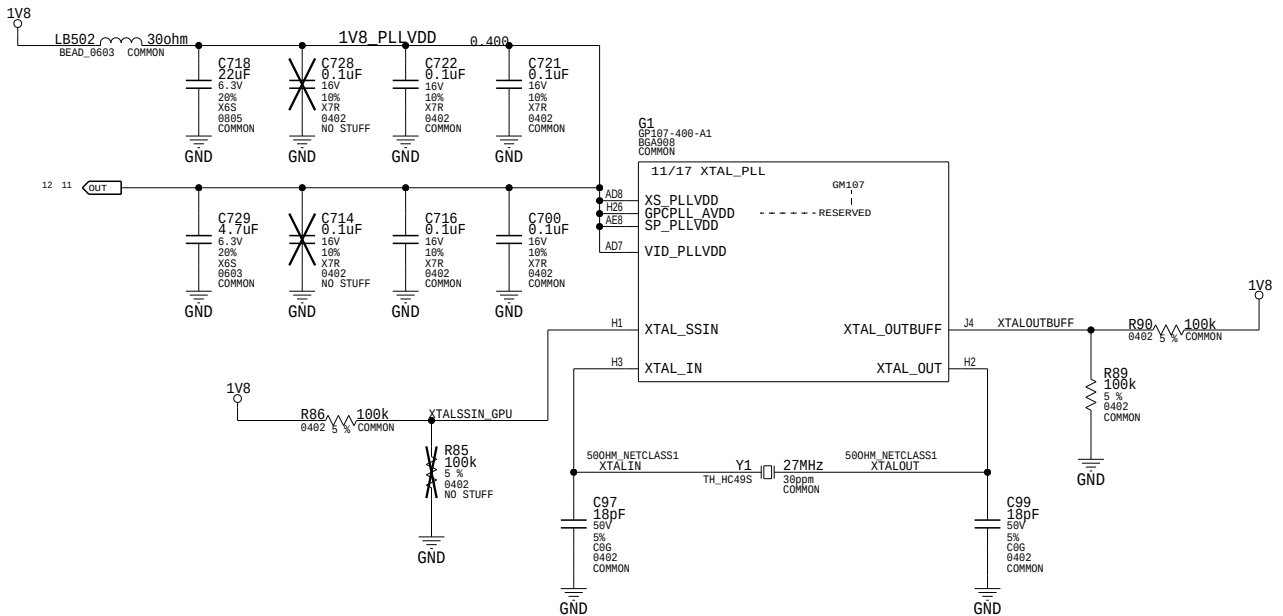
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



Smart Fan

XTALOUTBUFF	Volatge	SmartFan PWM	GPIO/PWM at the FAN
Low	0V	GPIO Disabled	100%
Middle	0.9V	66% PWM	33% PWM (Typical)
High	1.8V	33% PWM	66% PWM

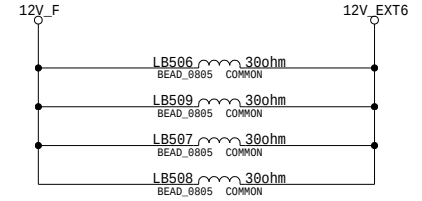
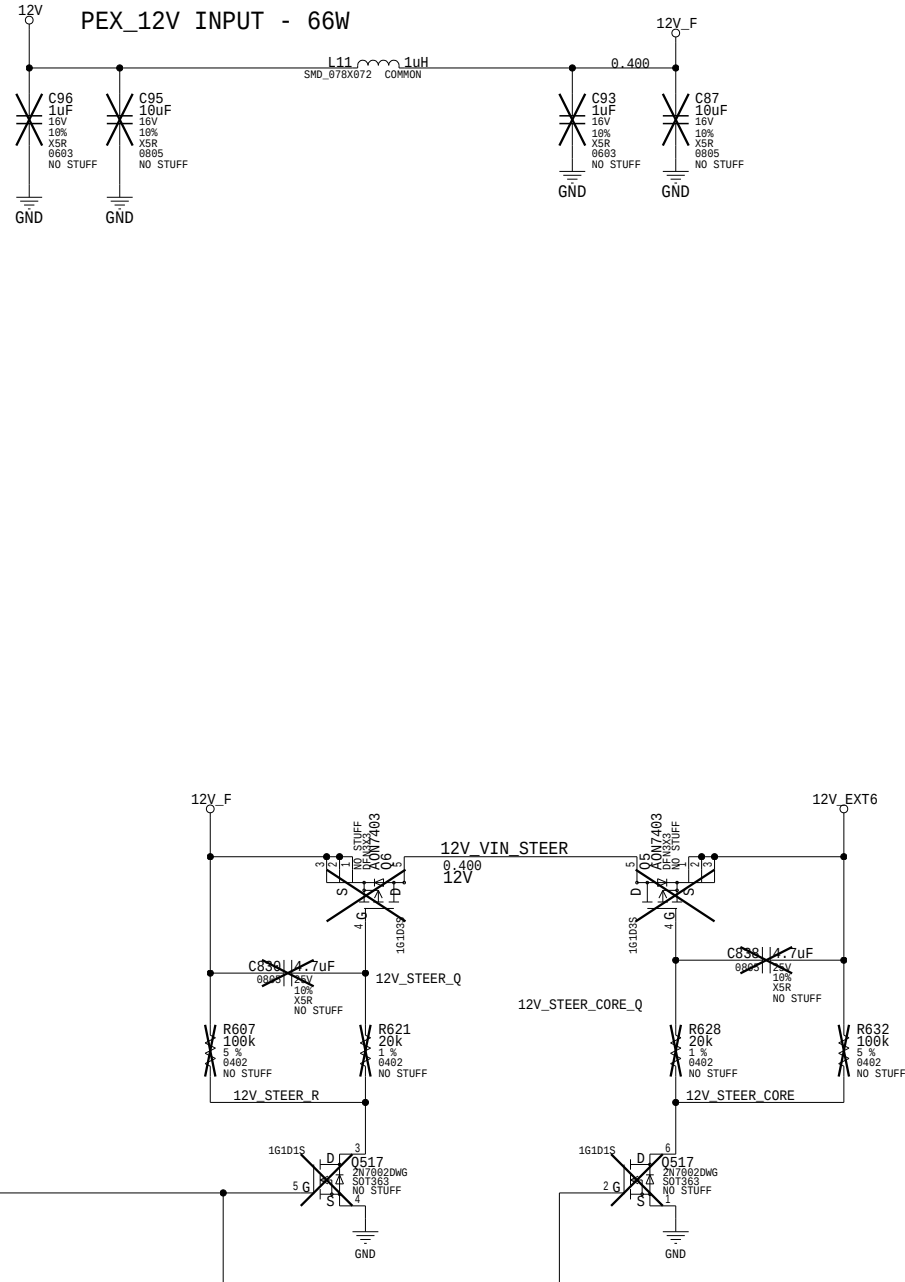
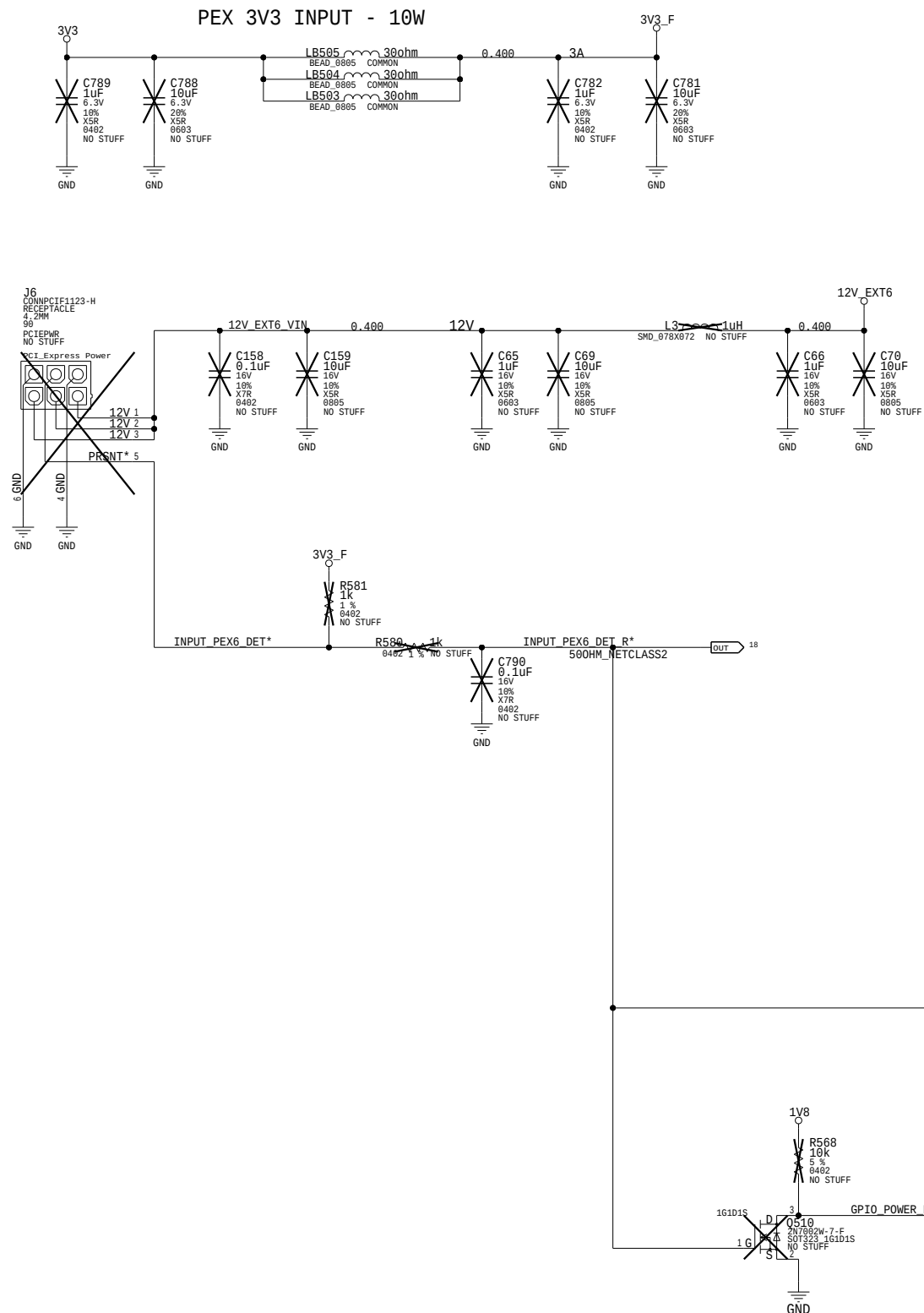


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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MISC2: ROM, XTAL, Straps

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Power Inputs and Filtering



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PAGE DETAIL	Power Inputs and Filtering

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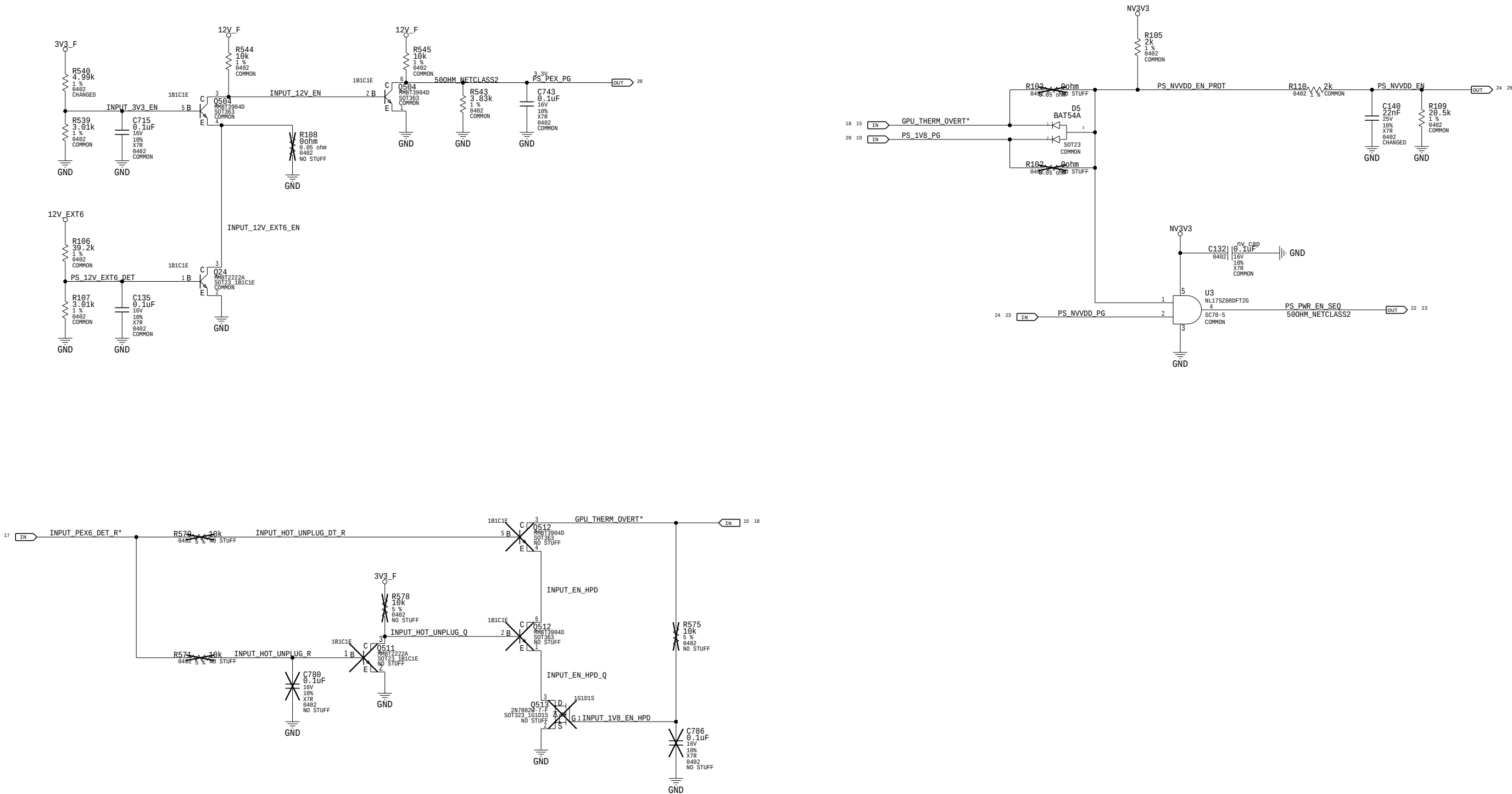
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Power sequence



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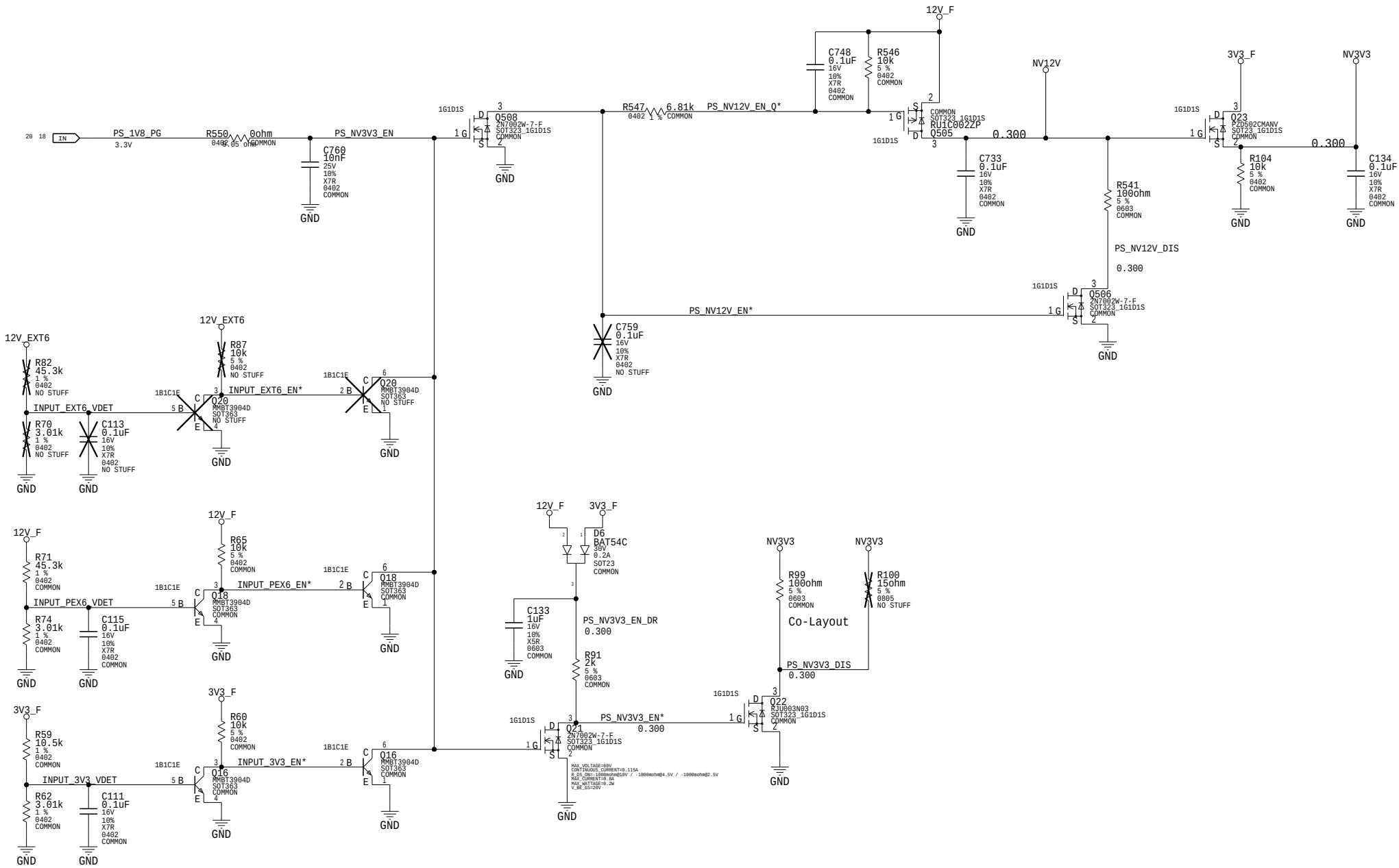
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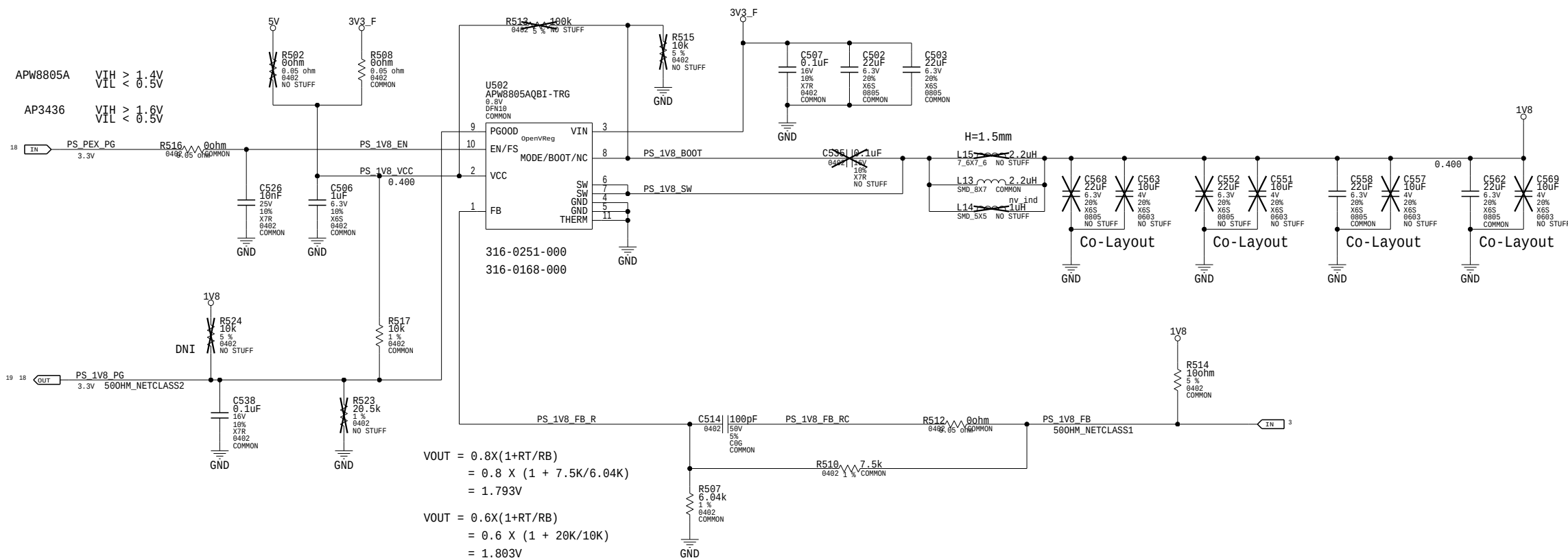
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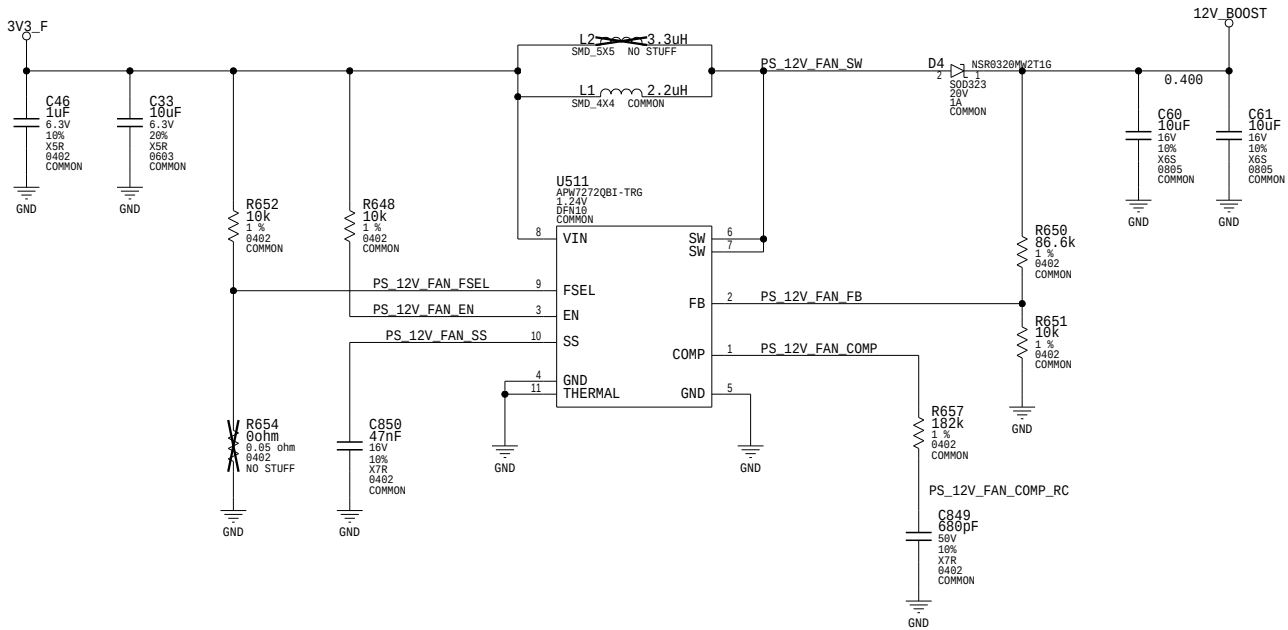
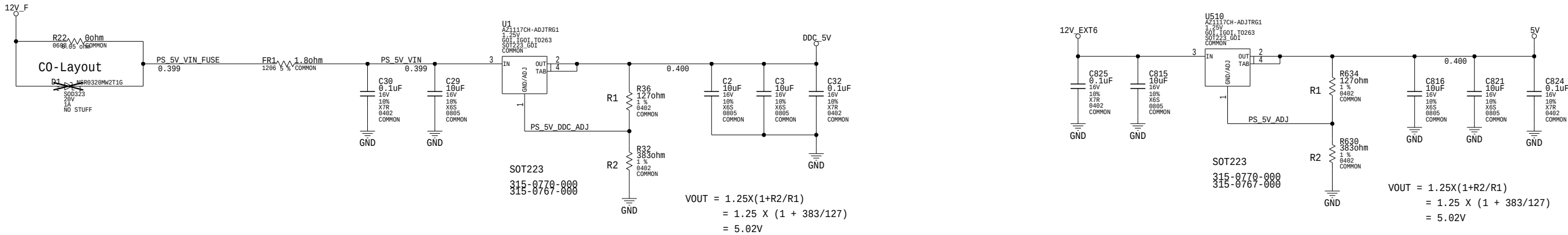
PS: NV3V3 & NV12V



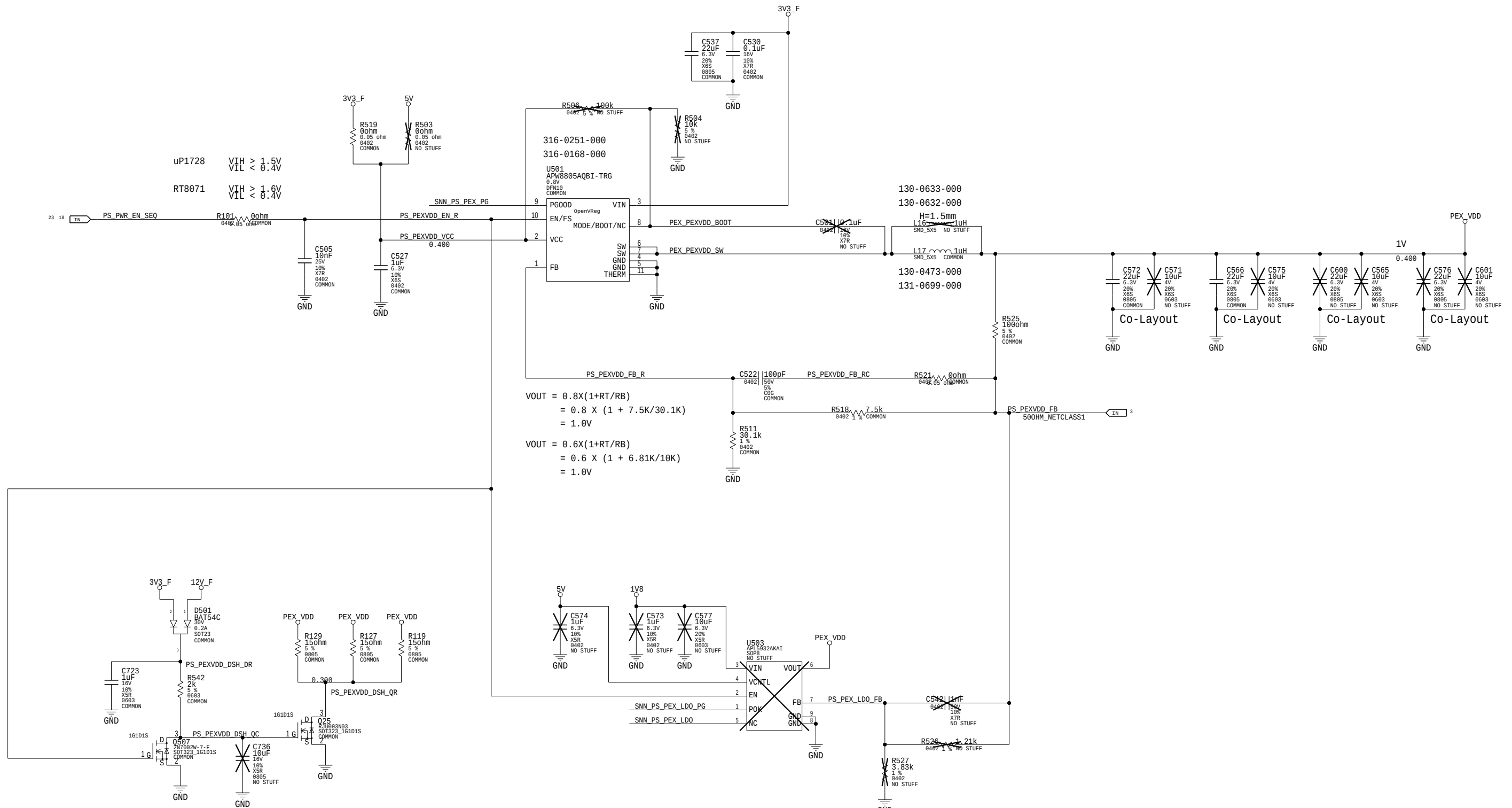
PS I: 1V8



PSII:5V & 12V_FAN



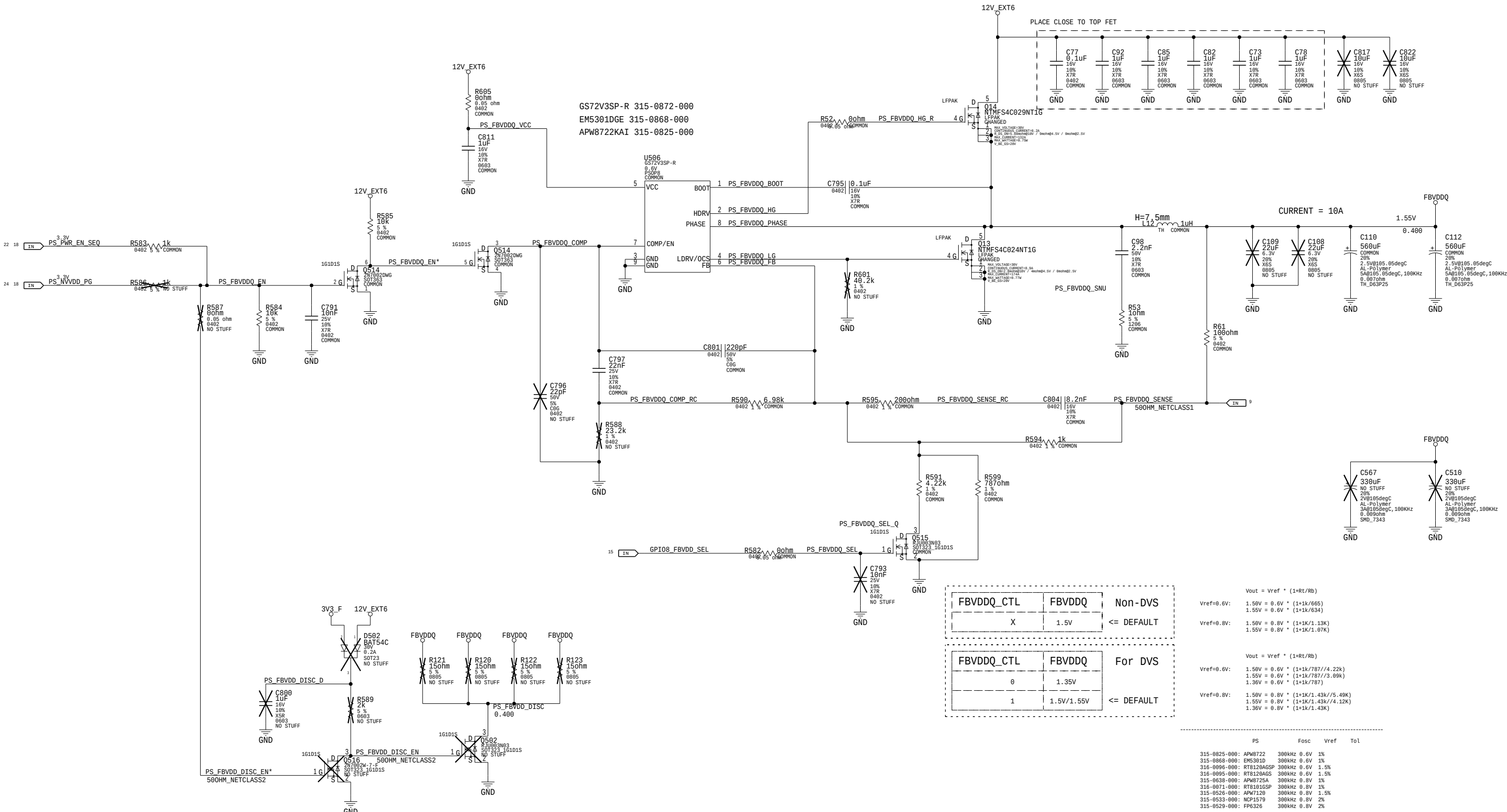
PS III: PEXVDD



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PS IV: FBVDDQ



FBVDDQ_CTL	FBVDDQ	Non-DVS
X	1.5V	<= DEFAULT

FBVDDQ_CTL	FBVDDQ	For DVS
0	1.35V	
1	1.5V/1.55V	<= DEFAULT

$$V_{out} = V_{ref} * (1 + R_T/R_b)$$

$$V_{ref}=0.6V: \begin{aligned} 1.50V &= 0.6V * (1 + 1k/665) \\ 1.55V &= 0.6V * (1 + 1k/634) \end{aligned}$$

$$V_{ref}=0.8V: \begin{aligned} 1.50V &= 0.8V * (1 + 1k/1.13K) \\ 1.55V &= 0.8V * (1 + 1k/1.07K) \end{aligned}$$

$$V_{out} = V_{ref} * (1 + R_T/R_b)$$

$$V_{ref}=0.6V: \begin{aligned} 1.50V &= 0.6V * (1 + 1k/787 // 4.22k) \\ 1.55V &= 0.6V * (1 + 1k/787 // 3.09k) \\ 1.36V &= 0.6V * (1 + 1k/787) \end{aligned}$$

$$V_{ref}=0.8V: \begin{aligned} 1.50V &= 0.8V * (1 + 1k/1.43k // 5.49k) \\ 1.55V &= 0.8V * (1 + 1k/1.43k // 4.12k) \\ 1.36V &= 0.8V * (1 + 1k/1.43k) \end{aligned}$$

PS	Fosc	Vref	Tol
315-0825-000: APM8722	300kHz	0.6V	1%
315-0868-000: EM5301D	300kHz	0.6V	1%
316-0096-000: RT8120AGSP	300kHz	0.6V	1.5%
316-0095-000: RT8120AGS	300kHz	0.6V	1.5%
315-0638-000: APM8725A	300kHz	0.8V	1%
316-0071-000: RT8101GSP	300kHz	0.8V	1%
315-0526-000: APM7120	300kHz	0.8V	1.5%
315-0533-000: NCP1579	300kHz	0.8V	2%
315-0529-000: FPG326	300kHz	0.8V	2%

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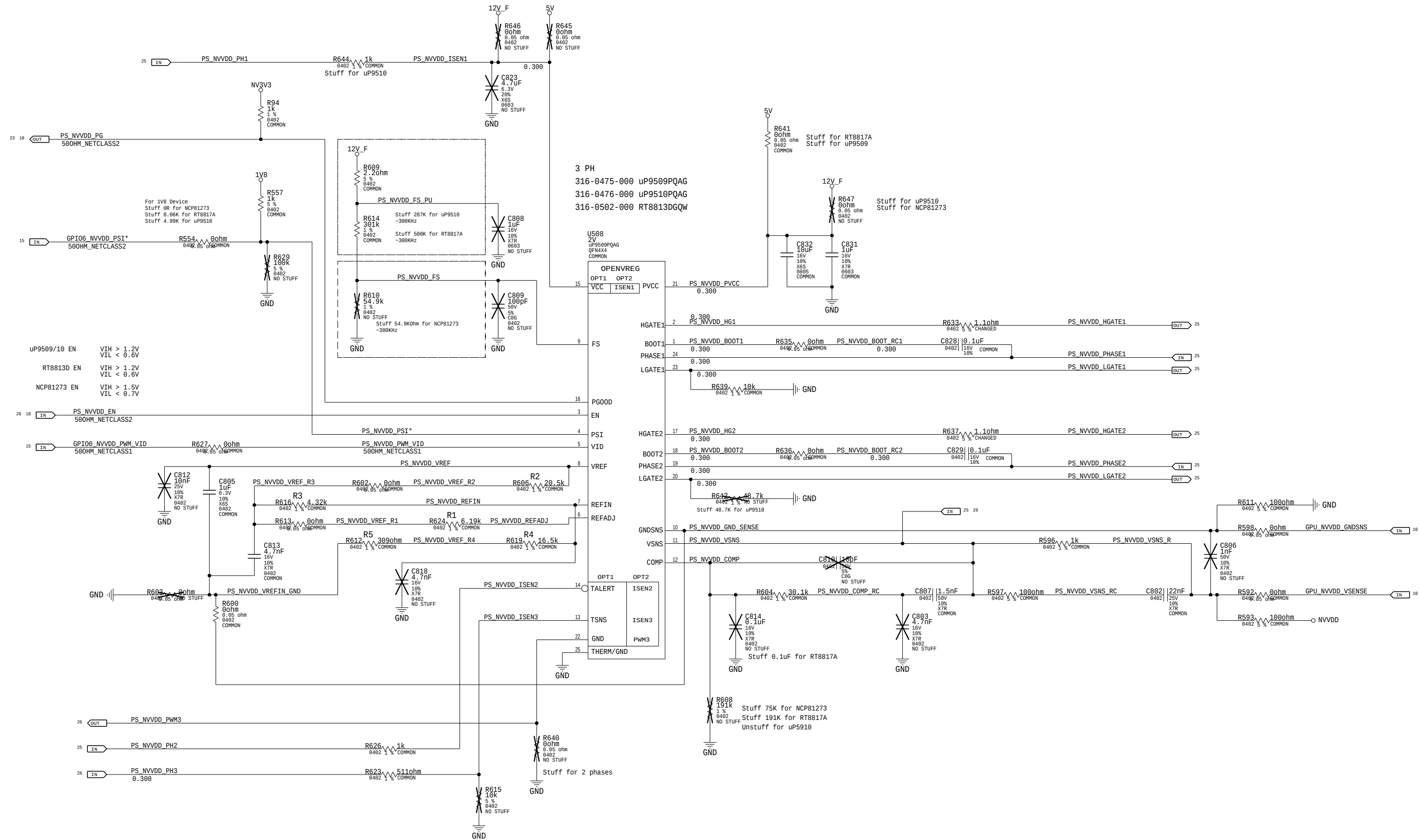


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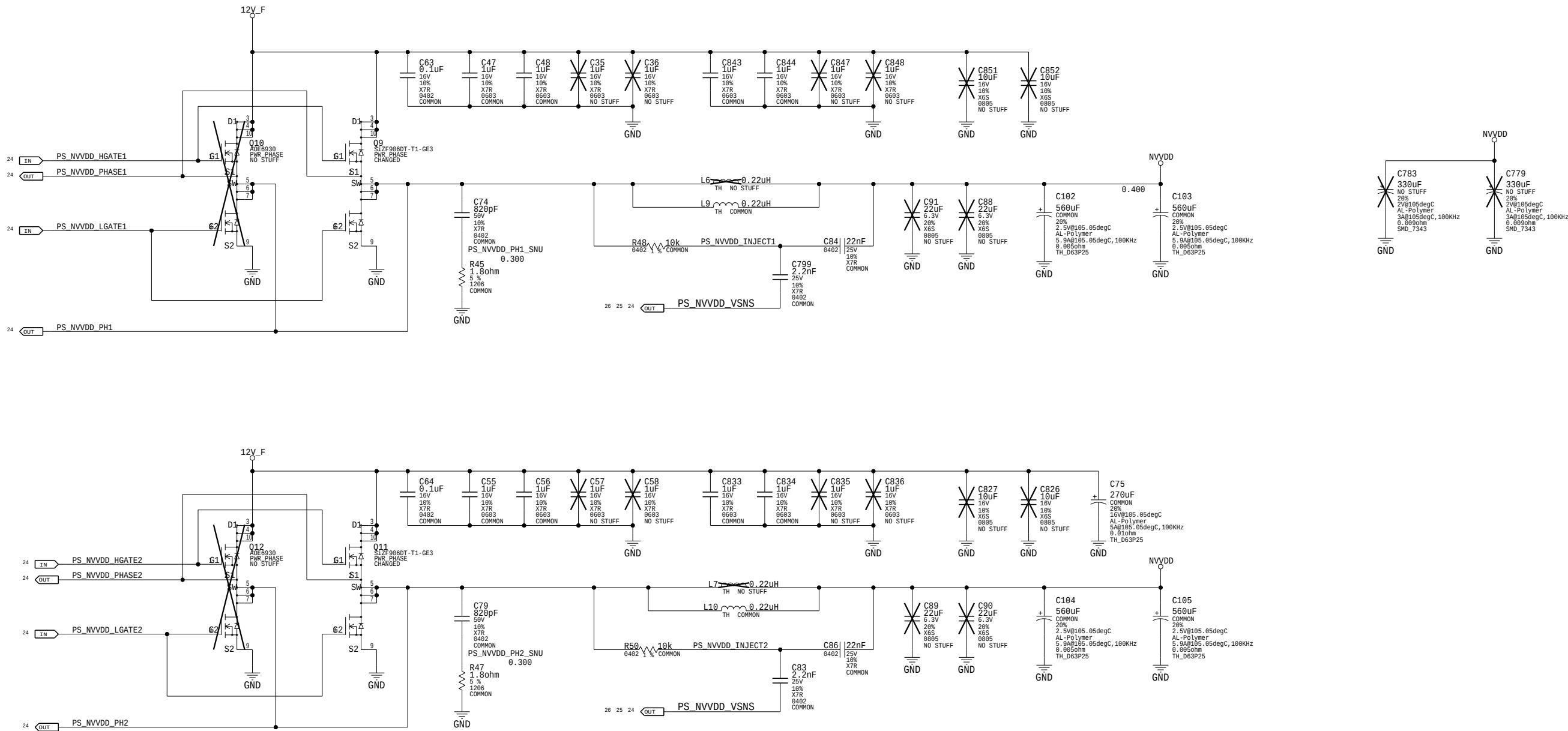
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PS V: NVVDD OVR2+1



PS V: NVVDD Phase 1,2



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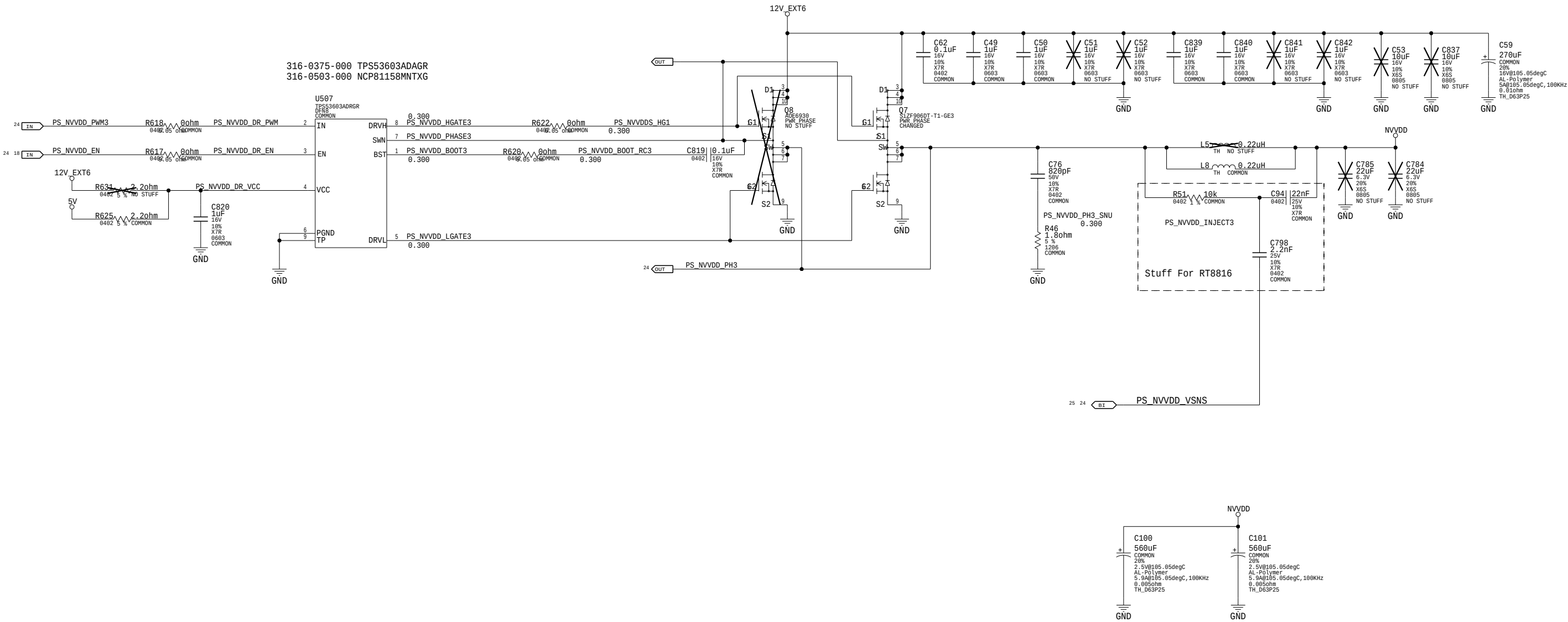
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PS V: NVVDD Phase 3



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Mechanical: Bracket/Thermal Solution

Brackets:

