

PG210 B00

GP107 128b GDDR5, 75W , PCB 5.7"
DVI-D_DL (DP + DP) + HDMI (DP) + DP

TABLE OF CONTENTS

Page	Description
1	Table of Contents
2	Block Diagram
3	PCI Express
4	MEMORY: GPU Partition A/B
5	MEMORY: FBA[31:0]
6	MEMORY: FBA[63:32]
7	MEMORY: FBB[31:0]
8	MEMORY: FBB[63:32]
9	GPU FBVDDQ & 1V8 Decoupling
10	GPU NVVDD & NVVDDS DECOUPLING
11	IFPAB DVI-DL
12	IFPD DP
13	IFPC HDMI
14	IFPEF UNUSED
15	MISC1: Fan, Thermal, JTAG, GPIO
16	MISC2: ROM, XTAL, Straps
17	Power Inputs and Filtering
18	Power Sequence
19	PS: NV3V3 & NV12V
20	PSI: 1V8
21	PSII: 5V & 12V_FAN
22	PS III: PEXVDD
23	PS IV: FBVDDQ
24	PS V: NVVDD OVR2+1
25	PS V: NVVDD Phase 1,2

Page	Description
26	PS V: NVVDD Phase 3
27	MECH: Bracket/Thermal

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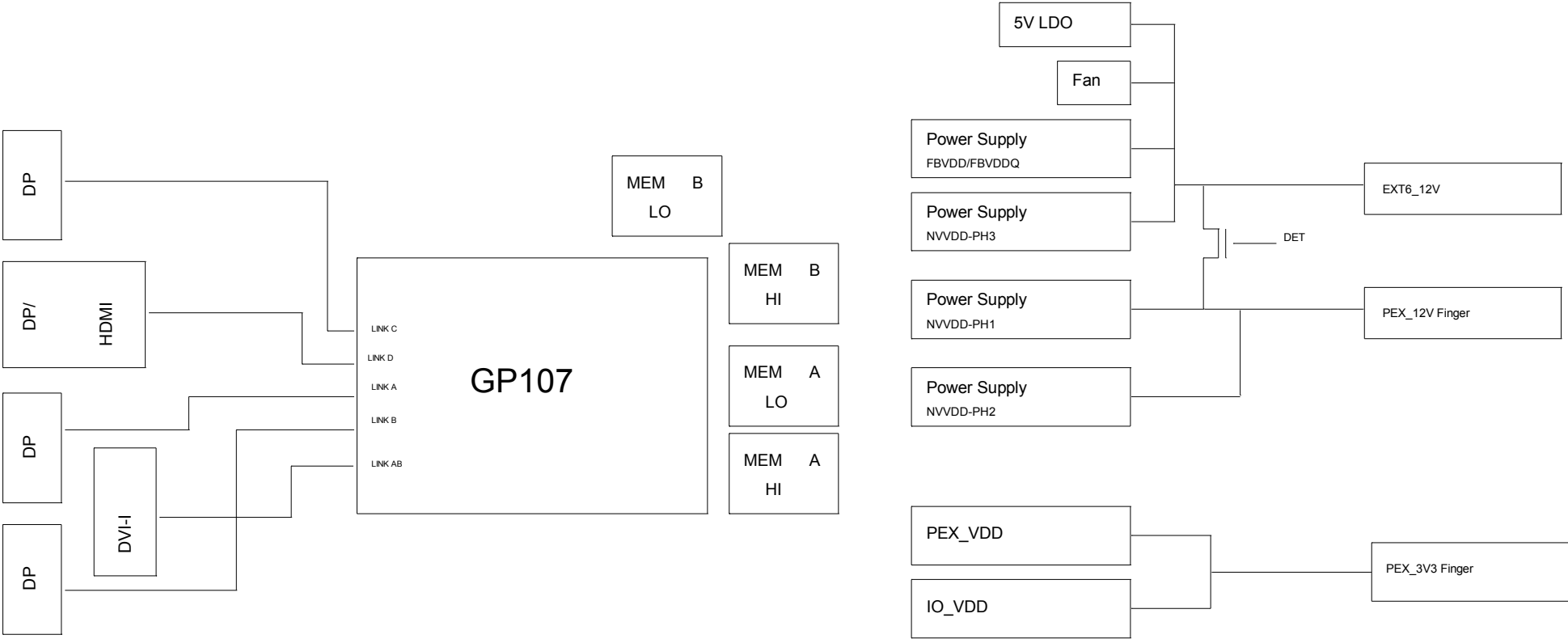
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NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	1 OF 27
BCM REV	A	DATE	05-mon-year

Block Diagram

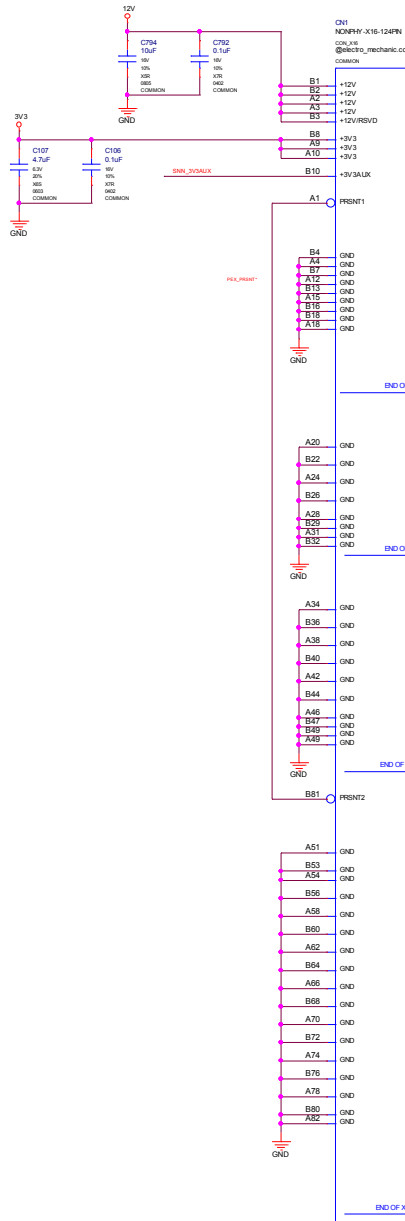


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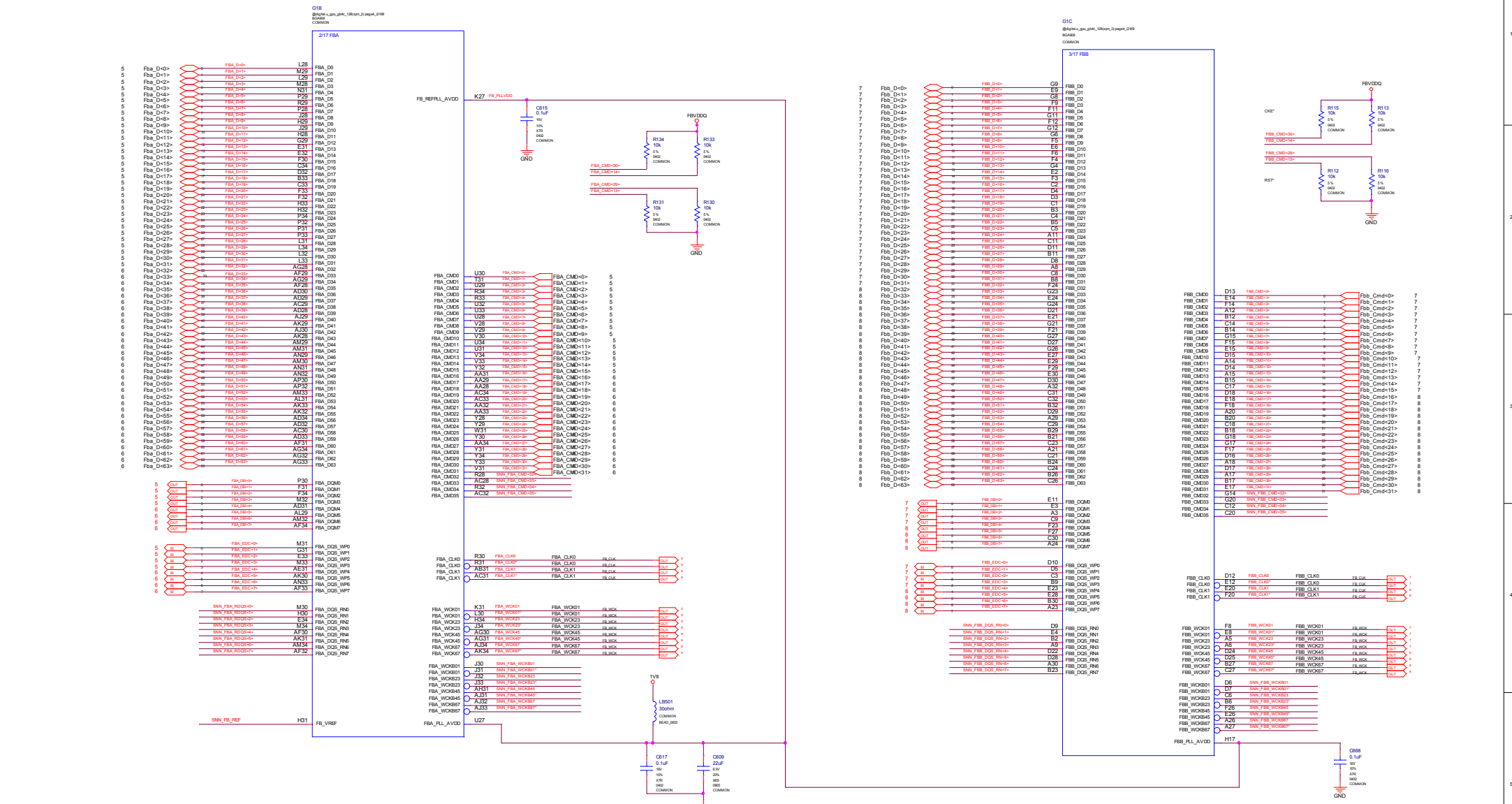
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NV_PN	600-1G210-BASE-SCH		
PCB REV	P0210-B00	PAGE	2 OF 27
BOM REV	A	DATE	18-DEC-2015

PCI Express



MEMORY: GPU Partition A/B



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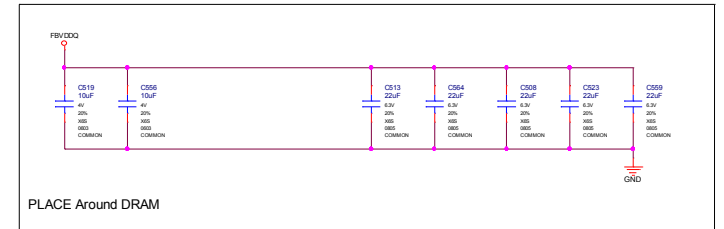
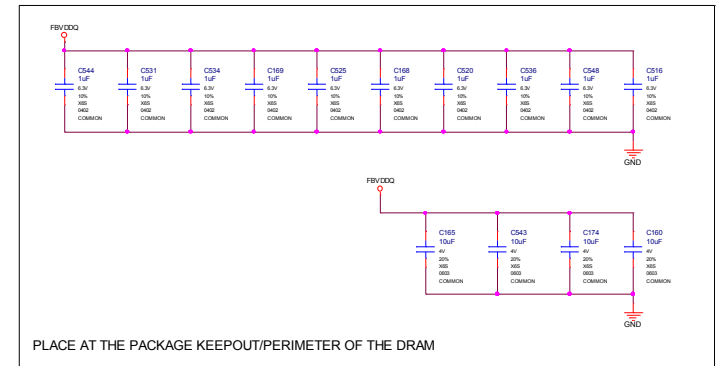
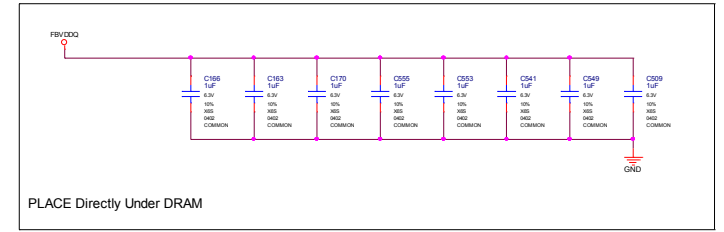
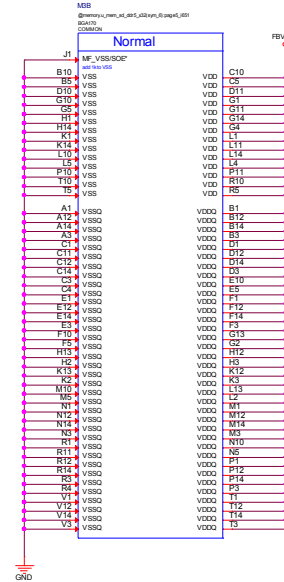
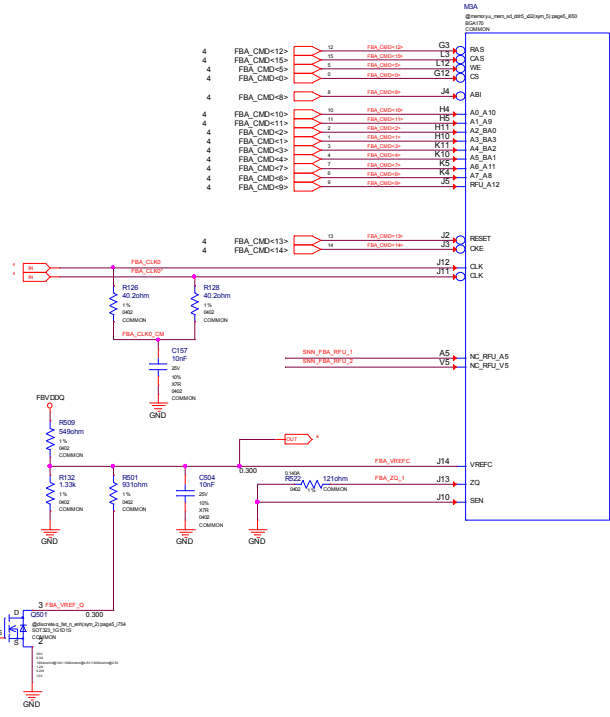
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PN	600-1G210-BASE-SCH
ICB REV	PC0210-000
ROM REV	A
PAGE	4 OF 27
DATE	18-DEC-2015

MEMORY: FBA Partition 31..0

CMD	0..31	32..63
CM00	CS*	
CM01	A3, BA3	
CM02	A2, BA2	
CM03	A4, BA2	
CM04	A2, BA1	
CM05	WE*	
CM06	A7, A8	
CM07	A6, A11	
CM08	AR*	
CM09	A12, RFU	
CM10	A0, A10	
CM11	A1, A9	
CM12	RA5*	
CM13	RS*	
CM14	CK*	
CM15	CAS*	
CM16		CS*
CM17		A3, BA3
CM18		A2, BA2
CM19		A4, BA2
CM20		A2, BA1
CM21		WE*
CM22		A7, A8
CM23		A6, A11
CM24		AR*
CM25		A12, RFU
CM26		A0, A10
CM27		A1, A9
CM28		RA5*
CM29		RS*
CM30		CK*
CM31		CAS*



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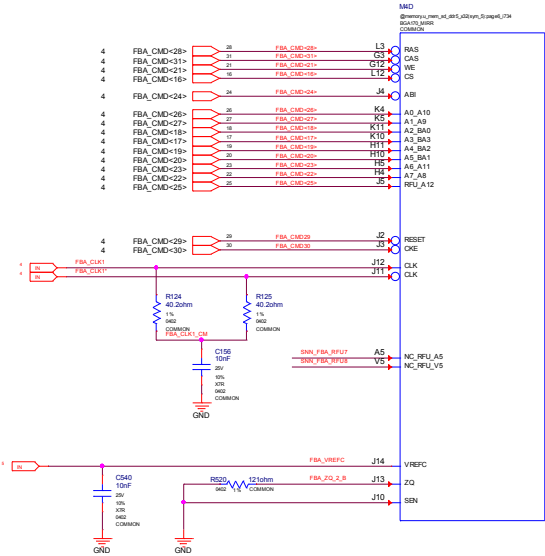
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PCB REV	PS210-800	PAGE	5 OF 27
ROM REV	A	DATE	18-DEC-2015

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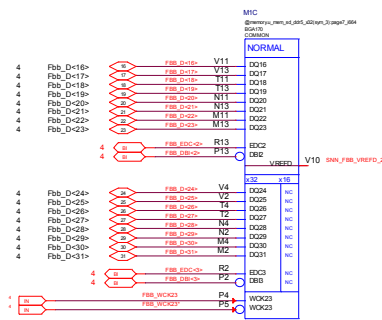
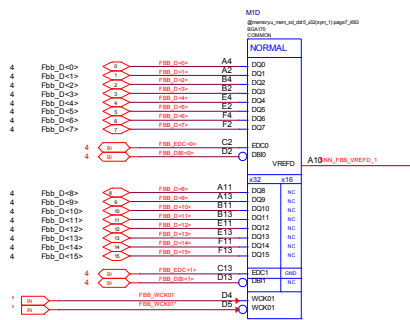
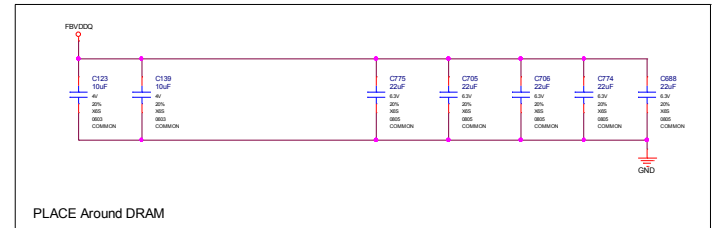
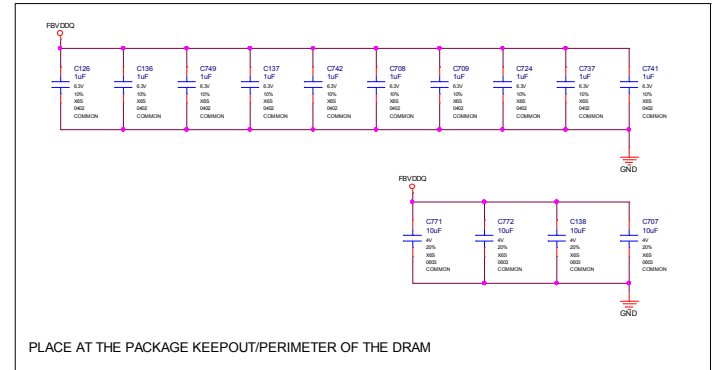
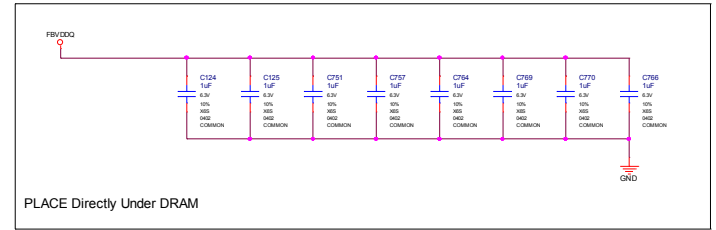
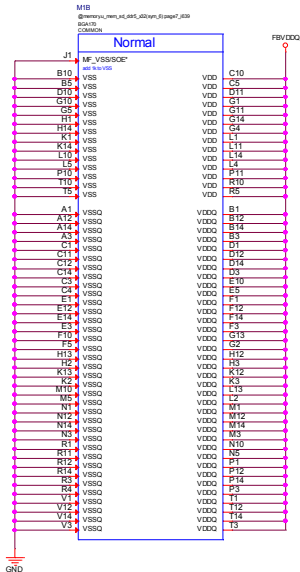
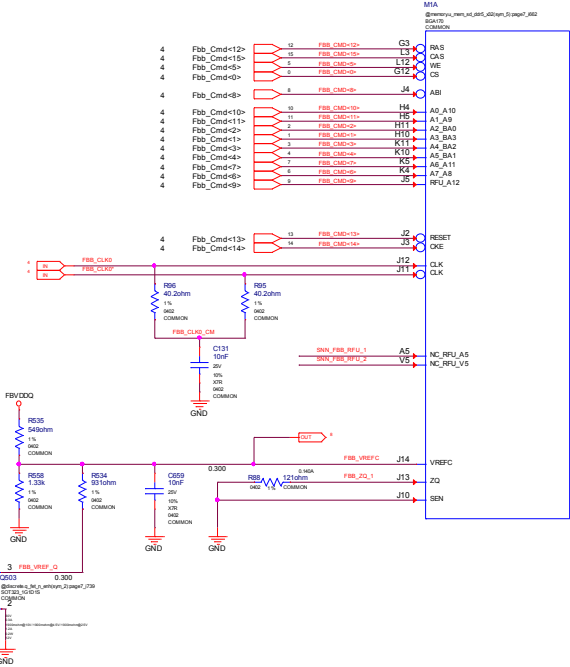
MEMORY: FBA Partition 63..32

CMD	0..31	32..63
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CM01	A3_BA3	
CM02	A2_BA0	
CM03	A4_BA2	
CM04	A5_BA1	
CM05	WE*	
CM06	A7_A8	
CM07	AE_A11	
CM08	AB*	
CM09	A12_RFU	
CM10	A0_A10	
CM11	A1_A9	
CM12	RA*	
CM13	RS*	
CM14	OE*	
CM15	CA*	
CM16		CS*
CM17		A3_BA3
CM18		A2_BA0
CM19		A4_BA2
CM20		A5_BA1
CM21		WE
CM22		A7_A8
CM23		AE_A11
CM24		AB*
CM25		A12_RFU
CM26		A0_A10
CM27		A1_A9
CM28		RA*
CM29		RS*
CM30		OE*
CM31		CA*



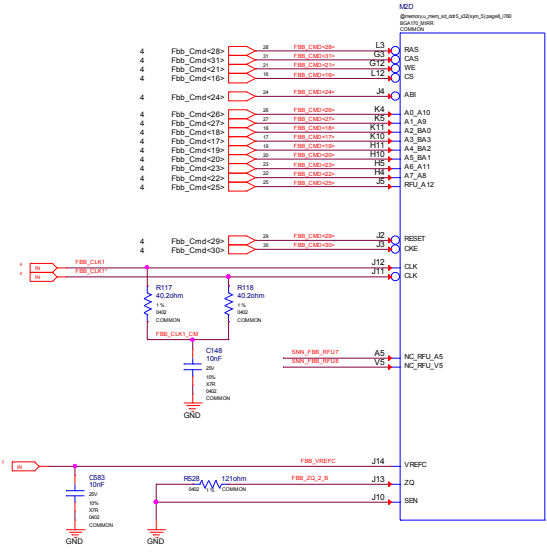
MEMORY: FBB Partition 31..0

CMD	0..31	32..63
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CM01	A3_BA3	
CM02	A2_BA2	
CM03	A4_BA2	
CM04	A5_BA1	
CM05	WE*	
CM06	A7_A8	
CM07	A6_A11	
CM08	AB*	
CM09	A12_RFU	
CM10	A0_A10	
CM11	A1_A9	
CM12	RA5*	
CM13	RS*	
CM14	OE*	
CM15	CAS*	
CM16		CS*
CM17		A3_BA3
CM18		A2_BA2
CM19		A4_BA2
CM20		A5_BA1
CM21		WE*
CM22		A7_A8
CM23		A6_A11
CM24		AB*
CM25		A12_RFU
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CM28		RA5*
CM29		RS*
CM30		OE*
CM31		CAS*

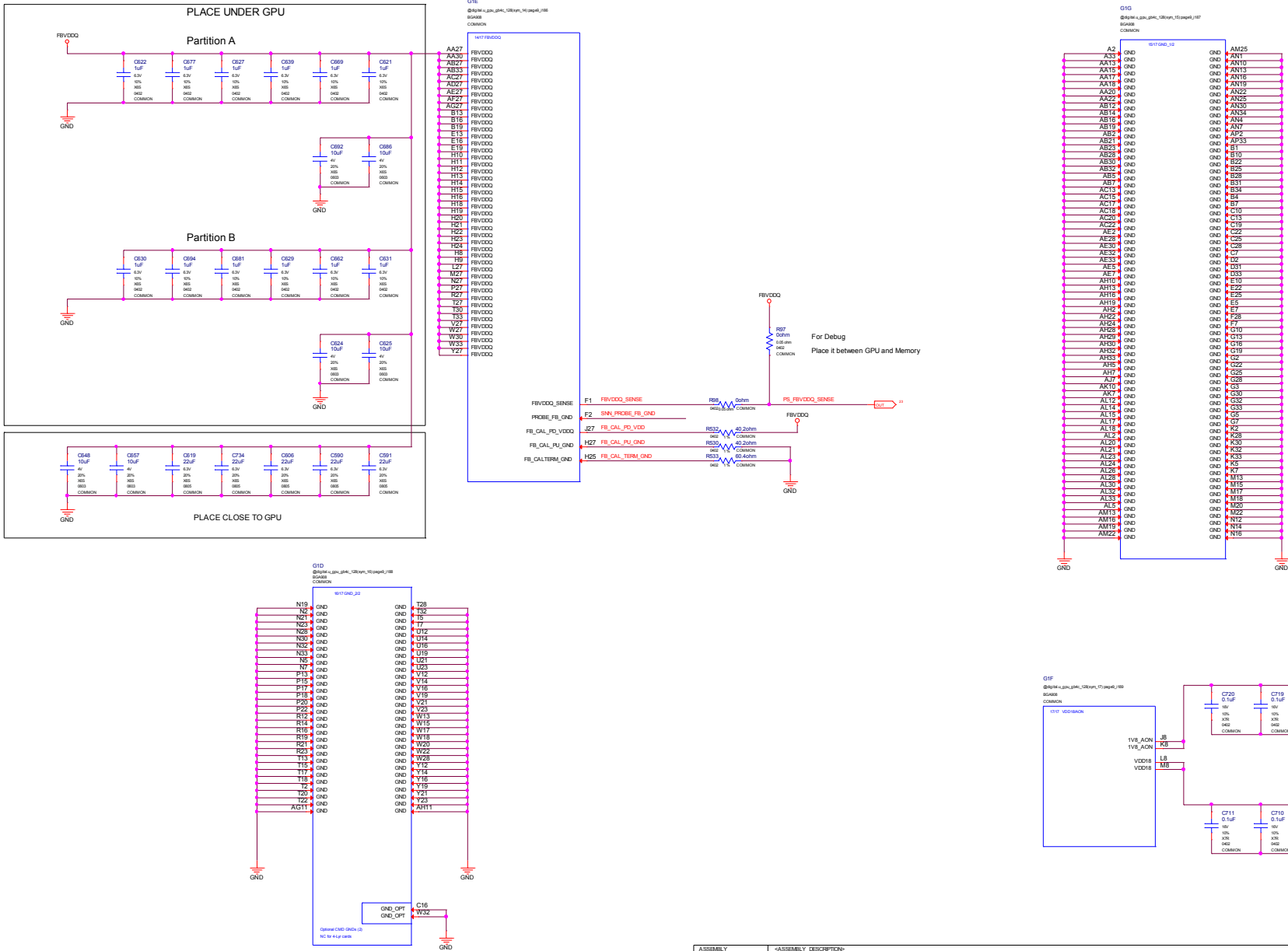


MEMORY: FBB Partition 63..32

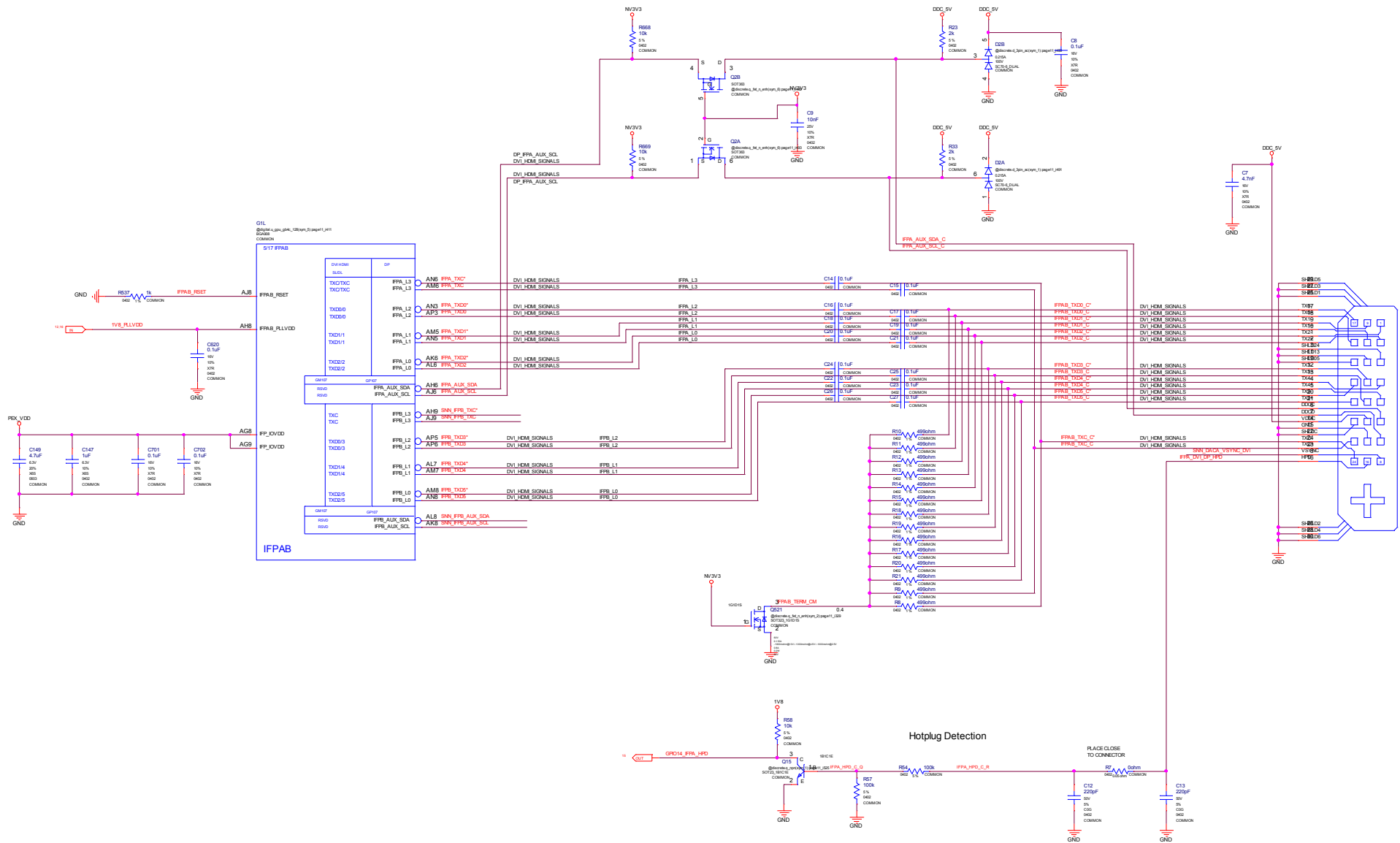
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CM01	A3_BA3	
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CM03	A4_BA2	
CM04	A3_BA1	
CM05	WE*	
CM06	A7_A8	
CM07	AL0_A11	
CM08	AS*	
CM09	A12_RFU	
CM010	A5_A10	
CM011	A7_A8	
CM012	RA5*	
CM013	RS1*	
CM014	QK*	
CM015	CAS*	
CM016		
CM017		
CM018	CS*	
CM019	A3_BA3	
CM020	A2_BA0	
CM021	A4_BA2	
CM022	WE*	
CM023	A7_A8	
CM024	AL0_A11	
CM025	AS*	
CM026	A12_RFU	
CM027	A5_A10	
CM028	A7_A8	
CM029	RA5*	
CM030	RS1*	
CM031	QK*	
CM032	CAS*	



GPU FBVDDQ & 1V8 Decoupling



IFPAB DVI-DL



17ci203

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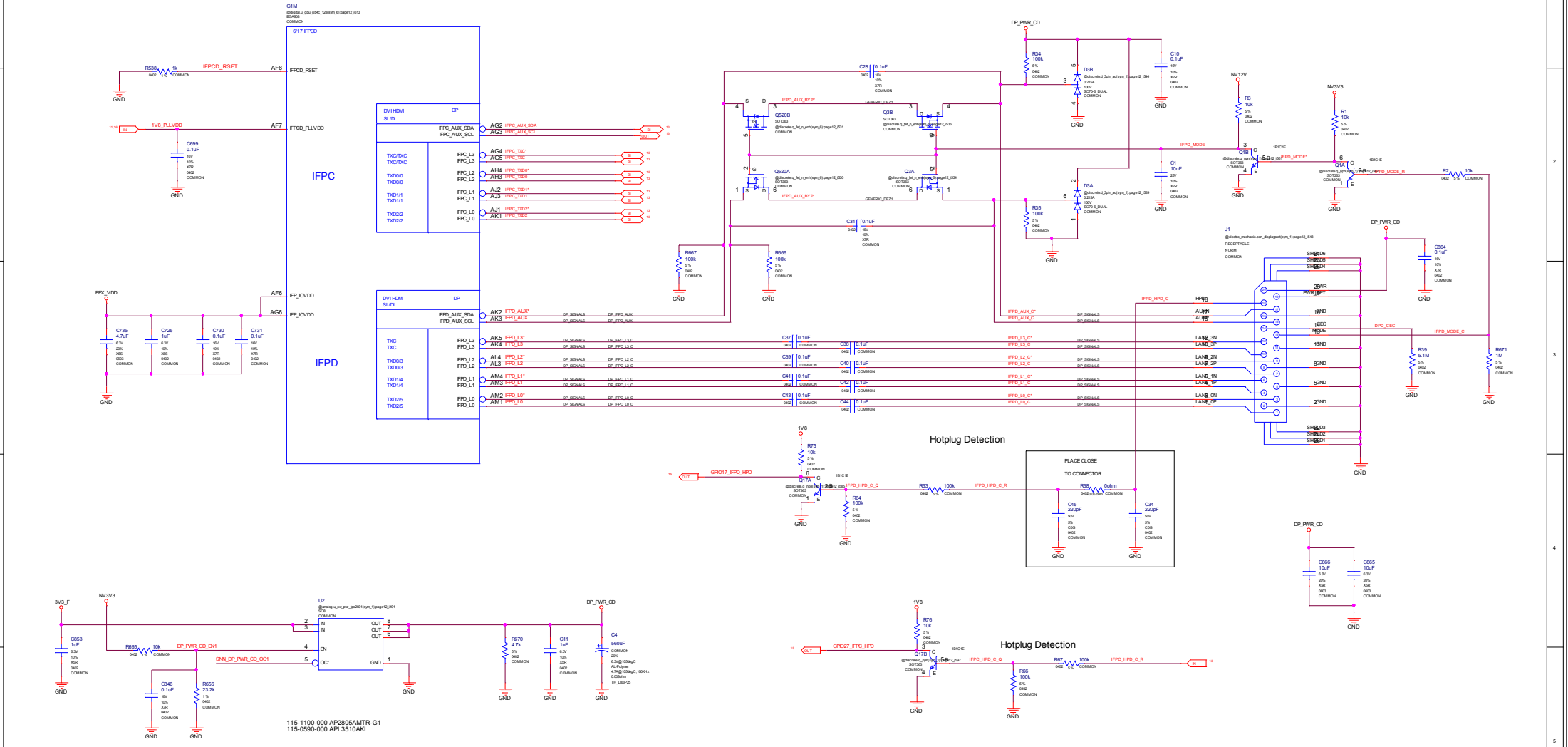
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				FCB REV		PG210-B00	
				BOM REV		A	
				DATE		18-DEC-2015	
				PAGE		11 OF 27	

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IFPD DP



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P0210-8000

ICOM REV

A

PAGE

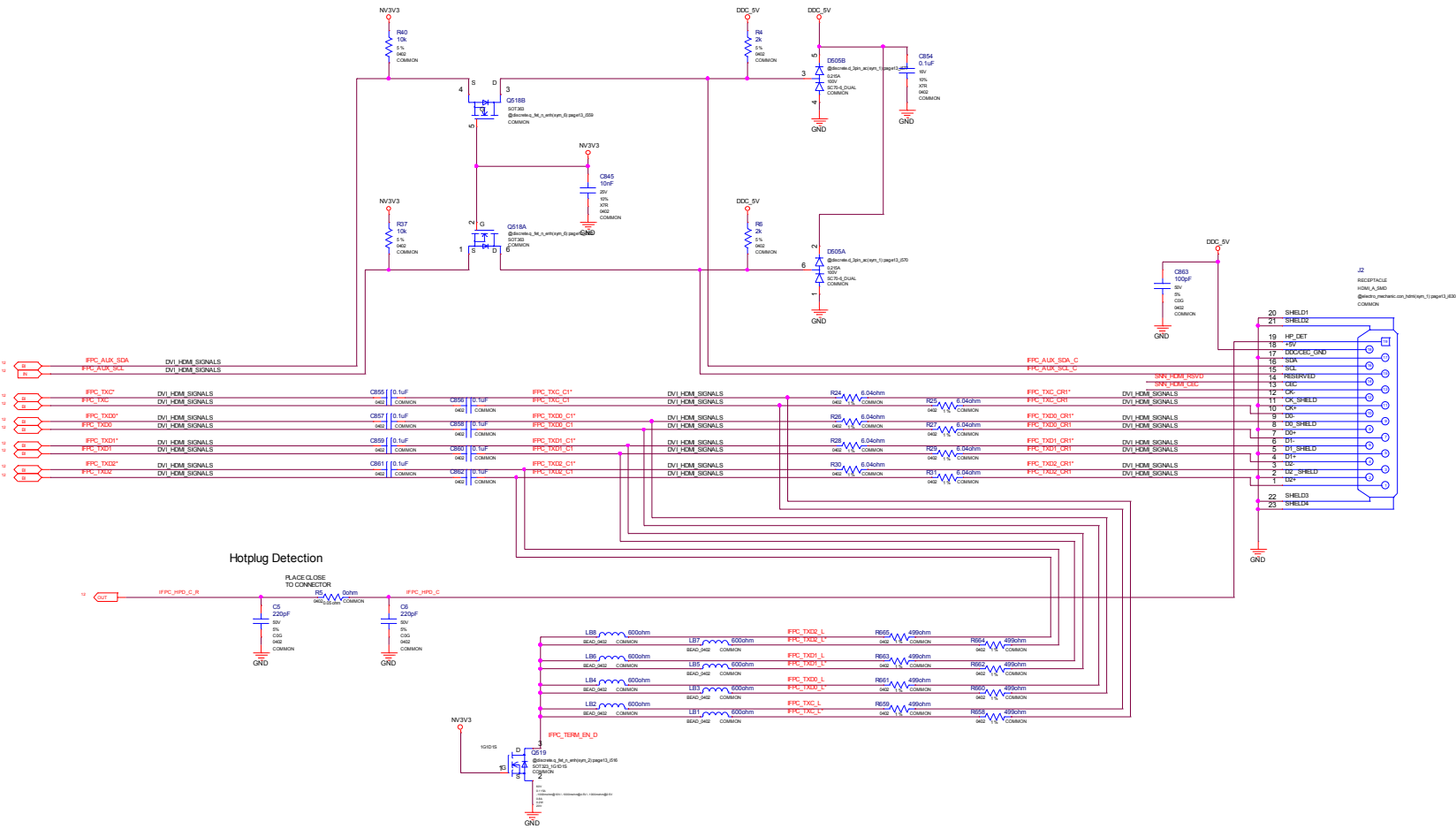
12 OF 27

DATE

18-DEC-2015



IFPC HDMI

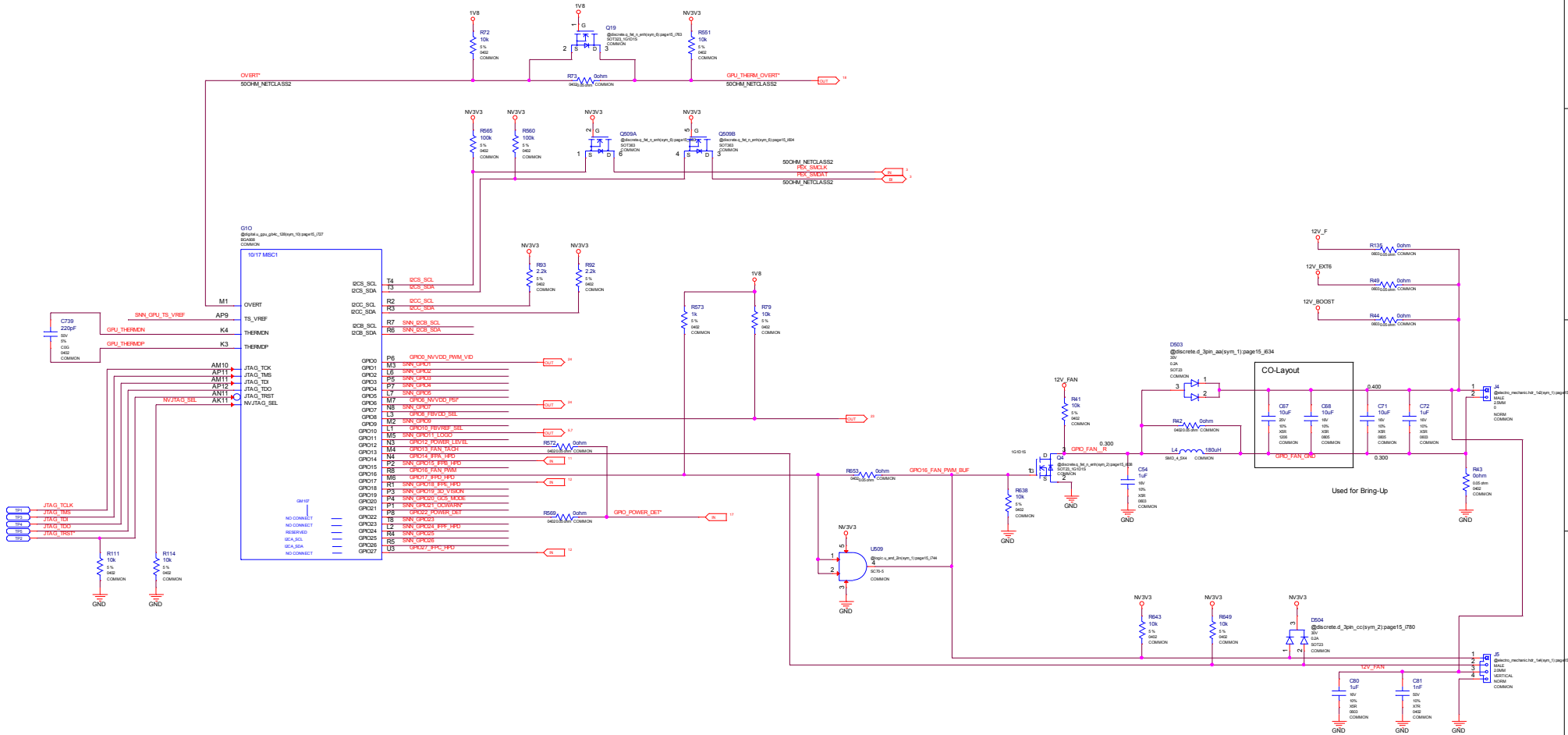




PCB REV	PG210-B00	PAGE	14 OF 2
BOM REV	A	DATE	18-DEC-2015

MISC1: GPIO, Fan, Thermal, JTAG

PADS FOR DEBUGGING

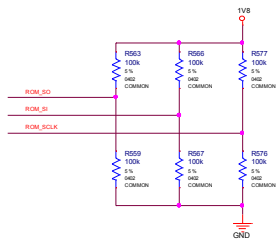


MISC2: ROM, XTAL, Straps

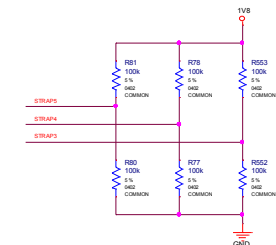
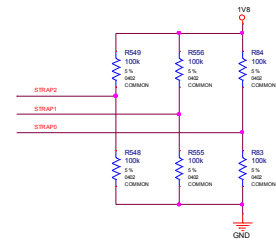
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L	L	L	1111	Default
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	Samsung B-Die 8Gb 256Mx32
L	L	H	0001	Micron F-Die 8Gb 256Mx32
L	H	L	0010	Hynix M-Die 8Gb 256Mx32
L	H	H	0011	
H	H	L	0110	Hynix A-Die 4Gb 128Mx32
H	H	H	0111	Samsung E-Die 4Gb 128Mx32
L	L	M	1000	Micron B-Die 4Gb 128Mx32
L	M	L	1001	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0



H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

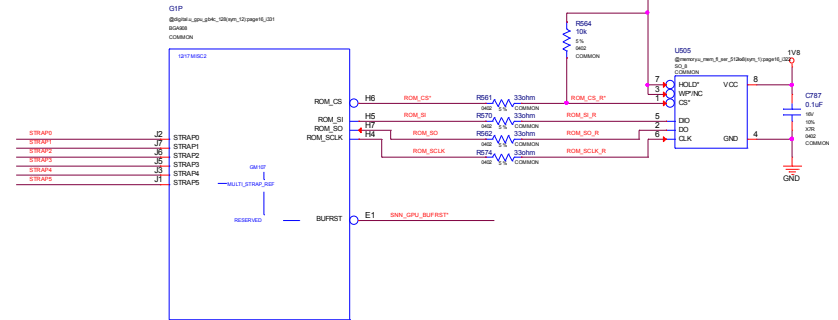


```
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

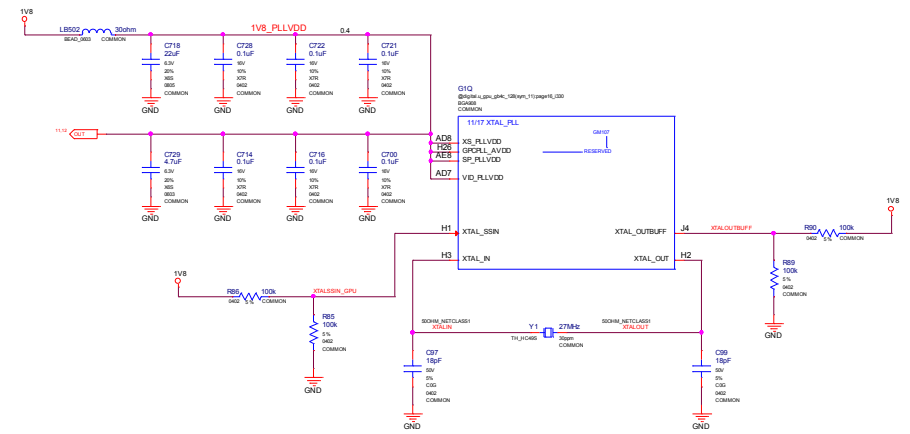
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE
```



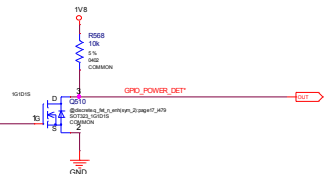
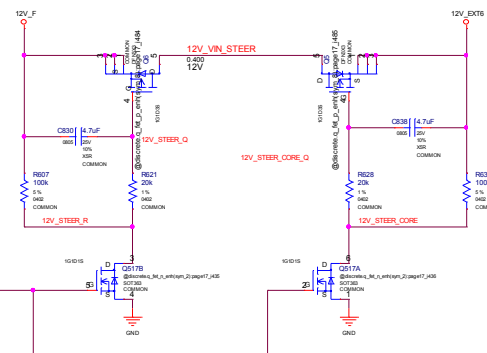
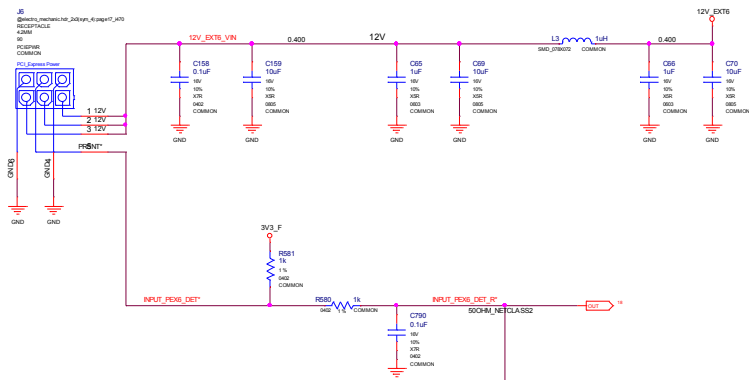
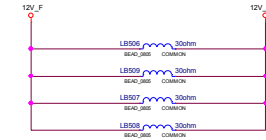
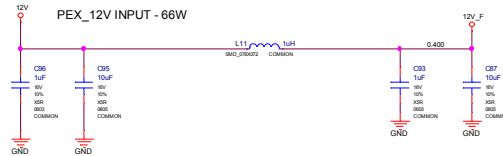
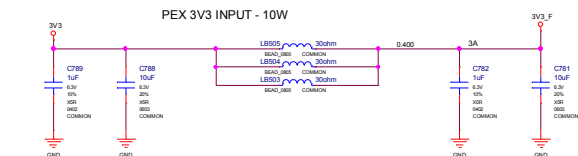
Smart Fan

XTALOUTBUFF	Voltage	SmartFan PWM	GPIO/PWM at the FAN
Low	0V	GPIO Disabled	100%
Middle	0.9V	66% PWM	33% PWM (Typical)
High	1.8V	33% PWM	66% PWM



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NV_PN		600-1G210-BASE-SCH		
PCB REV	PC210-B000	PAGE	16 OF 27	
BOM REV	A	DATE	18-DEC-2015	

Power Inputs and Filtering



ASSEMBLY	<ASSEMBLY_DESCRIPTION
PAGE DETAIL	Power Inputs and Filtering

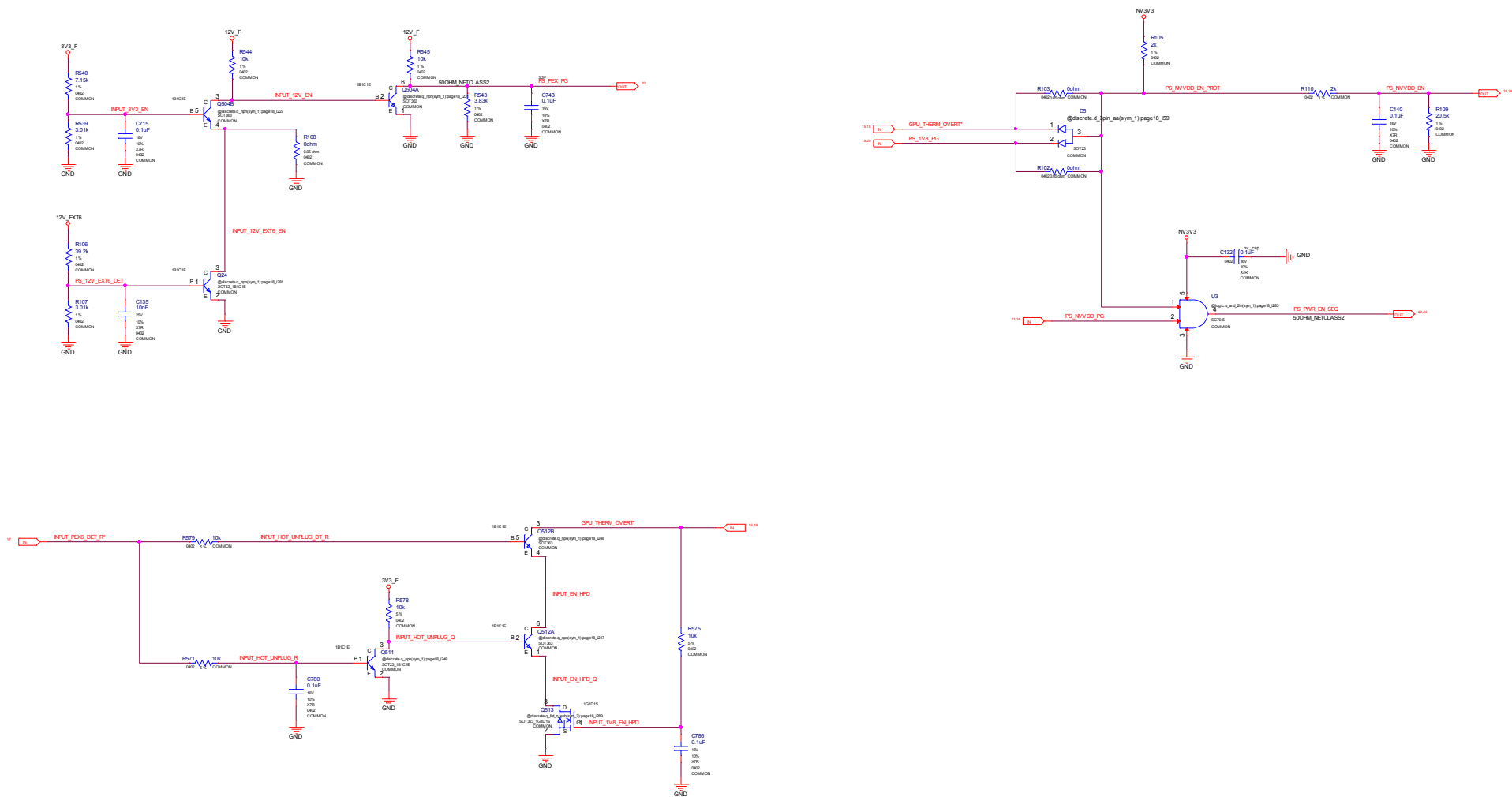
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NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	17 OF 27
BOM REV	A	DATE	18-DEC-2015

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Power sequence



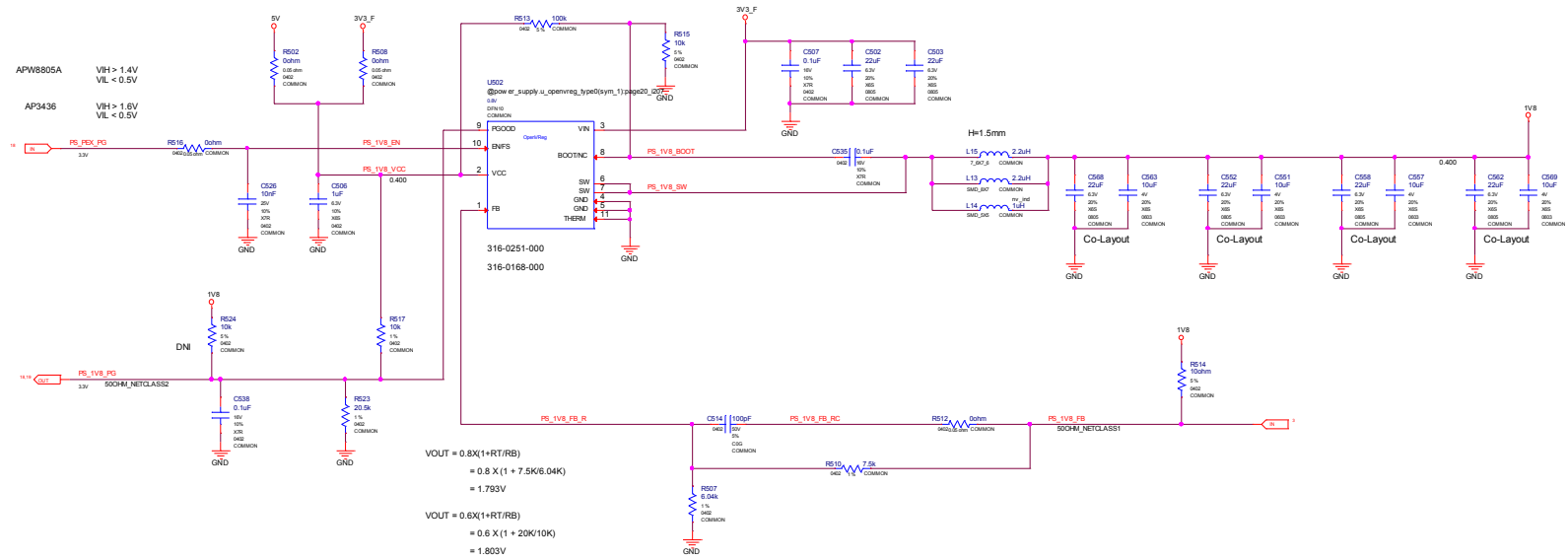
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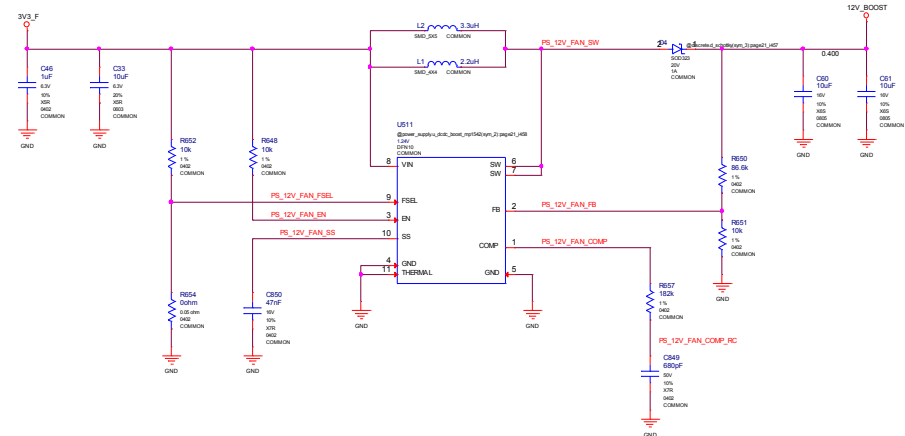
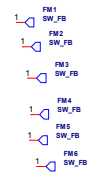
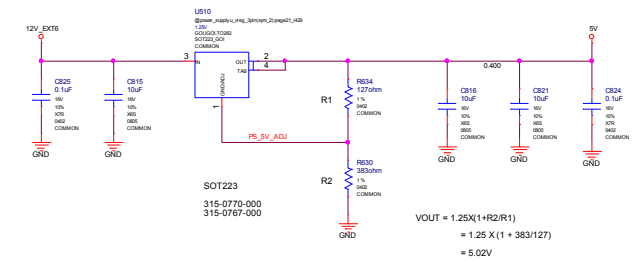
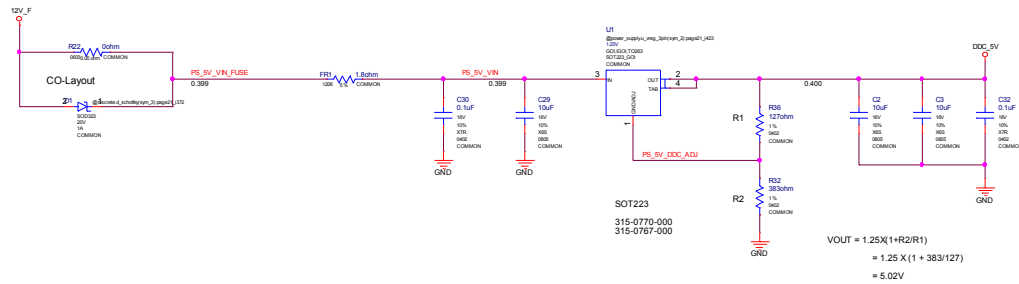


NV_PN	600-1G210-BASE-SCH		
PCB REV	P6210-B00	PAGE	18 OF 2
BOM REV	A	DATE	18-DEC-2015

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PSII:5V & 12V_FAN



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PAGE DETAIL	PS1: 5V & 12V_FAN

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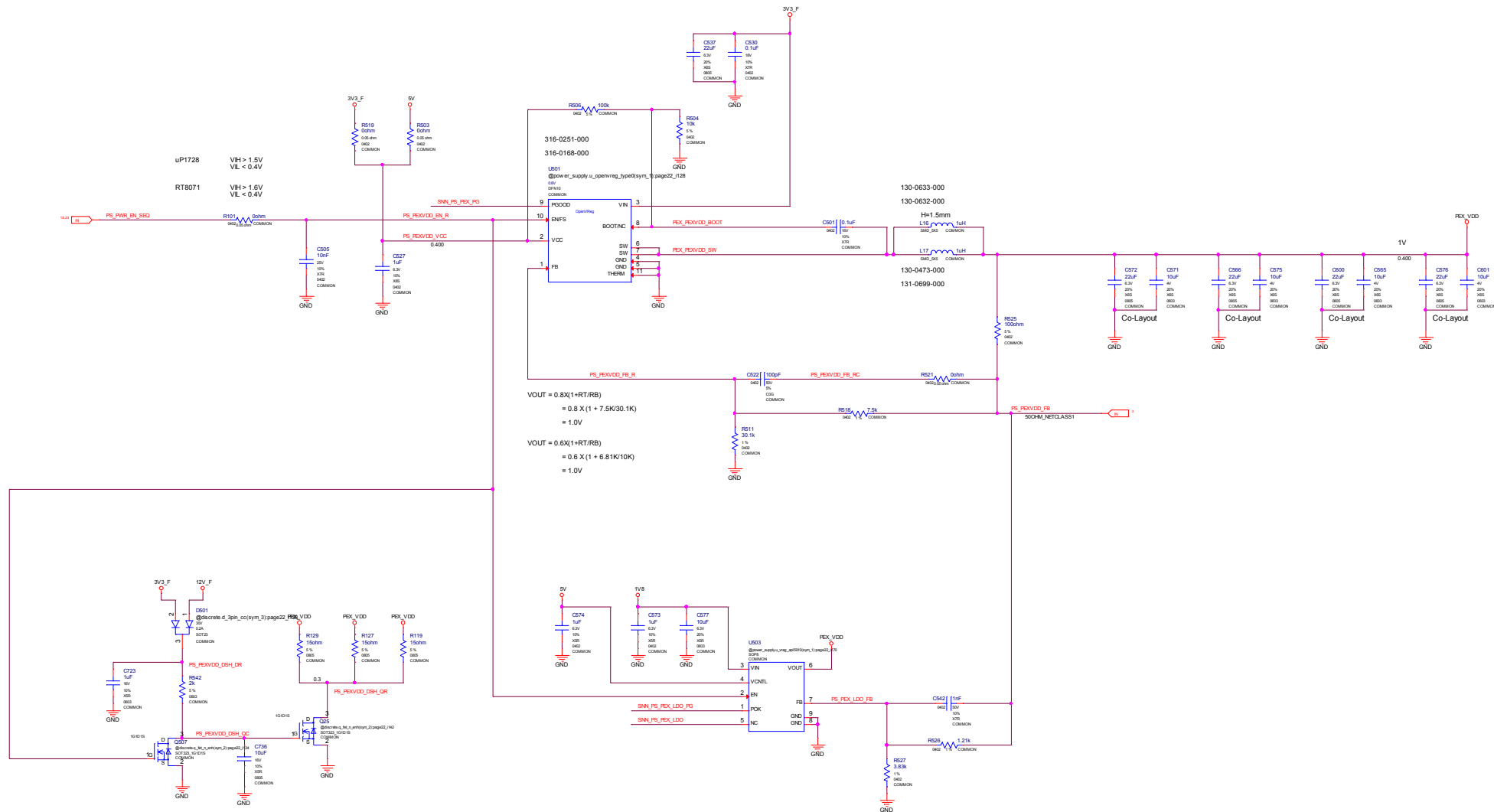
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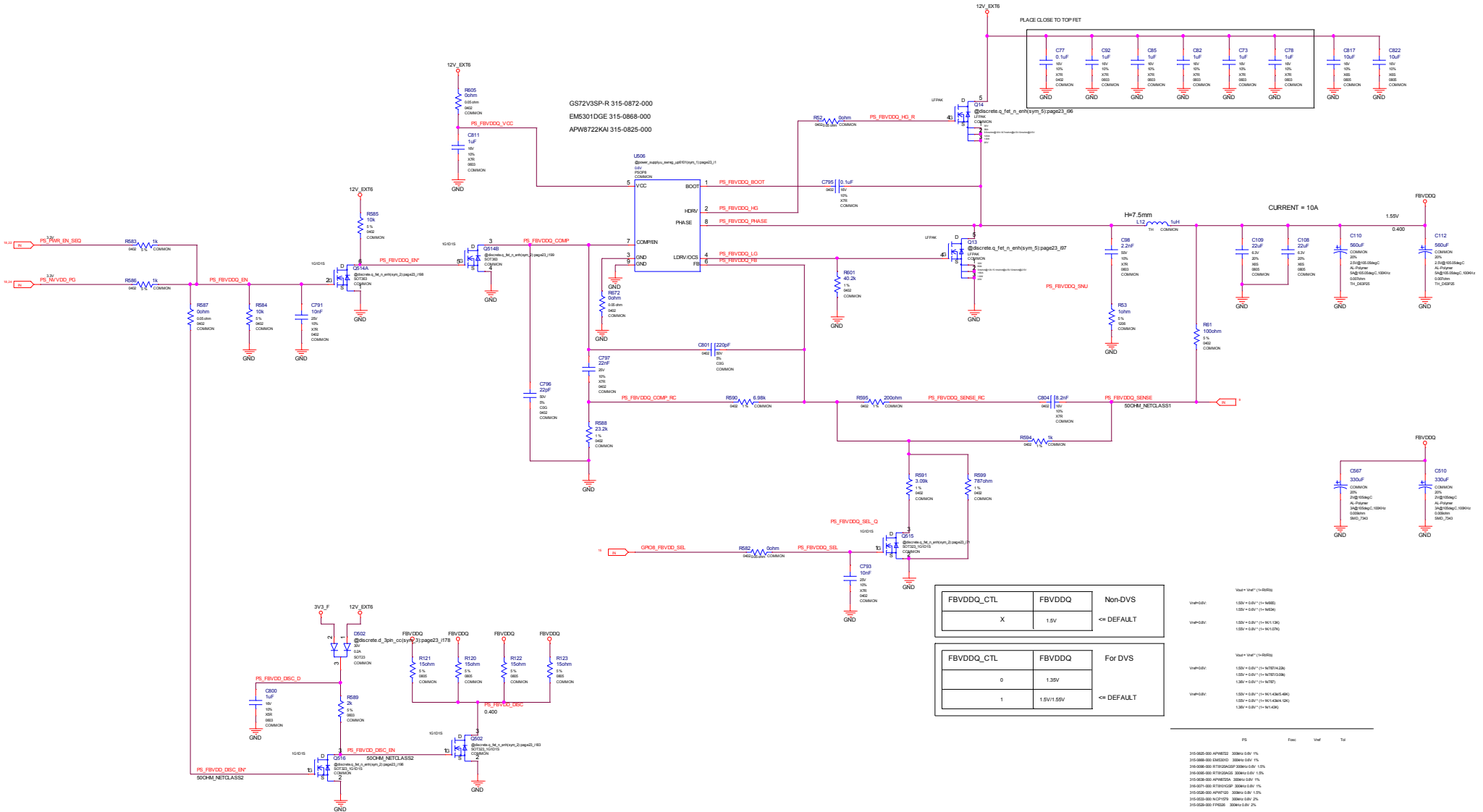
NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	21 OF 27
BCM REV	A	DATE	18-DEC-2015

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PS III: PEXVDD



PS IV: FBVDDQ

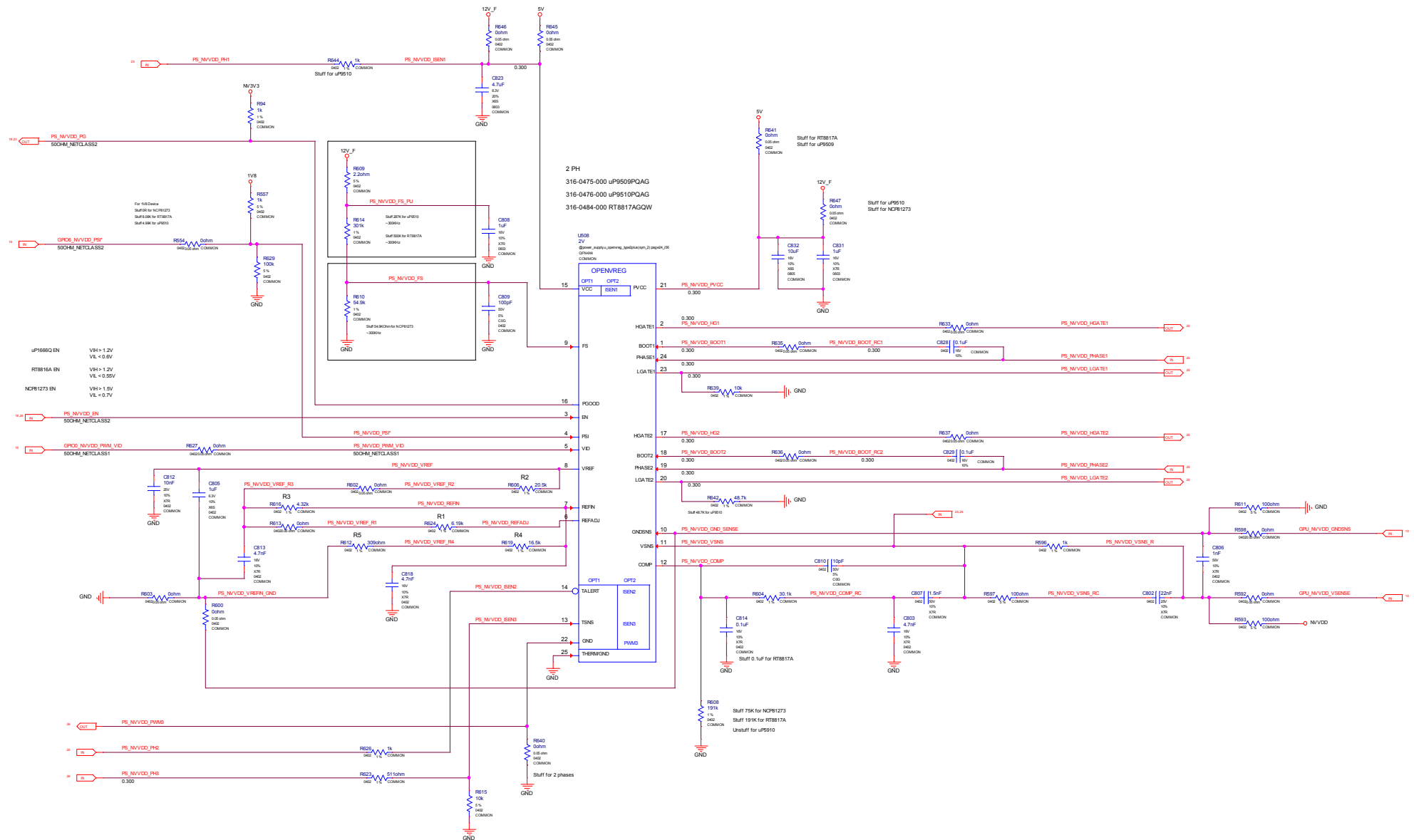


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ASSEMBLY	ASSEMBLY DESCRIPTION
PS IV: FBVDDQ	

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NV_PN	600-1G210-BASE-SCH
PCB REV	PC210-8000
ROM REV	A
PAGE	23 OF 27
DATE	18-DEC-2015

PS V: NVVDD OVR2+1



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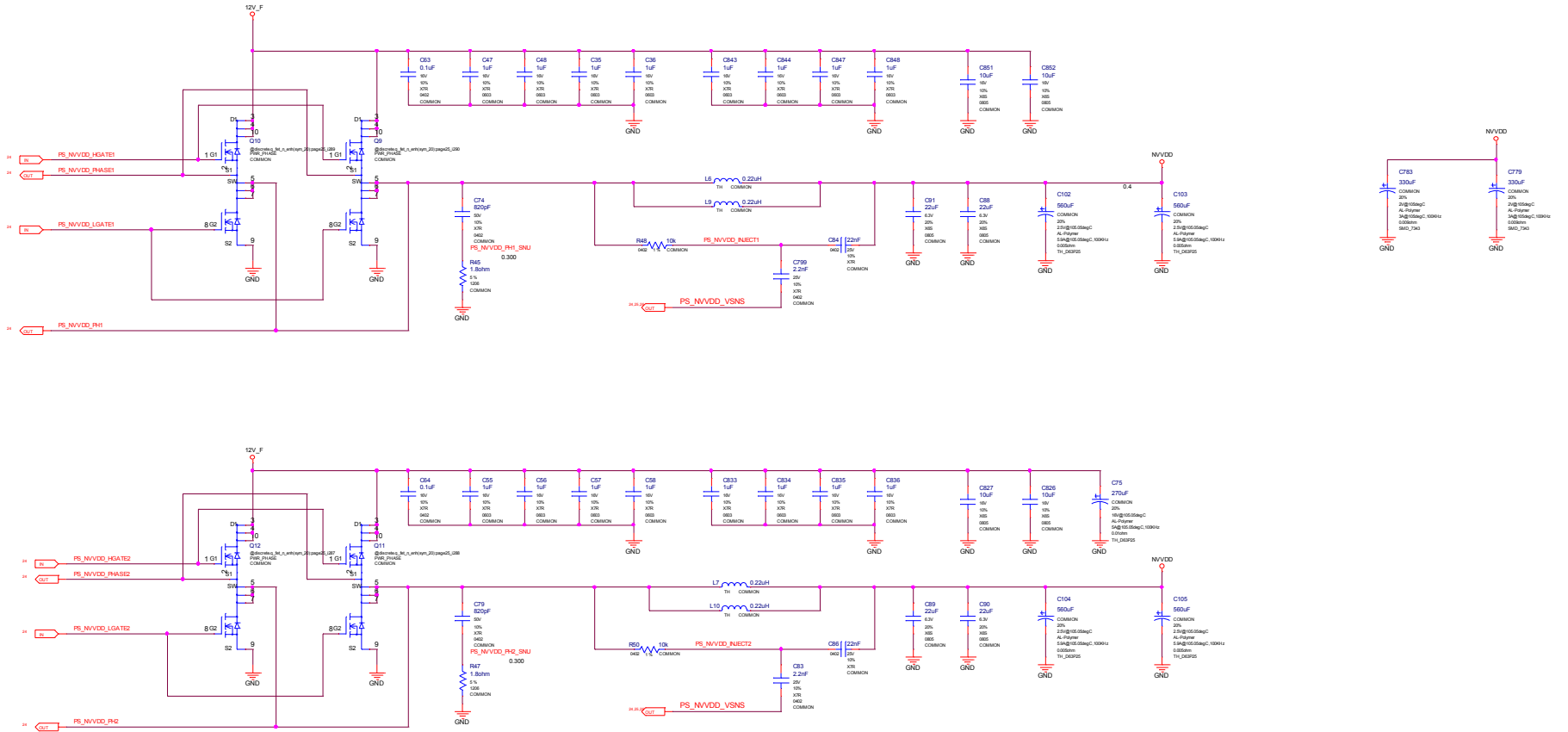


NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-B00	PAGE	24 OF 27
BOM REV	A	DATE	18-DEC-2015

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS V: NVDD OVR2+1

PS V: NVVDD Phase 1,2

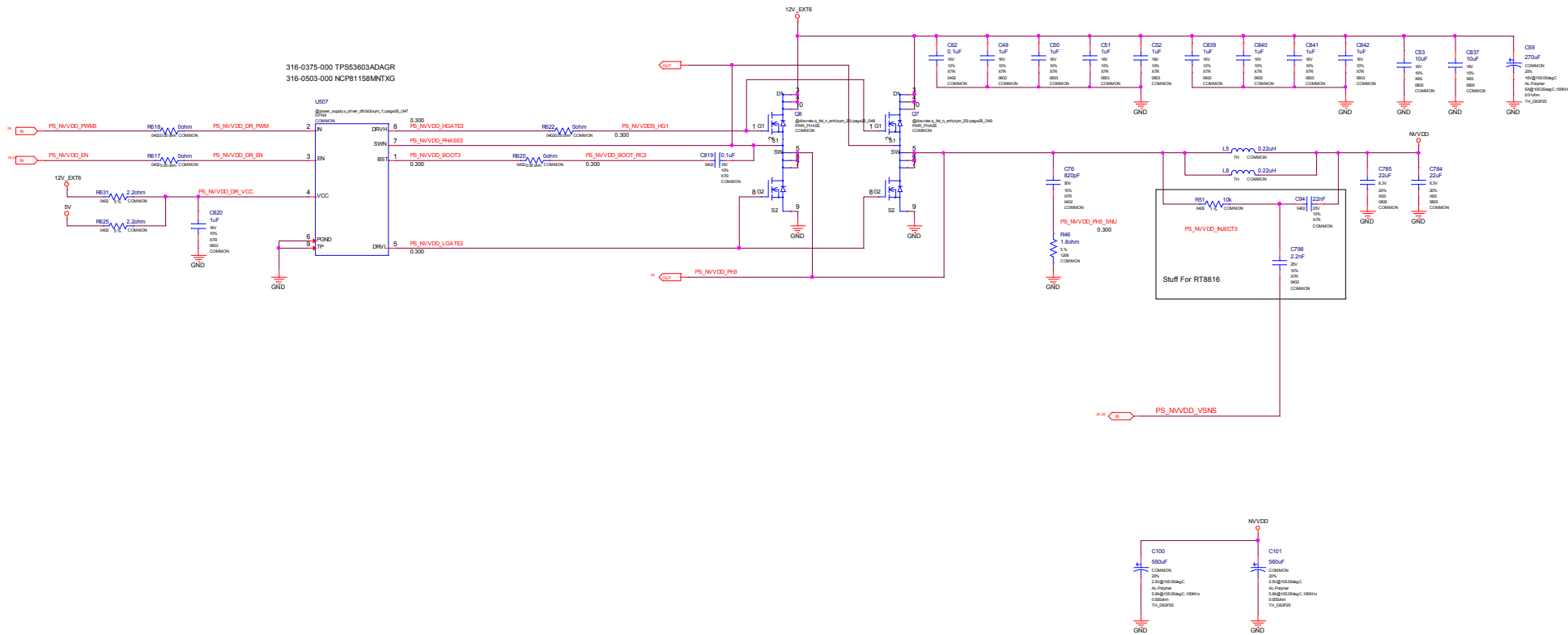


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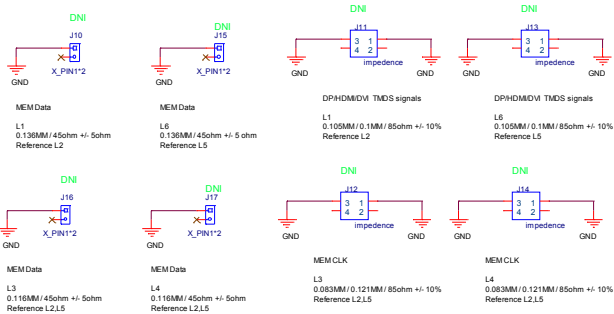
ASSEMBLY	ASSEMBLY_DESCRIPTION
PAGE DETAIL	PS V: NVVDD Phase 1,2

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NV_PN	600-1G210-BASE-SCH
PCB REV	PG210-800
ROM REV	A
PAGE	25 OF 27
DATE	18-DEC-2015

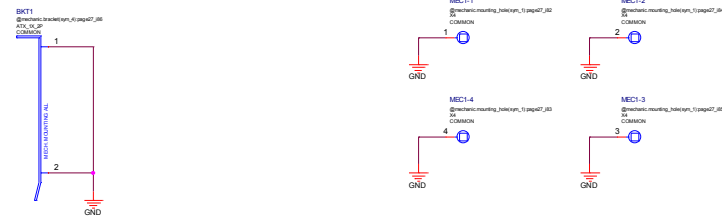
PS V: NVVDD Phase 3



Mechanical: Bracket/Thermal Solution



Brackets:



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MECH Bracket/Thermal

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NV_PN	600-1G210-BASE-SCH		
PCB REV	PG210-800	PAGE	27 OF 27
ROM REV	A	DATE	18-DEC-2015