PG410 A01

GP106 8GB/4GB GDDR5, 256b, 256Mx32/128MX32
Tall DVI-D + DP + DP + HDMI/DP + DP

TABLE OF CONTENTS

6.1
1.修改NVVDD_VREF線路
2.修改LED線路
3.增加COLAY線路
4.移除HDMI DP COLAY

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Custom	01	6.1

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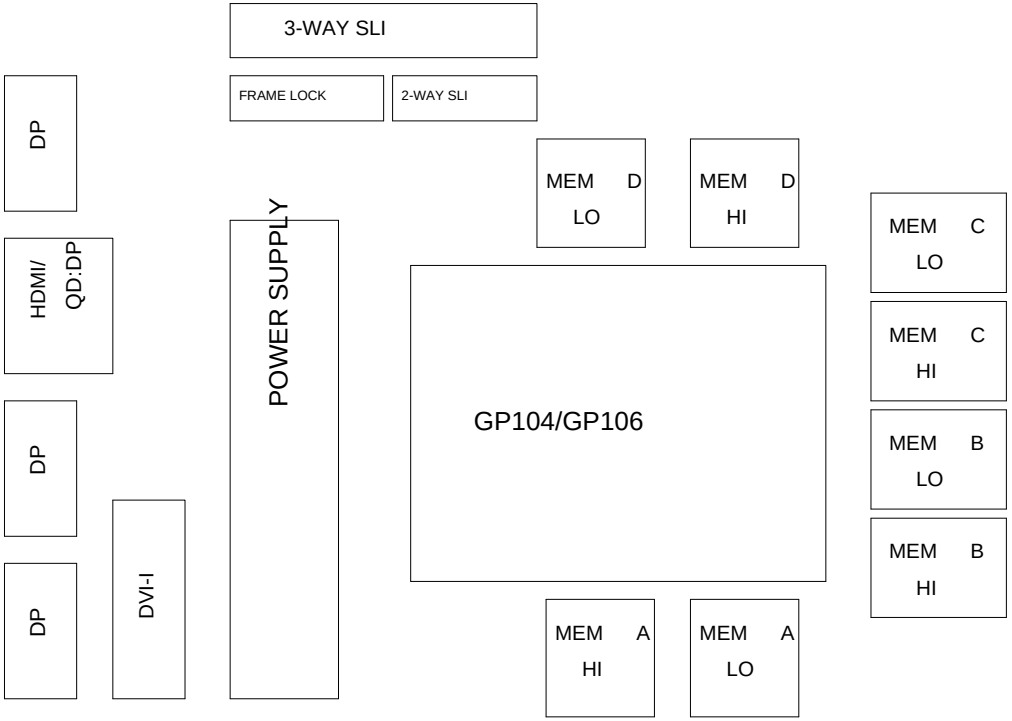
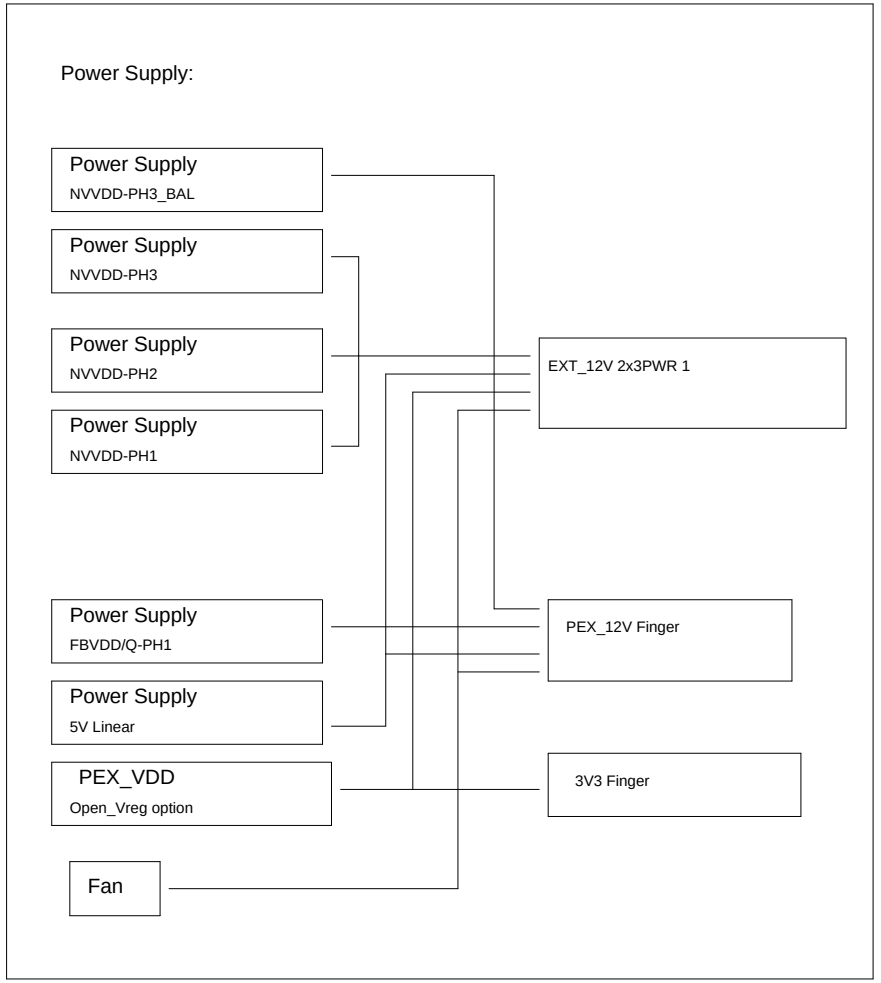
Page2: Block Diagram





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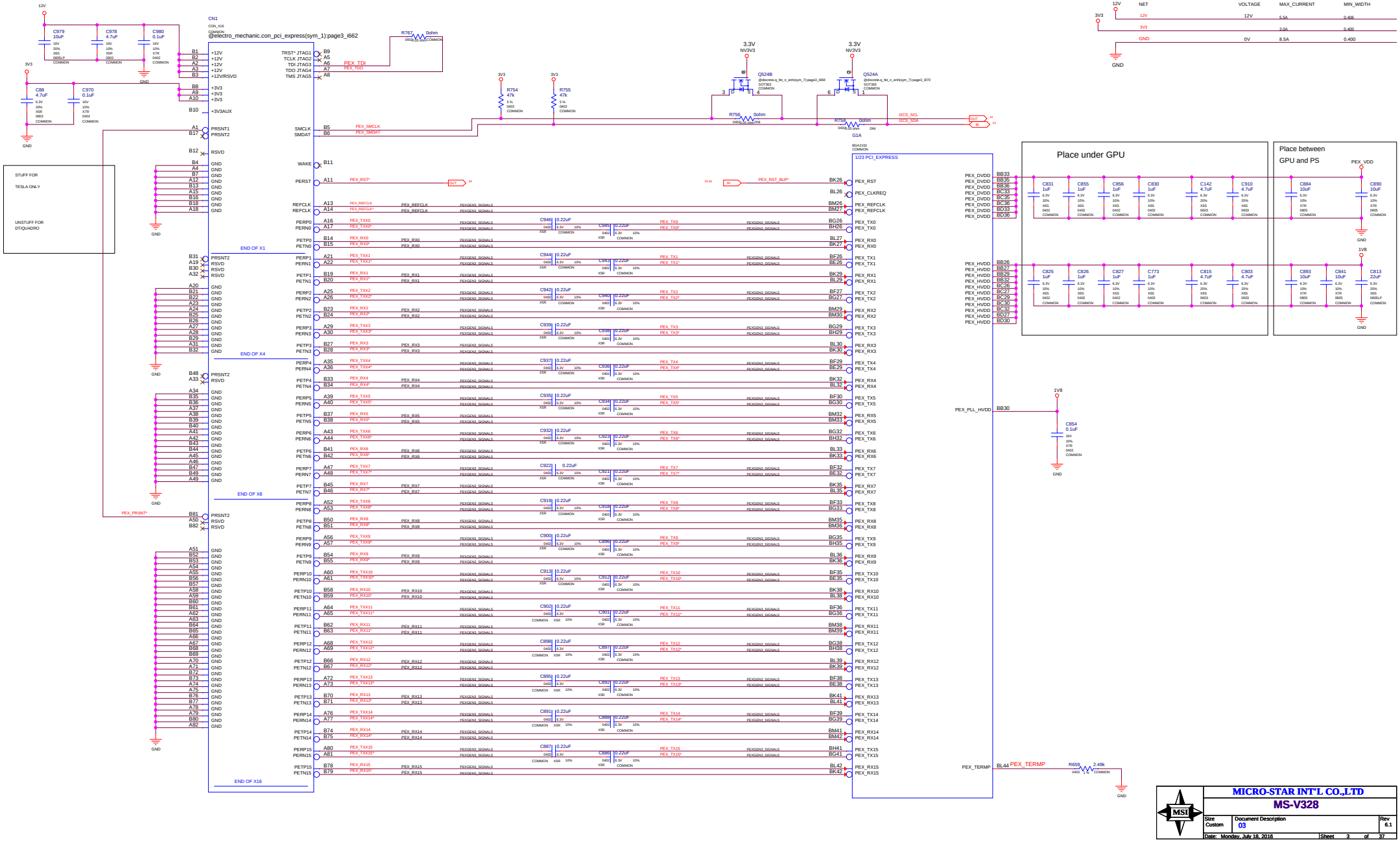
Page3: PCI Express



NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
12V	12V	5.5A	0.406
3V3	3.0A	0.400	
GND	0V	8.5A	0.400

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Page4: MEMORY: GPU Partition A/B

GDDR5 CMD Mapping

CMD	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

G1B
BGA2152
COMMON
2/23 FBA

G1C
BGA2152
COMMON
3/23 FBB

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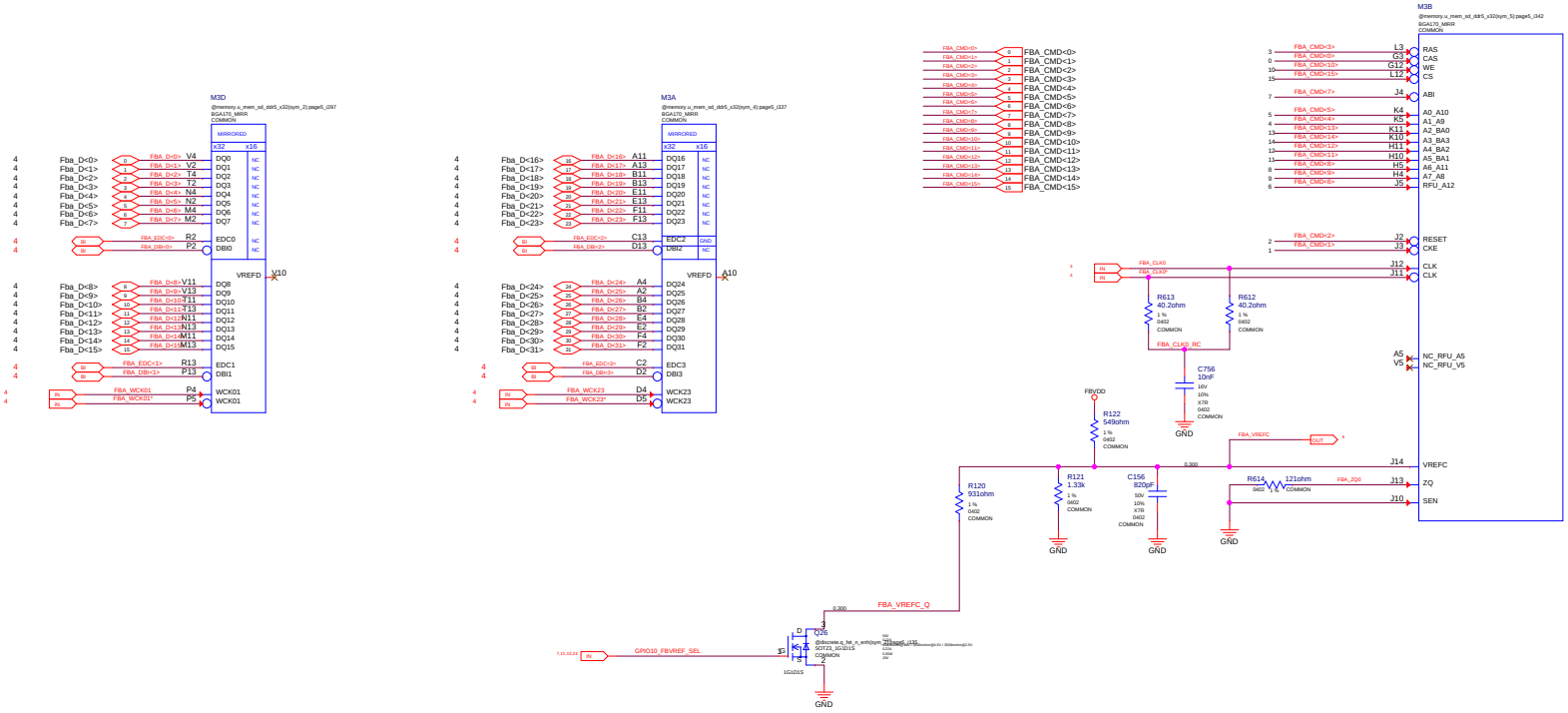
Page5: FRAME BUFFER PARTITION A [31:0]



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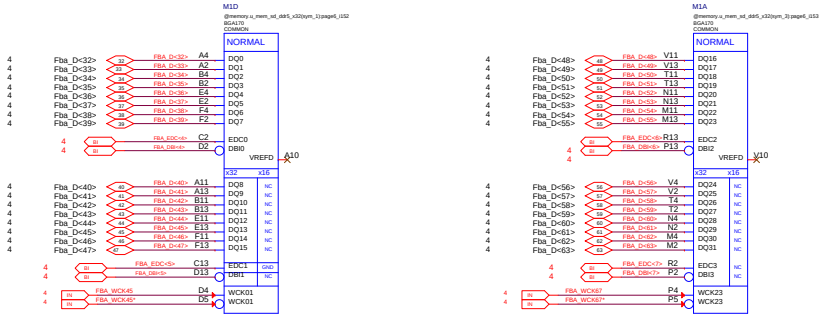
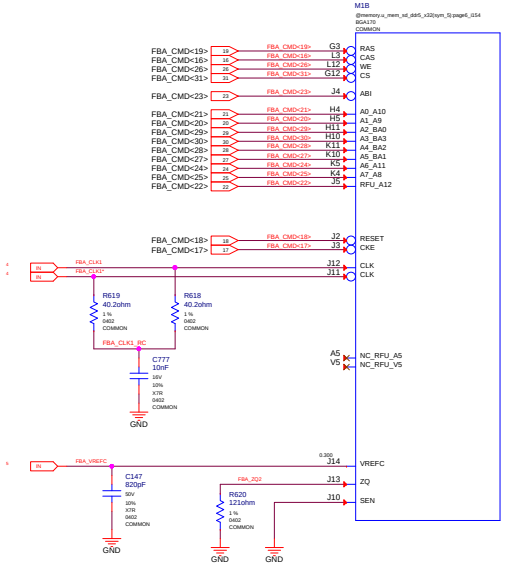
Page6: FRAME BUFFER PARTITION A [63:32]





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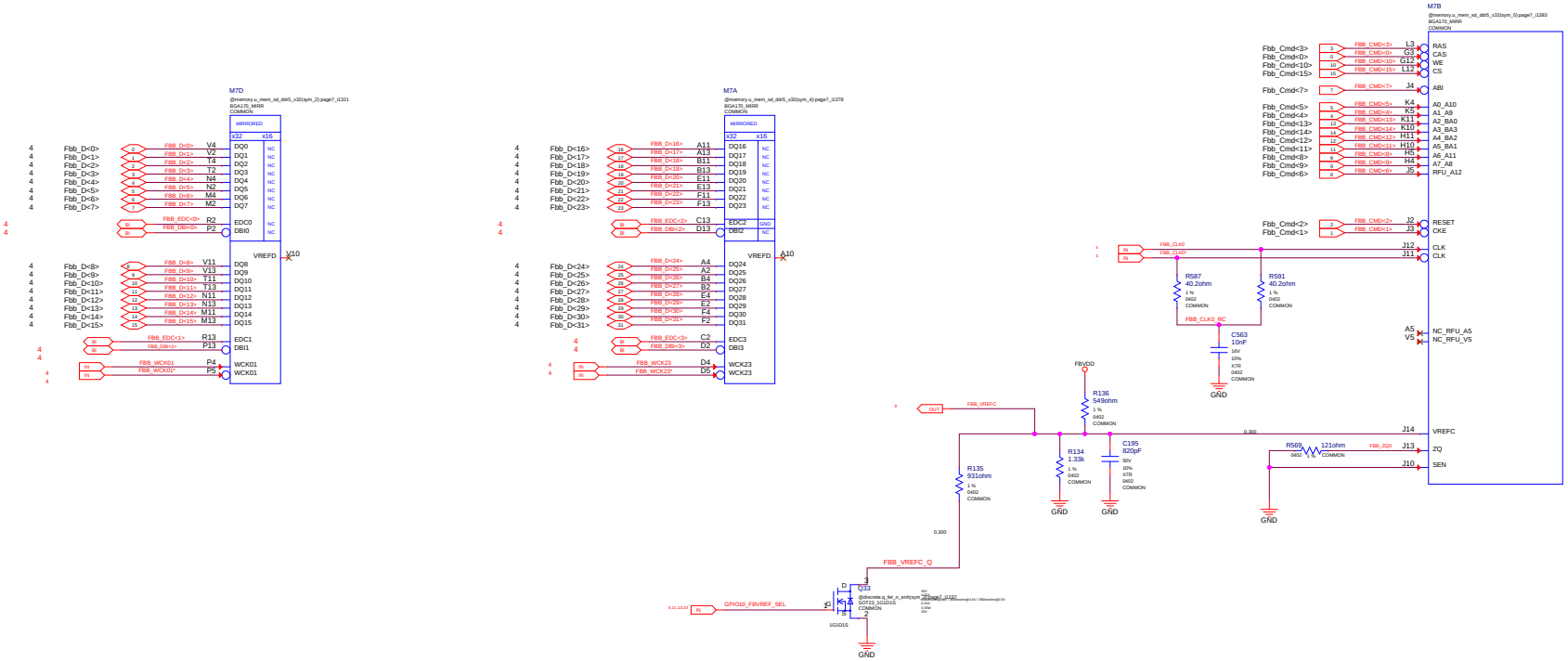
Page7: FRAME BUFFER PARTITION B [31:0]



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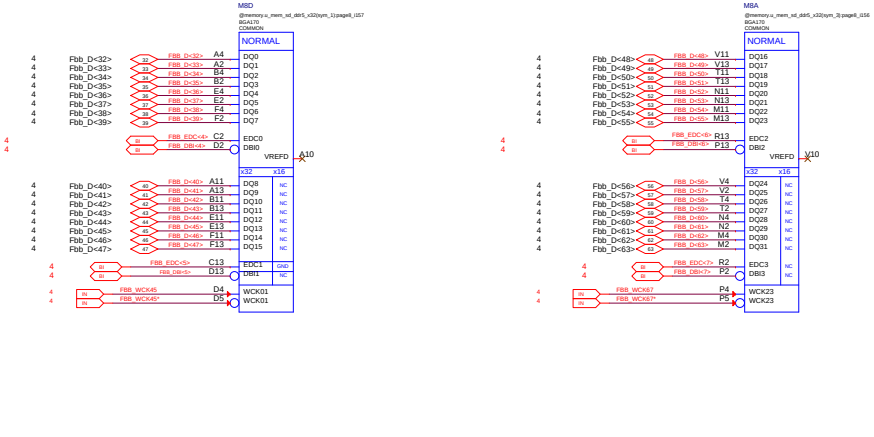
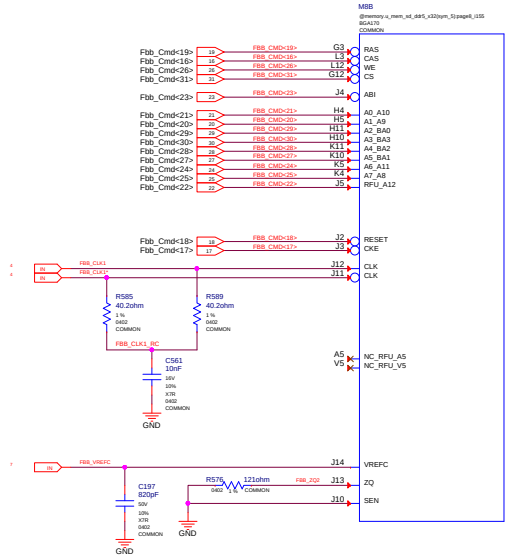
Page8: FRAME BUFFER PARTITION B [63:32]





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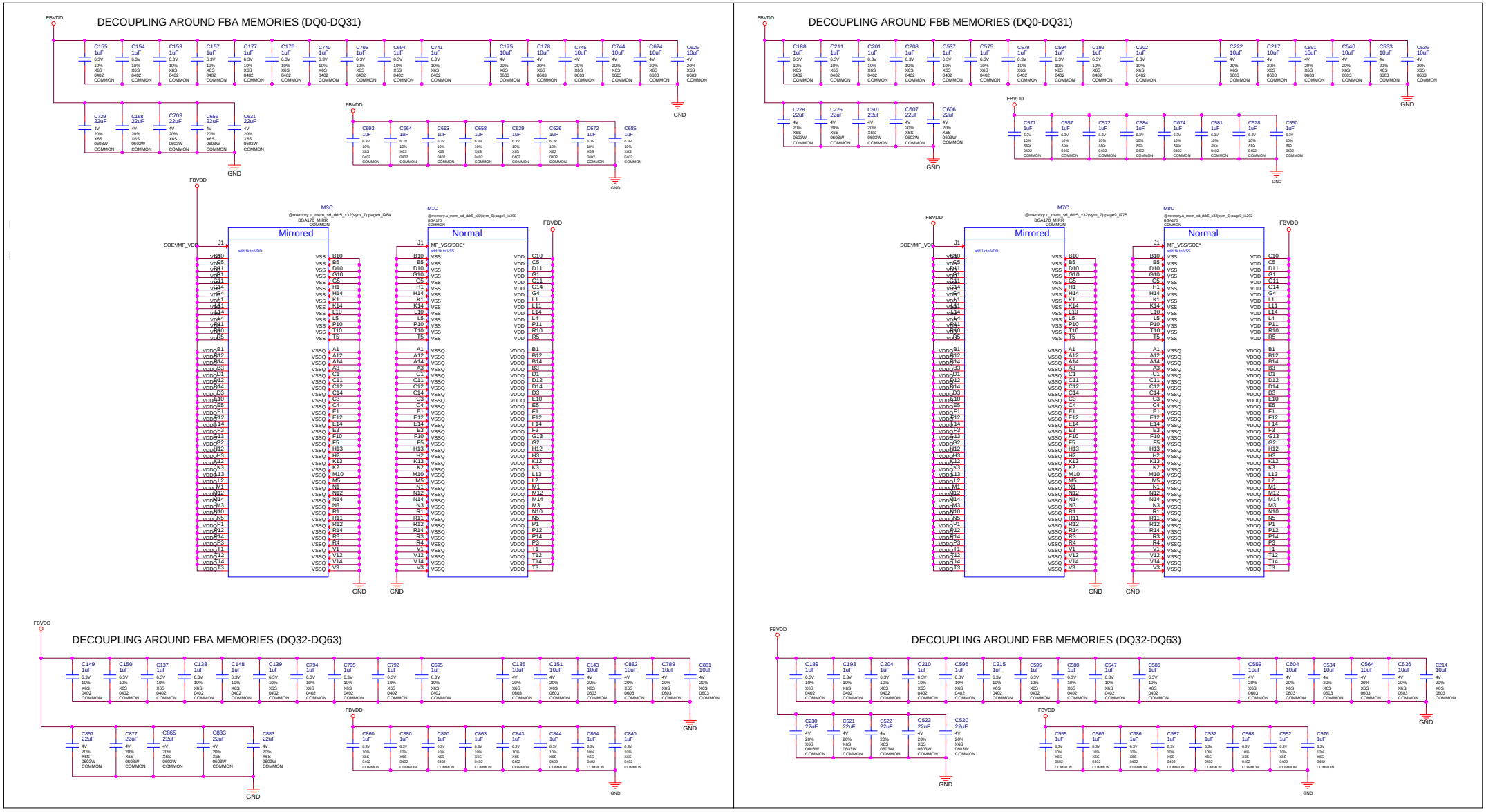
Page9: FRAME BUFFER PARTITION A/B DECOUPLING



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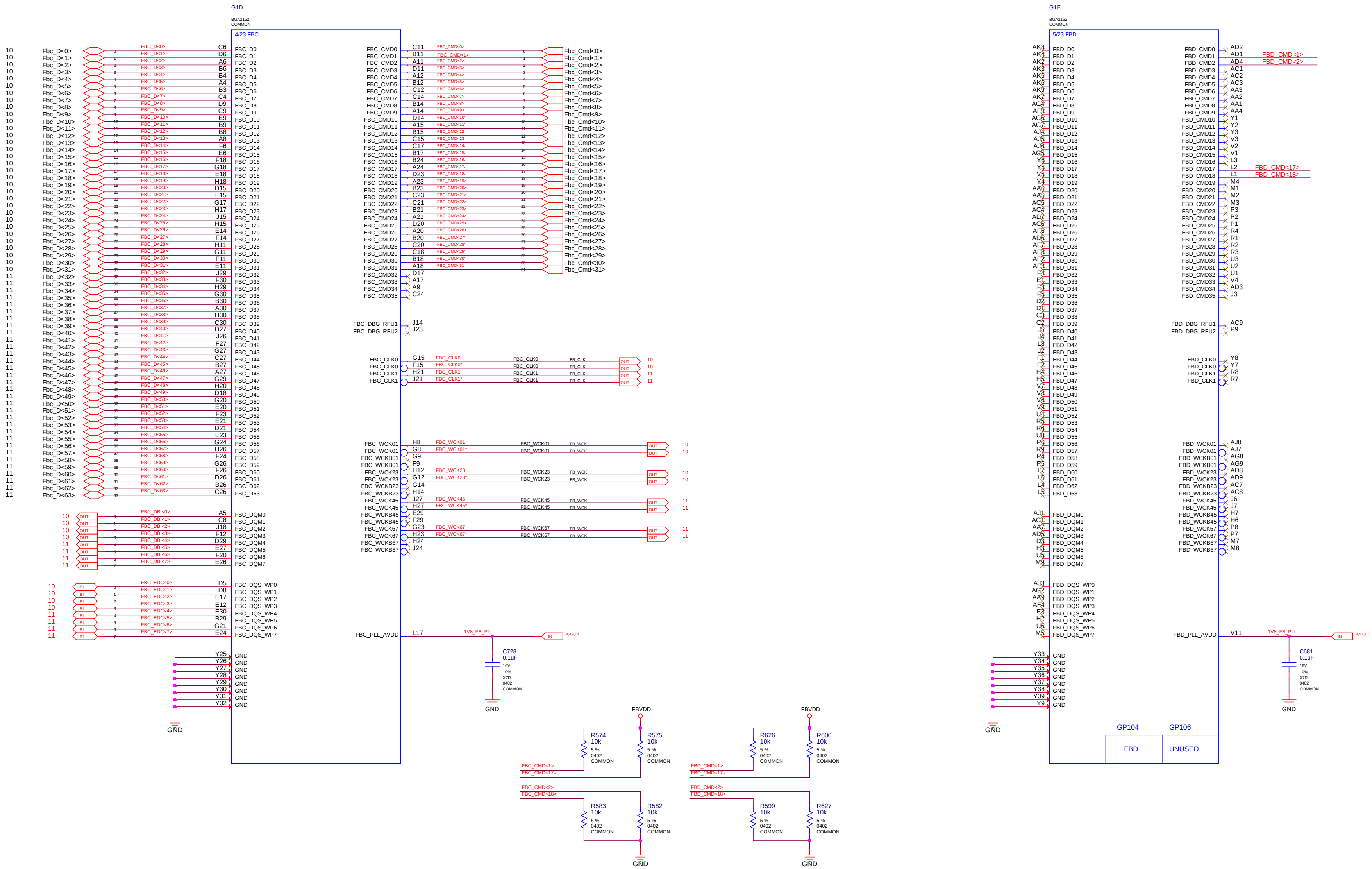
Page10: MEMORY: GPU Partition C/D

GDDR5 CMD Mapping

CMD	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*



G1D
BGA2152
COMMON
4/23 FBC
Fbc_D<0> ... Fbc_D<63>
FBC_D0 ... FBC_D63
FBC_CMD0 ... FBC_CMD35
Fbc_Cmd<0> ... Fbc_Cmd<31>
FBC_DBG_RFU1
FBC_DBG_RFU2
FBC_CLK0
FBC_CLK0*
FBC_CLK1
FBC_CLK1*
FB_CLK
FBC_WCK01
FBC_WCK23
FBC_WCK45
FBC_WCK67
FB_WCK
FBC_DQM0 ... FBC_DQM7
FBC_DBI<0> ... FBC_DBI<7>
FBC_DQS_WP0 ... FBC_DQS_WP7
FBC_EDC<0> ... FBC_EDC<7>
FBC_PLL_AVDD
1V8_FB_PLL
IN
4,4,4,10
C728
0.1uF
16V
10%
X7R
0402
COMMON
GND
FBVDD
R574 10k
R575 10k
R583 10k
R582 10k
R626 10k
R600 10k
R599 10k
R627 10k
5 %
0402
COMMON
FBC_CMD<1>
FBC_CMD<17>
FBC_CMD<2>
FBC_CMD<18>
FBD_CMD<1>
FBD_CMD<17>
FBD_CMD<2>
FBD_CMD<18>
G1E
BGA2152
COMMON
5/23 FBD
FBD_D0 ... FBD_D63
FBD_CMD0 ... FBD_CMD35
FBD_DBG_RFU1
FBD_DBG_RFU2
FBD_CLK0
FBD_CLK1
FBD_WCK01
FBD_WCKB01
FBD_WCK23
FBD_WCKB23
FBD_WCK45
FBD_WCKB45
FBD_WCK67
FBD_WCKB67
FBD_DQM0 ... FBD_DQM7
FBD_DQS_WP0 ... FBD_DQS_WP7
FBD_PLL_AVDD
V11
C681
0.1uF
GP104
GP106
FBD
UNUSED

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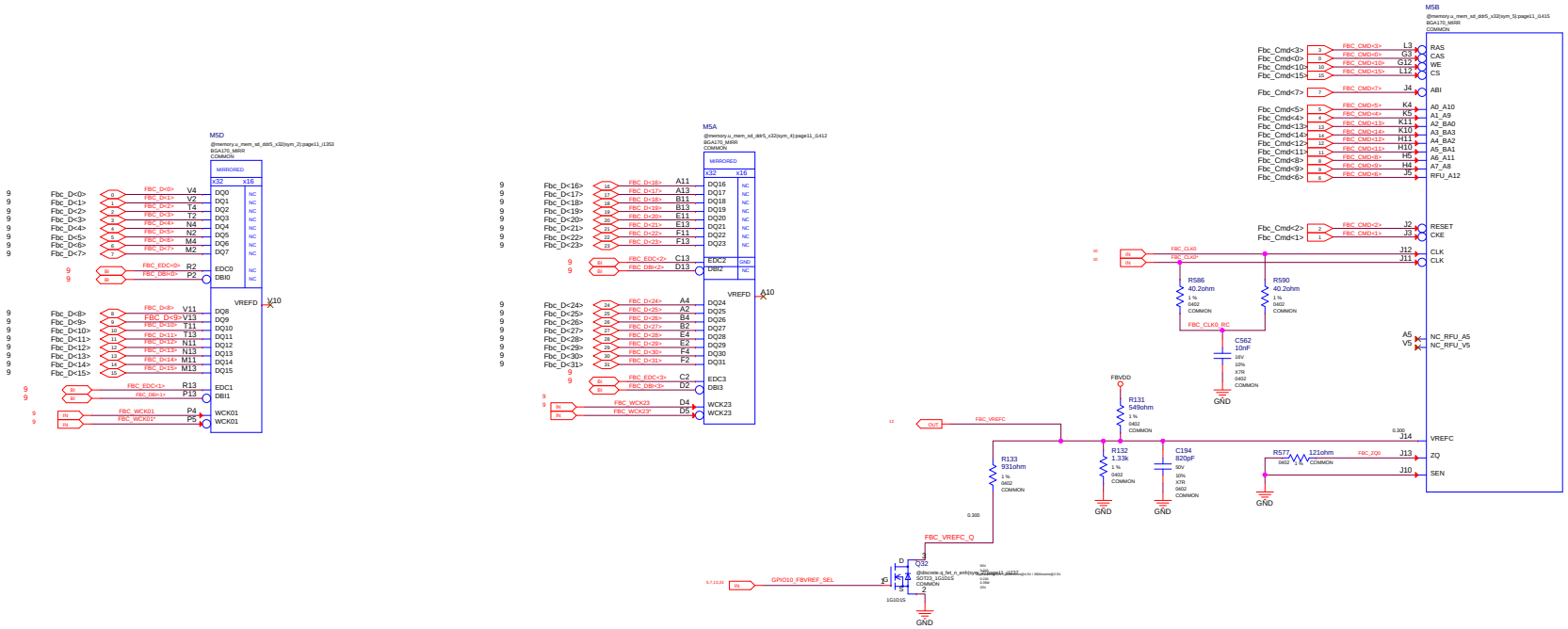
Page11: Frame Buffer Partition C [31:0]



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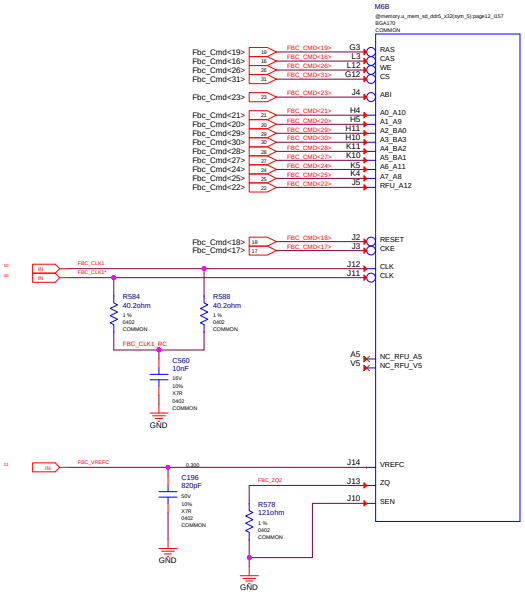
Page12: FRAME BUFFER PARTITION C [63:32]



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Page13: FRAME BUFFER PARTITION D[31:0]

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Page14: FRAME BUFFER PARTITION D[63:32]

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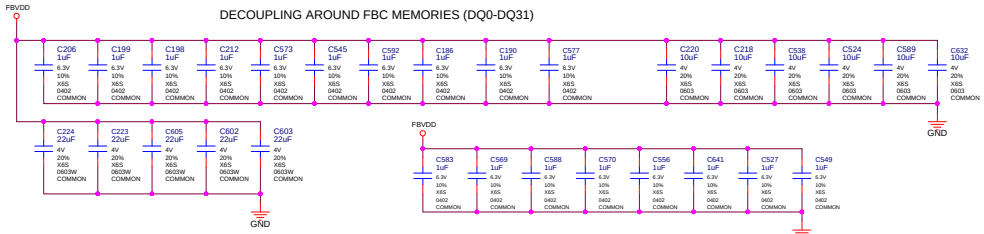
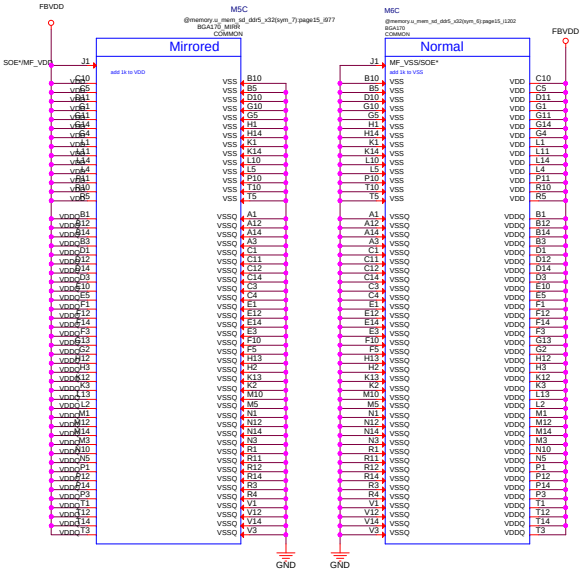
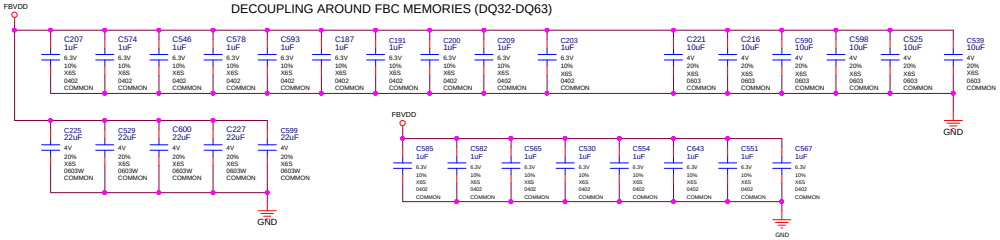
Page15: FRAME BUFFER PARTITION C/D DECOUPLING







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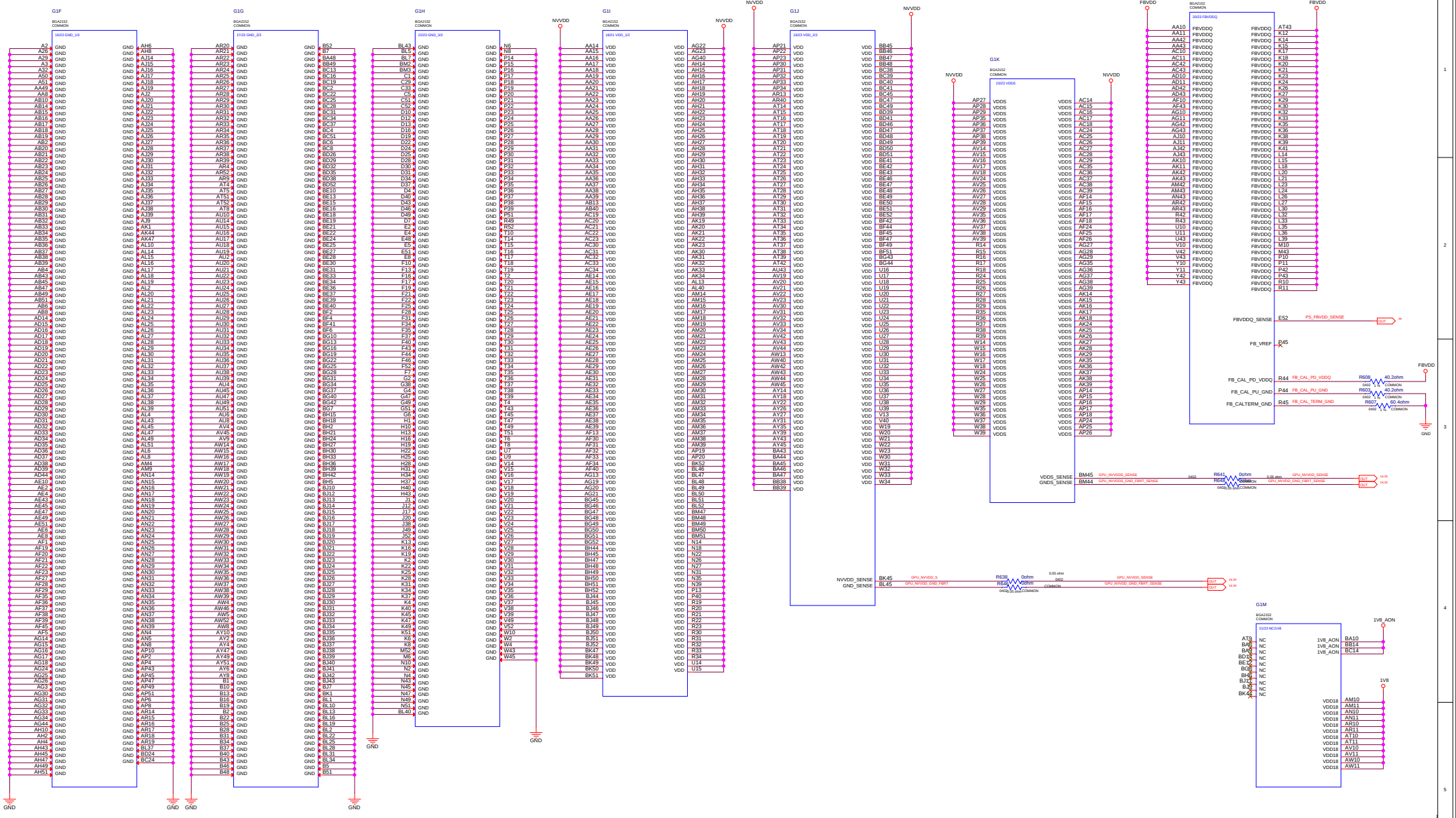
Page16: GPU PWR and GND



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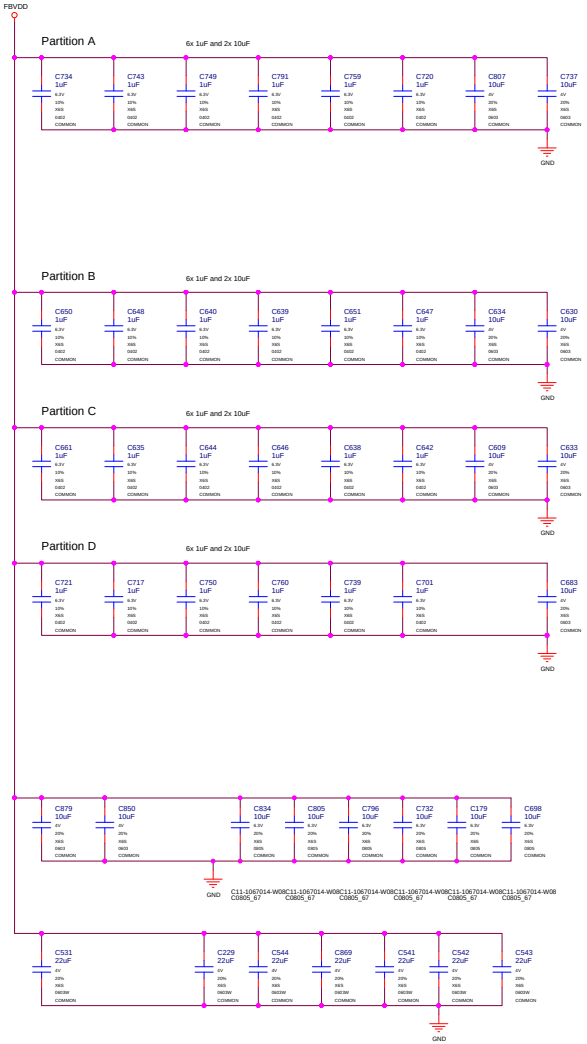
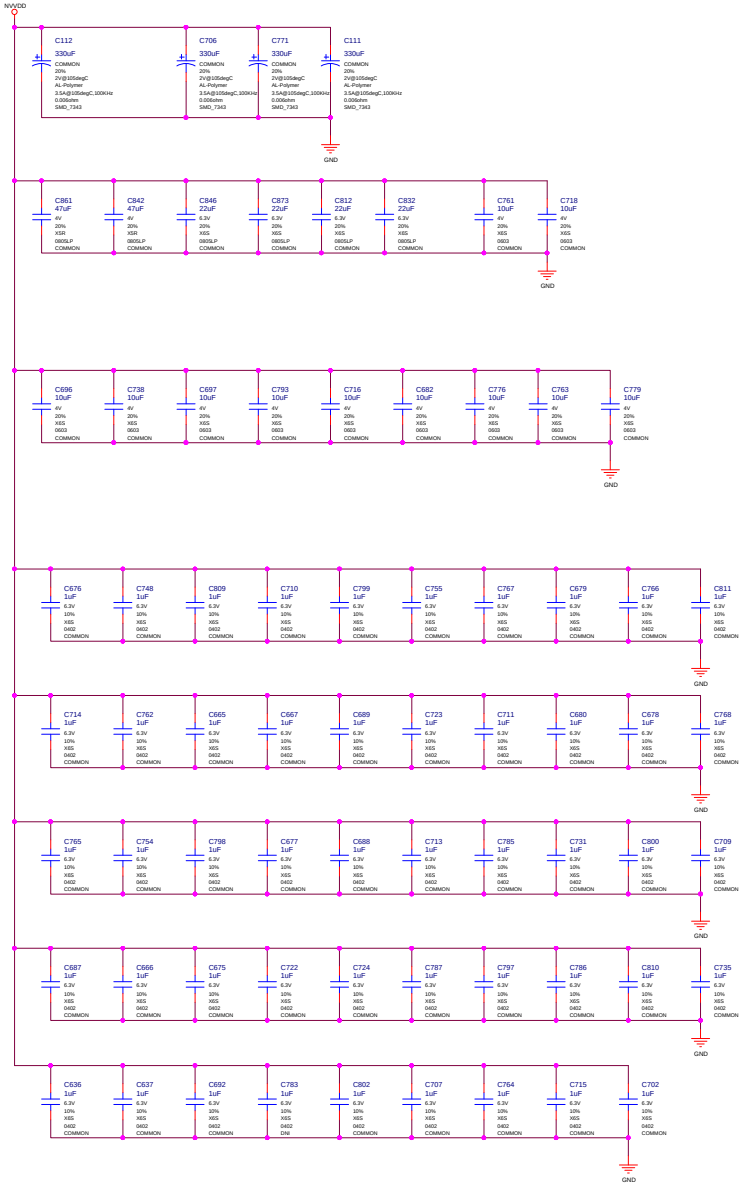
Page17: GPU Decoupling

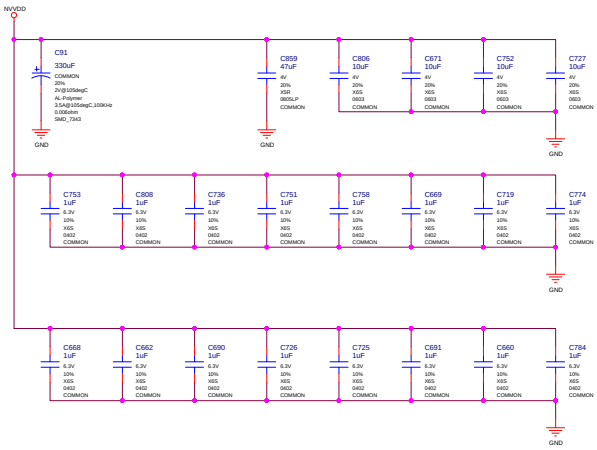
FBVDD



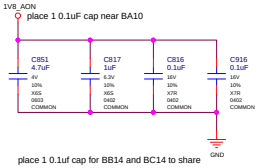
NVVDD



NVVDD

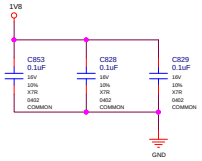


1V8_AON



place 1 0.1uf cap for BB14 and BC14 to share

1V8_MAIN



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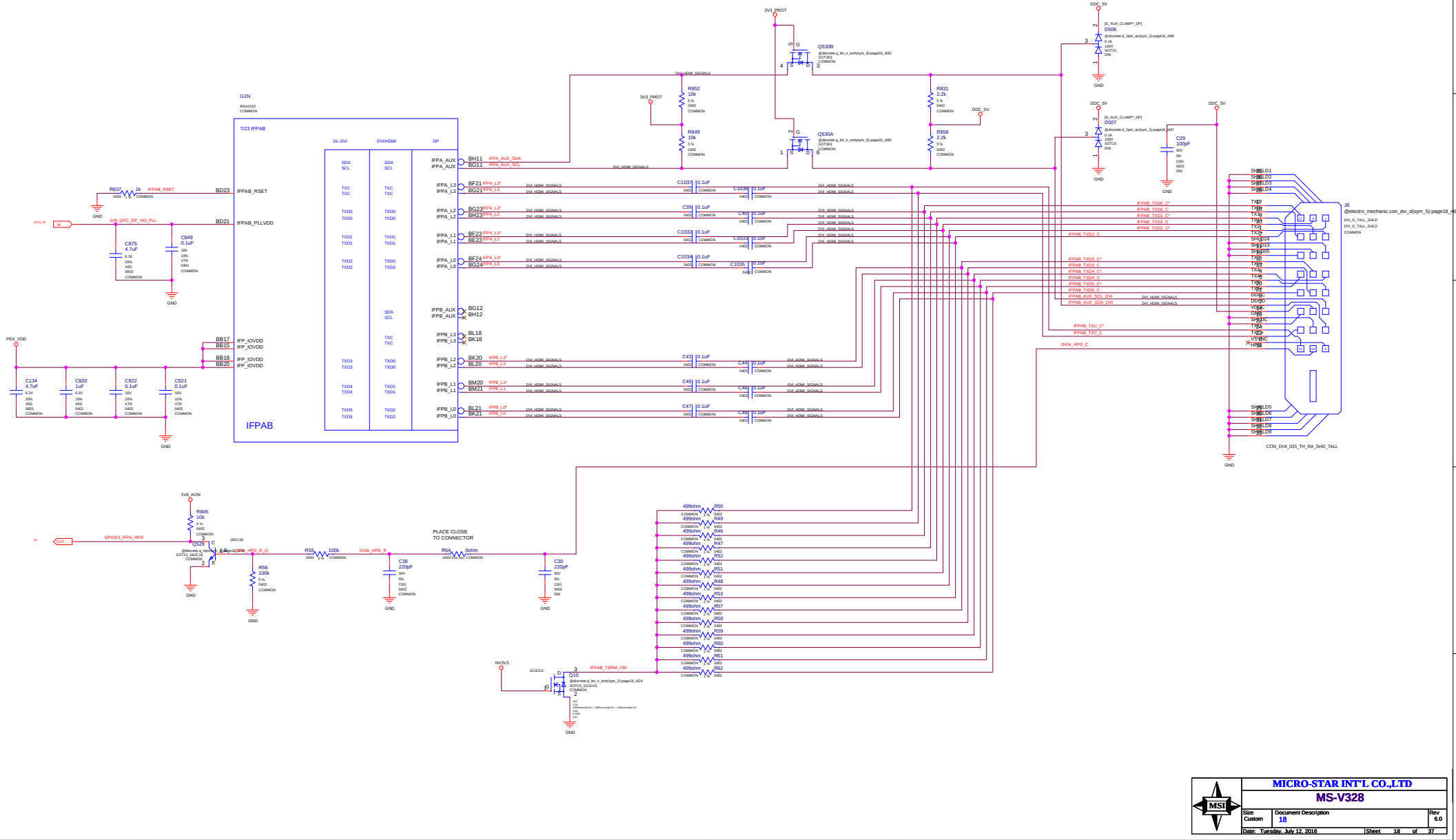
Page18: IFPAB DVI-D-DL



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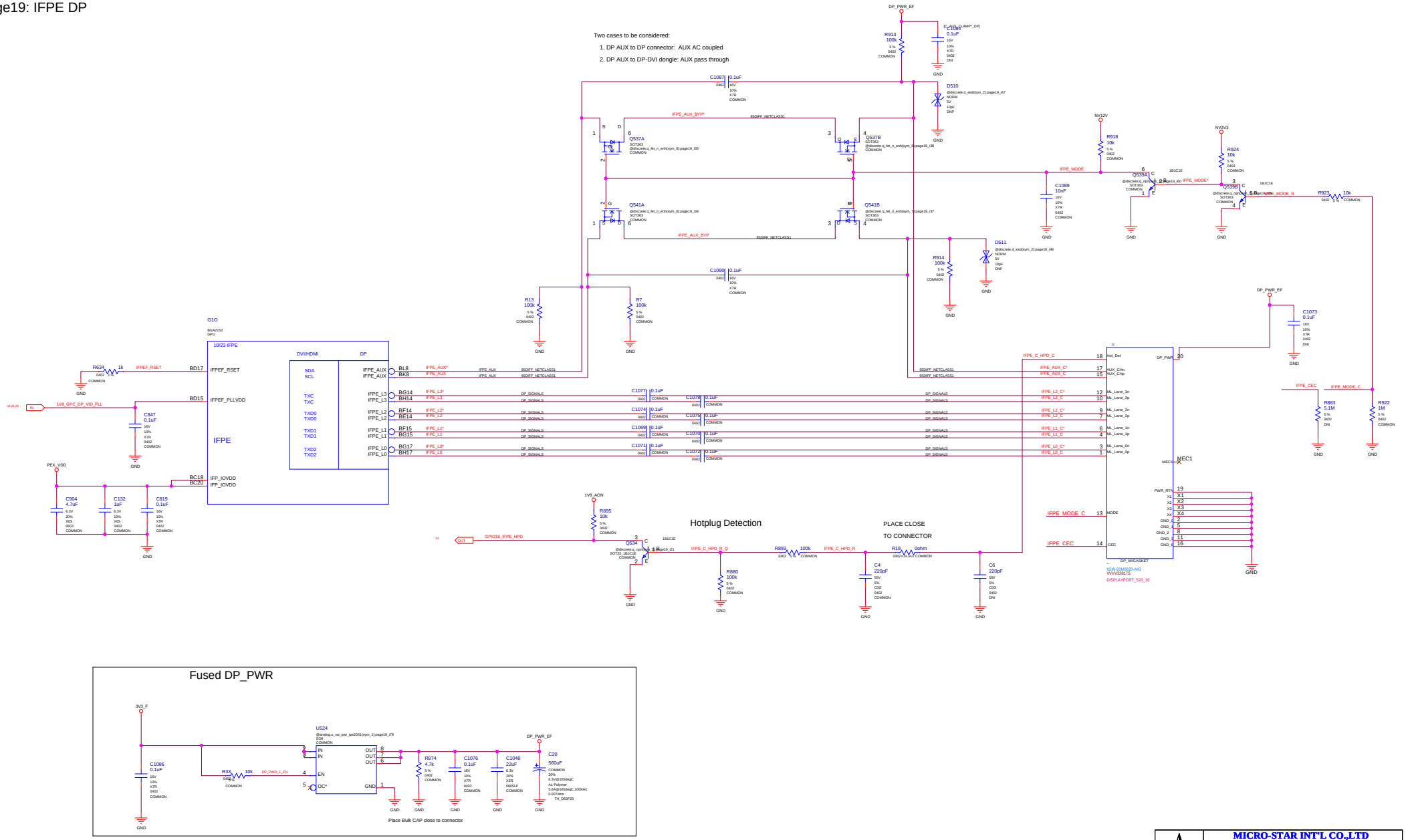
Page19: IFPE DP



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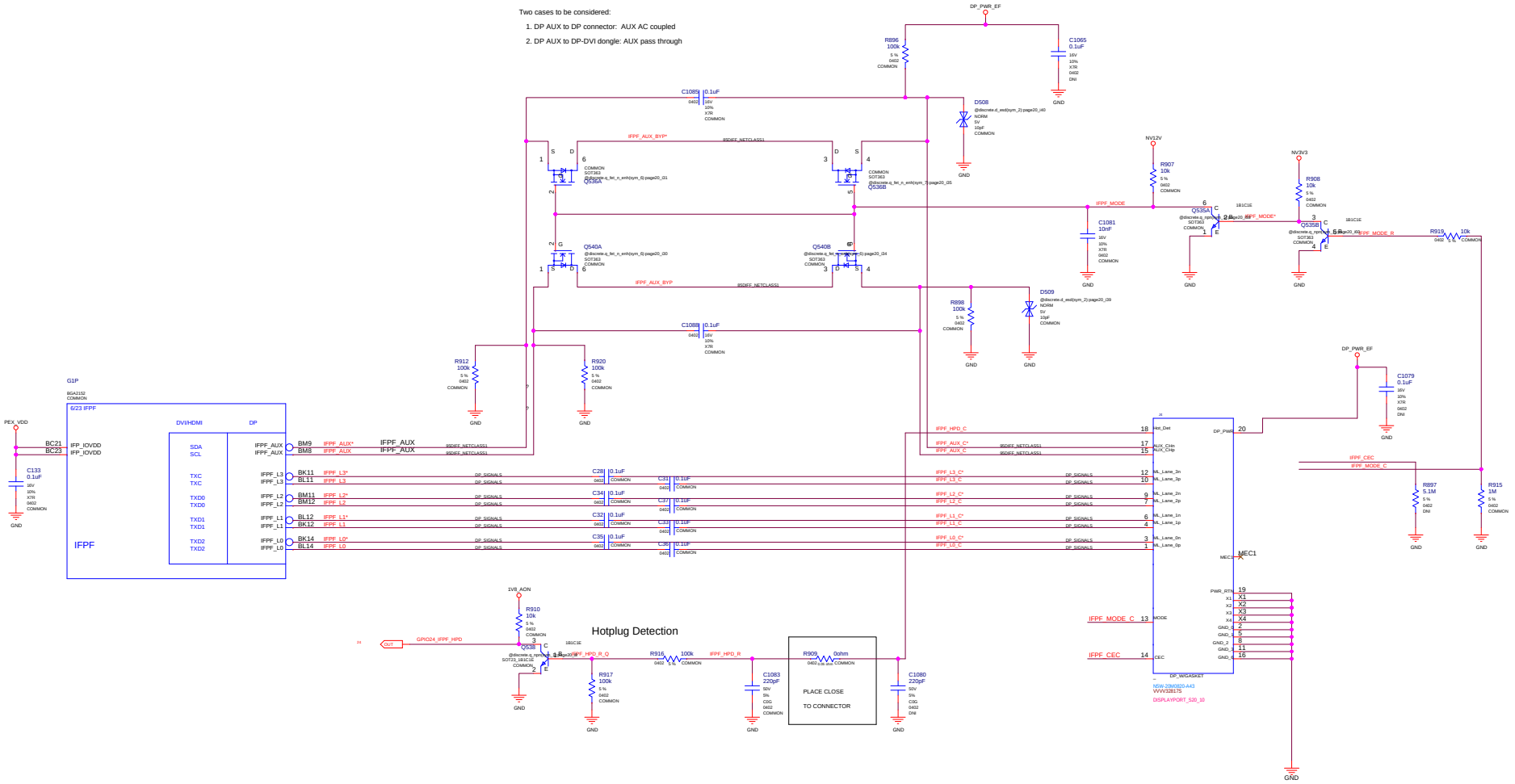
Page 20: IFPF DP



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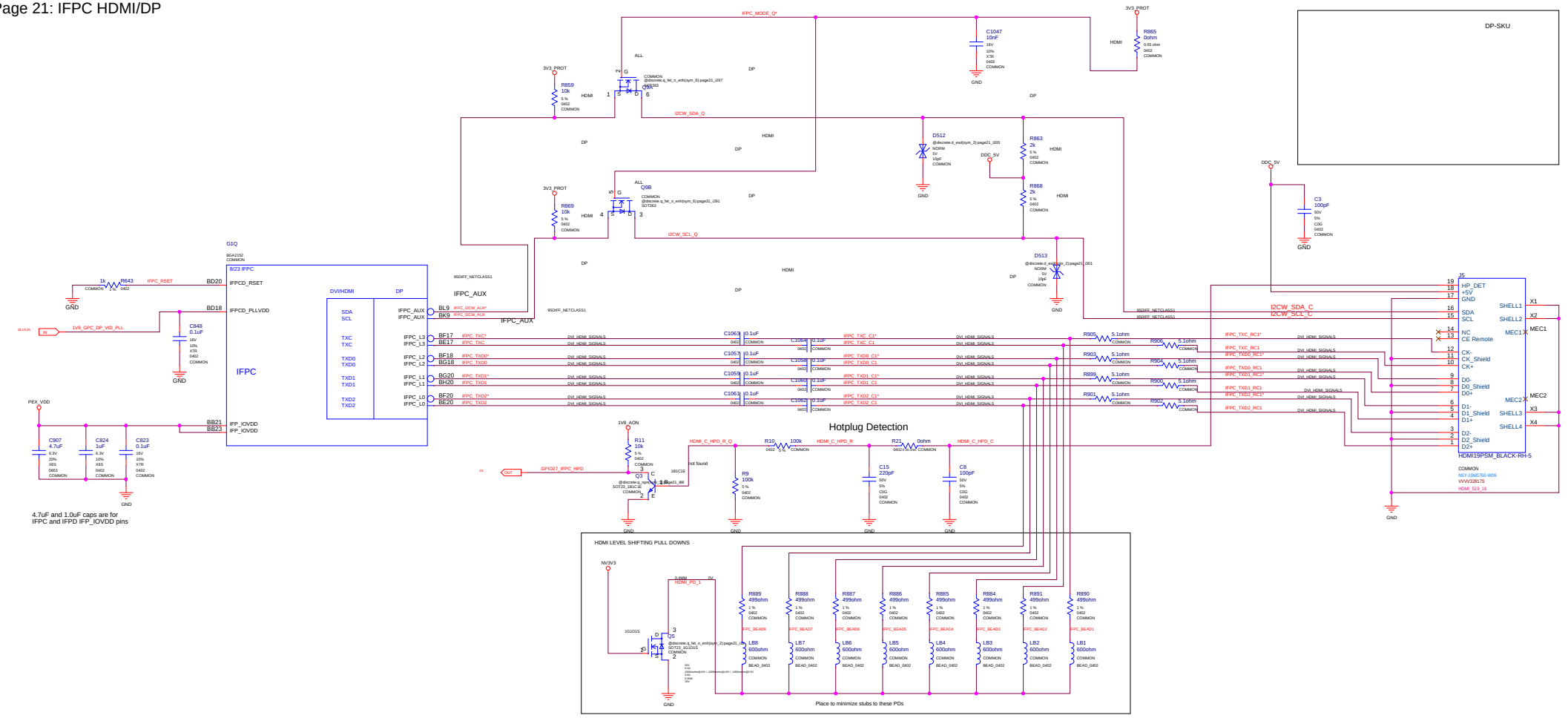
Page 21: IFPC HDMI/DP



Fused DP_PWR

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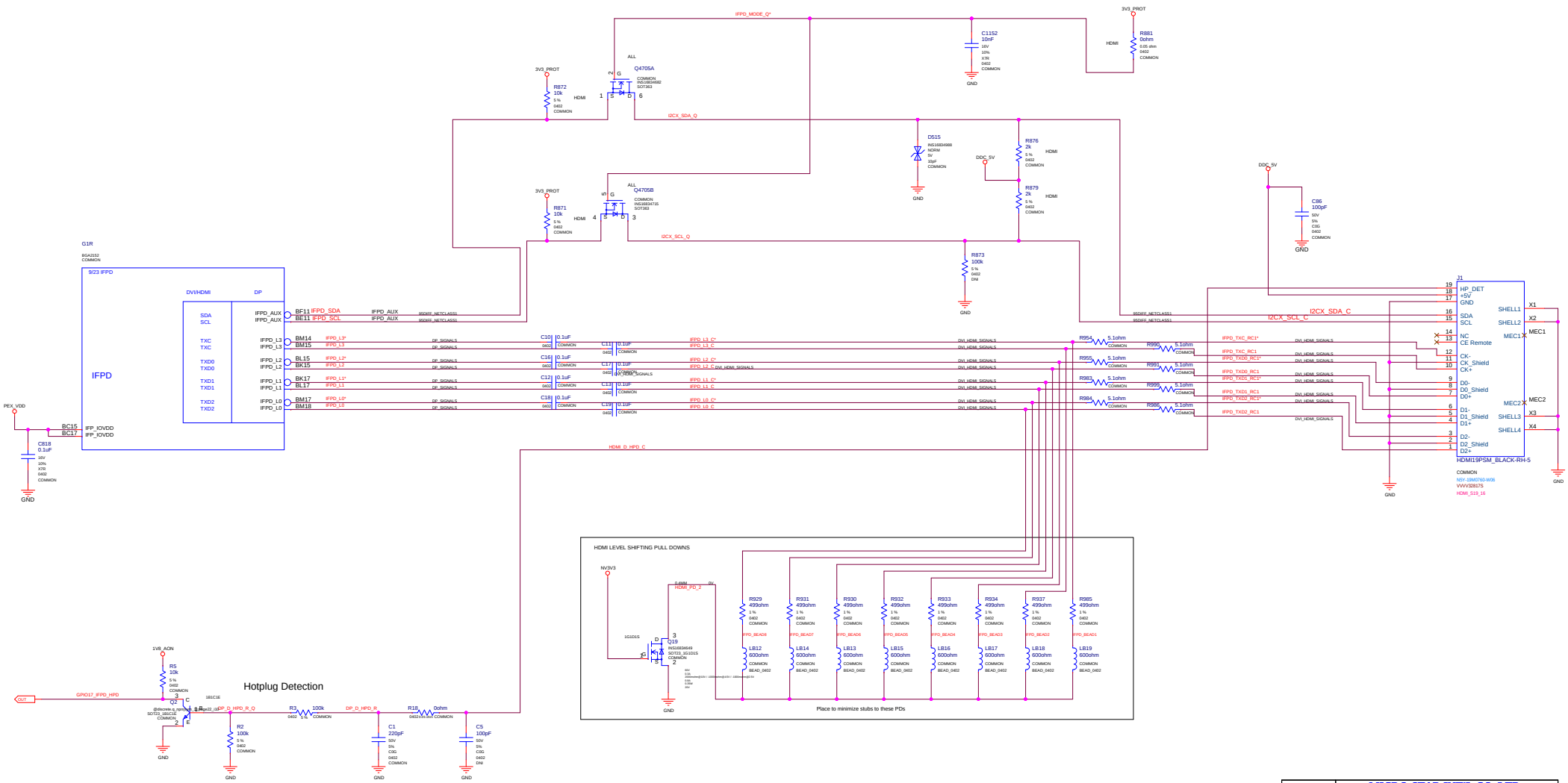

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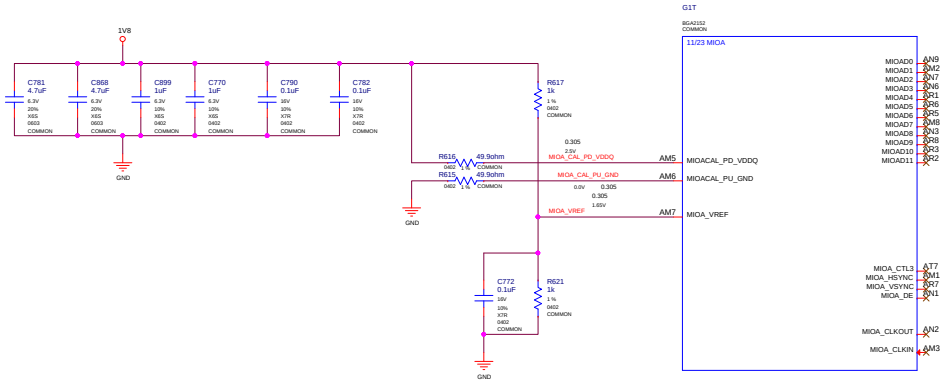
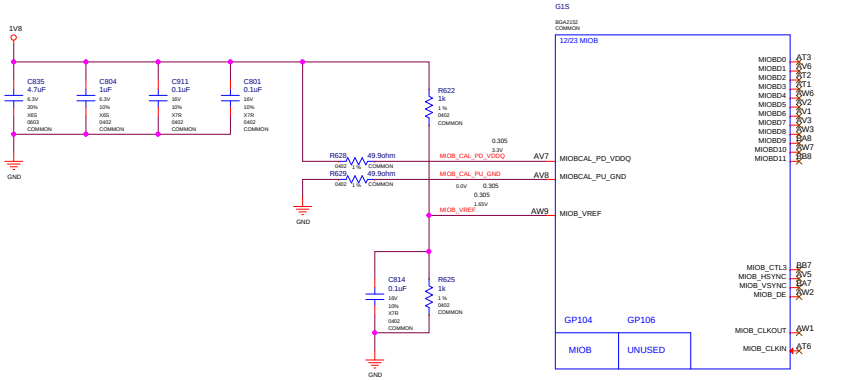
Page 23: MIOA/B Interface and Frame Lock





Pad Overlap R1042 & R1043

MSI	MICRO-STAR INT'L CO.,LTD	
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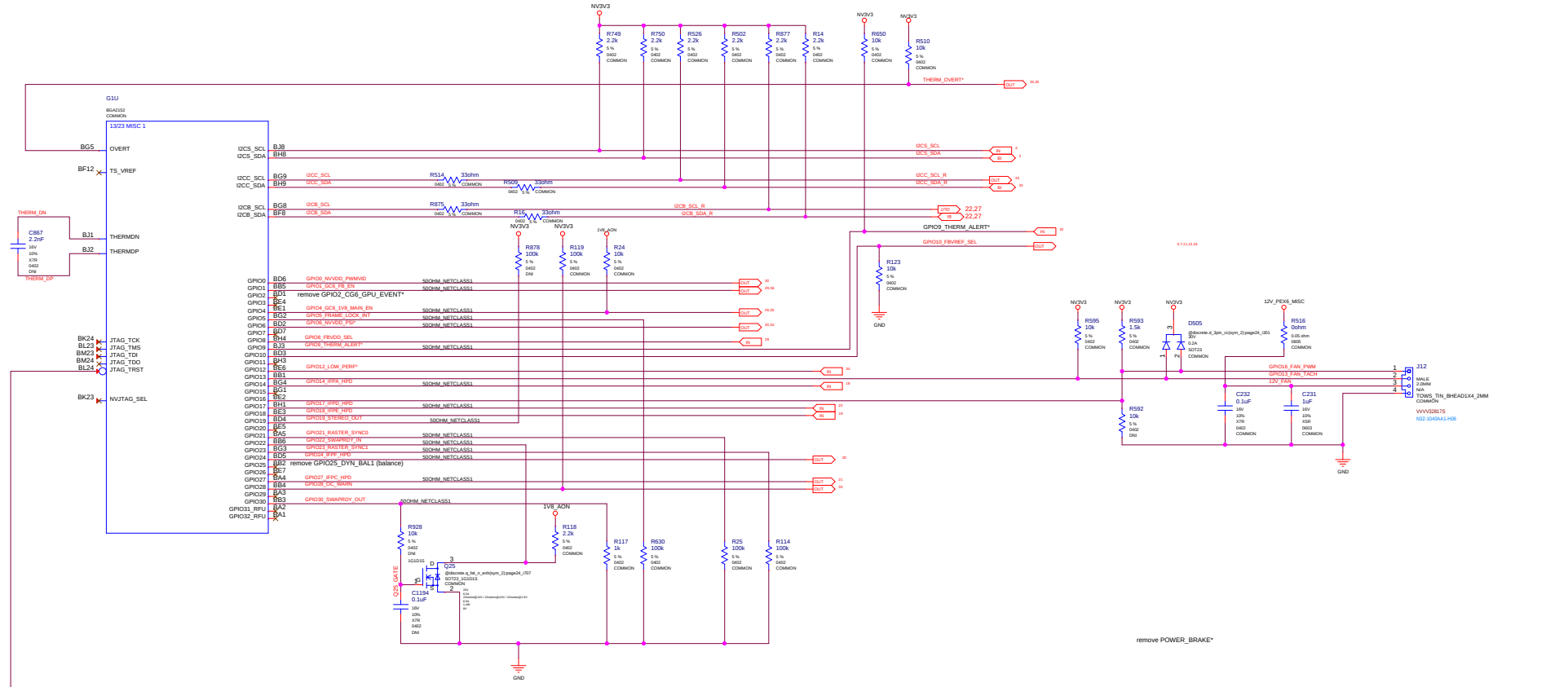

STEREO

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Page25: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

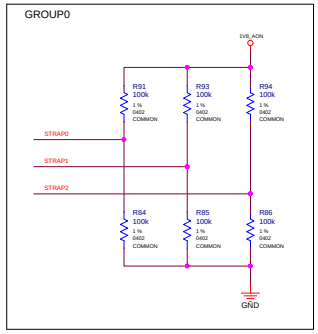
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

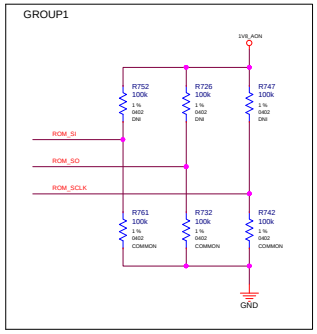
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

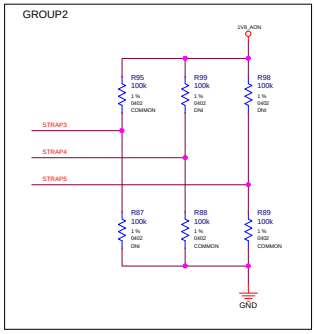
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

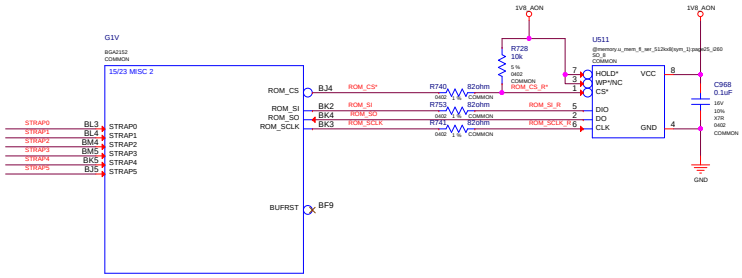
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

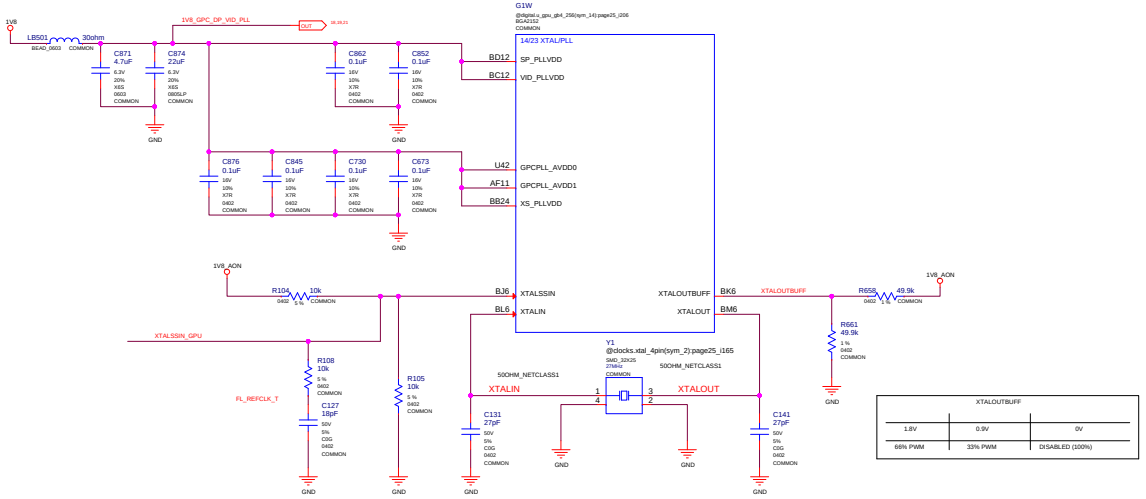






CFG[3:0]	Config Width	Vendor
0000	256Mx32 256-bit	Samsung
0001	256Mx32 256-bit	Micron
0010	256Mx32 256-bit	Hynix
0011	Reserved	
0100	Reserved	
0101	Reserved	
0110	Reserved	
0111	Reserved	





XTALOUTBUFF		
1.8V	0.9V	0V
66% PWM	33% PWM	DISABLED (100%)

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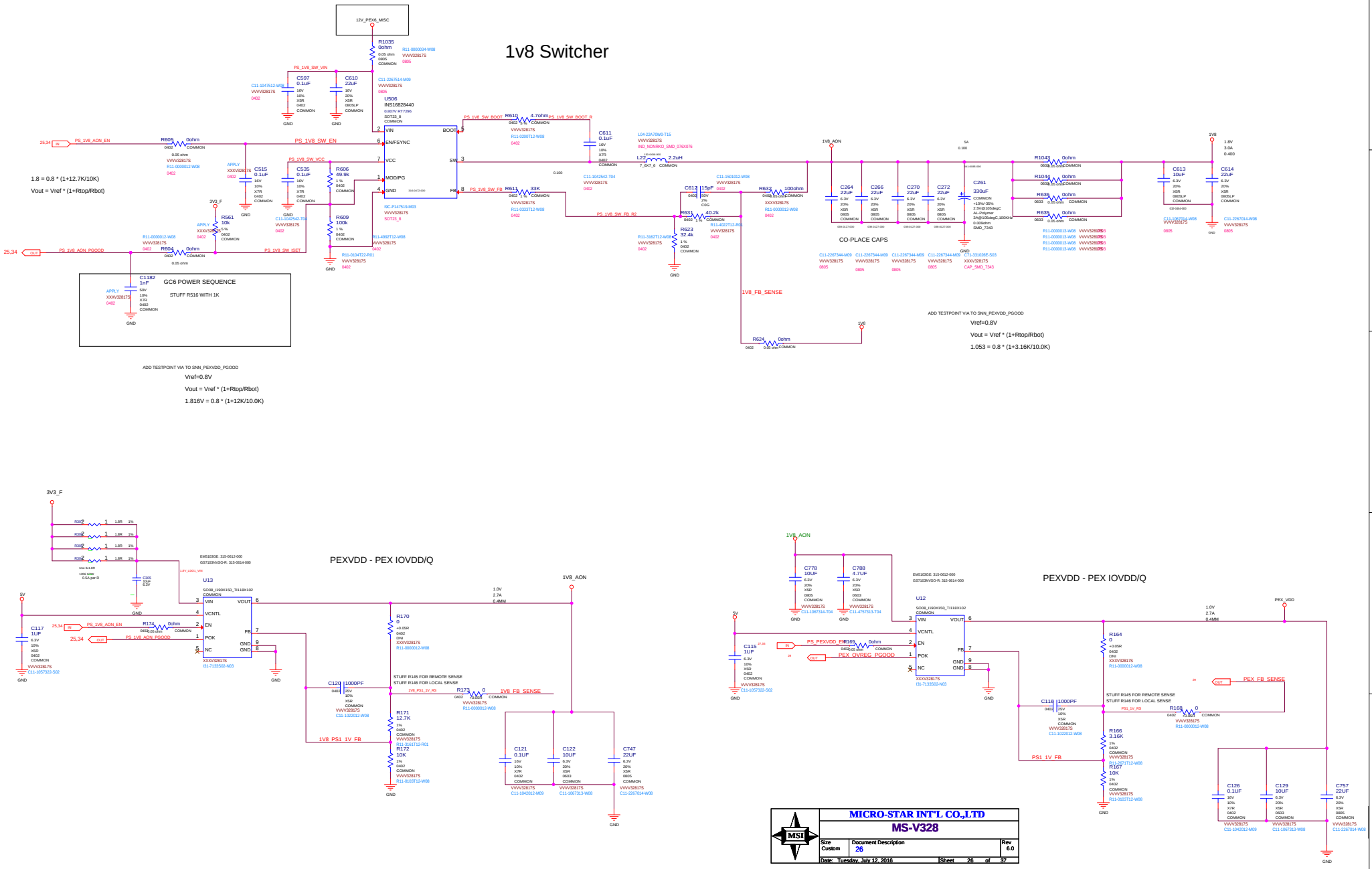
1v8 Switcher
12V_PEX6_MISC
R1035 0ohm
PS_1V8_SW_VIN
C597 0.1uF
C610 22uF
U506 INS16828440
PS_1V8_SW_BOOT
R610 4.7ohm
PS_1V8_SW_BOOT_R
C611 0.1uF
L22 2.2uH
PS_1V8_AON_EN
R605 0ohm
PS_1V8_SW_EN
PS_1V8_SW_VCC
C515 0.1uF
C535 0.1uF
R606 49.9k
R609 100k
PS_1V8_SW_FB
R611 33K
PS_1V8_SW_FB_R2
C612 15pF
R631 40.2k
R623 32.4k
R632 100ohm
C264 22uF
C266 22uF
C270 22uF
C272 22uF
C261 330uF
R1043 0ohm
R1044 0ohm
R635 0ohm
C613 10uF
C614 22uF
1V8_AON
1V8
1.8V
3.0A
0.400
1.8 = 0.8 * (1+12.7K/10K)
Vout = Vref * (1+Rtop/Rbot)
3V3_F
R561 10k
R604 0ohm
PS_1V8_AON_PGOOD
PS_1V8_SW_ISET
C1182 1nF
GC6 POWER SEQUENCE
STUFF RS16 WITH 1K
CO-PLACE CAPS
1V8_FB_SENSE
R624 0ohm
ADD TESTPOINT VIA TO SNN_PEXVDD_PGOOD
Vref=0.8V
Vout = Vref * (1+Rtop/Rbot)
1.816V = 0.8 * (1+12K/10.0K)
ADD TESTPOINT VIA TO SNN_PEXVDD_PGOOD
Vref=0.8V
Vout = Vref * (1+Rtop/Rbot)
1.053 = 0.8 * (1+3.16K/10.0K)
PEXVDD - PEX IOVDD/Q
3V3_F
5V
U13
C117 1UF
PS_1V8_AON_EN
R174 0ohm
PS_1V8_AON_PGOOD
C120 1000PF
R170 0
R171 12.7K
R172 10K
R173 0
1V8_FB_SENSE
1V8_PS1_1V_FB
STUFF R145 FOR REMOTE SENSE
STUFF R146 FOR LOCAL SENSE
C121 0.1UF
C122 10UF
C747 22UF
1V8_AON
PEXVDD - PEX IOVDD/Q
U12
C115 1UF
PS_PEXVDD_EN
R169 0ohm
PEX_OVREG_PGOOD
C778 10UF
C788 4.7UF
C116 1000PF
R164 0
R166 3.16K
R167 10K
R168 0
PEX_FB_SENSE
PS1_1V_FB
C126 0.1UF
C129 10UF
C757 22UF
PEX_VDD
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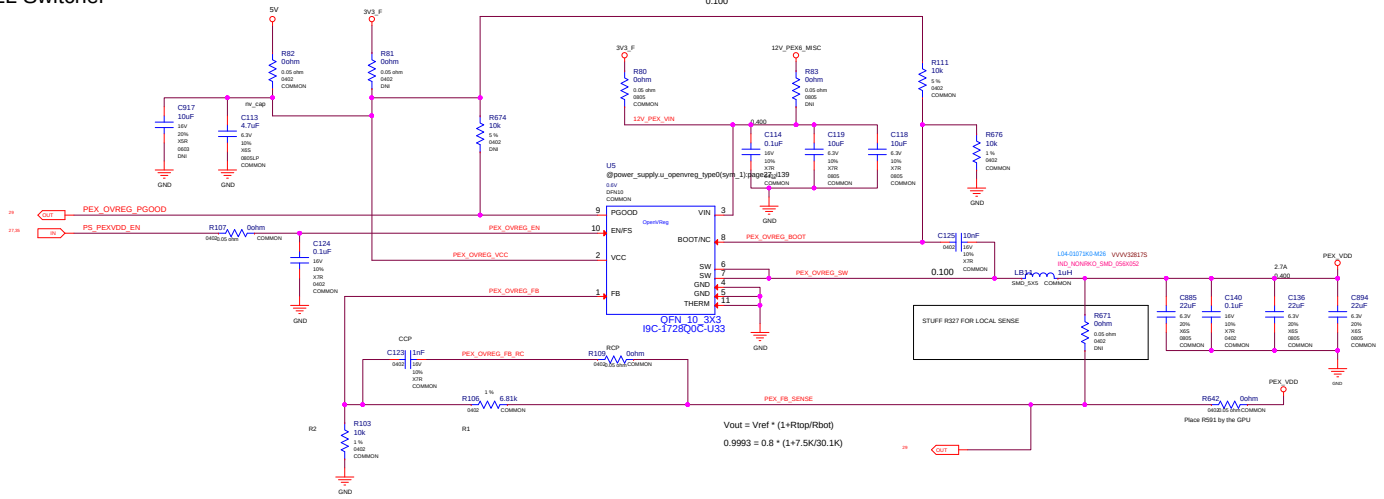
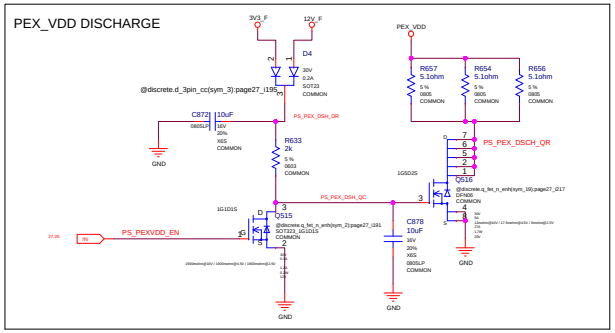
Page27: PS: 5V SWITCHER,PEX VDD

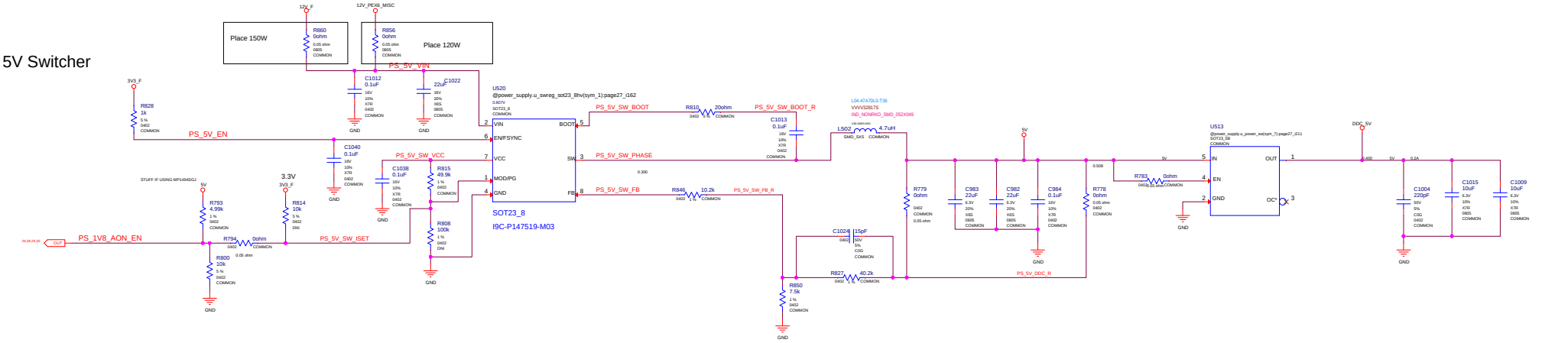
PEX PLL Switcher



PEX_VDD DISCHARGE



5V Switcher



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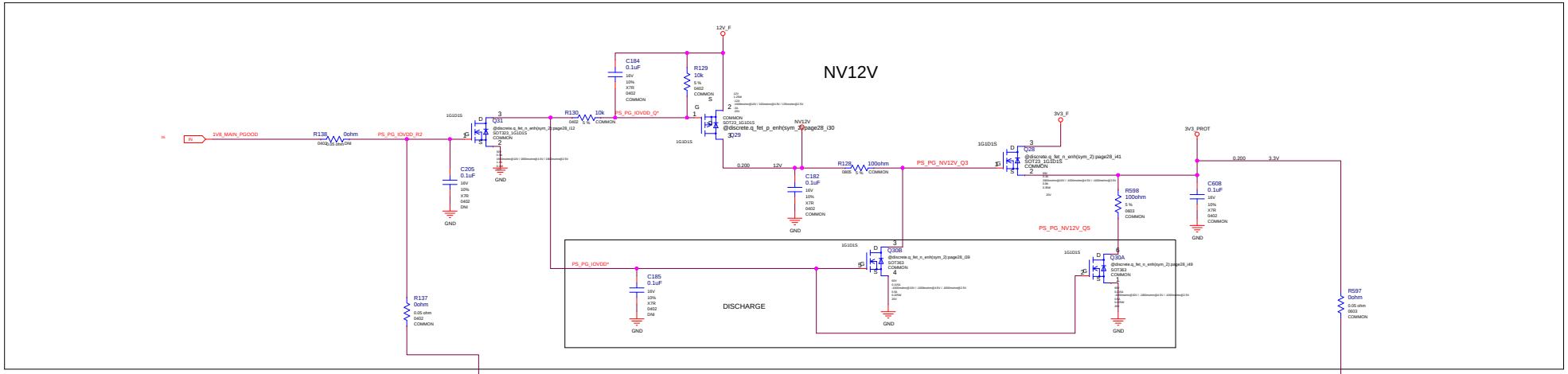

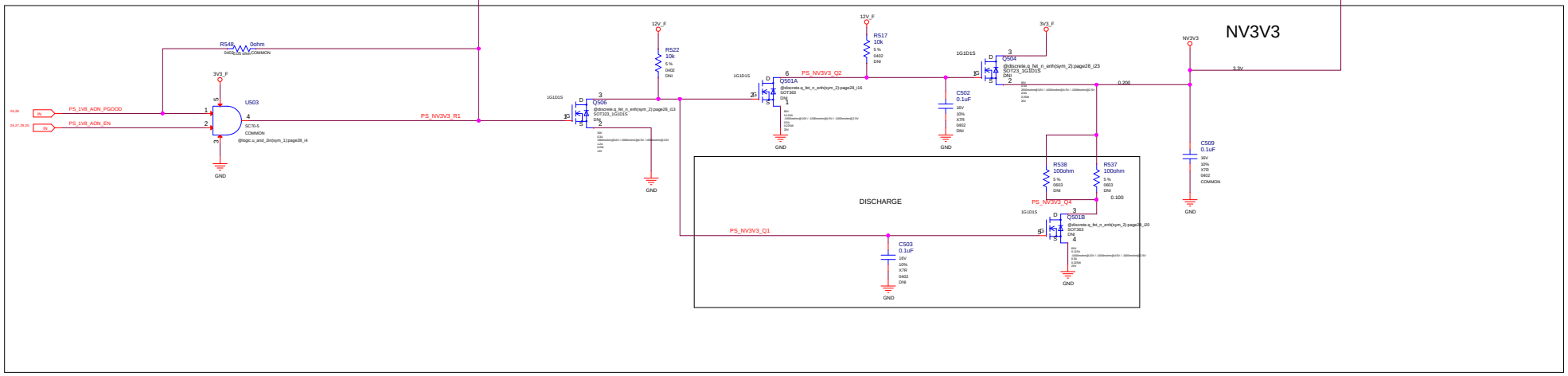

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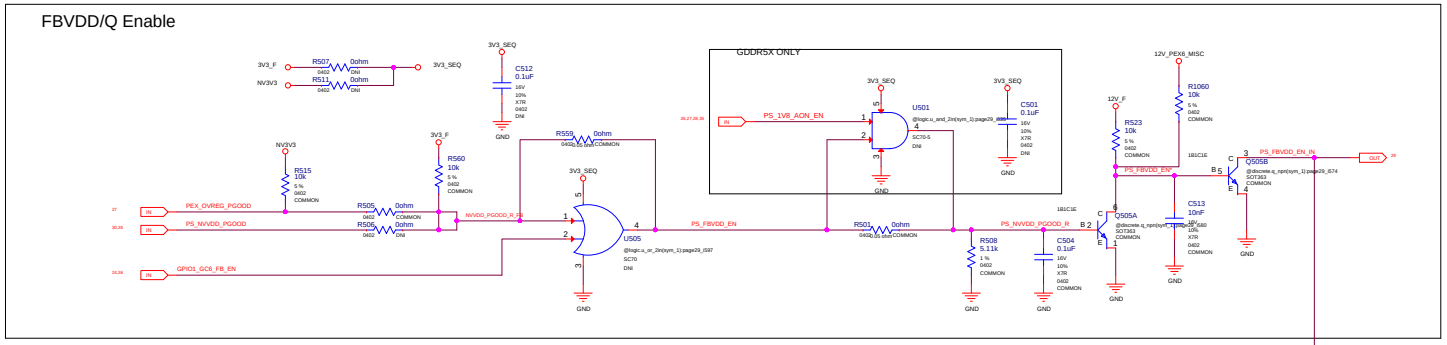
Page29: PS: FBVDDQ

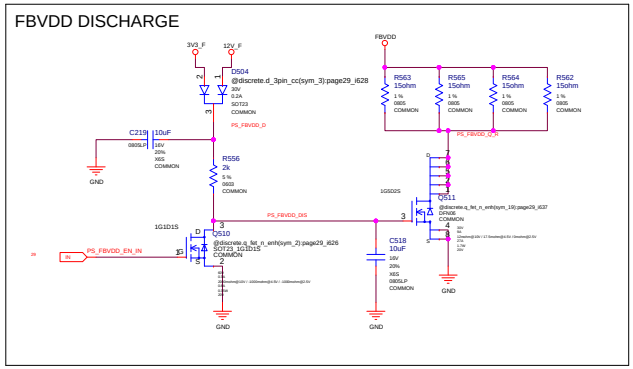
FBVDD

NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
FBVDD	FBVDD		

FBVDD/Q Enable

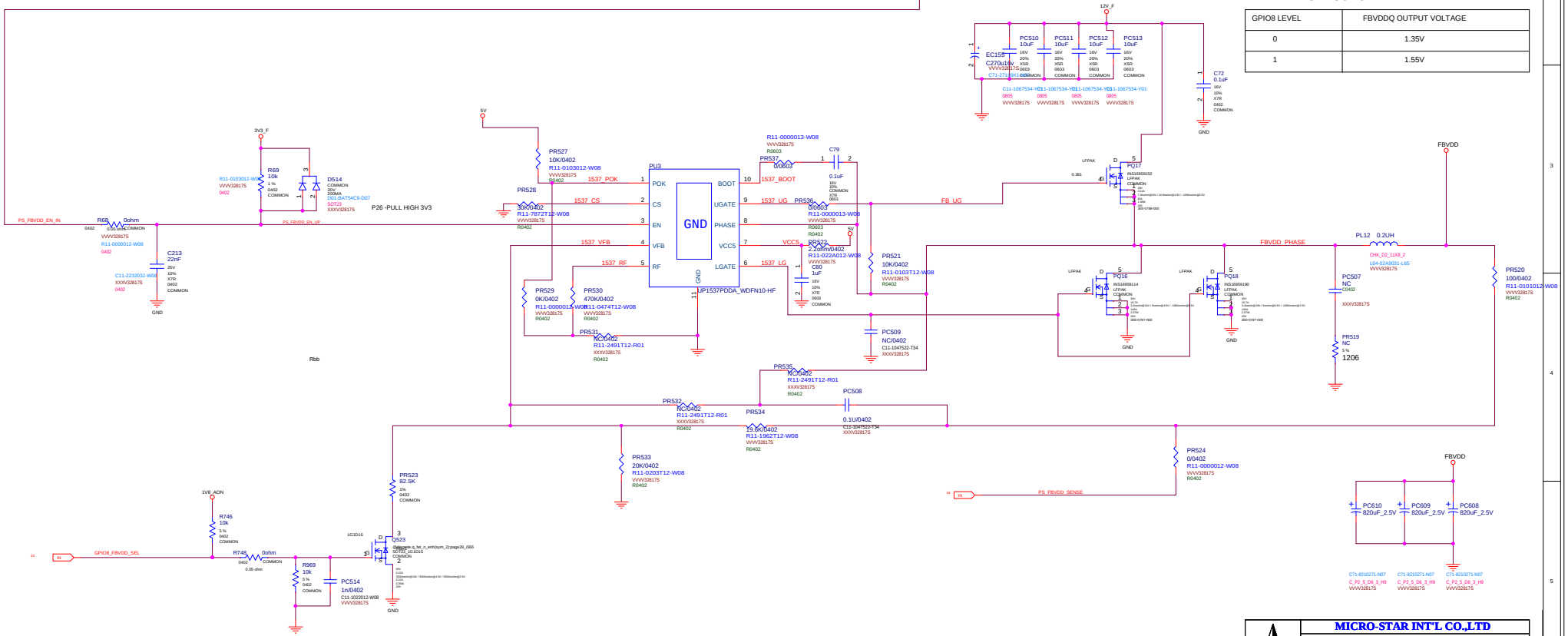


FBVDD DISCHARGE



SAMSUNG

GPIO8 LEVEL	FBVDDQ OUTPUT VOLTAGE
0	1.35V
1	1.55V



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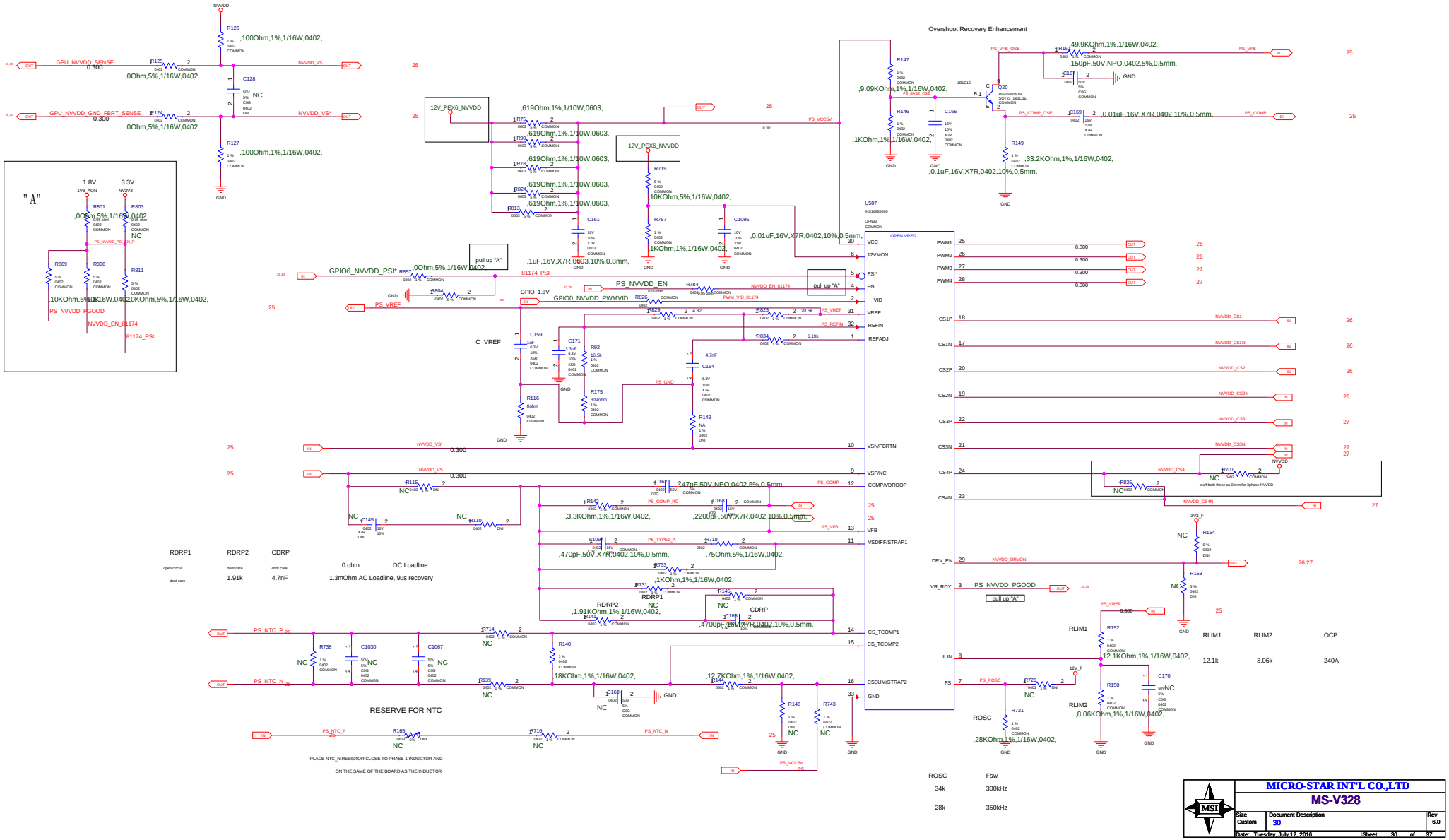
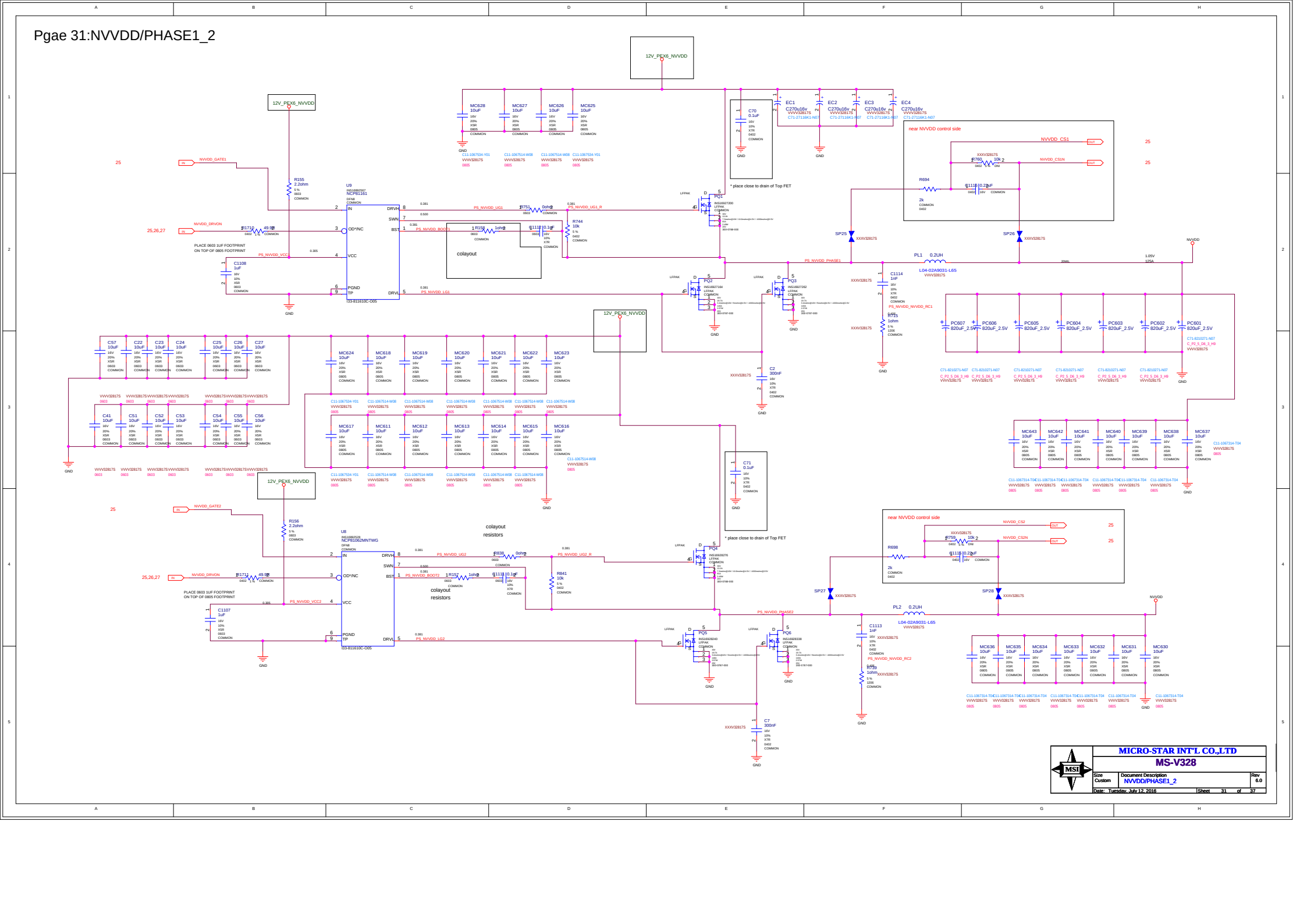
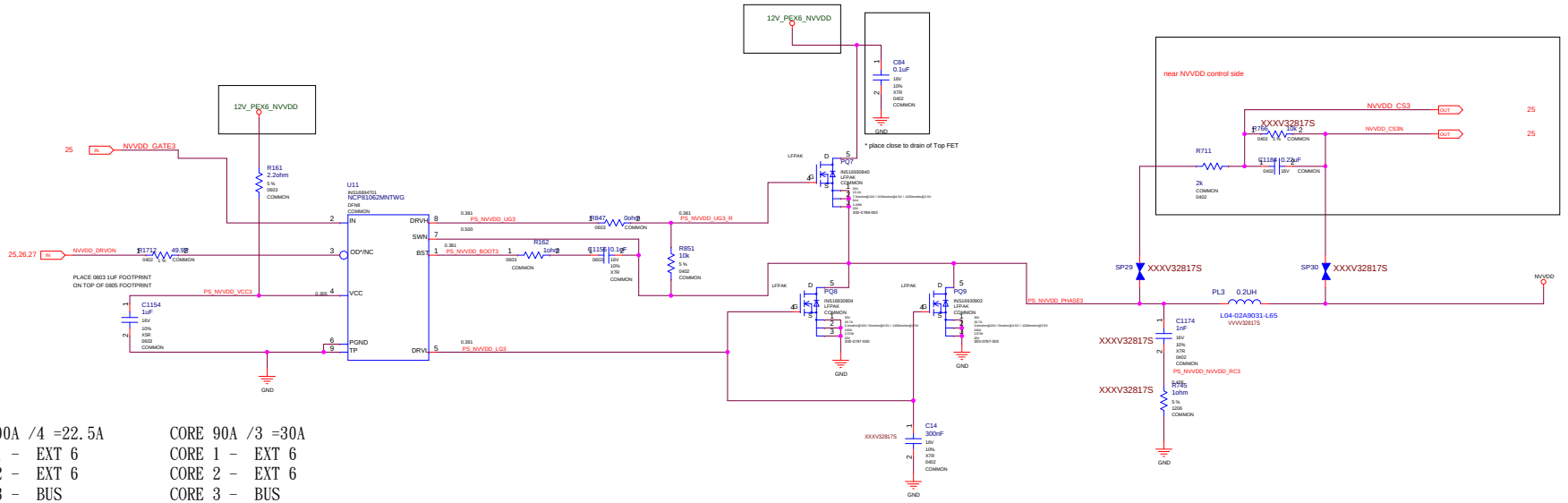
Page30: PS: NVVDD Controller



Pgae 31:NVVDD/PHASE1_2

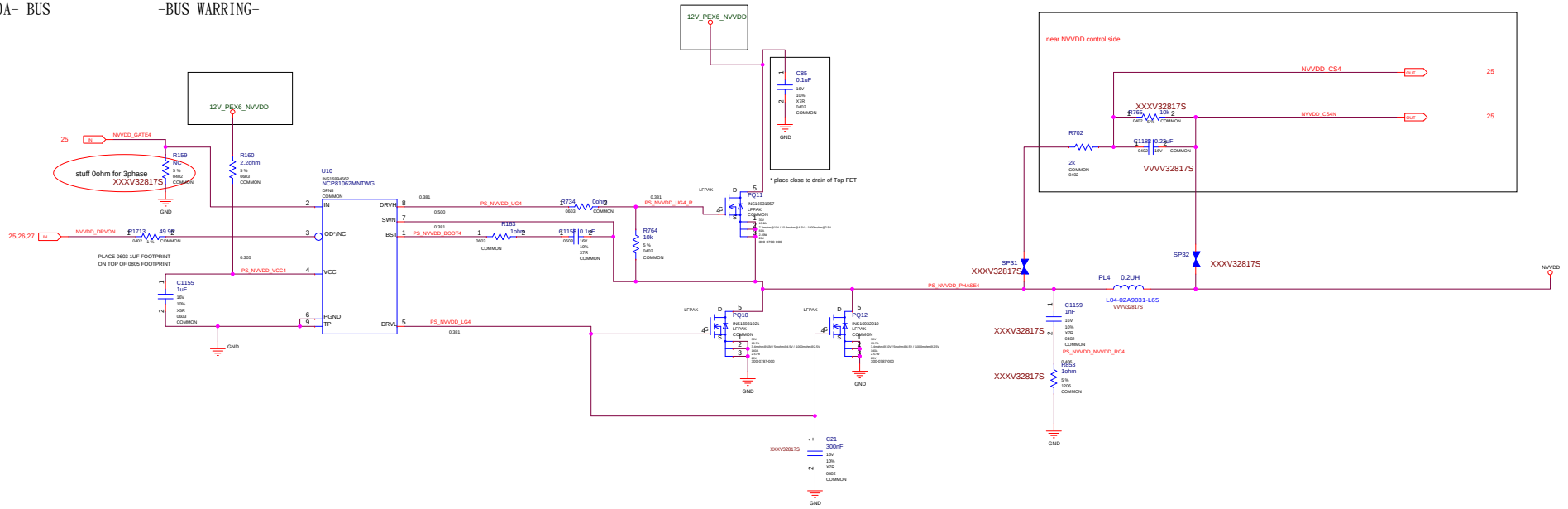


Page32: PS: NVVDD PHASE 3/4



CORE 90A /4 =22.5A
CORE 1 - EXT 6
CORE 2 - EXT 6
CORE 3 - BUS
CORE 4 - EXT 6
MEM 30A- BUS

CORE 90A /3 =30A
CORE 1 - EXT 6
CORE 2 - EXT 6
CORE 3 - BUS
MEM 30A- BUS
-BUS WARRING-



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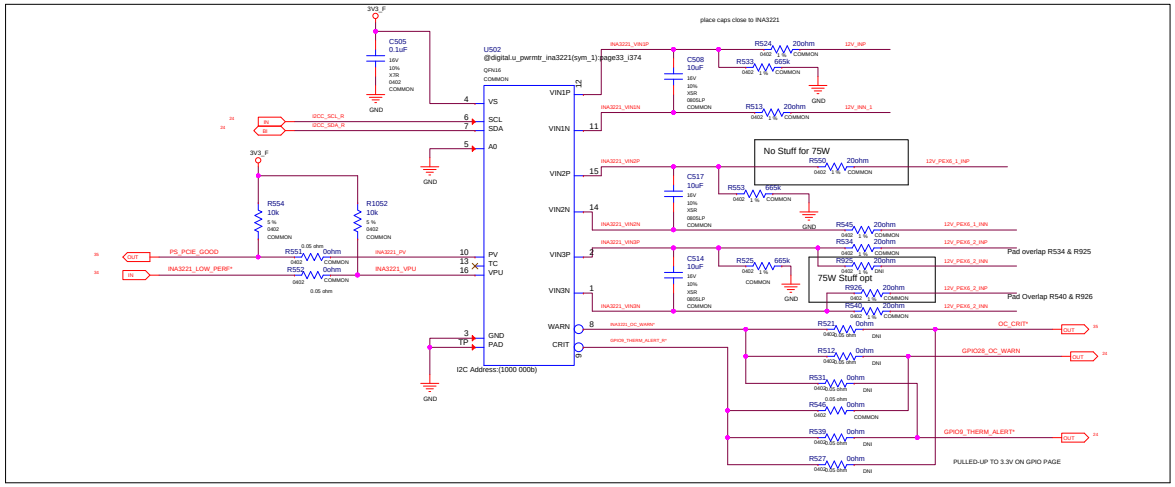
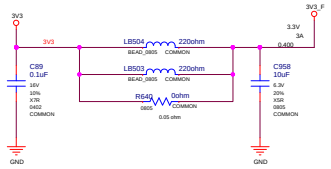
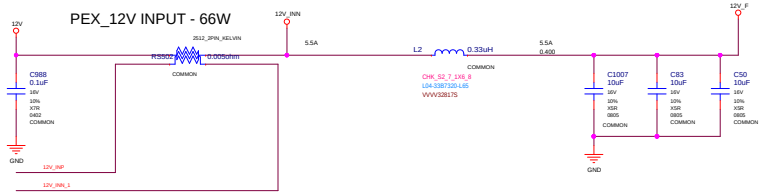
Page33: PS: Inputs, Filtering, and Monitoring



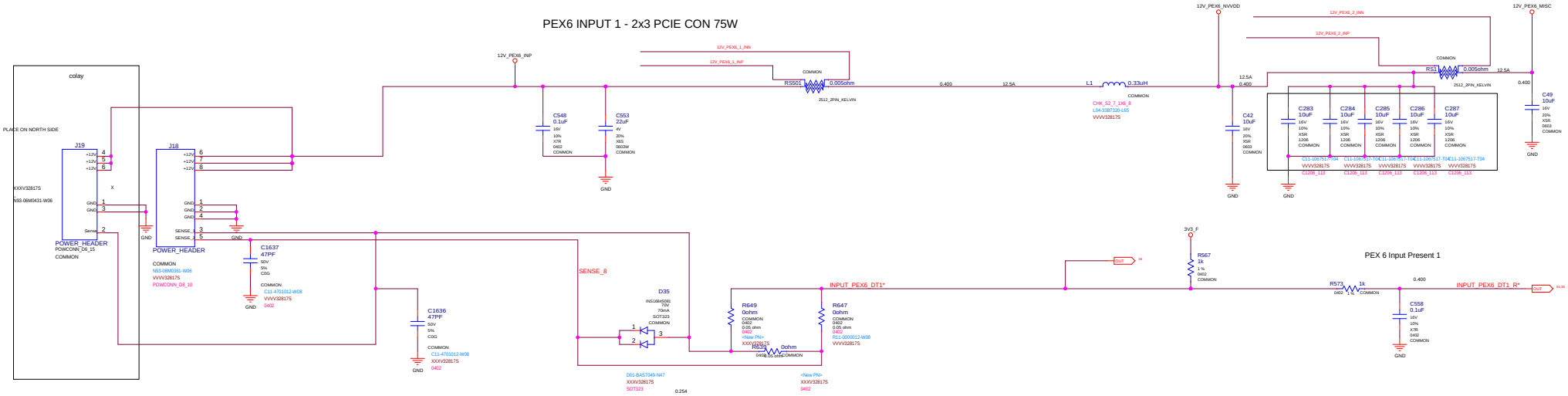
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



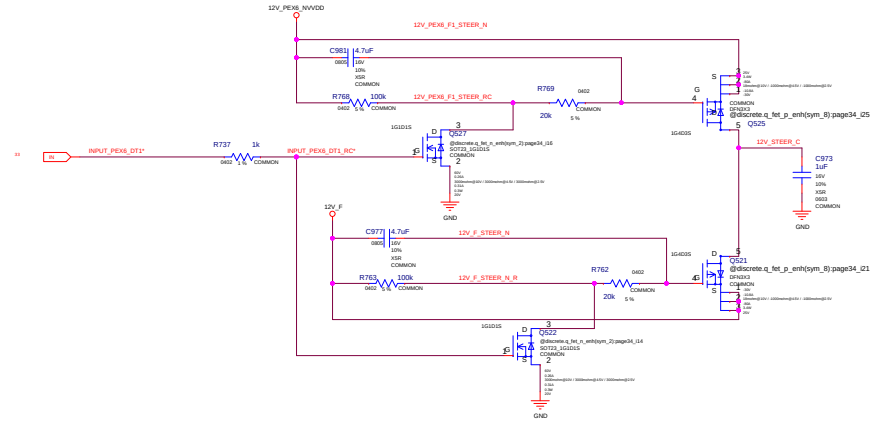
PEX6 INPUT 1 - 2x3 PCIE CON 75W



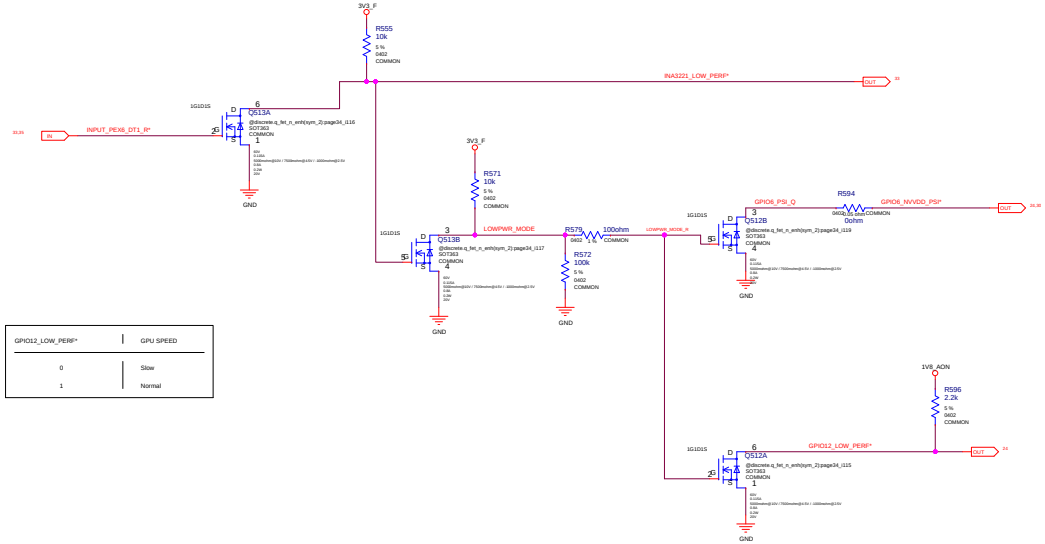
Page34: PS: 12V Current Steering, PSI Control, and LED

12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA



PEX Input - Power Level/PSI* Control



GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

GeForce Logo LED

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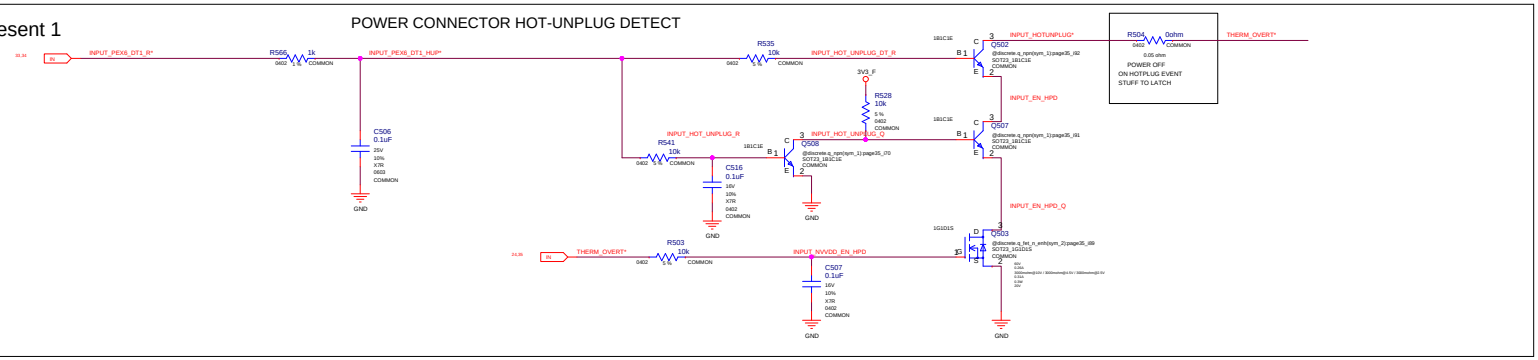
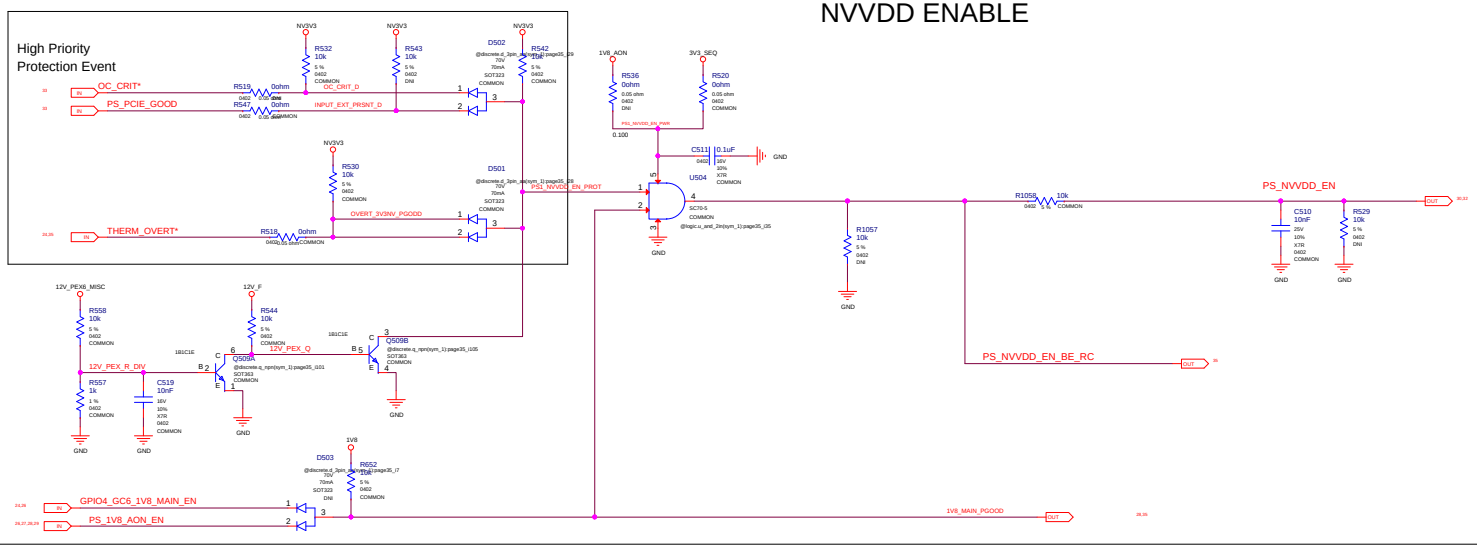
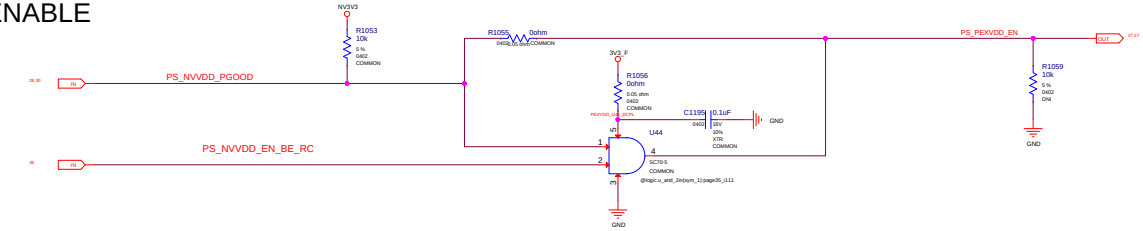
PEX Input Present 1



NVVDD ENABLE



PEX ENABLE



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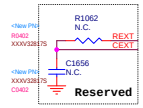
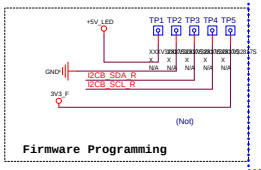
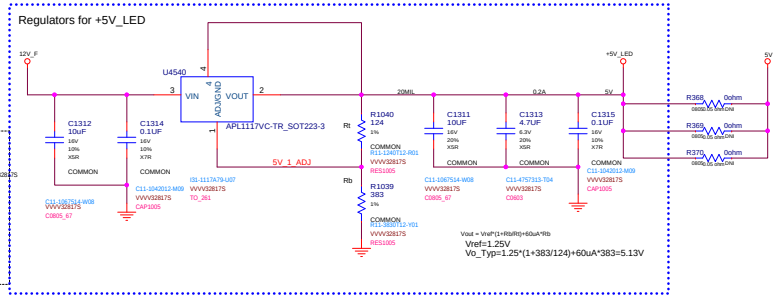
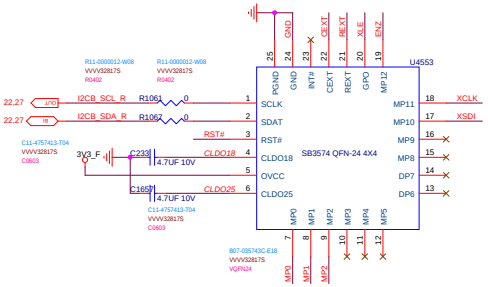
Page38: LED

remove GC6 FB ENABLE
remove GPU_EVENT*
remove PEX_CLKREQ*
PEX_RST# LOGIC

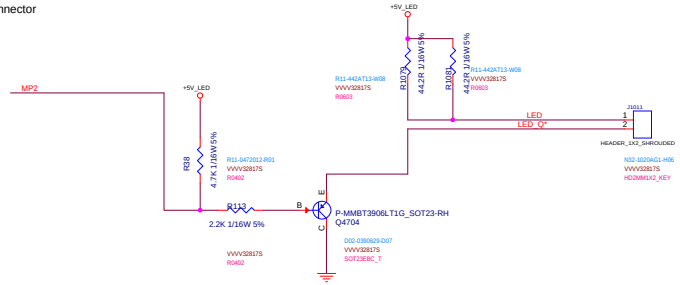


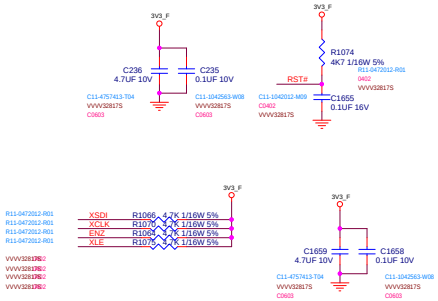


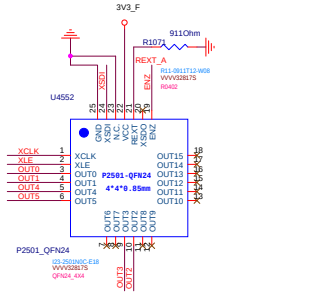


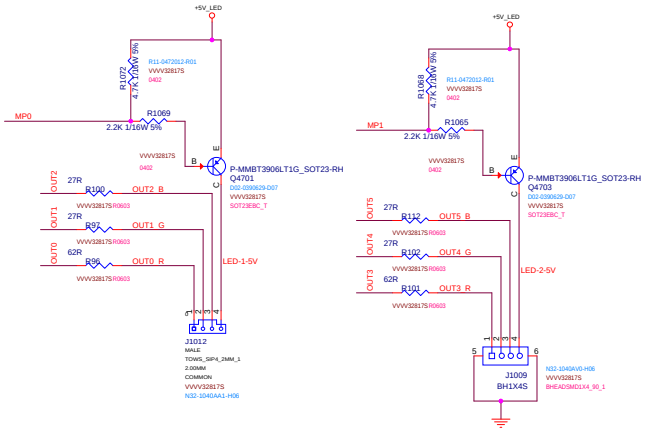


LED Connector









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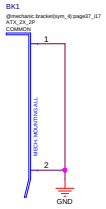
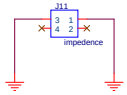
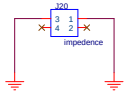
Page40: MECH

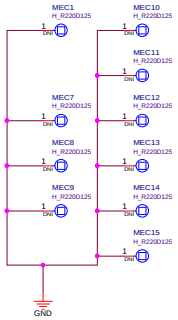
Brackets:



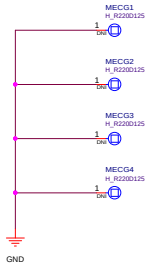


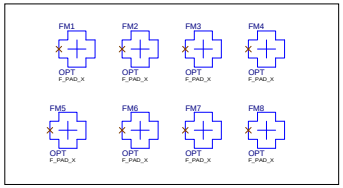


Mechanical Holes Symbol



GPU Stiffner





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