PG410 A01

GP106 8GB/4GB GDDR5, 256b, 256Mx32/128MX32
Tall DVI-D + DP + DP + HDMI/DP + DP

TABLE OF CONTENTS

6.1
1.修改 NVVDD_VR電路
2.修改 LED電路
3.增加 COLAY電路
4.修HDMI DP COLAY

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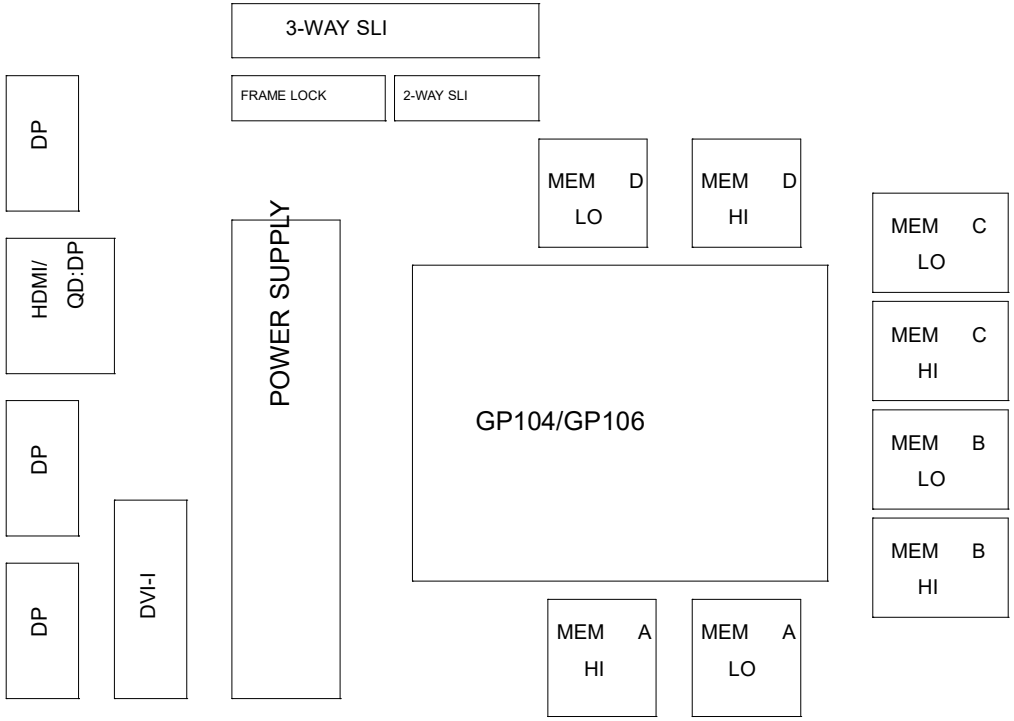
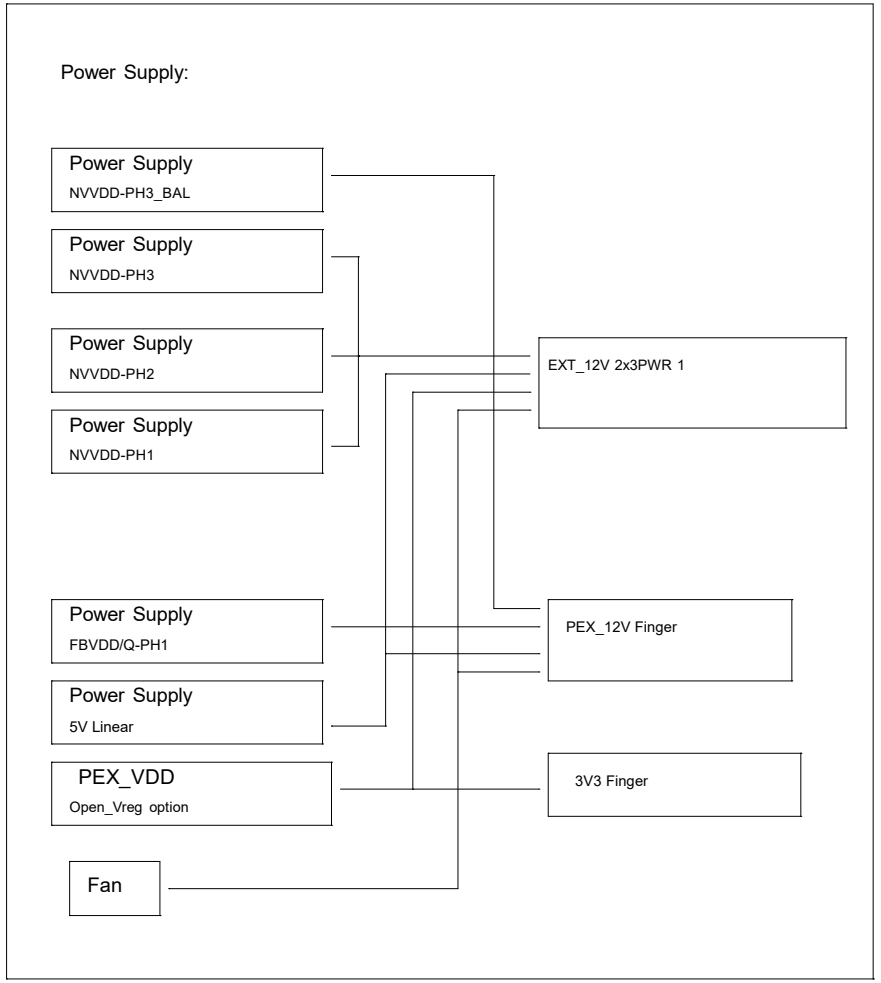
Page2: Block Diagram





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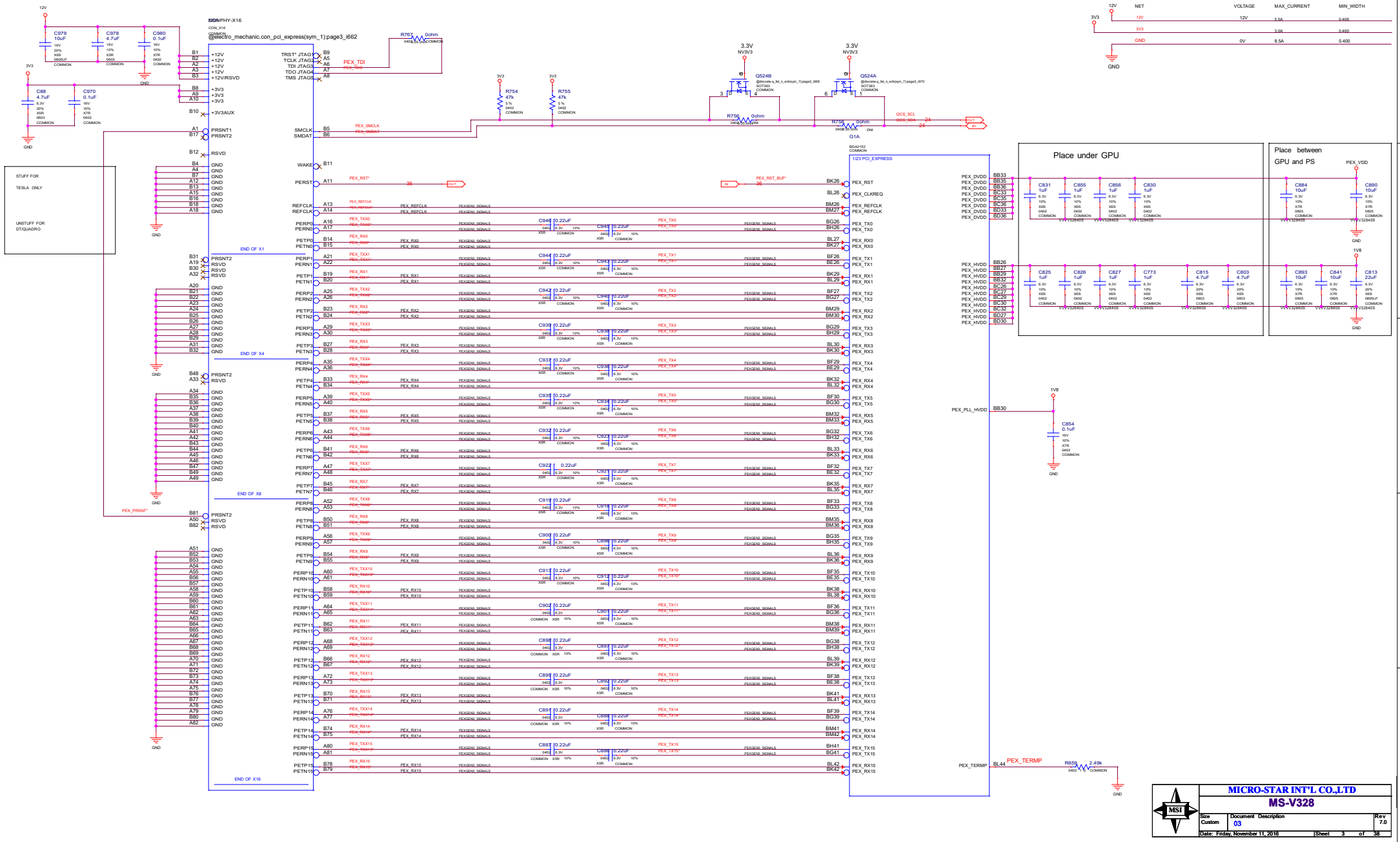
Page3: PCI Express



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Page4: MEMORY: GPU Partition A/B

GDDR5 CMD Mapping

CMD	0_31	32_63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

G1B

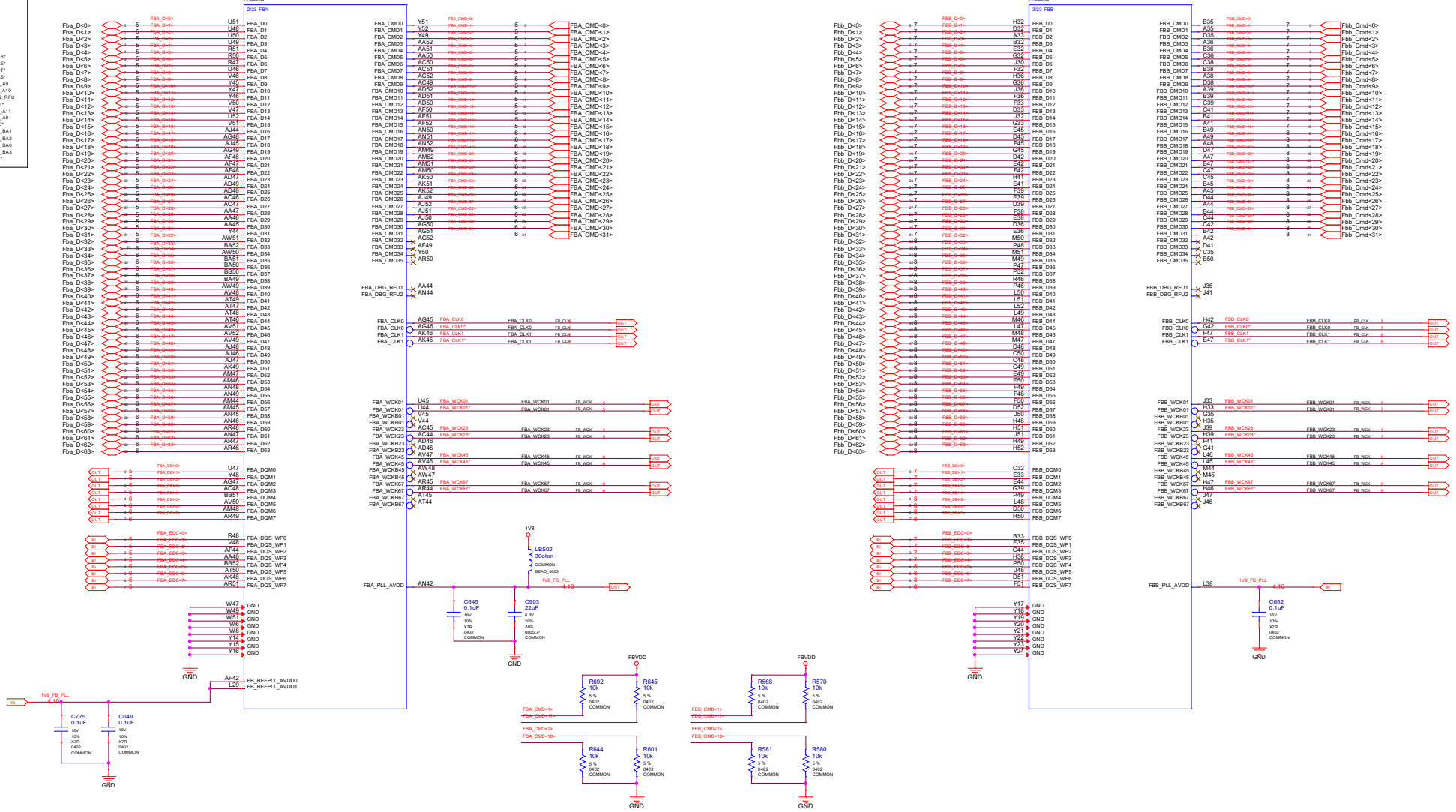
BGA2152
COMMON

2/23 FBA

G1C

BGA2152
COMMON

3/23 FBB



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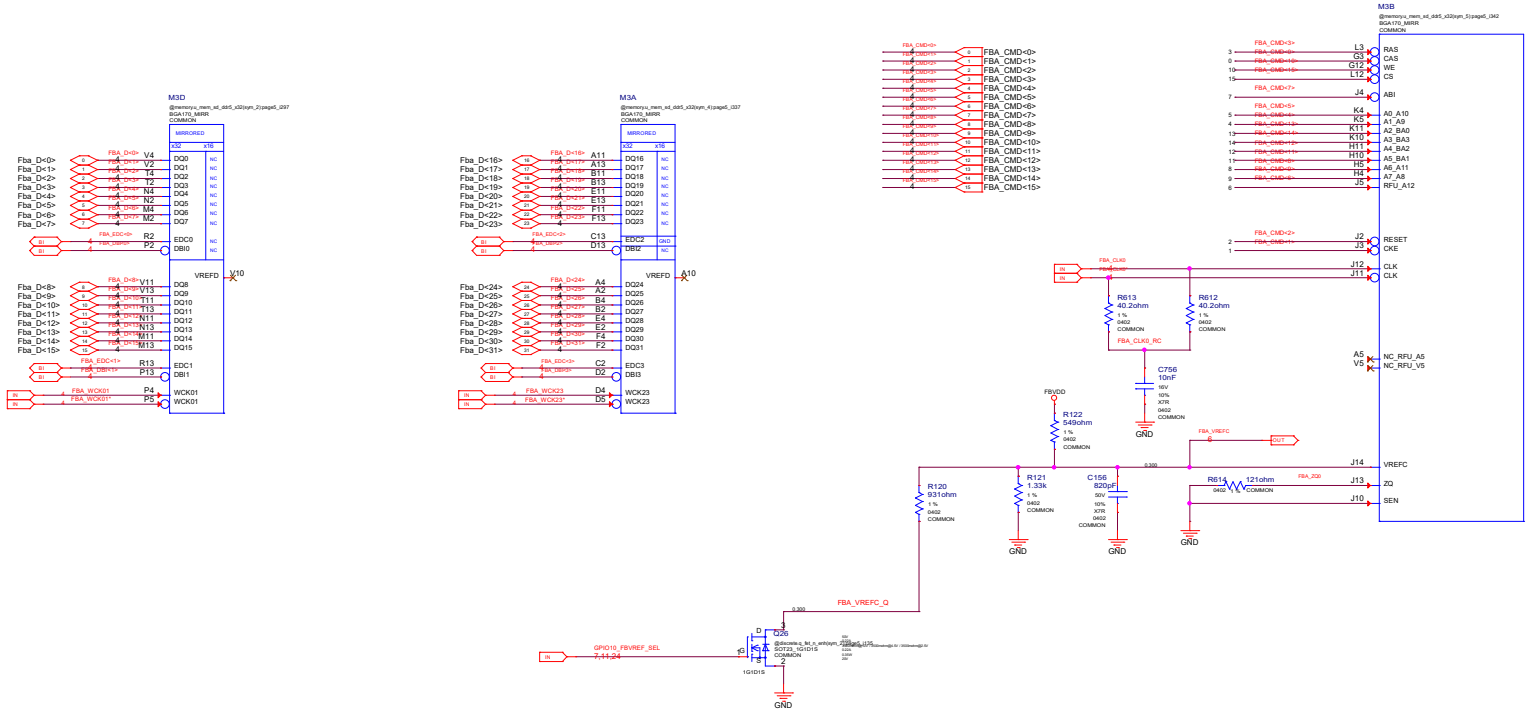
Page5: FRAME BUFFER PARTITION A [31:0]



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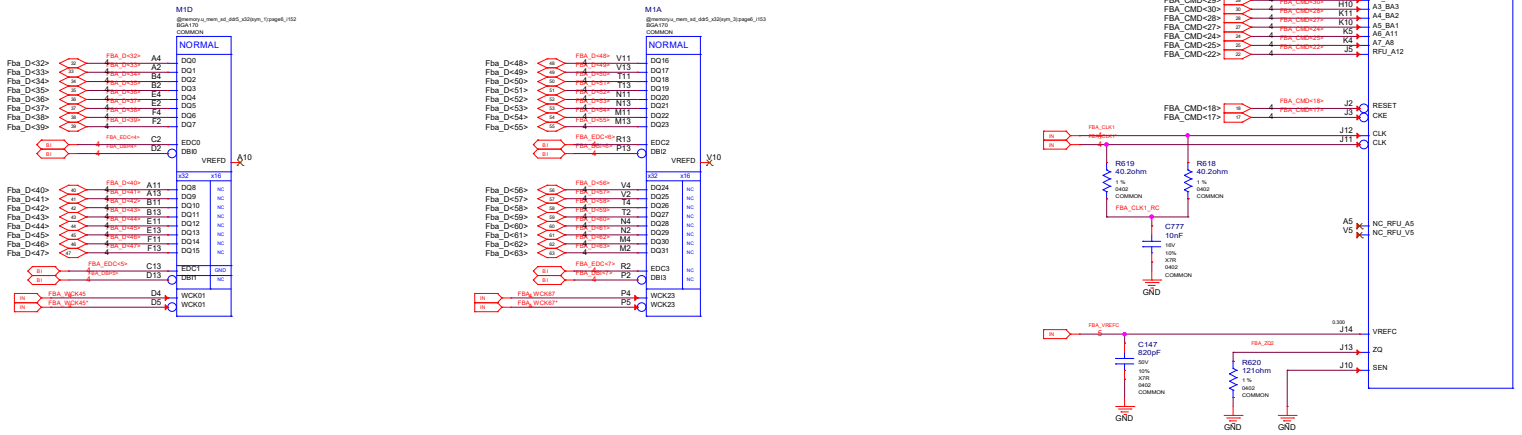
Page6: FRAME BUFFER PARTITION A [63:32]



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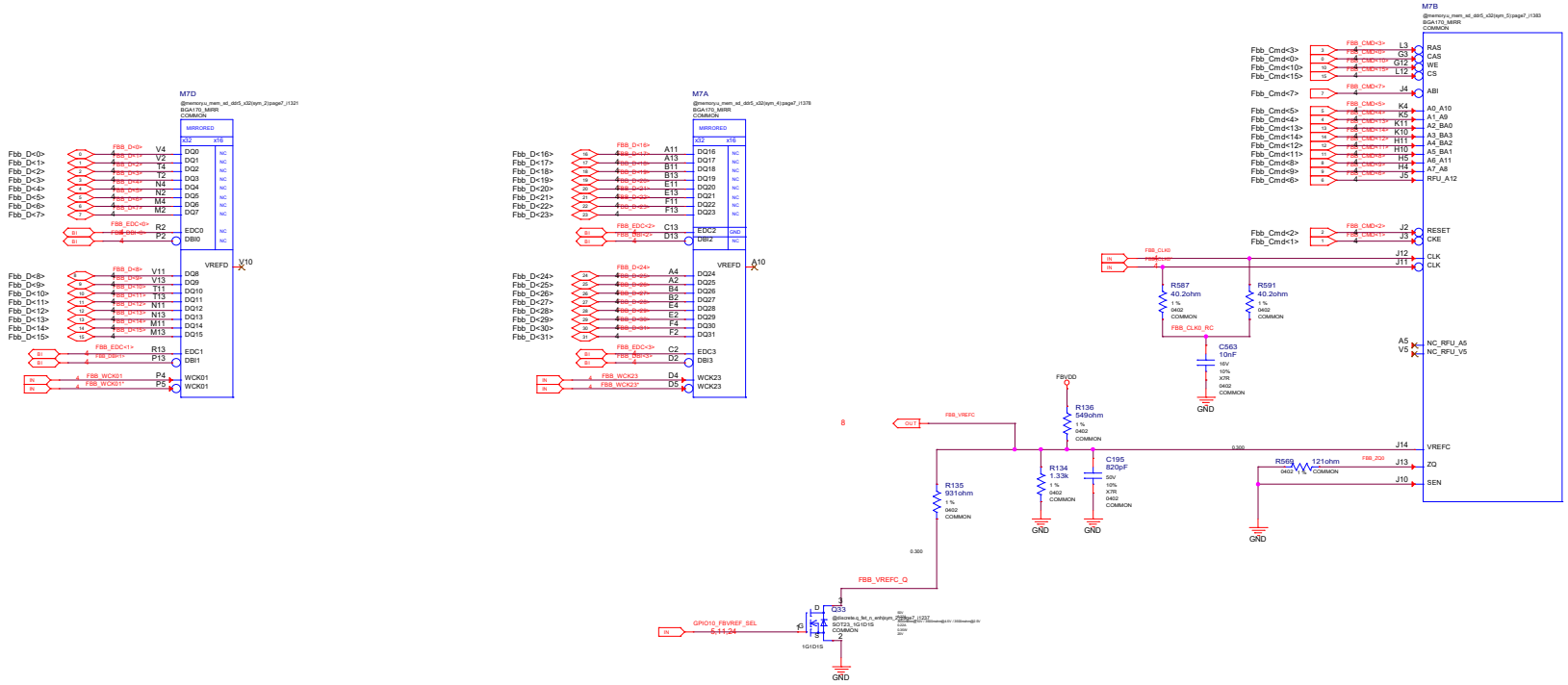
Page7: FRAME BUFFER PARTITION B [31:0]



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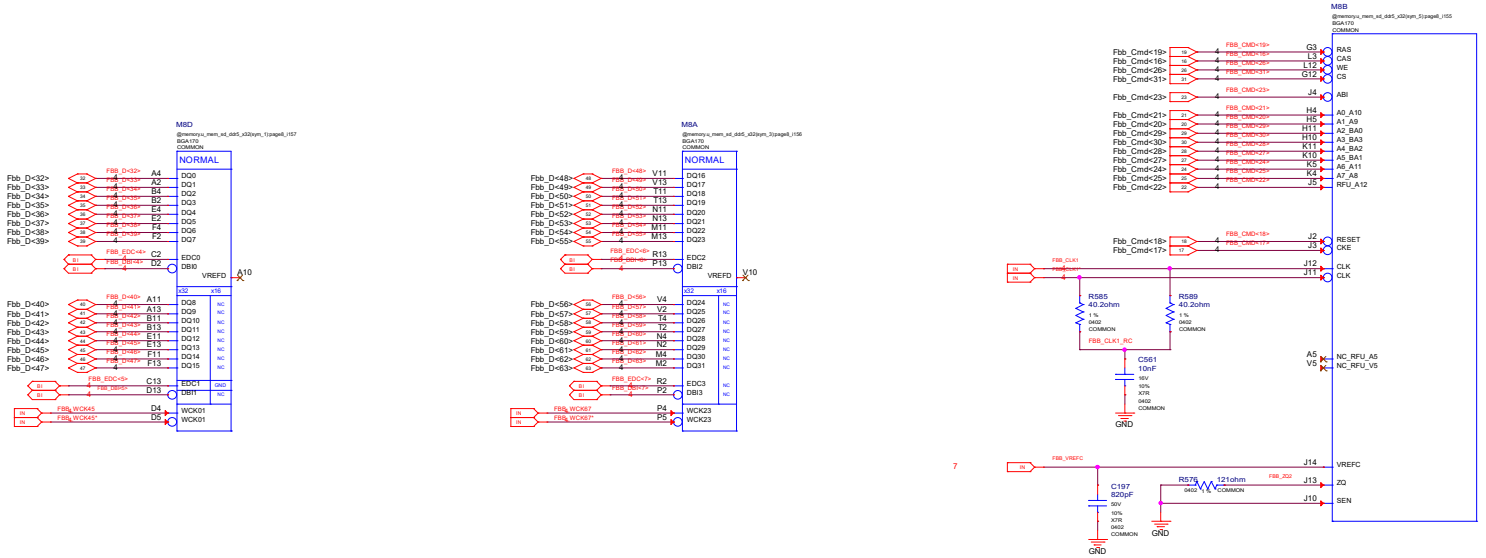
Page8: FRAME BUFFER PARTITION B [63:32]



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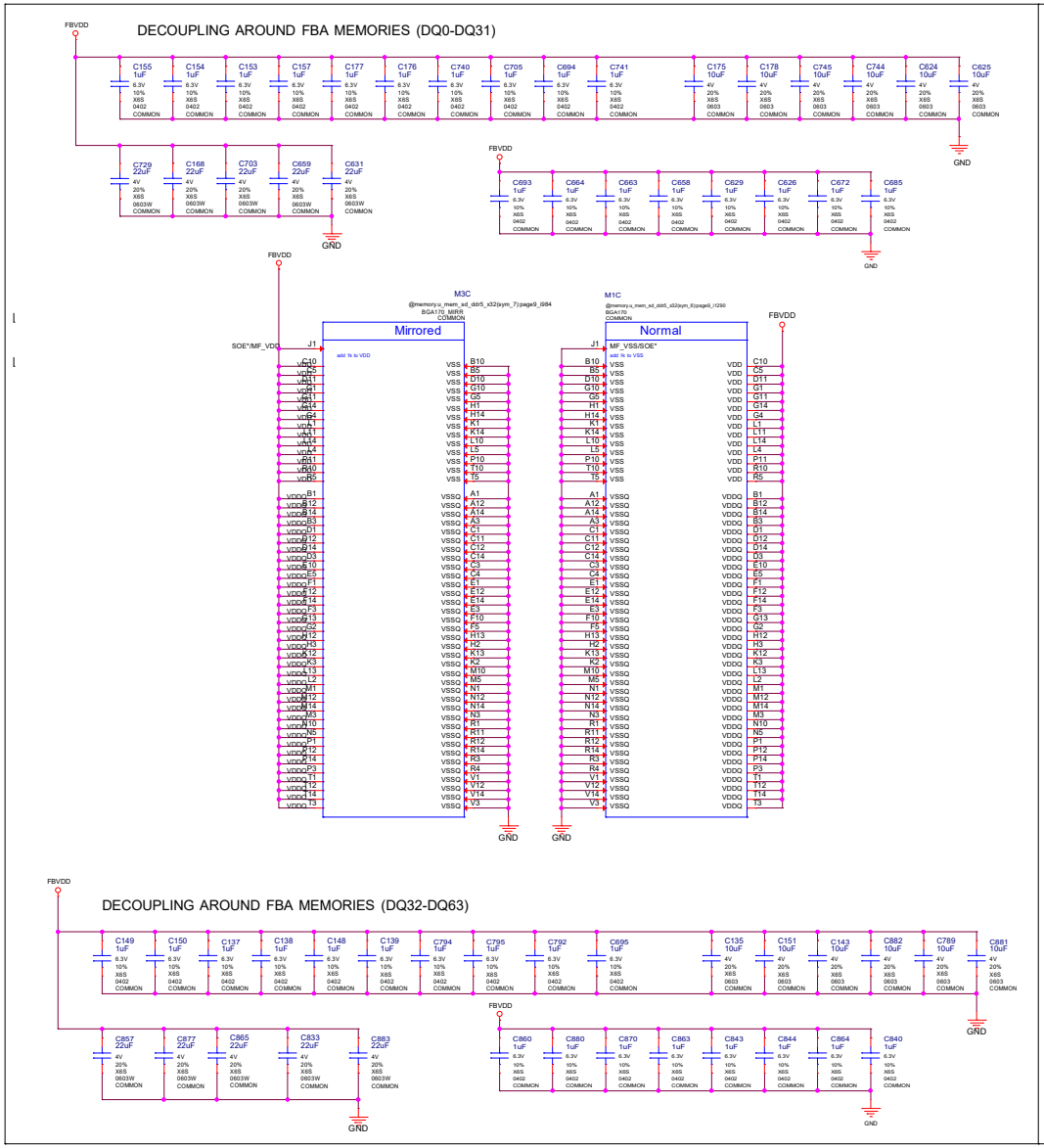
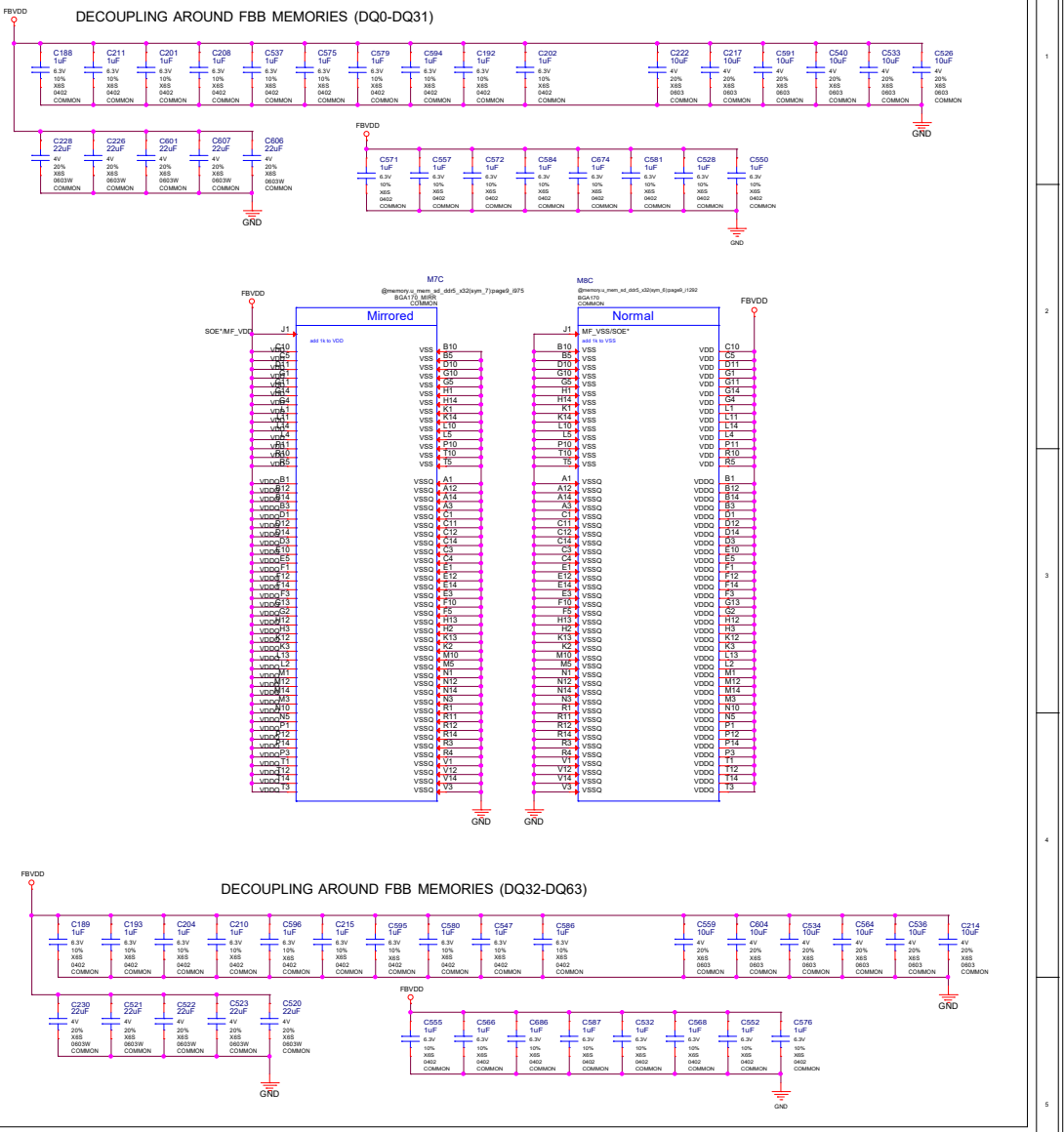
Page9: FRAME BUFFER PARTITION A/B DECOUPLING





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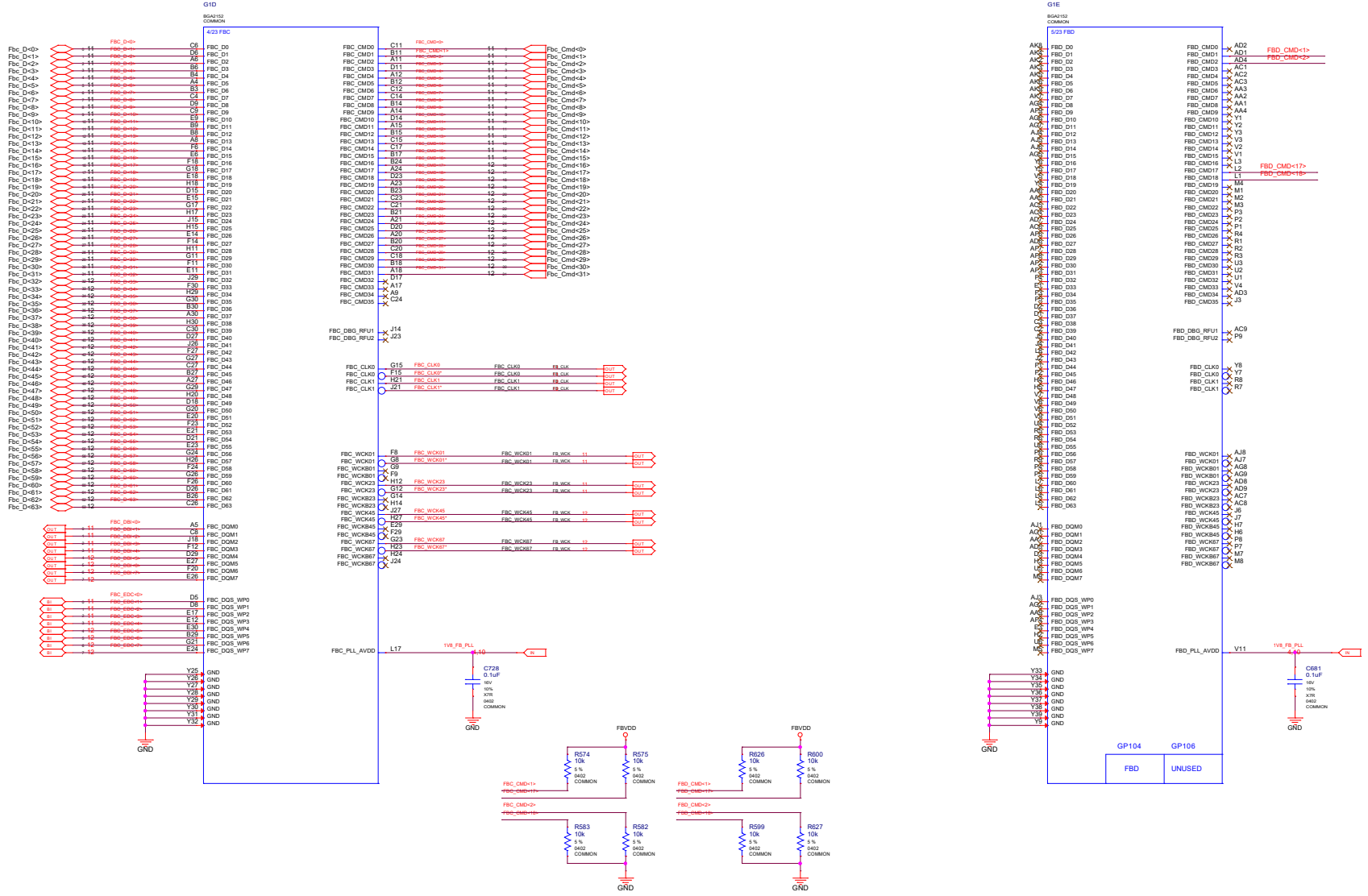
Page10: MEMORY: GPU Partition C/D

GDDR5 CMD Mapping		
CMD	0_31	32_63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*



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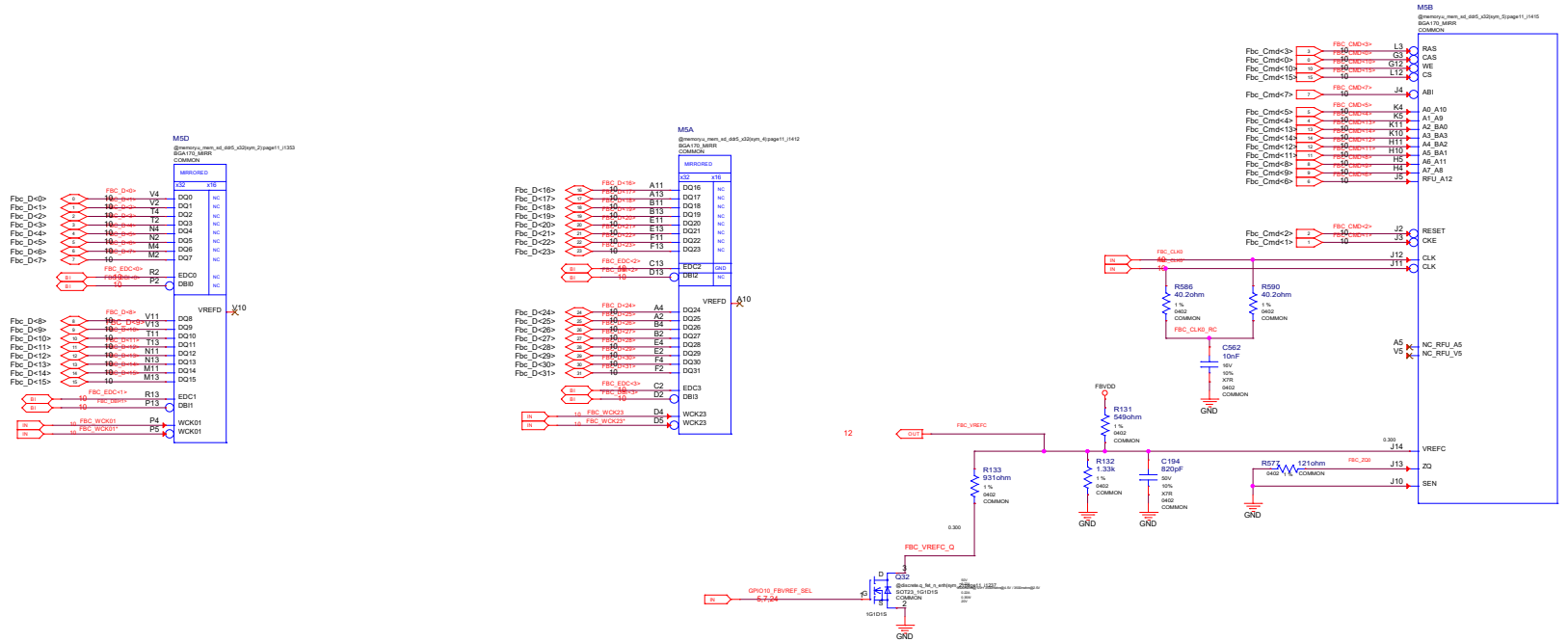
Page11: Frame Buffer Partition C [31:0]



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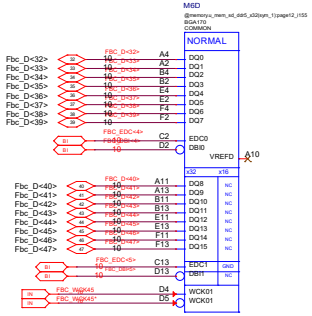
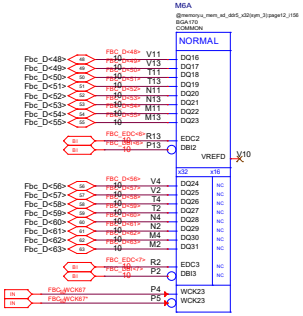
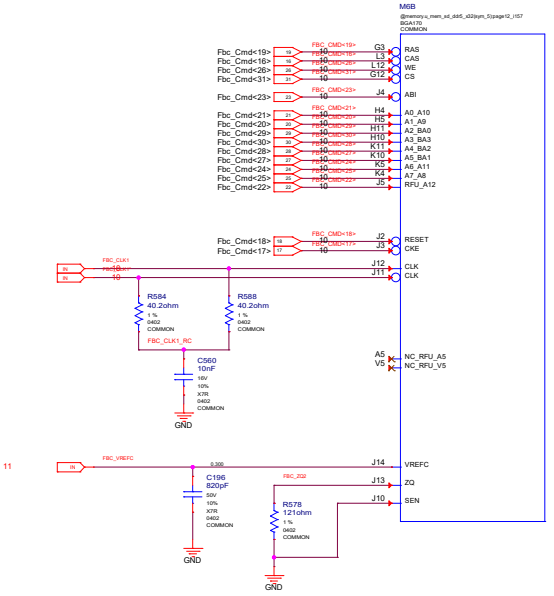
Page12: FRAME BUFFER PARTITION C [63:32]







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Page13: FRAME BUFFER PARTITION D[31:0]

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Page14: FRAME BUFFER PARTITION D[63:32]

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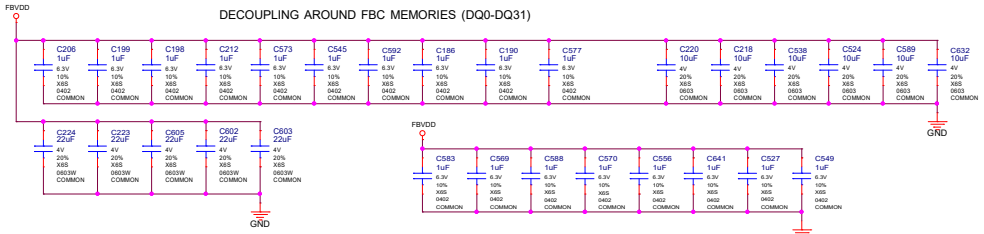
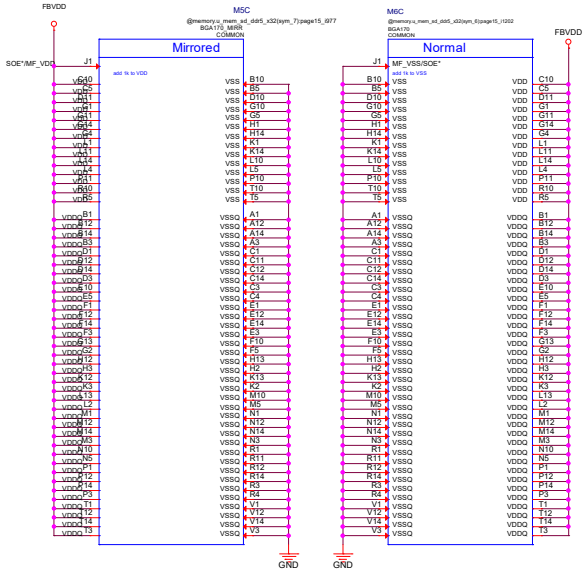
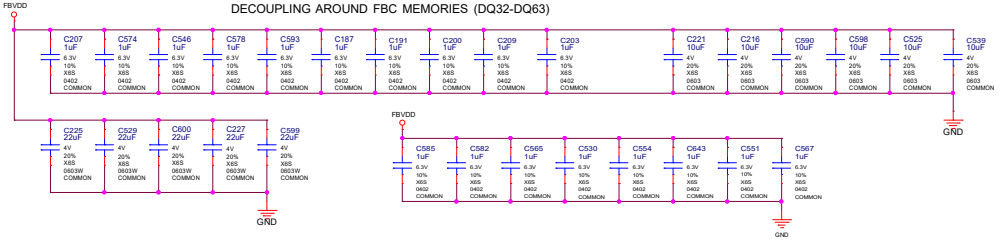
Page15: FRAME BUFFER PARTITION C/D DECOUPLING







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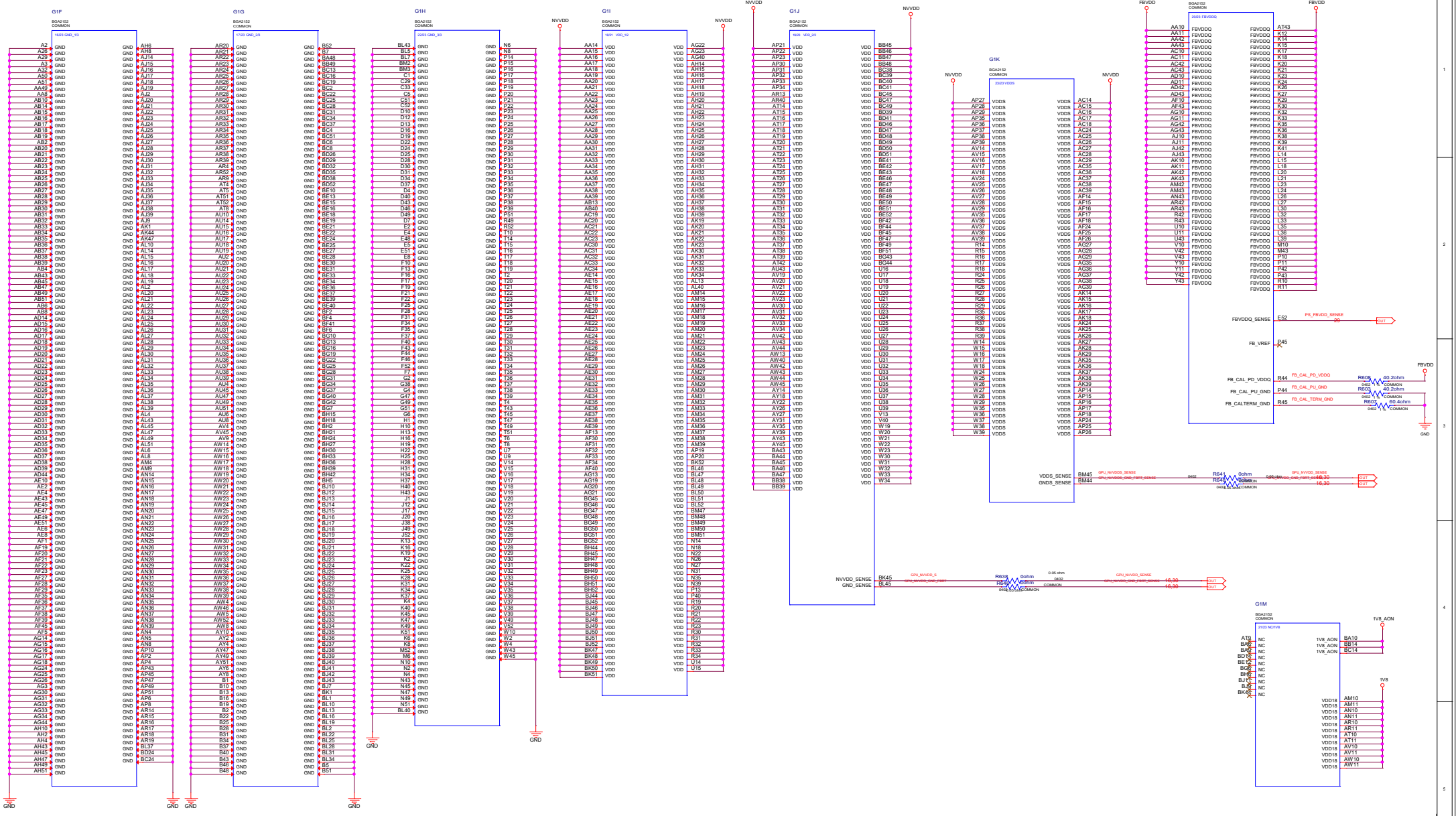
Page16: GPU PWR and GND



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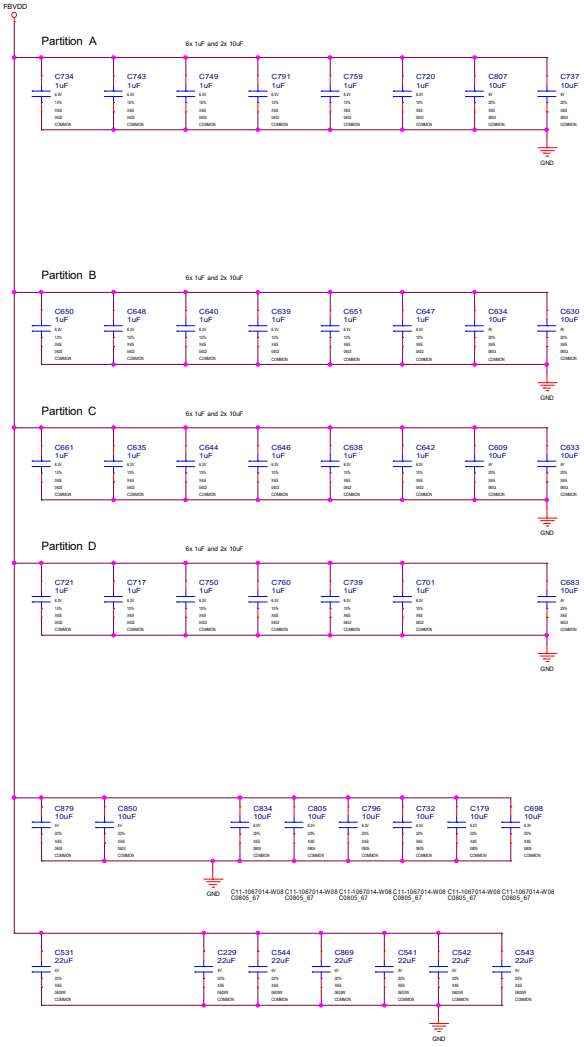
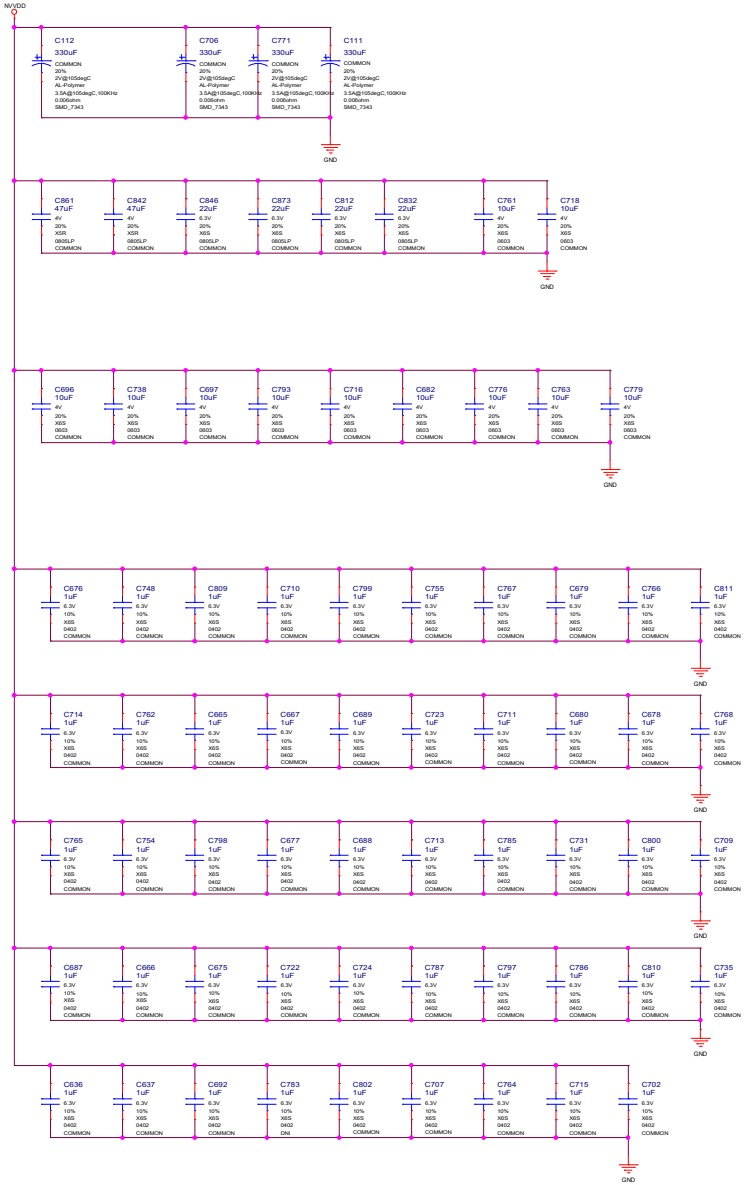
Page17: GPU Decoupling

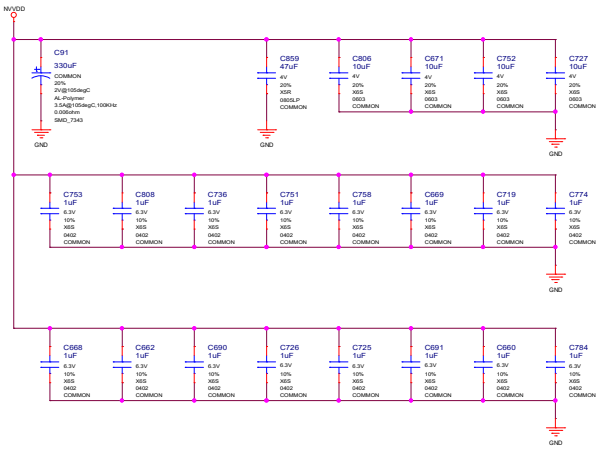
FBVDD



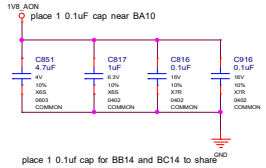
NVVDD



NVVDD

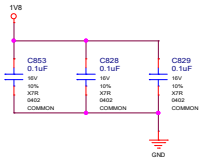


1V8_AON



place 1 0.1uf cap for BB14 and BC14 to share

1V8_MAIN



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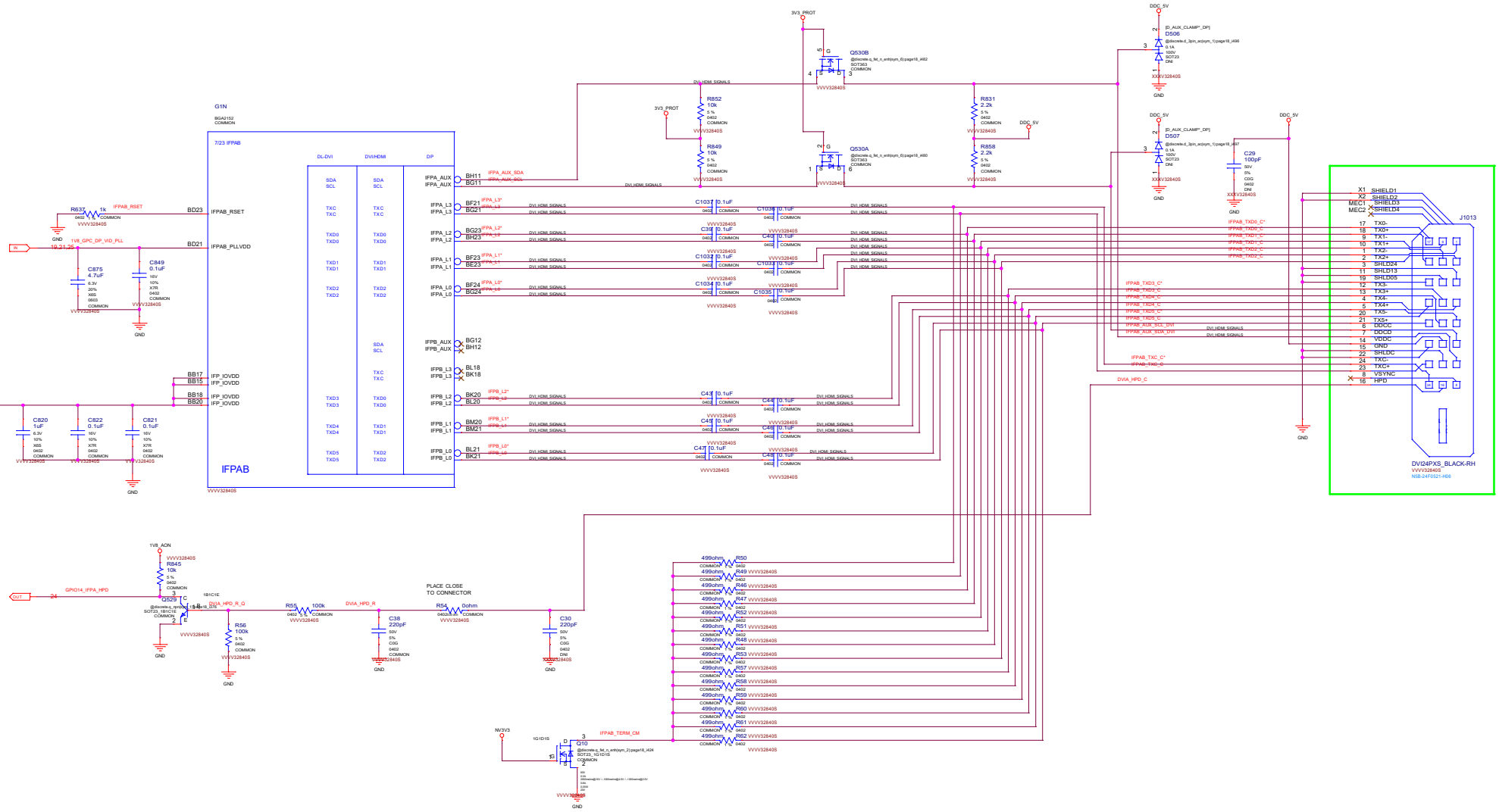
Page18: IFPAB DVI-D-DL



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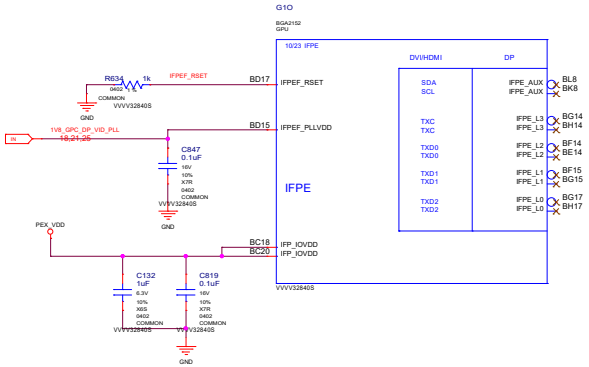
Page19: IFPE DP



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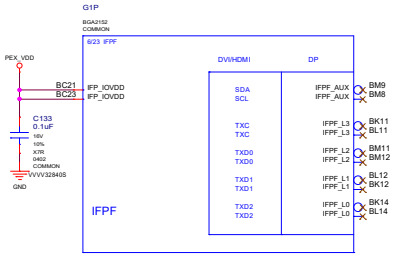
Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



Remove DP J4

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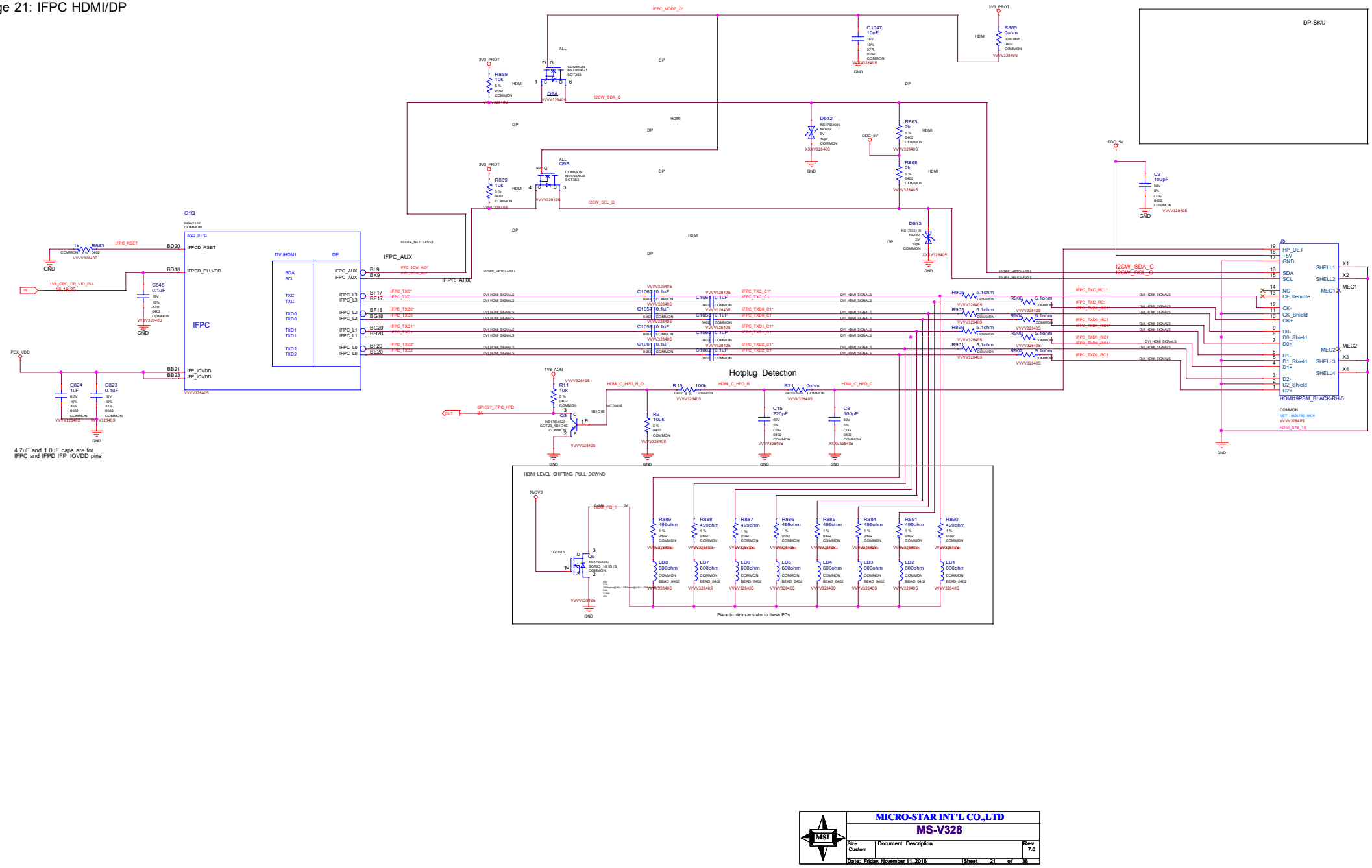
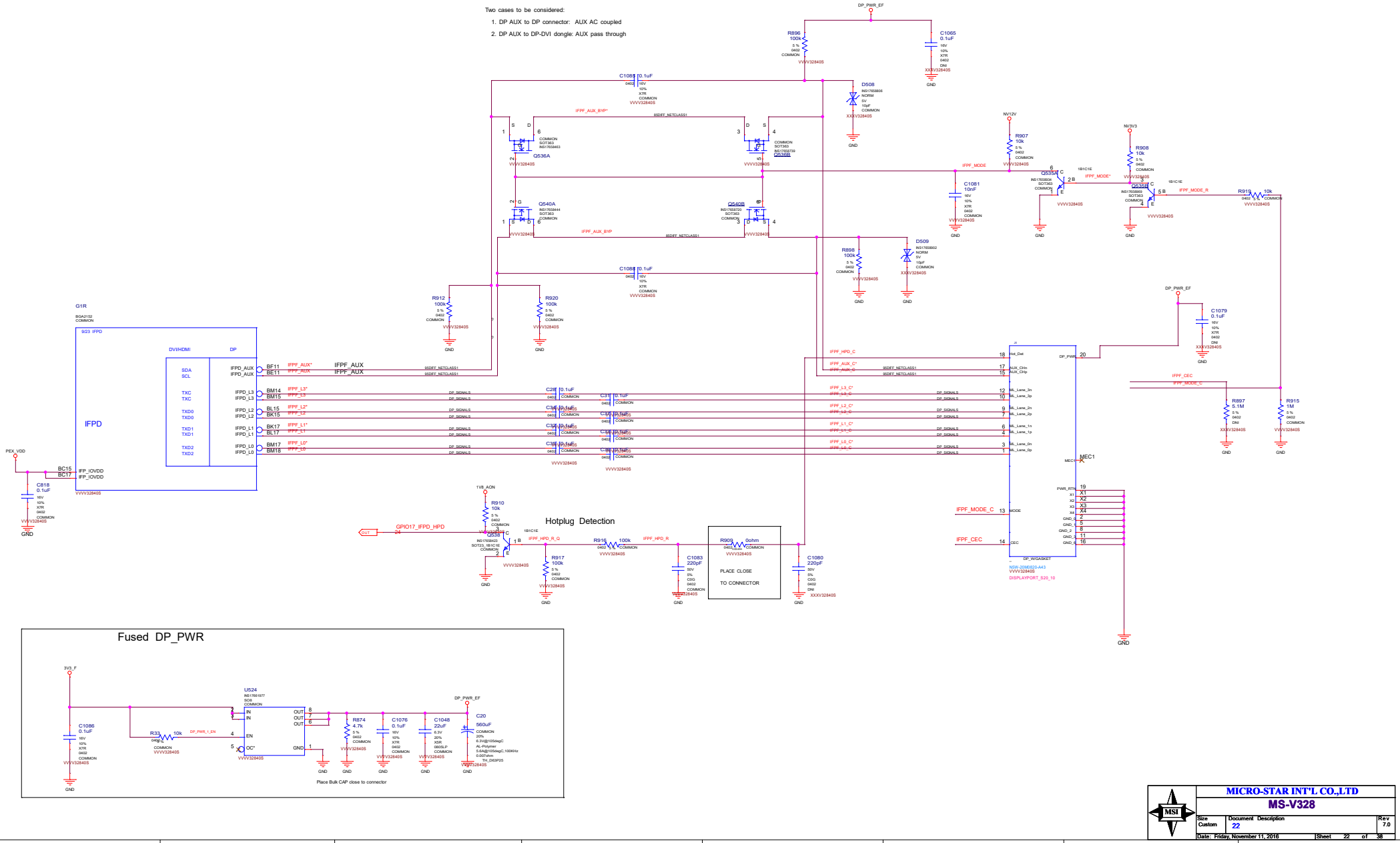
Page 21: IFPC HDMI/DP



Page 22: IFPD DP



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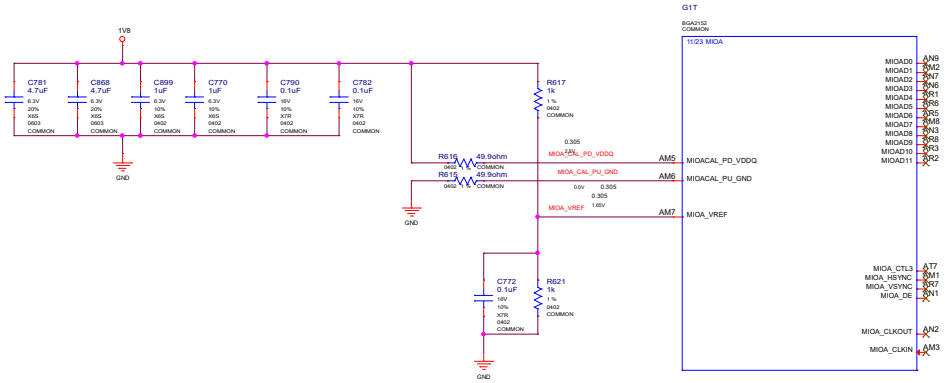
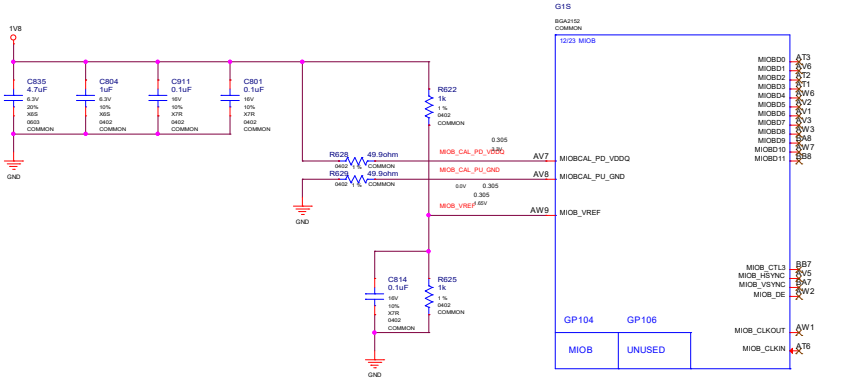
Page 23: MIOA/B Interface and Frame Lock



Pad Overlap R1042 & R1043



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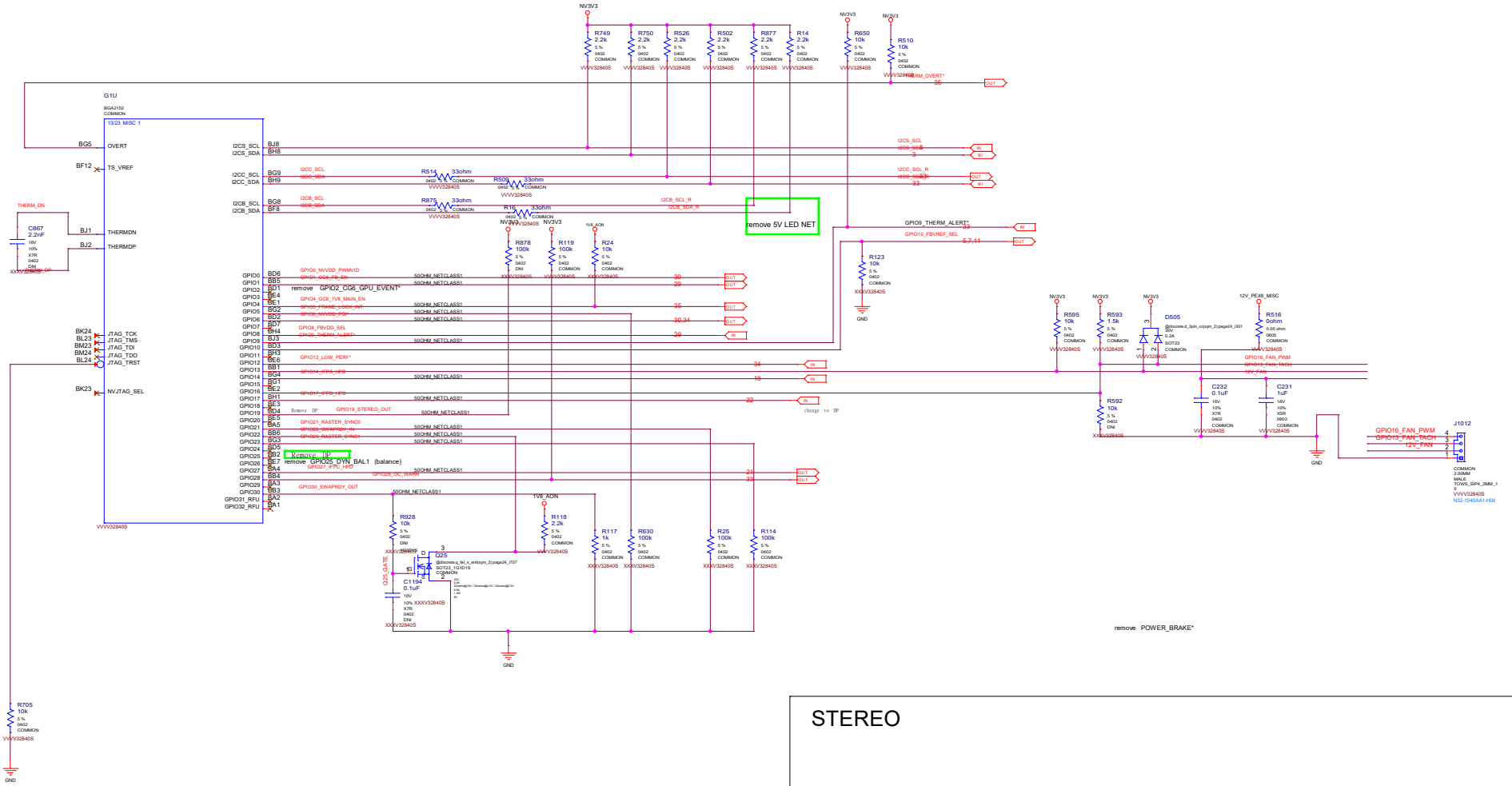
Page 24: MISC1: Fan, Thermal, JTAG, GPIO



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Page25: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

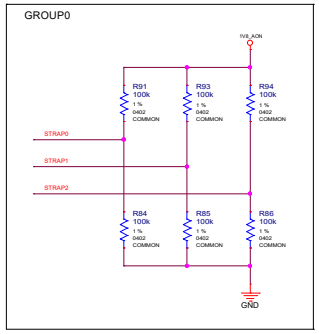
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

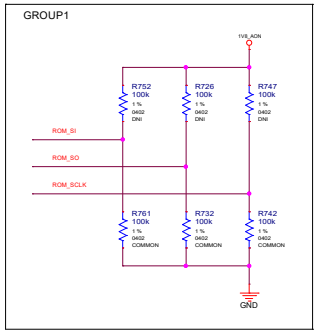
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

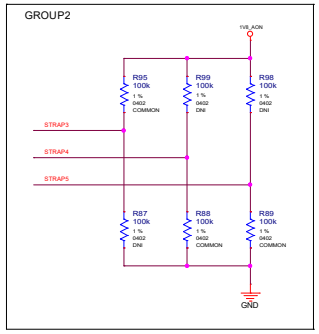
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

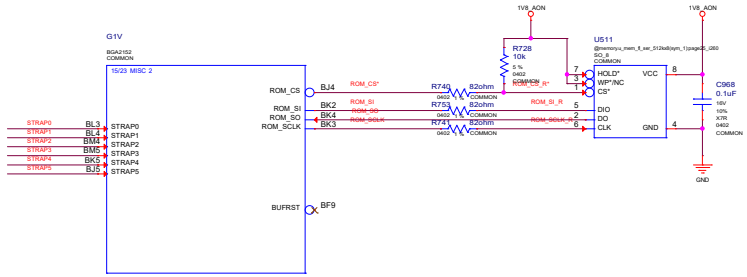
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

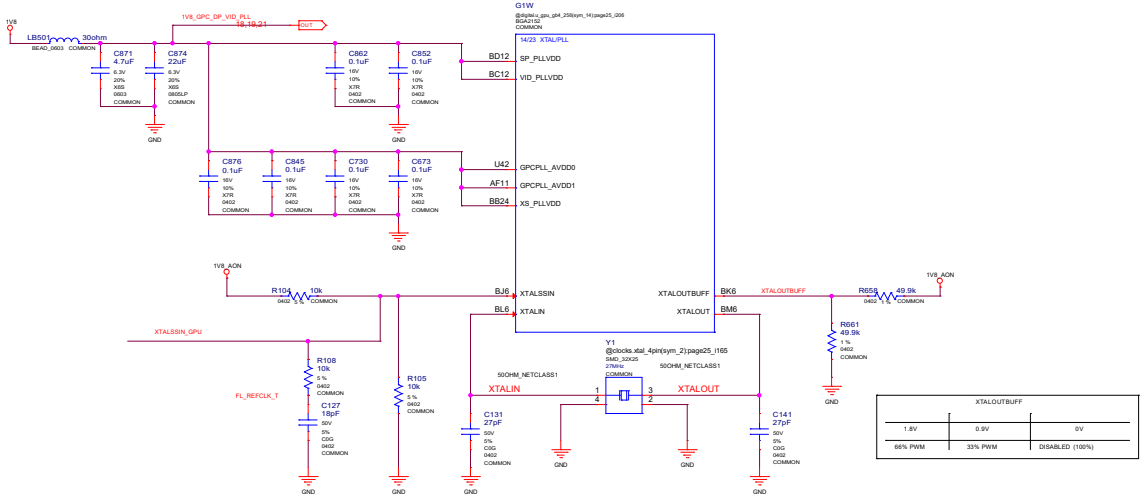






CFG[3:0]	Config	Width	Vendor
0000	256Mx32	256-bit	Samsung
0001	256Mx32	256-bit	Micron
0010	256Mx32	256-bit	Hynix
0011	Reserved		
0100	Reserved		
0101	Reserved		
0110	Reserved		
0111	Reserved		





XTALOUTBUFF		
1.8V	0.9V	0V
66% PWM	33% PWM	DISABLED (100%)

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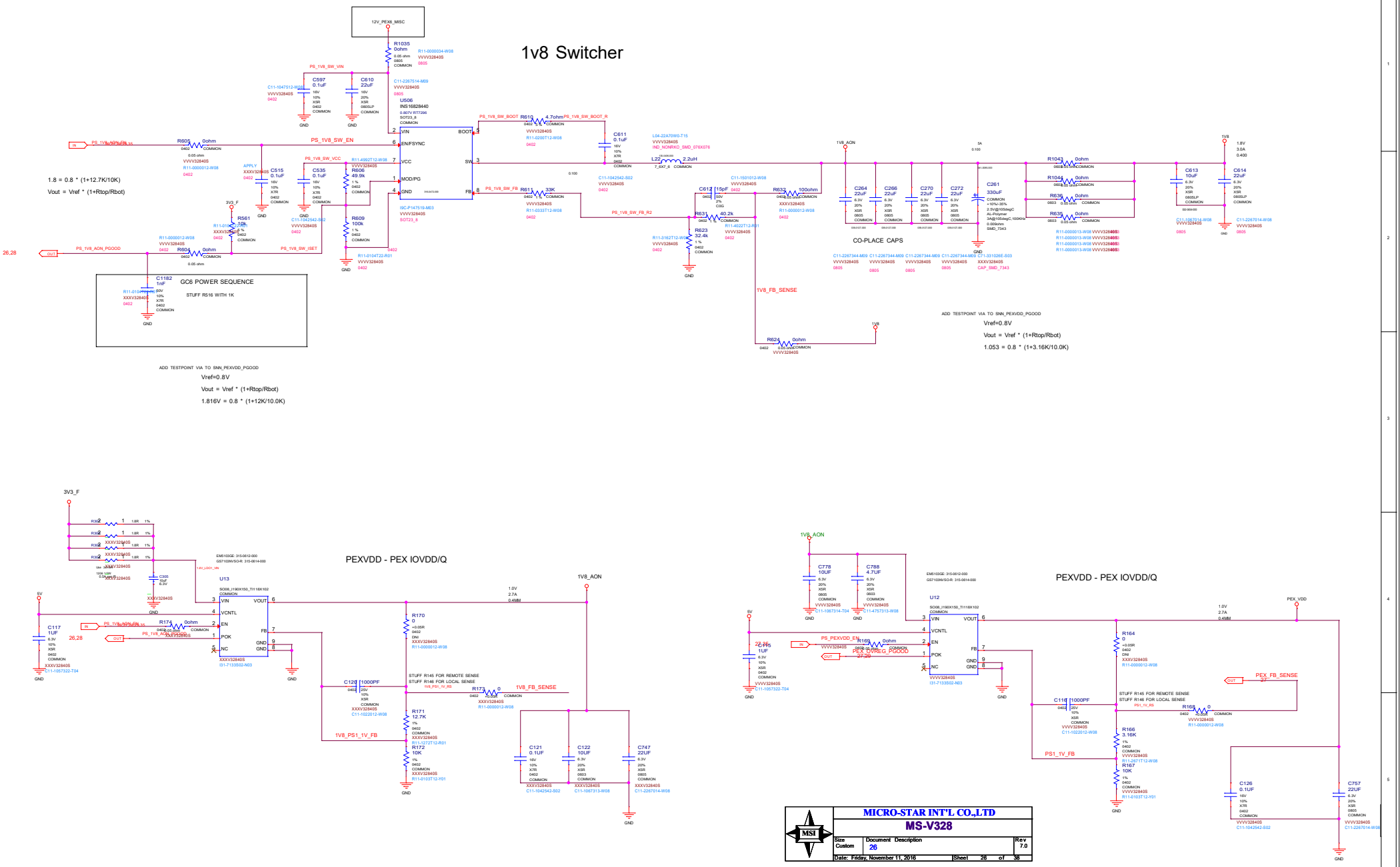
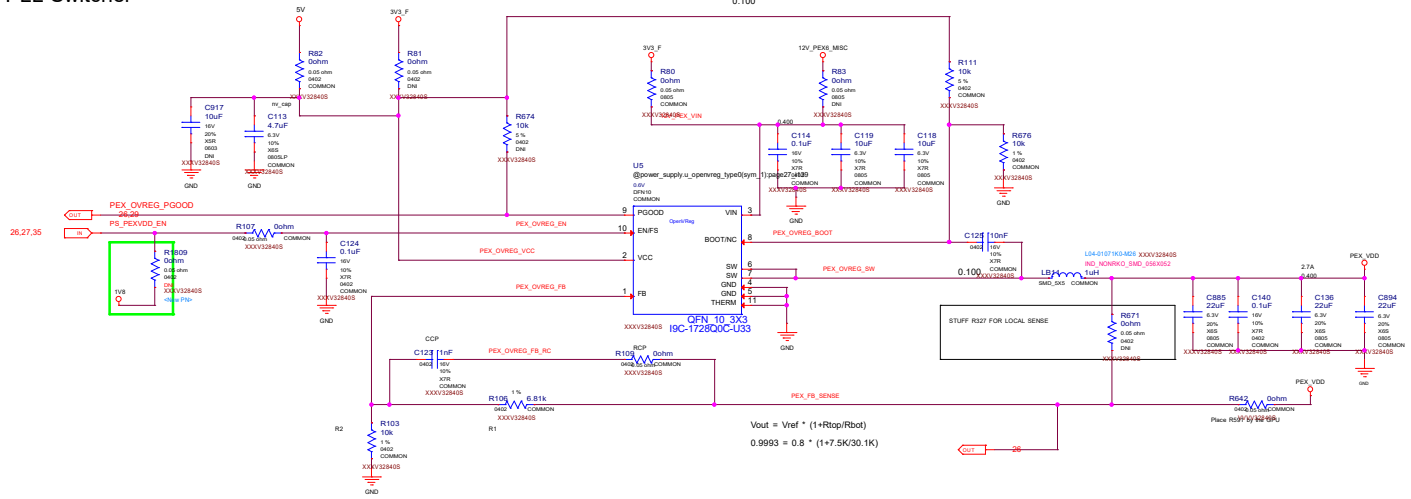
Page26: PS: 1V8 PLL, 1V8_AON

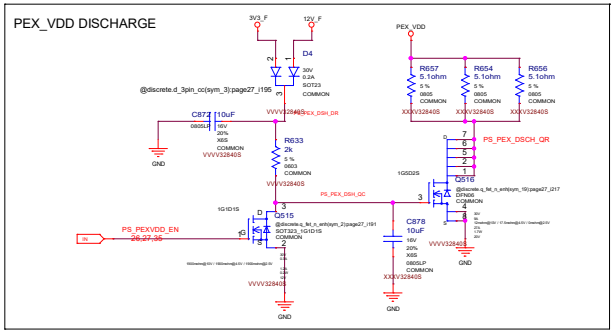


Page27: PS: 5V SWITCHER,PEX VDD

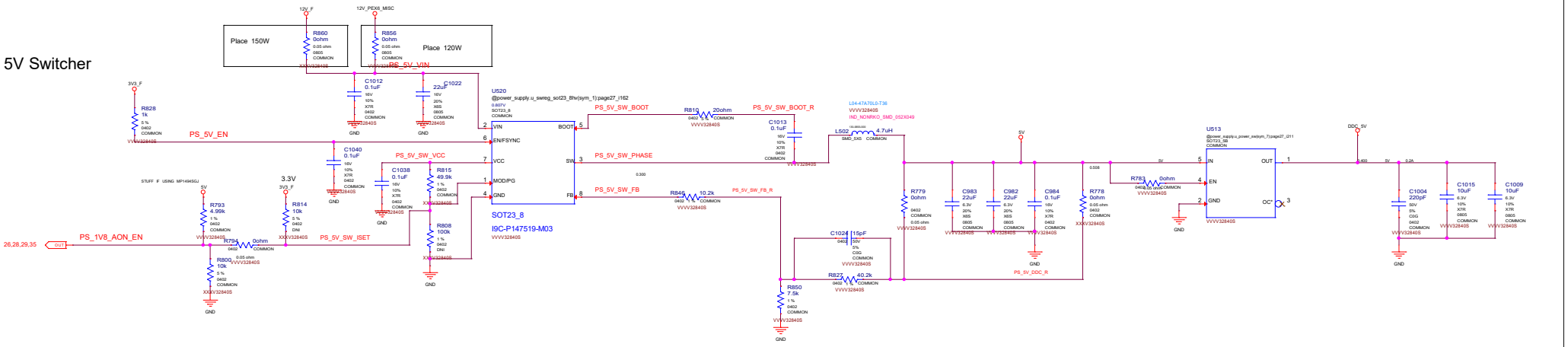
PEX PLL Switcher



PEX_VDD DISCHARGE



5V Switcher



17ci203

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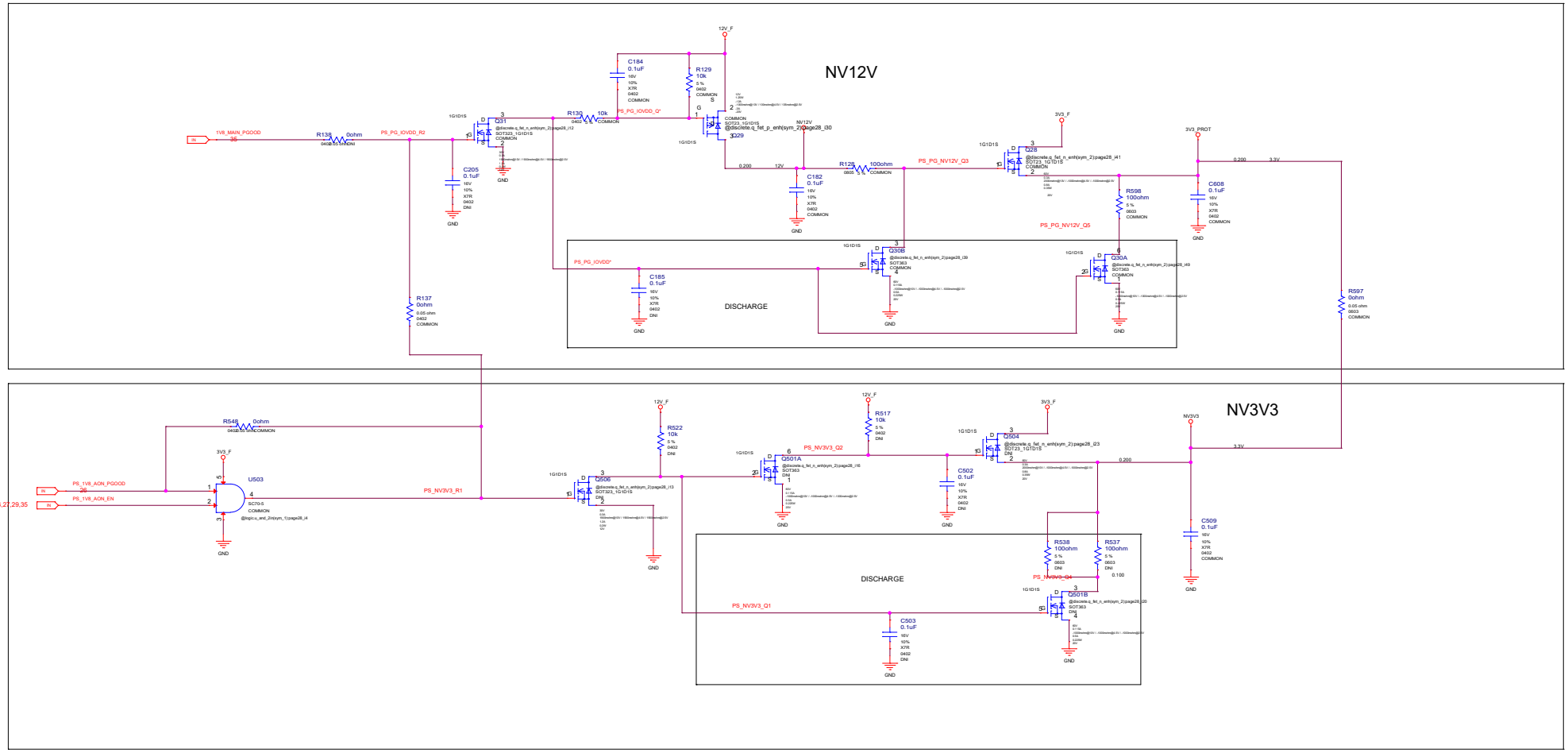

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Page29: PS: FBVDDQ

FBVDD

NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
FBVDD			

FBVDD/Q Enable

GDDR5X ONLY

FBVDD DISCHARGE

SAMSUNG

GPIO8 LEVEL	FBVDDQ OUTPUT VOLTAGE
0	1.35V
1	1.55V

P26 -PULL HIGH 3V3

Rbb

remove C610

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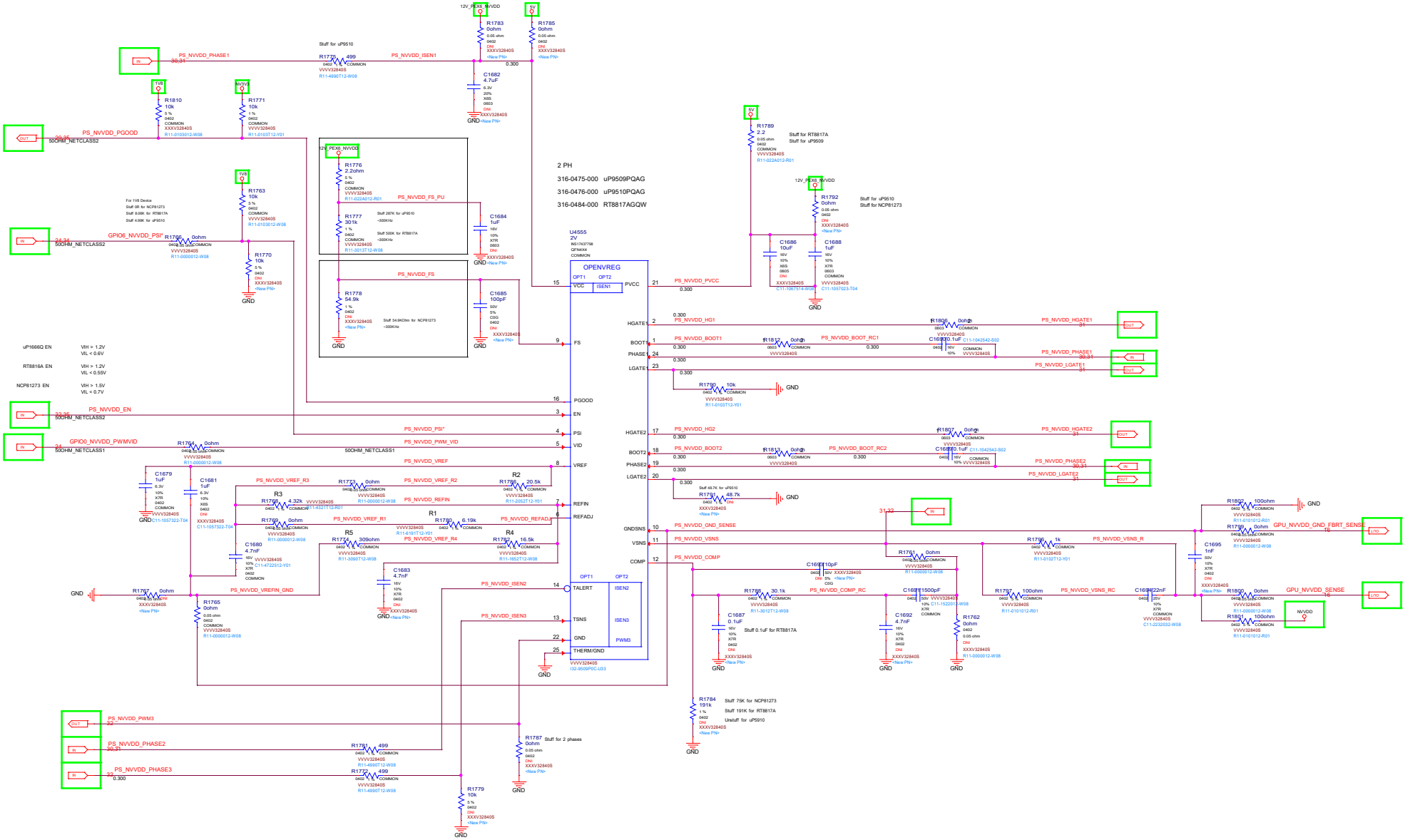
PS V: NVVDD OVR2+1



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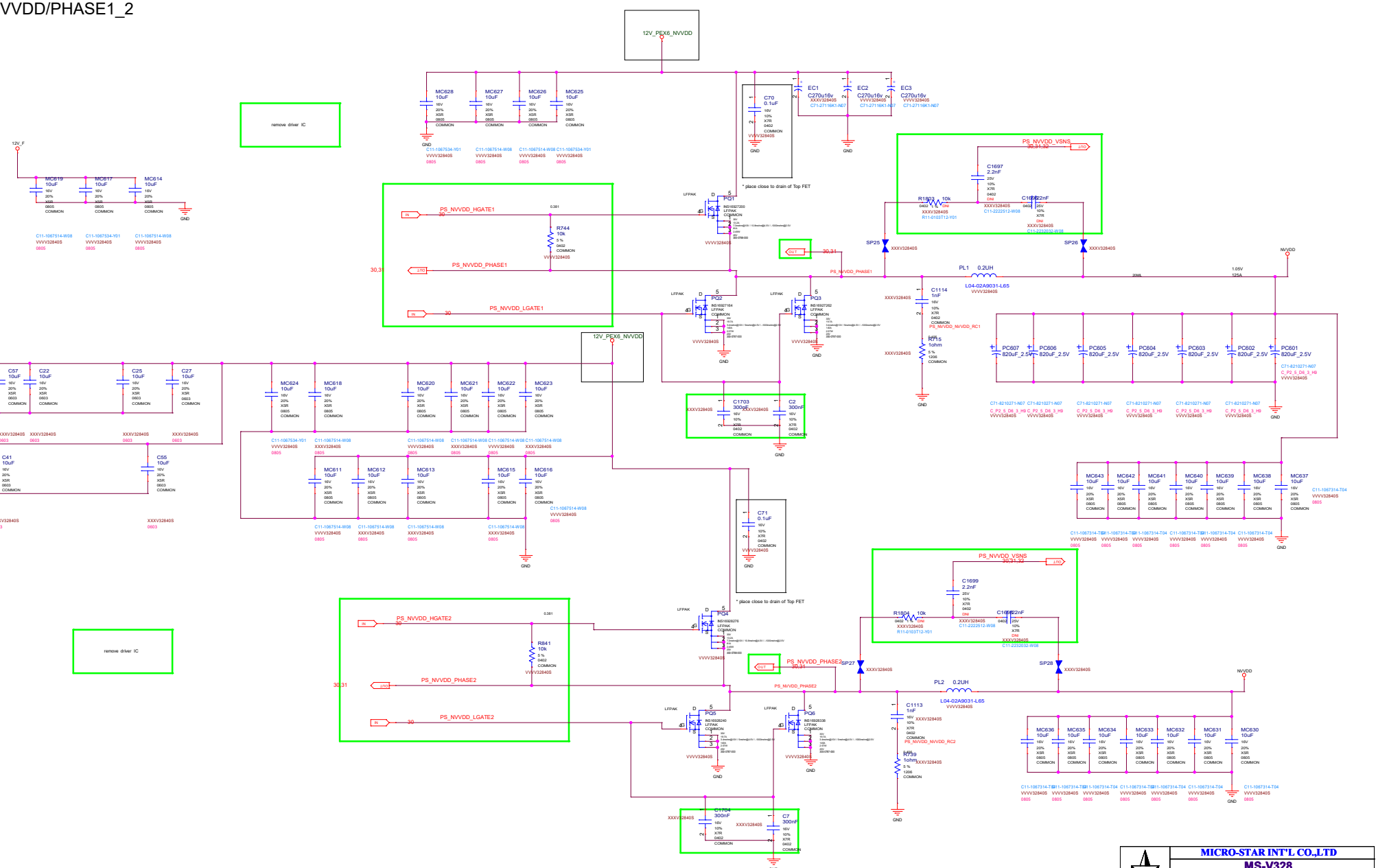
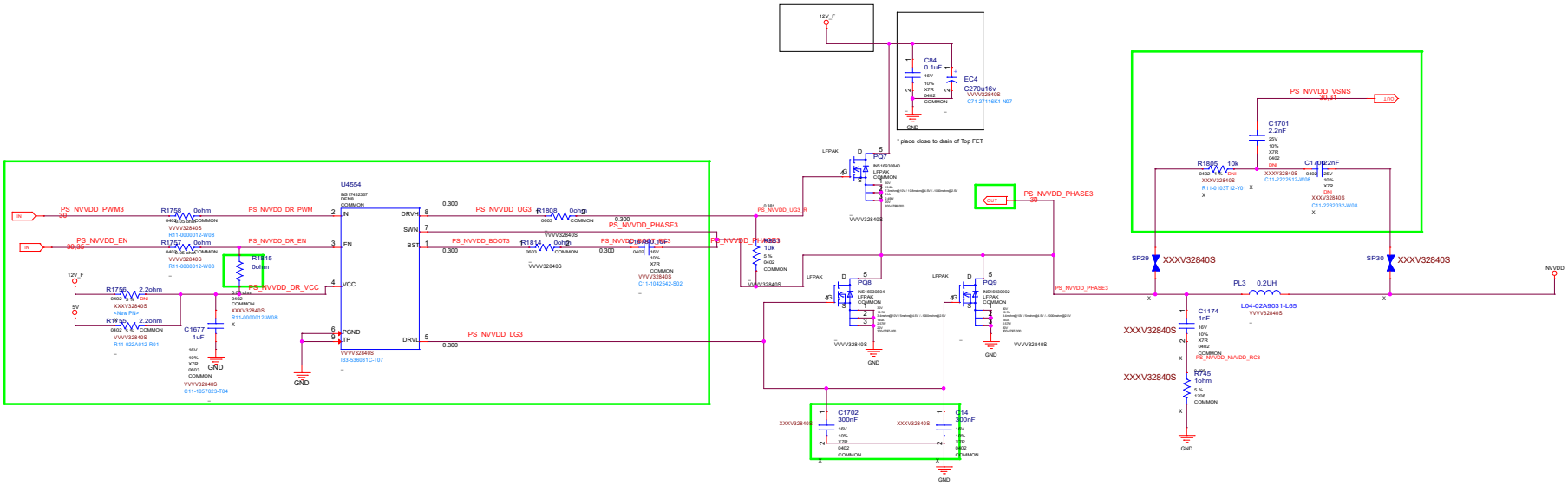
Pgae 31:NVVDD/PHASE1_2



Page32: PS: NVVDD PHASE 3/4



CORE 90A /3 =30A
CORE 1 - EXT 6
CORE 2 - EXT 6
CORE 3 - BUS
MEM 30A- BUS
-BUS WARRING-

CORE 90A /4 =22.5A
CORE 1 - EXT 6
CORE 2 - EXT 6
CORE 3 - BUS
CORE 4 - EXT 6
MEM 30A- BUS

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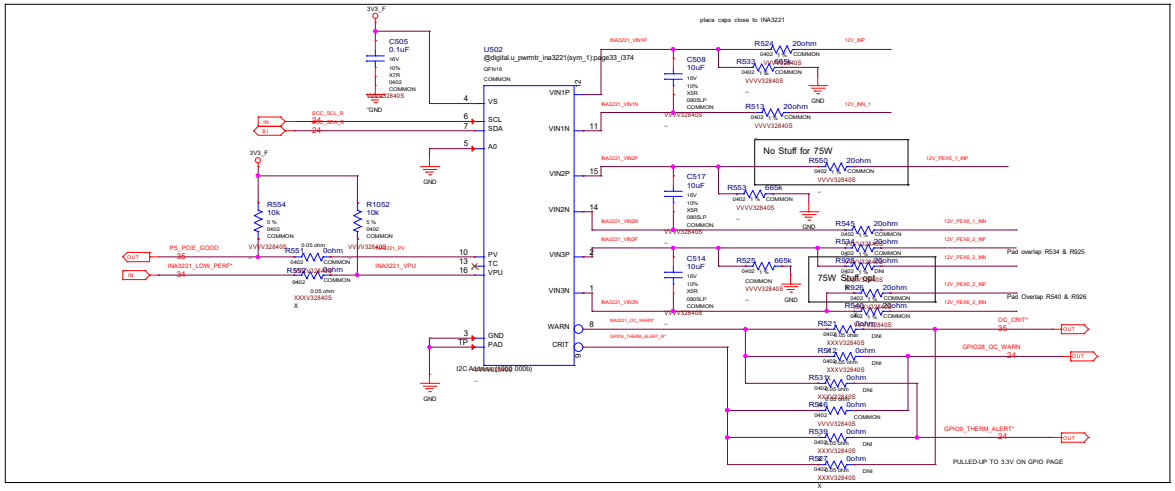
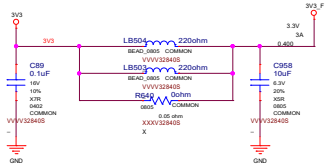
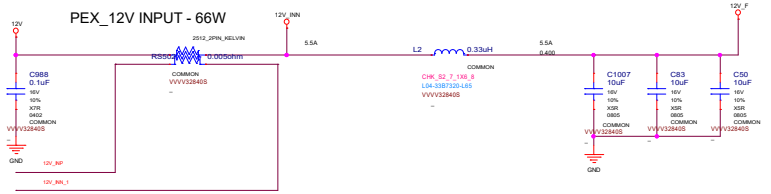
Page33: PS: Inputs, Filtering, and Monitoring



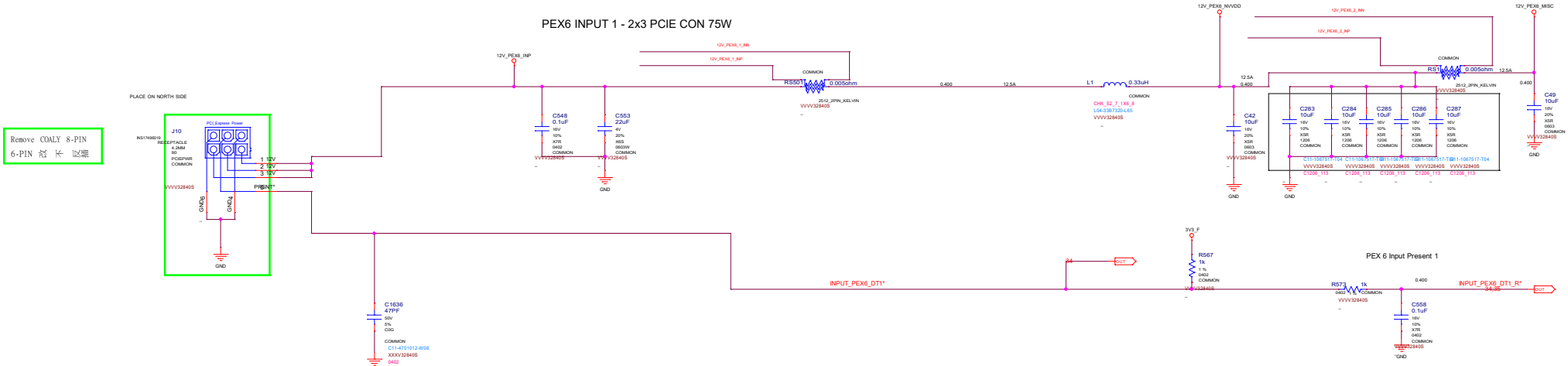
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



PEX6 INPUT 1 - 2x3 PCIE CON 75W



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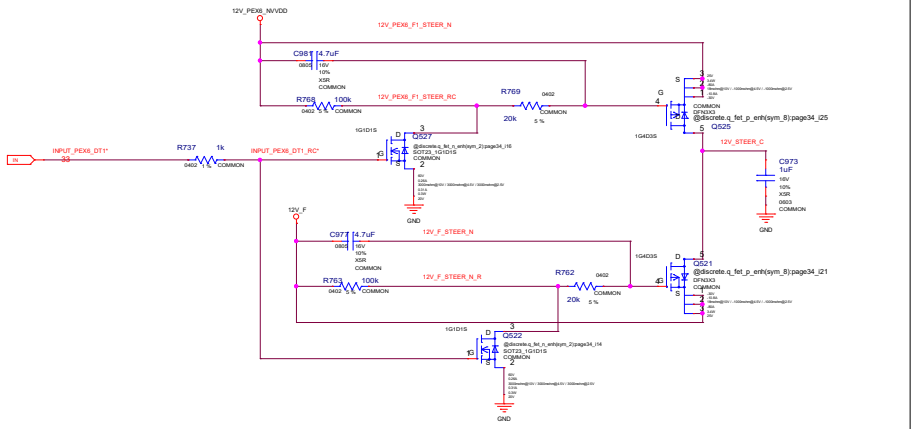
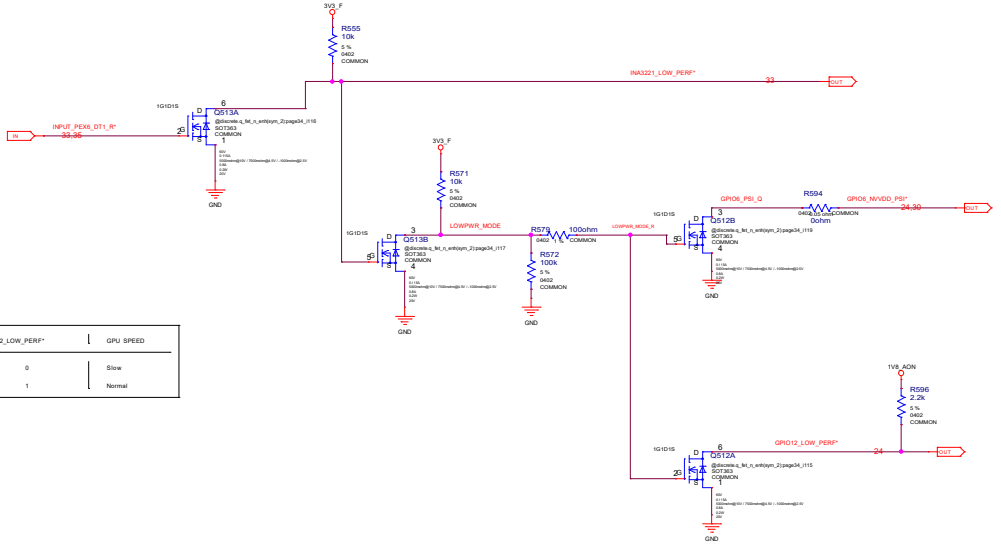
Page34: PS: 12V Current Steering, PSI Control, and LED

12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA



PEX Input - Power Level/PSI* Control



GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

GeForce Logo LED

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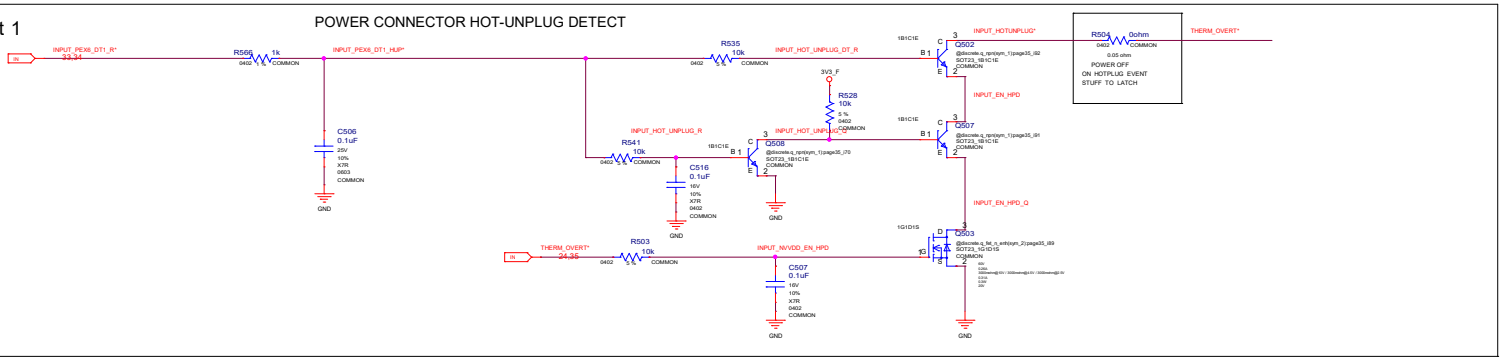
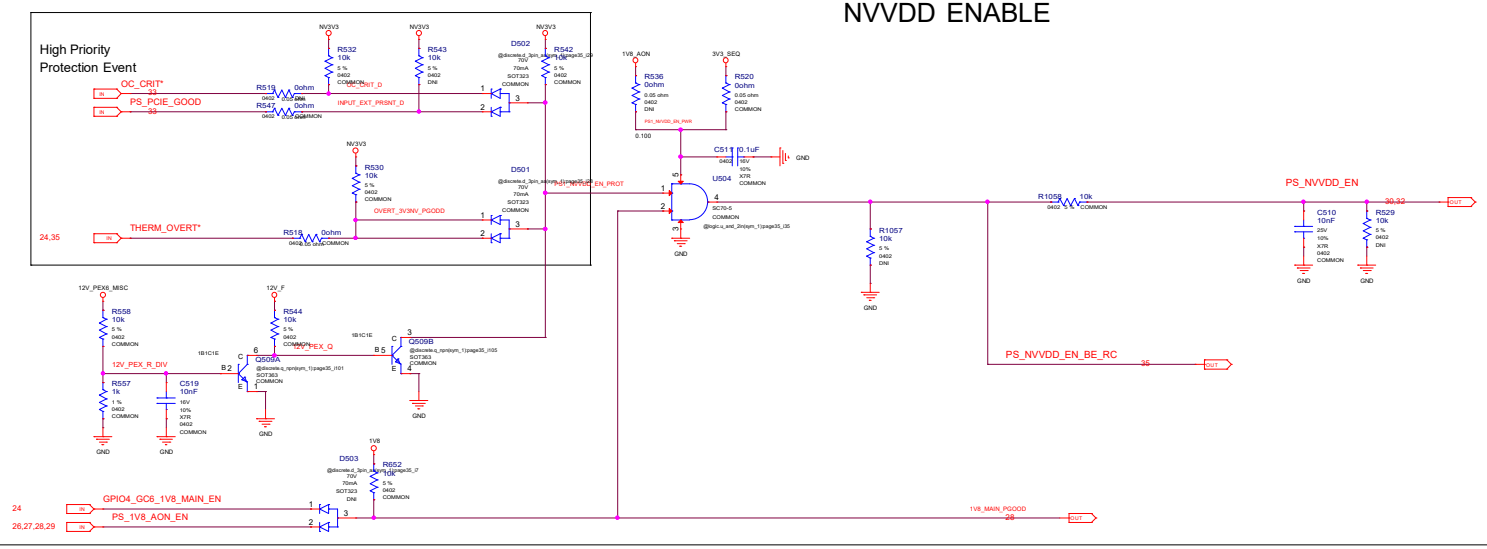
Page37: PS: Shutdown and Sequencing

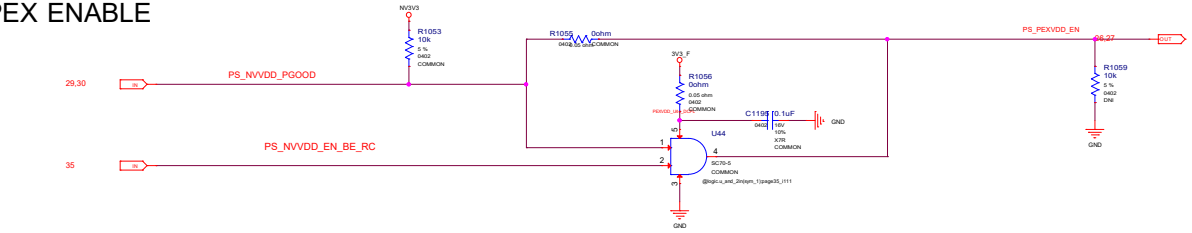
PEX Input Present 1



NVVDD ENABLE



PEX ENABLE



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Page38: LED

remove GC6 FB ENABLE
remove GPU_EVENT*
remove PEX_CLKREQ*
PEX_RST# LOGIC

Accept 3V3 Logic

remove 5V LED NET

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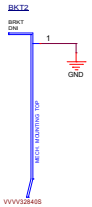
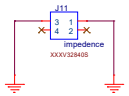
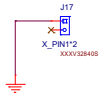
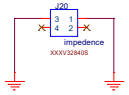
Page37: MECH

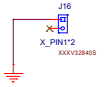
Brackets:

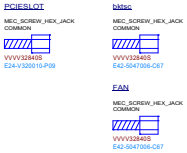


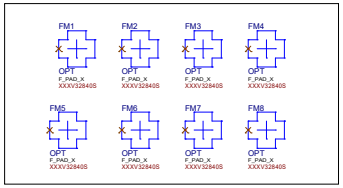






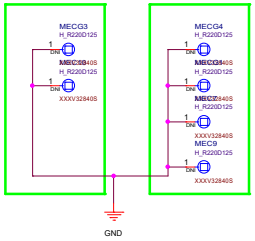






NVVDD MOS Holes Symbol

GPU Holes Symbol



Remove: MEC12/MEC13/MEC14/MEC15/MEC11/MEC8/MECG2/MECG1

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2016/10/19 Change history

Page: 18	DVI-D 更換為單層無架
Page: 19	Remove DP
Page: 20	Remove DP
Page: 22	from HDMI change to DP
Page: 24	Remove gpio 24 DP HPD Remove Remove gpio 18 DP HPD remove LED NET gpio 17 , from HDMI change to DP HPD
Page: 27	預留1.8V to PEX-VDD convertor
Page: 29	預留0402 MLCC*2 for L side mos
Page: 30	change PWM to I32-9509P0C-U33
Page: 31	remove phase1 & phase2 driver IC
Page: 32	change phase3 driver IC to I33-536031C-T07 remove phase4
Page: 33	Remove COALY 8-PIN 6-PIN 改不反插
Page: 36	remove 5V LED NET
Page: 37	Remove: MEC12/MEC13/MEC14/MEC15/MEC11/MEC8/MECG2/MECG1