PG410 A01

GP106 8GB/4GB GDDR5, 256b, 256Mx32/128MX32
Tall DVI-D + DP + DP + HDMI/DP + DP

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6.1
1.修改 NVVDD_VRM線路
2.修改 LED線路
3.增加 COLAY線路
4.修HDMI DP COLAY

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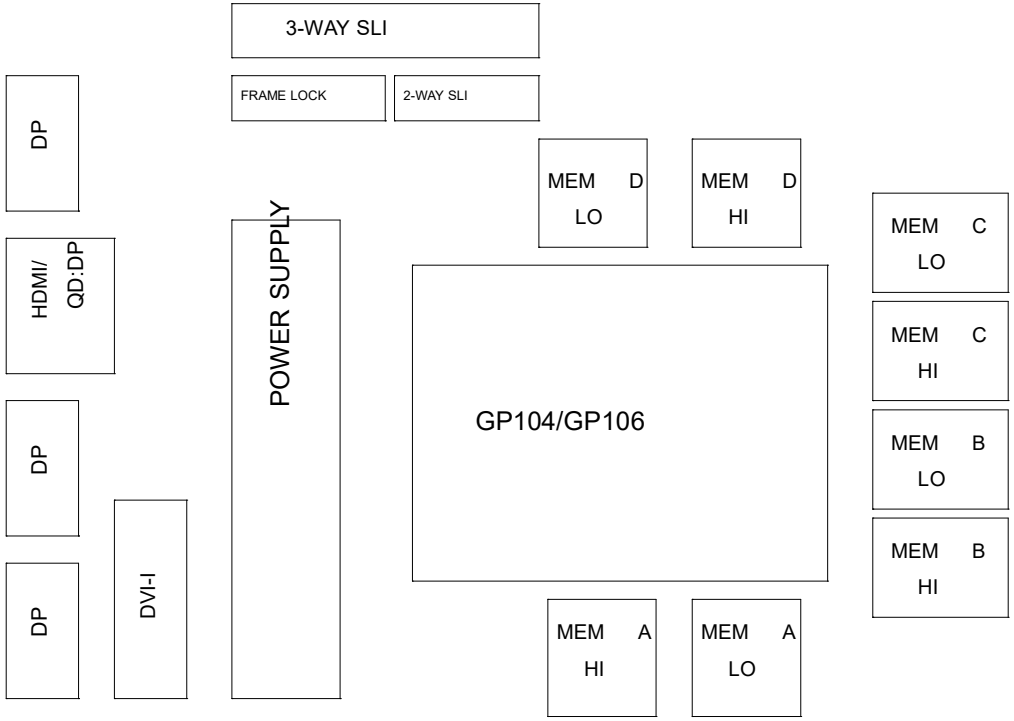
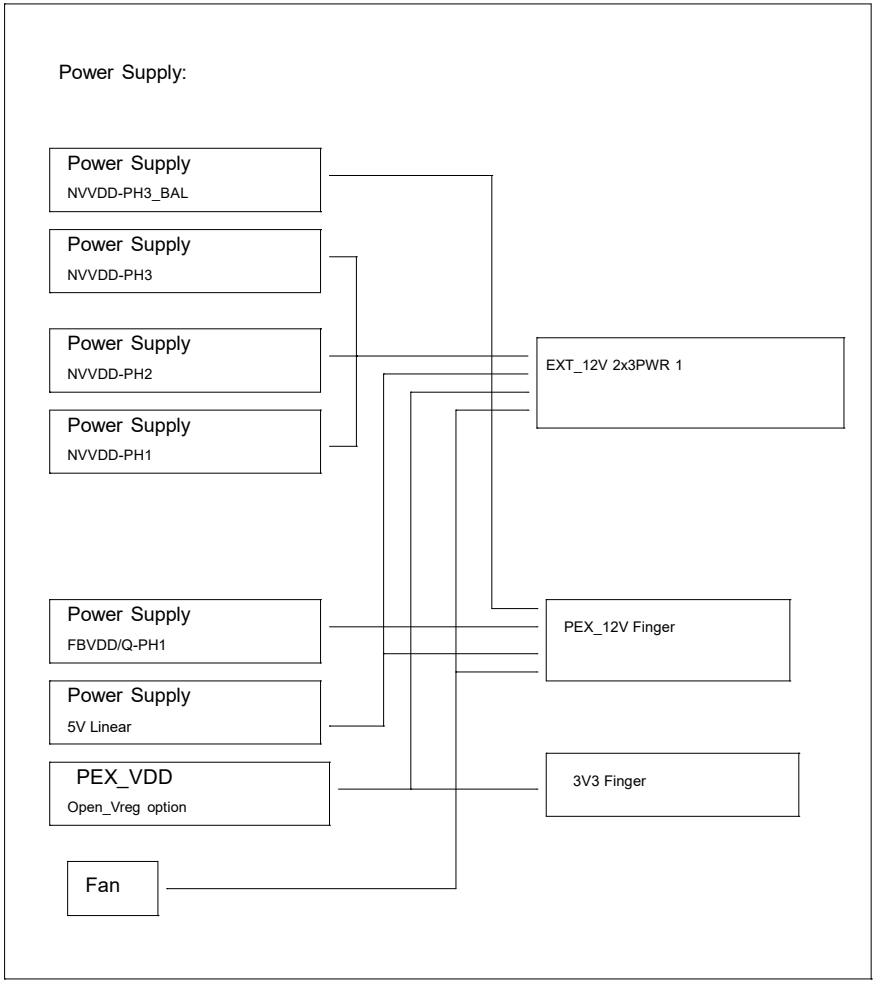
Page2: Block Diagram





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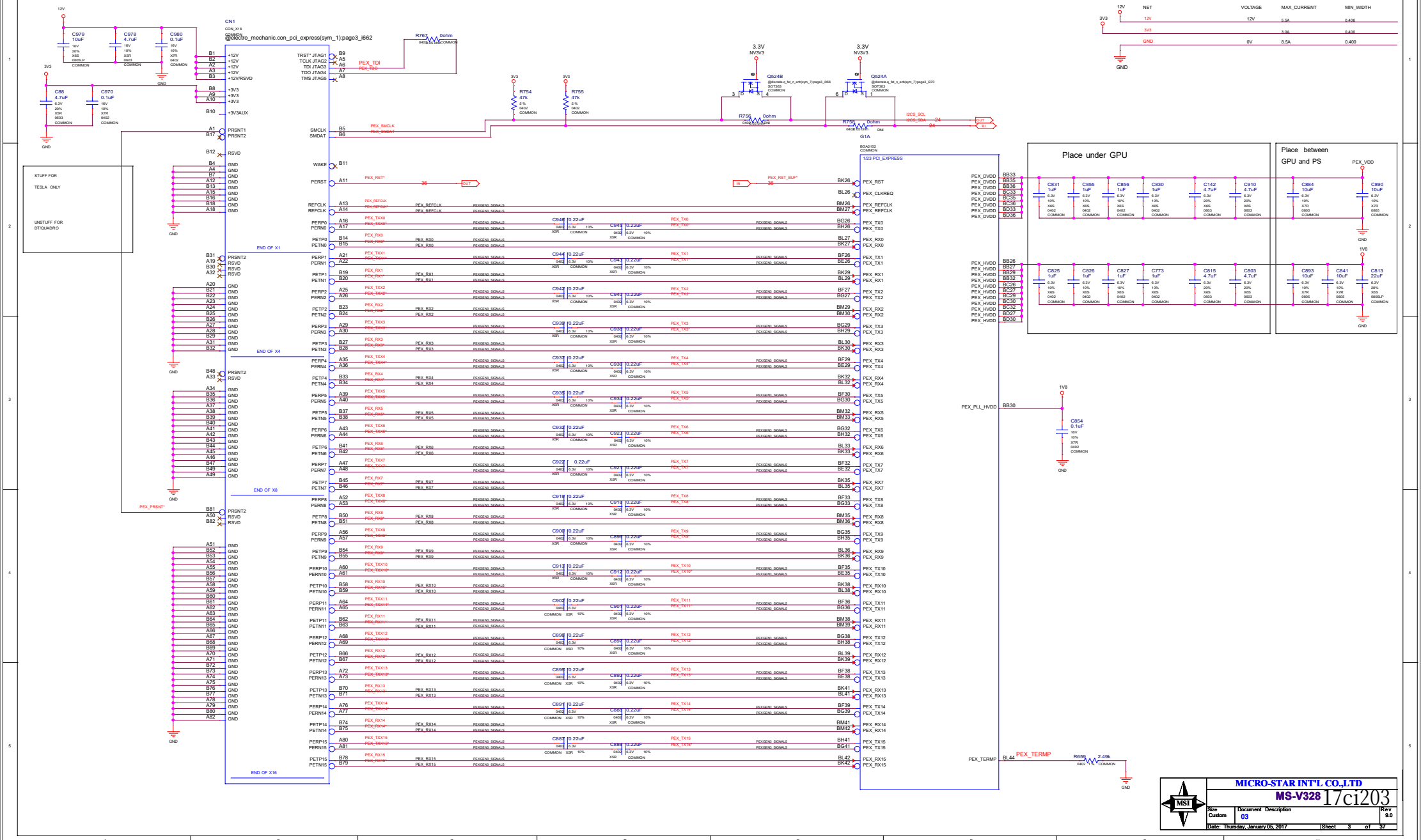
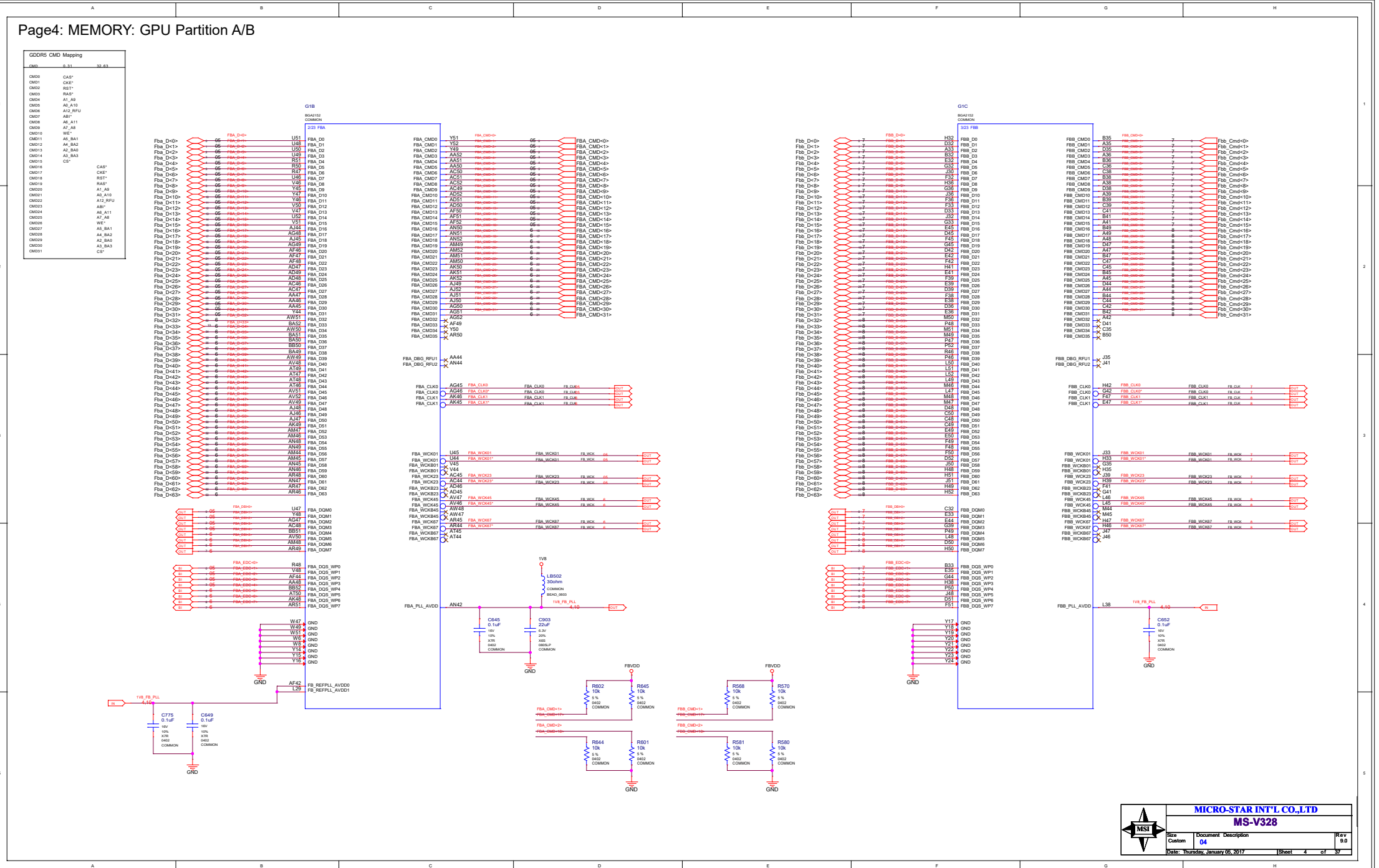
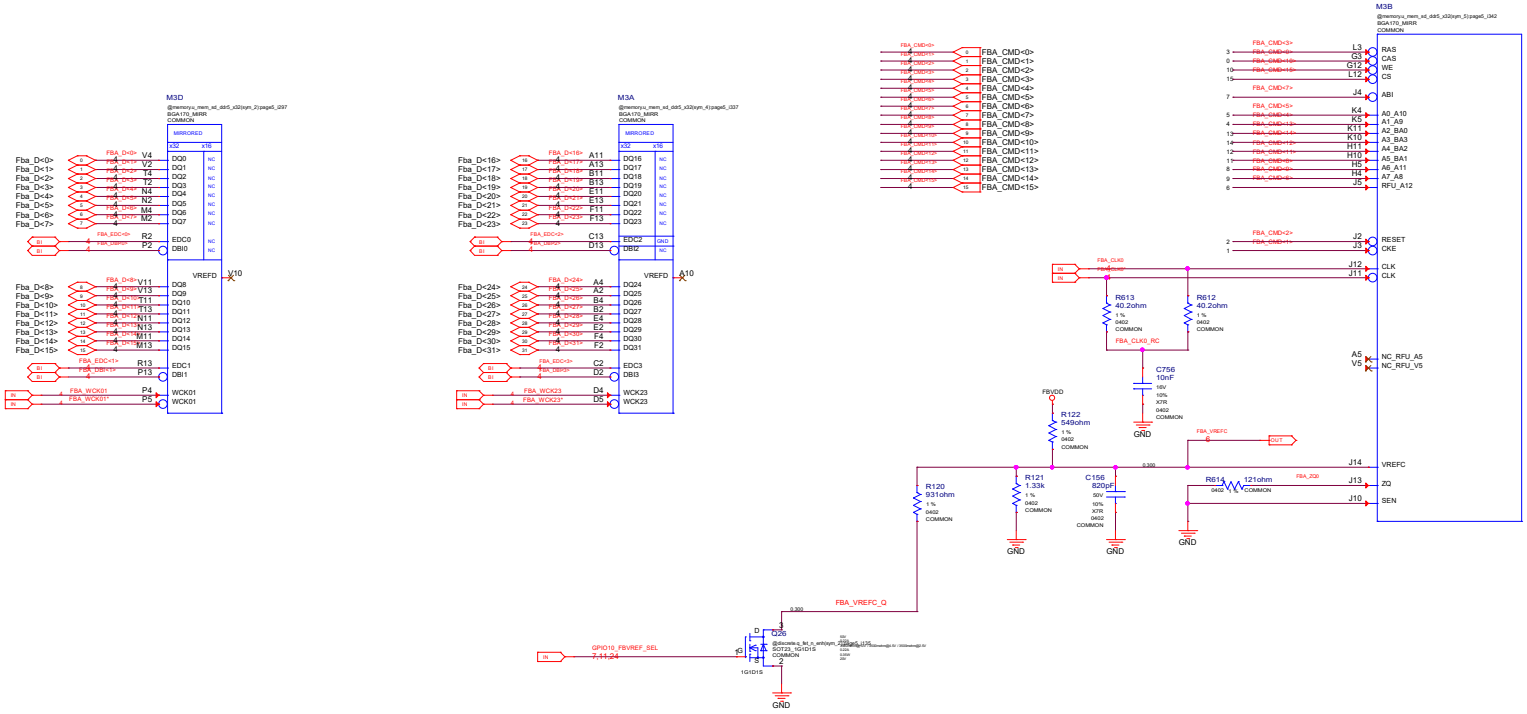
Page3: PCI Express



Page4: MEMORY: GPU Partition A/B



Page5: FRAME BUFFER PARTITION A [31:0]



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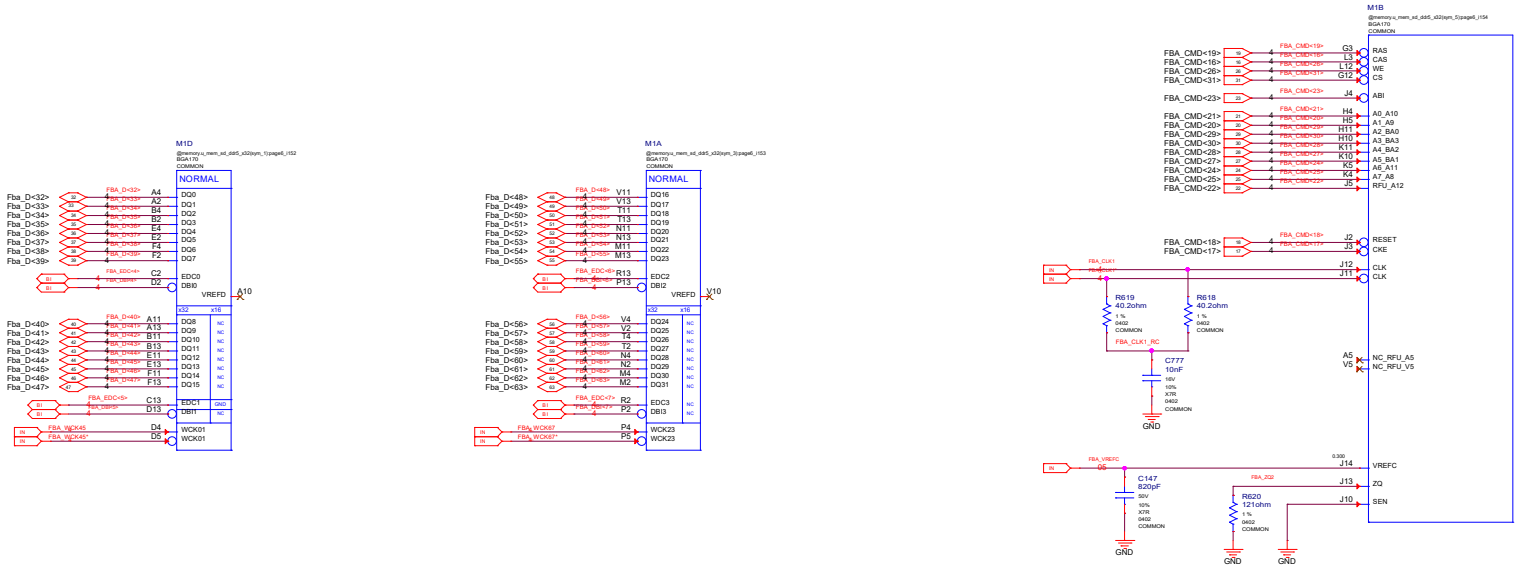
Page6: FRAME BUFFER PARTITION A [63:32]



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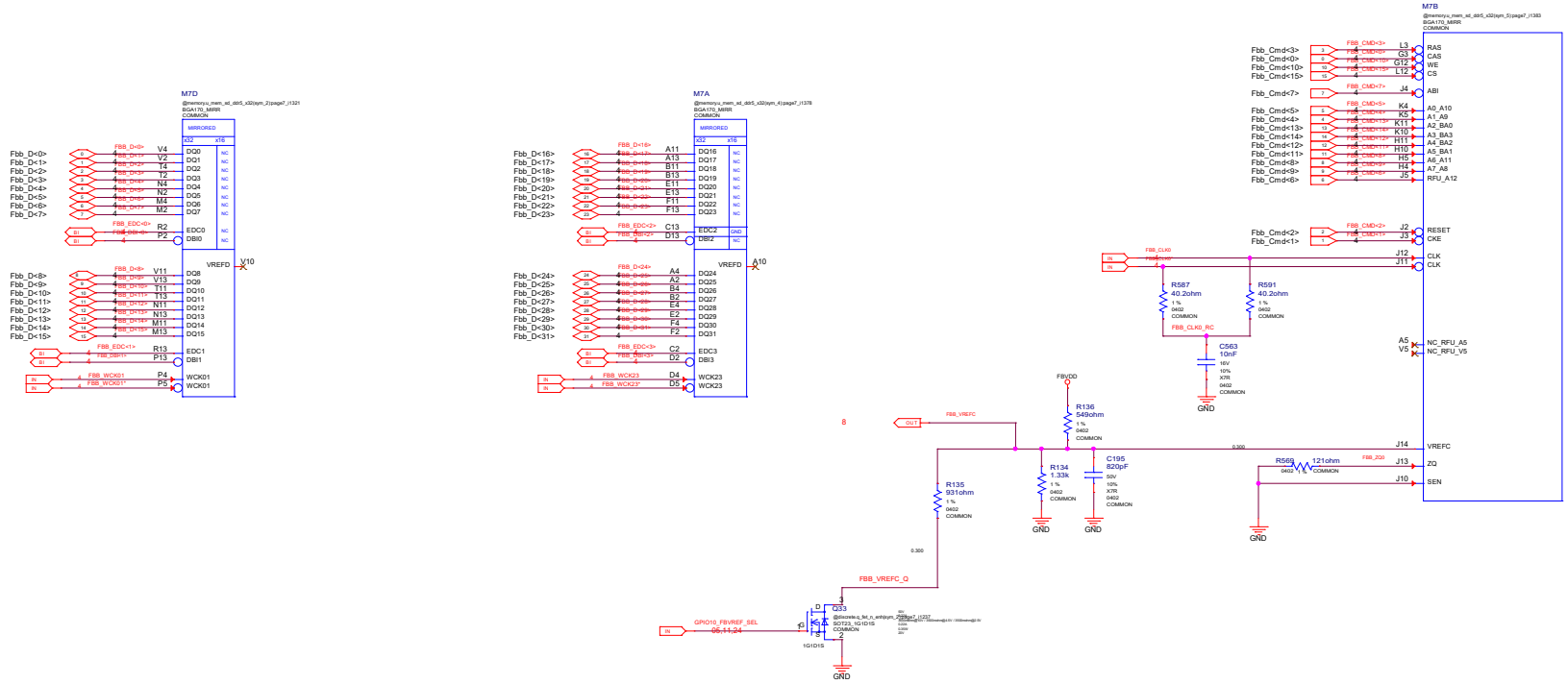
Page7: FRAME BUFFER PARTITION B [31:0]



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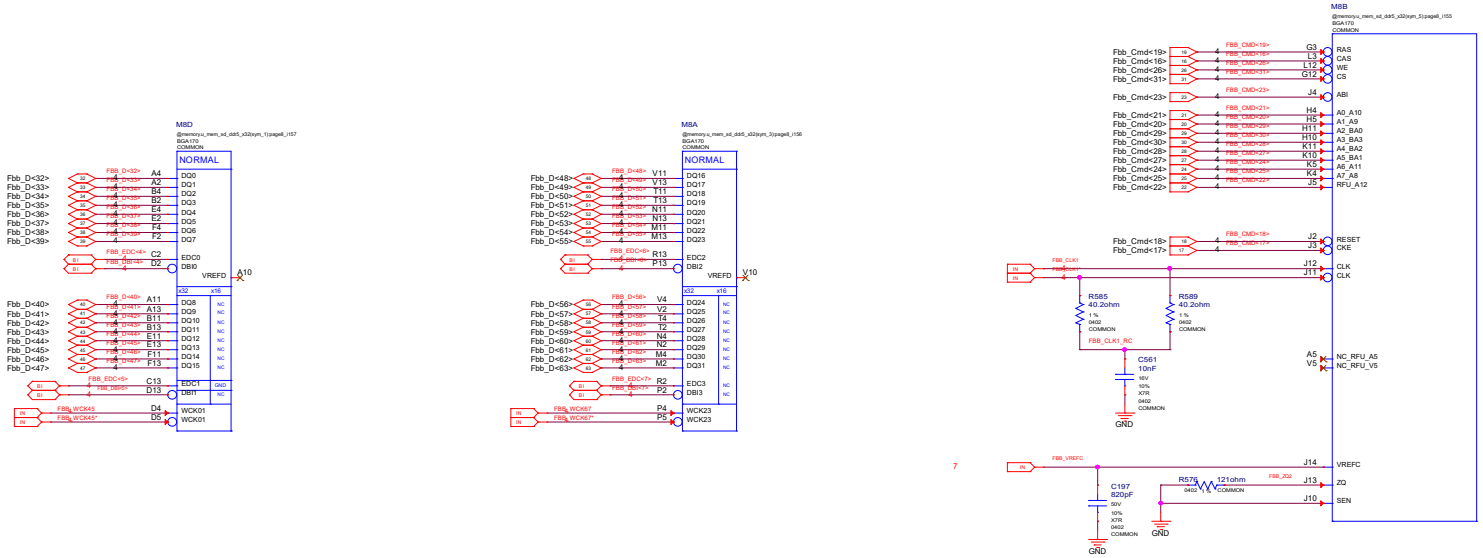
Page8: FRAME BUFFER PARTITION B [63:32]



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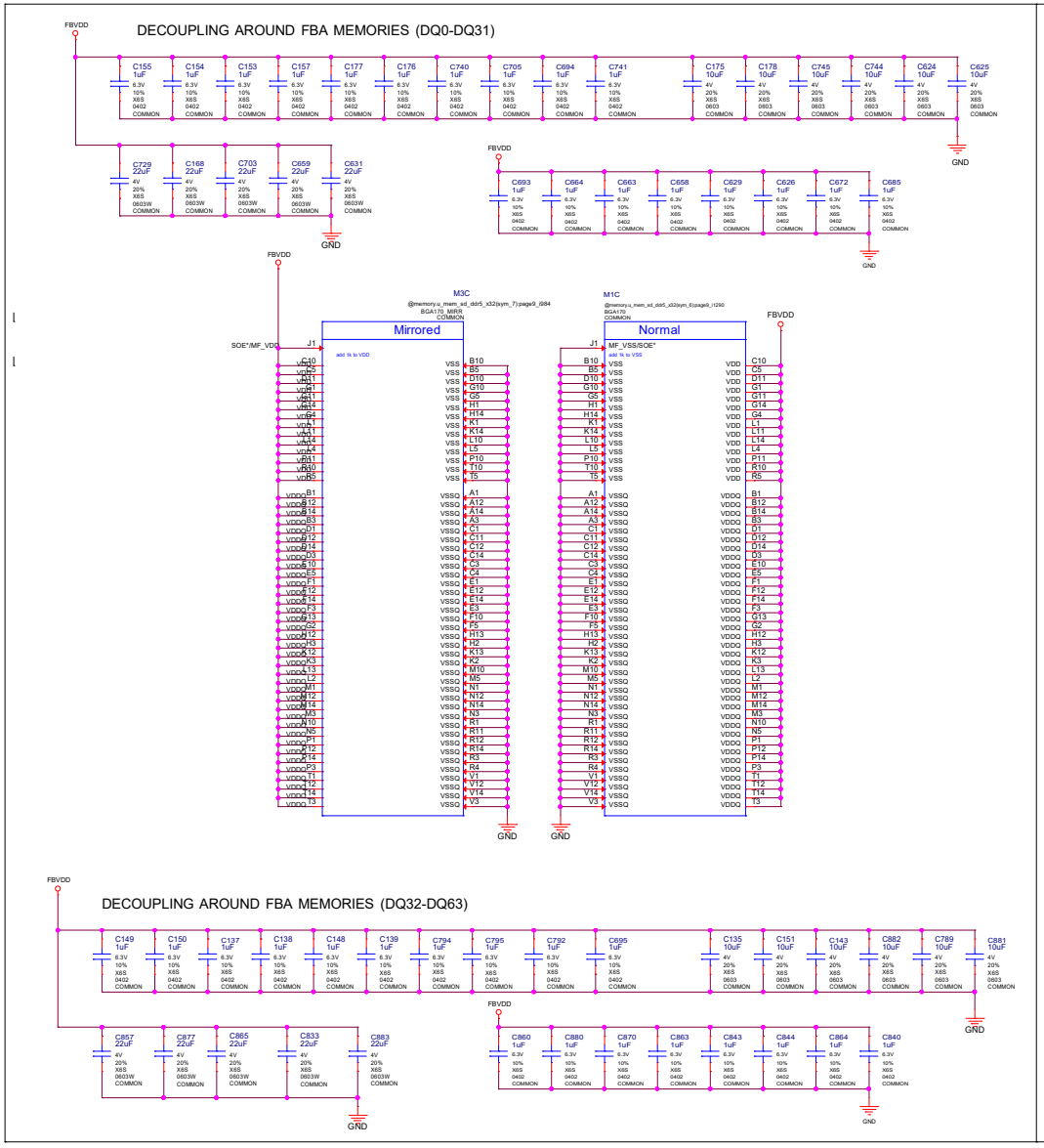
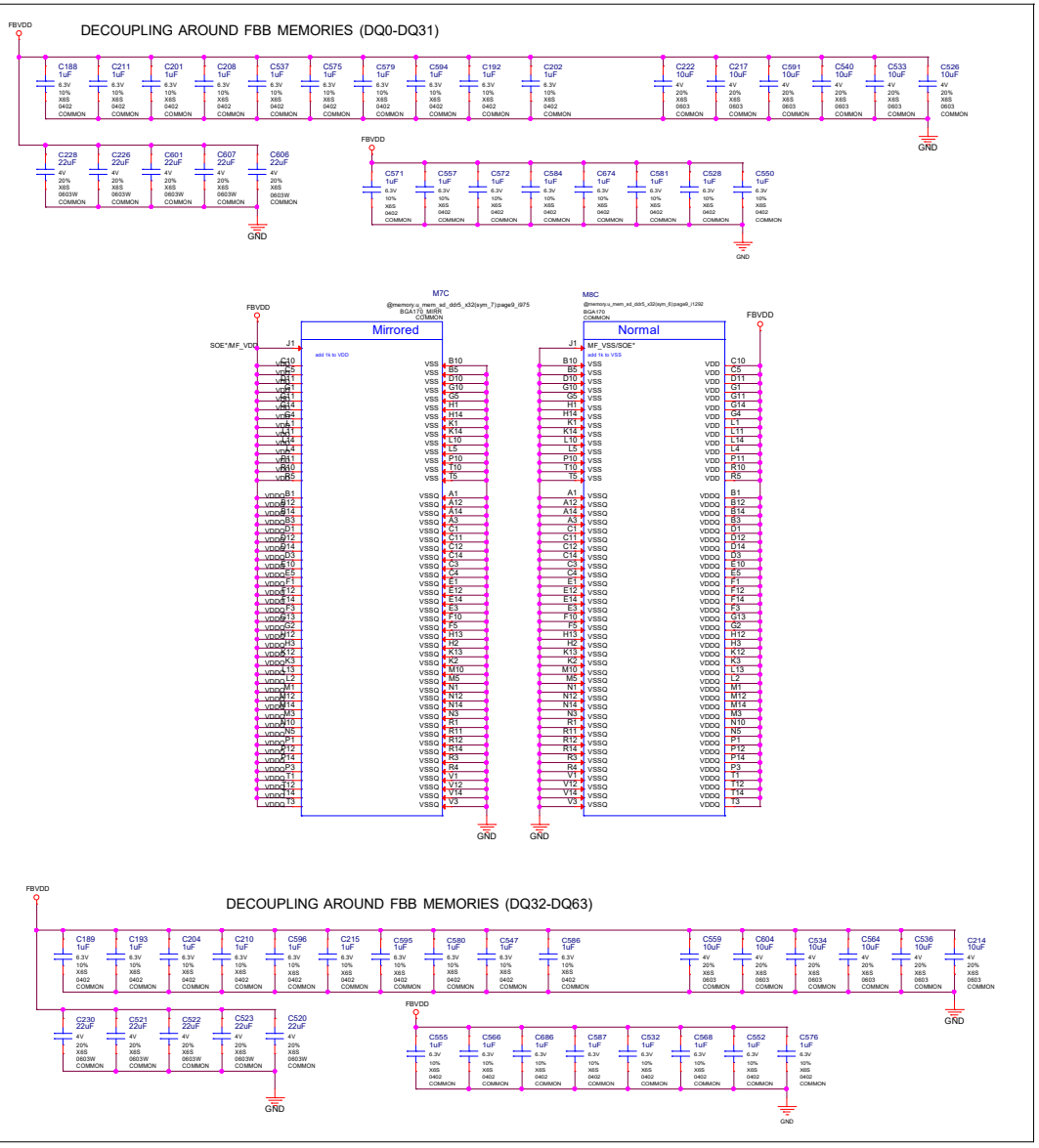
Page9: FRAME BUFFER PARTITION A/B DECOUPLING





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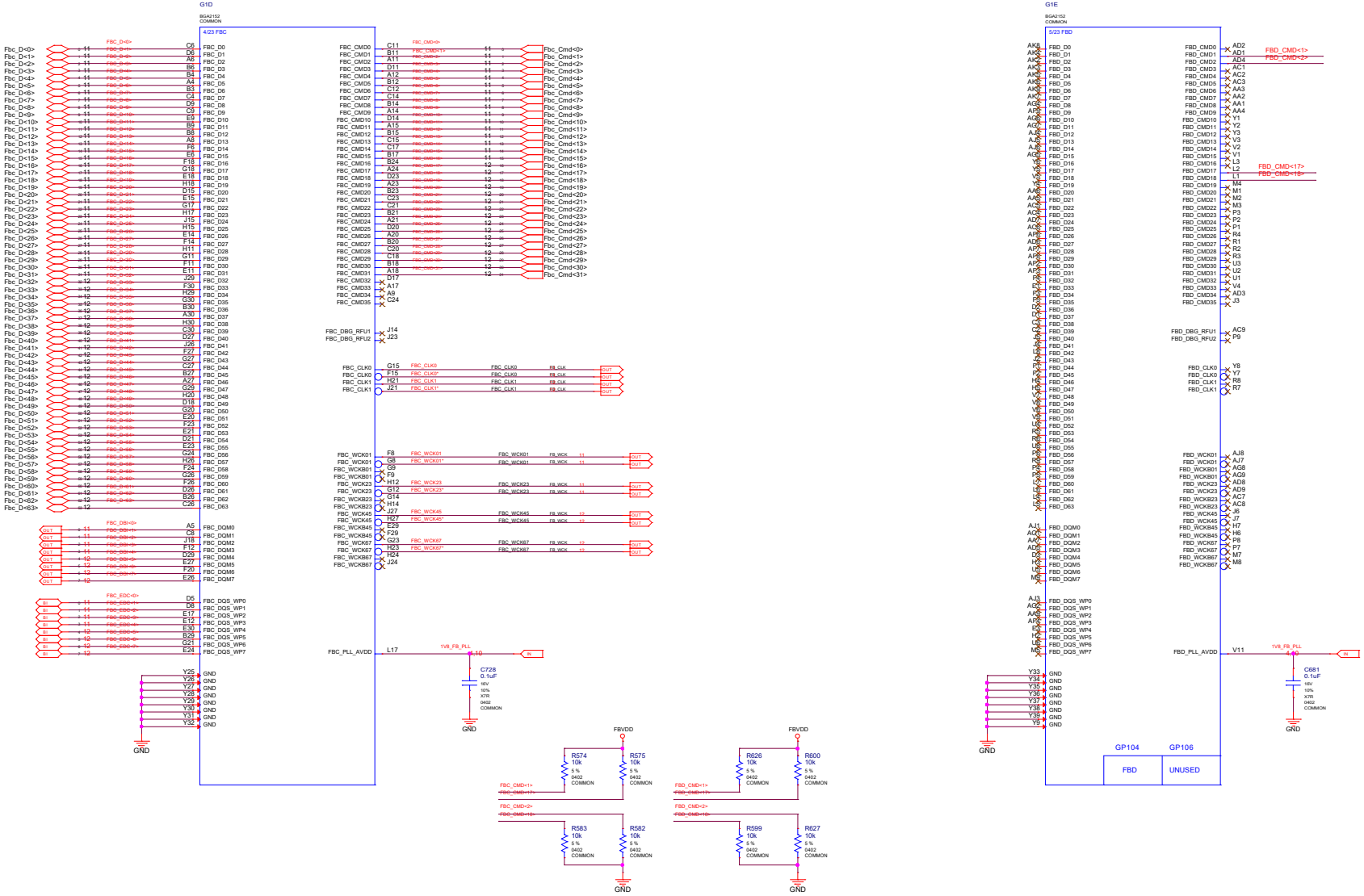
Page10: MEMORY: GPU Partition C/D

GDDR5 CMD Mapping

CMD	0_31	32_63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	AB*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		AB*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*



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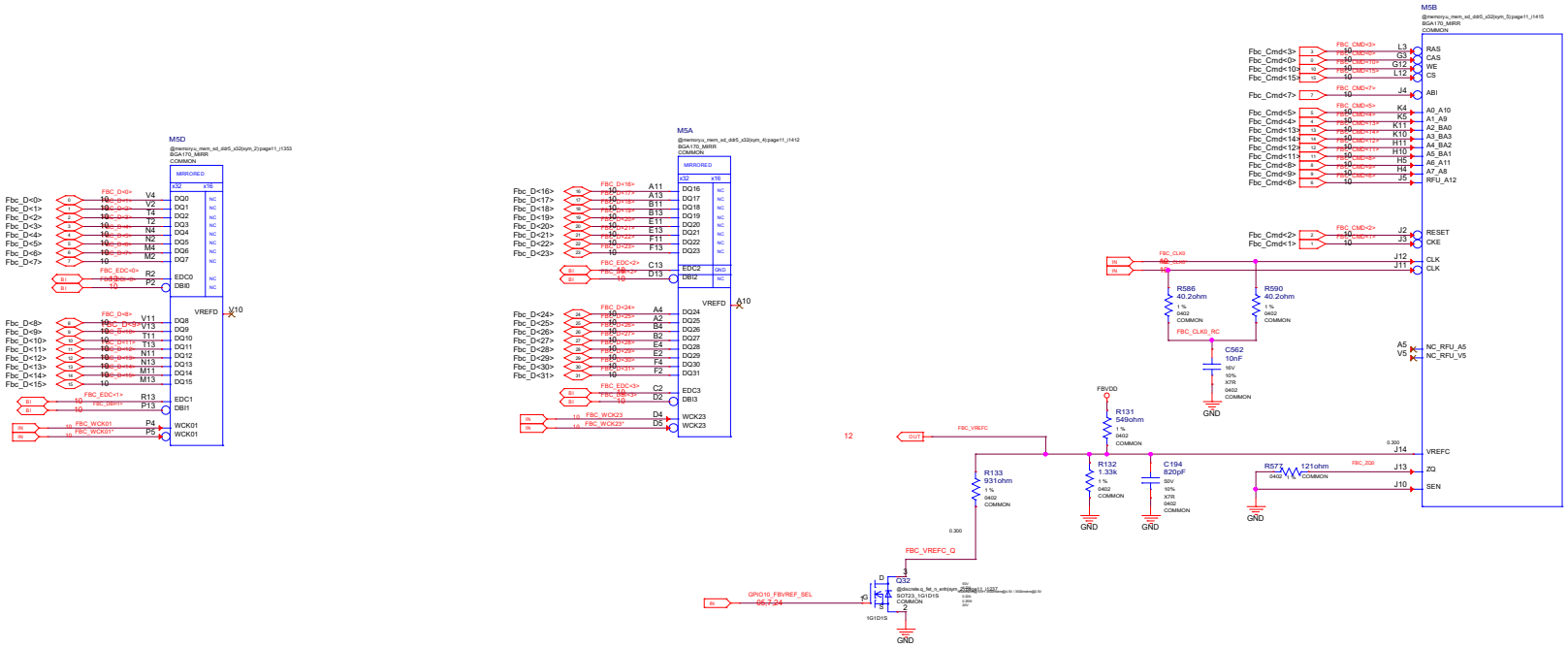
Page11: Frame Buffer Partition C [31:0]



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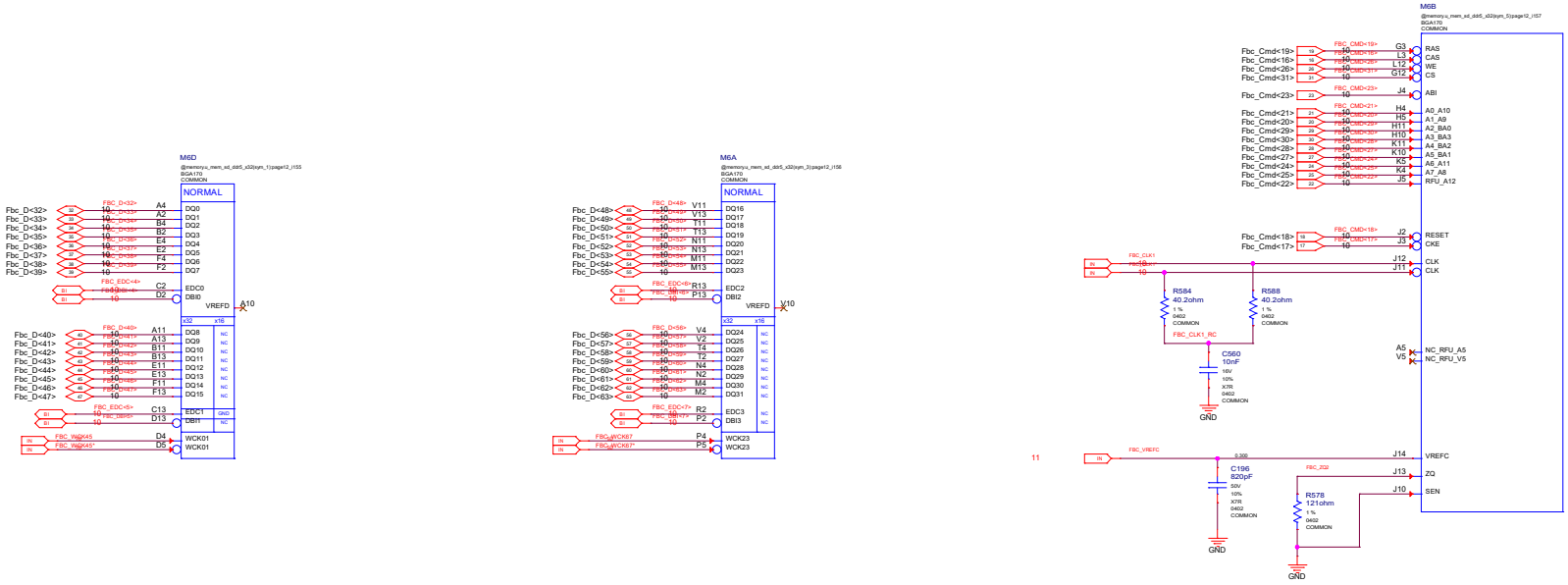
Page12: FRAME BUFFER PARTITION C [63:32]



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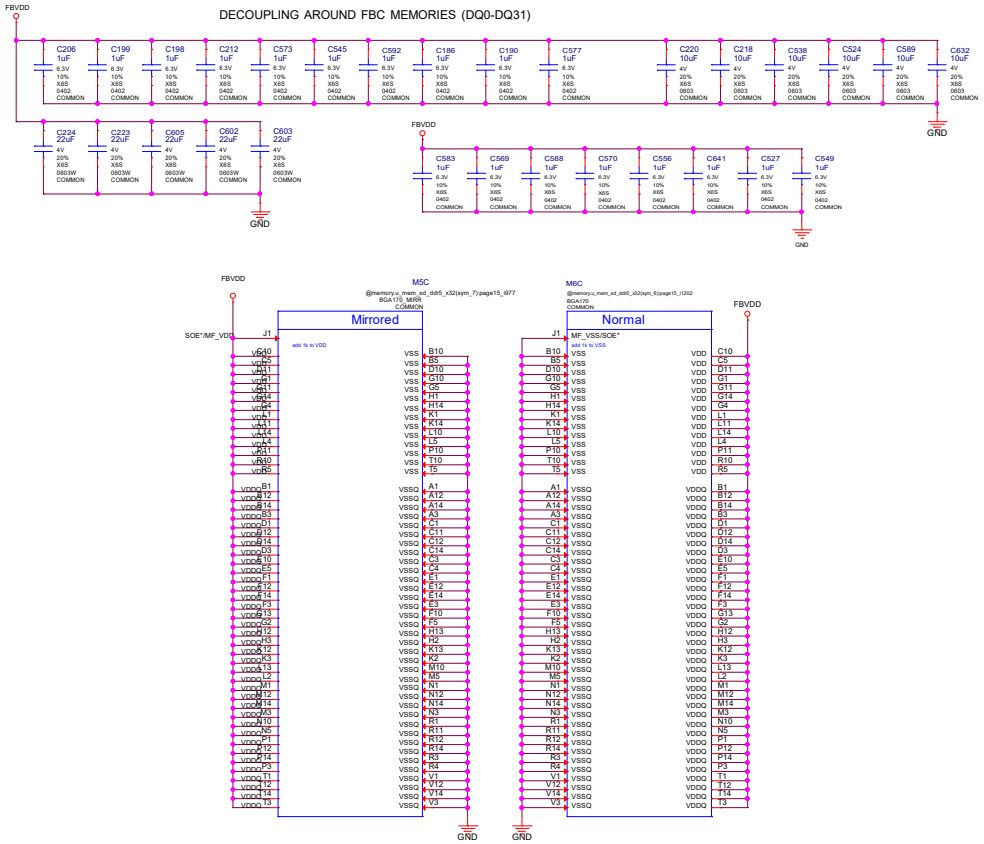
Page13: FRAME BUFFER PARTITION D[31:0]

Page14: FRAME BUFFER PARTITION D[63:32]

Page15: FRAME BUFFER PARTITION C/D DECOUPLING



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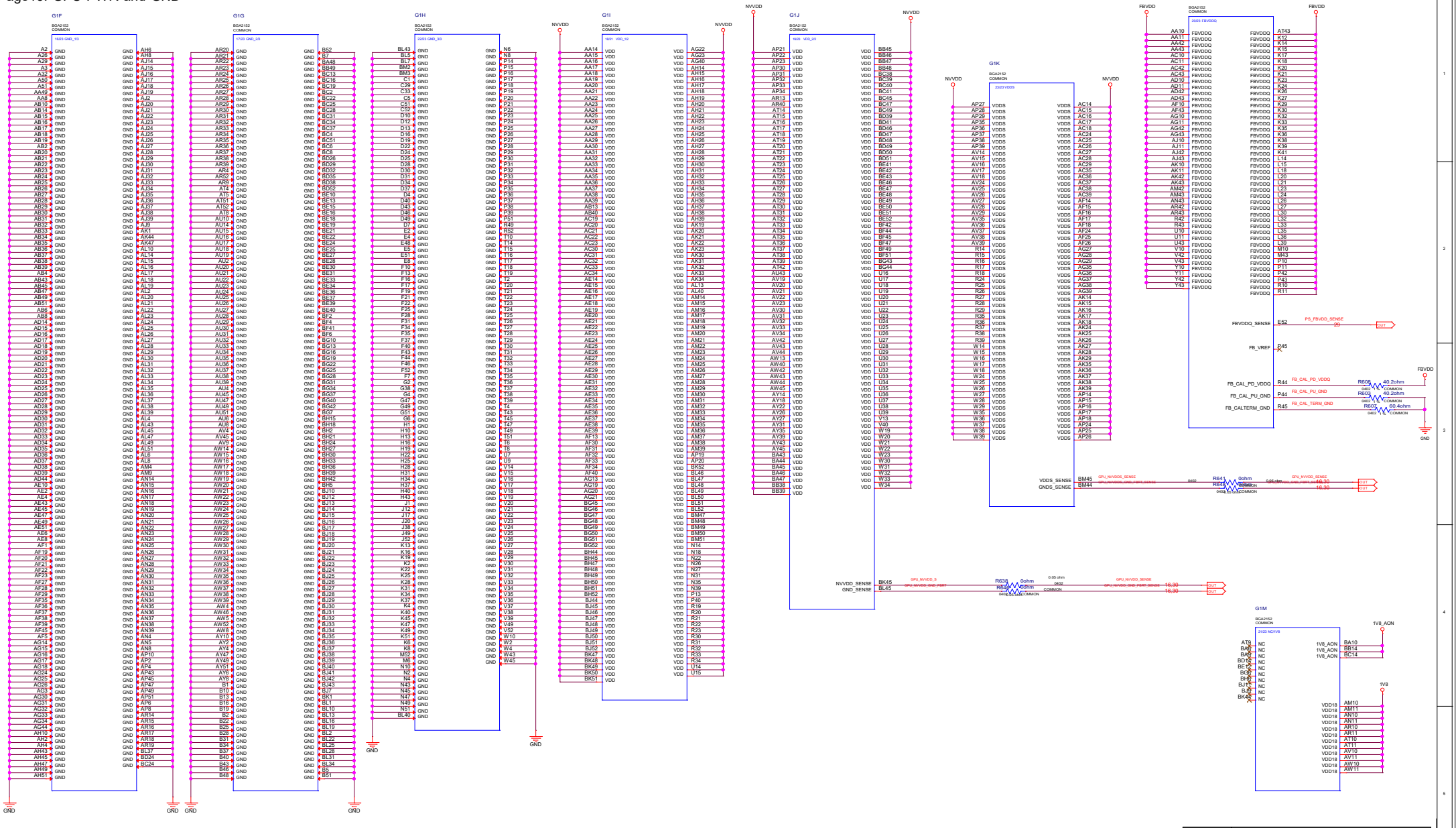
Page16: GPU PWR and GND



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Page17: GPU Decoupling

FBVDD

FBVDD

Partition A — 6x 1uF and 2x 10uF

C734 1uF, C743 1uF, C749 1uF, C791 1uF, C759 1uF, C720 1uF, C807 10uF, C737 10uF

Partition B — 6x 1uF and 2x 10uF

C650 1uF, C648 1uF, C640 1uF, C639 1uF, C651 1uF, C647 1uF, C634 10uF, C630 10uF

Partition C — 6x 1uF and 2x 10uF

C661 1uF, C635 1uF, C644 1uF, C646 1uF, C638 1uF, C642 1uF, C609 10uF, C633 10uF

Partition D — 6x 1uF and 2x 10uF

C721 1uF, C717 1uF, C750 1uF, C760 1uF, C739 1uF, C701 1uF, C683 10uF

C879 10uF, C850 10uF, C834 10uF, C805 10uF, C796 10uF, C732 10uF, C179 10uF, C698 10uF

C11-1067014-W08 C805_67, C11-1067014-W08 C805_67, C11-1067014-W08 C805_67, C11-1067014-W08 C805_67, C11-1067014-W08 C805_67, C11-1067014-W08 C805_67

C531 22uF, C229 22uF, C544 22uF, C869 22uF, C541 22uF, C542 22uF, C543 22uF

NVVDD

NVVDD

C112 330uF COMMON 20% 2V@105degC AL-Polymer 3.5A@105degC,100KHz 0.006ohm SMD_7343

C706 330uF COMMON 20% 2V@105degC AL-Polymer 3.5A@105degC,100KHz 0.006ohm SMD_7343

C771 330uF COMMON 20% 2V@105degC AL-Polymer 3.5A@105degC,100KHz 0.006ohm SMD_7343

C111 330uF COMMON 20% 2V@105degC AL-Polymer 3.5A@105degC,100KHz 0.006ohm SMD_7343

C861 47uF, C842 47uF, C846 22uF, C873 22uF, C812 22uF, C832 22uF, C761 10uF, C718 10uF

C696 10uF, C738 10uF, C697 10uF, C793 10uF, C716 10uF, C682 10uF, C776 10uF, C763 10uF, C779 10uF

C676 1uF, C748 1uF, C809 1uF, C710 1uF, C799 1uF, C755 1uF, C767 1uF, C679 1uF, C766 1uF, C811 1uF

C714 1uF, C762 1uF, C665 1uF, C667 1uF, C689 1uF, C723 1uF, C711 1uF, C680 1uF, C678 1uF, C768 1uF

C765 1uF, C754 1uF, C798 1uF, C677 1uF, C688 1uF, C713 1uF, C785 1uF, C731 1uF, C800 1uF, C709 1uF

C687 1uF, C666 1uF, C675 1uF, C722 1uF, C724 1uF, C787 1uF, C797 1uF, C786 1uF, C810 1uF, C735 1uF

C636 1uF, C637 1uF, C692 1uF, C783 1uF, C802 1uF, C707 1uF, C764 1uF, C715 1uF, C702 1uF

NVVDD

NVVDD

C91 330uF COMMON 20% 2V@105degC AL-Polymer 3.5A@105degC,100KHz 0.006ohm SMD_7343

C859 47uF, C806 10uF, C671 10uF, C752 10uF, C727 10uF

C753 1uF, C808 1uF, C736 1uF, C751 1uF, C758 1uF, C669 1uF, C719 1uF, C774 1uF

C668 1uF, C662 1uF, C690 1uF, C726 1uF, C725 1uF, C691 1uF, C660 1uF, C784 1uF

1V8_AON

1V8_AON

place 1 0.1uF cap near BA10

C851 4.7uF, C817 1uF, C816 0.1uF, C916 0.1uF

place 1 0.1uf cap for BB14 and BC14 to share

1V8_MAIN

1V8

C853 0.1uF, C828 0.1uF, C829 0.1uF

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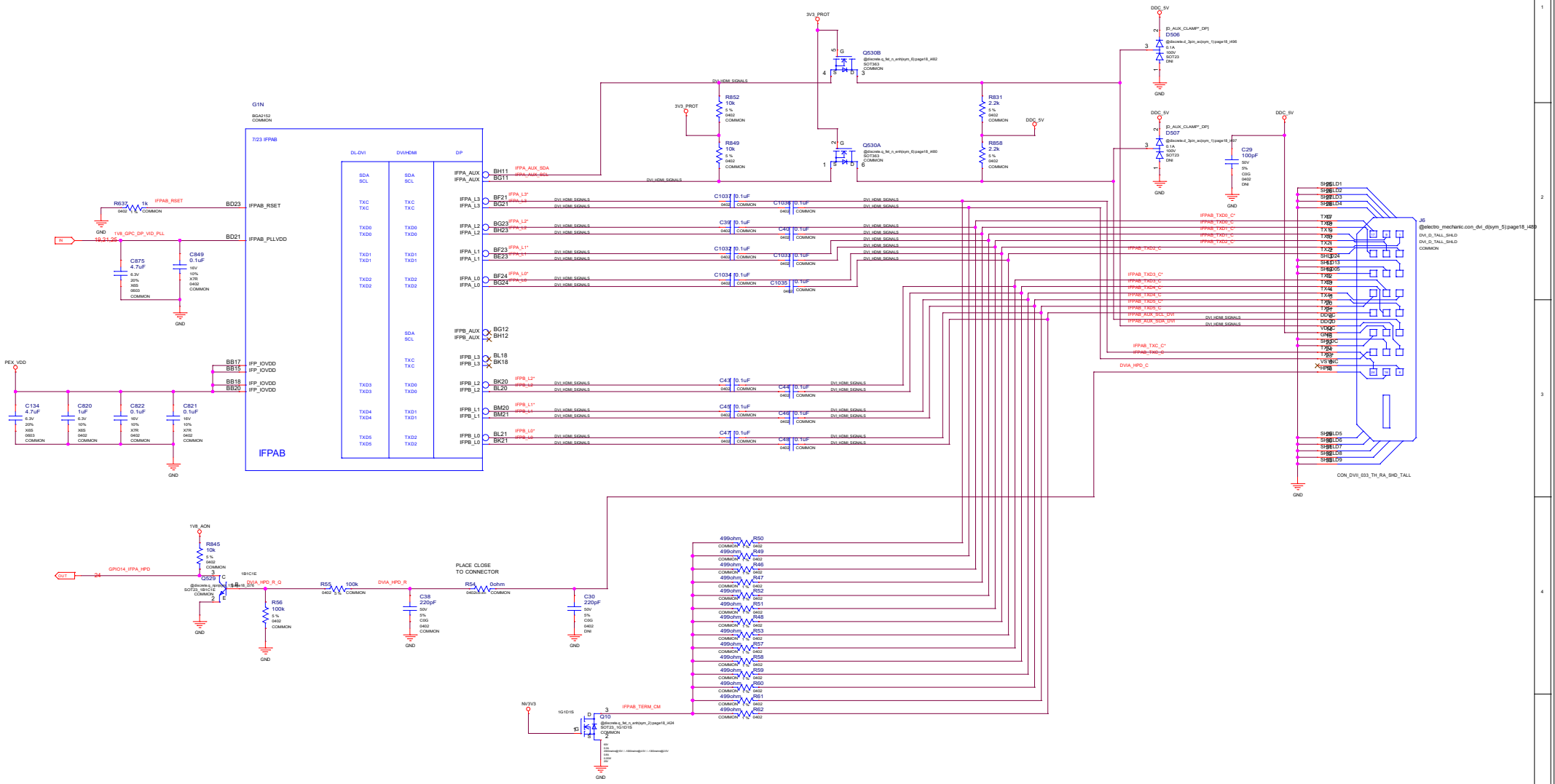
Page18: IFPAB DVI-D-DL



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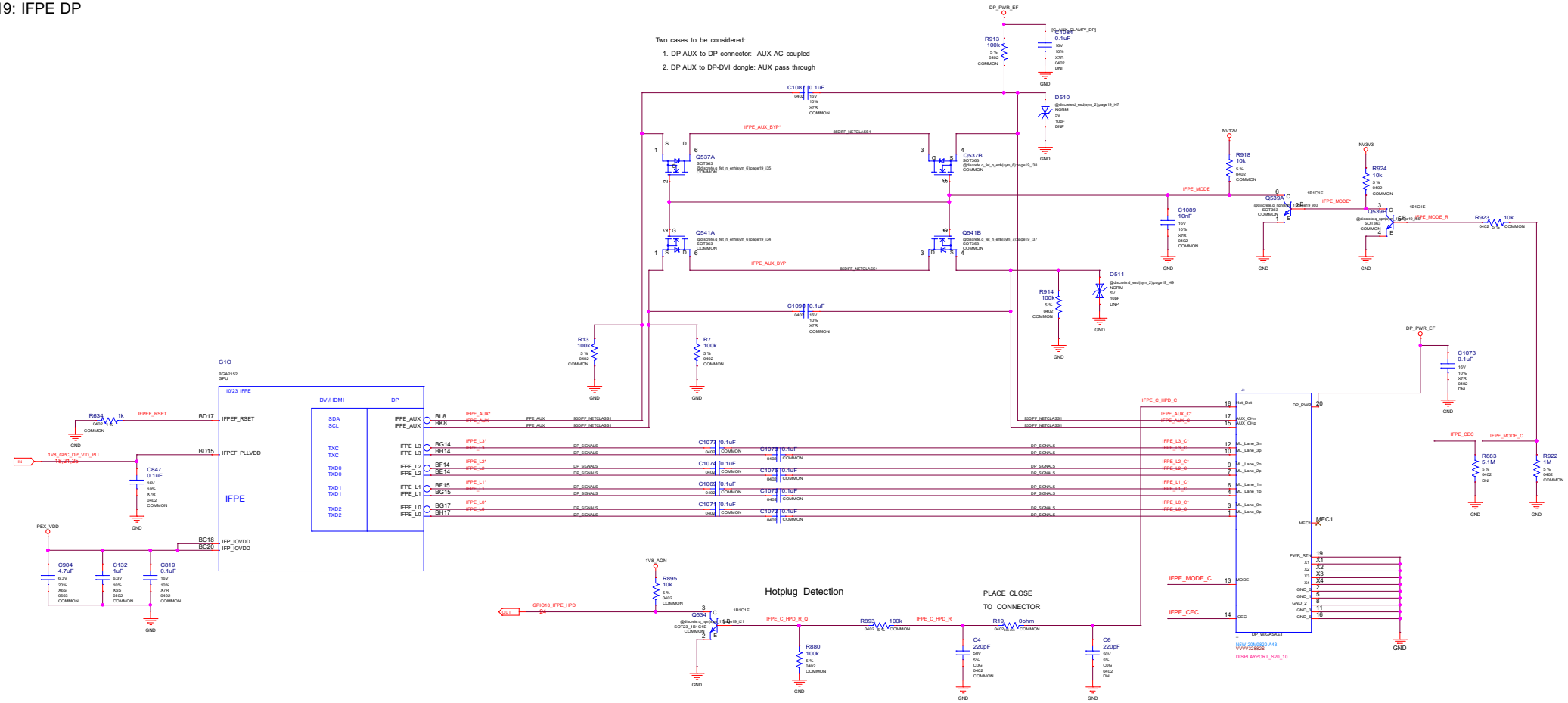
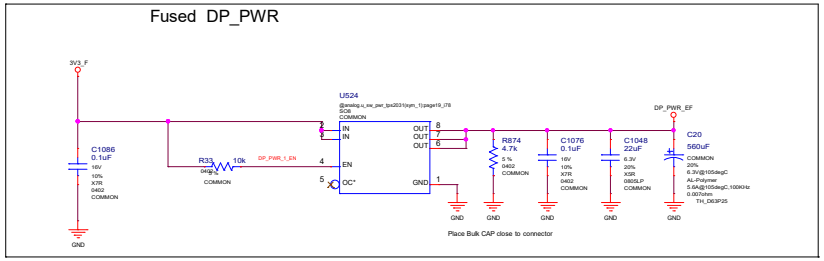
Page19: IFPE DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



Fused DP_PWR



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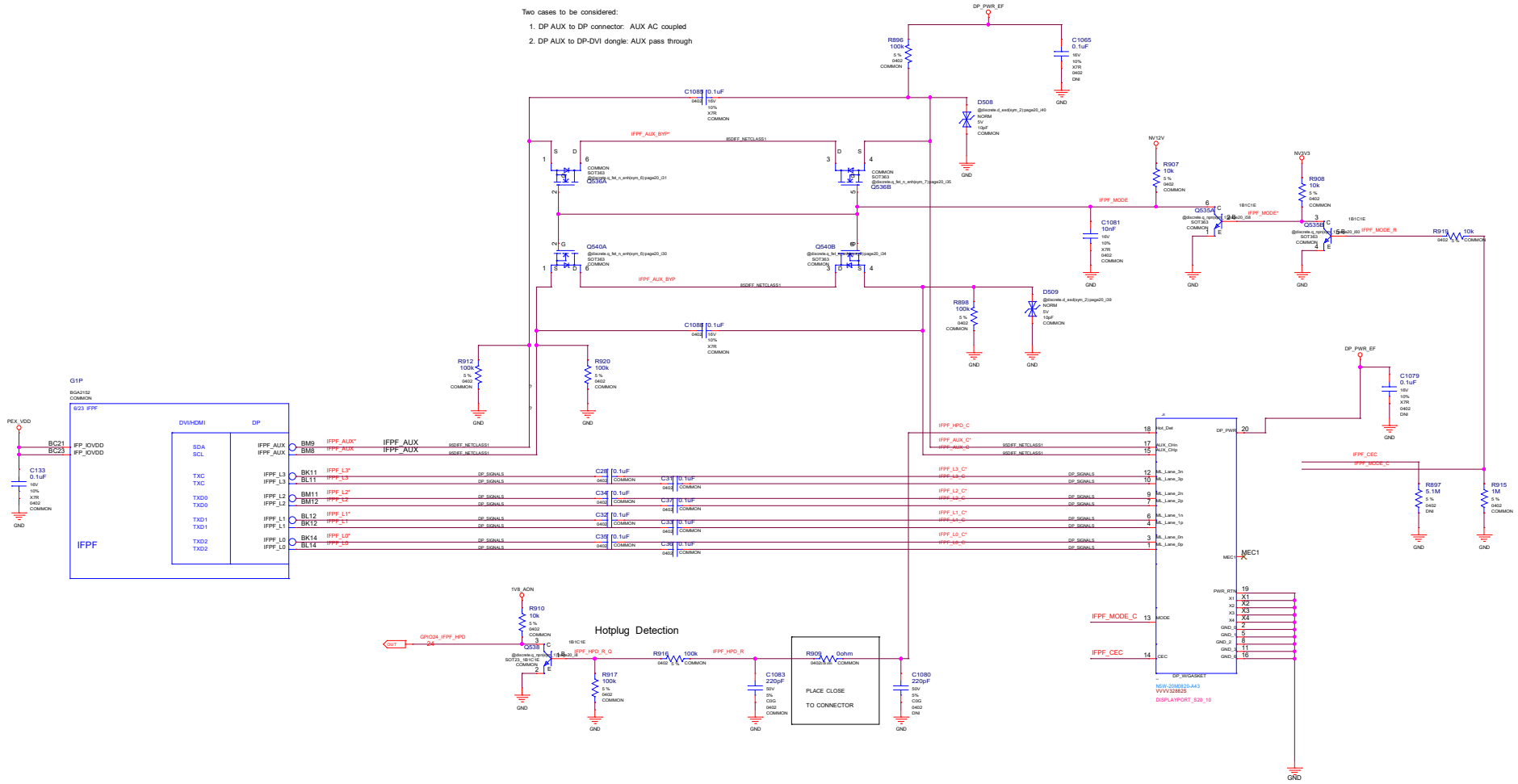
Page 20: IFPF DP



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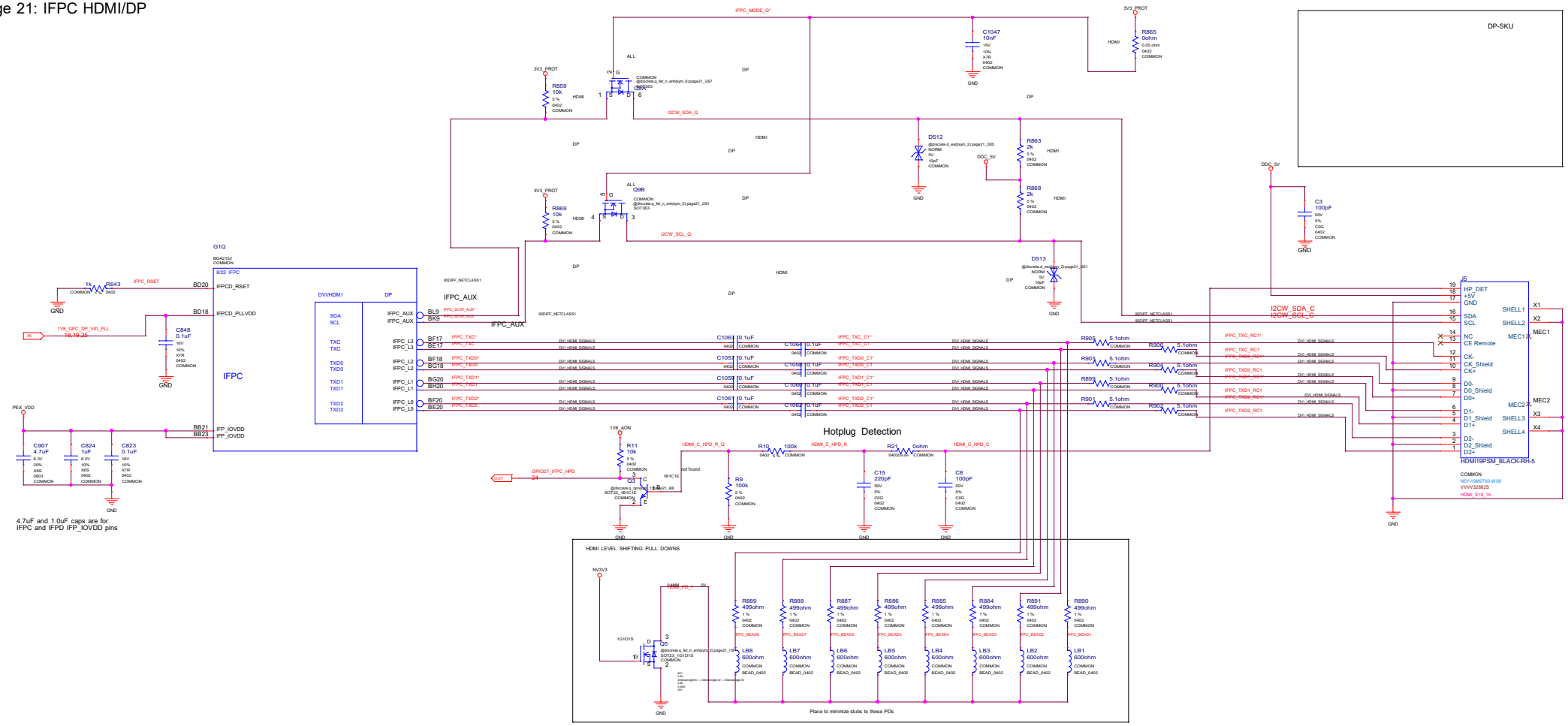
Page 21: IFPC HDMI/DP



Fused DP_PWR

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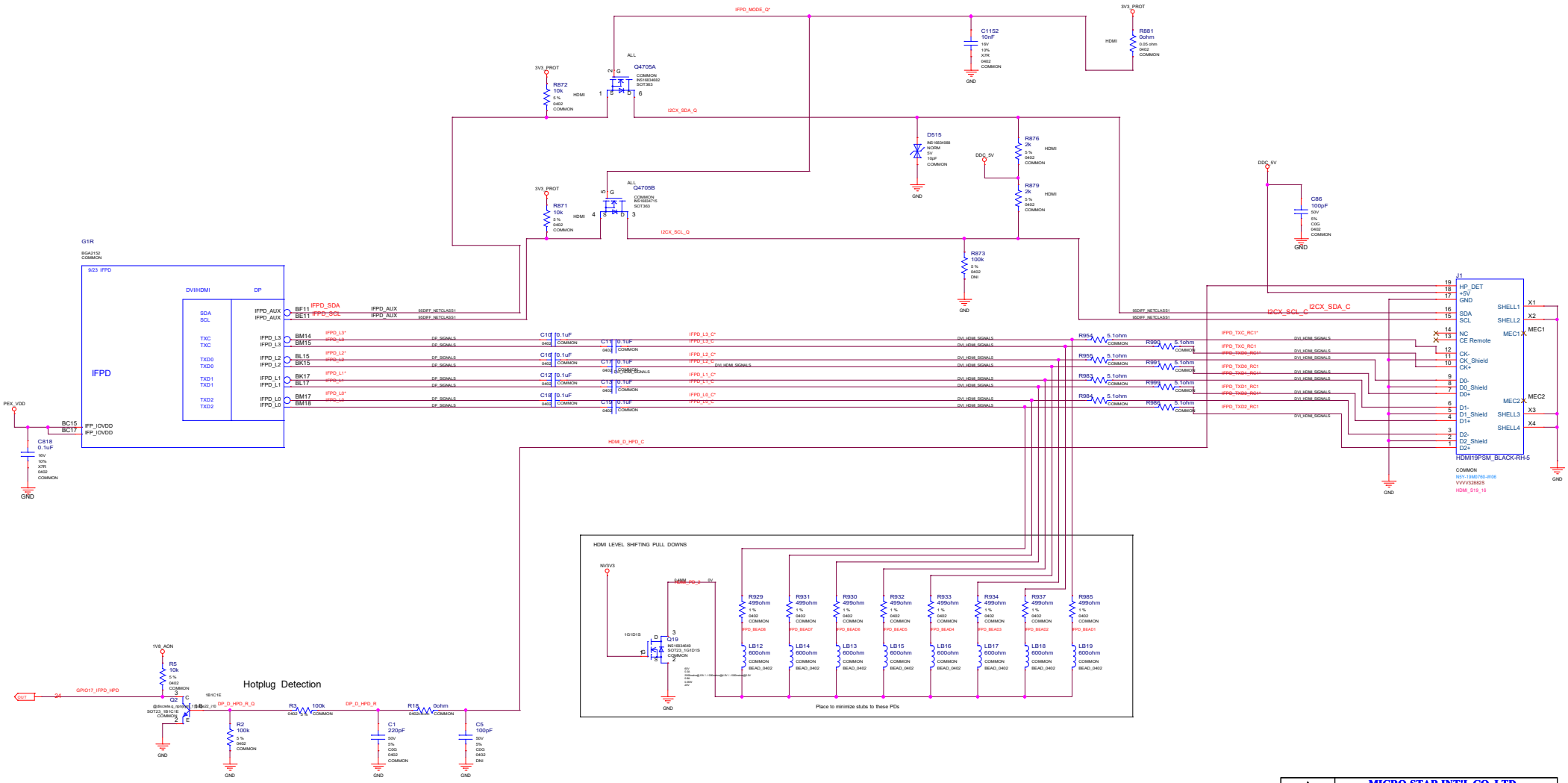
Page 22: IFPD DP



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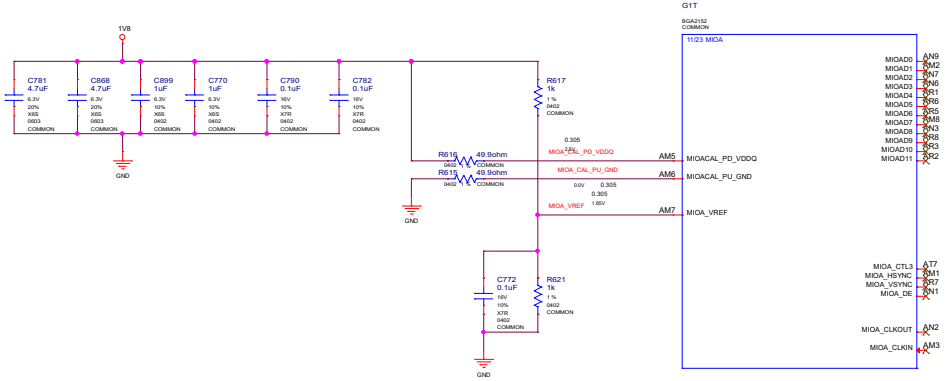
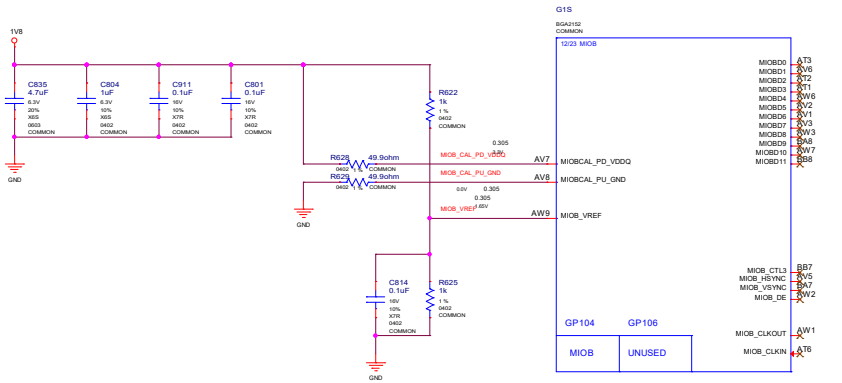
Page 23: MIOA/B Interface and Frame Lock



Pad Overlap R1042 & R1043



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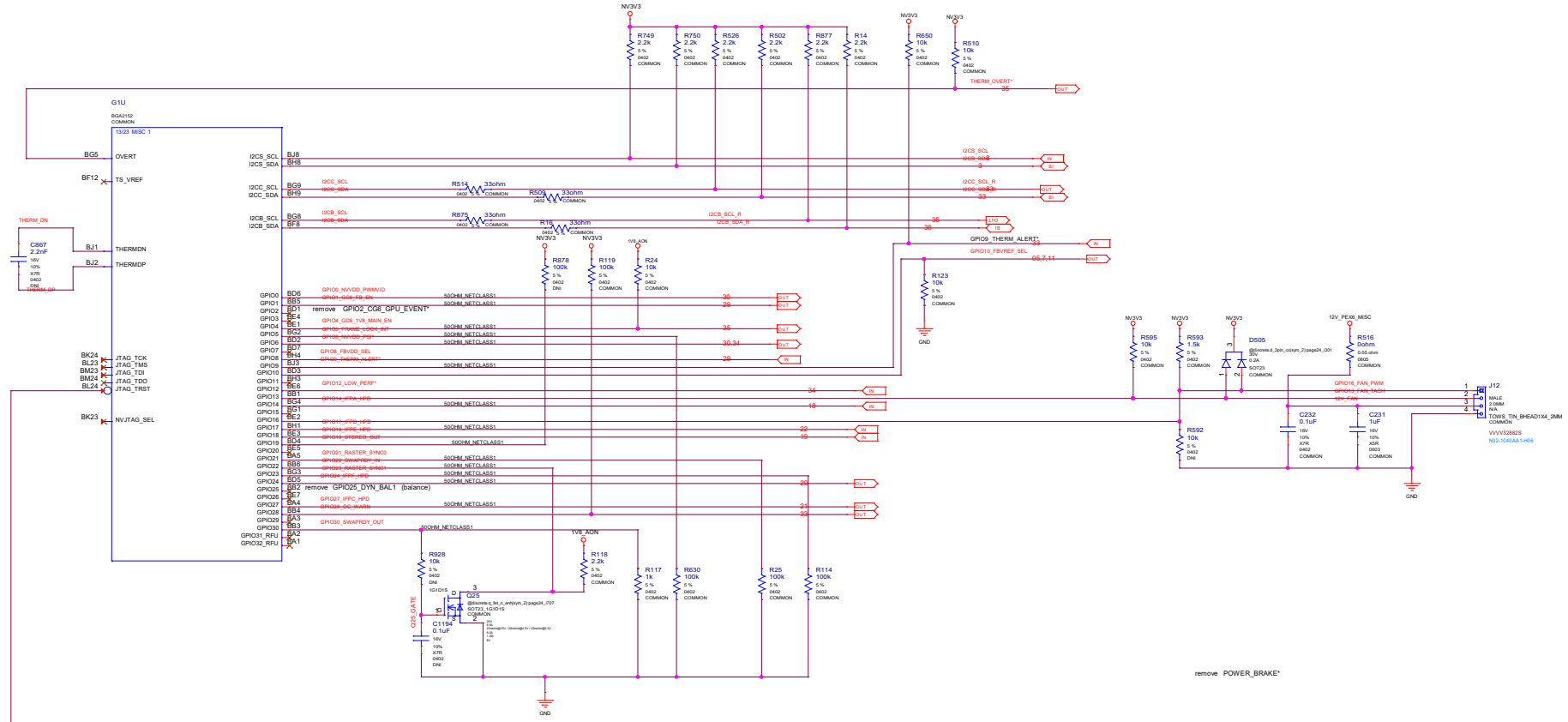
Page 24: MISC1: Fan, Thermal, JTAG, GPIO



STEREO

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Page25: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

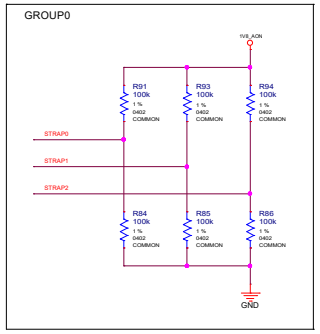
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

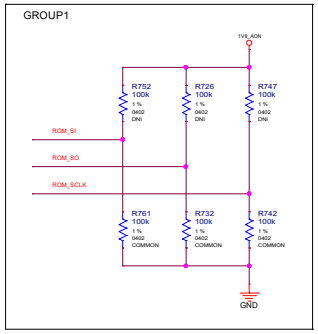
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

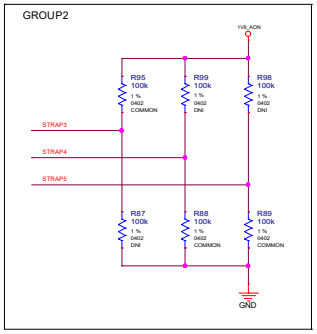
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

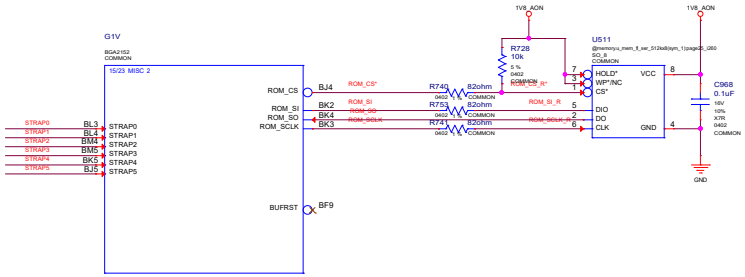
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

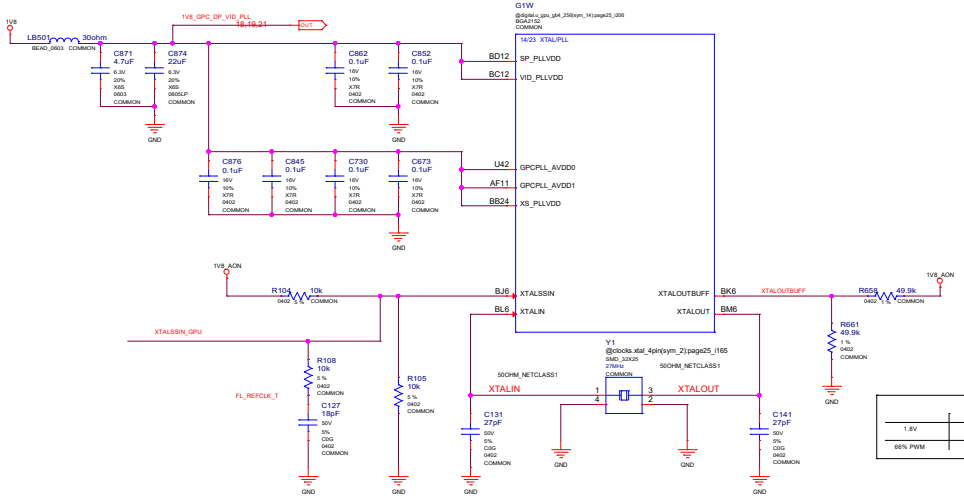






CFG[3:0]	Config Width	Vendor
0000	256Mx32 256-bit	Samsung
0001	256Mx32 256-bit	Micron
0010	256Mx32 256-bit	Hynix
0011	Reserved	
0100	Reserved	
0101	Reserved	
0110	Reserved	
0111	Reserved	





XTALOUTBUFF		
1.8V	0.9V	0V
66% PWM	33% PWM	DISABLED (100%)

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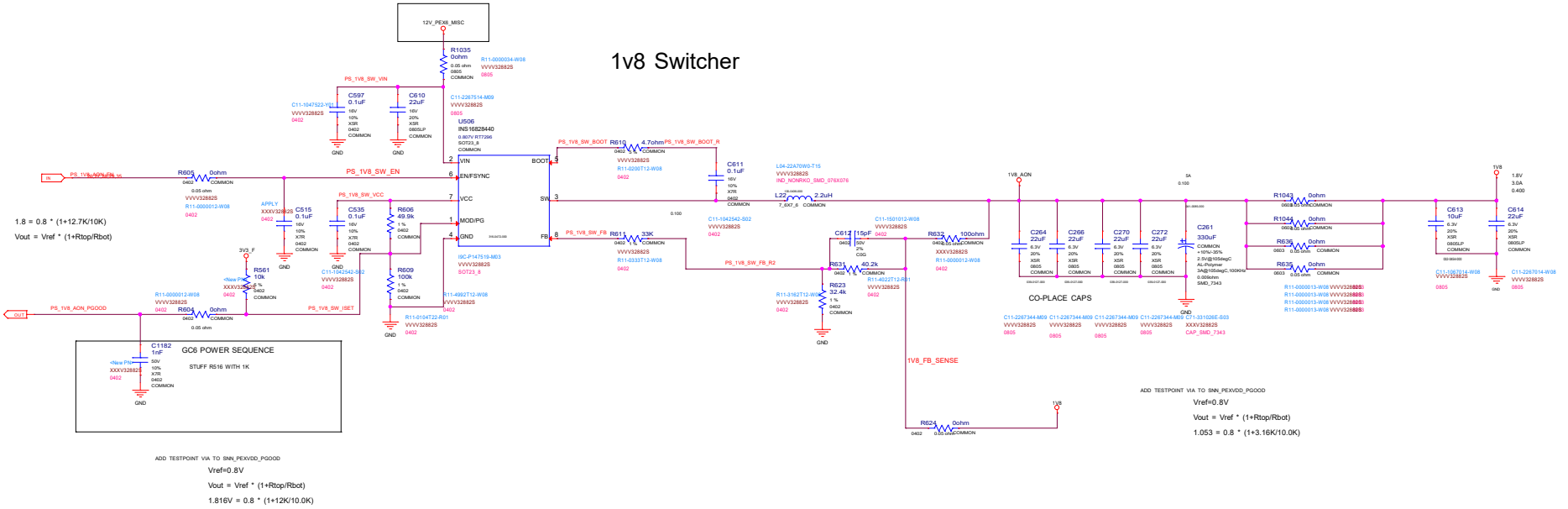
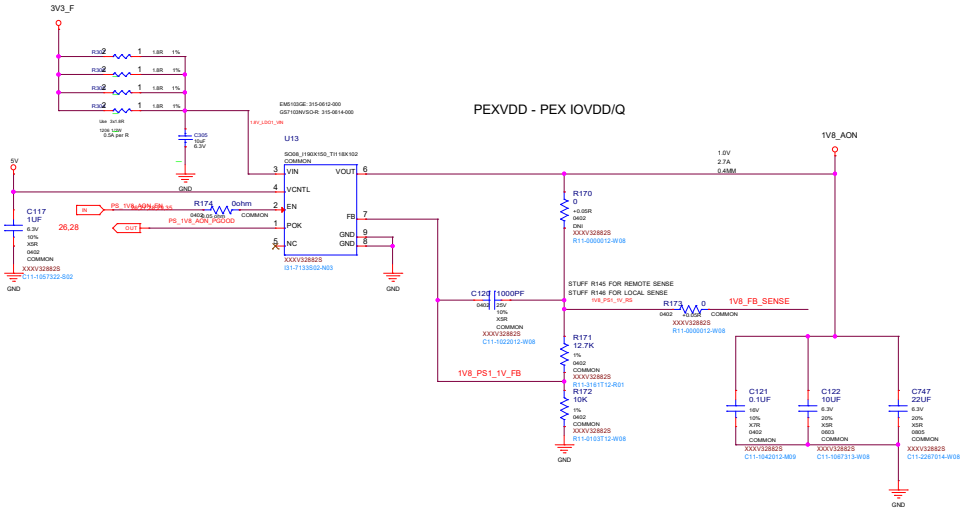
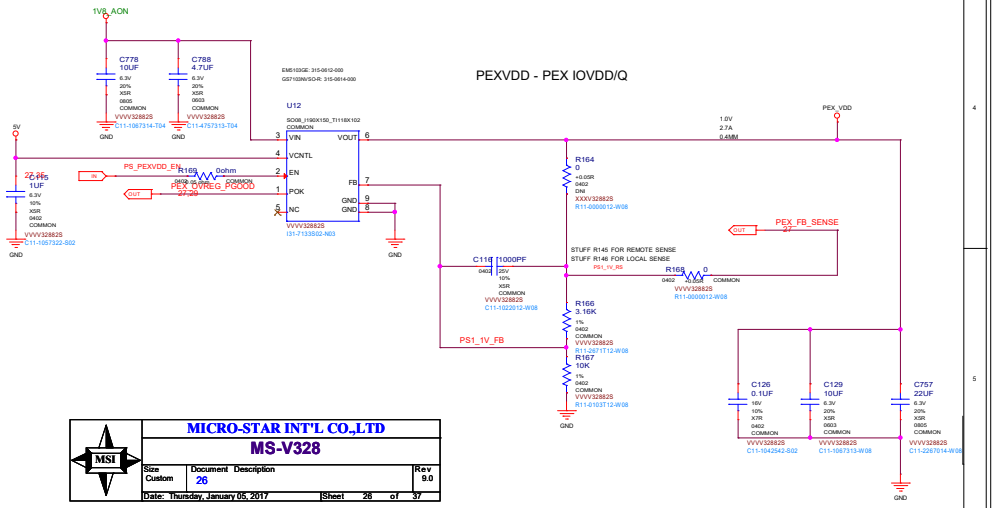
Page26: PS: 1V8 PLL, 1V8_AON







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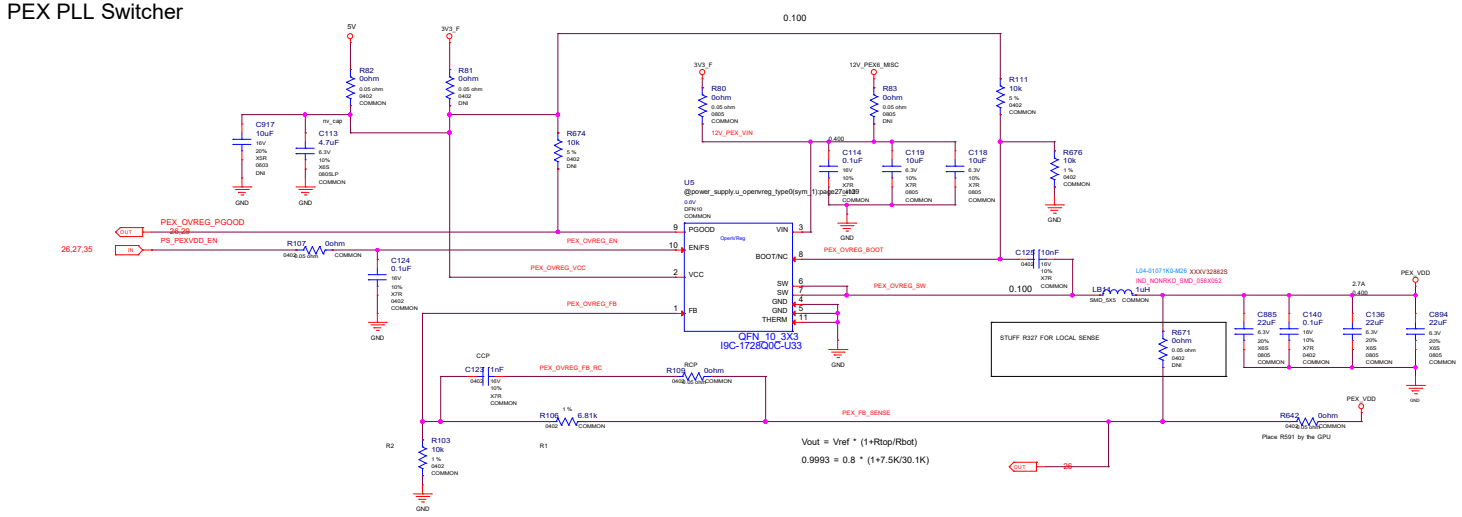
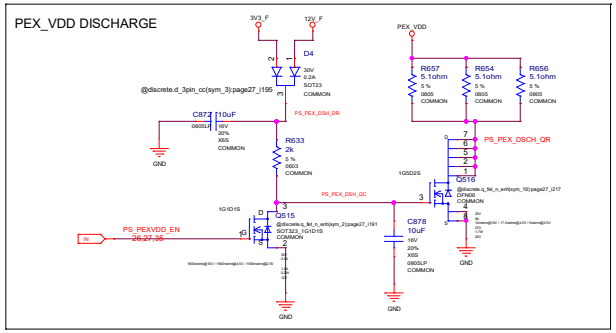
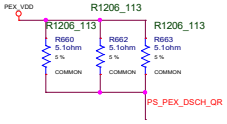
Page27: PS: 5V SWITCHER,PEX VDD

PEX PLL Switcher

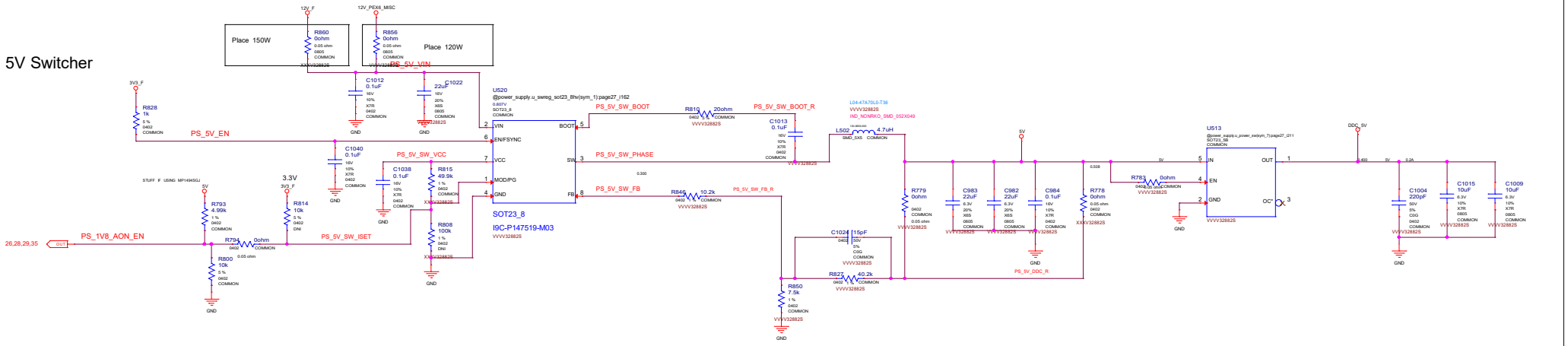


PEX_VDD DISCHARGE





5V Switcher



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MS-V328 17ci203		
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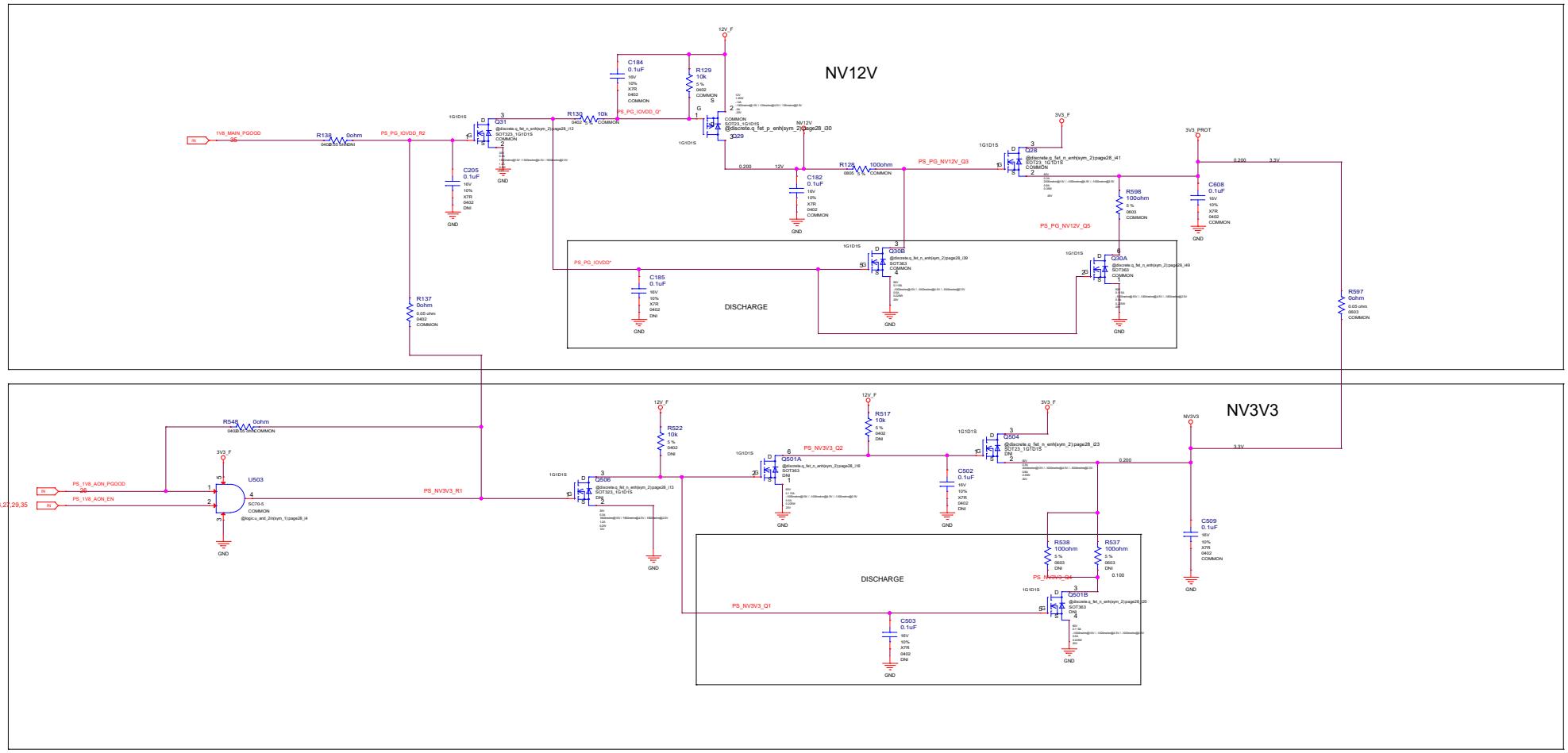

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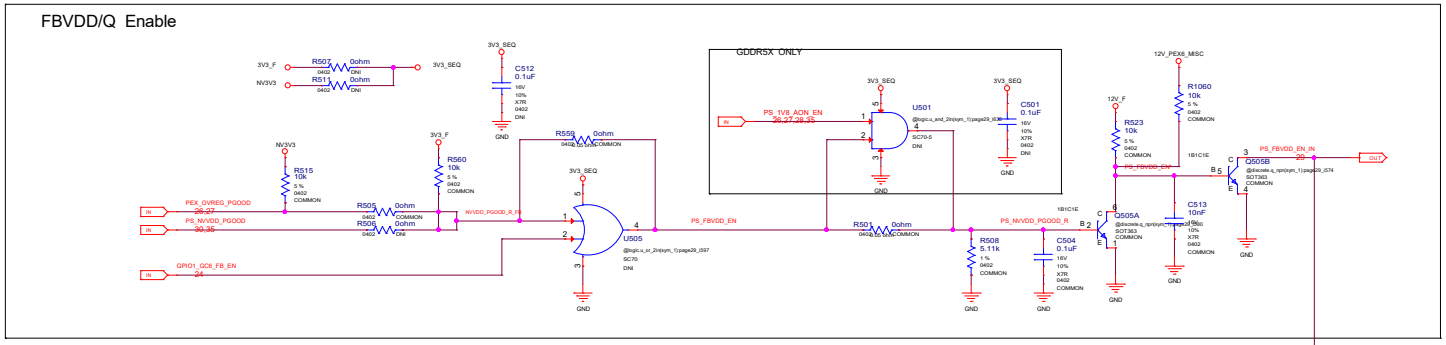
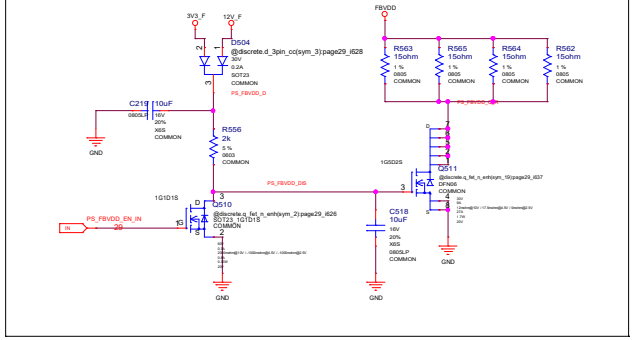
Page29: PS: FBVDDQ

NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
FBVDD			

FBVDD/Q Enable

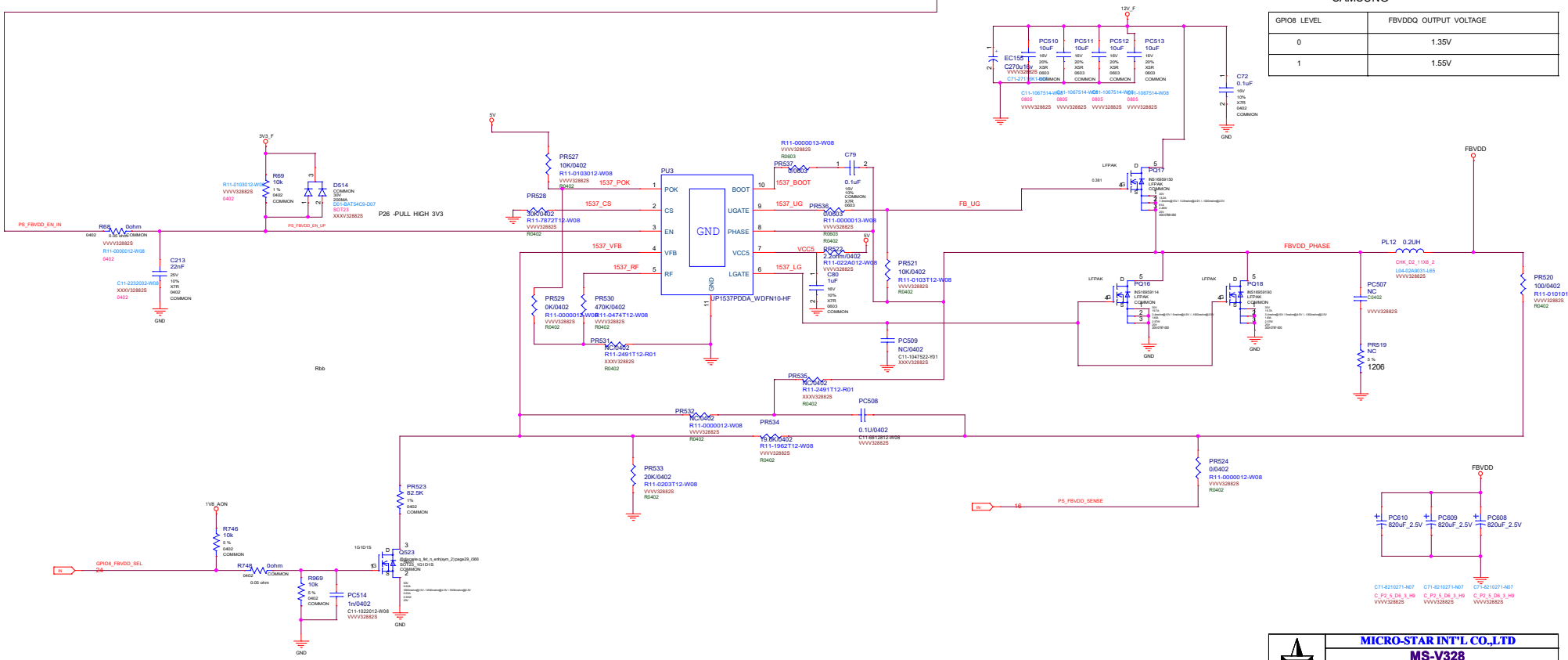


FBVDD DISCHARGE



SAMSUNG

GPIO8 LEVEL	FBVDDQ OUTPUT VOLTAGE
0	1.35V
1	1.55V



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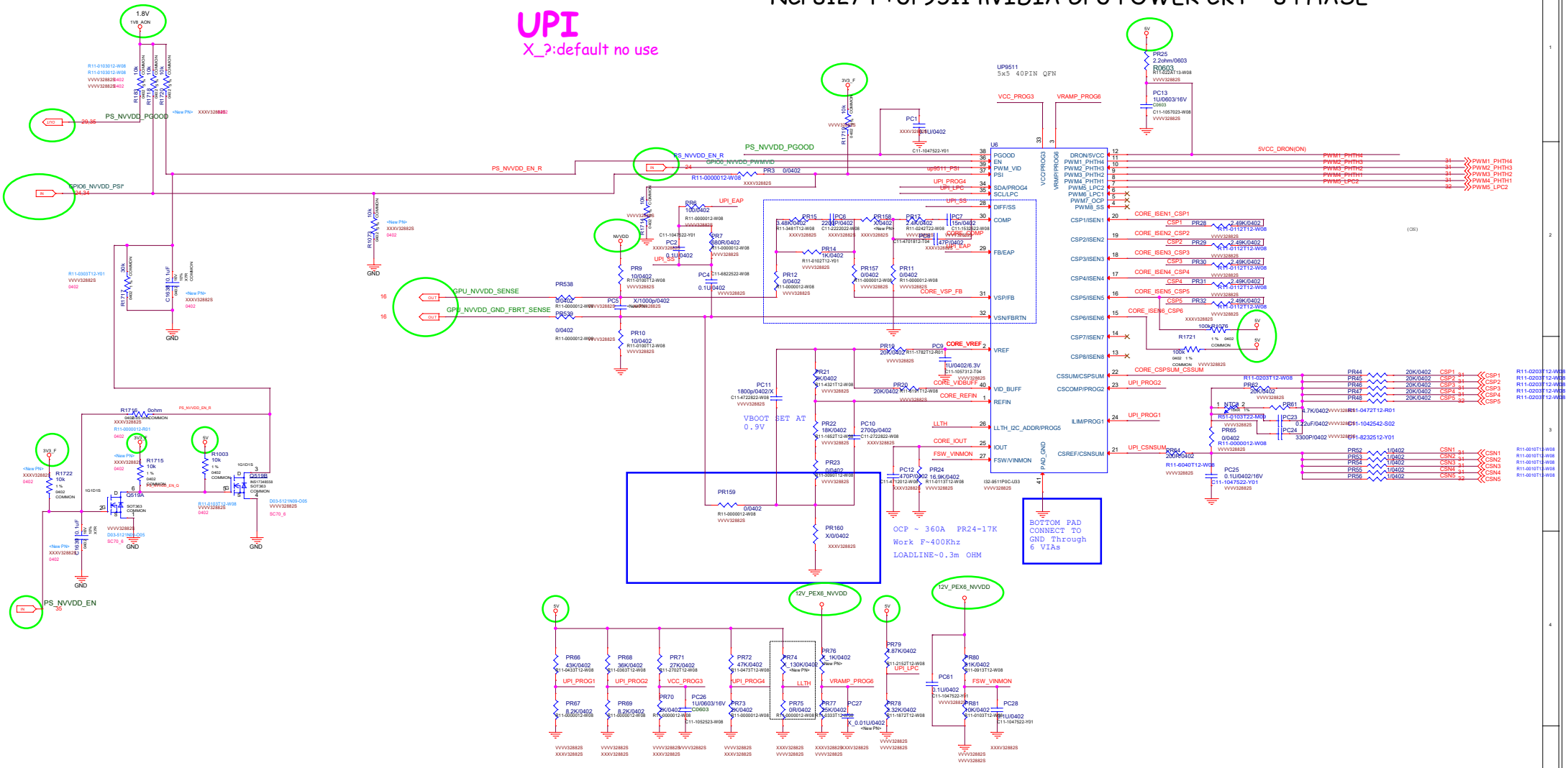
Page30: PS: NVVDD Controller

NCP81274 +UP9511 nVIDIA GPU POWER CKT - 8 PHASE



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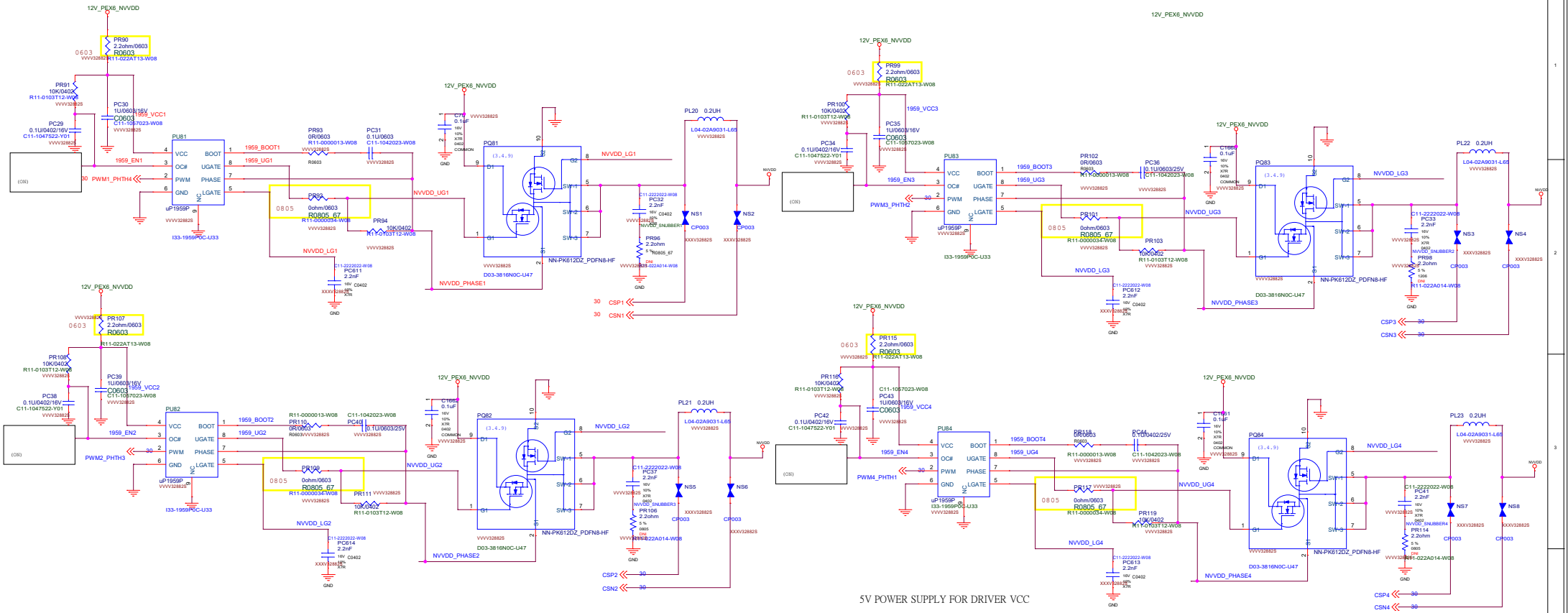
Pgae 31:NVVDD/PHASE1_4



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MS-V328		
Size: Custom	Document Description: NVVDD/PHASE1_2	Rev: 9.0
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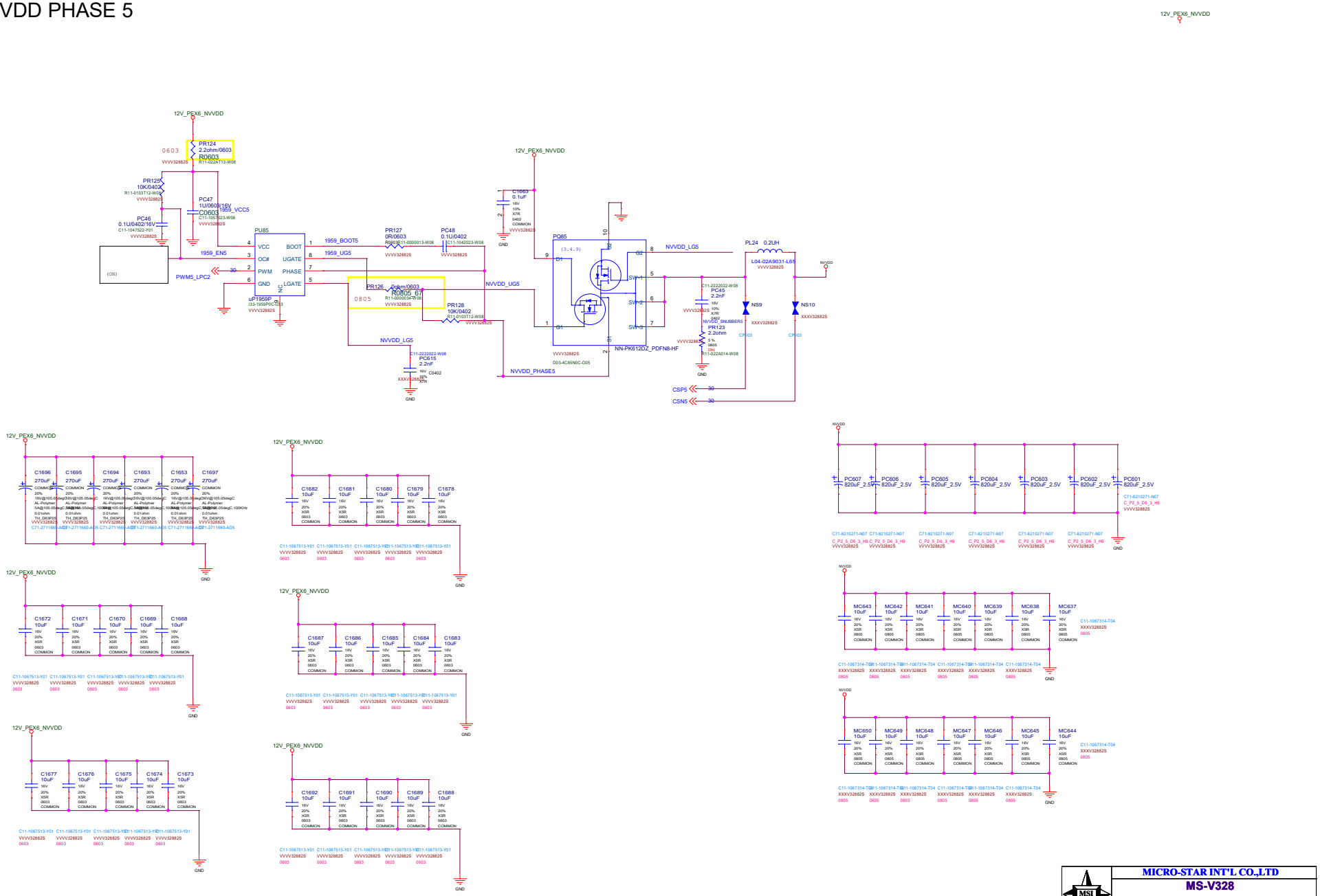
Page32: PS: NVVDD PHASE 5



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V328	
Size: Custom	Document Description: NVVDD/PHASE3_4	Rev: 9.0
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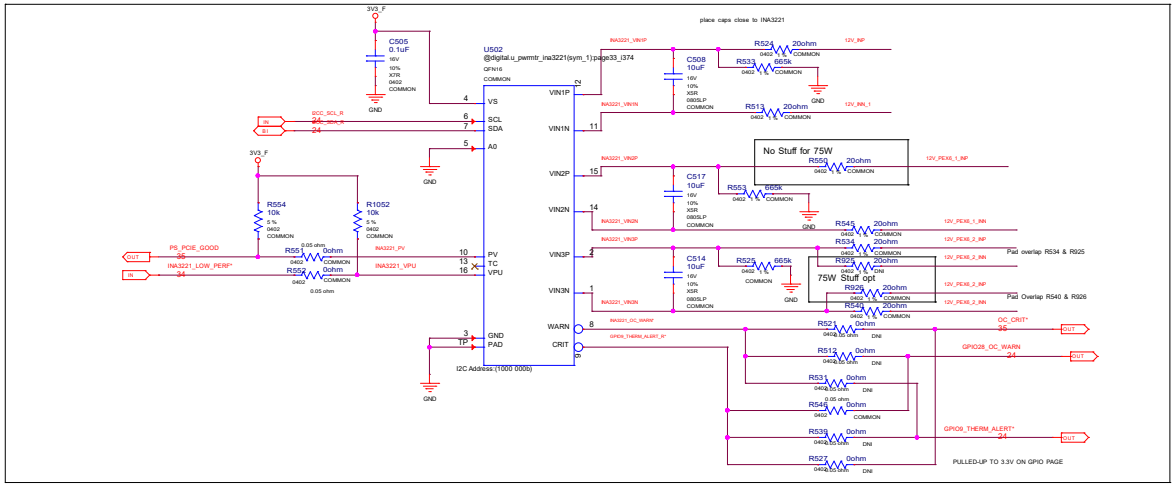
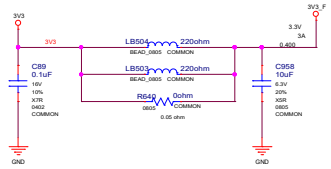
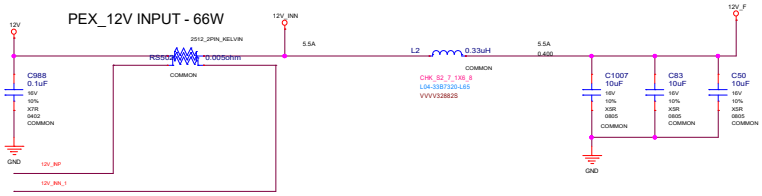
Page33: PS: Inputs, Filtering, and Monitoring



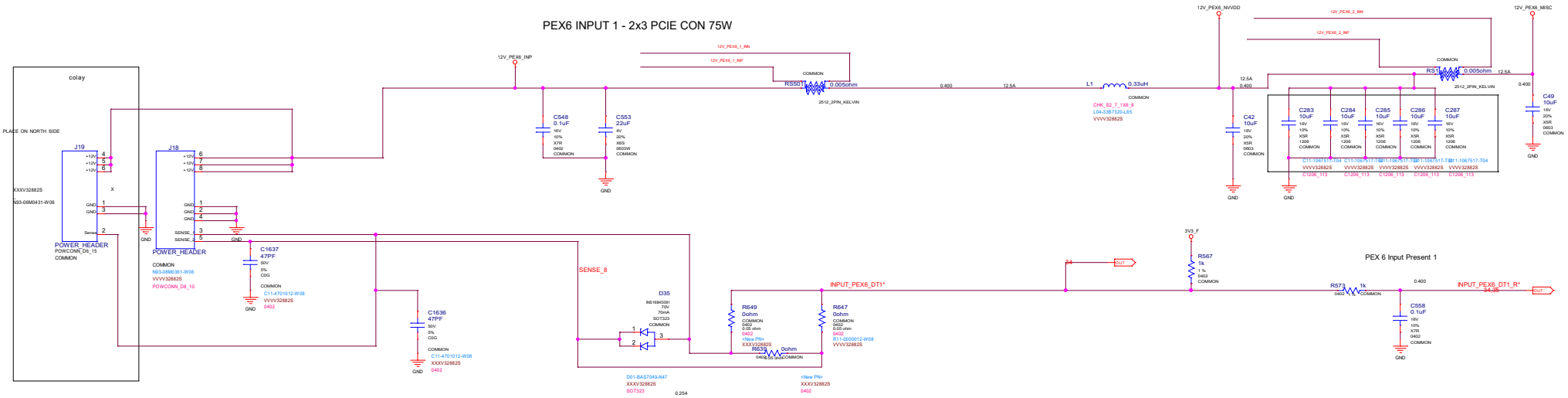
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



PEX6 INPUT 1 - 2x3 PIECE CON 75W



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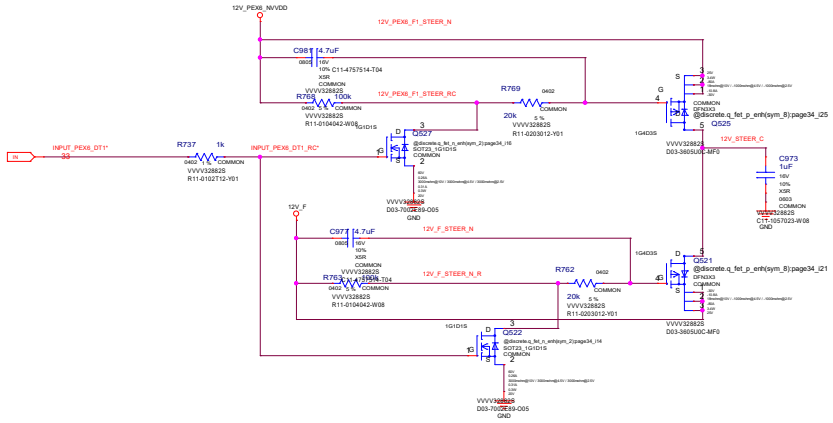
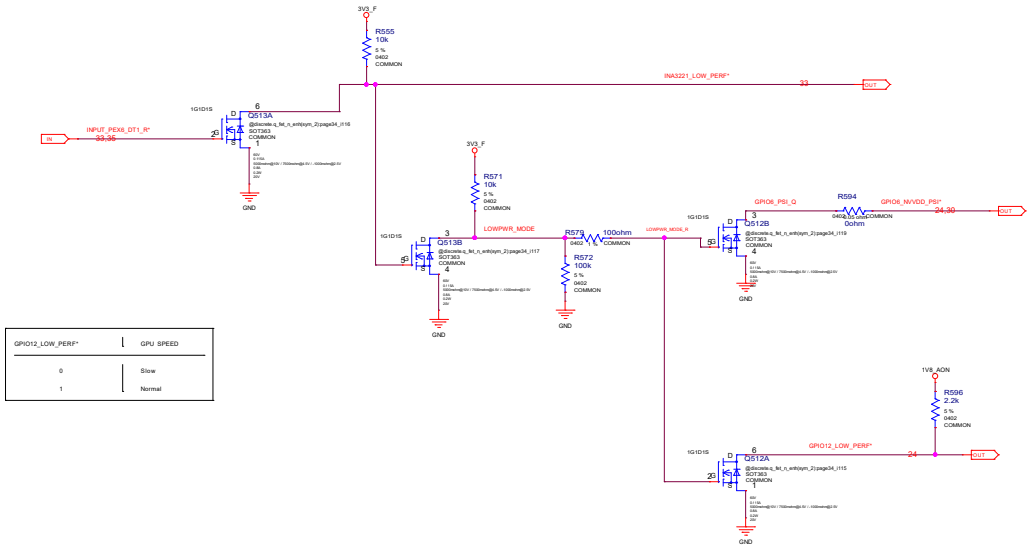
Page34: PS: 12V Current Steering, PSI Control, and LED

12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA



PEX Input - Power Level/PSI* Control



GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

GeForce Logo LED

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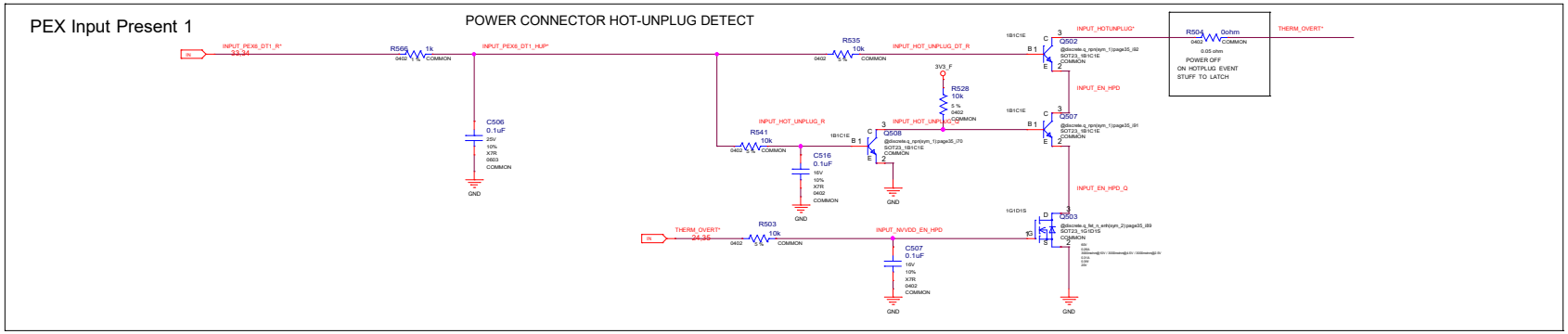
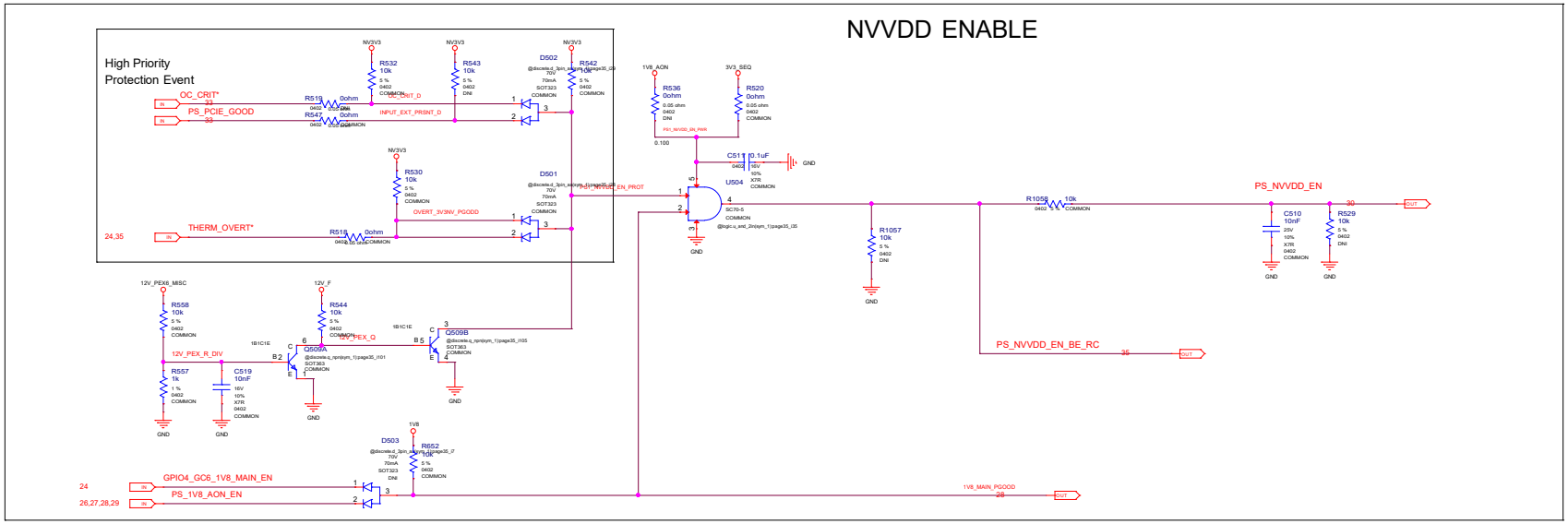
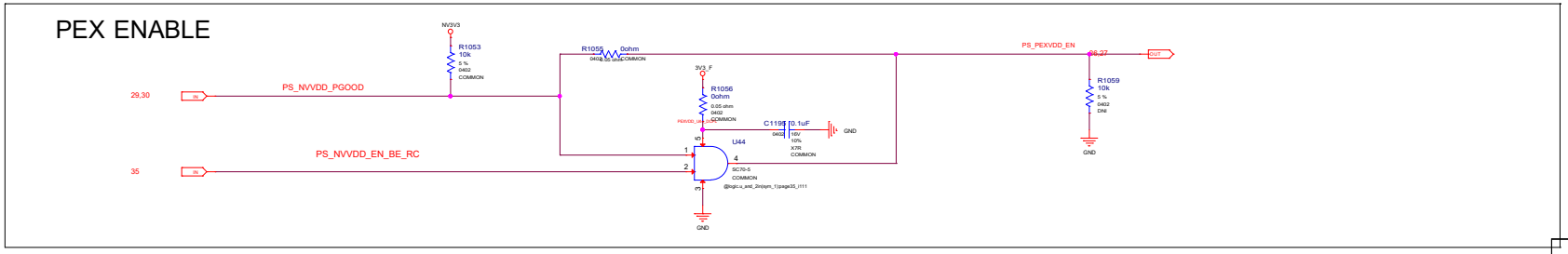
Page37: PS: Shutdown and Sequencing







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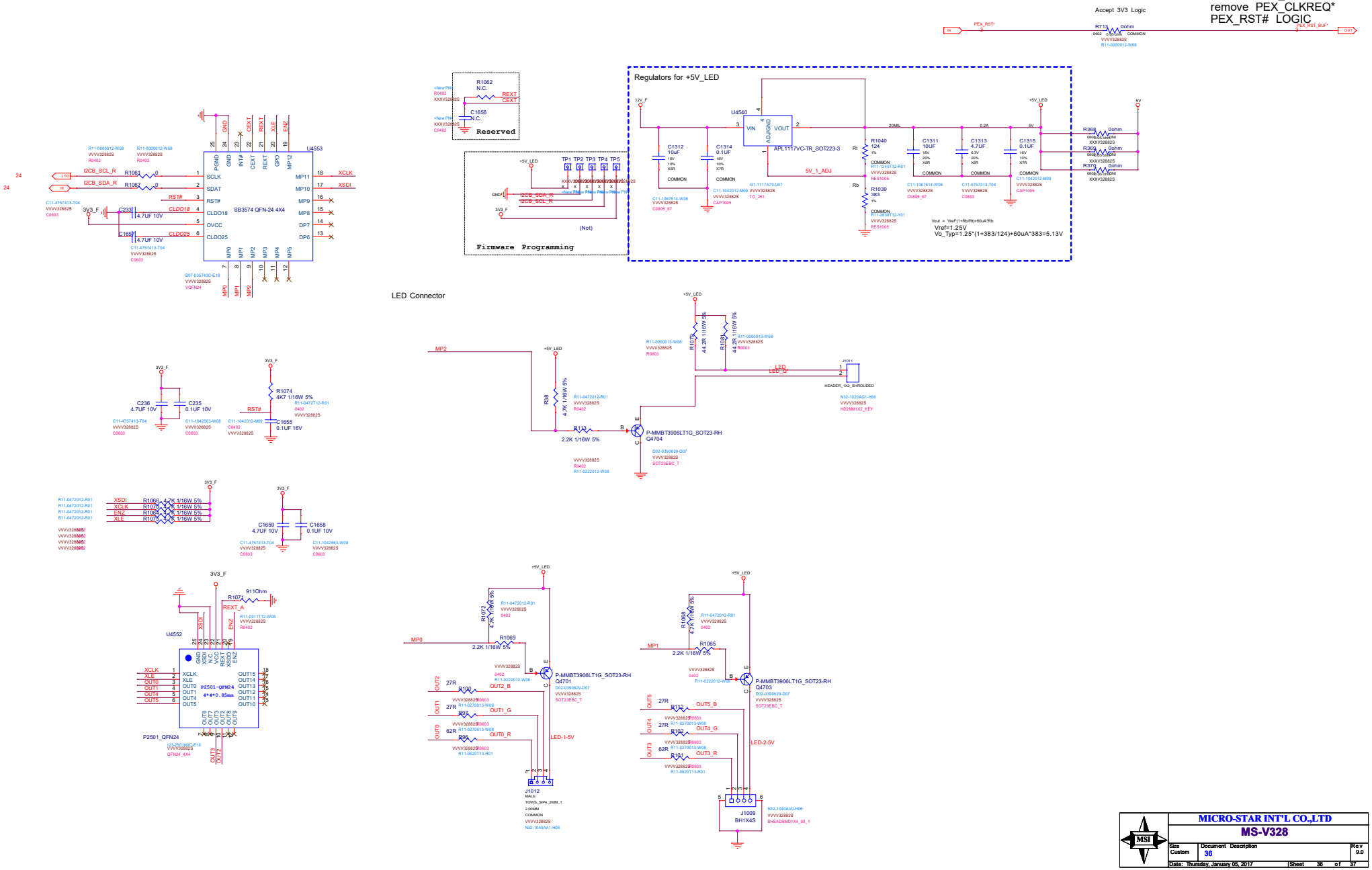
Page38: LED

remove GC6 FB ENABLE
remove GPU_EVENT*
remove PEX_CLKREQ*
PEX_RST# LOGIC



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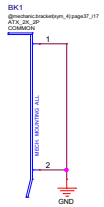
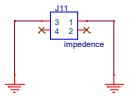
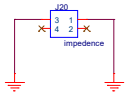
Page40: MECH

Brackets:





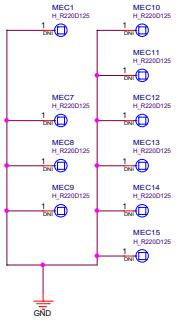


COMMON
VVVV32882S
PD0-0V32890-T53

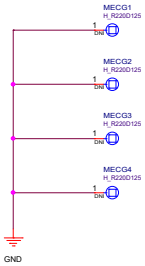
HDMI_FEE

HDMI_FEE
COMMON
VVVV32882S
Y01-RHDMI03-000

Mechanical Holes Symbol



GPU Stiffner



HDMI SC

MEC_SCREW_HEX_JACK
COMMON

VVVV32882S
E43-1303004-P65

HDMI SC1

MEC_SCREW_HEX_JACK
COMMON

VVVV32882S
E43-1303004-P65

PCIESLOT

MEC_SCREW_HEX_JACK
COMMON

VVVV32882S
E24-V3200-10-P09

FAN1

MEC_SCREW_HEX_JACK
COMMON

VVVV32882S
E32-0405262-A87

FAN2

MEC_SCREW_HEX_JACK
COMMON

VVVV32882S
OE3-V303002

FAN3

MEC_SCREW_HEX_JACK
COMMON

VVVV32882S
OE3-V328101

MEC6

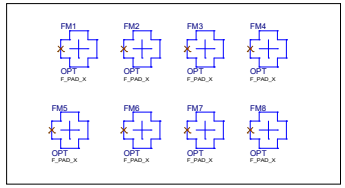
MEC_SCREW_HEX_JACK
COMMON

VVVV32882S
E42-5047006-C67

MEC19

MEC_SCREW_HEX_JACK
COMMON

VVVV32882S
E42-5047006-C67



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