PG410 A01

GP106 8GB/4GB GDDR5, 256b, 256Mx32/128MX32
Tall DVI-D + DP + DP + HDMI/DP + DP

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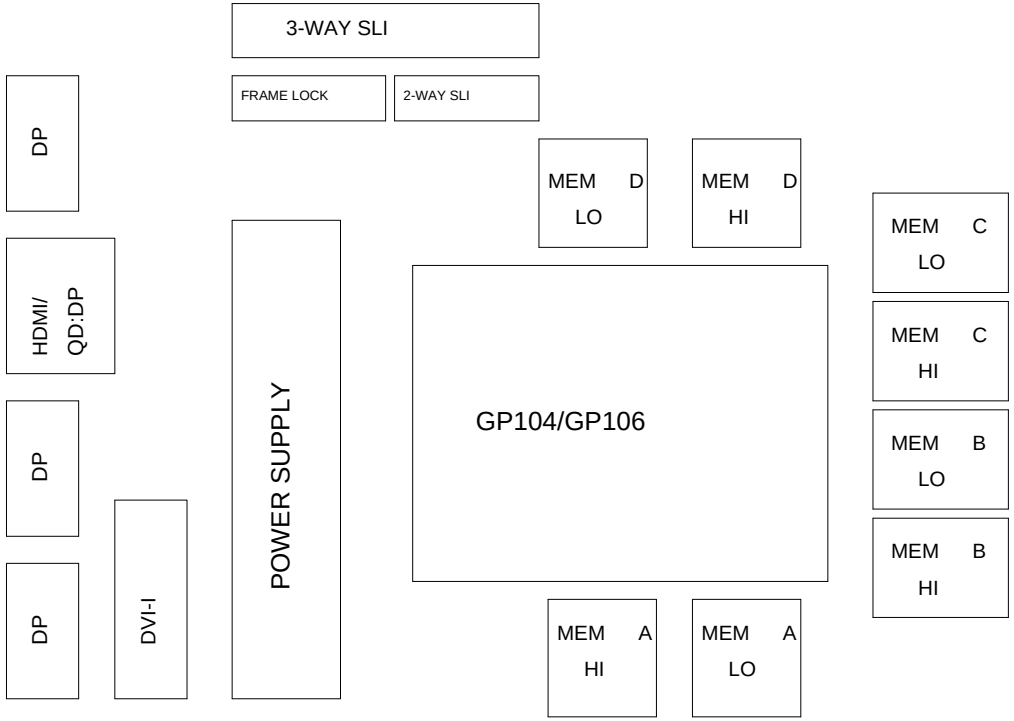
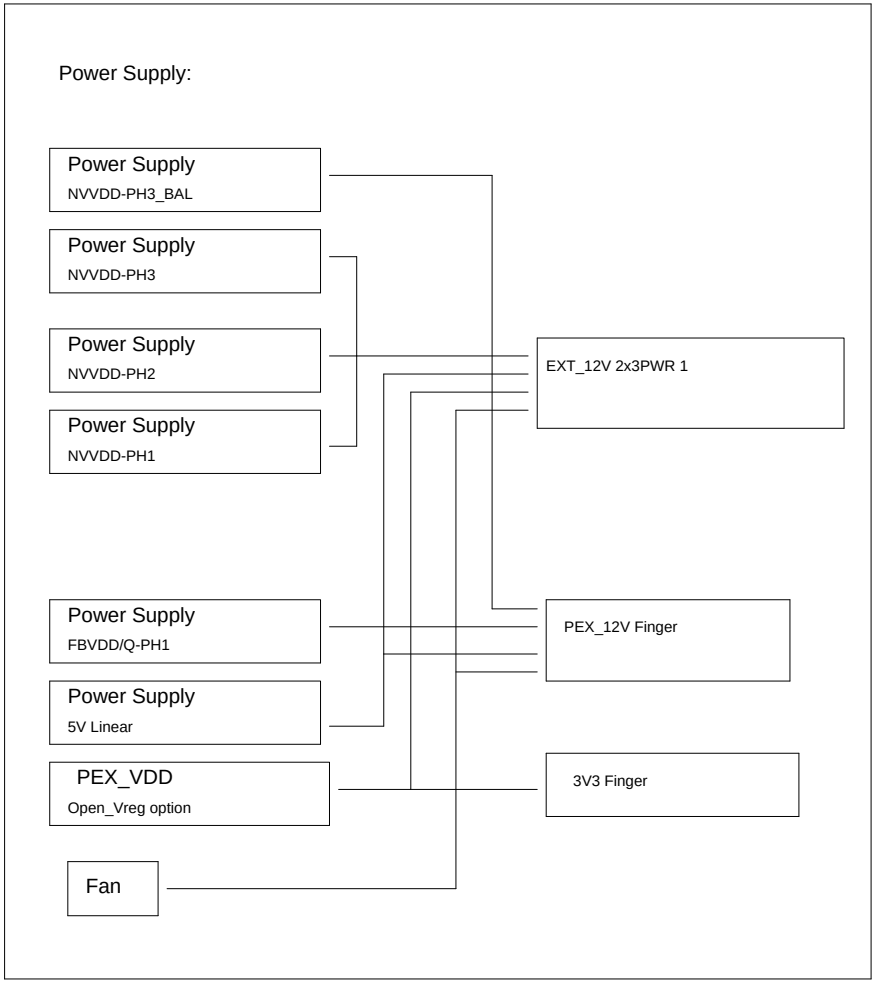
Page2: Block Diagram





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PAGE DETAIL	Block Diagram

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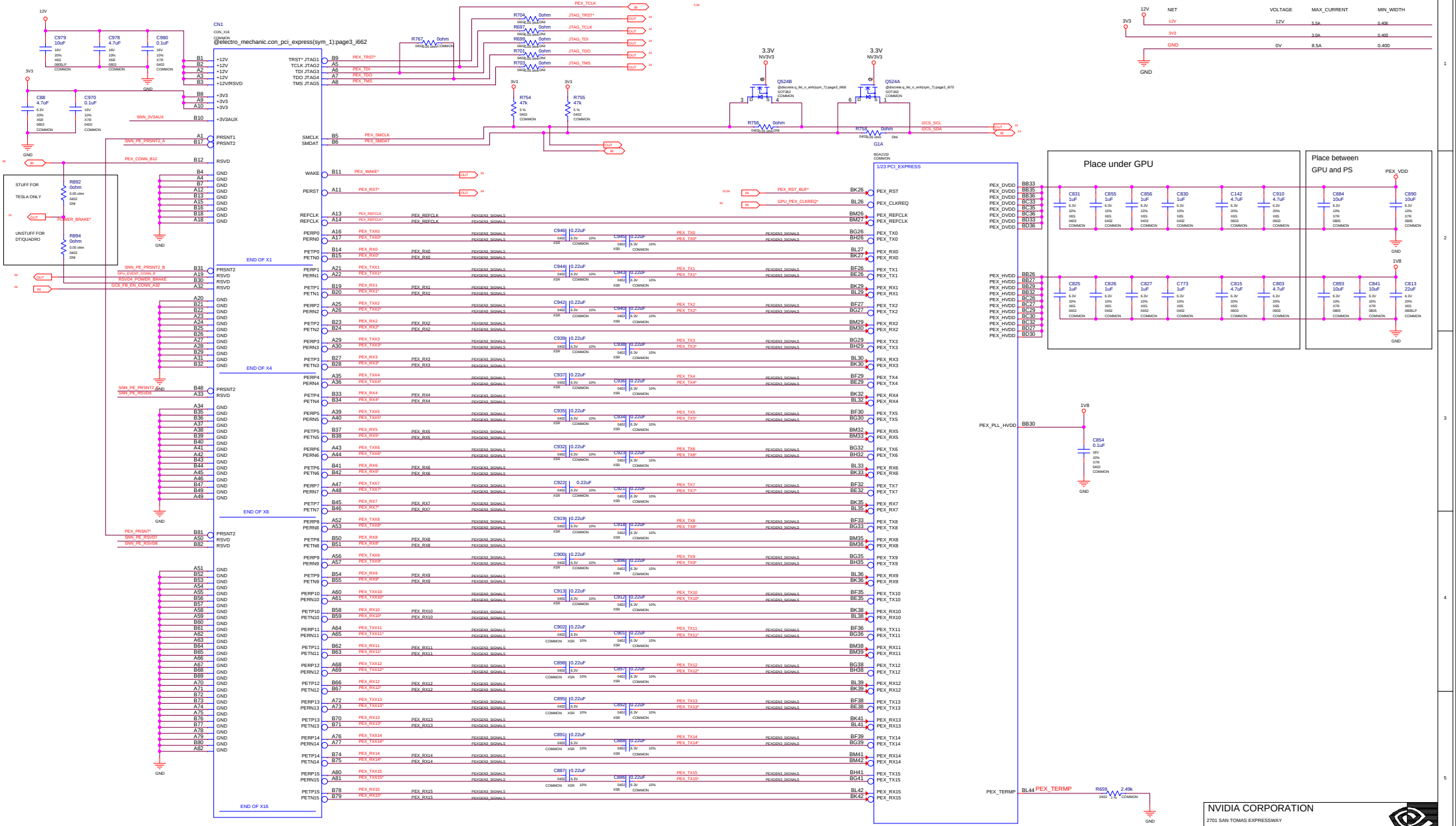
Page3: PCI Express



NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
12V	12V	5.5A	0.406
3V3	3.0A	0.400	
GND	0V	8.5A	0.400

ASSEMBLY	<ASSEMBLY_DESCRIPTION>		
PAGE DETAIL	PCI Express		

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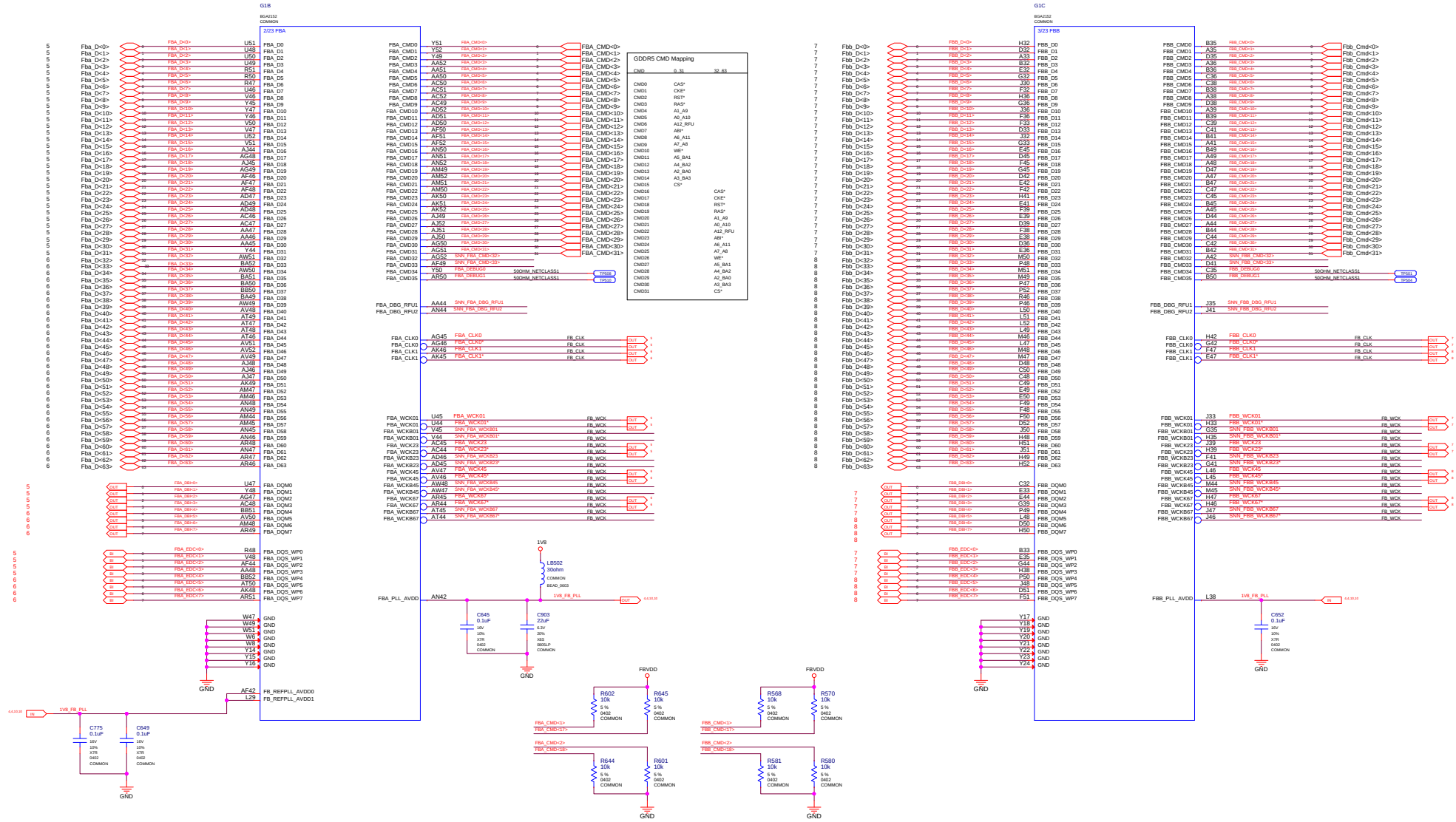
Page4: MEMORY: GPU Partition A/B



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PAGE DETAIL	GPU FB_AB

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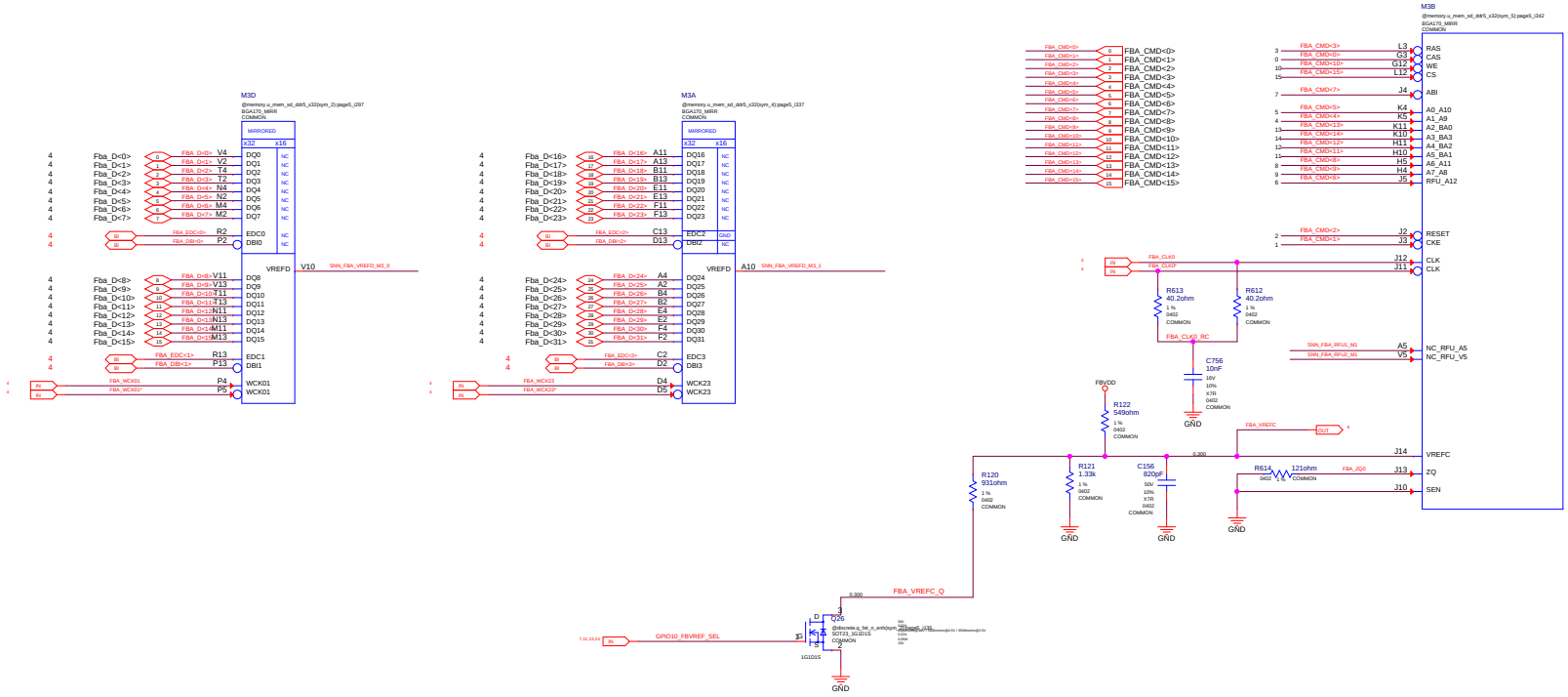
Page5: FRAME BUFFER PARTITION A [31:0]



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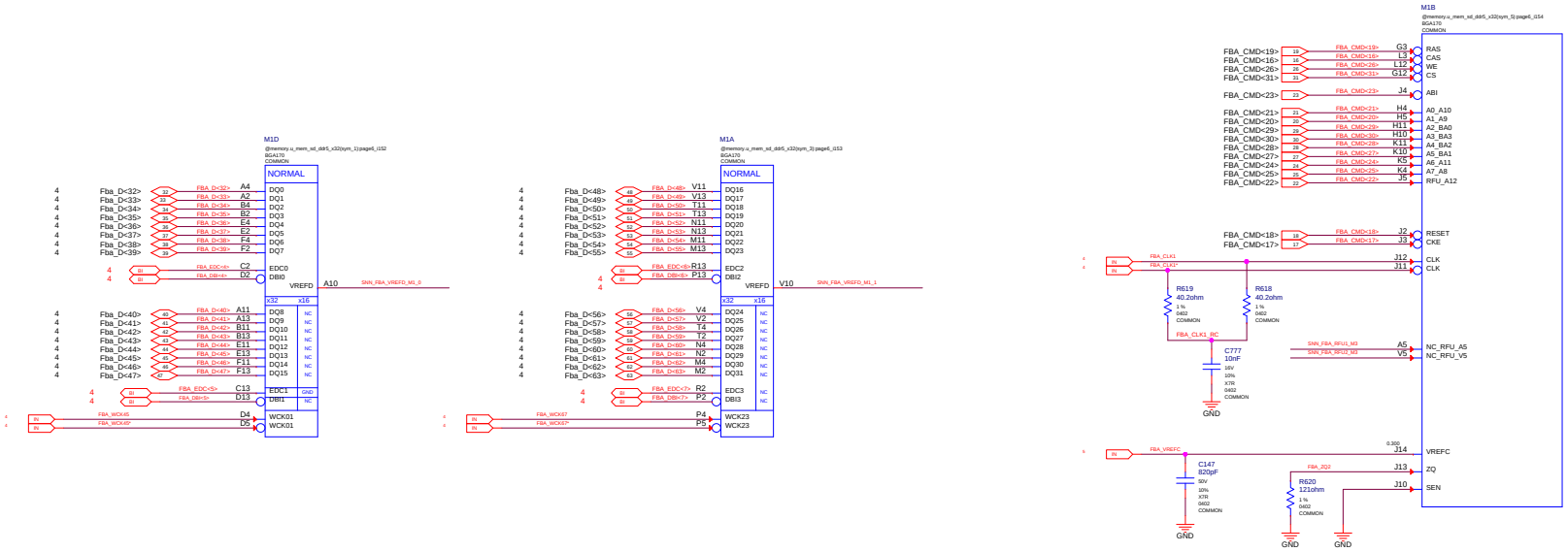
Page6: FRAME BUFFER PARTITION A [63:32]



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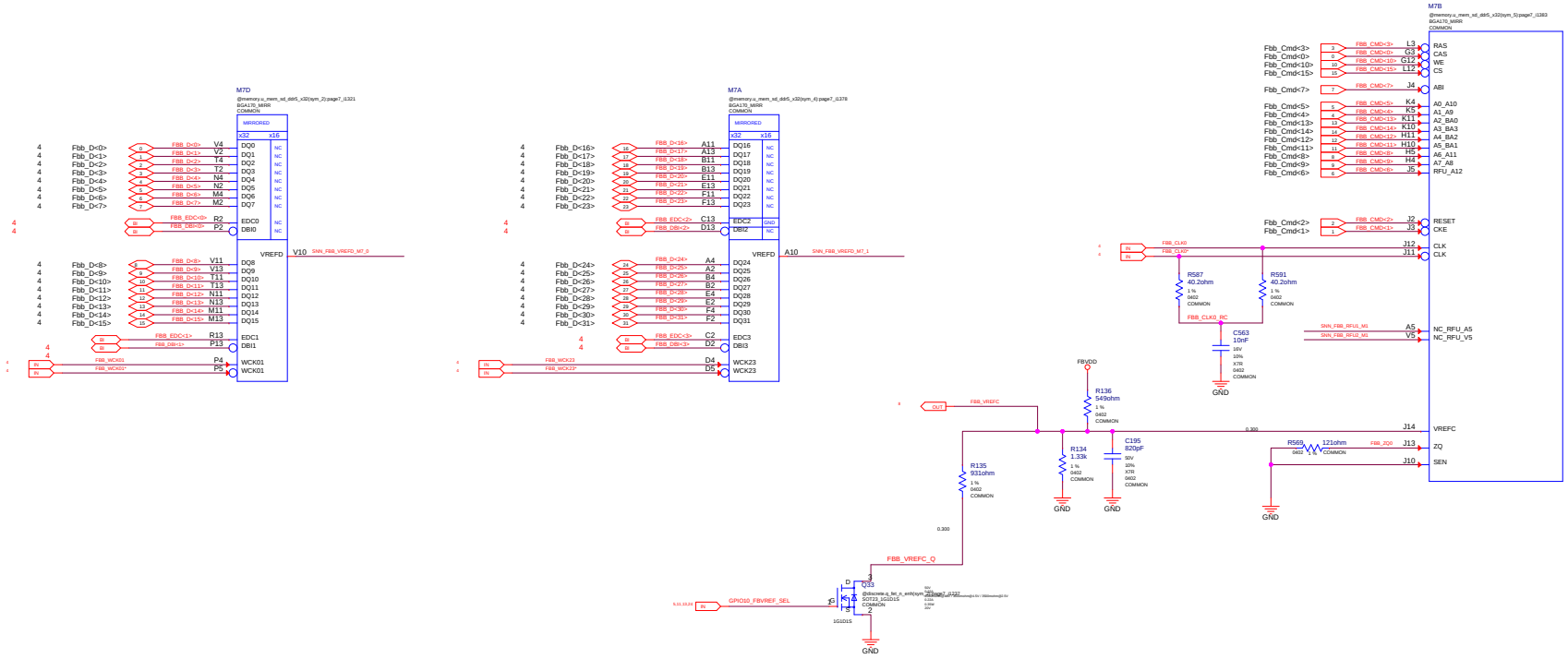
Page7: FRAME BUFFER PARTITION B [31:0]



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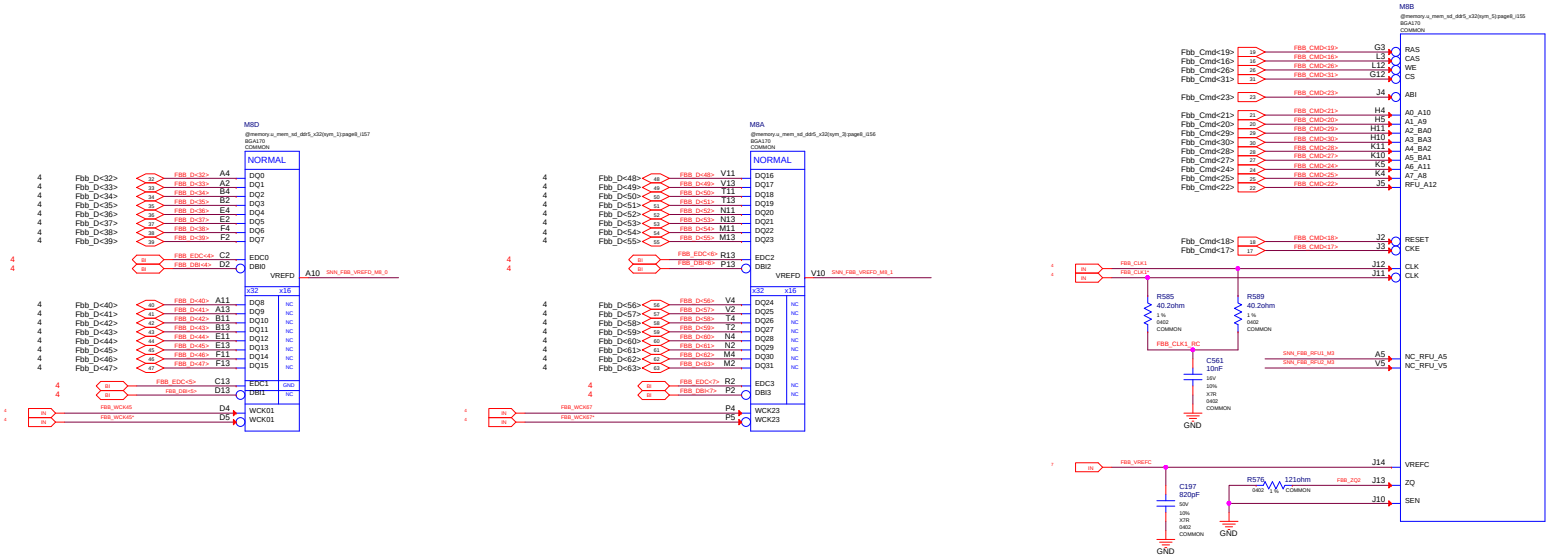
Page8: FRAME BUFFER PARTITION B [63:32]



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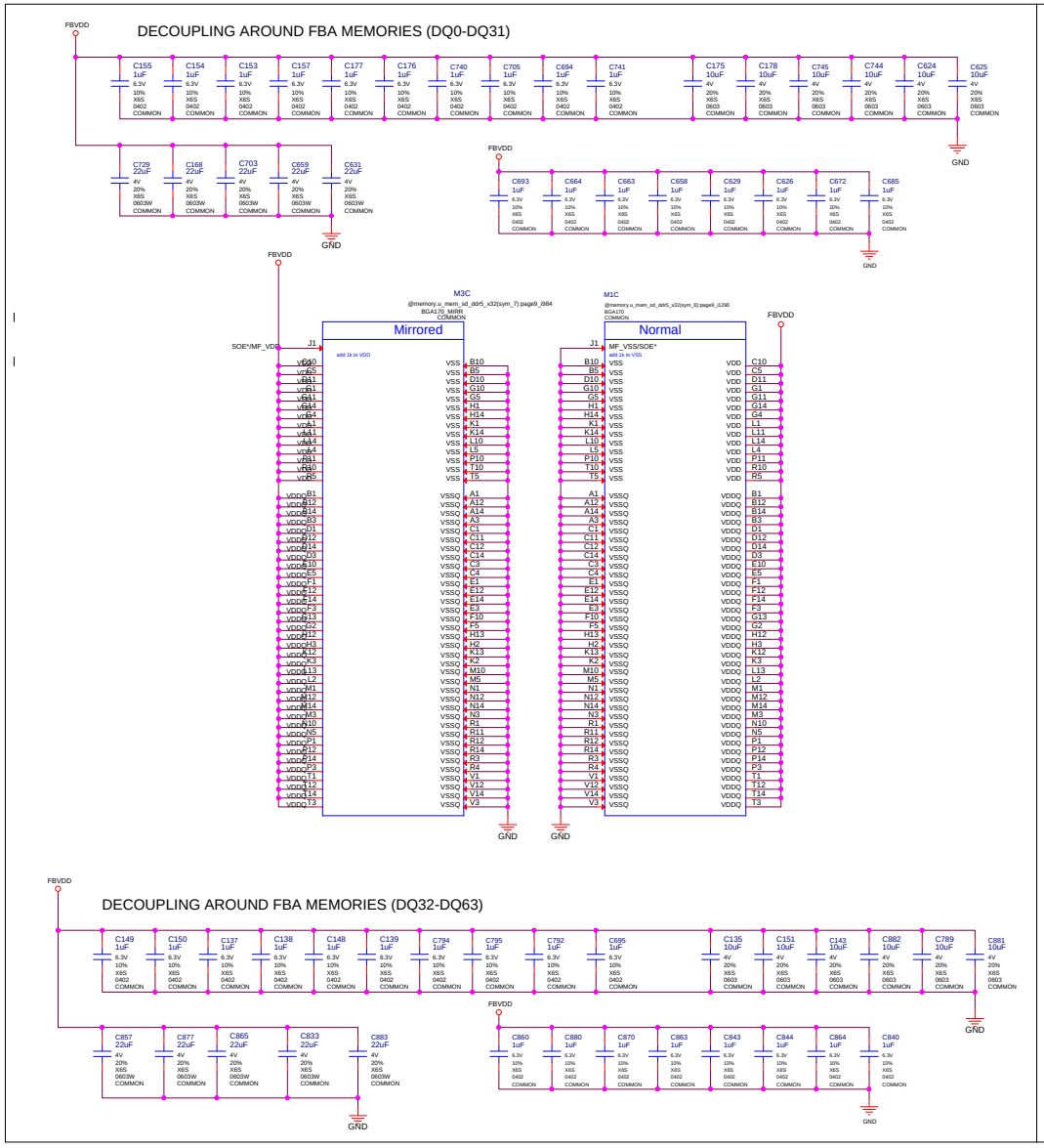
Page9: FRAME BUFFER PARTITION A/B DECOUPLING



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEM FB_AB PWR

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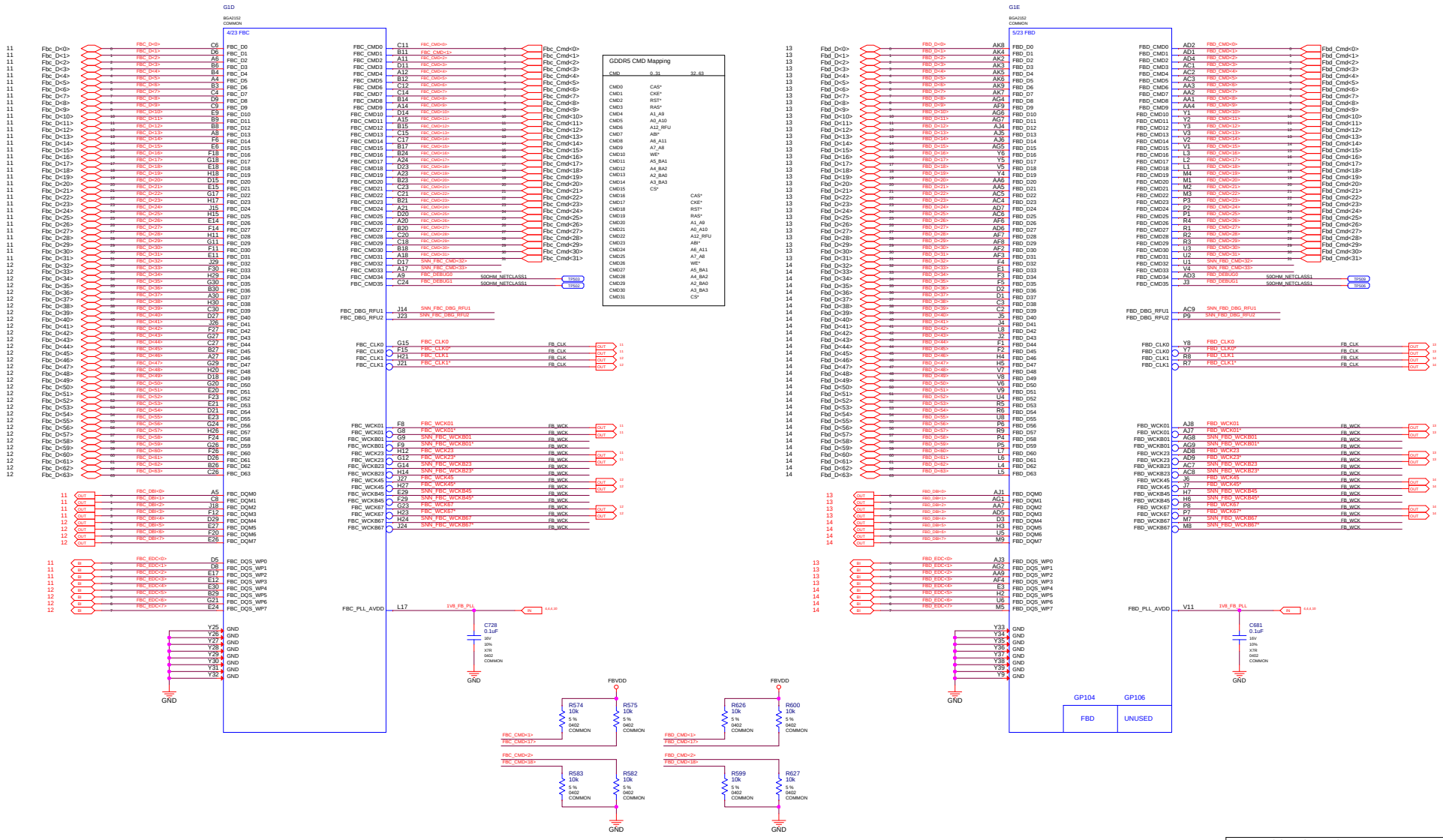
Page10: MEMORY: GPU Partition C/D



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU FB_CD

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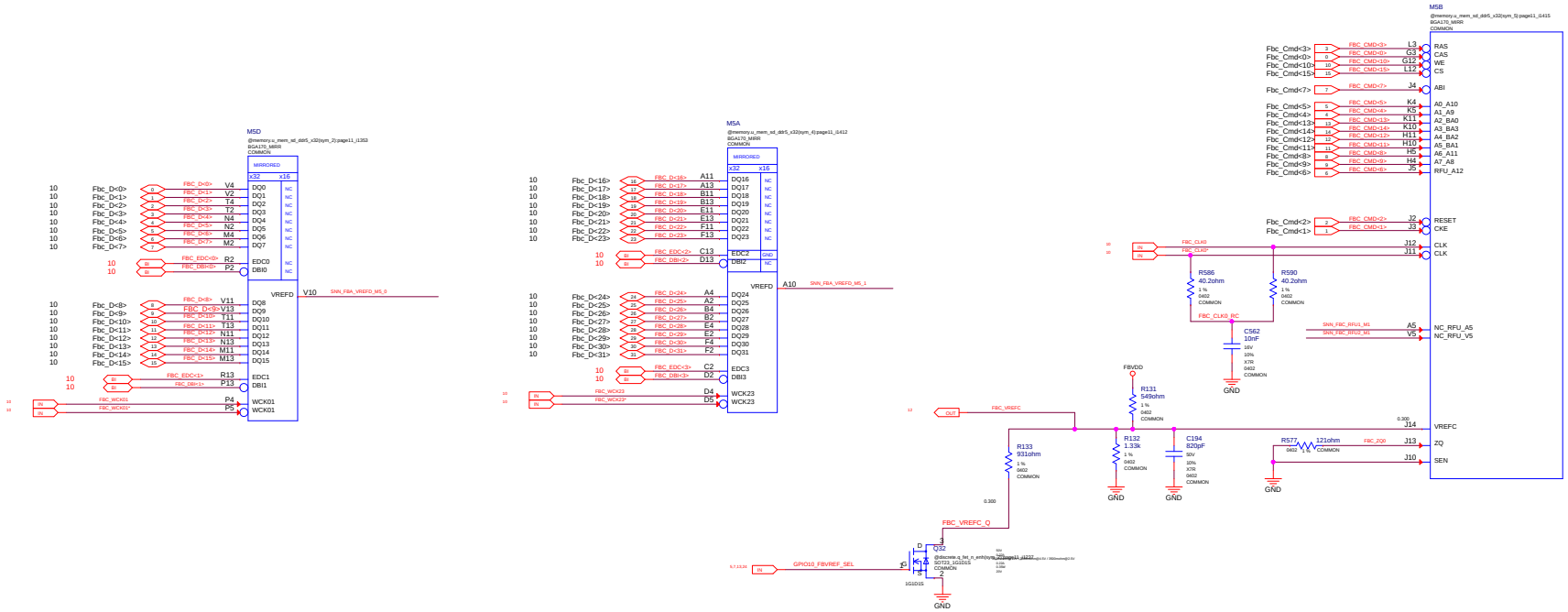
Page11: Frame Buffer Partition C [31:0]



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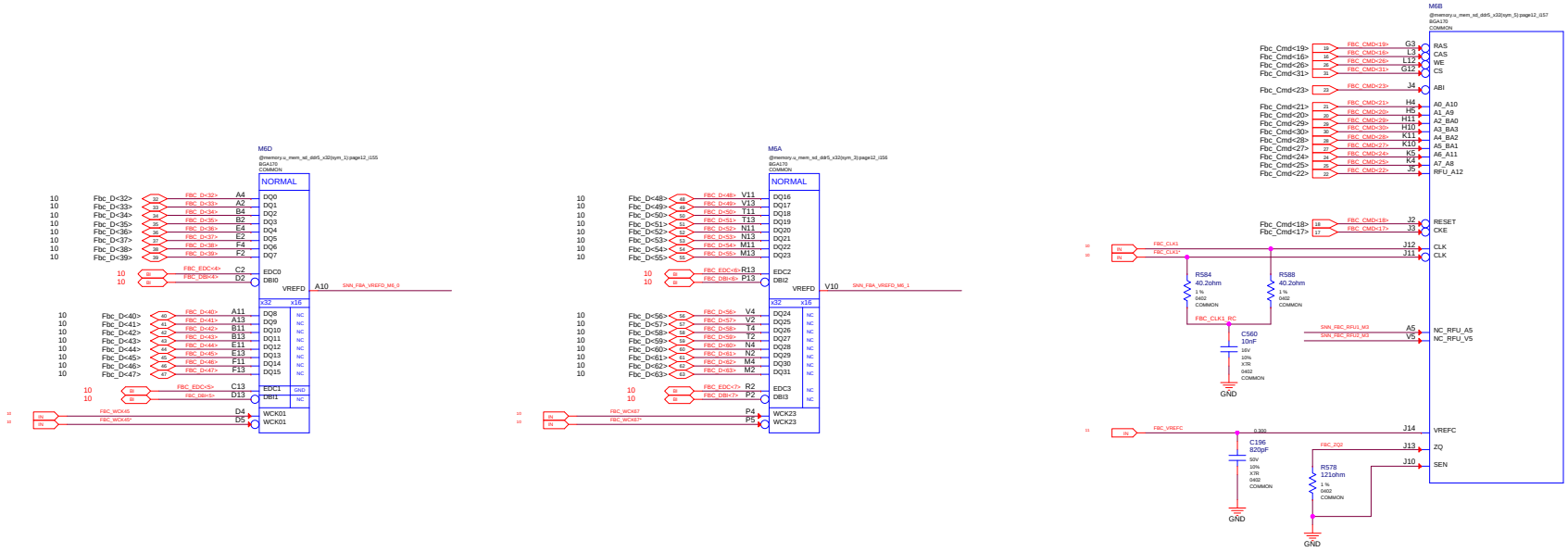
Page12: FRAME BUFFER PARTITION C [63:32]



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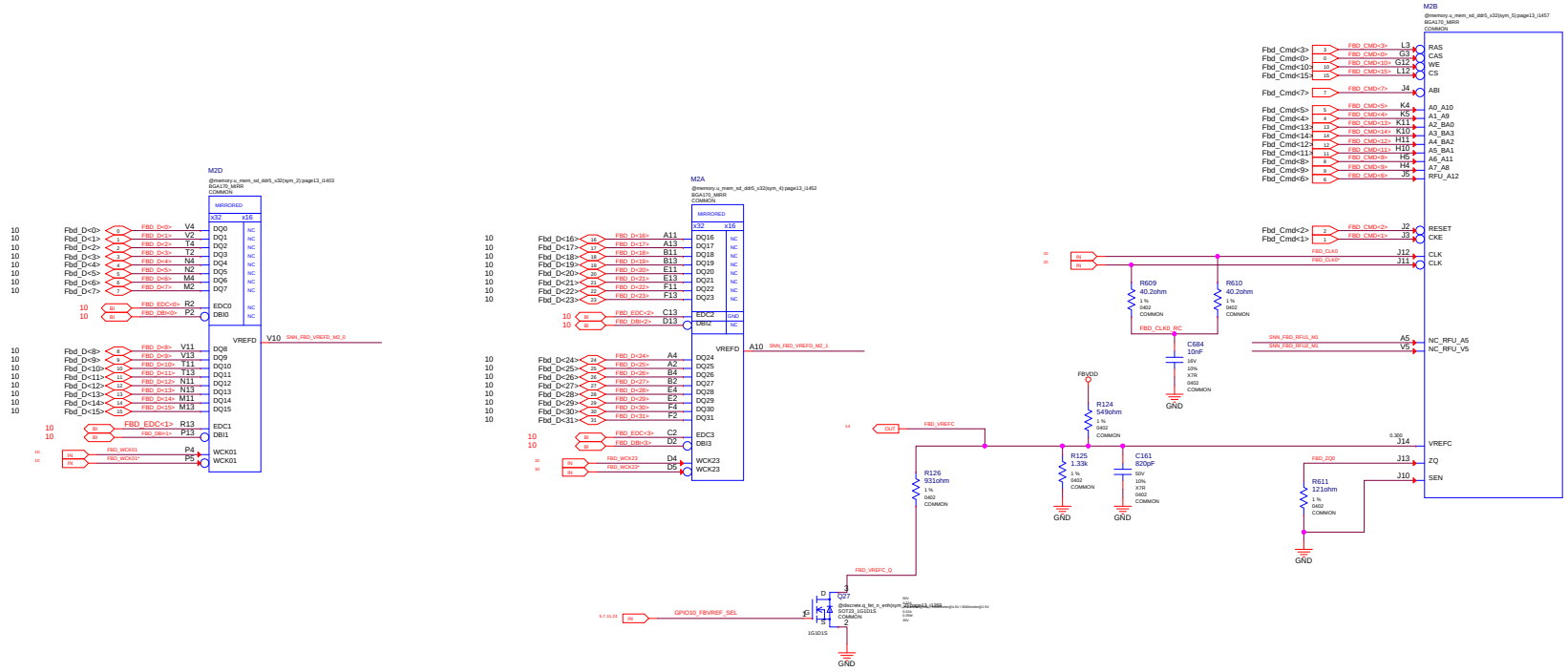
Page13: FRAME BUFFER PARTITION D[31:0]



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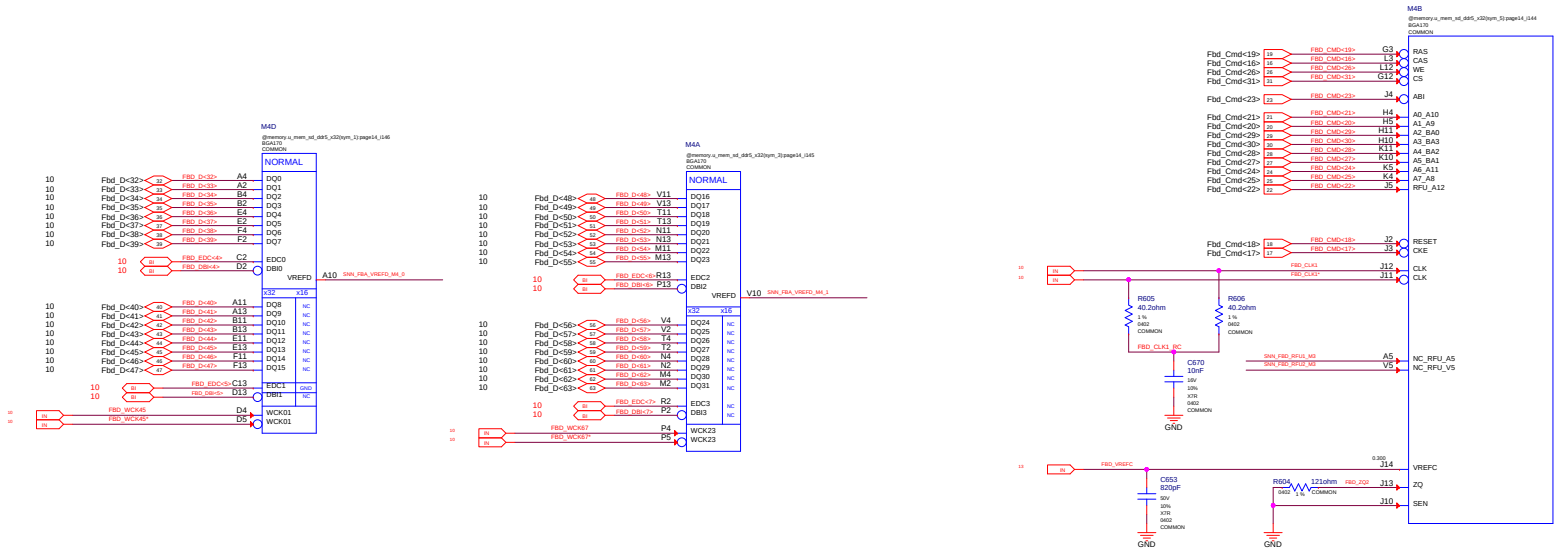
Page14: FRAME BUFFER PARTITION D[63:32]



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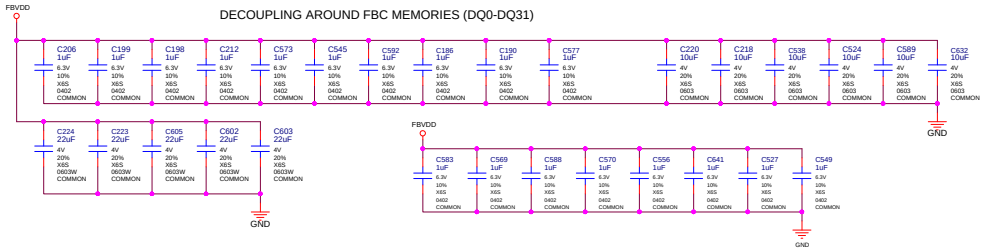
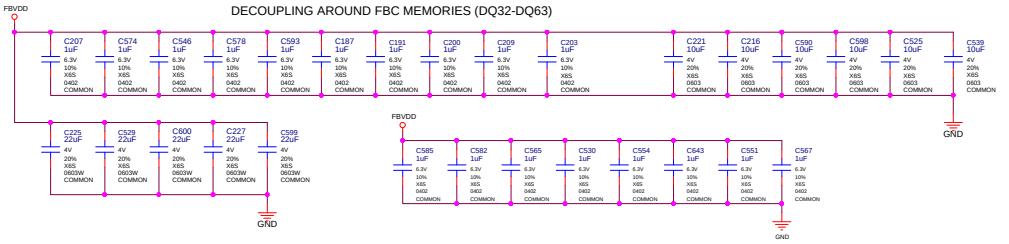
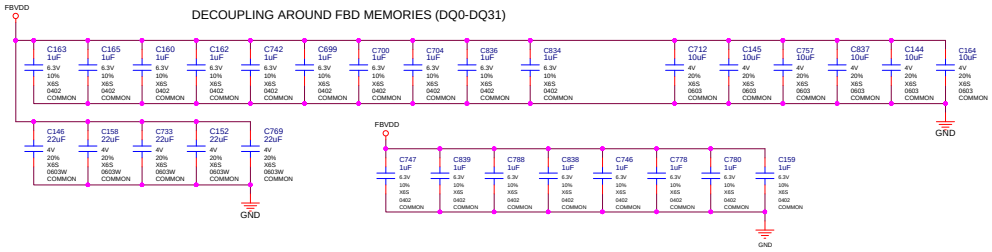
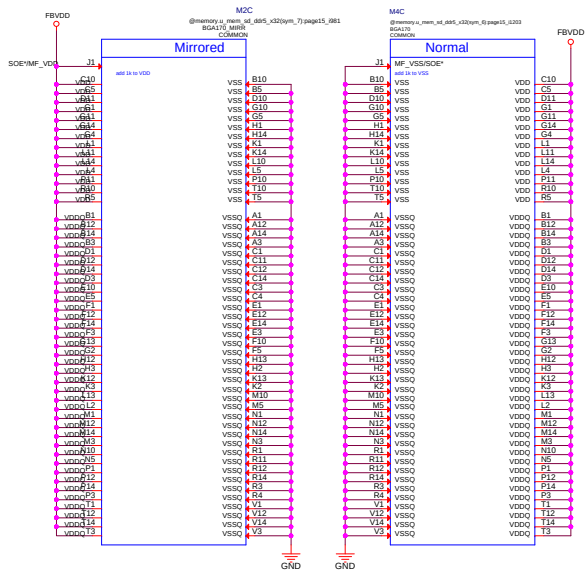
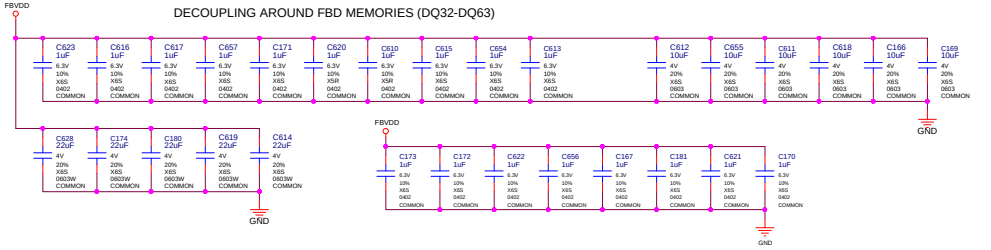
Page15: FRAME BUFFER PARTITION C/D DECOUPLING











ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEM FB_CD PWR

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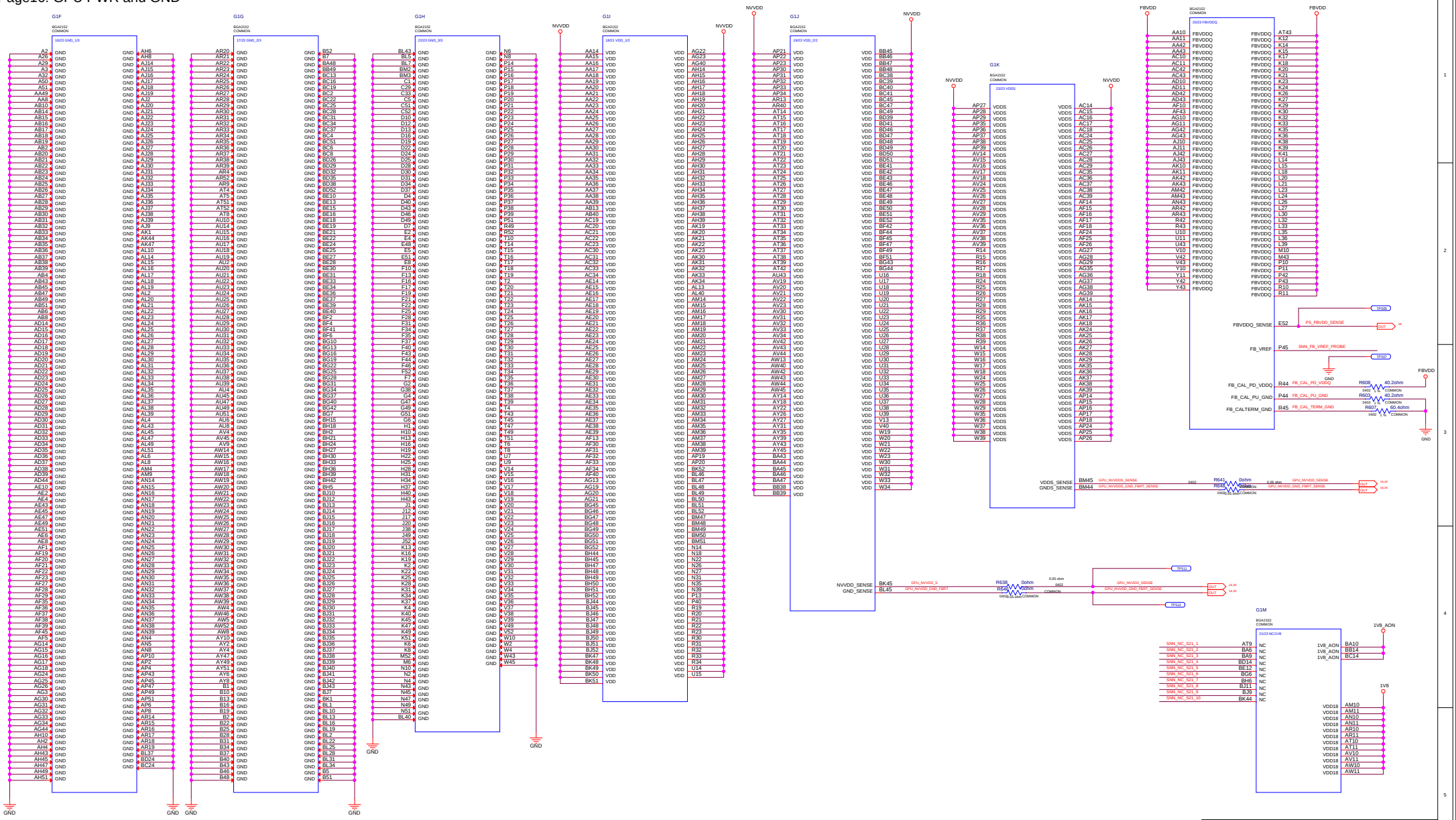
Page16: GPU PWR and GND



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU PWR & GND

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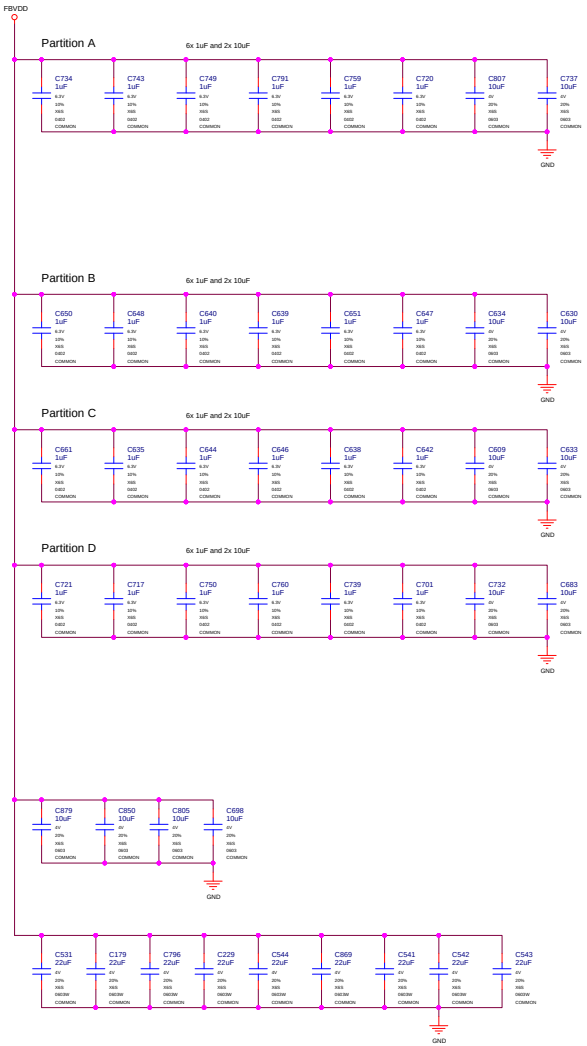
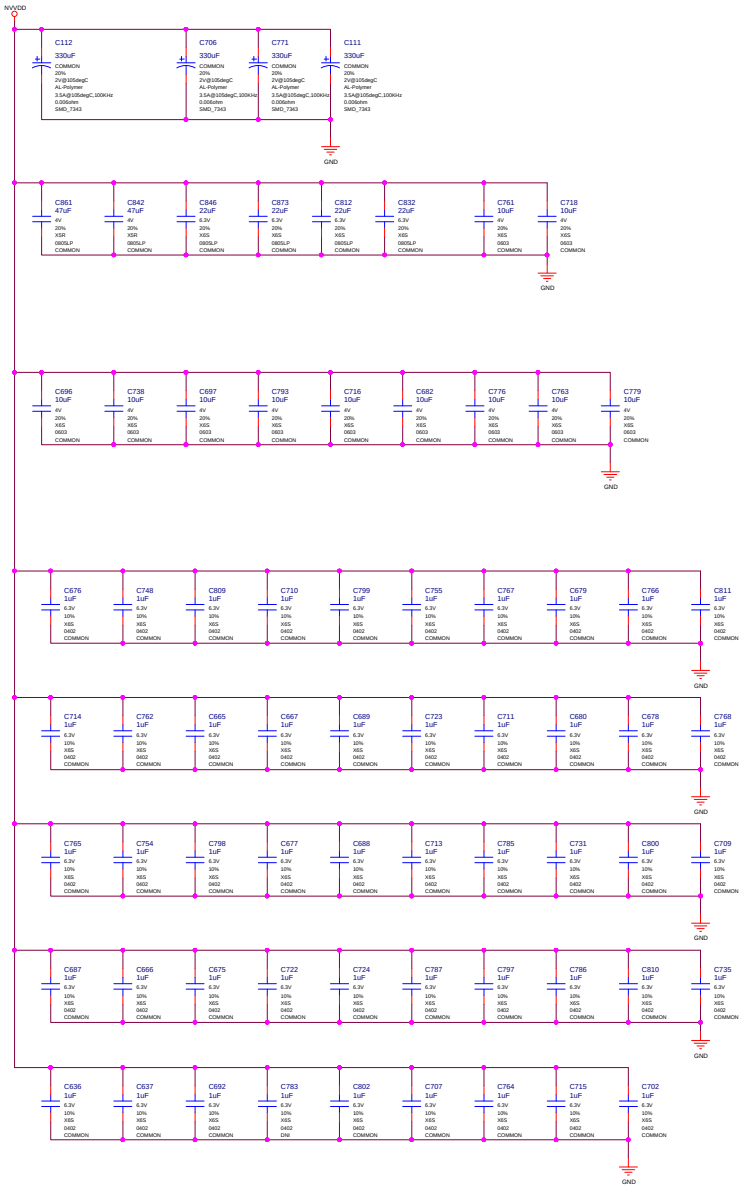
Page17: GPU Decoupling

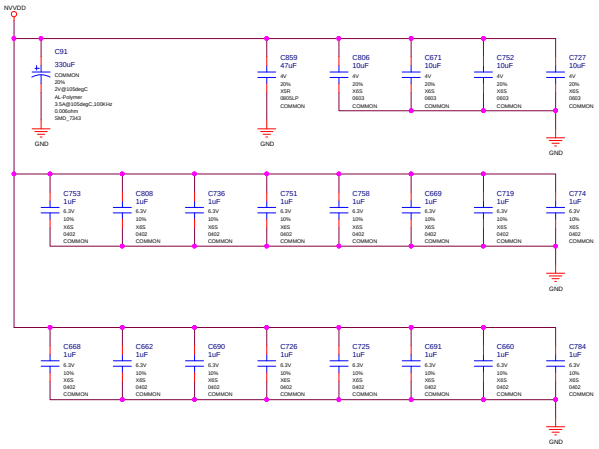
FBVDD



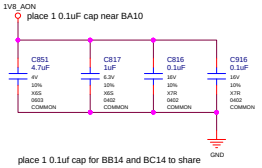
NVVDD



NVVDD

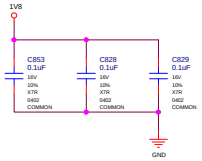


1V8_AON



place 1 0.1uf cap for BB14 and BC14 to share

1V8_MAIN



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU Decoupling

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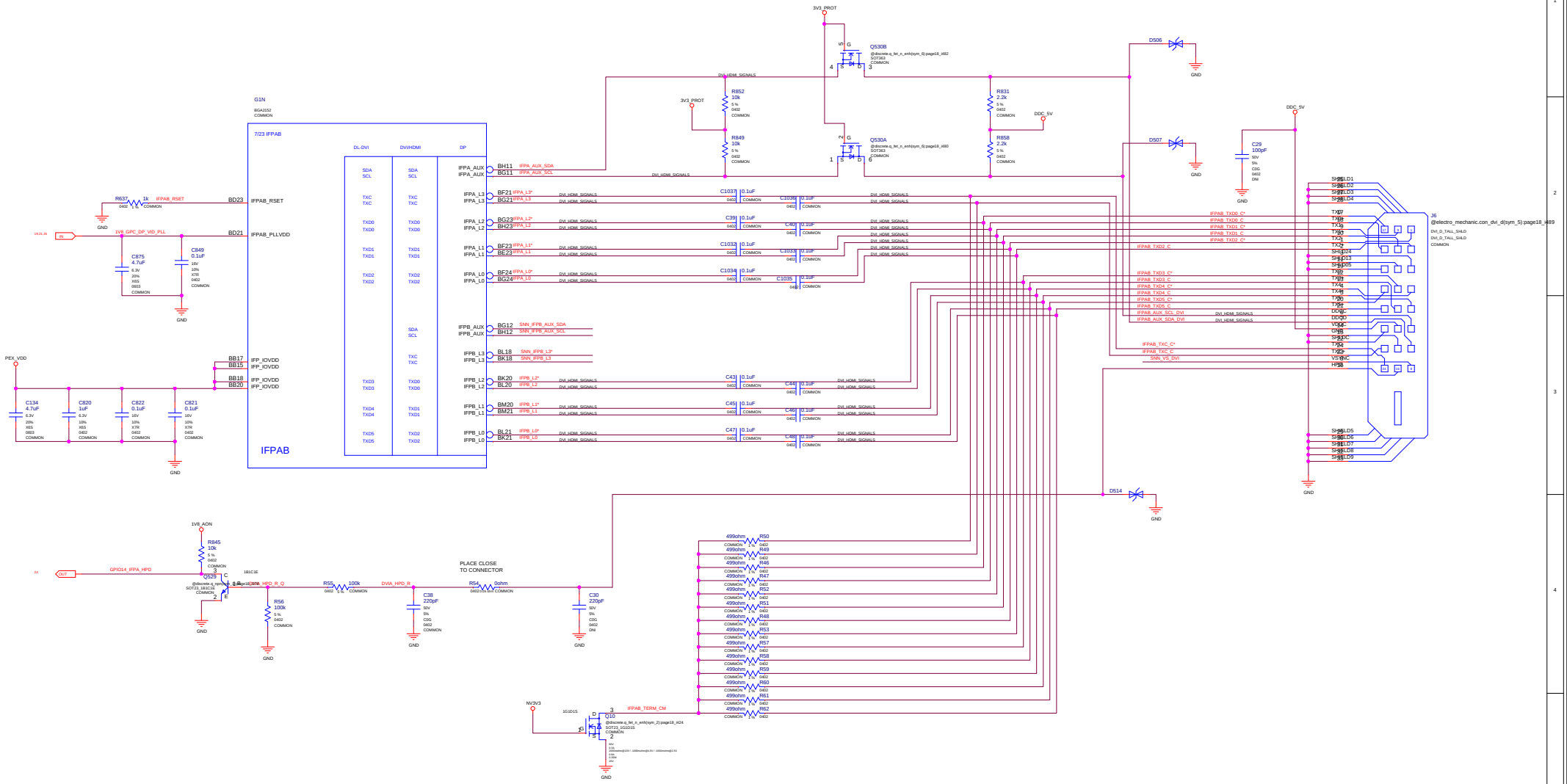
Page18: IFPAB DVI-D-DL



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPAB DVI-D-DL

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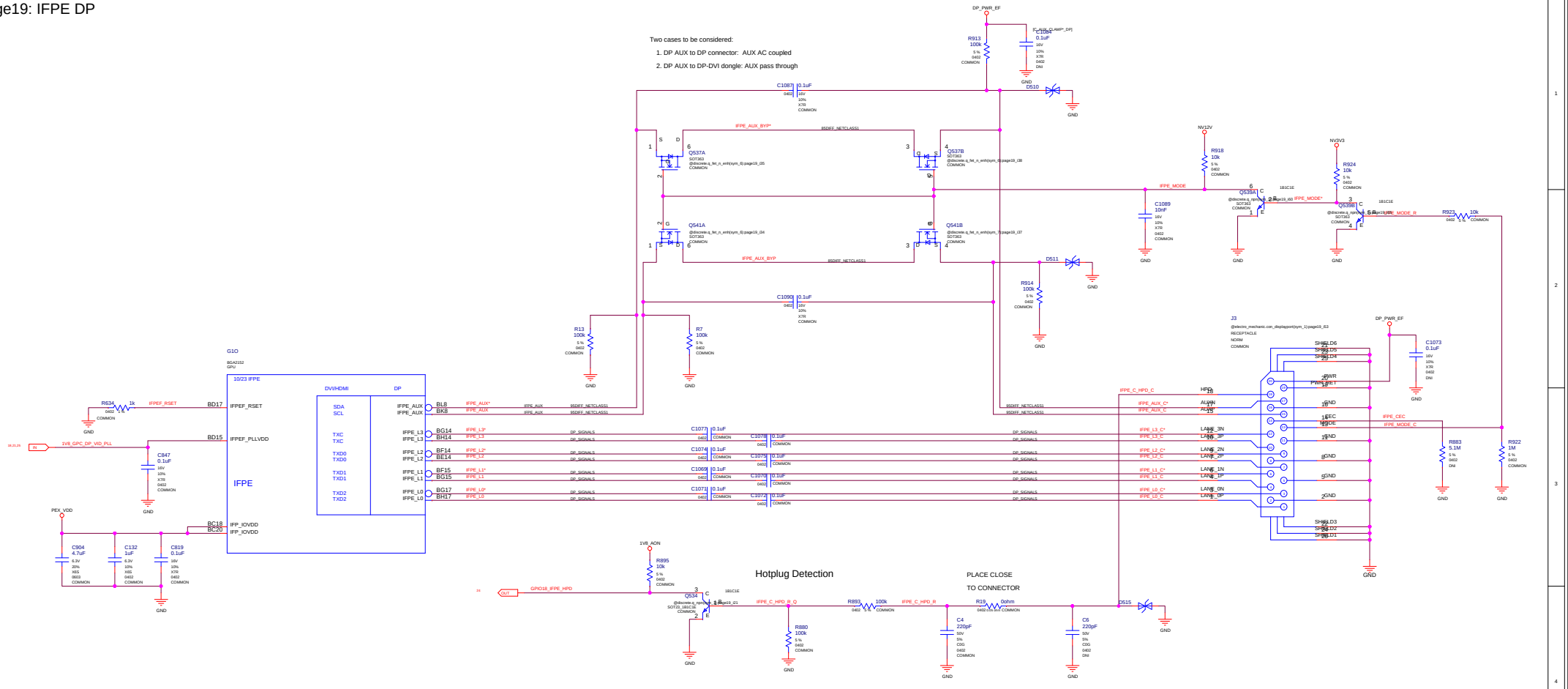
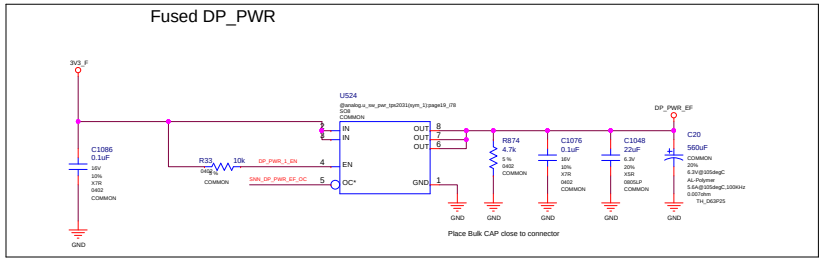
Page19: IFPE DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



Fused DP_PWR



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPE DP

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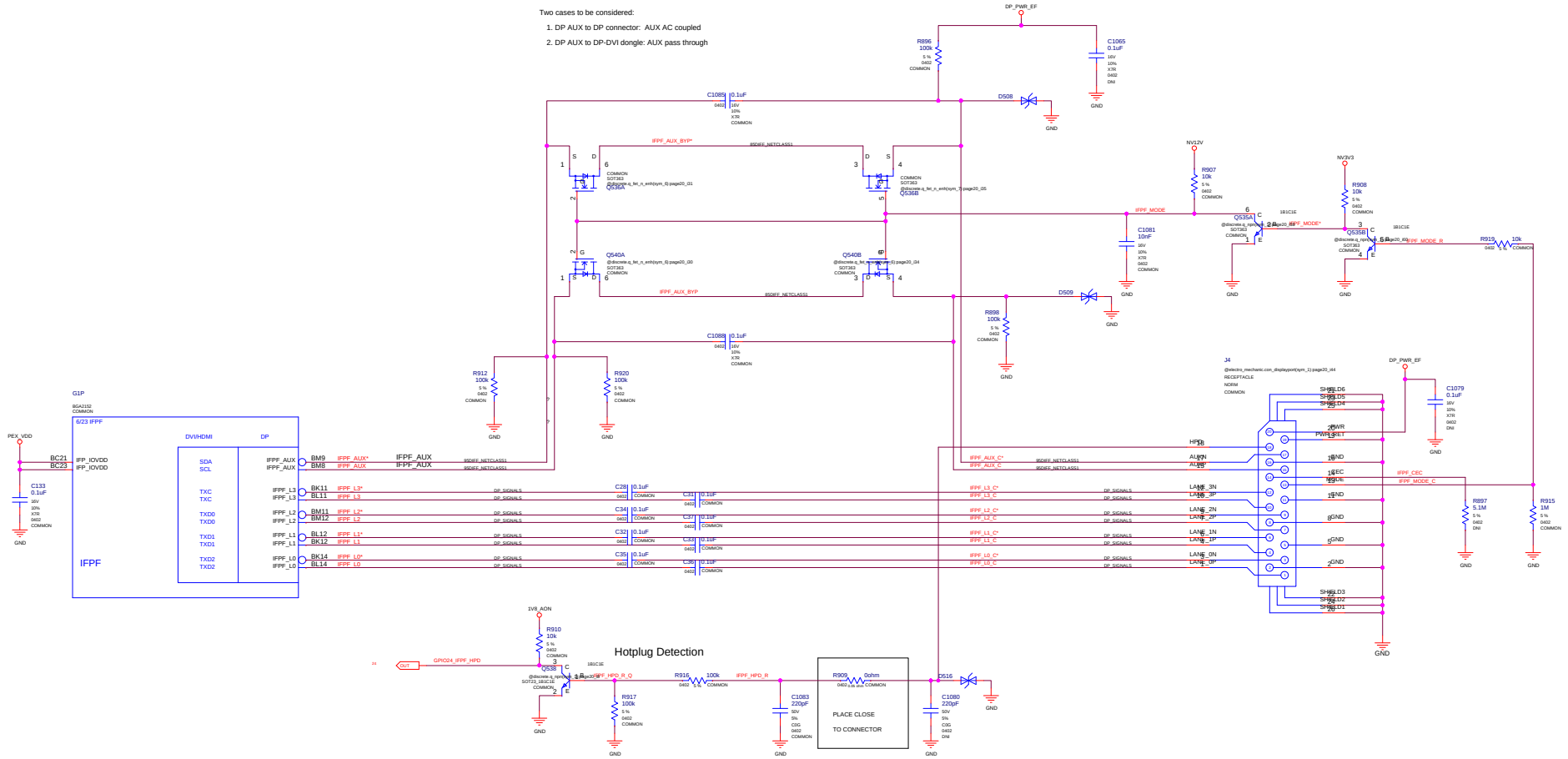
Page 20: IFPF DP



ASSEMBLY <ASSEMBLY_DESCRIPTION>

PAGE DETAIL IFPF DP

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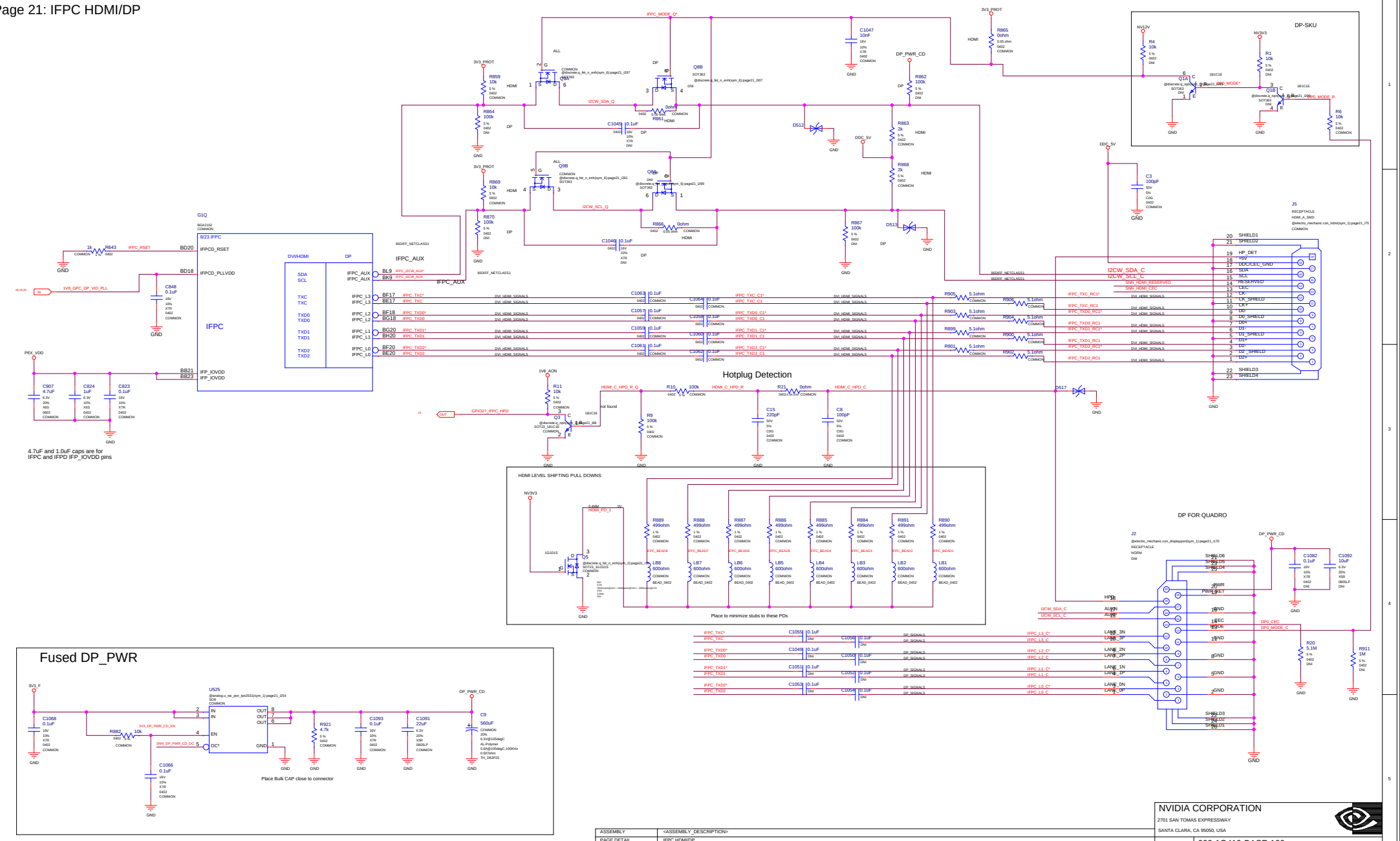
Page 21: IFPC HDMI/DP



Fused DP_PWR

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPC HDMI/DP

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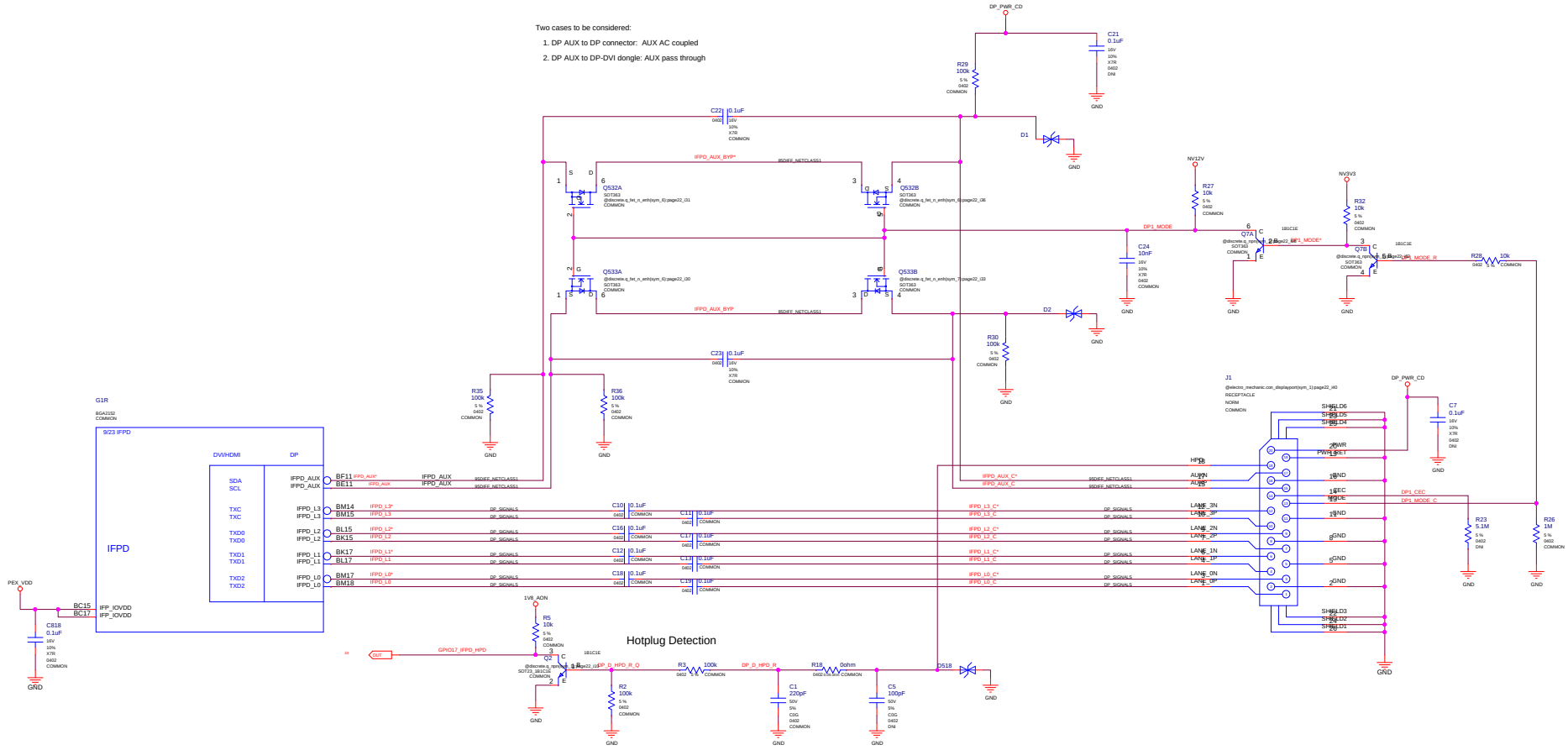
Page 22: IFPD DP



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPD DP

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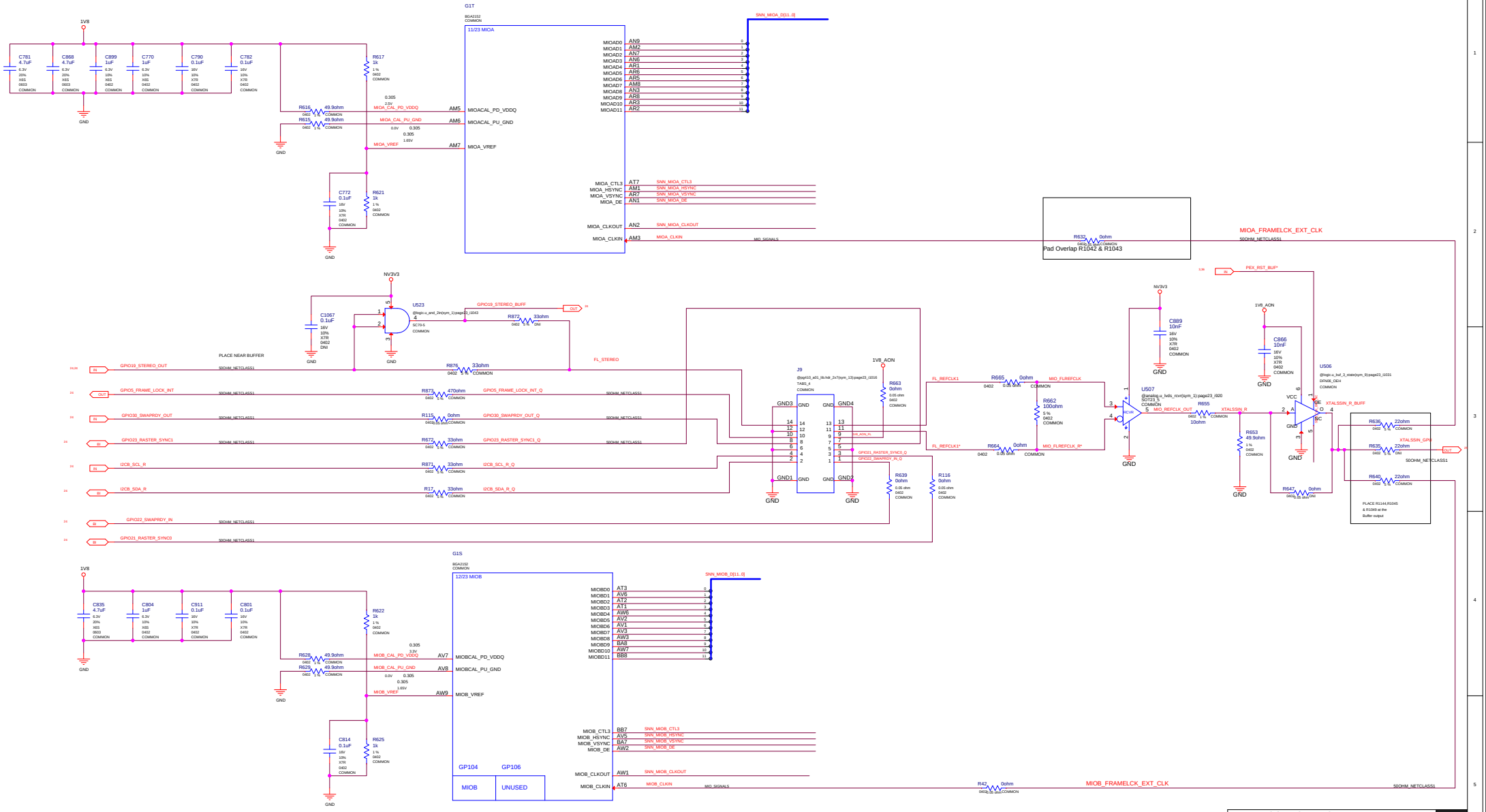
Page 23: MIOA/B Interface and Frame Lock



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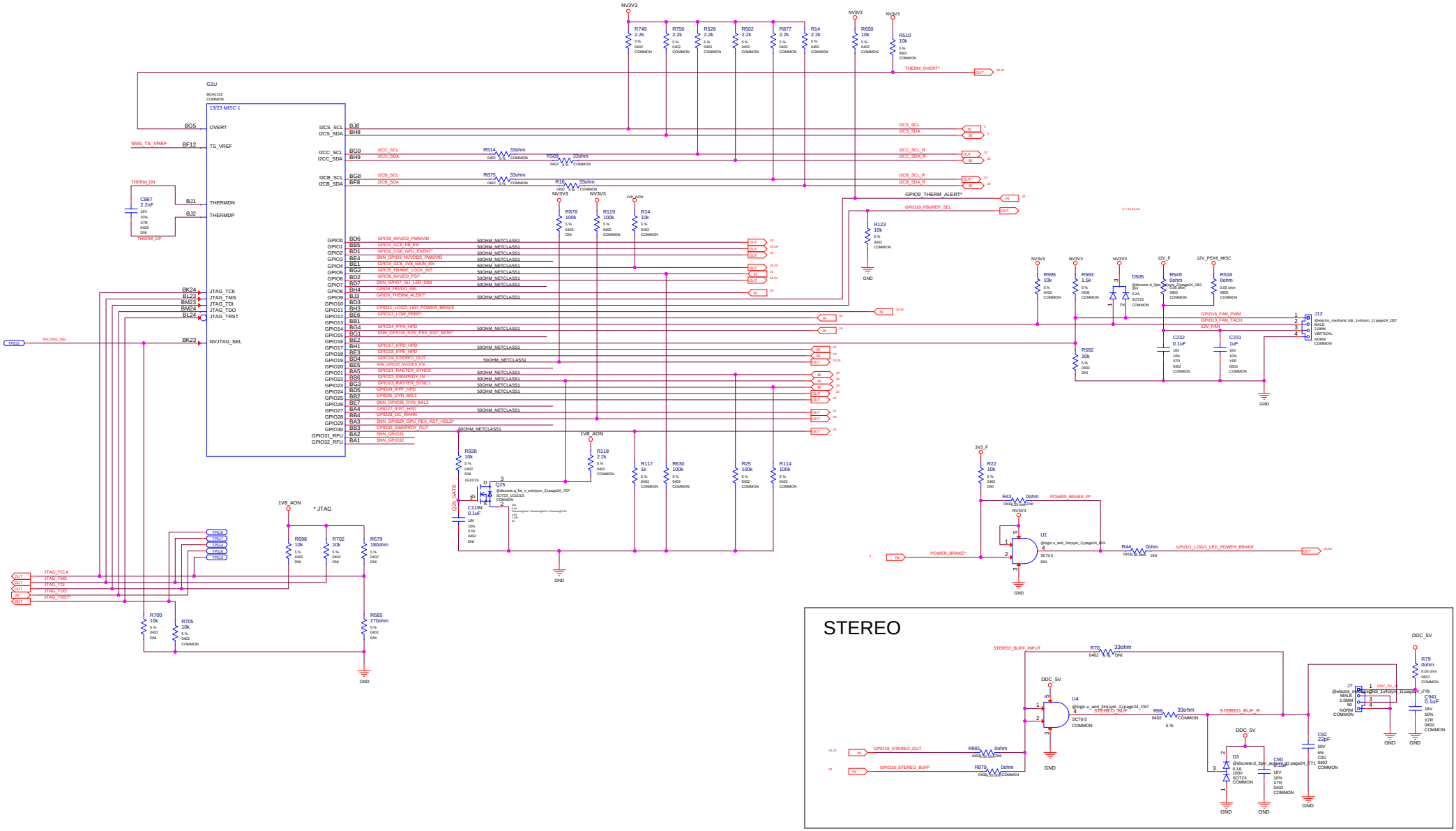
Page 24: MISC1: Fan, Thermal, JTAG, GPIO



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC1: Fan, Thermal, JTAG, GPIO,STEREO

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Page25: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

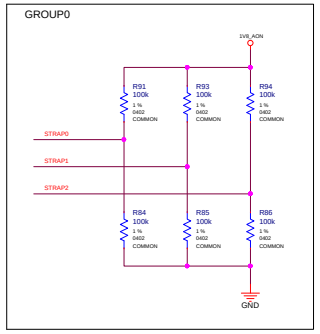
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

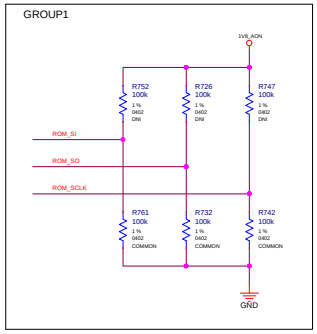
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

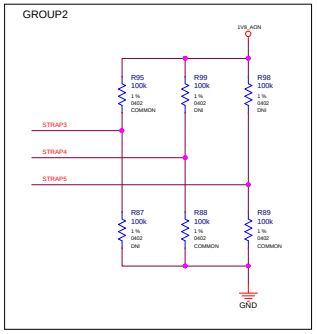
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

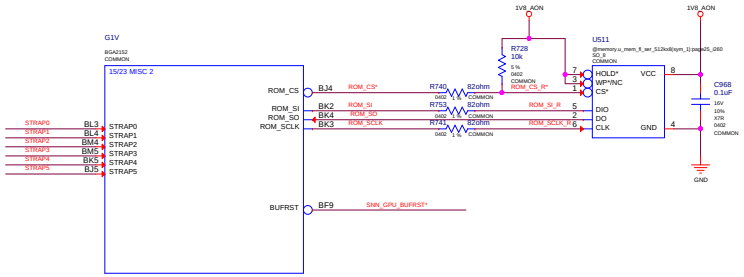
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

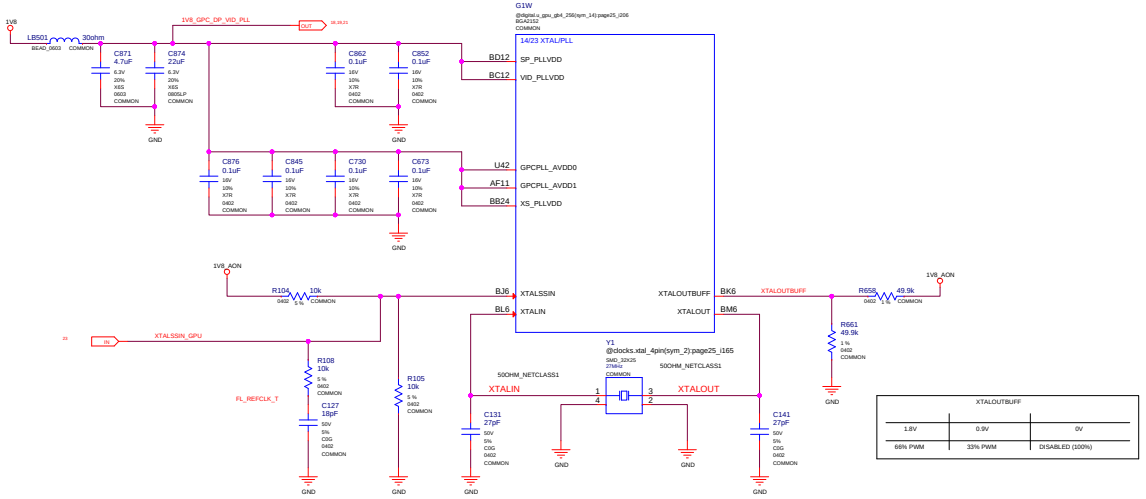






CFG[3:0]	Config Width	Vendor
0000	256Mx32 256-bit Samsung	
0001	256Mx32 256-bit Micron	
0010	256Mx32 256-bit Hynix	
0011	Reserved	
0100	Reserved	
0101	Reserved	
0110	Reserved	
0111	Reserved	





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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC2: ROM, XTAL,STRAPS

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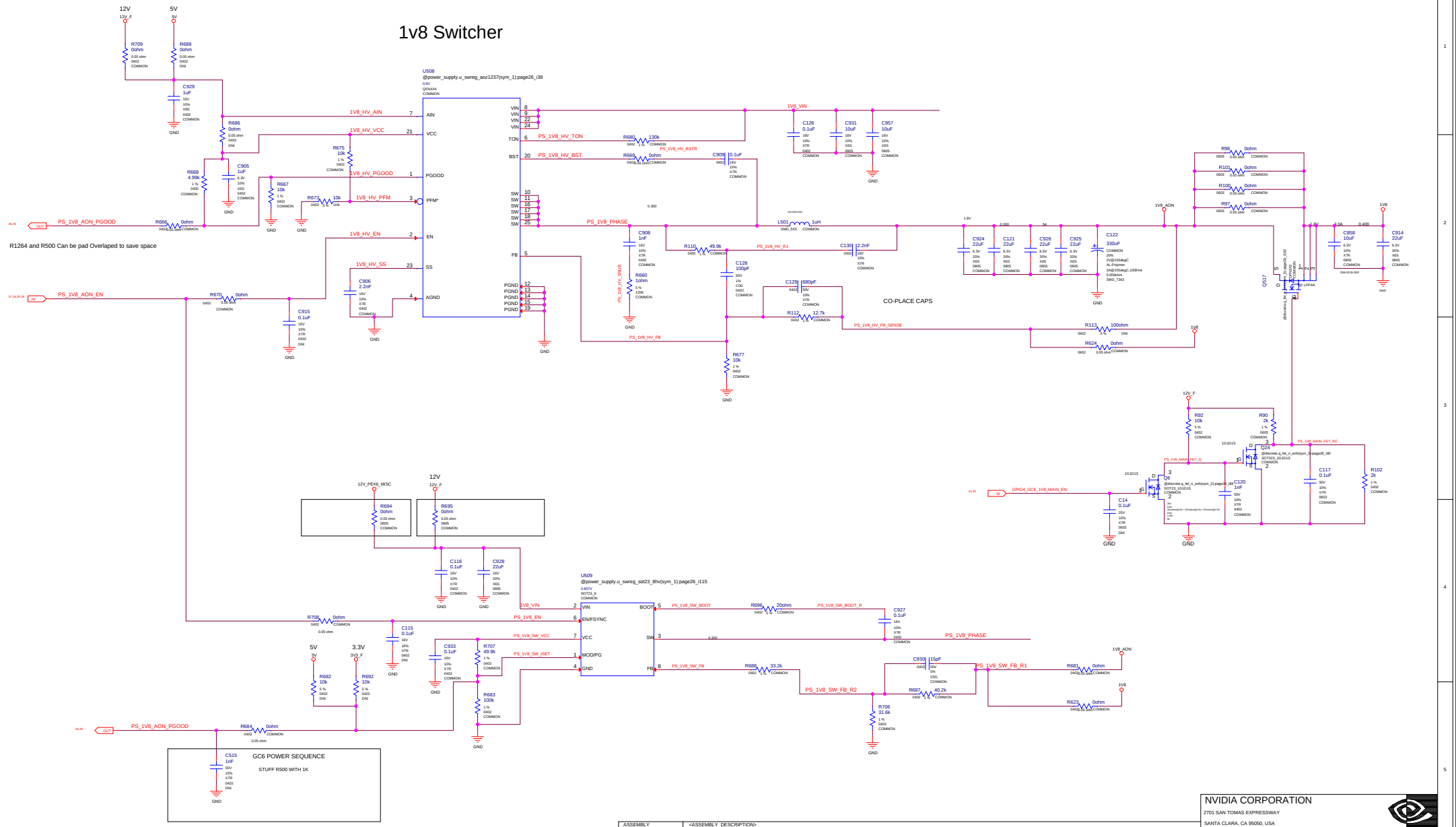
Page26: PS: 1V8 PLL, 1V8_AON



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: 1V8_PLL, 1V8_AON

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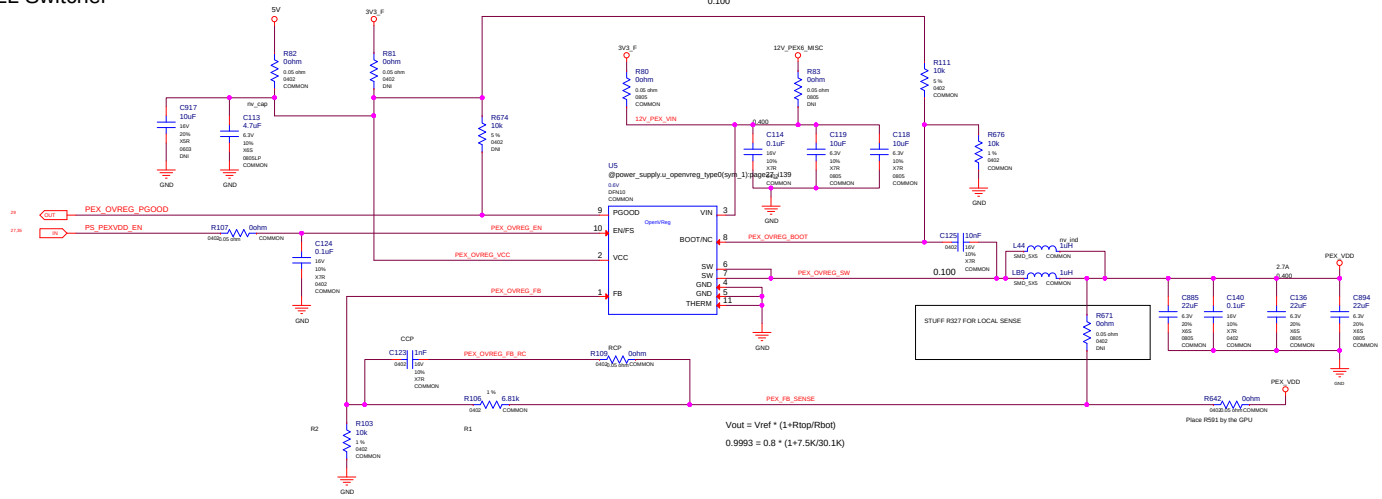
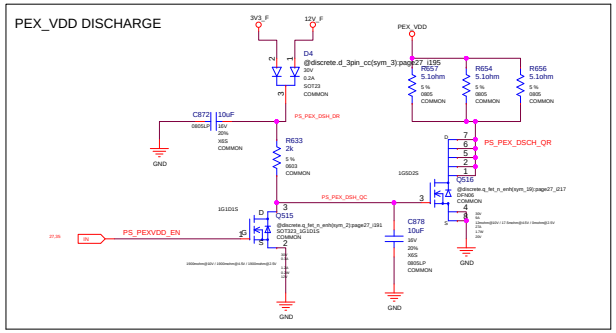
Page27: PS: 5V SWITCHER,PEX VDD

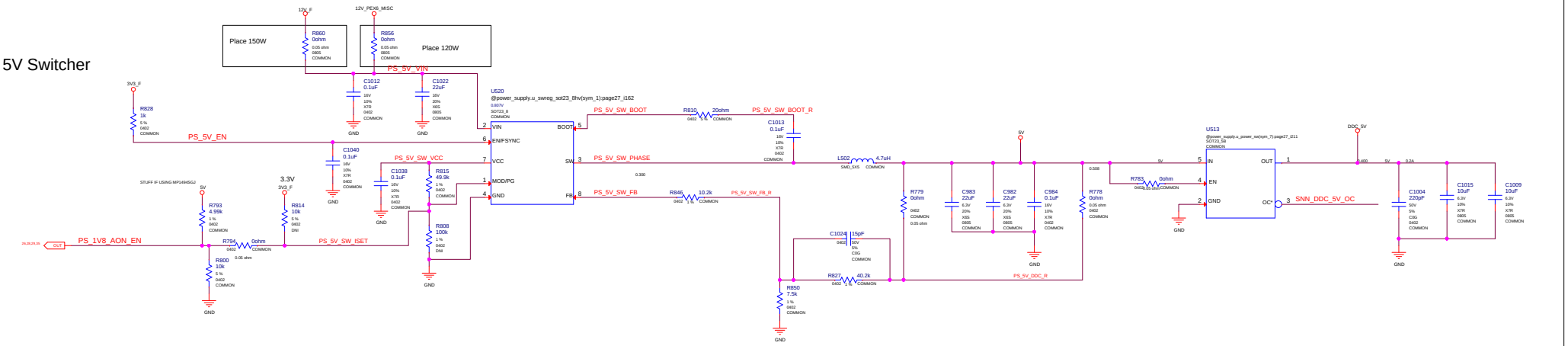
PEX PLL Switcher



PEX_VDD DISCHARGE



5V Switcher



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: 5V, PEX_VDD

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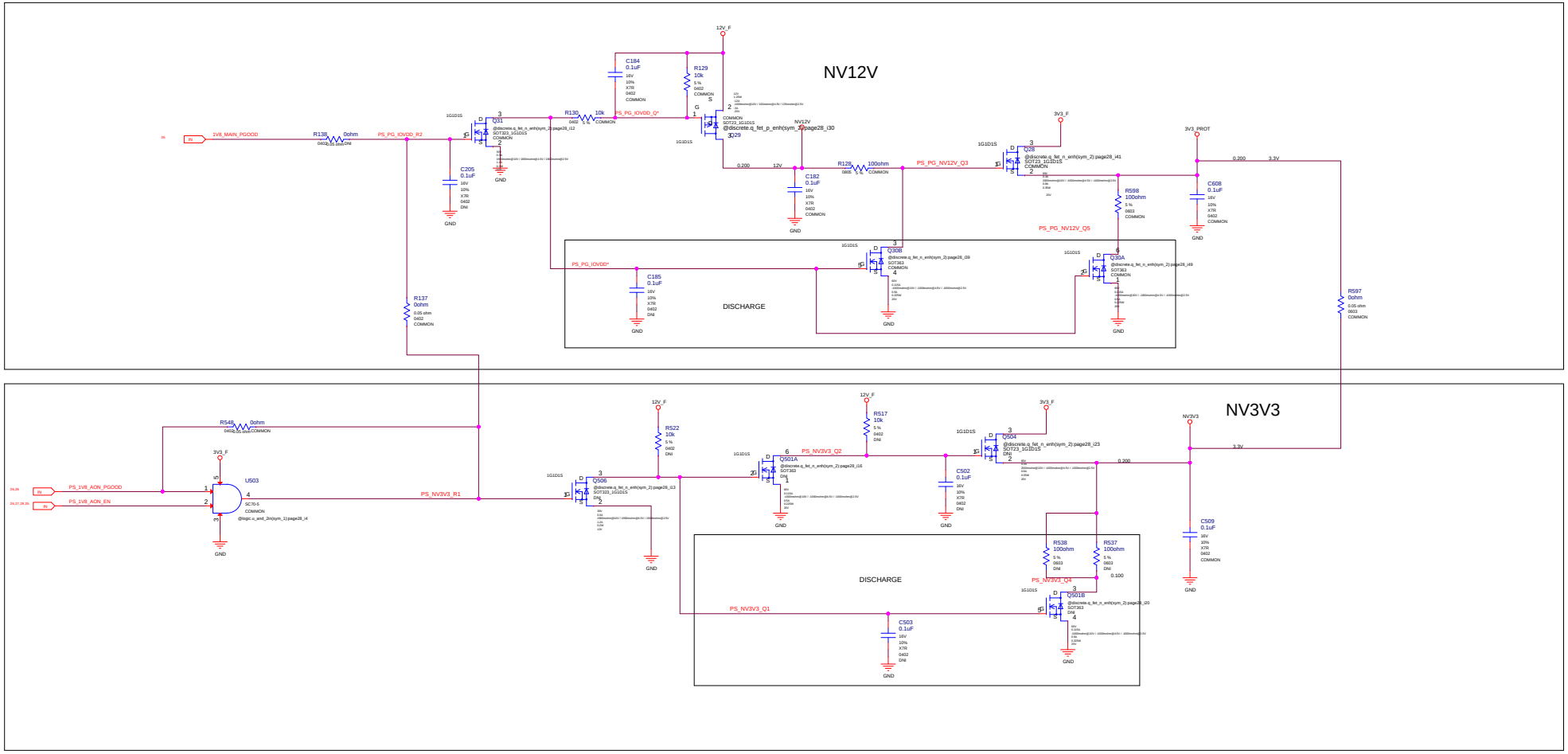
Page 28:PS: NV3V3, NV12V



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NV3V3, NV12V

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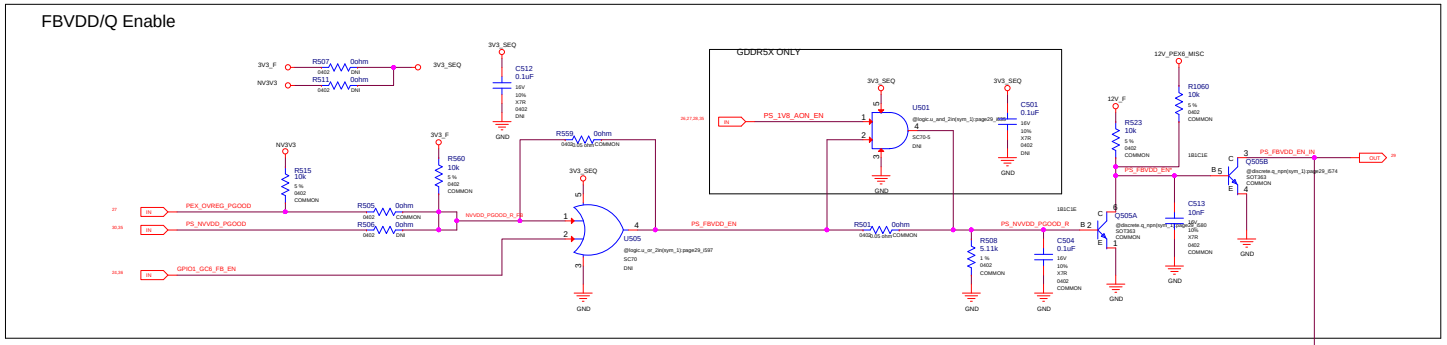
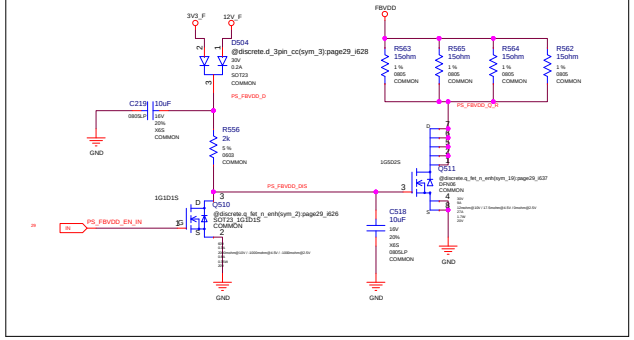
Page29: PS: FBVDDQ

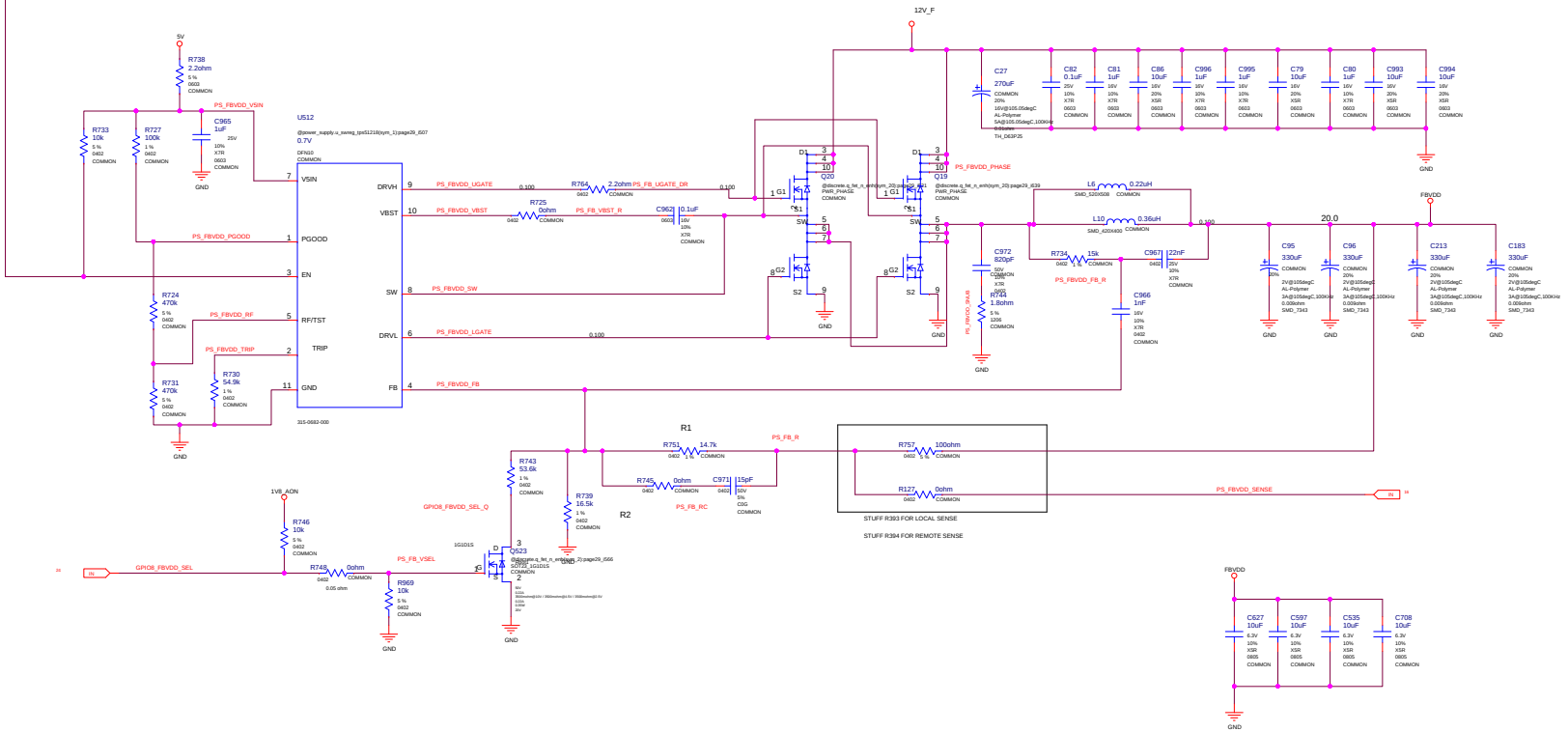
FBVDD	NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE

FBVDD/Q Enable



FBVDD DISCHARGE





SAMSUNG

GPIO8 LEVEL	FBVDDQ OUTPUT VOLTAGE
0	1.35V
1	1.55V

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: FBVDD

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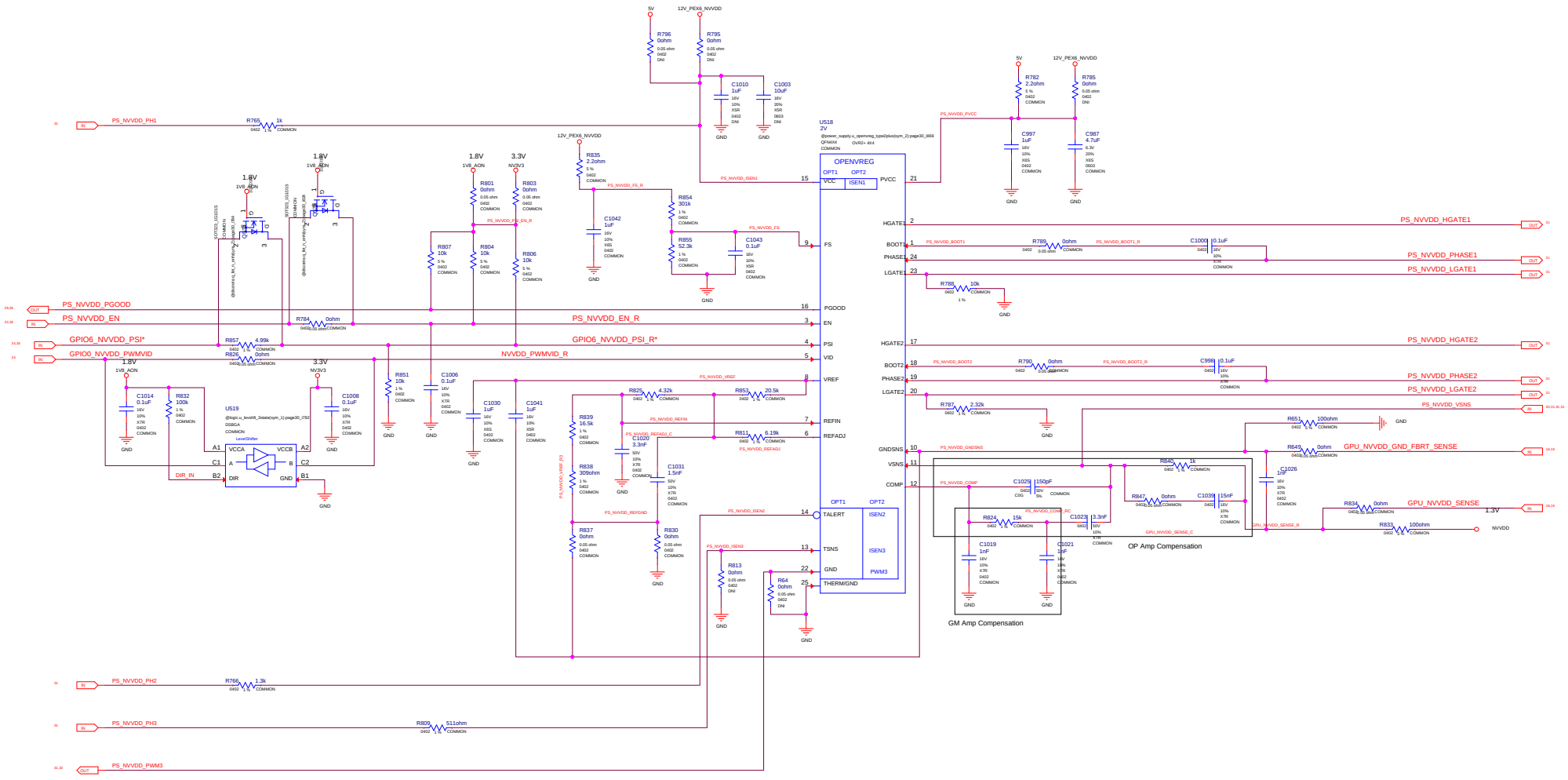
Page30: PS: NVVDD Controller



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD Controller

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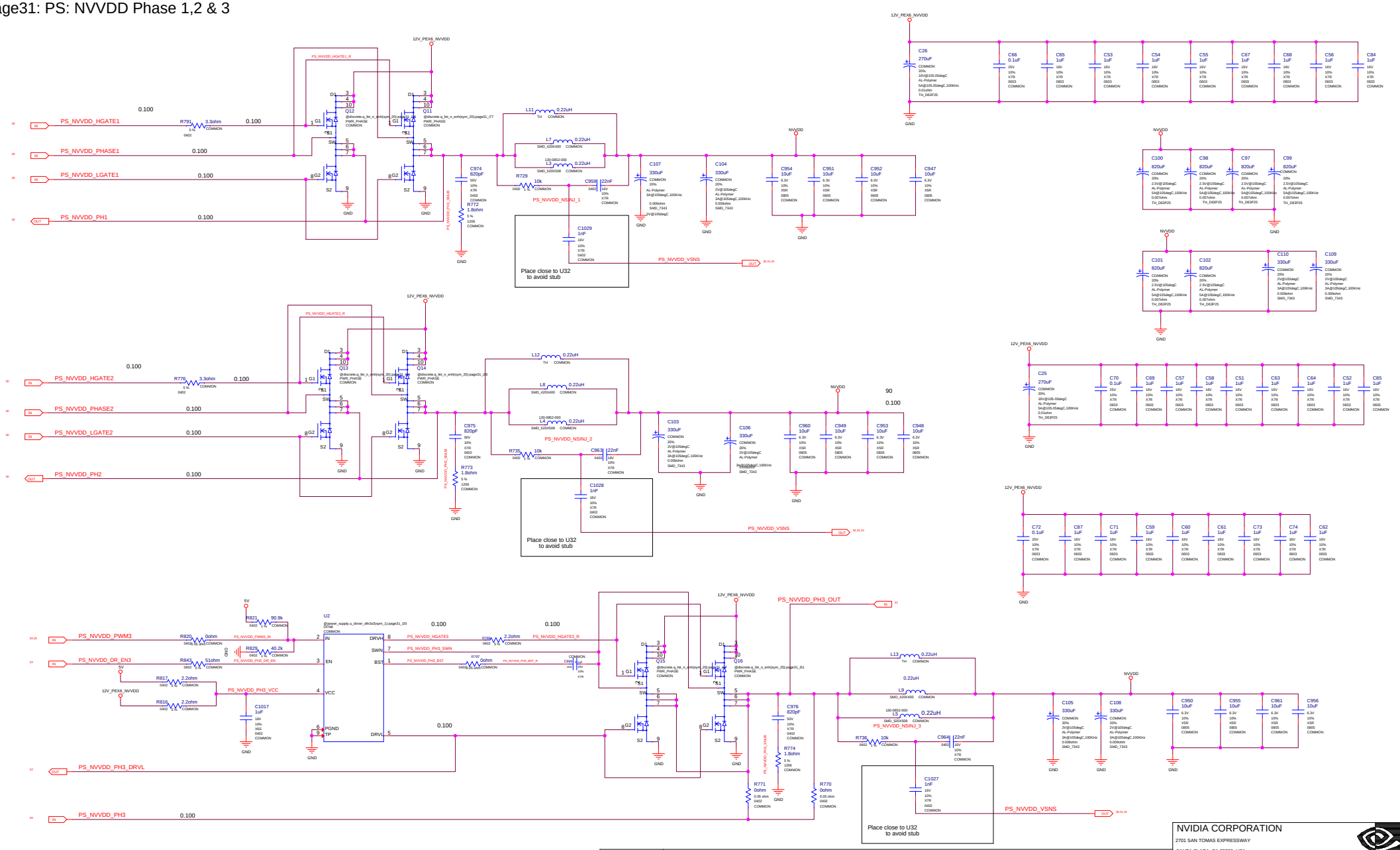
Page31: PS: NVVDD Phase 1,2 & 3



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD Phase 1,2 & 3

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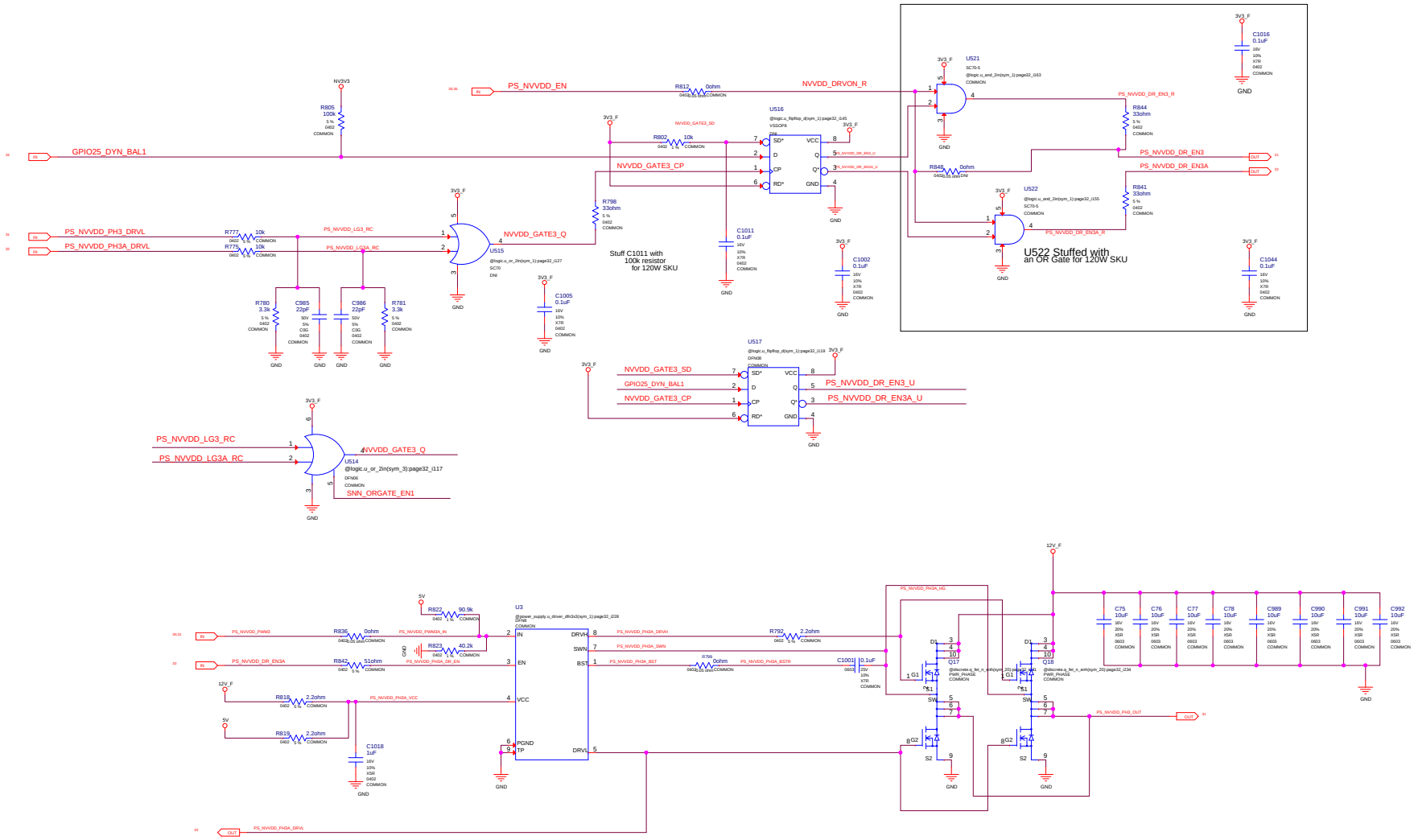
Page32: PS: NVVDD RAIL BALANCE LOGIC & DYNAMIC RAIL



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD Rail Balance Login & Dynamic Phase

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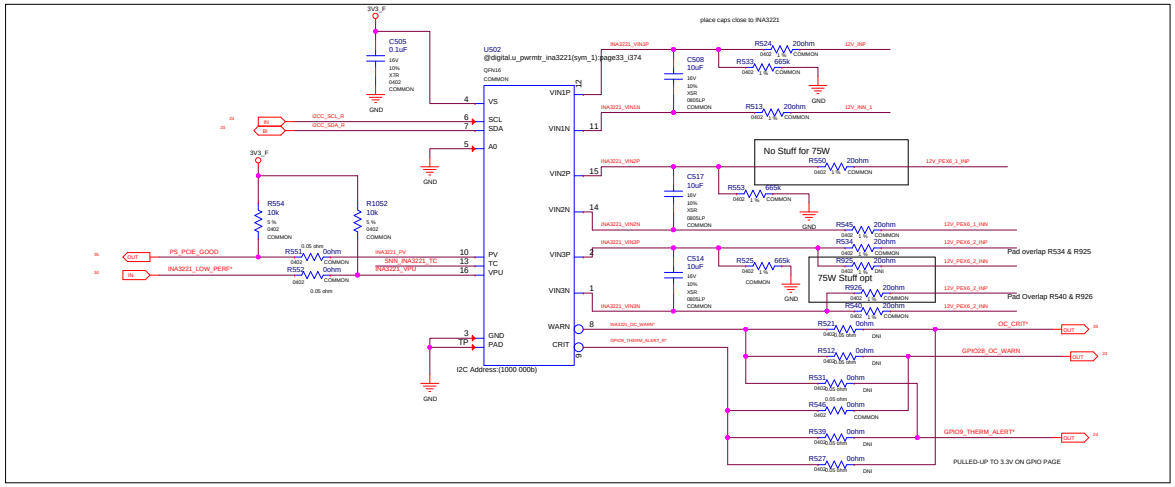
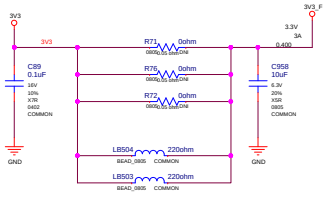
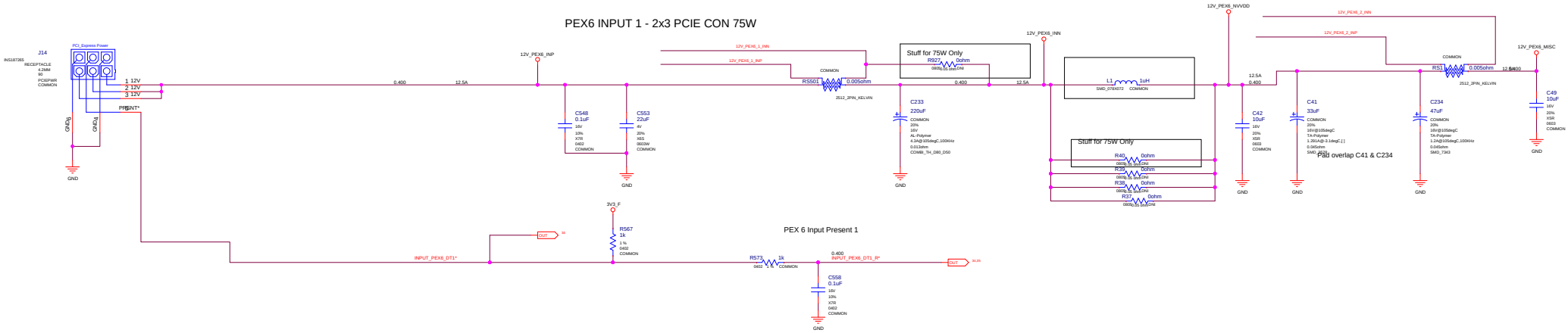
Page33: PS: Inputs, Filtering, and Monitoring



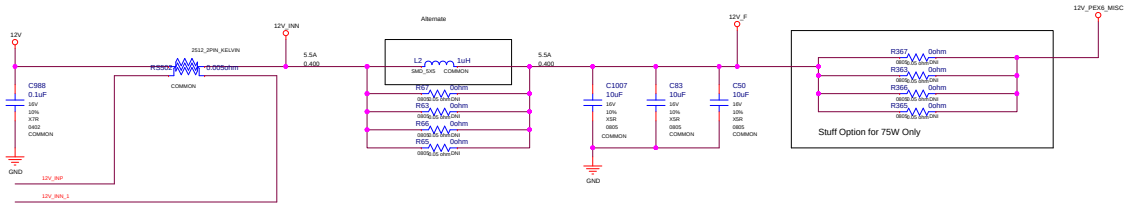
PEX 3V3 INPUT - 10W



PEX6 INPUT 1 - 2x3 PCIE CON 75W



PEX_12V INPUT - 66W



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Input, Filtering, and Monitoring

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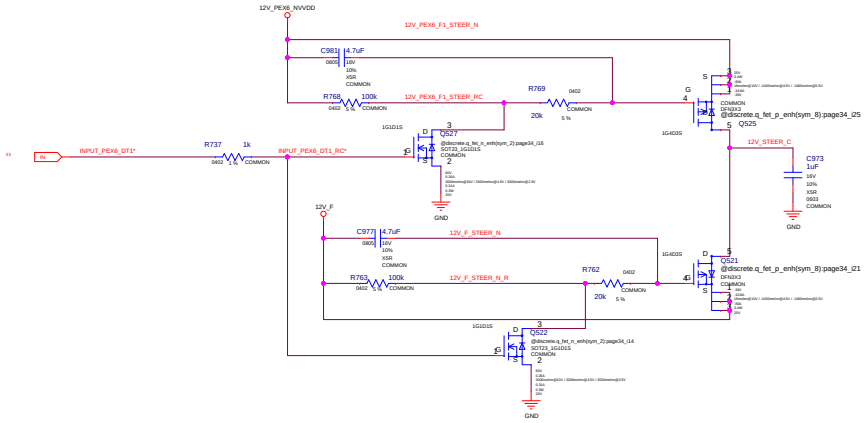
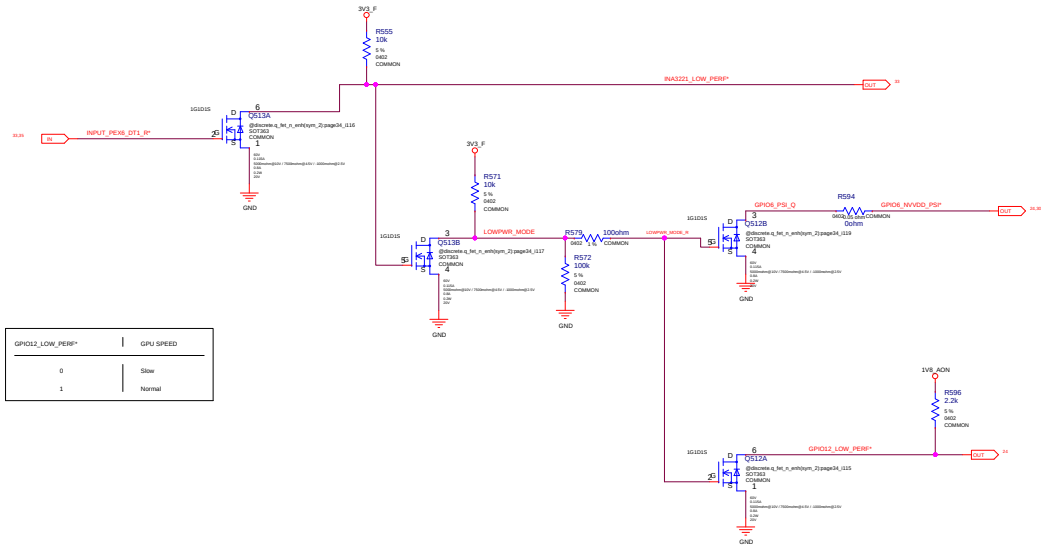
Page34: PS: 12V Current Steering, PSI Control, and LED

12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA

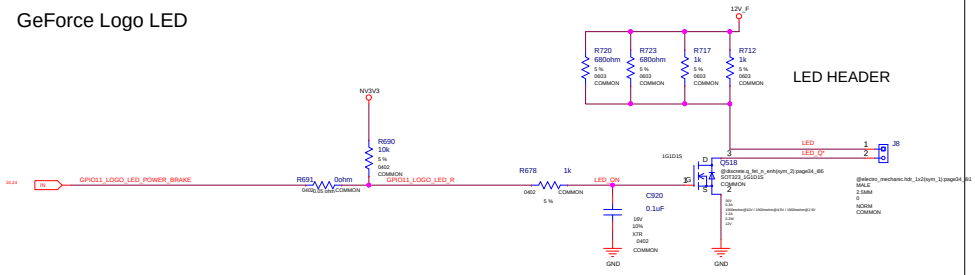


PEX Input - Power Level/PSI* Control



GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

GeForce Logo LED



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: 12V Power Steering,PSI Control & LED

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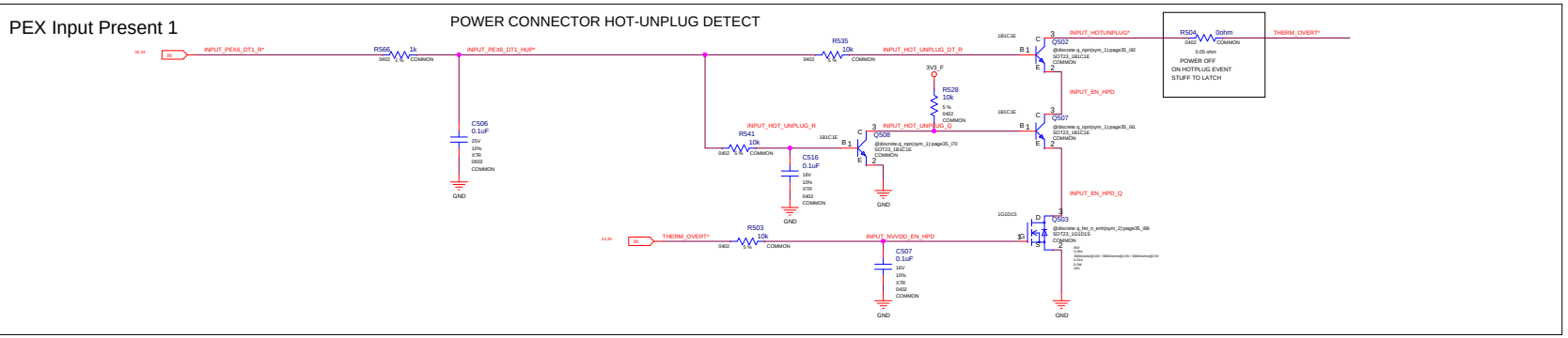
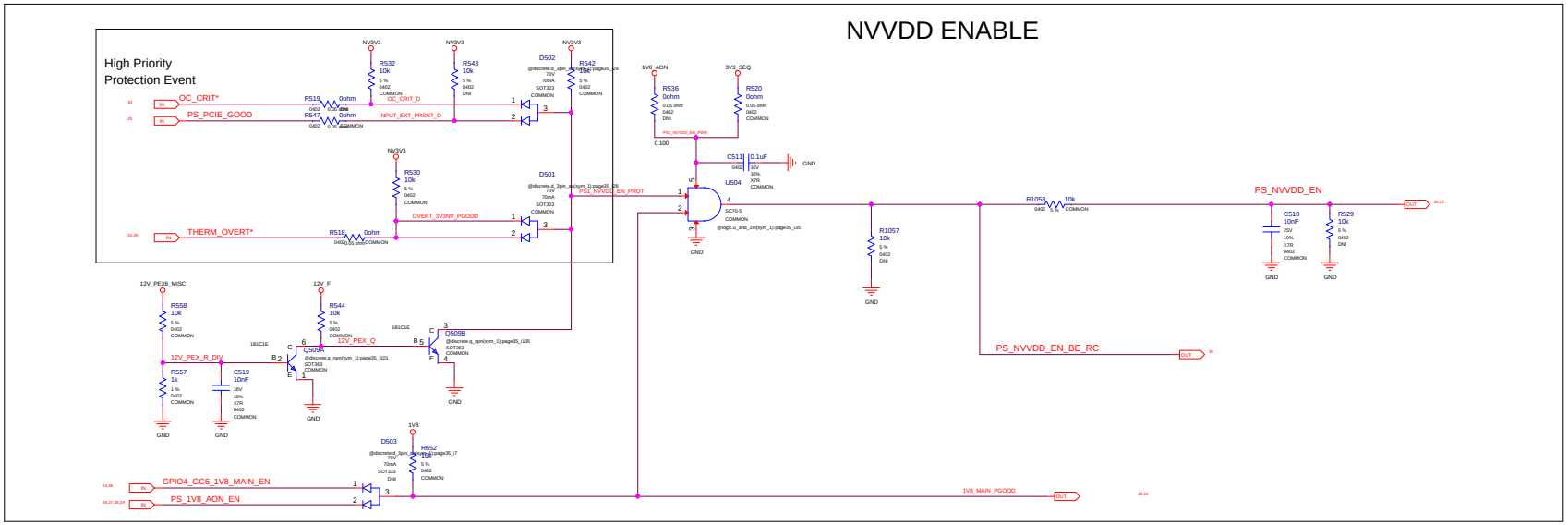
Page37: PS: Shutdown and Sequencing

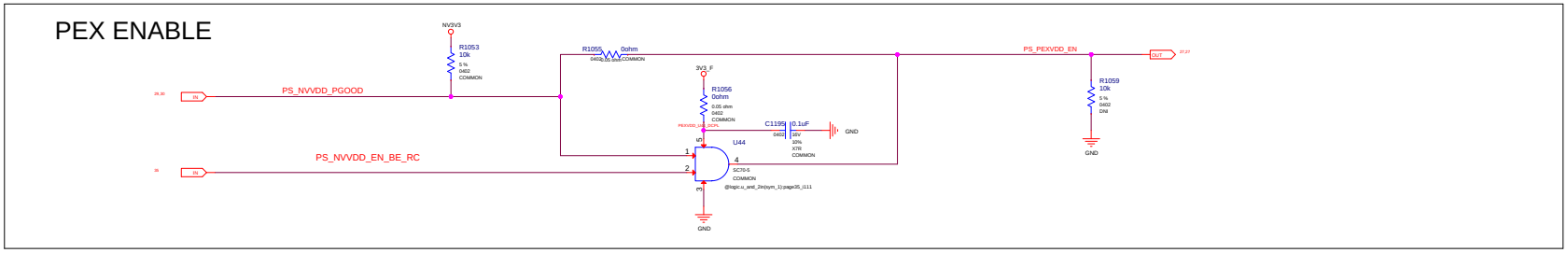
PEX Input Present 1



NVVDD ENABLE



PEX ENABLE



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Shut Down and Sequencing

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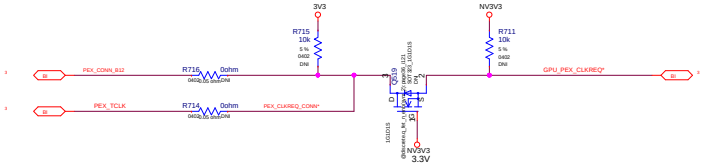
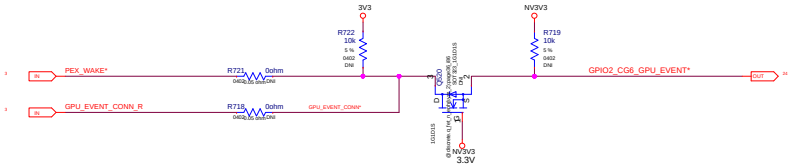
Page38: GC6 MISC

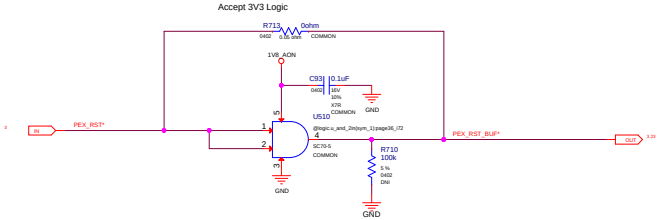
PEX_CLKREQ*



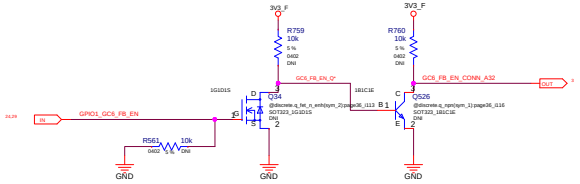
GPU_EVENT*



PEX_RST# LOGIC



GC6 FB ENABLE



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: GC6 MISC

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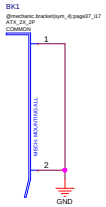
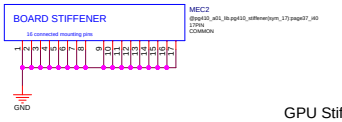
Page40: MECH

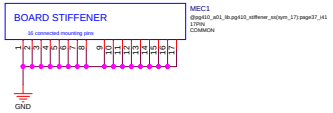
Brackets:



MOUNTING HOLES FOR HS DS:



MOUNTING HOLES FOR HS SS:

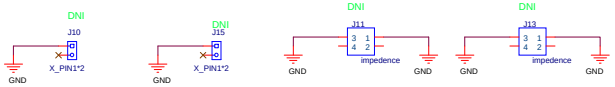


GPU Stiffener:

Vout = 0.8V * (1+Rt/Rb)

1.05V = 0.8V * (1+3.57k/11.5k)

Reserve J8 - J12 for Impedance check

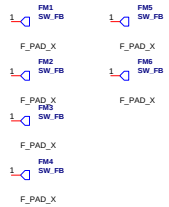


MEM Data
FBA_D<26>
L3
0.143MM / 40ohm +/- 10%
Reference L2 GND

MEM Data
FBA_D<9>
L6
0.144MM / 40ohm +/- 10%
Reference L7 GND

MEM CLK
FBD_CLK0 / FBD_CLK0*
L6
0.088MM / 0.1MM / 80ohm +/- 10%
Reference L7 GND

HDMI/DVI TMDS signals
IFPC_TXD0 / IFPC_TXD0*
L6
0.08MM / 0.206MM / 95ohm +/- 10%
Reference L7 GND



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MECH

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