PG411 A01

GP104 - 8GB GDDR5, 256b, 256Mx32
Tall DVI-D + DP + DP + HDMI + DP

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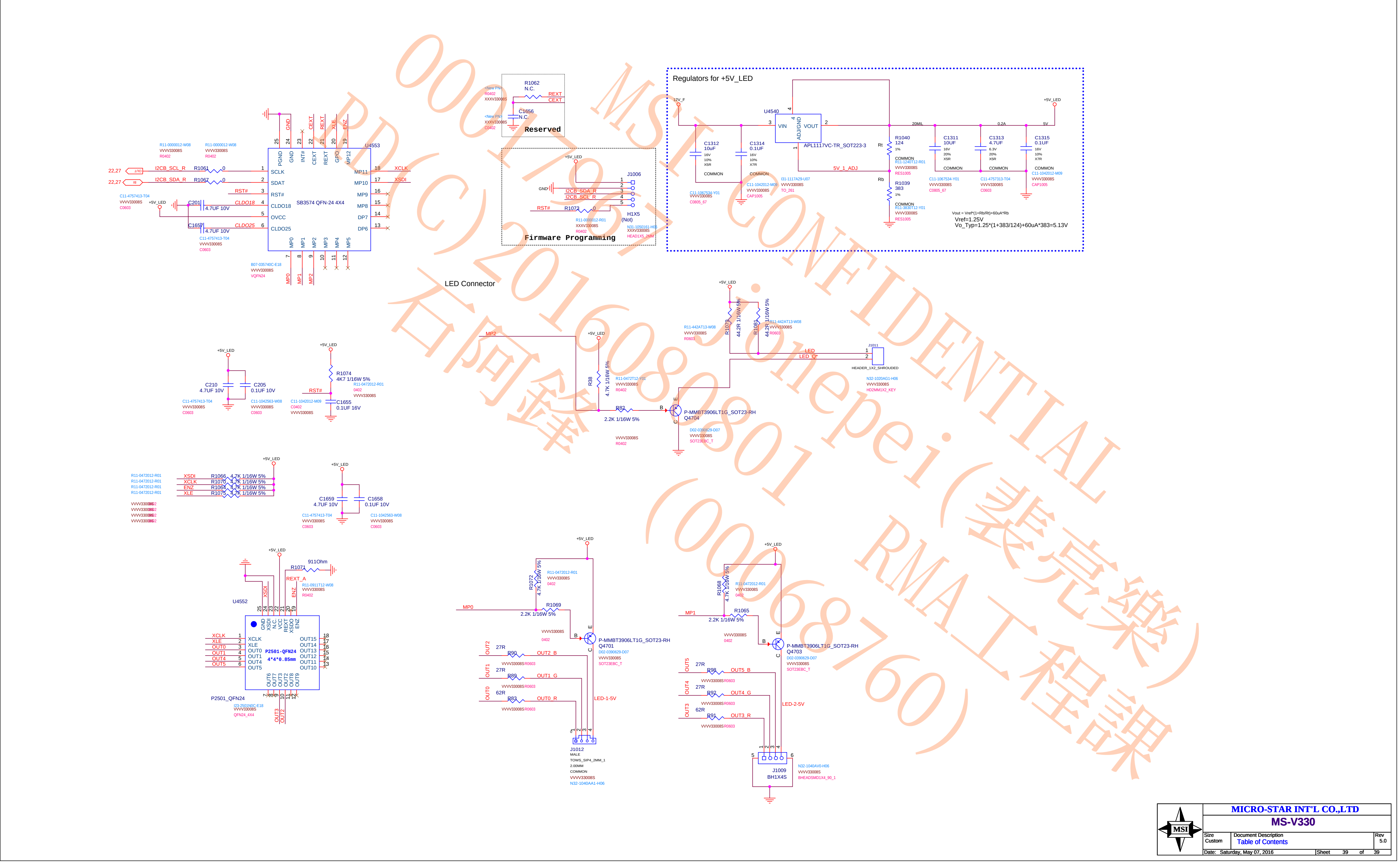
Page39: RGB LED



Regulators for +5V_LED
U4540
APL1117VC-TR_SOT223-3
VIN
VOUT
ADJ/GND
5V_1_ADJ
Vout = Vref*(1+Rb/Rt)+60uA*Rb
Vref=1.25V
Vo_Typ=1.25*(1+383/124)+60uA*383=5.13V
Reserved
R1062 N.C.
C1656 N.C.
Firmware Programming
J1006
H1X5 (Not)
U4553
SB3574 QFN-24 4X4
SCLK
SDAT
RST#
CLDO18
OVCC
CLDO25
I2CB_SCL_R
I2CB_SDA_R
LED Connector
J1011
HEADER_1X2_SHROUDED
P-MMBT3906LT1G_SOT23-RH
Q4704
Q4701
Q4703
U4552
P2501_QFN24
P2501-QFN24
4*4*0.85mm
J1012
J1009
BH1X4S
LED-1-5V
LED-2-5V
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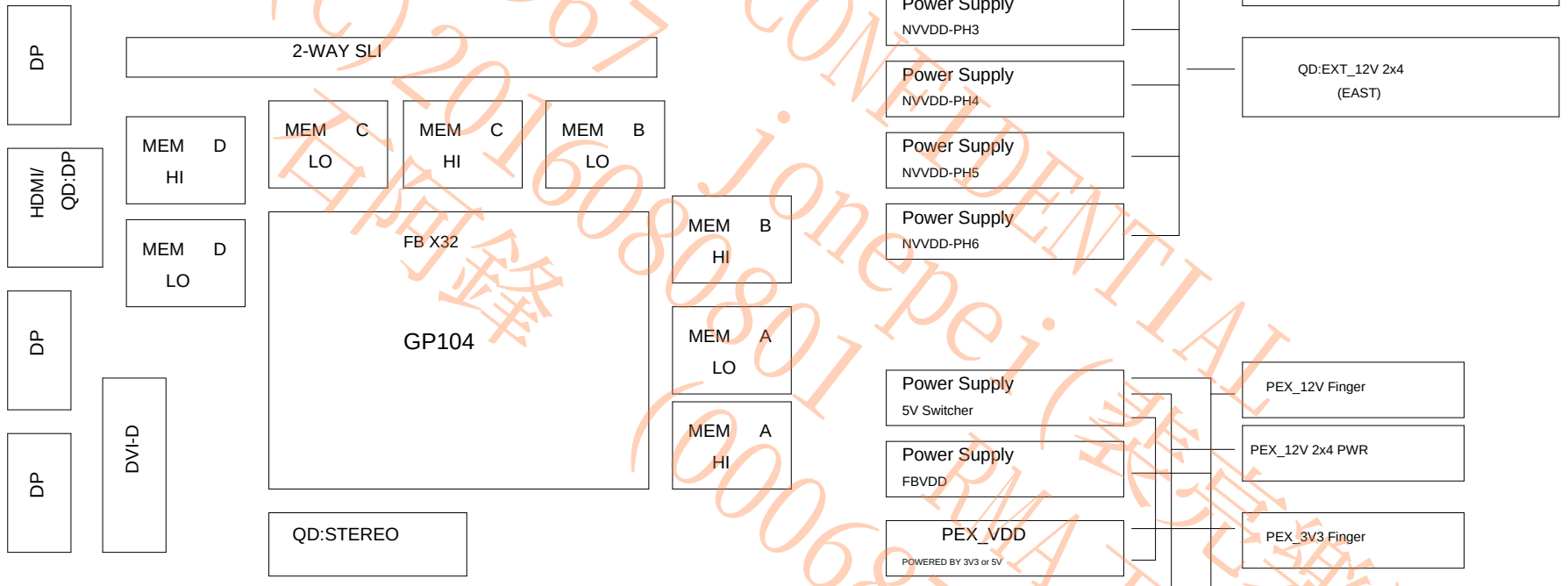
Page2: Block Diagram



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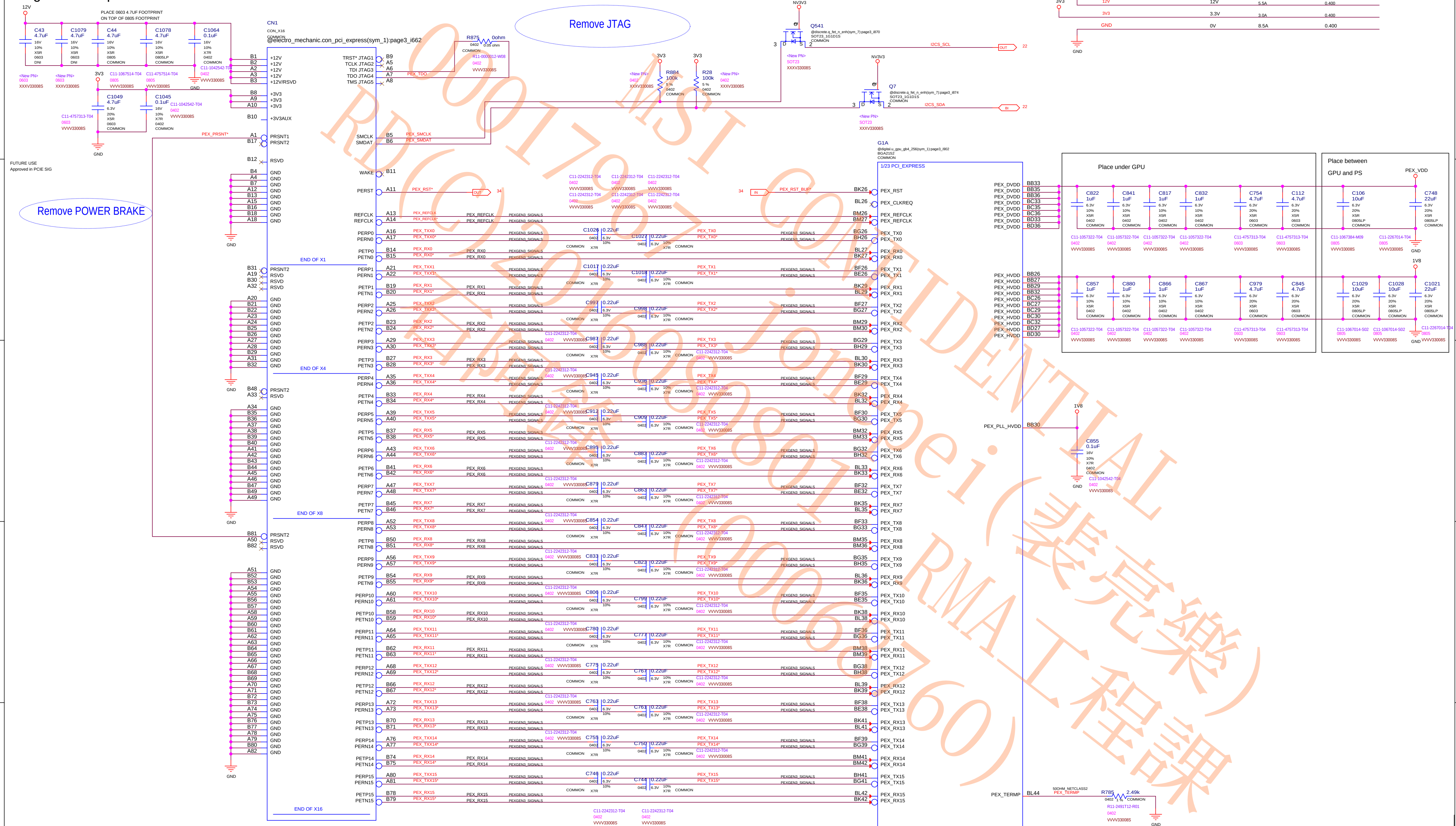
Page3: PCI Express



PLACE 0603 4.7UF FOOTPRINT
ON TOP OF 0805 FOOTPRINT
C43 4.7uF
C1079 4.7uF
C44 4.7uF
C1078 4.7uF
C1064 0.1uF
C1049 4.7uF
C1045 0.1uF
FUTURE USE
Approved in PCIE SIG
Remove POWER BRAKE
Remove JTAG
CN1
CON_X16
@electro_mechanic.con_pci_express(sym_1):page3_i662
+12V
+12V/RSVD
+3V3
+3V3AUX
PRSNT1
PRSNT2
RSVD
GND
TRST* JTAG1
TCLK JTAG2
TDI JTAG3
TDO JTAG4
TMS JTAG5
SMCLK
SMDAT
WAKE
PERST
REFCLK
END OF X1
END OF X4
END OF X8
END OF X16
R875 0ohm
R884 100k
R28 100k
Q541
Q7
I2CS_SCL
I2CS_SDA
G1A
@digital.u_gpu_gb4_256(sym_1):page3_i802
BGA2152
1/23 PCI_EXPRESS
PEX_RST
PEX_CLKREQ
PEX_REFCLK
PEX_TX0 … PEX_TX15
PEX_RX0 … PEX_RX15
PEX_DVDD
PEX_HVDD
PEX_PLL_HVDD
PEX_TERMP
R785 2.49k
C855 0.1uF
Place under GPU
Place between GPU and PS
PEX_VDD
NET | VOLTAGE | MAX_CURRENT | MIN_WIDTH
12V | 12V | 5.5A | 0.400
3V3 | 3.3V | 3.0A | 0.400
GND | 0V | 8.5A | 0.400

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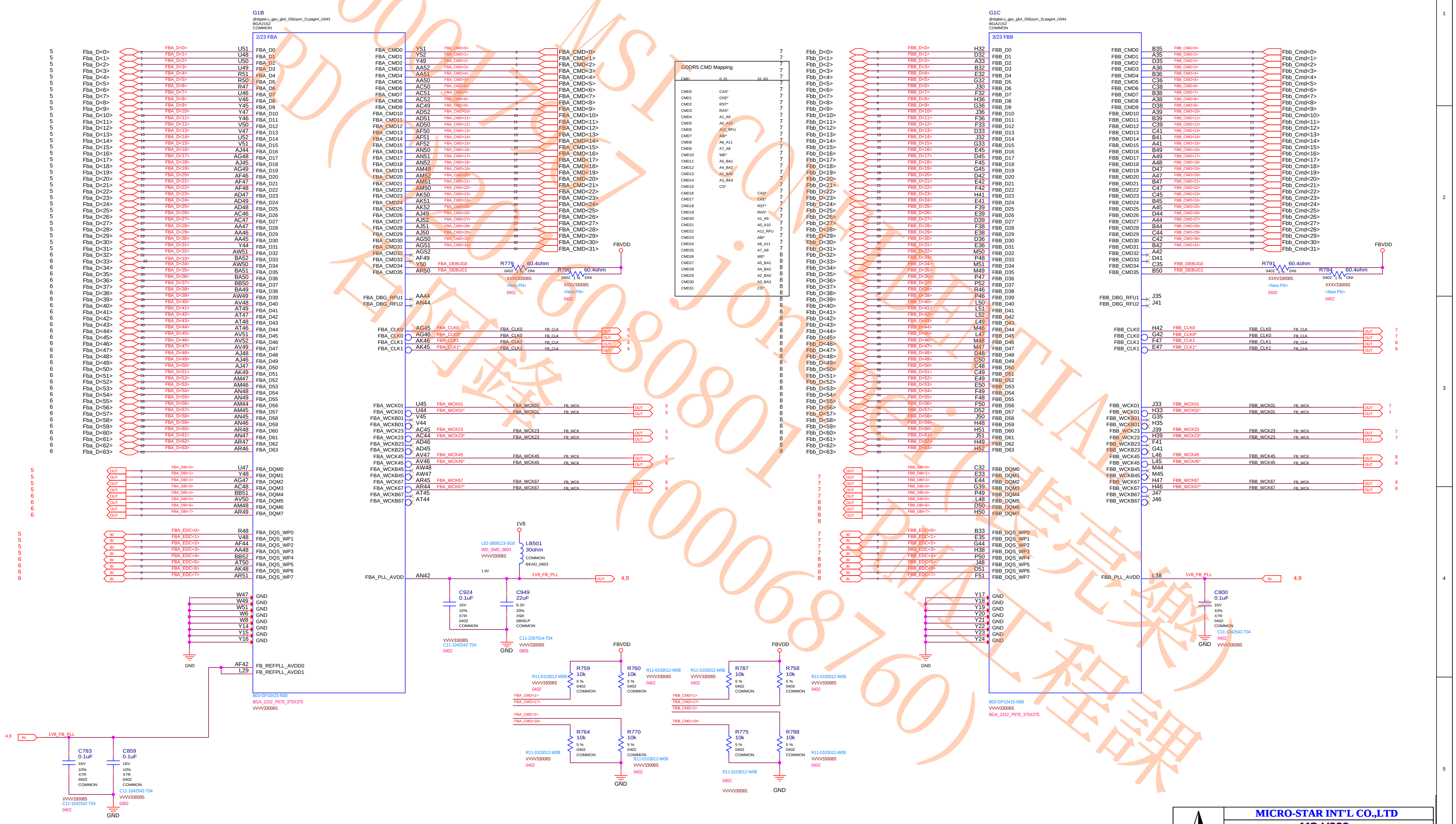
XXXV33008S

Page4: MEMORY: GPU Partition A/B



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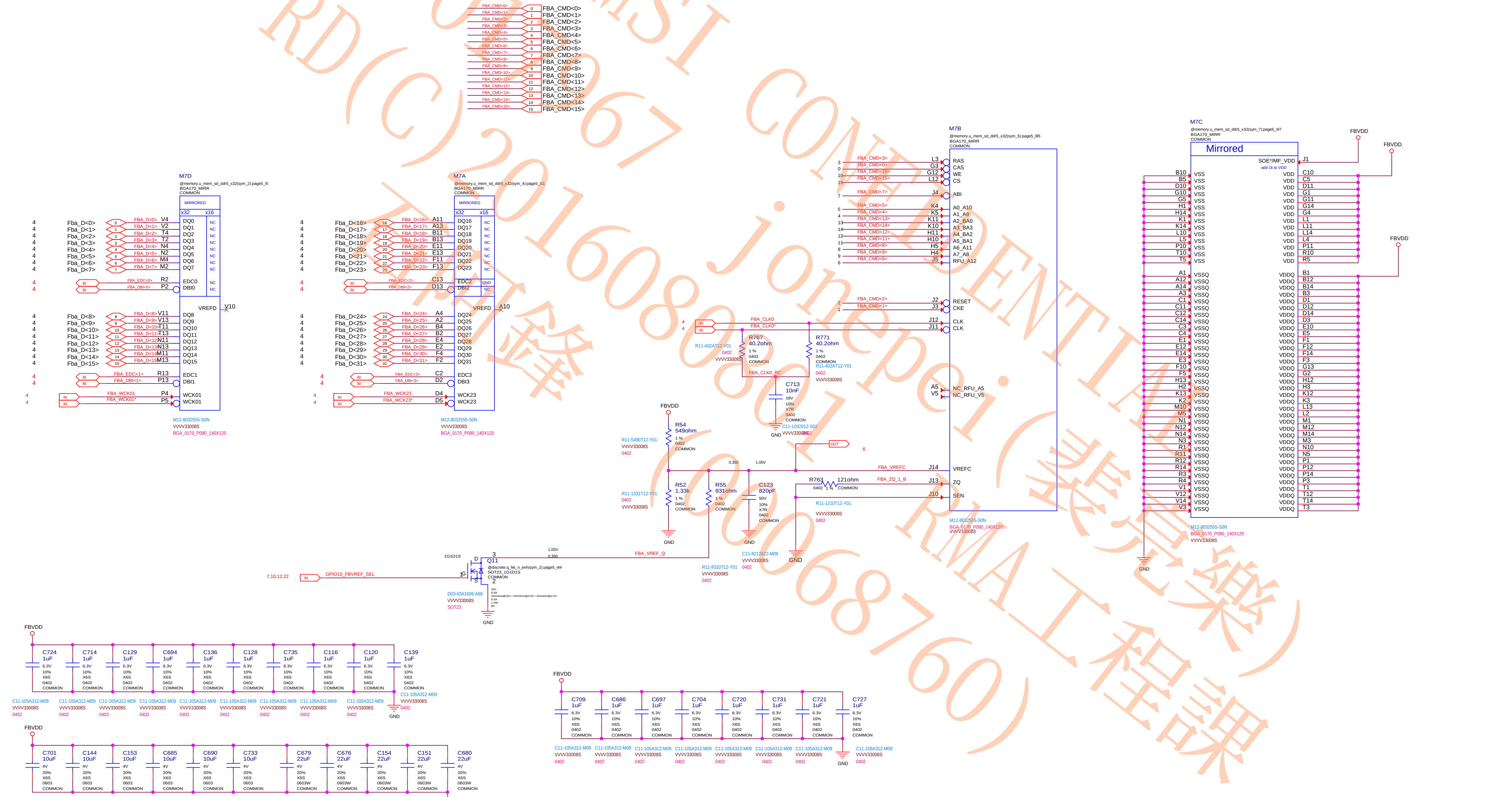
Page5: MEMORY: FBA Partition 31..0



M7D
M7A
M7B
M7C
Mirrored
FBA_CMD<0> … FBA_CMD<15>
Fba_D<0> … Fba_D<31>
VREFD
VREFC
ZQ
SEN
RESET
CKE
CLK
ABI
NC_RFU_A5
NC_RFU_V5
SOE*/MF_VDD
VSS
VDD
VSSQ
VDDQ
FBVDD
GND
FBA_VREF_C
FBA_VREF_Q
FBA_ZQ_1_8
FBA_CLK0
FBA_CLK0*
FBA_WCK01
FBA_WCK23
GPIO10_FBVREF_SEL
Q11
R54 549ohm
R52 1.33k
R55 931ohm
R767 40.2ohm
R771 40.2ohm
R763 121ohm
C713 10nF
C123 820pF
C724 1uF
C714 1uF
C129 1uF
C694 1uF
C136 1uF
C128 1uF
C735 1uF
C116 1uF
C120 1uF
C139 1uF
C701 10uF
C144 10uF
C153 10uF
C685 10uF
C690 10uF
C733 10uF
C679 22uF
C676 22uF
C154 22uF
C151 22uF
C680 22uF
C709 1uF
C686 1uF
C697 1uF
C704 1uF
C720 1uF
C731 1uF
C721 1uF
C727 1uF

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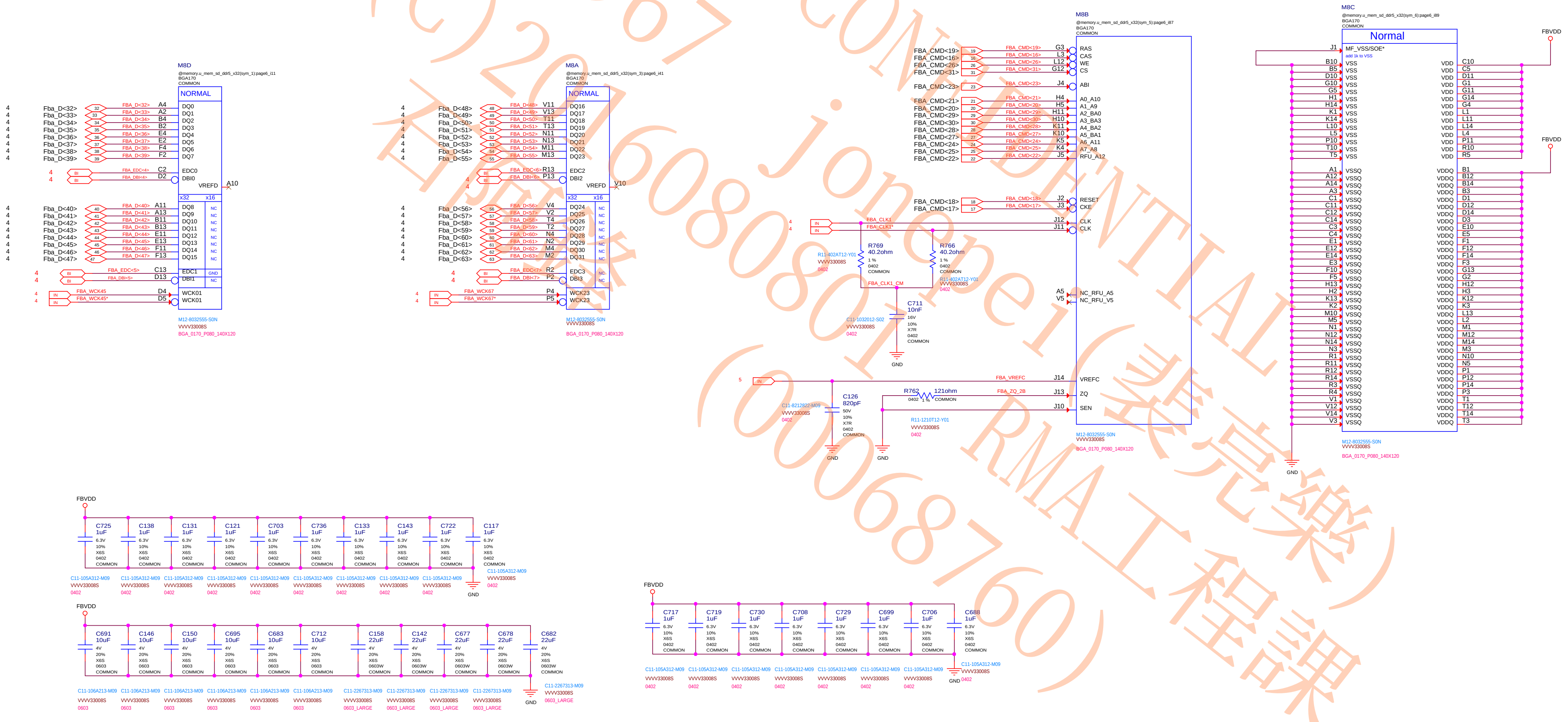
Page6: MEMORY: FBA Partition 63..32



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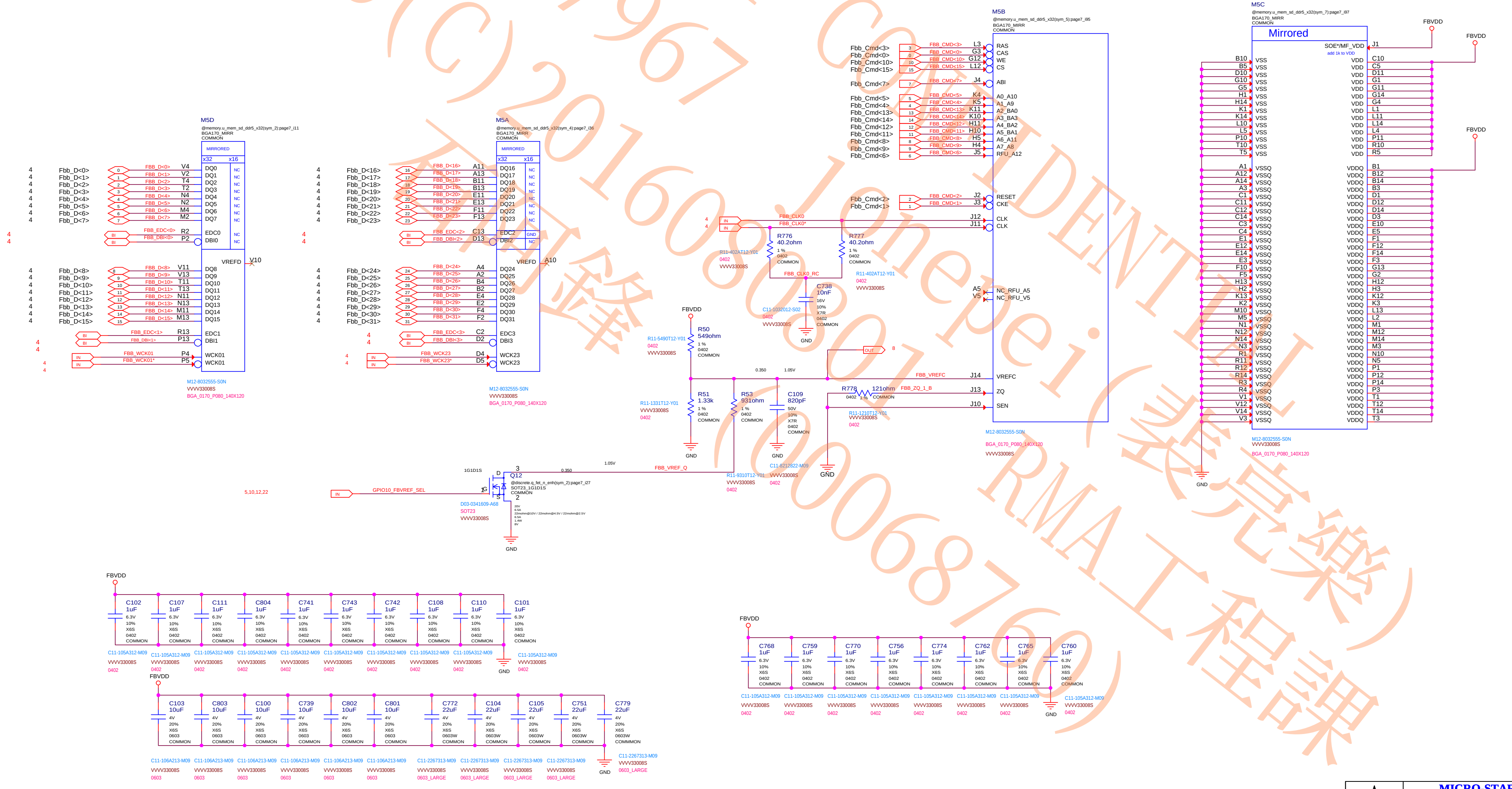
Page7: MEMORY: FBB Partition 31..0



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Page8: MEMORY: FBB Partition 63..32

M6D
NORMAL
M6A
NORMAL
M6B
M6C
Normal
FBVDD
GND
VREFD
VREFC
RAS
CAS
WE
CS
ABI
RESET
CKE
CLK
ZQ
SEN
NC_RFU_A5
NC_RFU_V5
MF_VSS/SOE*
VSS
VSSQ
VDD
VDDQ
WCK01
WCK23
EDC0
DBI0
EDC1
DBI1
EDC2
DBI2
EDC3
DBI3
R768 40.2ohm
R765 40.2ohm
R761 121ohm
C710 10nF
C124 820pF
FBB_VREFC
FBB_ZQ_2B
FBB_CLK1
FBB_CLK1*
FBB_CLK1_CM
FBB_WCK45
FBB_WCK45*
FBB_WCK67
FBB_WCK67*
C723 1uF
C137 1uF
C115 1uF
C141 1uF
C130 1uF
C702 1uF
C135 1uF
C715 1uF
C734 1uF
C119 1uF
C155 10uF
C696 10uF
C148 10uF
C152 10uF
C689 10uF
C684 10uF
C681 22uF
C156 22uF
C675 22uF
C674 22uF
C732 22uF
C726 1uF
C728 1uF
C707 1uF
C718 1uF
C705 1uF
C716 1uF
C698 1uF
C687 1uF

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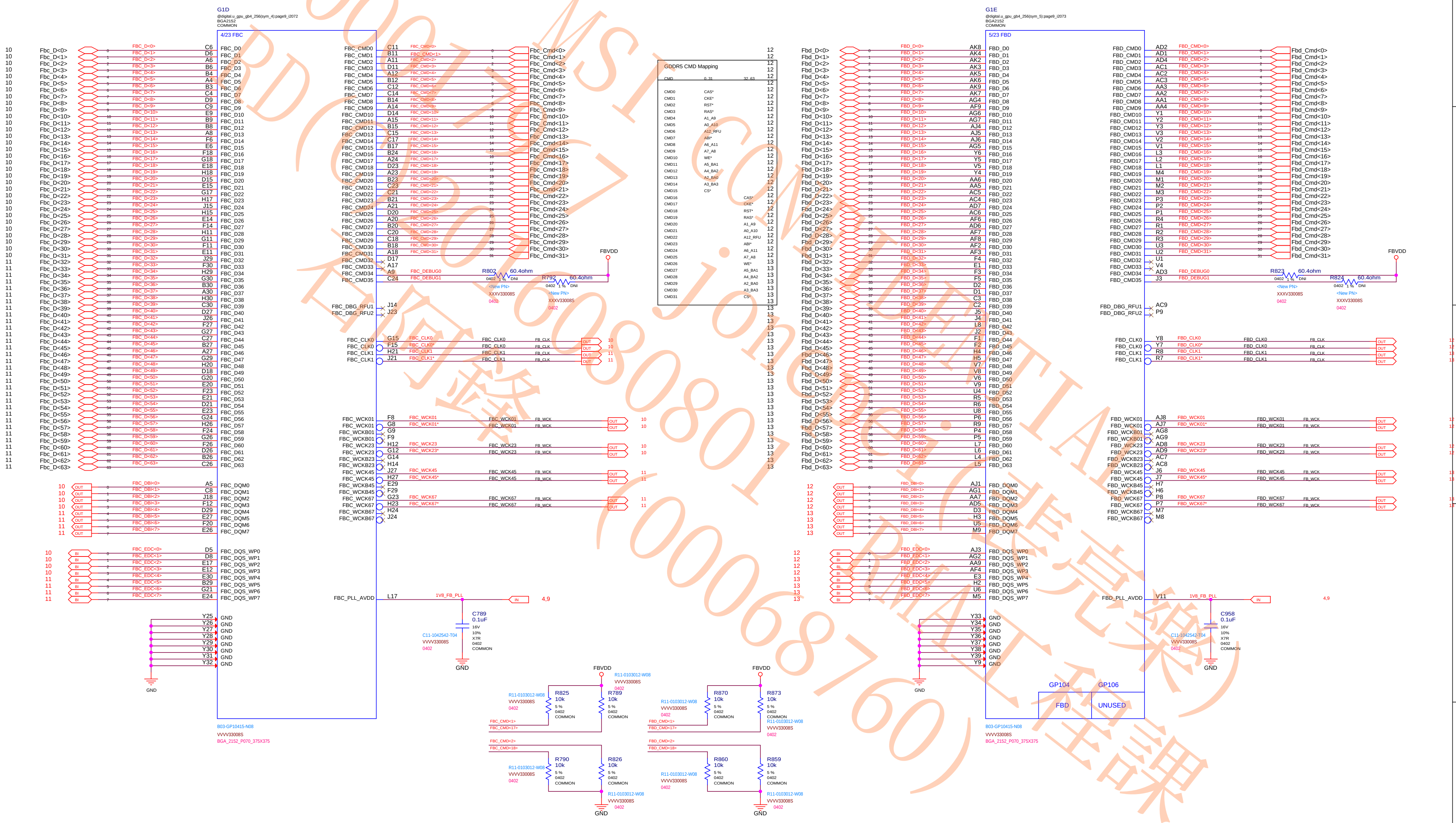
Page9: MEMORY: GPU Partition C/D



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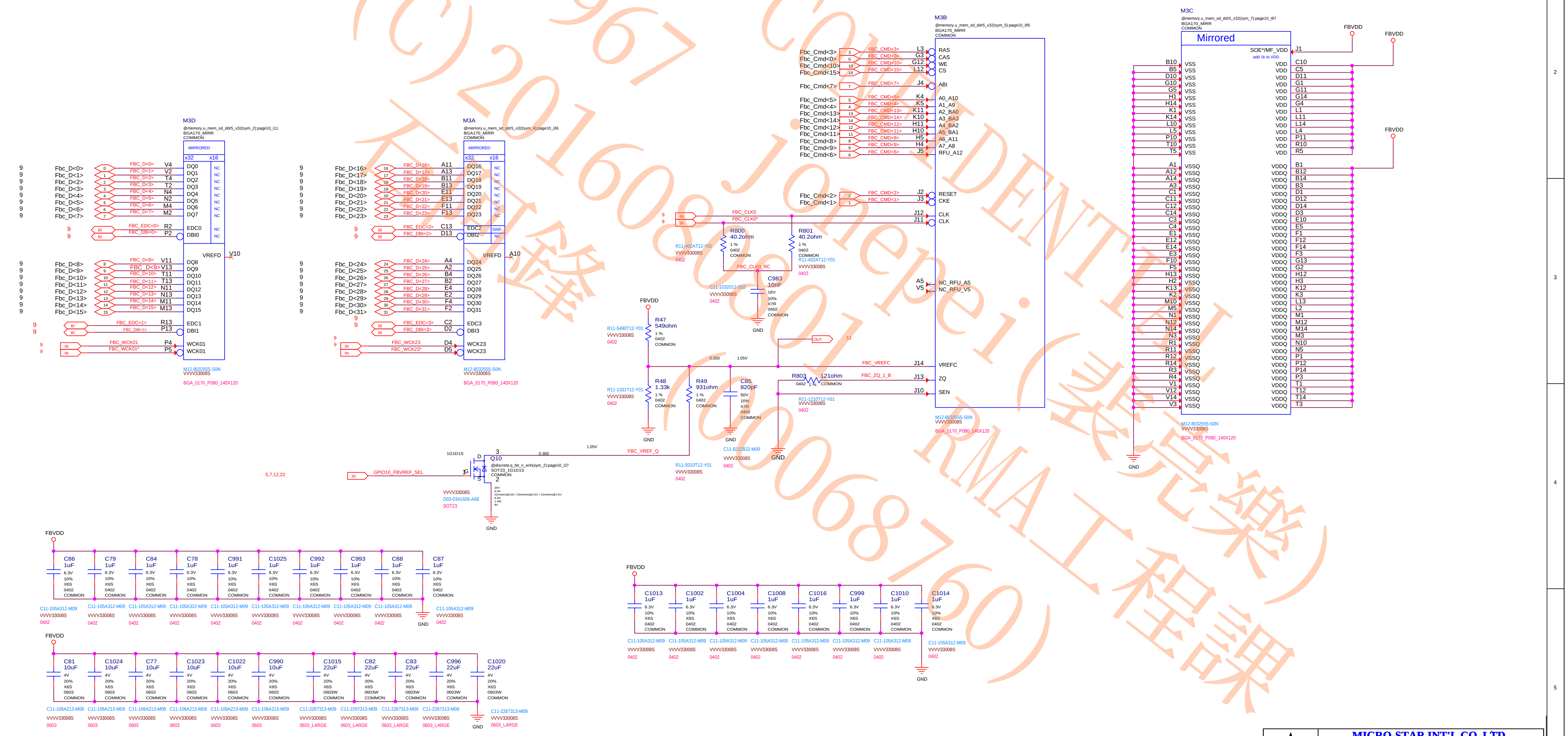
Page10: MEMORY: FBC Partition 31..0



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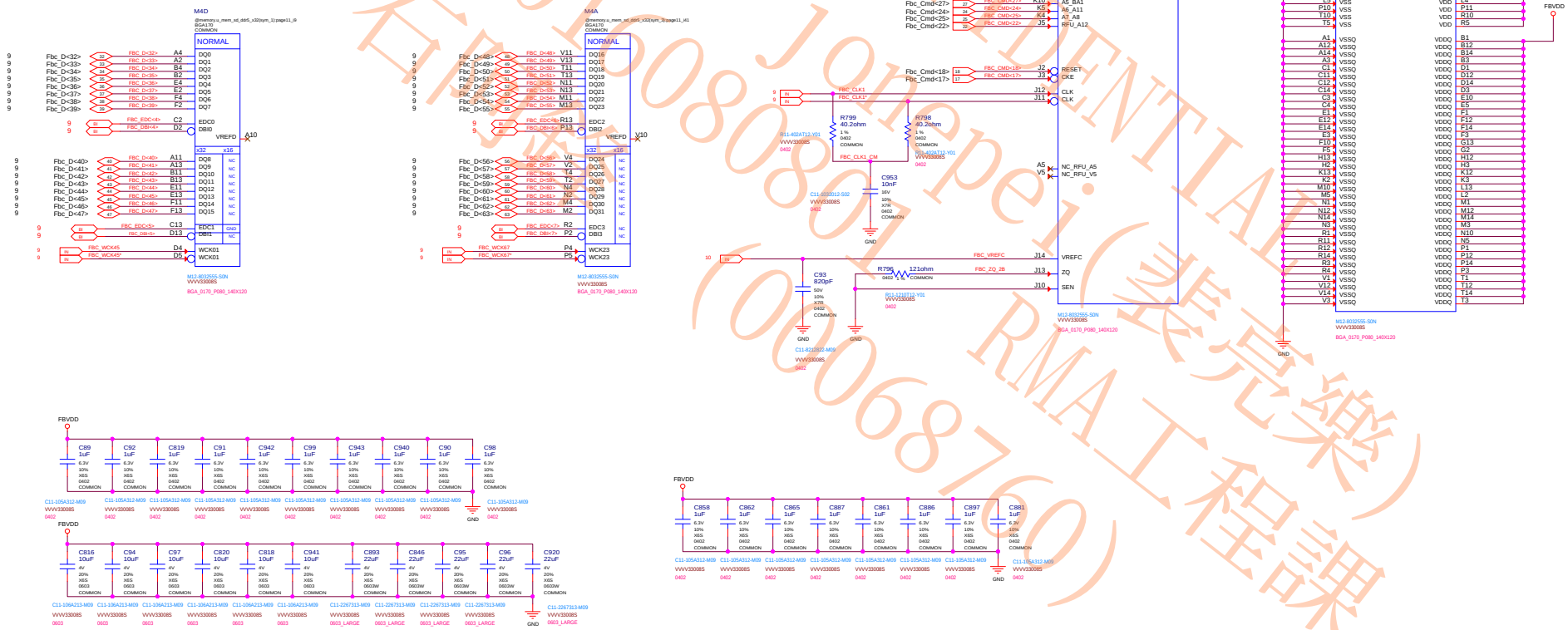
Page11: MEMORY: FBC Partition 63..32



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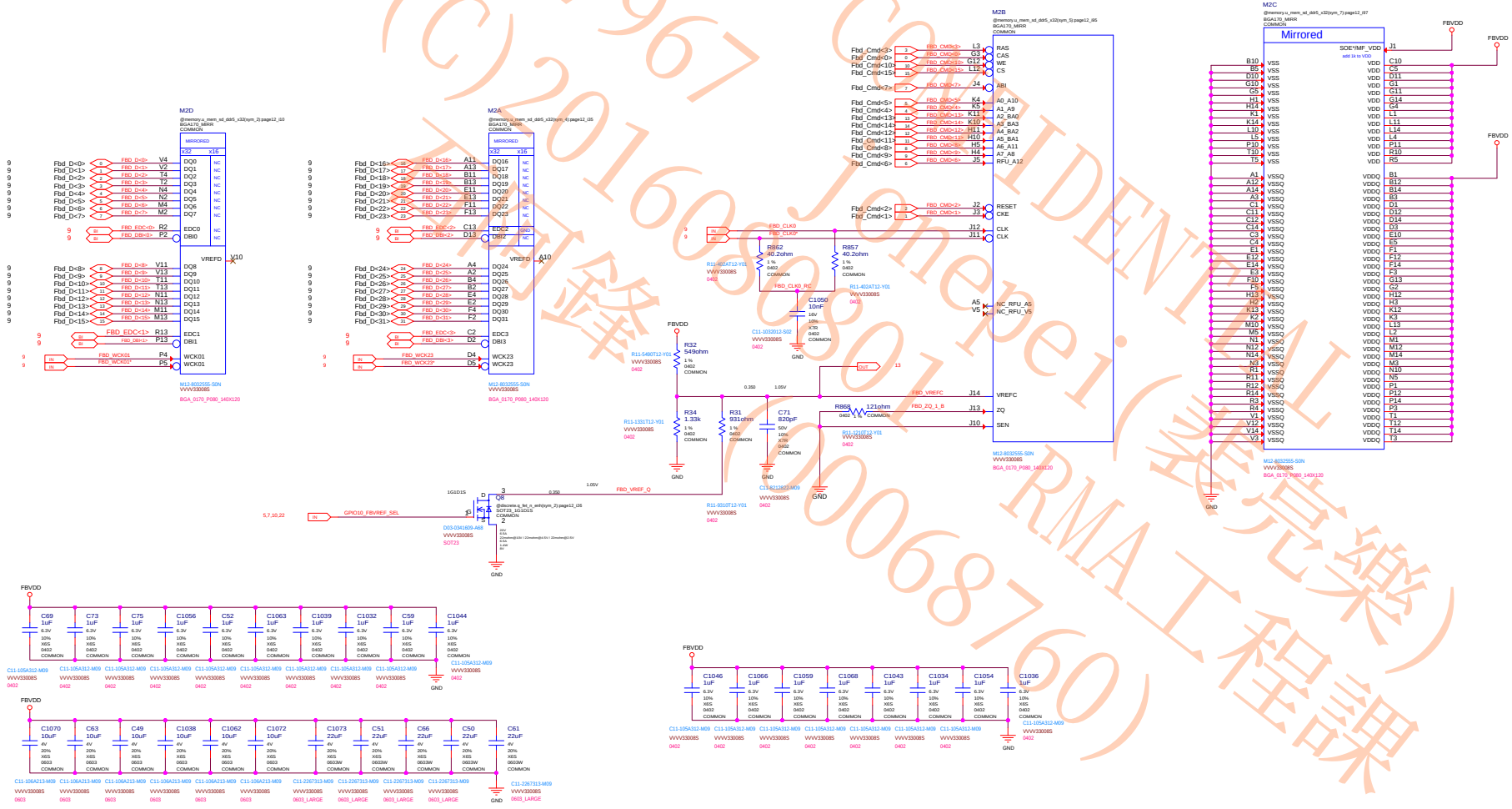

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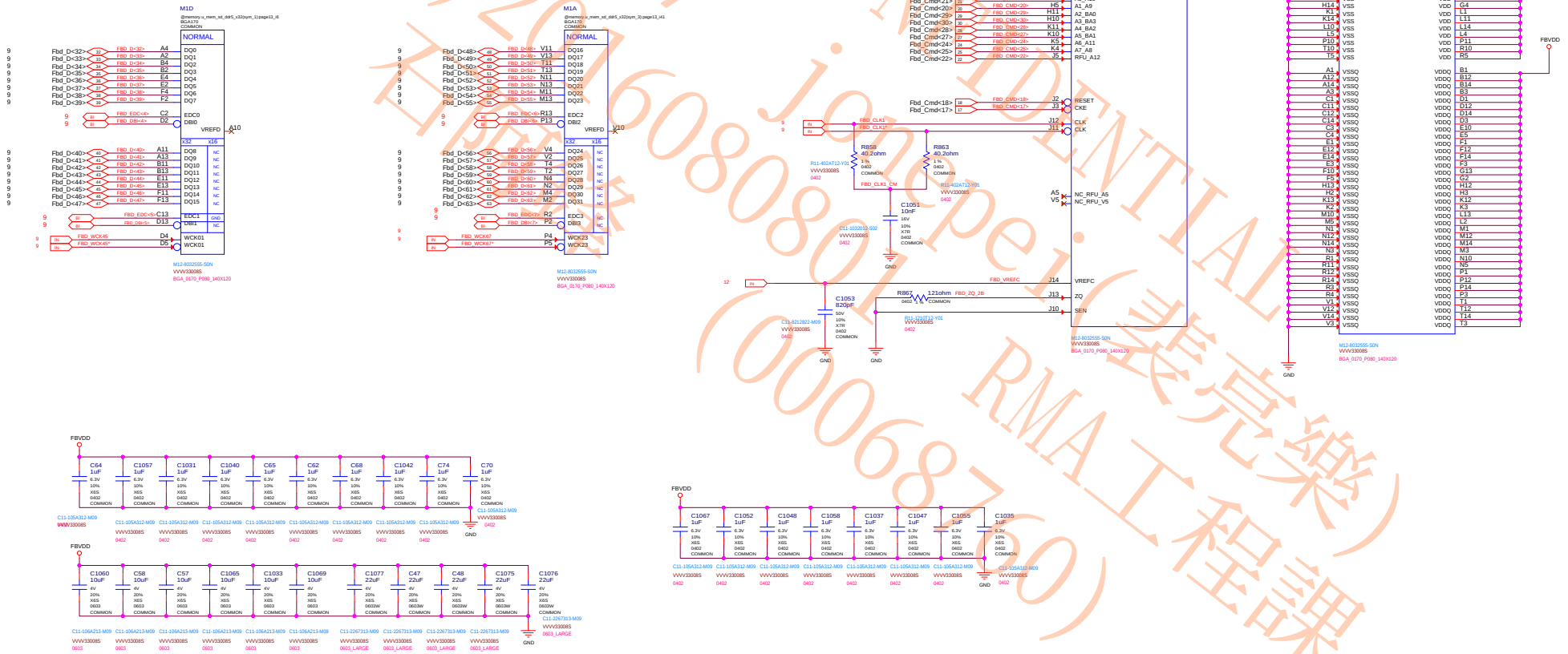
Page13: MEMORY: FBD Partition 63..32



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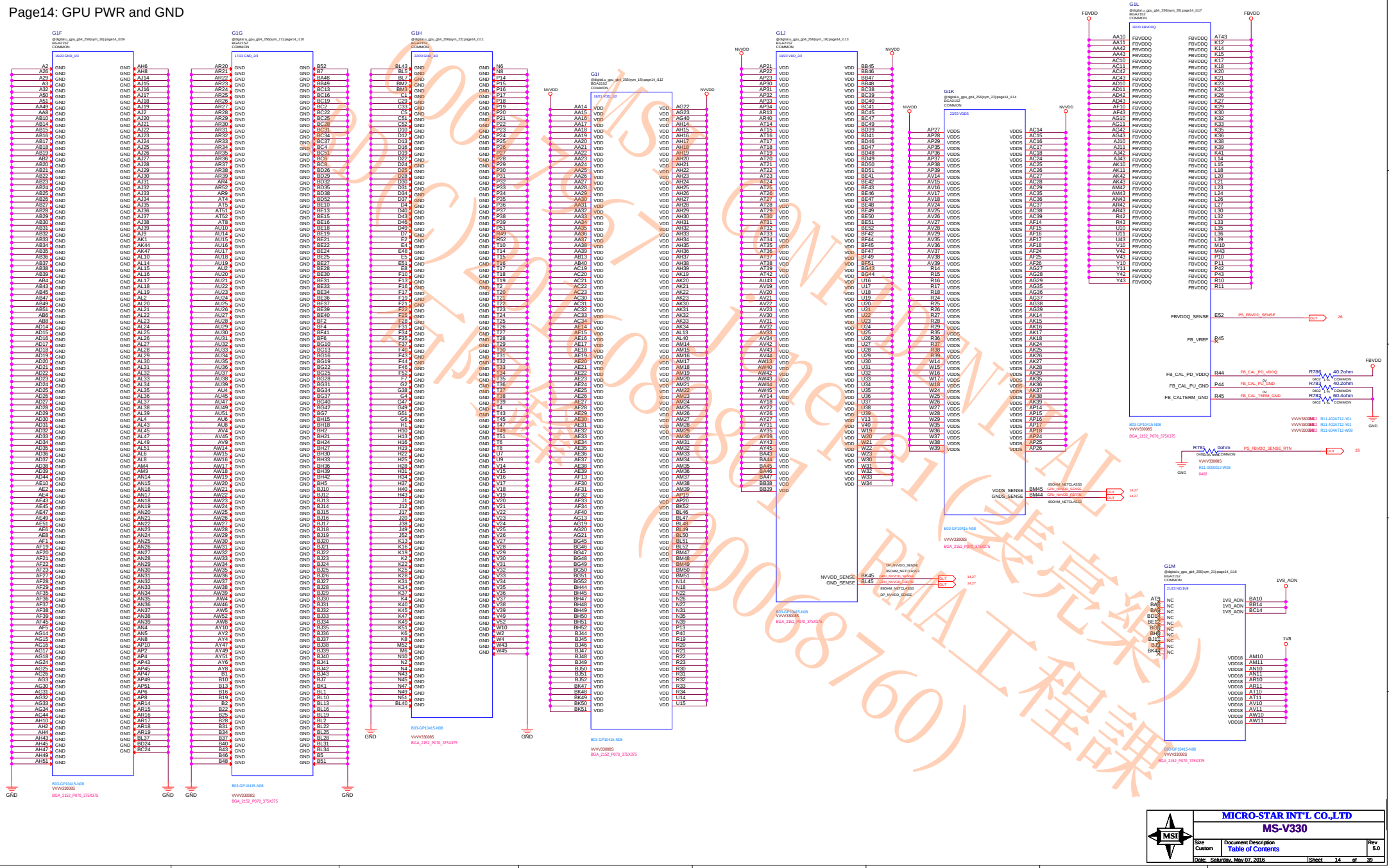
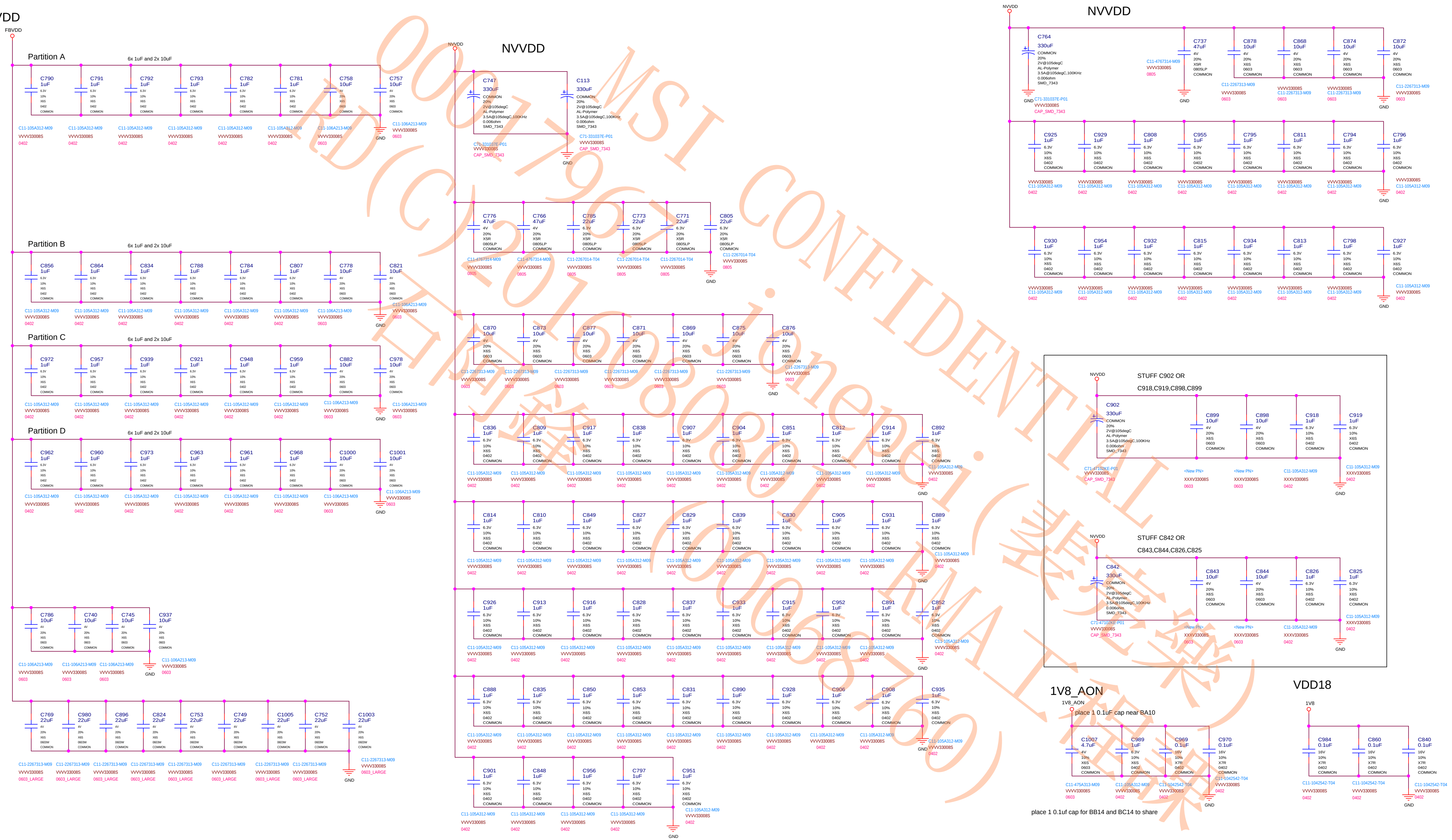
Page14: GPU PWR and GND



Page15: GPU Decoupling



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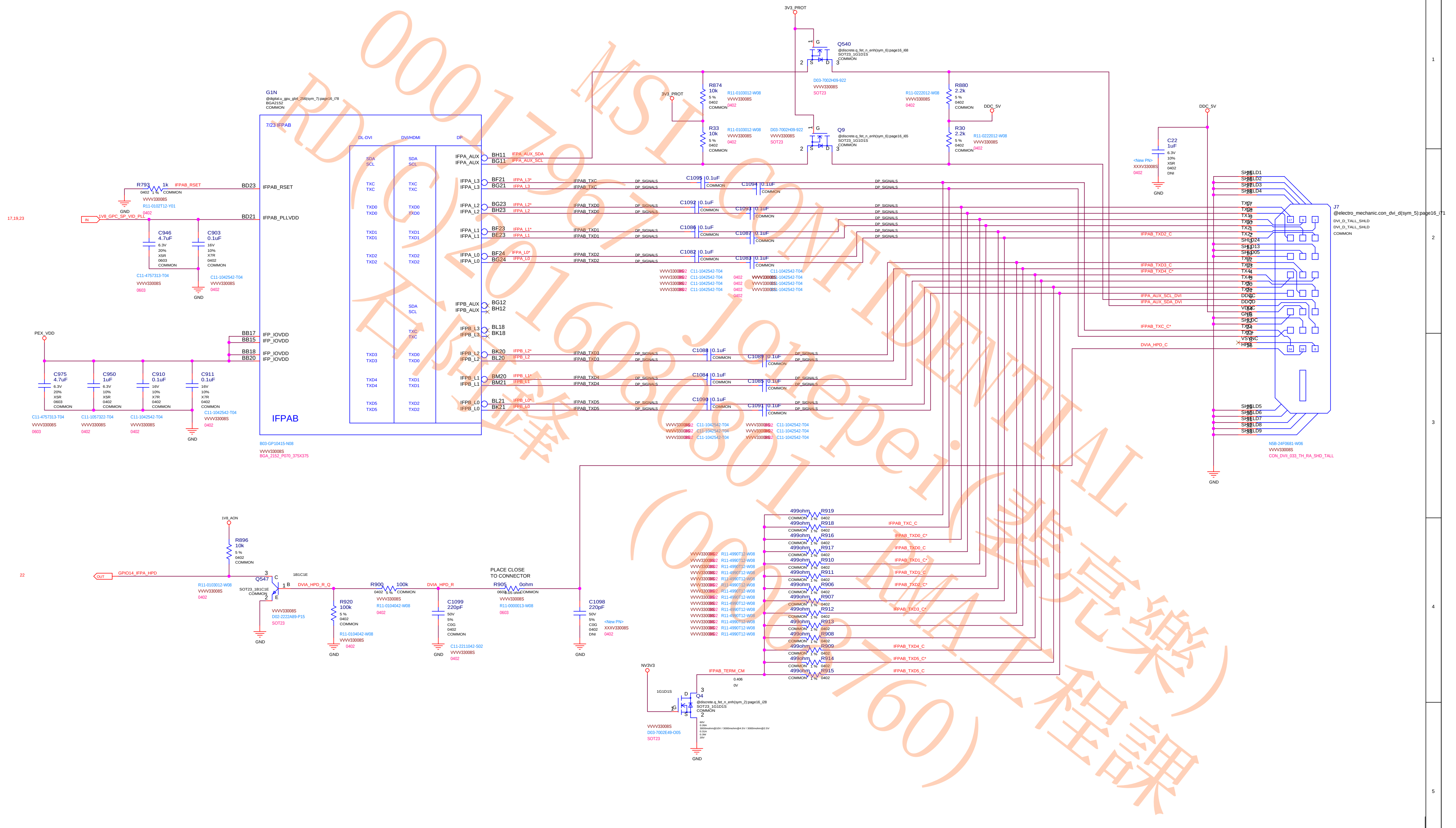
Page16: IFPAB DVI-D-DL



3V3_PROT
Q540
Q9
R874 10k
R33 10k
R880 2.2k
R30 2.2k
DDC_5V
C22 1uF
G1N
7/23 IFPAB
DL-DVI
DVI/HDMI
DP
IFPAB_RSET
IFPAB_PLLVDD
IFP_IOVDD
IFPAB
R793 1k
C946 4.7uF
C903 0.1uF
C975 4.7uF
C950 1uF
C910 0.1uF
C911 0.1uF
PEX_VDD
1V8_GPC_SP_VID_PLL
IFPA_AUX_SDA
IFPA_AUX_SCL
IFPAB_TXC
IFPAB_TXD0
IFPAB_TXD1
IFPAB_TXD2
IFPAB_TXD3
IFPAB_TXD4
IFPAB_TXD5
DP_SIGNALS
J7
DVIA_HPD_C
1V8_AON
R896 10k
Q547
GPIO14_IFPA_HPD
DVIA_HPD_R_Q
R900 100k
R920 100k
DVIA_HPD_R
C1099 220pF
PLACE CLOSE
TO CONNECTOR
R905 0ohm
C1098 220pF
NV3V3
Q4
IFPAB_TERM_CM
GND

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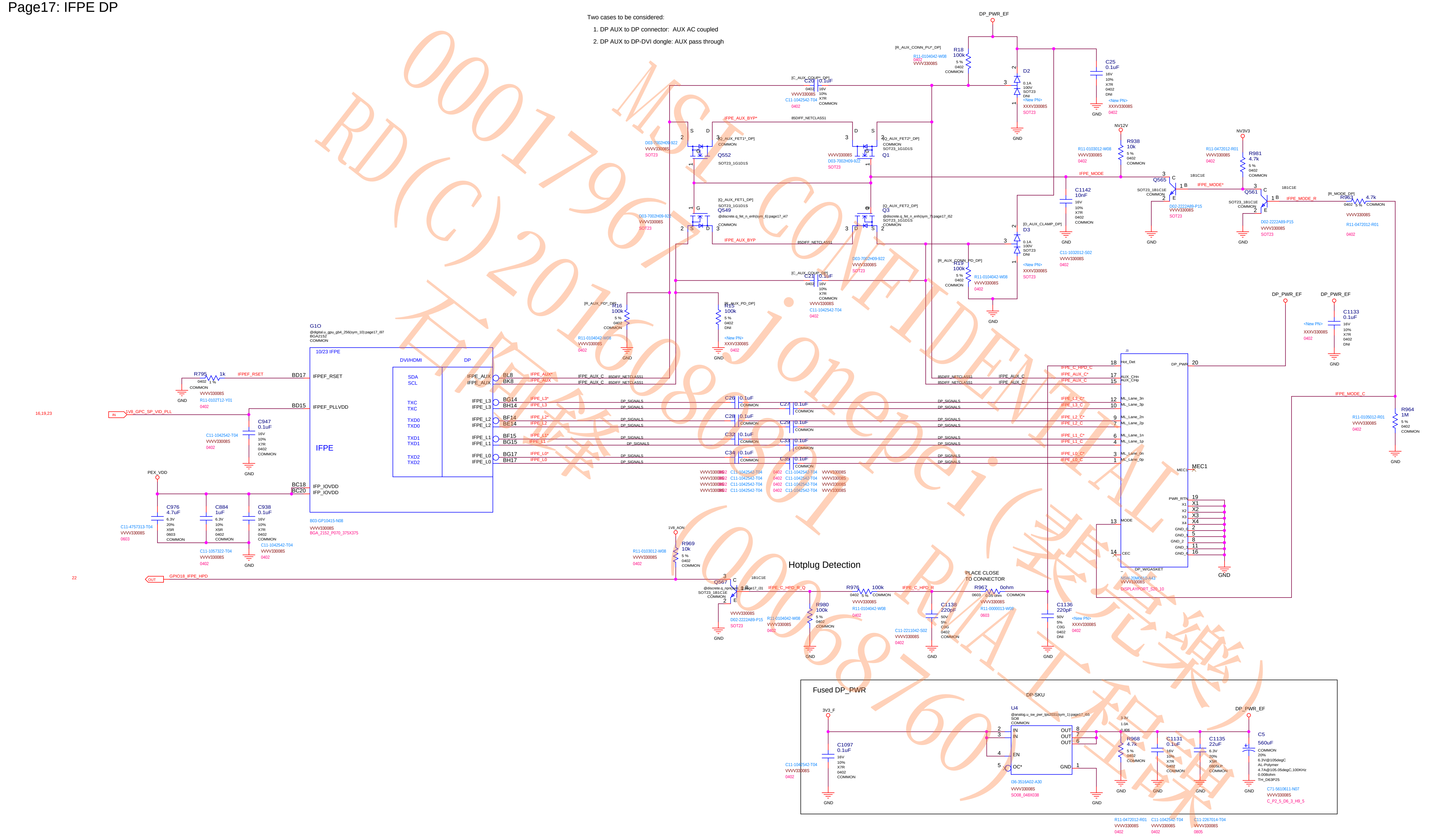
Page17: IFPE DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



DP_PWR_EF
G10
10/23 IFPE
DVI/HDMI
DP
IFPEF_RSET
IFPEF_PLLVDD
IFPE
IFP_IOVDD
SDA
SCL
TXC
TXD0
TXD1
TXD2
IFPE_AUX
IFPE_L3
IFPE_L2
IFPE_L1
IFPE_L0
R795 1k
C947 0.1uF
C976 4.7uF
C884 1uF
C938 0.1uF
PEX_VDD
1V8_GPC_SP_VID_PLL
Q552
Q549
Q1
Q3
R18 100k
R19 100k
R15 100k
R16 100k
C20 0.1uF
C21 0.1uF
C25 0.1uF
D2
D3
R938 10k
R981 4.7k
Q565
Q561
C1142 10nF
R963 4.7k
IFPE_MODE
IFPE_MODE_R
NV12V
NV3V3
C26 0.1uF
C27 0.1uF
C28 0.1uF
C29 0.1uF
C32 0.1uF
C33 0.1uF
C34 0.1uF
C35 0.1uF
MEC1
Hot_Det
AUX_CHn
AUX_CHp
ML_Lane_3n
ML_Lane_3p
ML_Lane_2n
ML_Lane_2p
ML_Lane_1n
ML_Lane_1p
ML_Lane_0n
ML_Lane_0p
MODE
CEC
DP_PWR
DISPLAYPORT_S20_10
C1133 0.1uF
R964 1M
IFPE_MODE_C
Hotplug Detection
1V8_AON
R969 10k
GPIO18_IFPE_HPD
Q567
R976 100k
R980 100k
IFPE_C_HPD_R_Q
IFPE_C_HPD_R
PLACE CLOSE TO CONNECTOR
R967 0ohm
C1138 220pF
C1136 220pF
Fused DP_PWR
DP-SKU
3V3_F
U4
C1097 0.1uF
R968 4.7k
C1131 0.1uF
C1135 22uF
C5 560uF
GND

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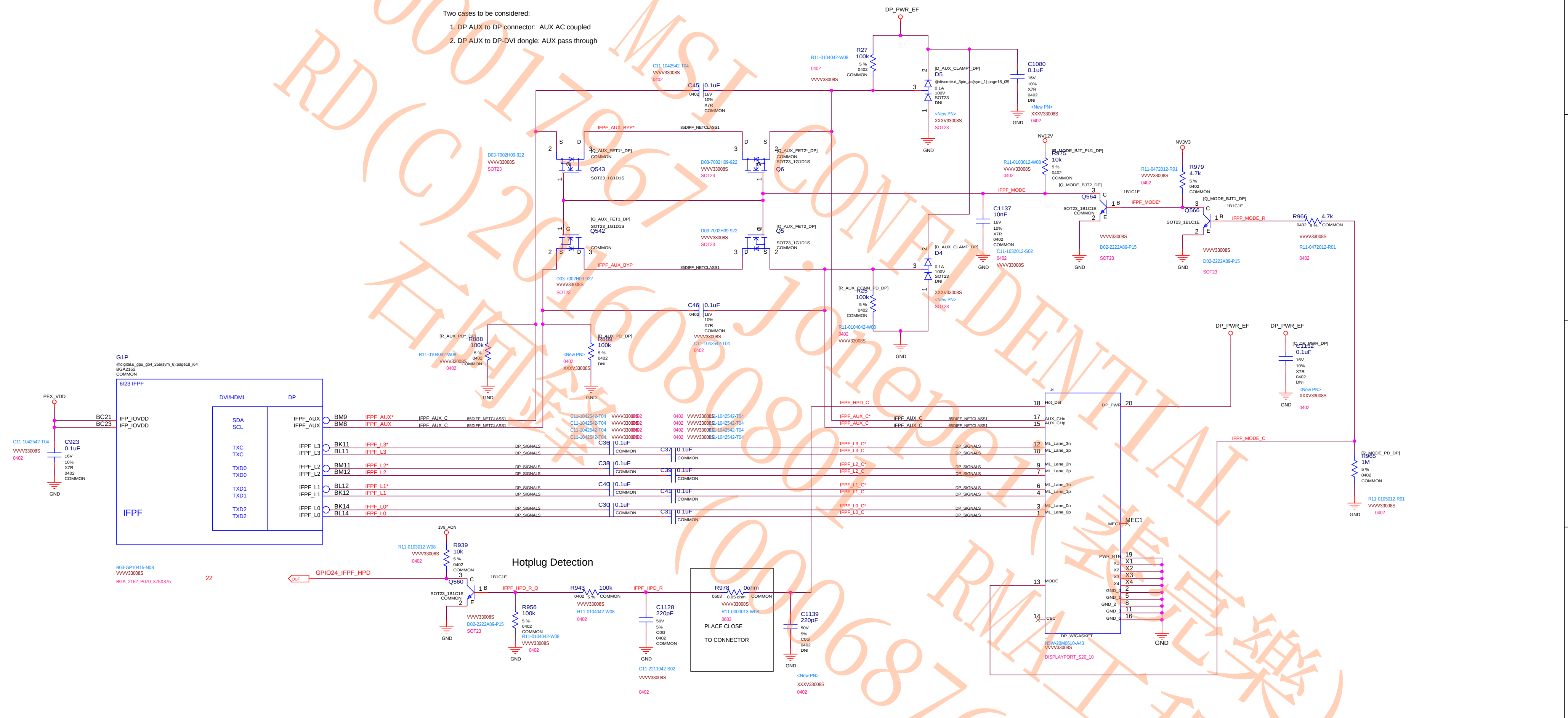
Page18: IFPF DP



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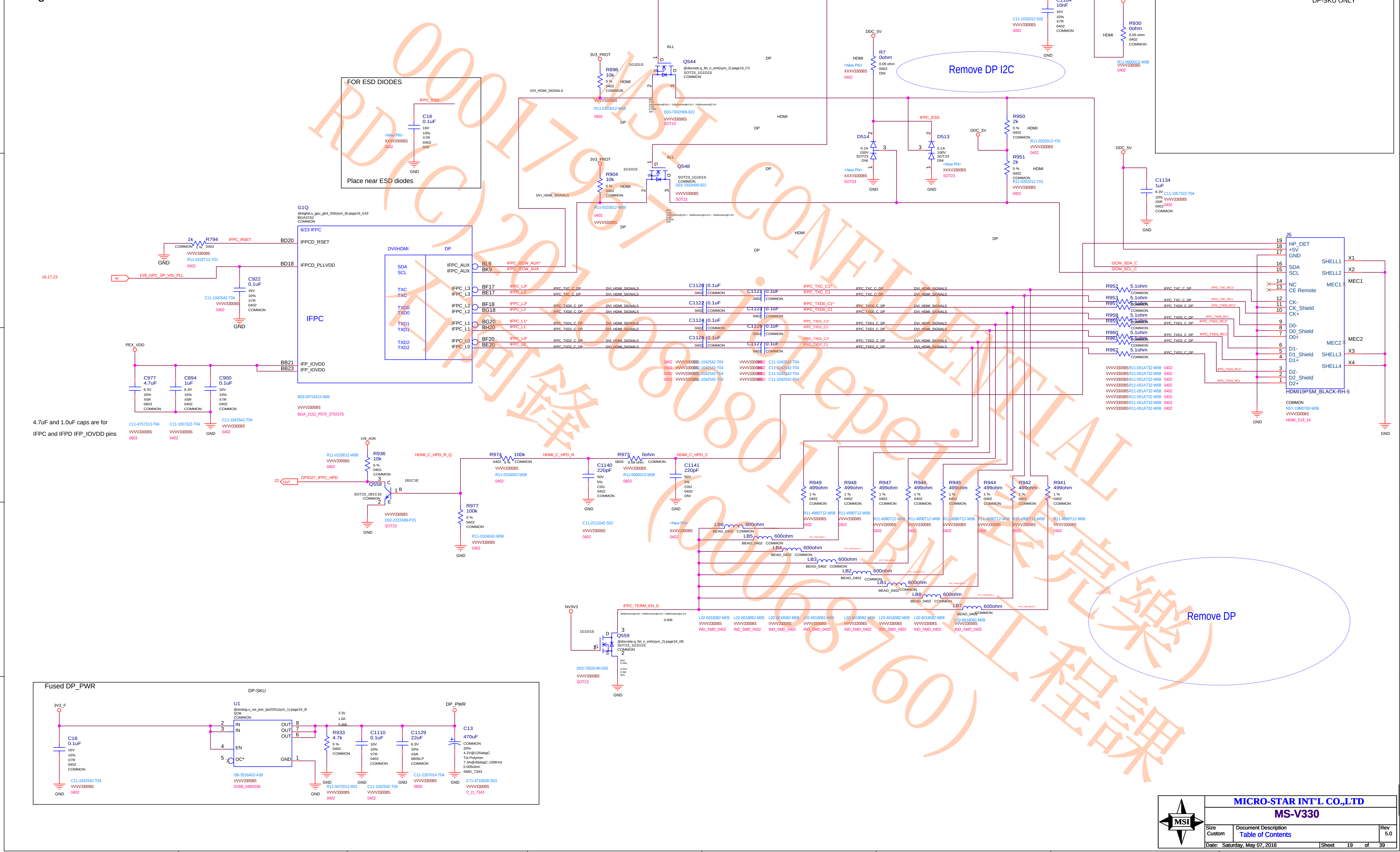
Page19: IFPC HDMI 2.0/DP



* I2C to DDC level switching
IFPC_MODE_Q*
DP-SKU ONLY
Remove DP I2C
FOR ESD DIODES
Place near ESD diodes
IFPC_ESD
C16 0.1uF
3V3_PROT
R898 10k
Q544
Q548
R904 10k
DDC_5V
R7 0ohm
D514
D513
R950 2k
R951 2k
C1104 10nF
R930 0ohm
C1134 1uF
G1Q
8/23 IFPC
IFPCD_RSET
IFPCD_PLLVDD
IFPC
IFP_IOVDD
DVI/HDMI
DP
SDA
SCL
TXC
TXD0
TXD1
TXD2
IFPC_AUX
IFPC_L3
IFPC_L2
IFPC_L1
IFPC_L0
IFPC_I2CW_AUX*
IFPC_I2CW_AUX
R794 1k
IFPC_RSET
1V8_GPC_SP_VID_PLL
C922 0.1uF
PEX_VDD
C977 4.7uF
C894 1uF
C900 0.1uF
4.7uF and 1.0uF caps are for
IFPC and IFPD IFP_IOVDD pins
C1120 0.1uF
C1121 0.1uF
C1122 0.1uF
C1123 0.1uF
C1124 0.1uF
C1125 0.1uF
C1126 0.1uF
C1127 0.1uF
DVI_HDMI_SIGNALS
J5
HP_DET
+5V
GND
SDA
SCL
NC
CE Remote
CK-
CK_Shield
CK+
D0-
D0_Shield
D0+
D1-
D1_Shield
D1+
D2-
D2_Shield
D2+
SHELL1
SHELL2
SHELL3
SHELL4
MEC1
MEC2
HDMI19PSM_BLACK-RH-5
I2CW_SDA_C
I2CW_SCL_C
R952 5.1ohm
R953 5.1ohm
R957 5.1ohm
R958 5.1ohm
R959 5.1ohm
R960 5.1ohm
R961 5.1ohm
R962 5.1ohm
1V8_AON
R936 10k
GPIO27_IFPC_HPD
Q558
HDMI_C_HPD_R_Q
R974 100k
HDMI_C_HPD_R
R973 0ohm
HDMI_C_HPD_C
C1140 220pF
C1141 220pF
R977 100k
R949 499ohm
R948 499ohm
R947 499ohm
R946 499ohm
R945 499ohm
R944 499ohm
R942 499ohm
R941 499ohm
LB6 600ohm
LB5 600ohm
LB4 600ohm
LB3 600ohm
LB2 600ohm
LB1 600ohm
LB8 600ohm
LB7 600ohm
NV3V3
IFPC_TERM_EN_D
Q559
Remove DP
Fused DP_PWR
DP-SKU
3V3_F
U1
IN
EN
OC*
OUT
GND
DP_PWR
C18 0.1uF
R933 4.7k
C1110 0.1uF
C1129 22uF
C13 470uF

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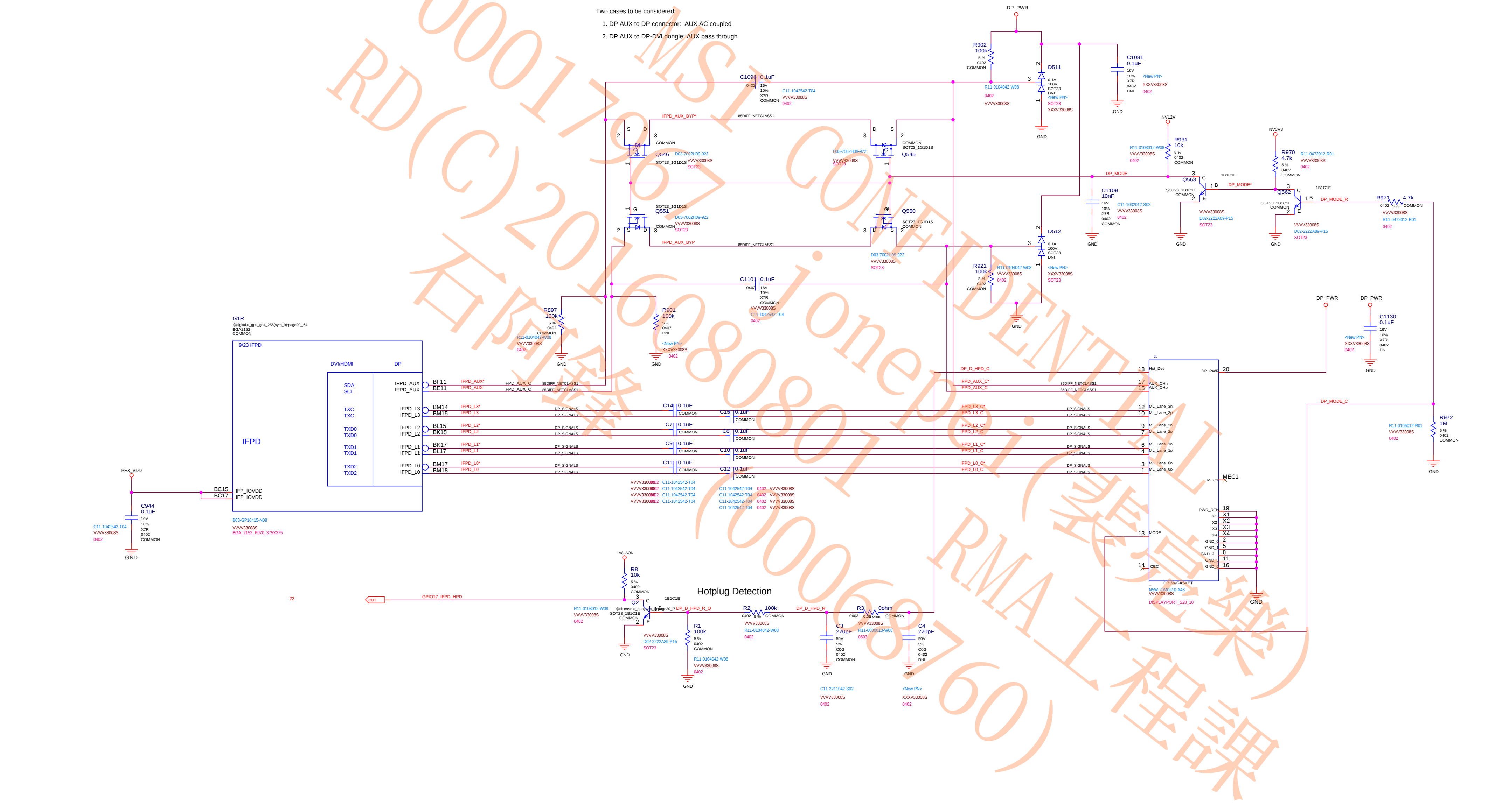
Page20: IFPD DP



Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through
DP_PWR
R902 100k
D511
C1081 0.1uF
C1096 0.1uF
IFPD_AUX_BYP*
Q546
Q545
Q551
Q550
IFPD_AUX_BYP
D512
C1101 0.1uF
R921 100k
NV12V
R931 10k
NV3V3
R970 4.7k
DP_MODE
C1109 10nF
Q563
DP_MODE*
Q562
DP_MODE_R
R971 4.7k
R897 100k
R901 100k
G1R
9/23 IFPD
DVI/HDMI
DP
IFPD
SDA
SCL
TXC
TXD0
TXD1
TXD2
IFPD_AUX
IFPD_L3
IFPD_L2
IFPD_L1
IFPD_L0
IFP_IOVDD
PEX_VDD
C944 0.1uF
C14 0.1uF
C15 0.1uF
C7 0.1uF
C8 0.1uF
C9 0.1uF
C10 0.1uF
C11 0.1uF
C12 0.1uF
DP_D_HPD_C
IFPD_AUX_C*
IFPD_AUX_C
DP_SIGNALS
Hot_Det
AUX_CHn
AUX_CHp
ML_Lane_3n
ML_Lane_3p
ML_Lane_2n
ML_Lane_2p
ML_Lane_1n
ML_Lane_1p
ML_Lane_0n
ML_Lane_0p
DP_PWR
C1130 0.1uF
DP_MODE_C
R972 1M
MEC1
MODE
CEC
DP_W/GASKET
DISPLAYPORT_S20_10
1V8_AON
R8 10k
Q2
GPIO17_IFPD_HPD
Hotplug Detection
DP_D_HPD_R_Q
R1 100k
R2 100k
DP_D_HPD_R
R3 0ohm
C3 220pF
C4 220pF
GND

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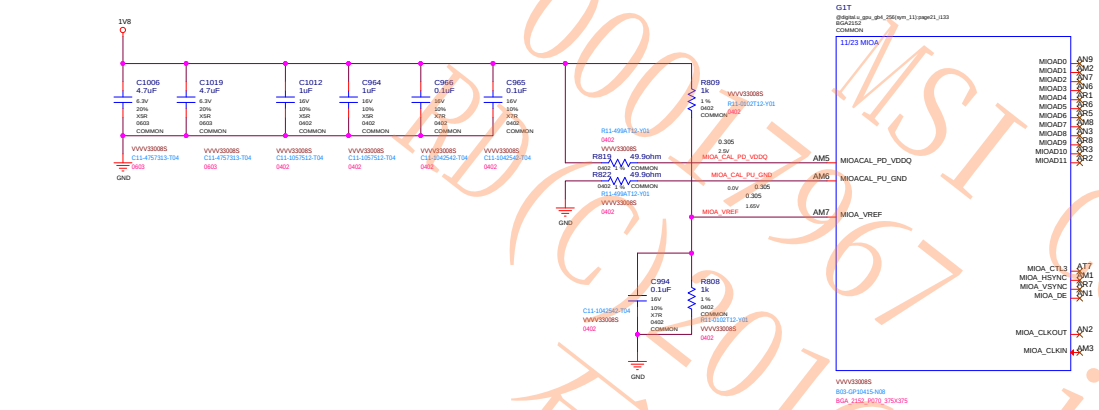
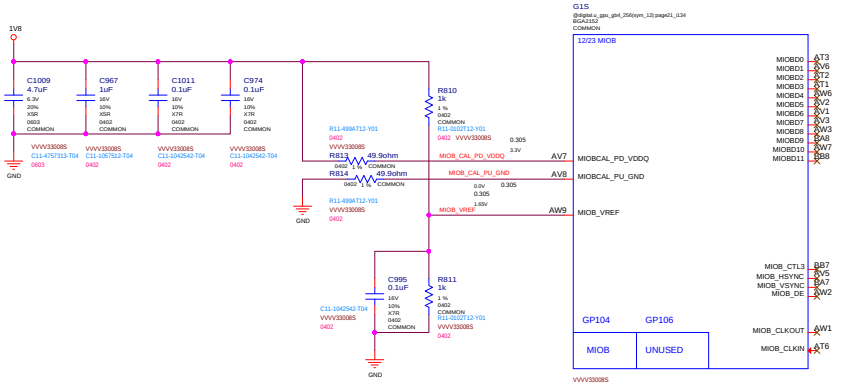
Page21: MIOA/B Interface and FRAME LOCK





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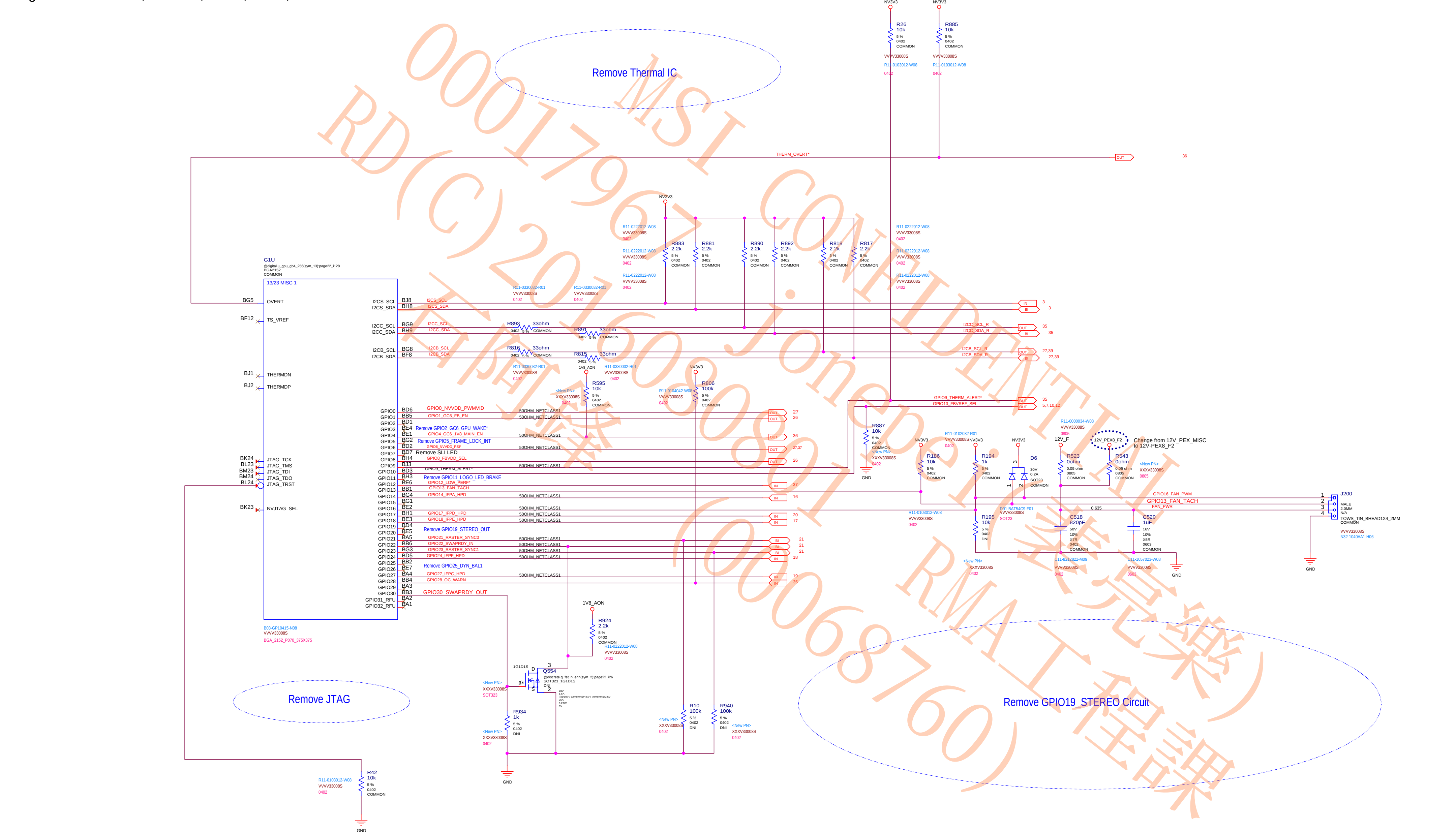
Page22: MISC1: Fan, Thermal, JTAG, GPIO, STEREO



Remove Thermal IC
NV3V3
R26
10k
R885
10k
THERM_OVERT*
G1U
13/23 MISC 1
OVERT
TS_VREF
THERMDN
THERMDP
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST
NVJTAG_SEL
I2CS_SCL
I2CS_SDA
I2CC_SCL
I2CC_SDA
I2CB_SCL
I2CB_SDA
R883 2.2k
R881 2.2k
R890 2.2k
R892 2.2k
R818 2.2k
R817 2.2k
R893 33ohm
R891 33ohm
R816 33ohm
R815 33ohm
R595 10k
R806 100k
GPIO0_NVVDD_PWMVID
GPIO1_GC6_FB_EN
Remove GPIO2_GC6_GPU_WAKE*
GPIO4_GC6_1V8_MAIN_EN
Remove GPIO5_FRAME_LOCK_INT
GPIO6_NVVDD_PS*
Remove SLI LED
GPIO8_FBVDD_SEL
GPIO9_THERM_ALERT*
Remove GPIO11_LOGO_LED_BRAKE
GPIO12_LOW_PERF*
GPIO13_FAN_TACH
GPIO14_IFPA_HPD
GPIO17_IFPD_HPD
GPIO18_IFPE_HPD
Remove GPIO19_STEREO_OUT
GPIO21_RASTER_SYNC0
GPIO22_SWAPRDY_IN
GPIO23_RASTER_SYNC1
GPIO24_IFPF_HPD
Remove GPIO25_DYN_BAL1
GPIO27_IFPC_HPD
GPIO28_OC_WARN
GPIO30_SWAPRDY_OUT
GPIO9_THERM_ALERT*
GPIO10_FBVREF_SEL
R887 10k
R186 10k
R194 1k
D6
R523 0ohm
R543 0ohm
12V_F
12V_PEX8_F2
Change from 12V_PEX_MISC to 12V-PEX8_F2
GPIO16_FAN_PWM
GPIO13_FAN_TACH
FAN_PWR
J200
TOWS_TIN_BHEAD1X4_2MM
R195 10k
C518 820pF
C520 1uF
1V8_AON
R924 2.2k
Q554
R934 1k
R10 100k
R940 100k
Remove JTAG
Remove GPIO19_STEREO Circuit
R42 10k
GND

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Page23: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	
L	H	L	00010	
L	H	H	00011	
H	H	L	00110	
H	H	H	00111	
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

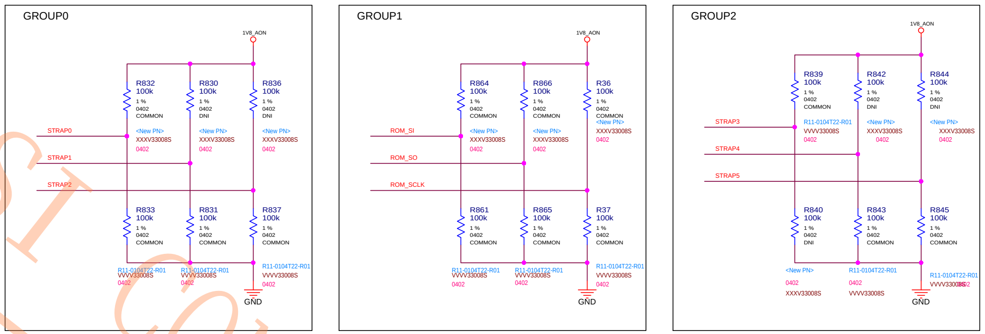
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

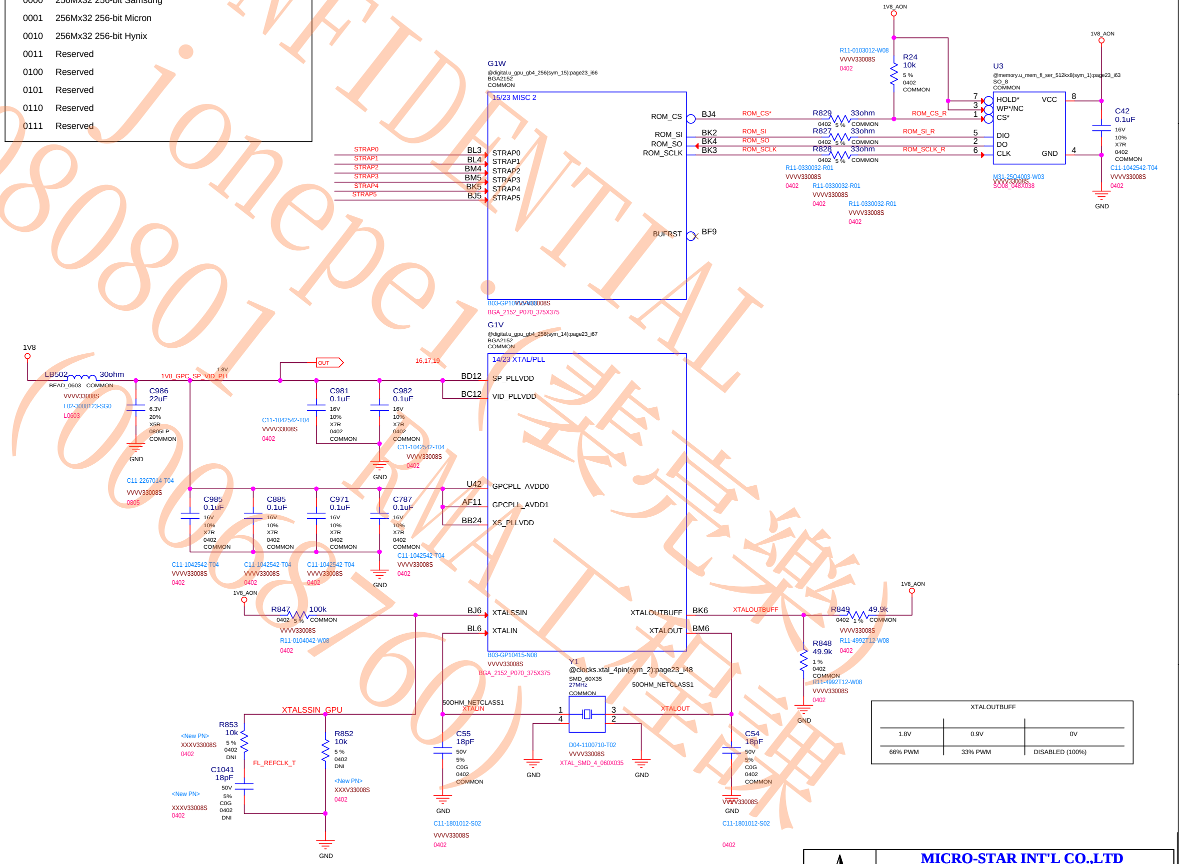
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



CFG[3:0]	Config Width	Vendor
0000	256Mx32 256-bit	Samsung
0001	256Mx32 256-bit	Micron
0010	256Mx32 256-bit	Hynix
0011	Reserved	
0100	Reserved	
0101	Reserved	
0110	Reserved	
0111	Reserved	



XTALOUTBUFF		
1.8V	0.9V	0V
66% PWM	33% PWM	DISABLED (100%)

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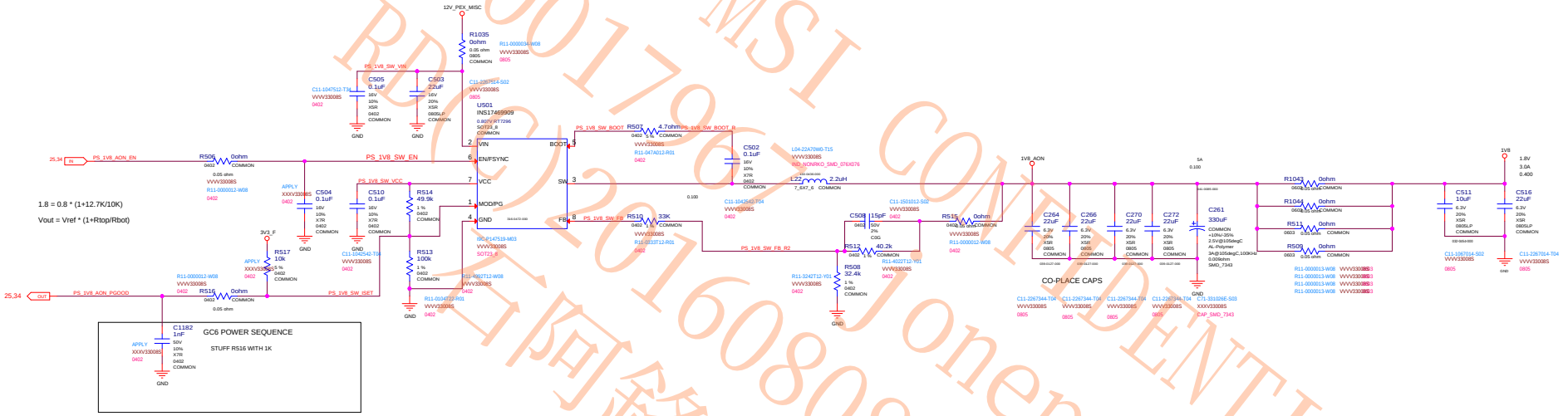

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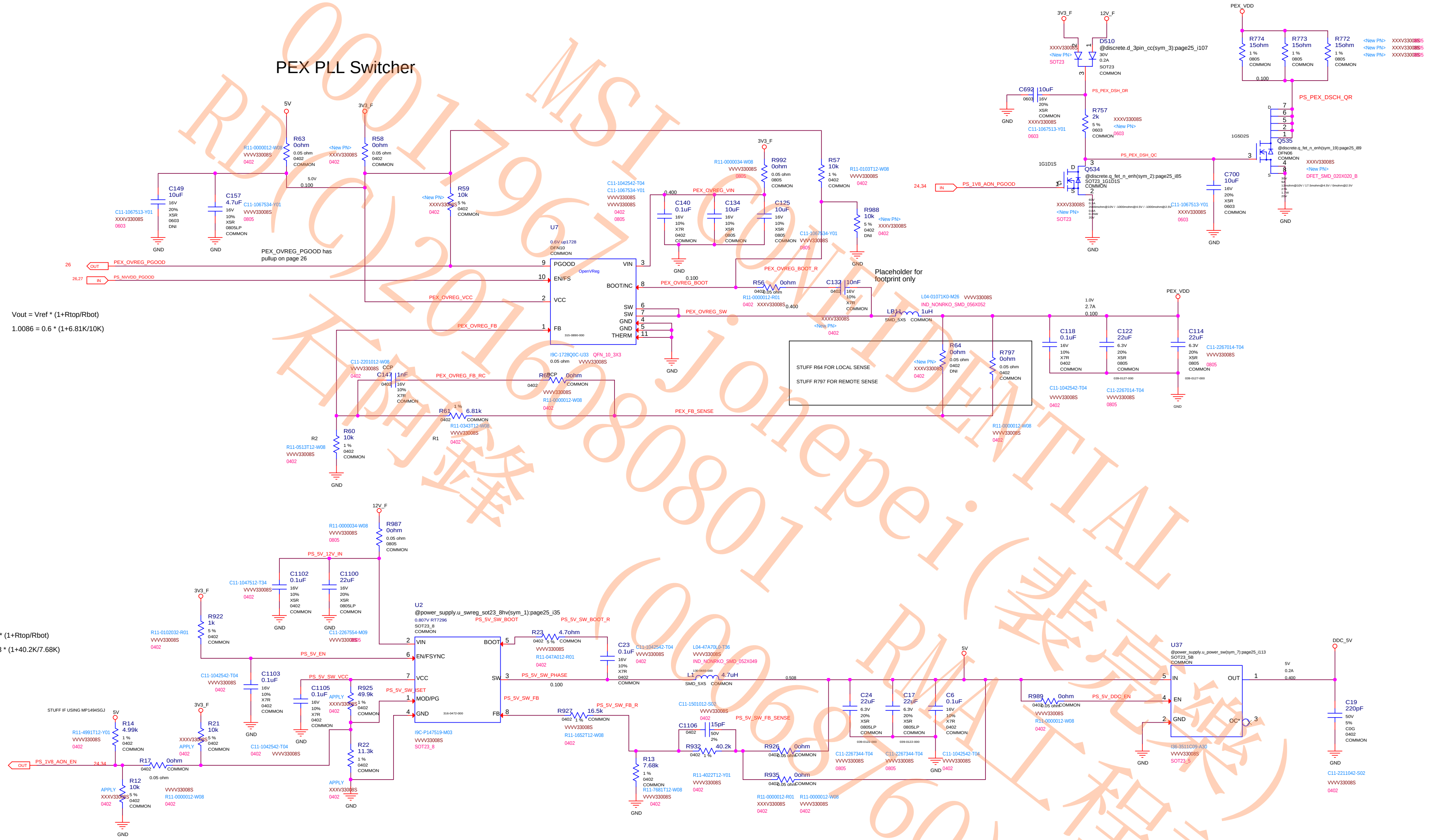
Page25: PS: 5V, PEX_VDD



PEX PLL Switcher
5V
3V3_F
12V_F
PEX_VDD
U7
PGOOD
EN/FS
VCC
FB
VIN
BOOT/NC
SW
GND
THERM
PEX_OVREG_PGOOD
PS_NVVDD_PGOOD
PEX_OVREG_VCC
PEX_OVREG_FB
PEX_OVREG_FB_RC
PEX_OVREG_VIN
PEX_OVREG_BOOT
PEX_OVREG_BOOT_R
PEX_OVREG_SW
PEX_FB_SENSE
PEX_OVREG_PGOOD has pullup on page 26
Vout = Vref * (1+Rtop/Rbot)
1.0086 = 0.6 * (1+6.81K/10K)
Placeholder for footprint only
STUFF R64 FOR LOCAL SENSE
STUFF R797 FOR REMOTE SENSE
PS_PEX_DSCH_QR
PS_PEX_DSH_QC
PS_1V8_AON_PGOOD
Q534
Q535
D510
U2
@power_supply.u_sweg_sot23_8hv(sym_1):page25_i35
VIN
EN/FSYNC
VCC
MOD/PG
GND
BOOT
SW
FB
PS_5V_12V_IN
PS_5V_EN
PS_5V_SW_VCC
PS_5V_SW_SET
PS_5V_SW_BOOT
PS_5V_SW_BOOT_R
PS_5V_SW_PHASE
PS_5V_SW_FB
PS_5V_SW_FB_R
PS_5V_SW_FB_SENSE
PS_5V_DDC_EN
PS_1V8_AON_EN
Vout = Vref * (1+Rtop/Rbot)
4.9875 = 0.8 * (1+40.2K/7.68K)
STUFF IF USING MP1494SGJ
U37
@power_supply.u_power_sw(sym_7):page25_i113
IN
OUT
EN
GND
OC*
DDC_5V
GND

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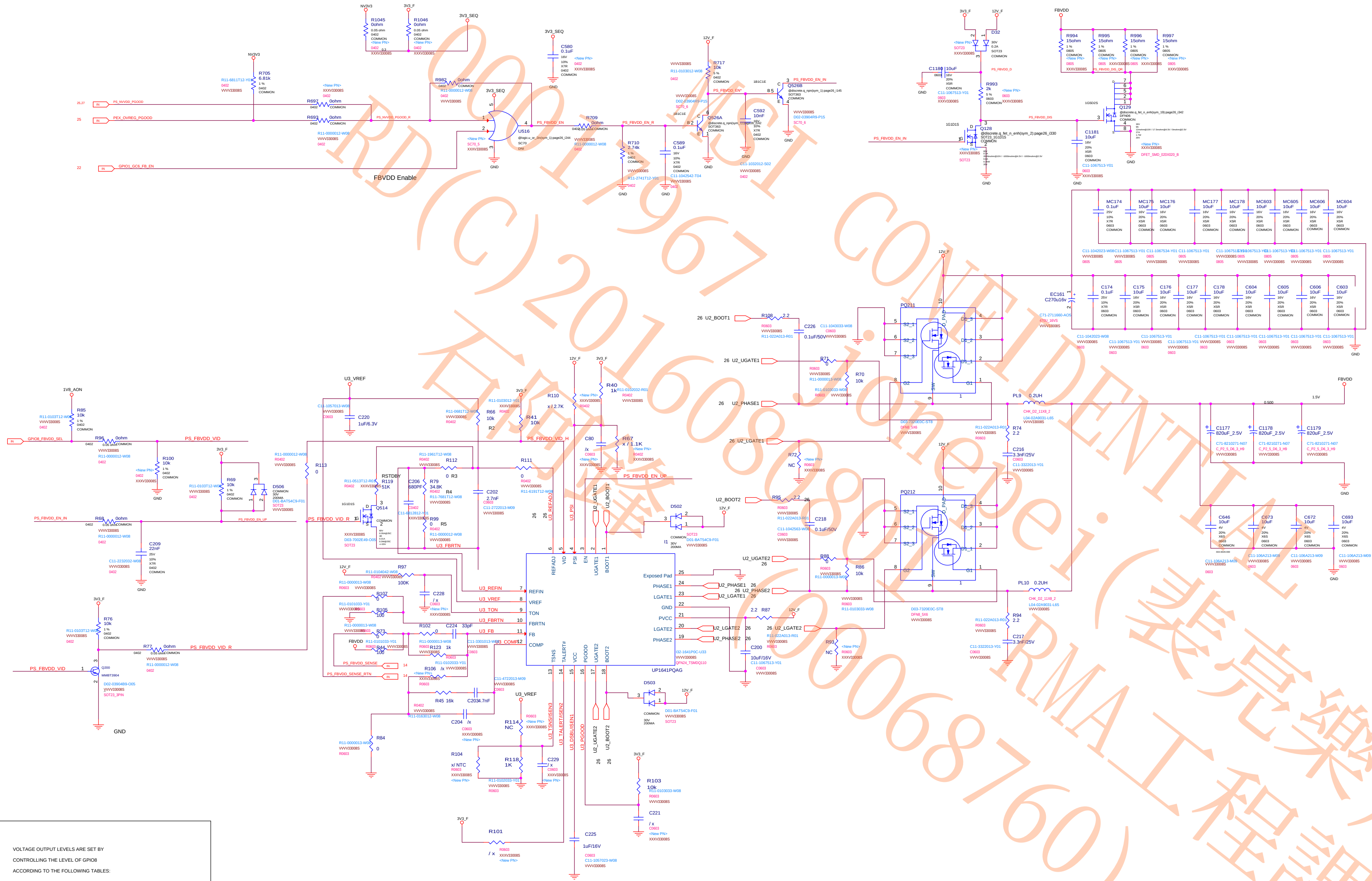
Page26: PS: FBVDD



VOLTAGE OUTPUT LEVELS ARE SET BY
CONTROLLING THE LEVEL OF GPIO8
ACCORDING TO THE FOLLOWING TABLES:

SAMSUNG K4G1325FC-HC28

GPIO8 LEVEL	FBVDD OUTPUT VOLTAGE
0	1.35V
1	1.55V

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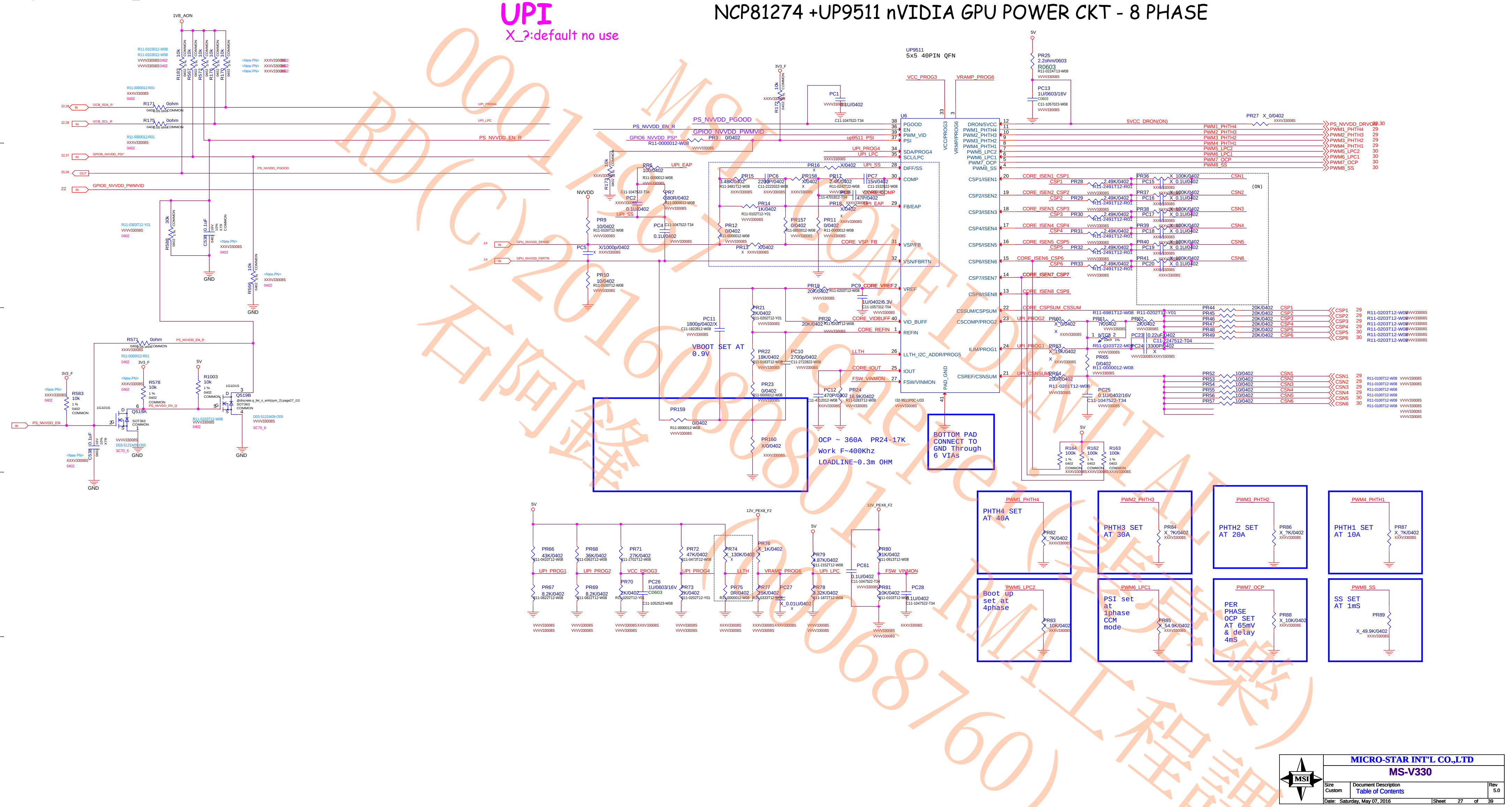
Page27: PS: NVVDD_OVR8

NCP81274 +UP9511 nVIDIA GPU POWER CKT - 8 PHASE

UPI
X_?:default no use



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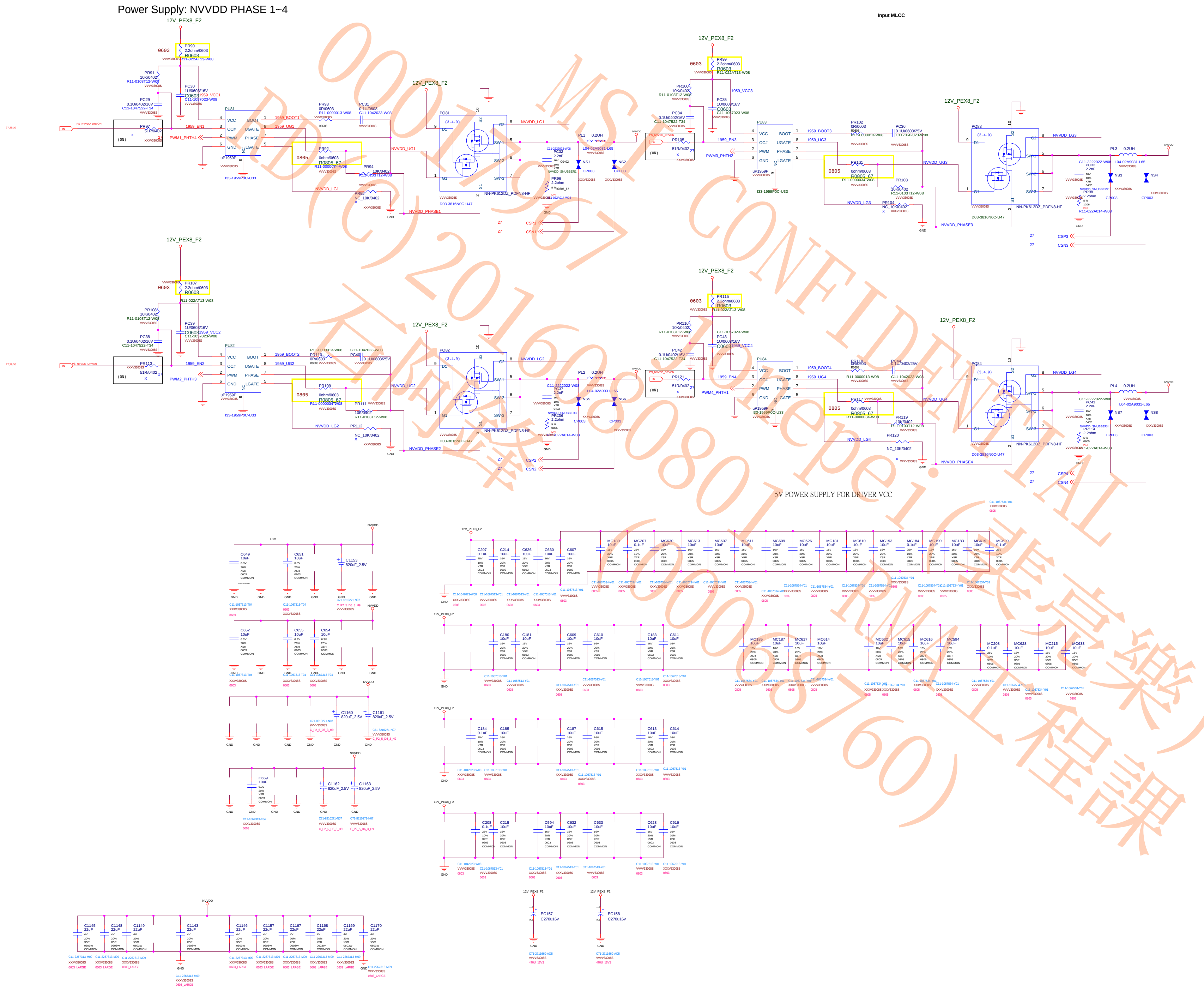
Page29: PS: NVVDD Phase 1-4



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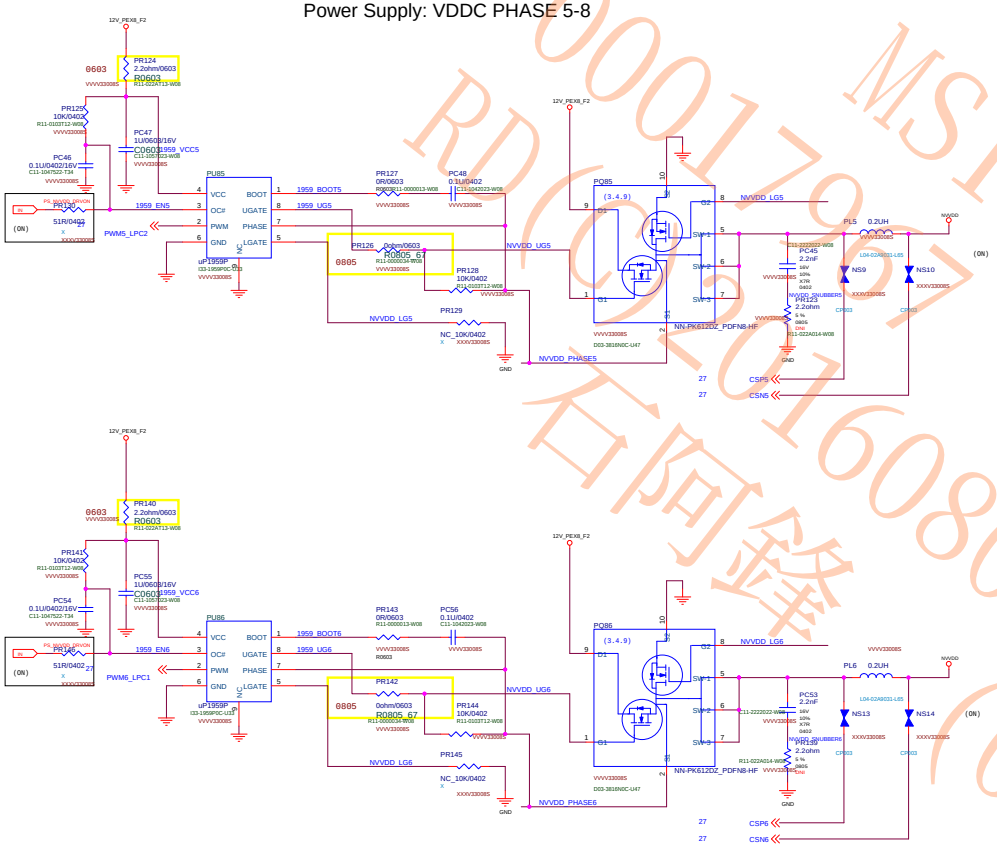
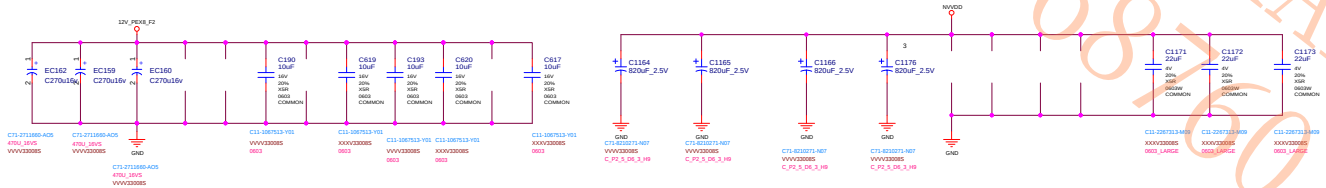
Page30: PS: NVVDD Phase 5 ~8

Power Supply: VDDC PHASE 5-8





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Page32: PS: Dynamic Power Balance Phases

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Page33: PS: Dynamic Power Balance Logic

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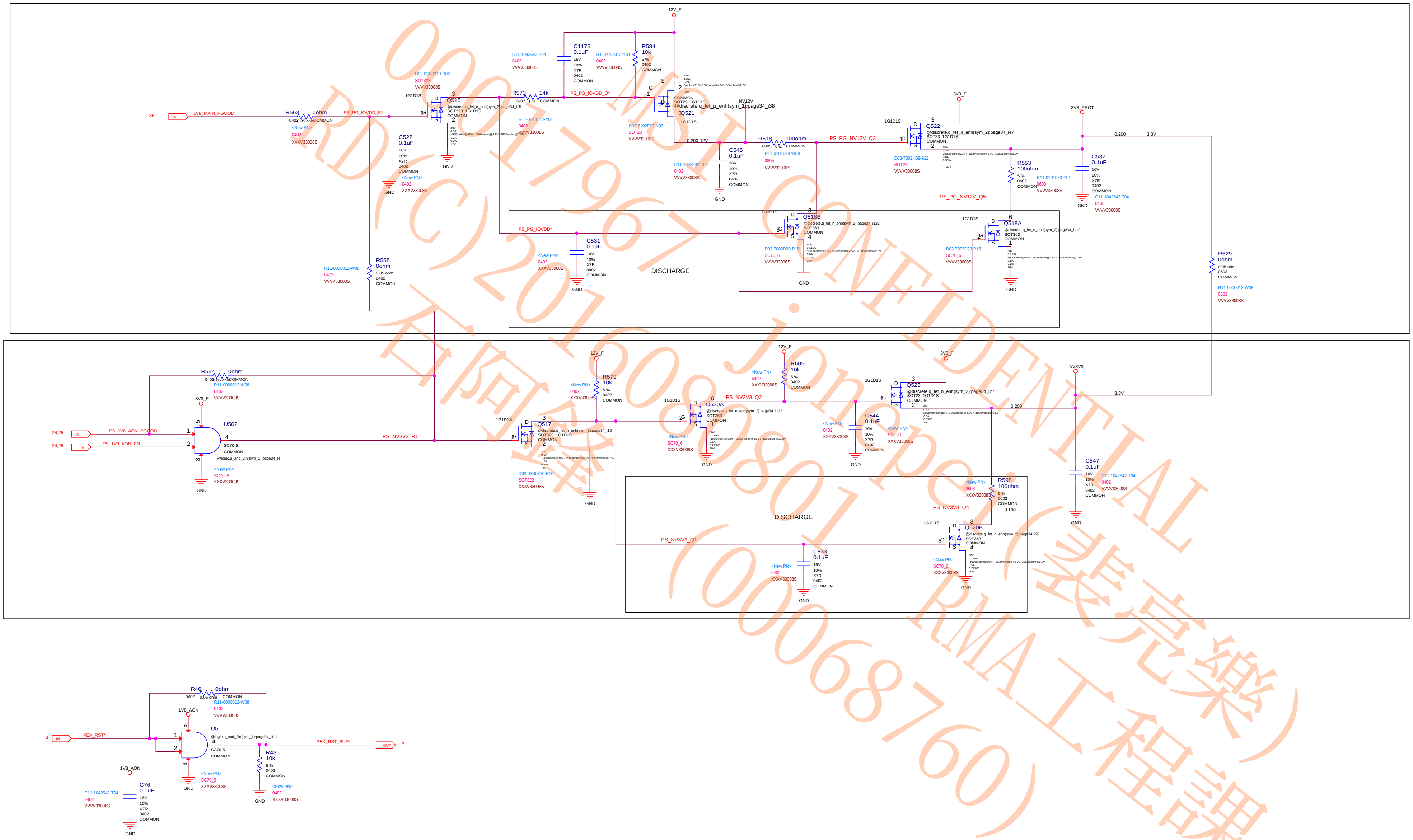
Page34:PS: NV3V3, NV12V



12V_F
1V8_MAIN_PGOOD
PS_PG_IOVDD_R2
PS_PG_IOVDD_Q*
PS_PG_IOVDD*
PS_PG_NV12V_Q3
PS_PG_NV12V_Q5
NV12V
3V3_F
3V3_PROT
DISCHARGE
Q515
Q521
Q522
Q518B
Q518A
R563 0ohm
R573 14k
R584 10k
R618 100ohm
R553 100ohm
R555 0ohm
R629 0ohm
C1175 0.1uF
C522 0.1uF
C545 0.1uF
C532 0.1uF
C531 0.1uF
GND
PS_1V8_AON_PGOOD
PS_1V8_AON_EN
PS_NV3V3_R1
PS_NV3V3_Q2
PS_NV3V3_Q4
PS_NV3V3_Q1
NV3V3
U502
Q517
Q520A
Q523
Q520B
R554 0ohm
R579 10k
R605 10k
R598 100ohm
C544 0.1uF
C547 0.1uF
C533 0.1uF
PEX_RST*
PEX_RST_BUF*
1V8_AON
U5
R46 0ohm
R43 10k
C76 0.1uF

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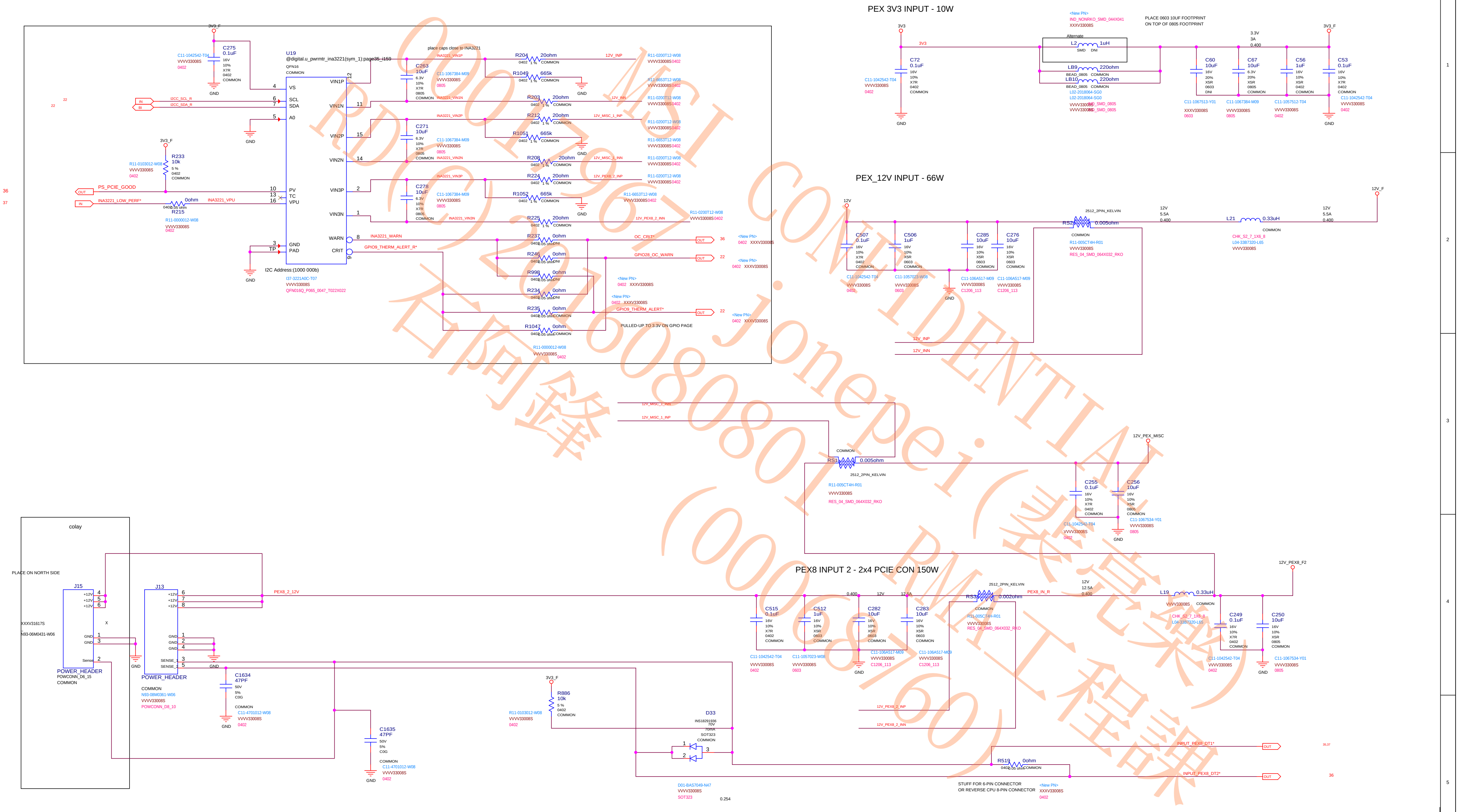
Page35: PS: Inputs, Filtering, and Monitoring



PEX 3V3 INPUT - 10W
PEX_12V INPUT - 66W
PEX8 INPUT 2 - 2x4 PCIE CON 150W
U19
@digital.u_pwrmtr_ina3221(sym_1):page35_i159
QFN16
place caps close to INA3221
I2C Address:(1000 000b)
PULLED-UP TO 3.3V ON GPIO PAGE
PLACE 0603 10UF FOOTPRINT ON TOP OF 0805 FOOTPRINT
PLACE ON NORTH SIDE
J15
POWER_HEADER
J13
POWER_HEADER
D33
STUFF FOR 6-PIN CONNECTOR OR REVERSE CPU 8-PIN CONNECTOR
PS_PCIE_GOOD
INA3221_LOW_PERF*
OC_CRIT*
GPIO28_OC_WARN
GPIO9_THERM_ALERT*
INPUT_PEX8_DT1*
INPUT_PEX8_DT2*
12V_PEX_MISC
12V_PEX8_F2

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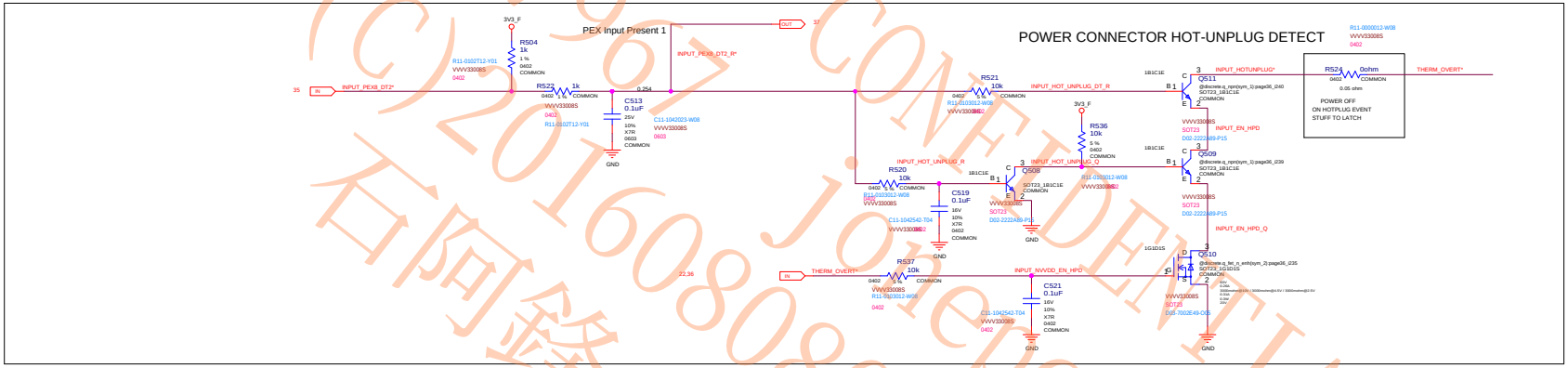

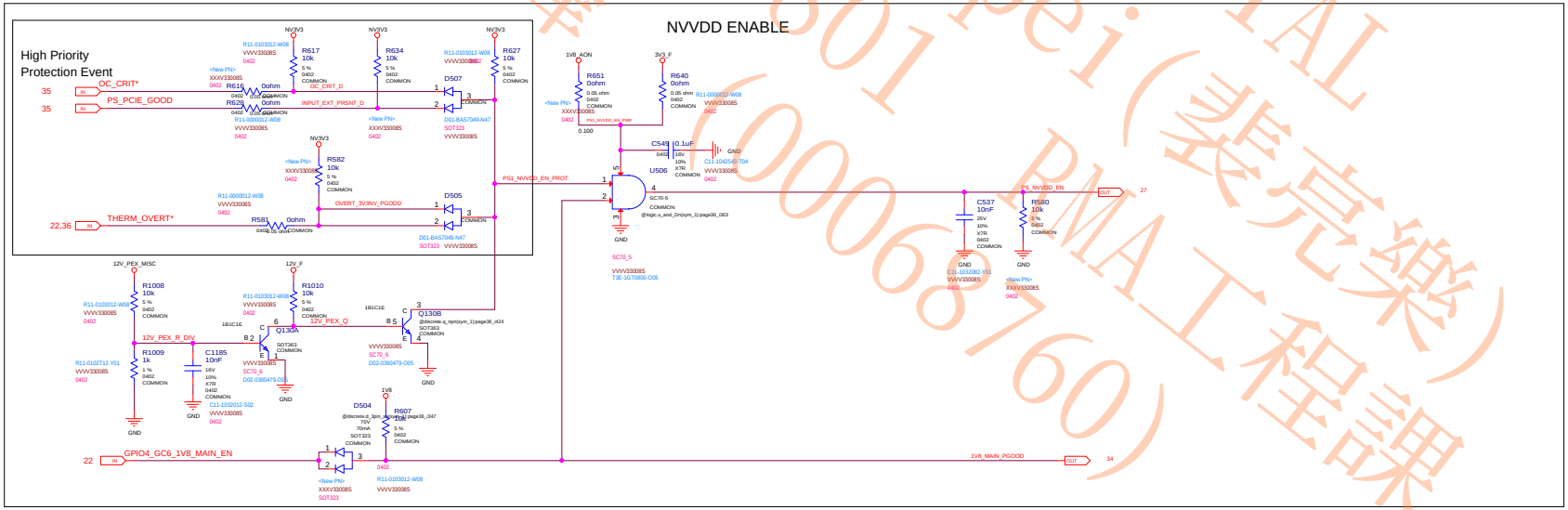

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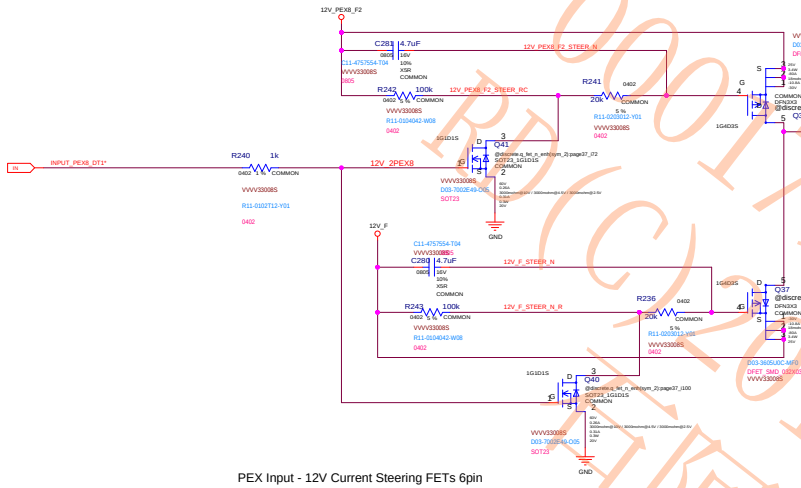
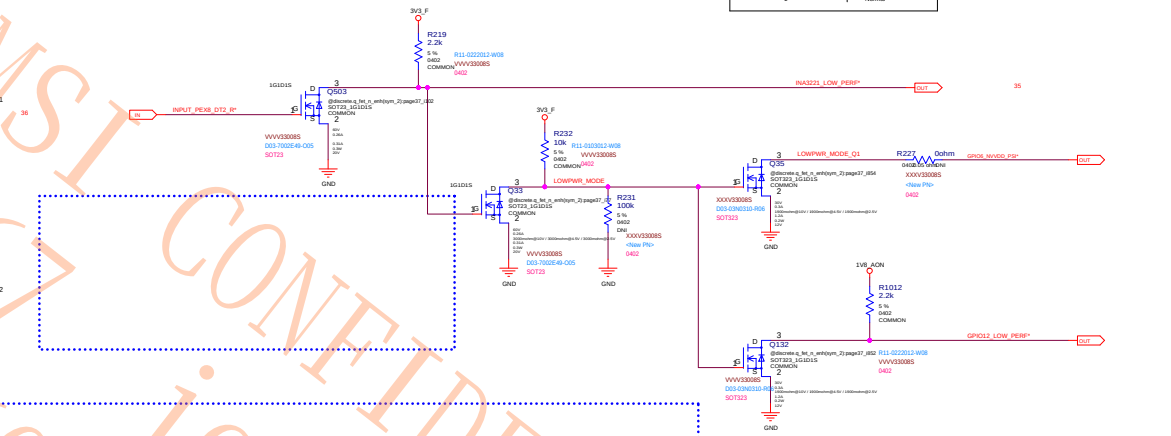
Page37: PS: 12V Current Steering, PSI Control, and LED

PEX Input - 12V Current Steering FETs 8pin



PEX Input - 12V Current Steering FETs 6pin

PEX Input - Power Level/PSI* Control



GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

Remove POWER BRAKE

POWER BRAKE

REMOVE SLI LED (GEFORCE ONLY)

GeForce Logo LED

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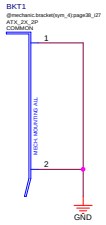
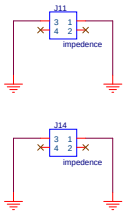
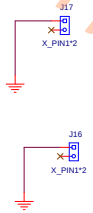
Page38: Mechanical: Bracket/Thermal Solution

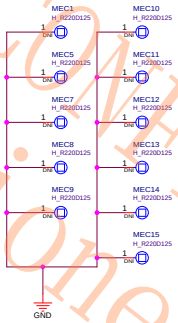
Brackets:



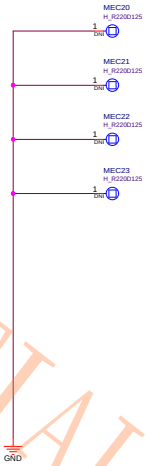


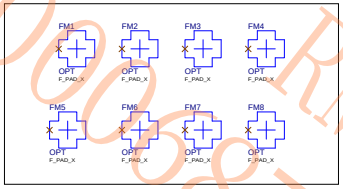


Mechanical Holes Symbol



GPU Stiffner





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