

PG411 A01

GP104 - 8GB GDDR5, 256b, 256Mx32

Tall DVI-D + DP + DP + DP/HDMI + DP

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A

B

C

D

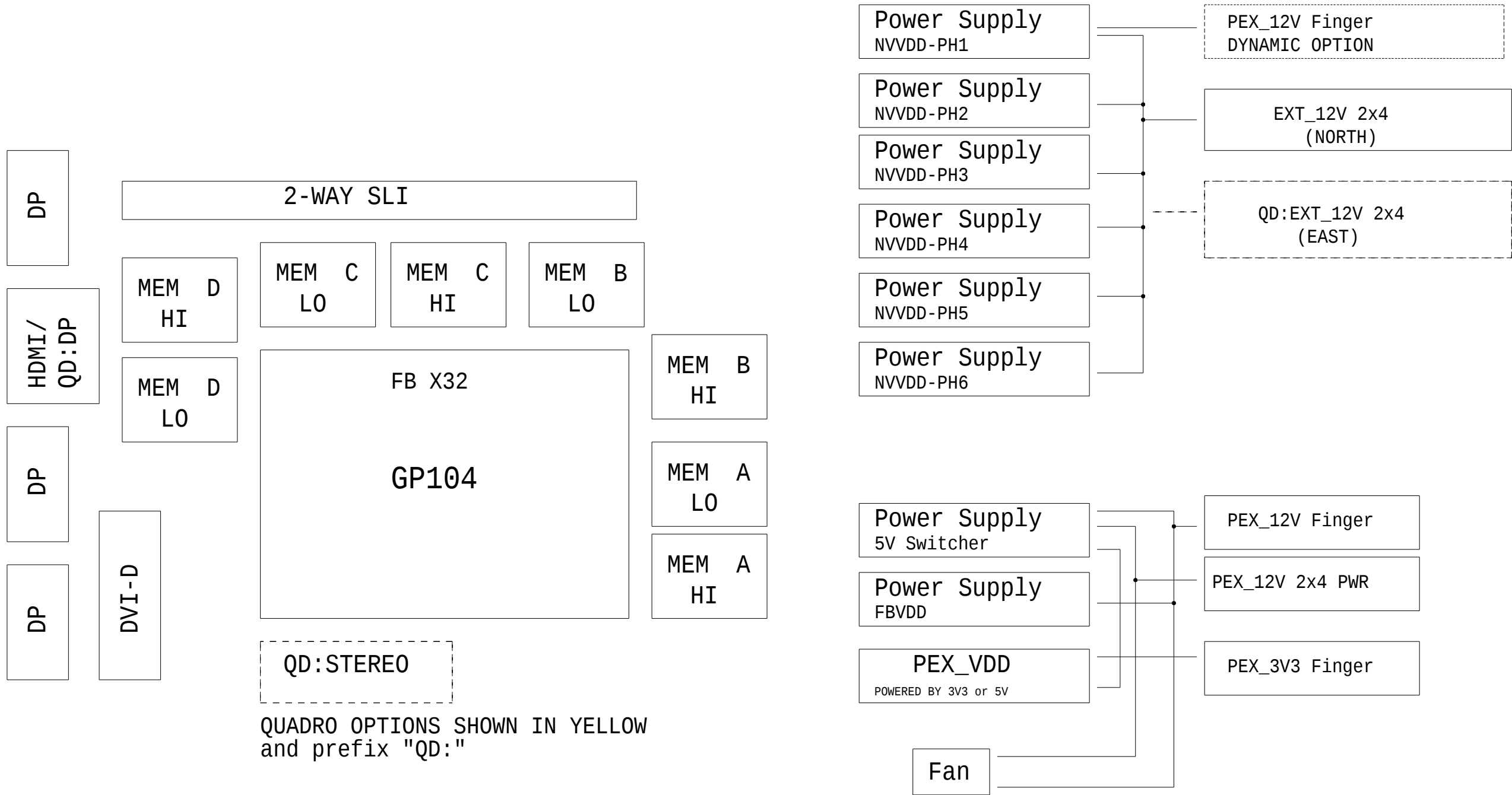
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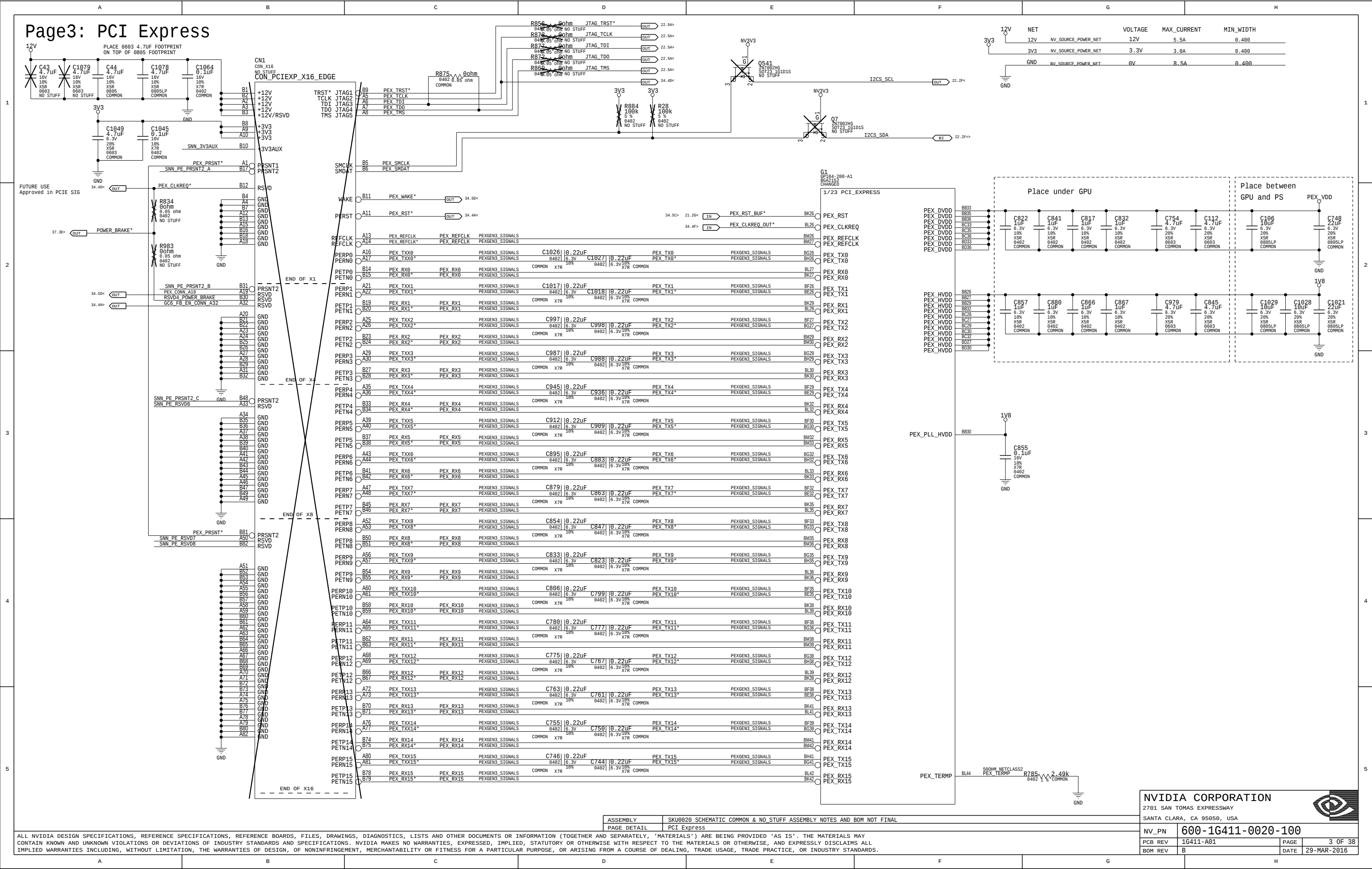
Page2: Block Diagram



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Page3: PCI Express



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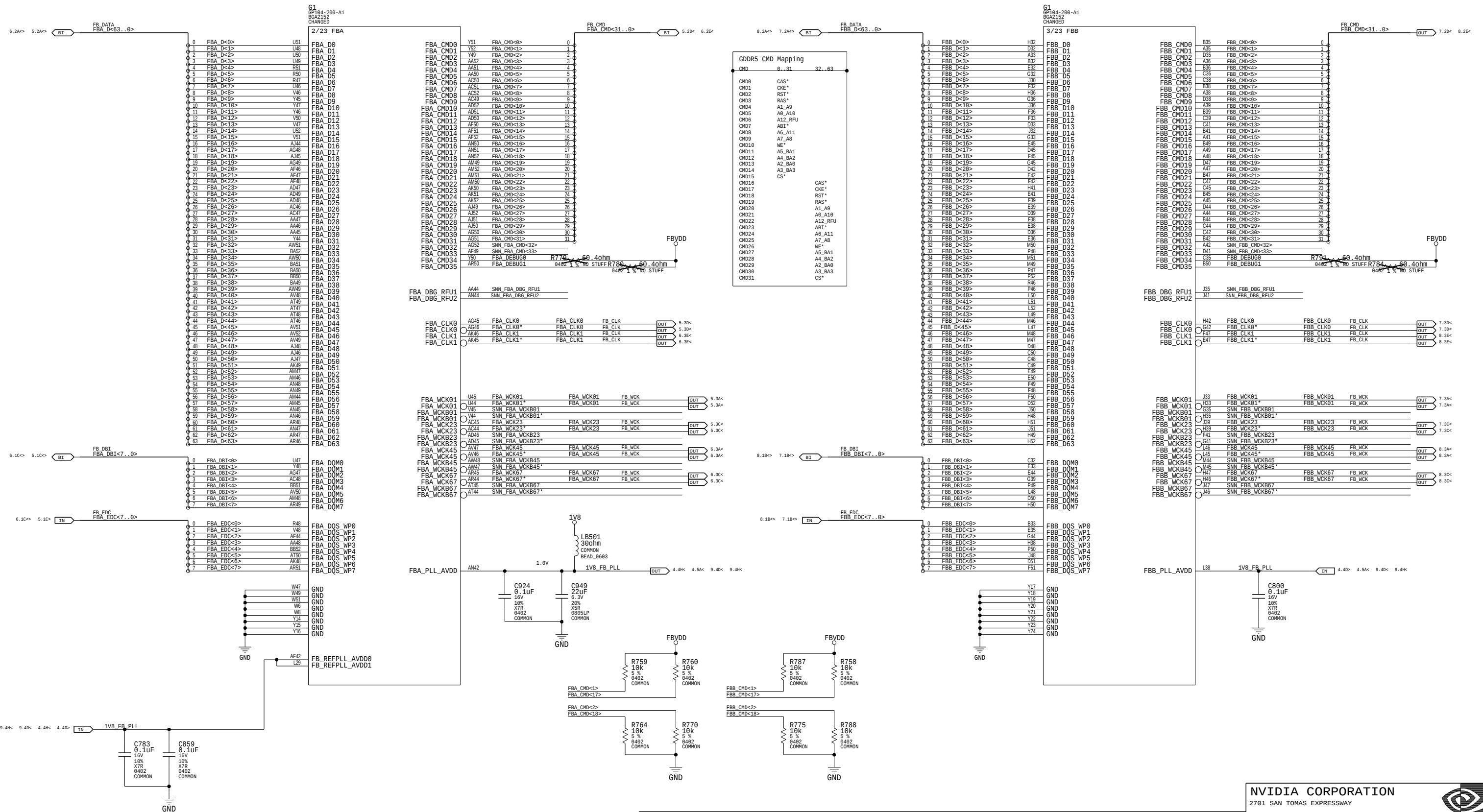
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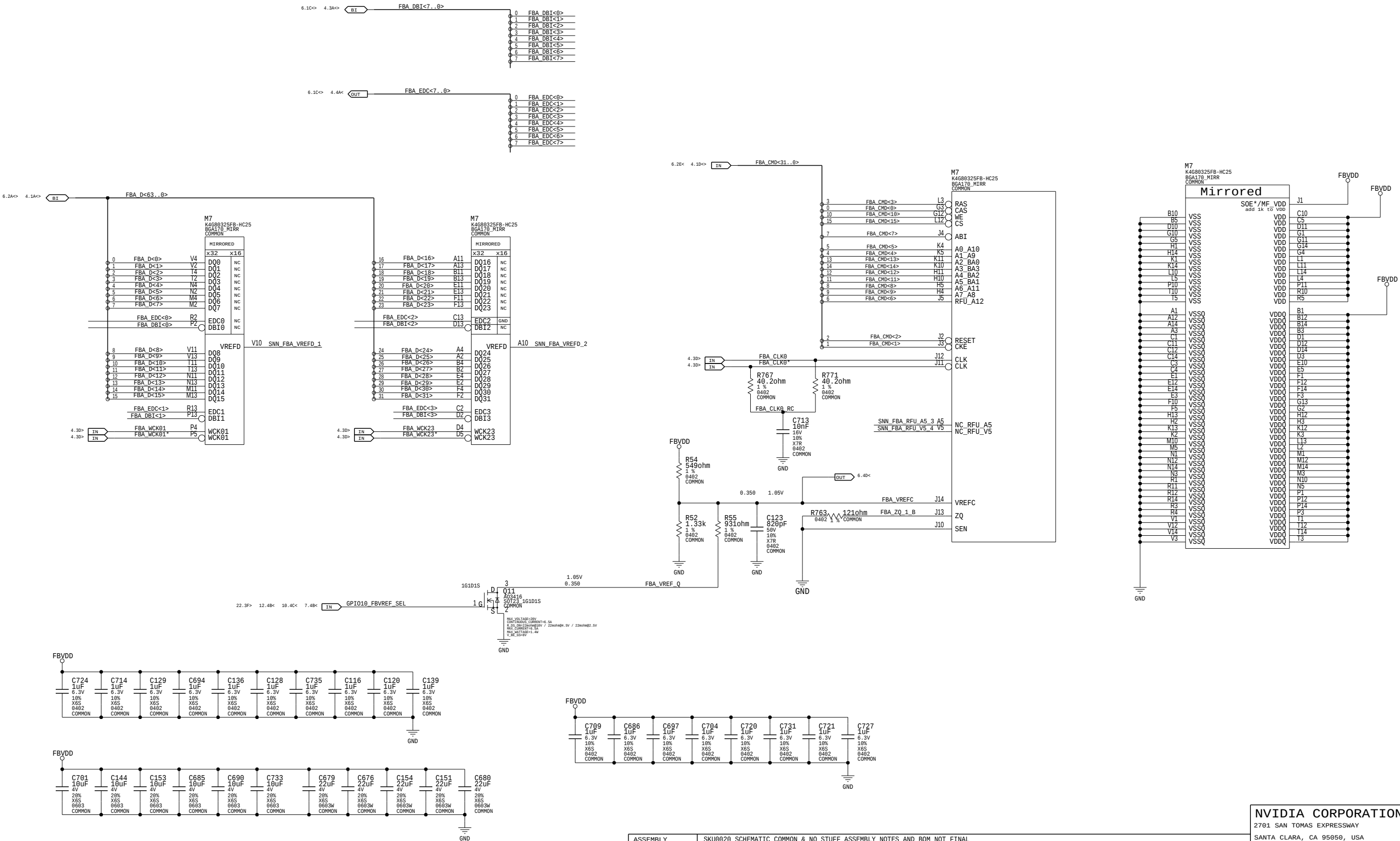
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Page4: MEMORY: GPU Partition A/B





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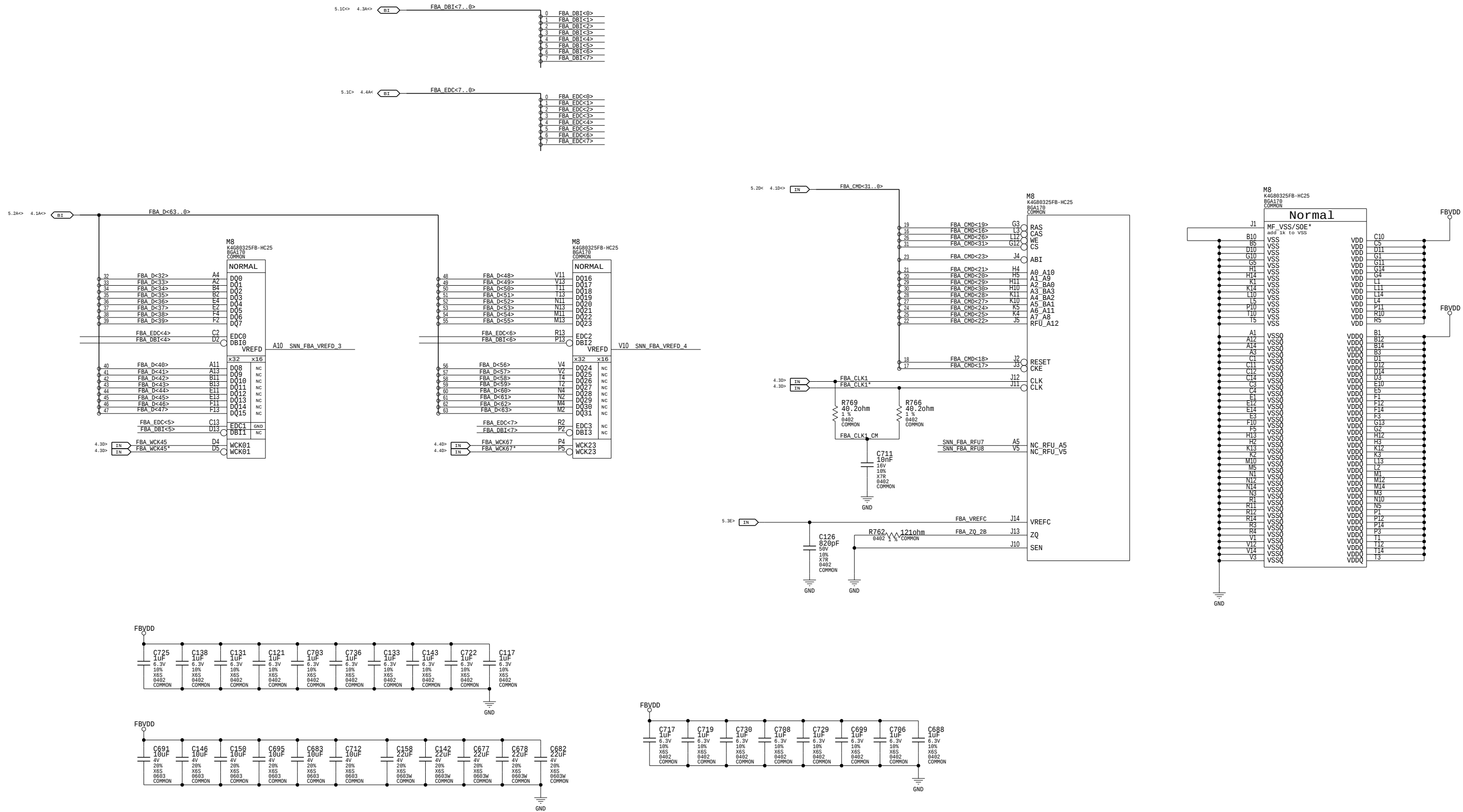


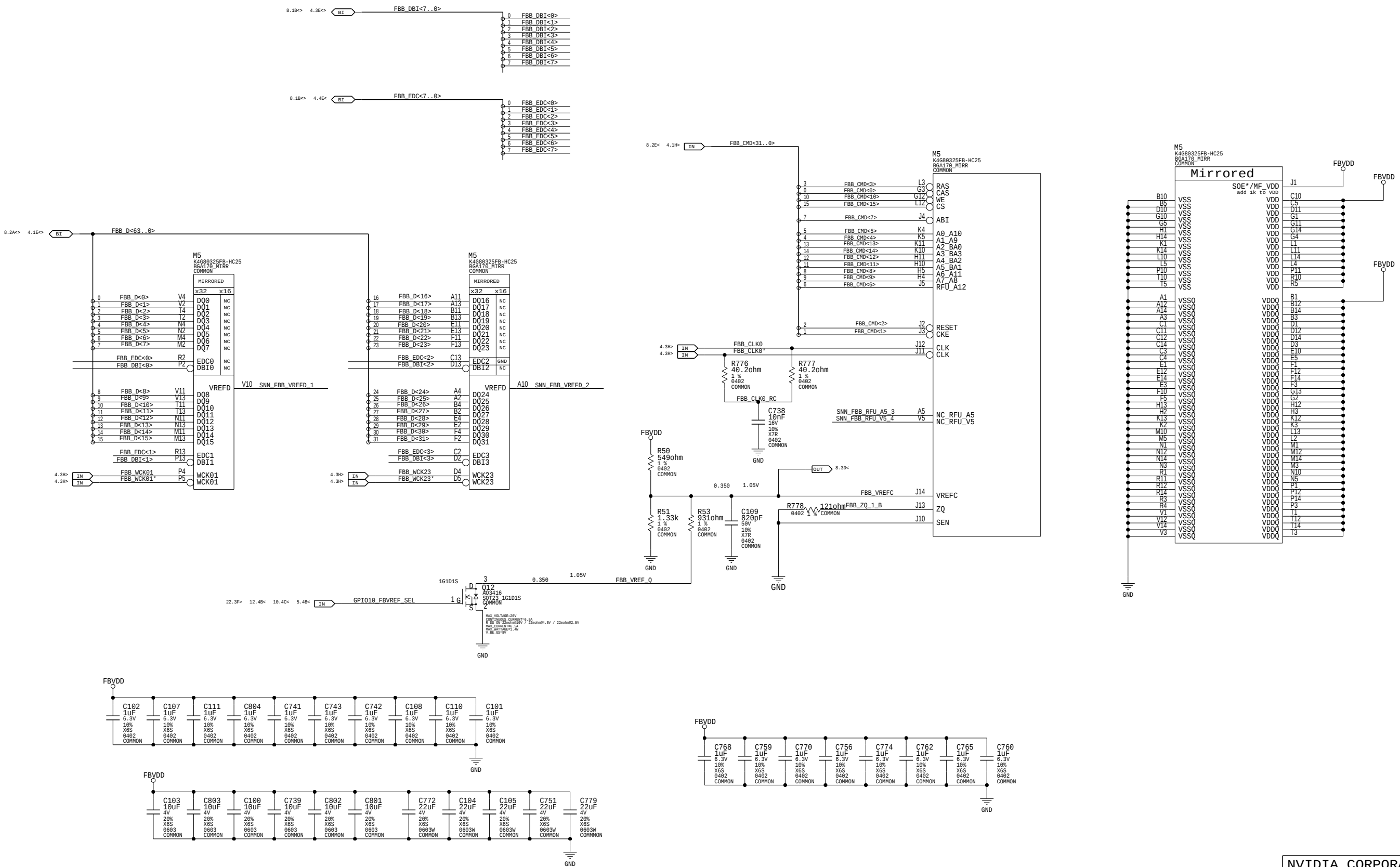
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ASSEMBLY	SKU0020 SCHEMATIC COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MEMORY: FBA[31:0]





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2

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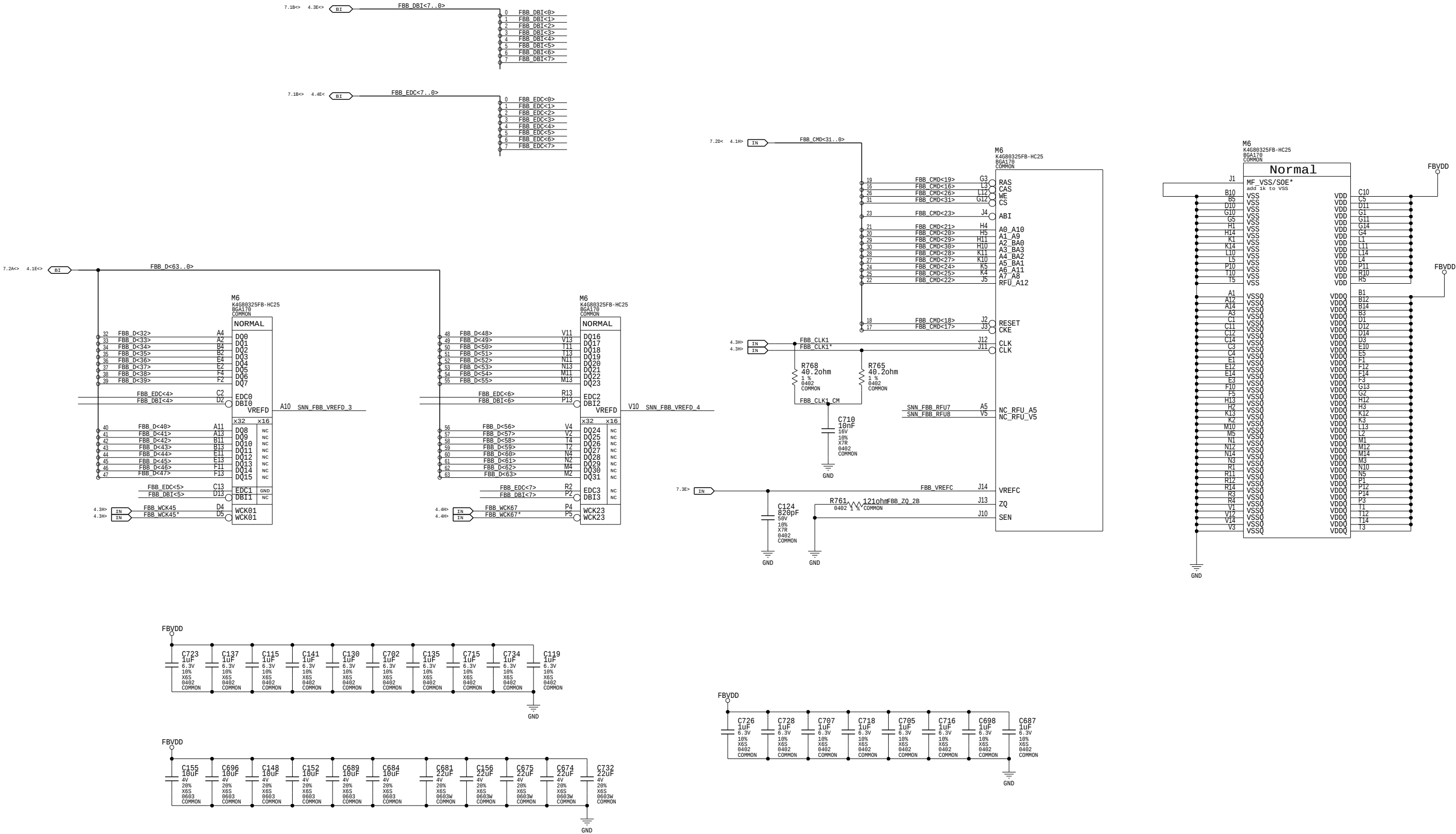
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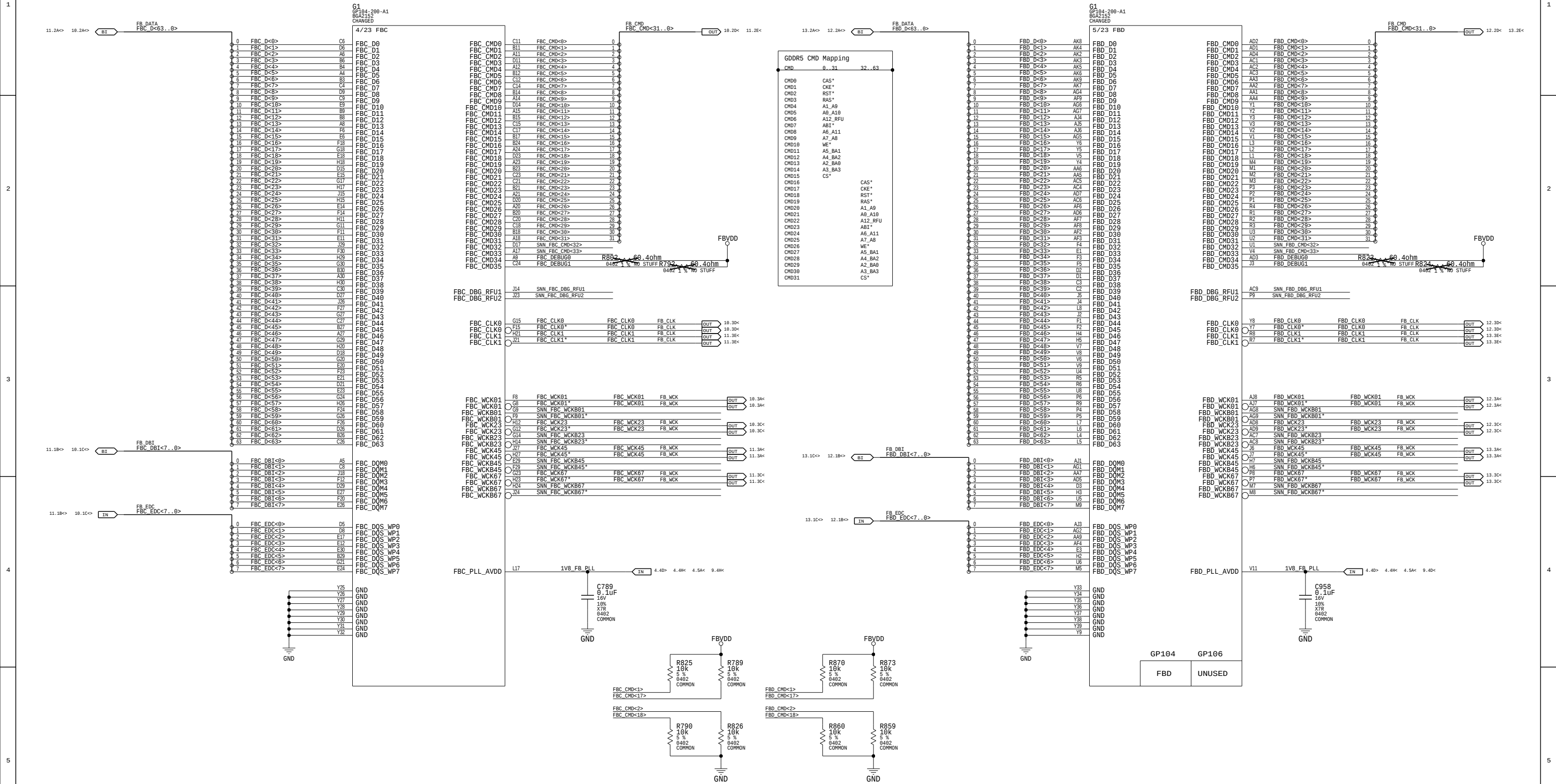
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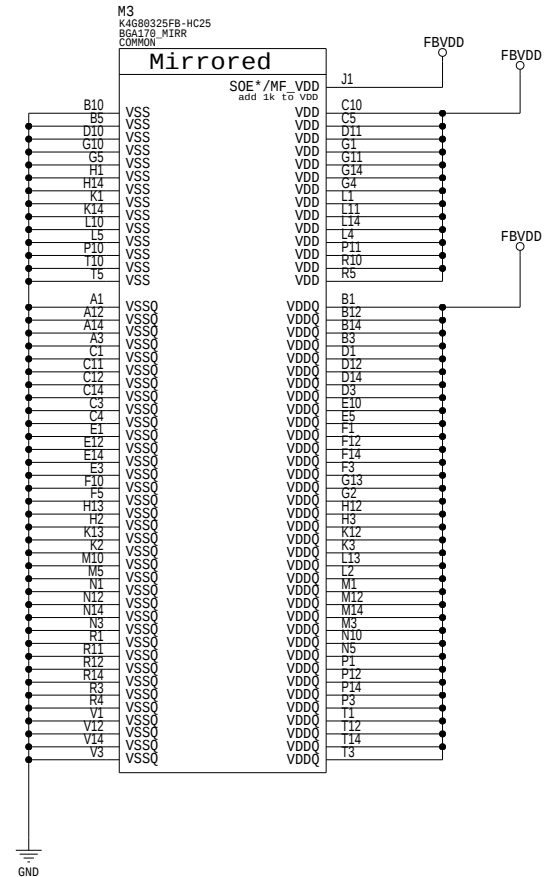
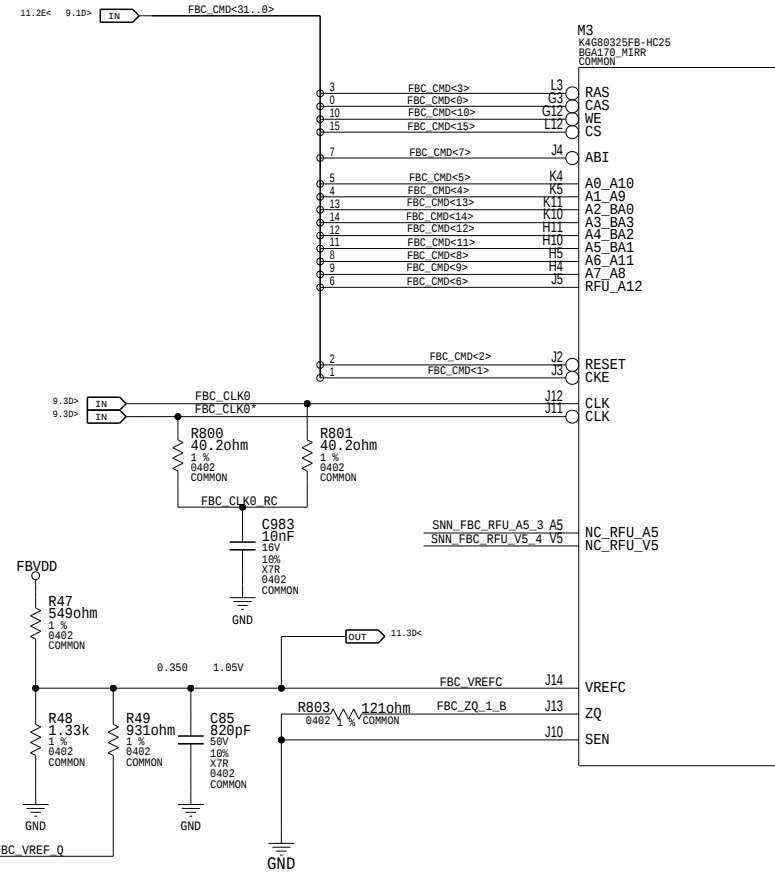
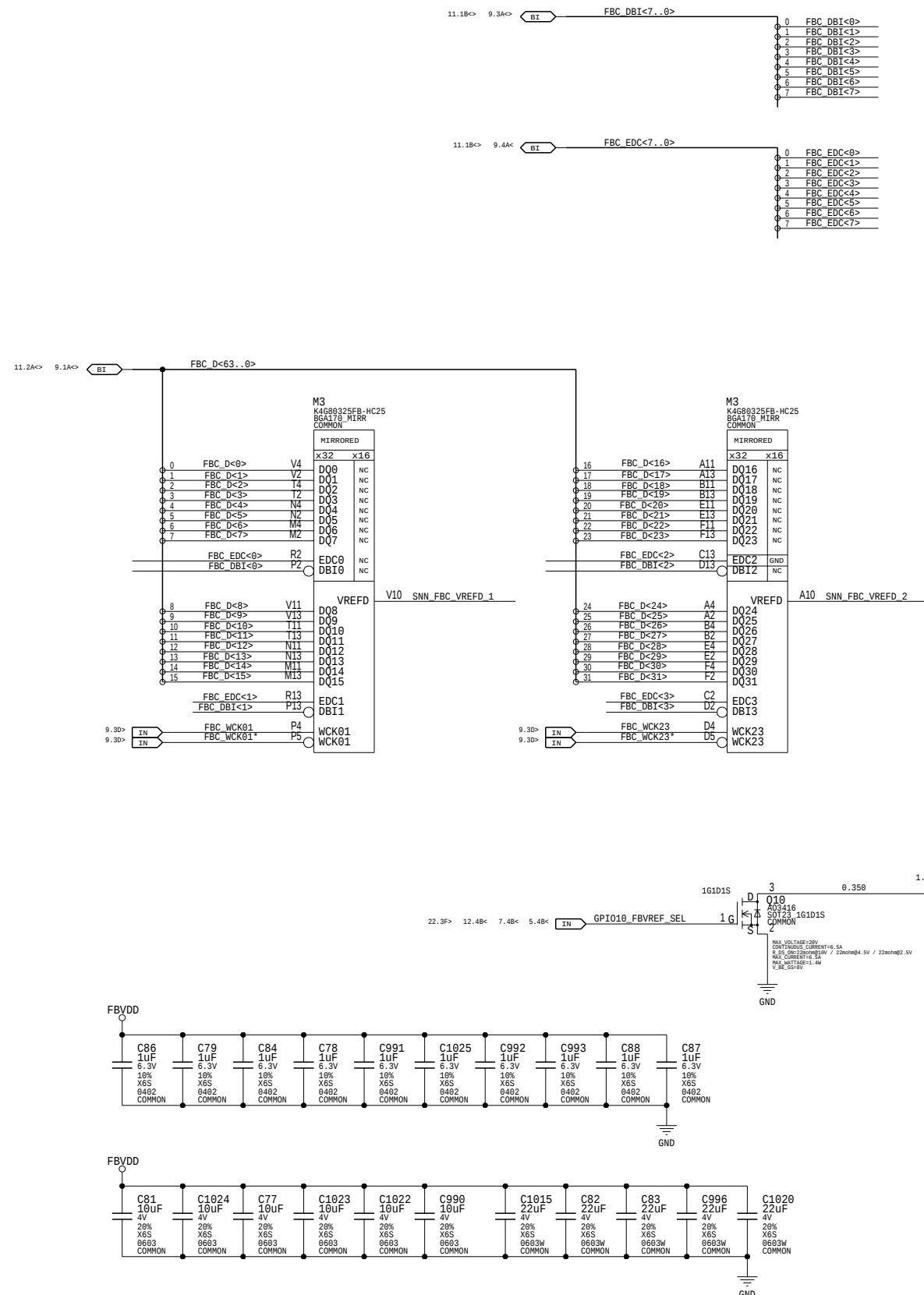
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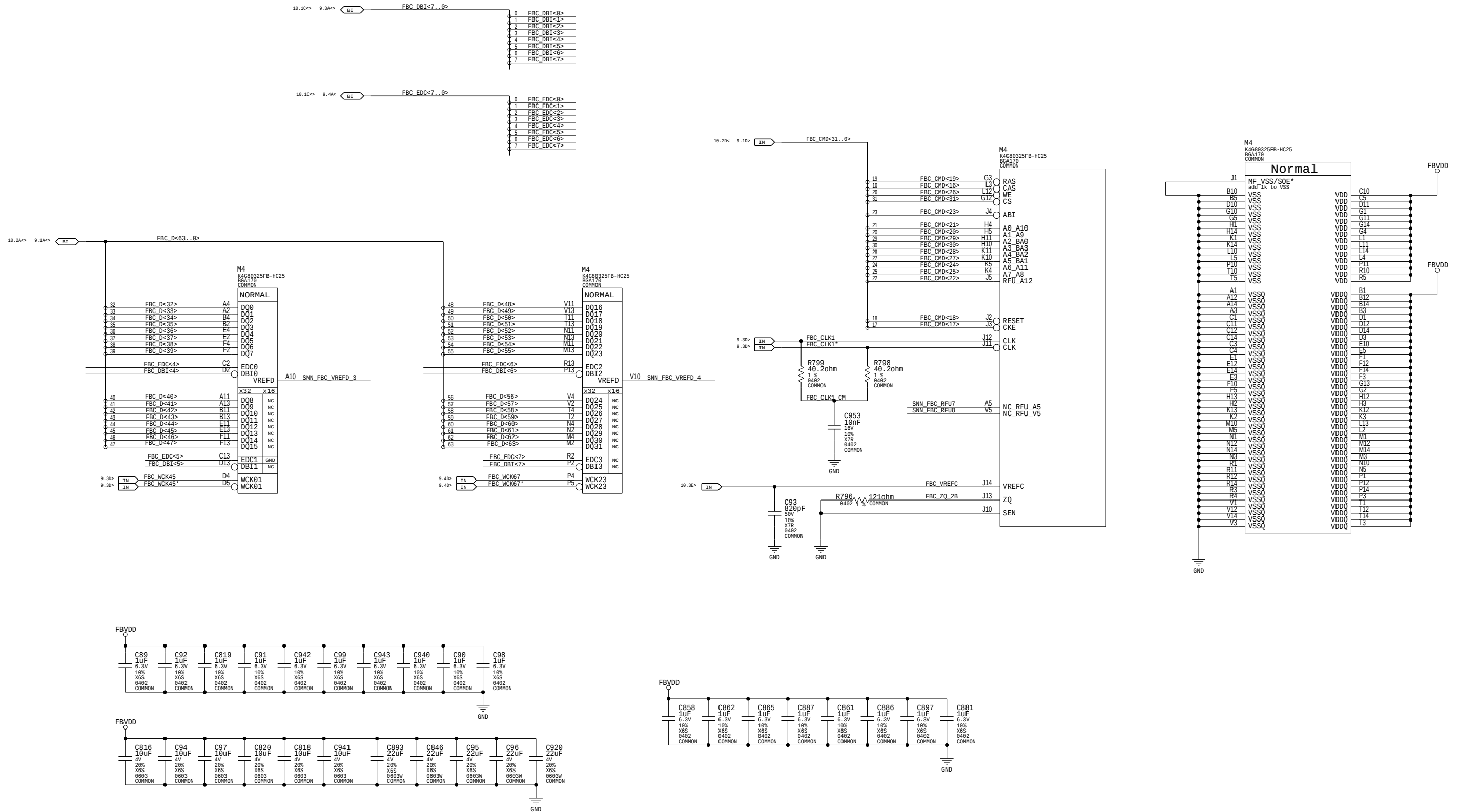


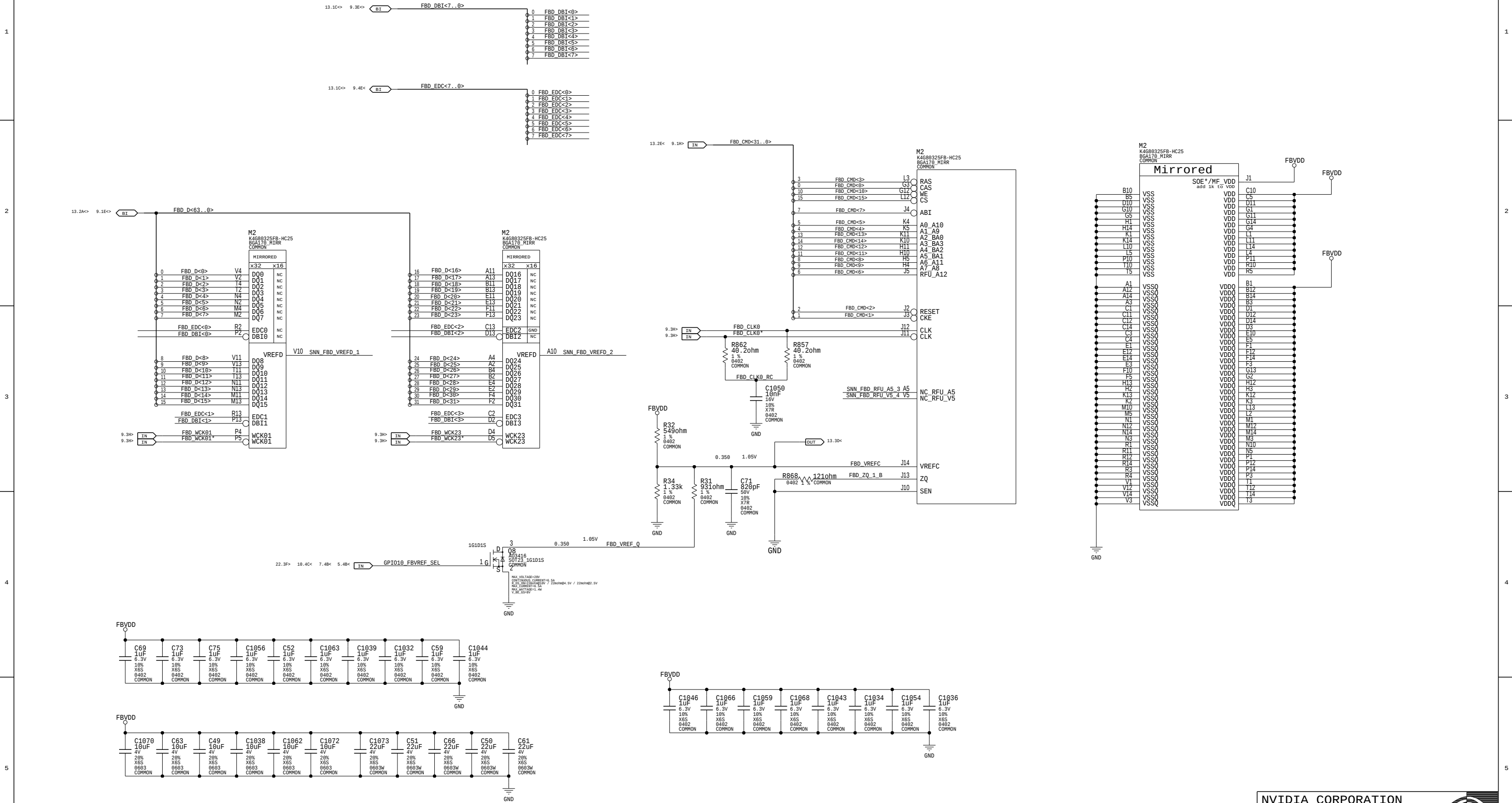


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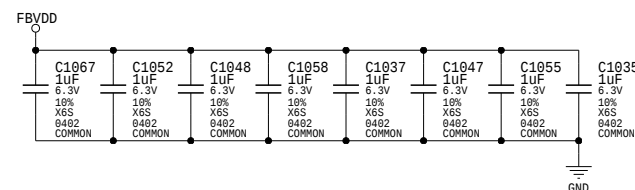
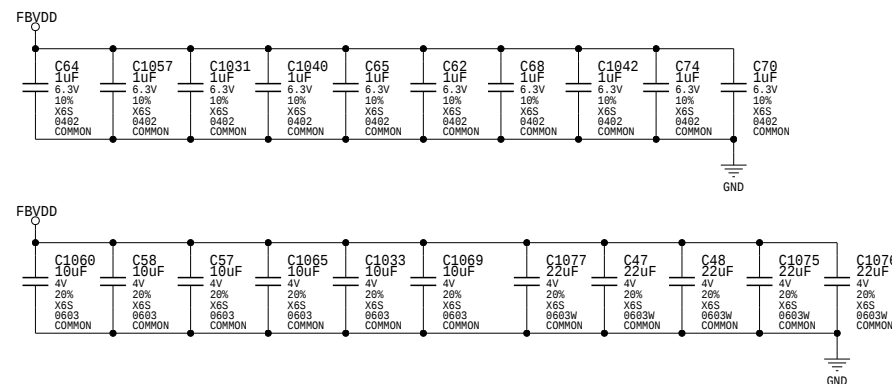
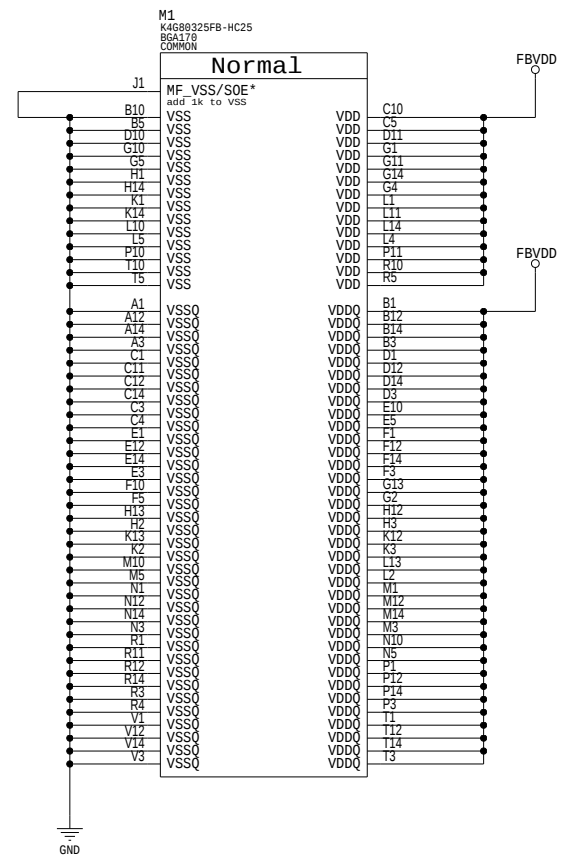
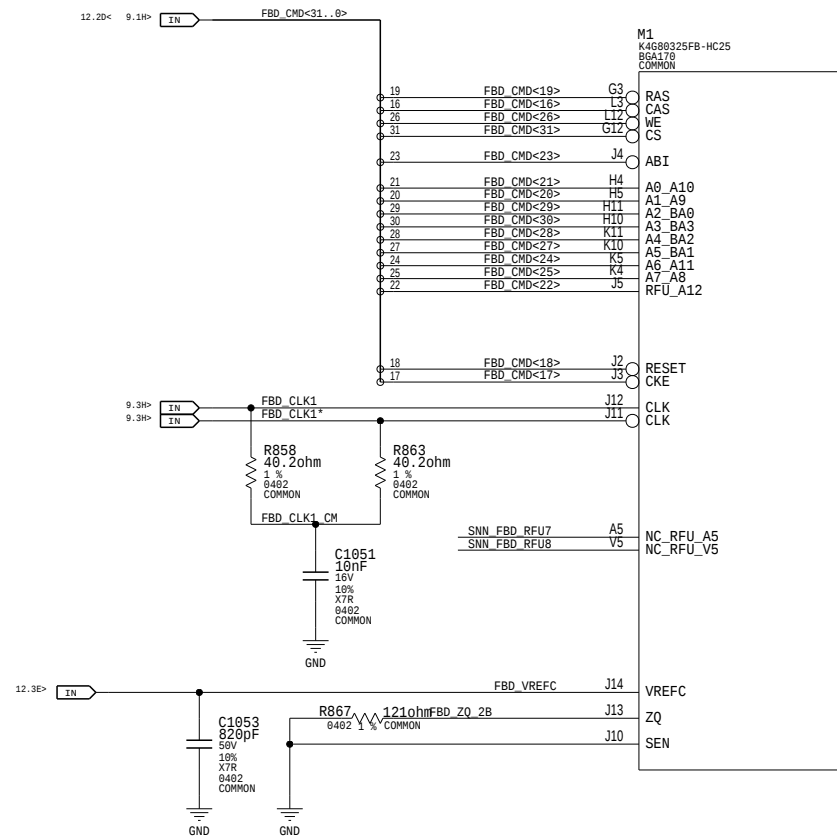
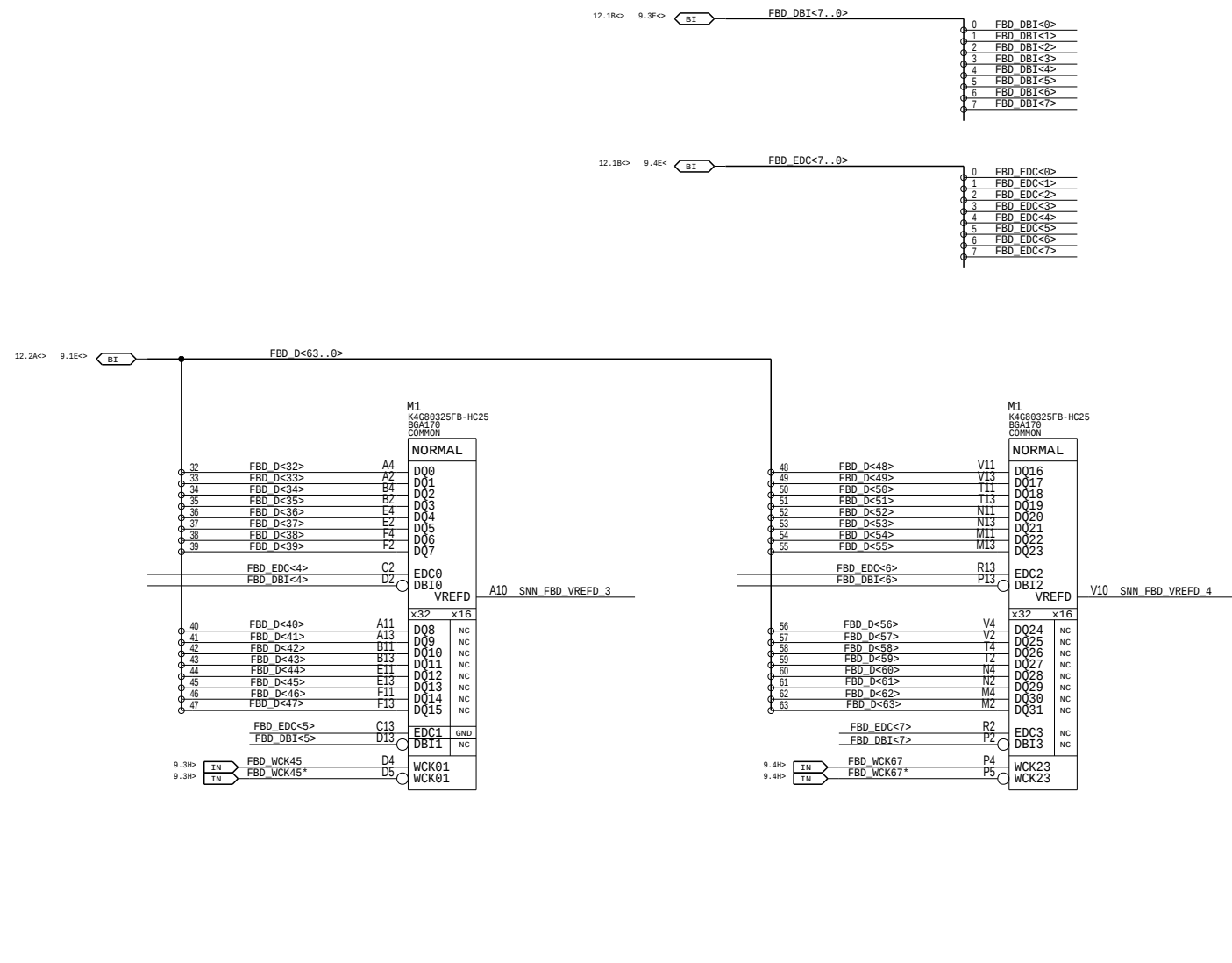
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Page11: MEMORY: FBC Partition 63..32

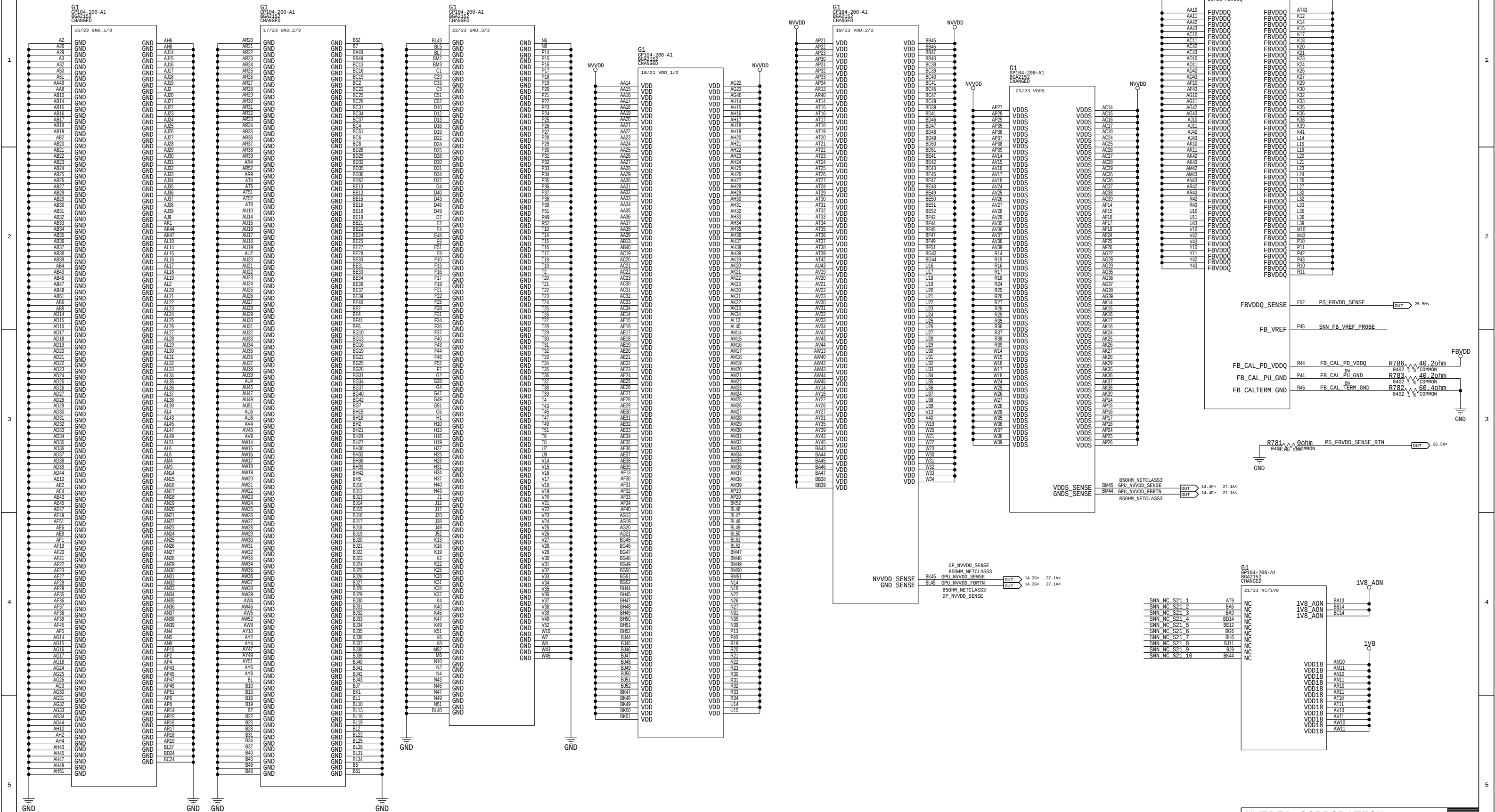




Page13: MEMORY: FBD Partition 63..32

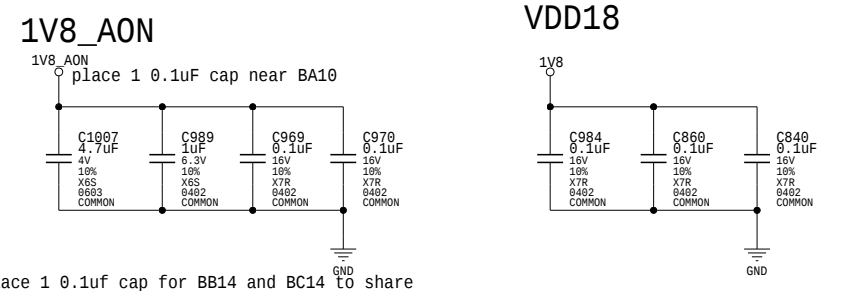
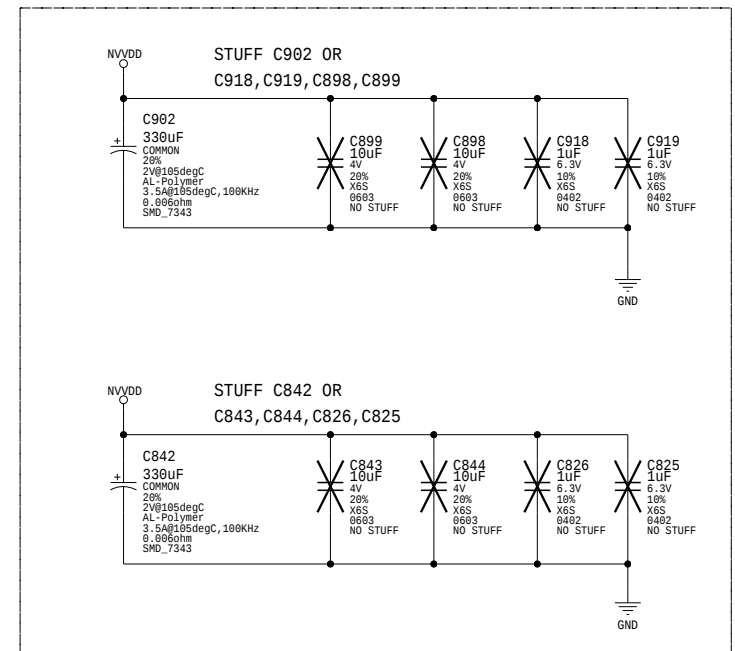
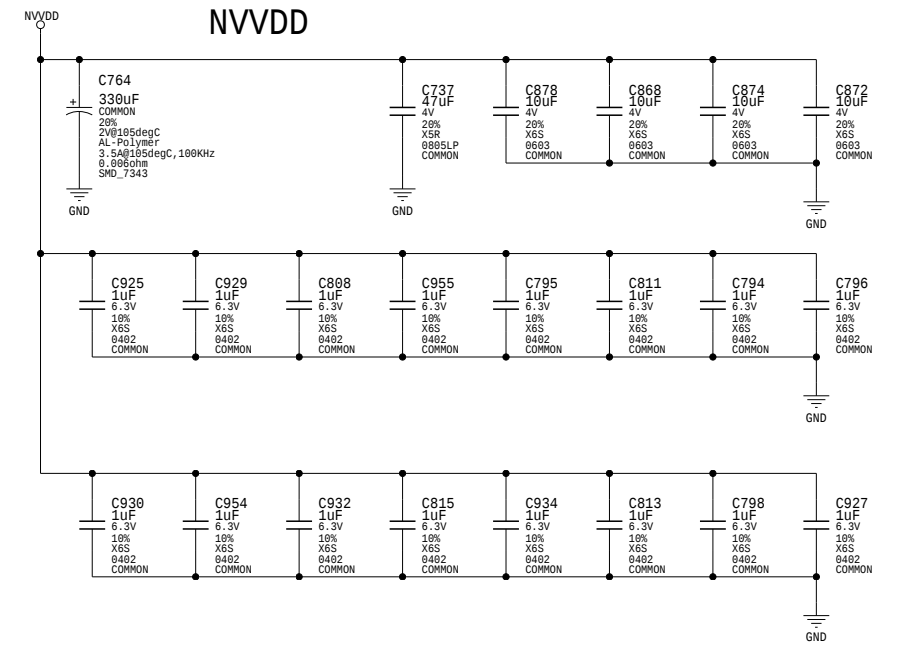
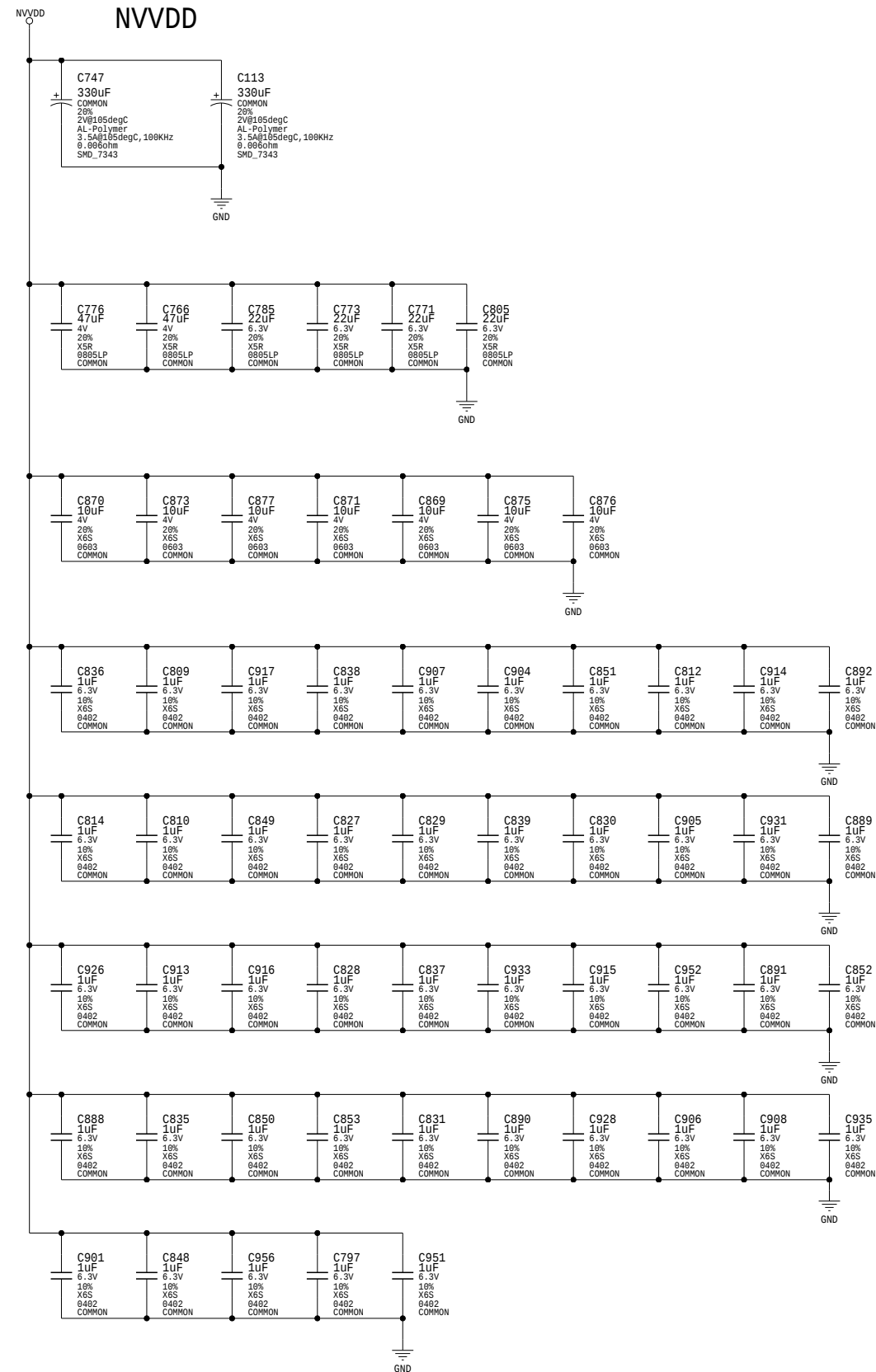
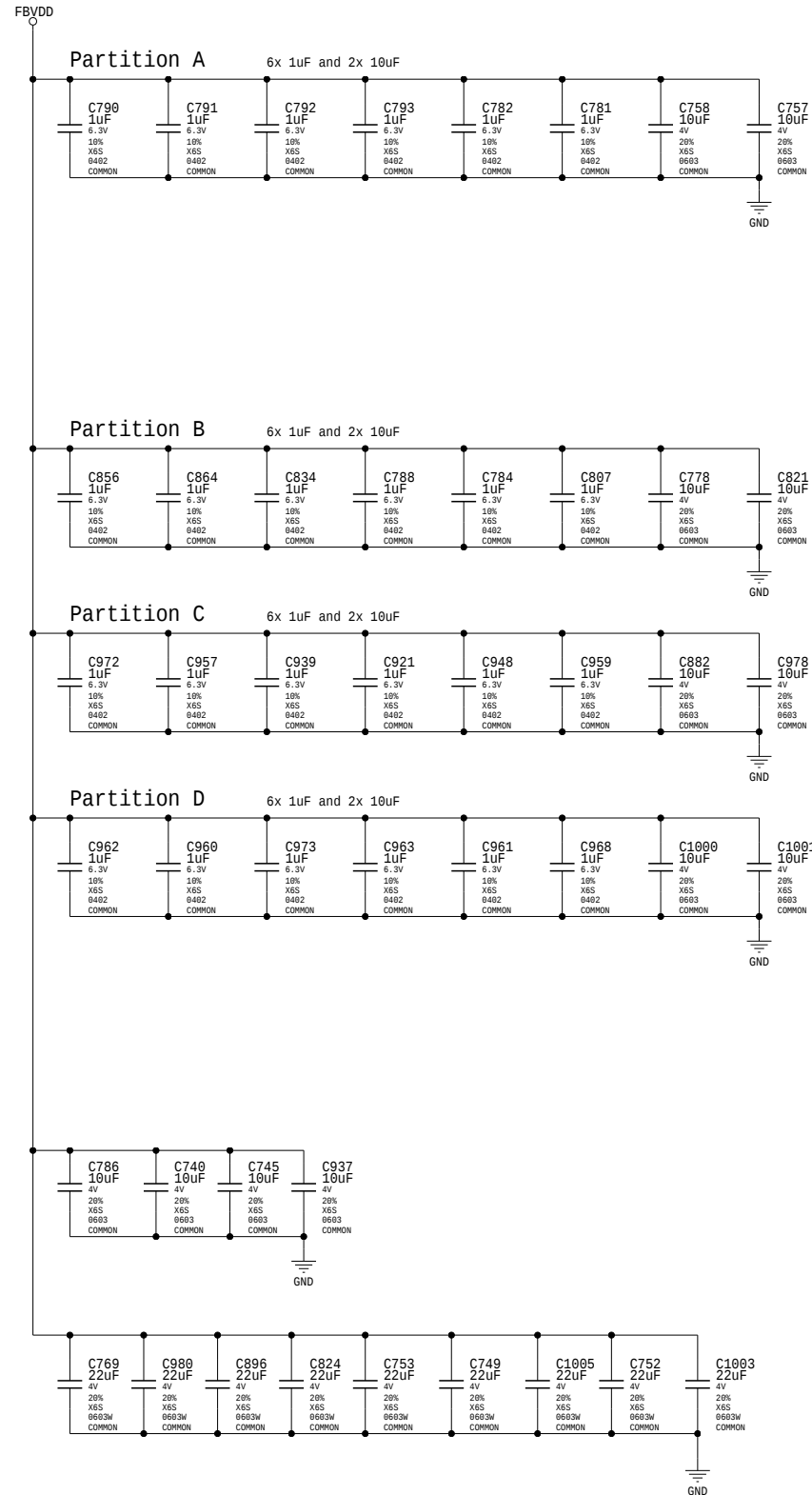


Page14: GPU PWR and GND



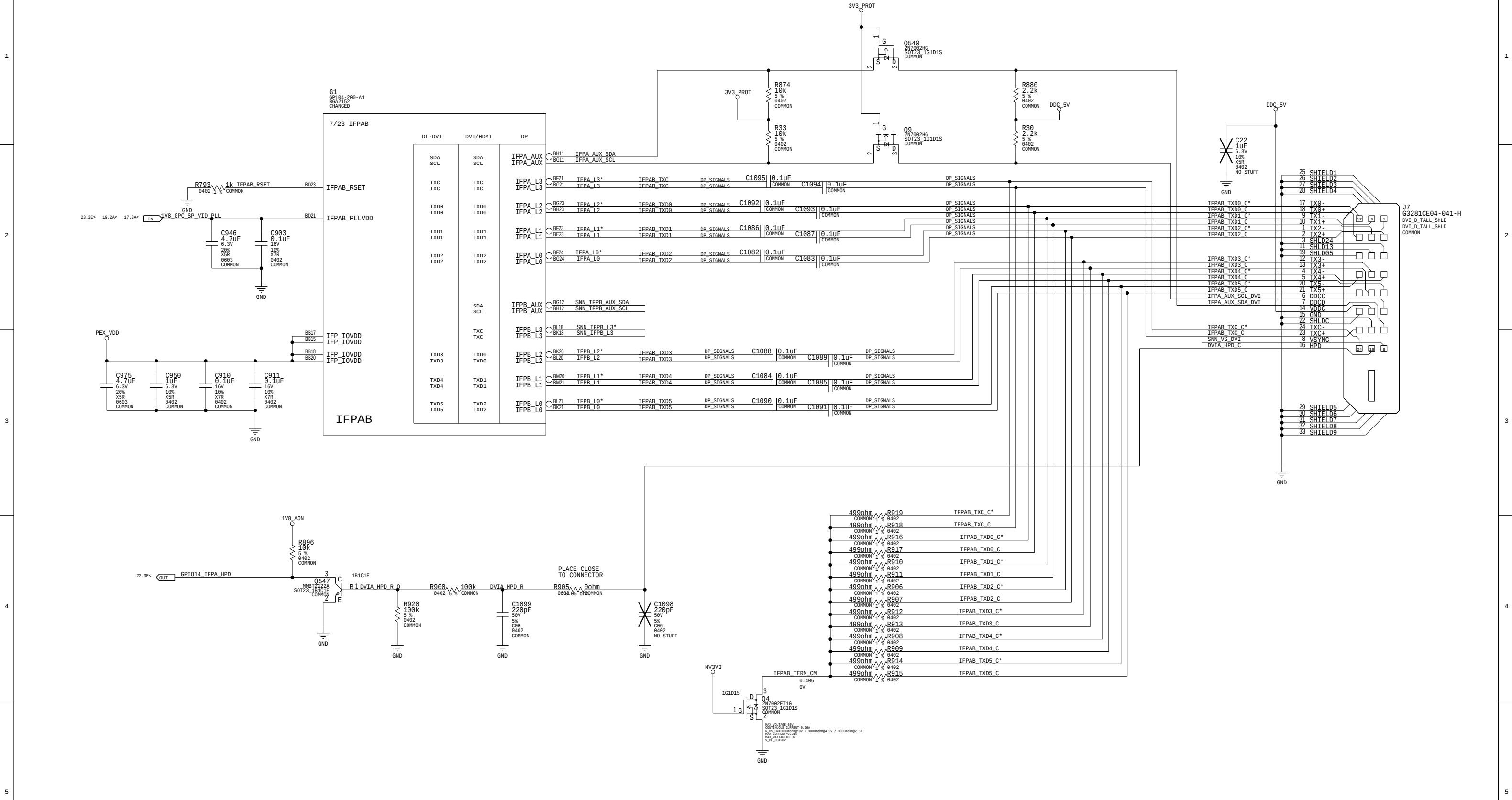
Page15: GPU Decoupling

FBVDD

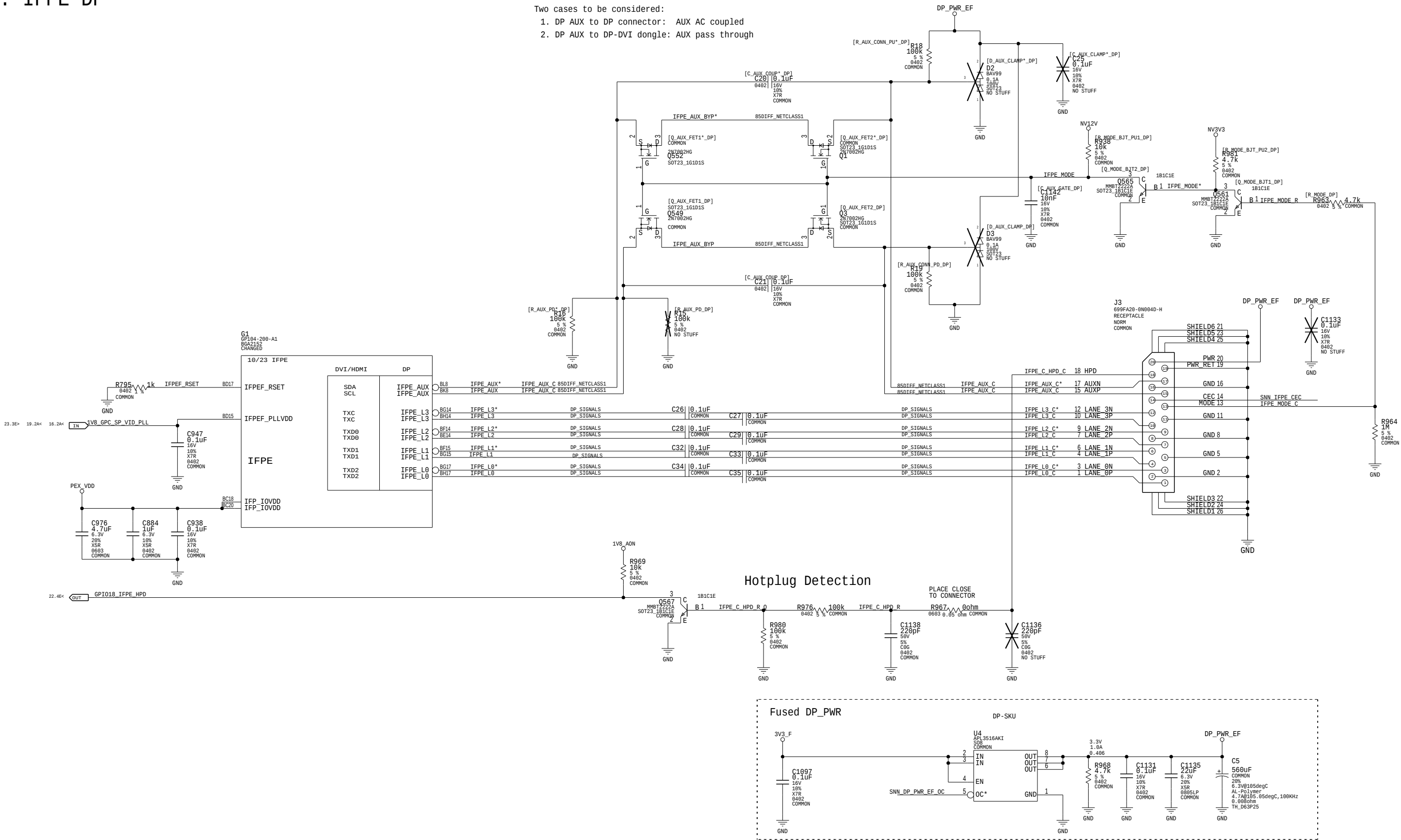


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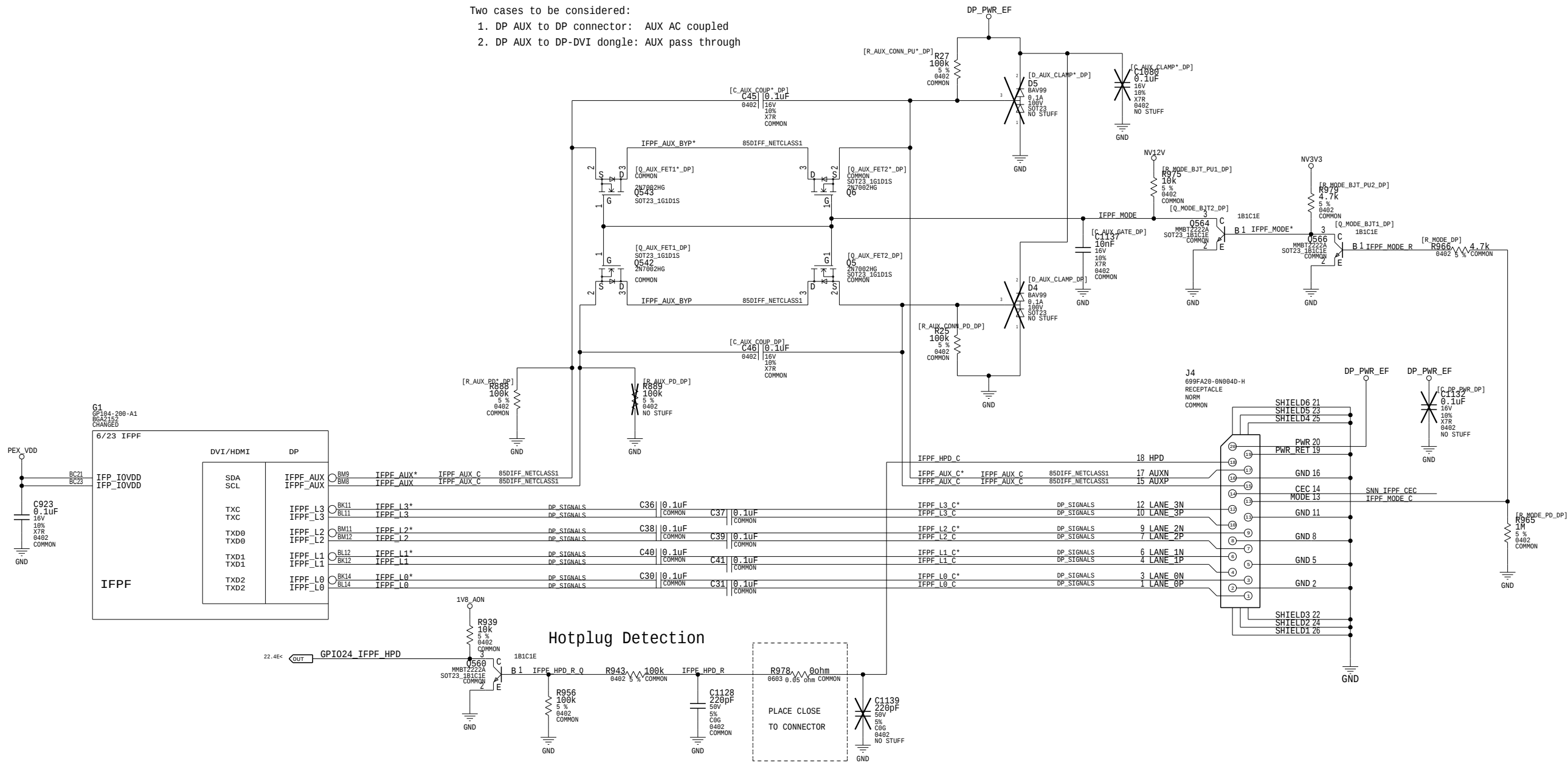
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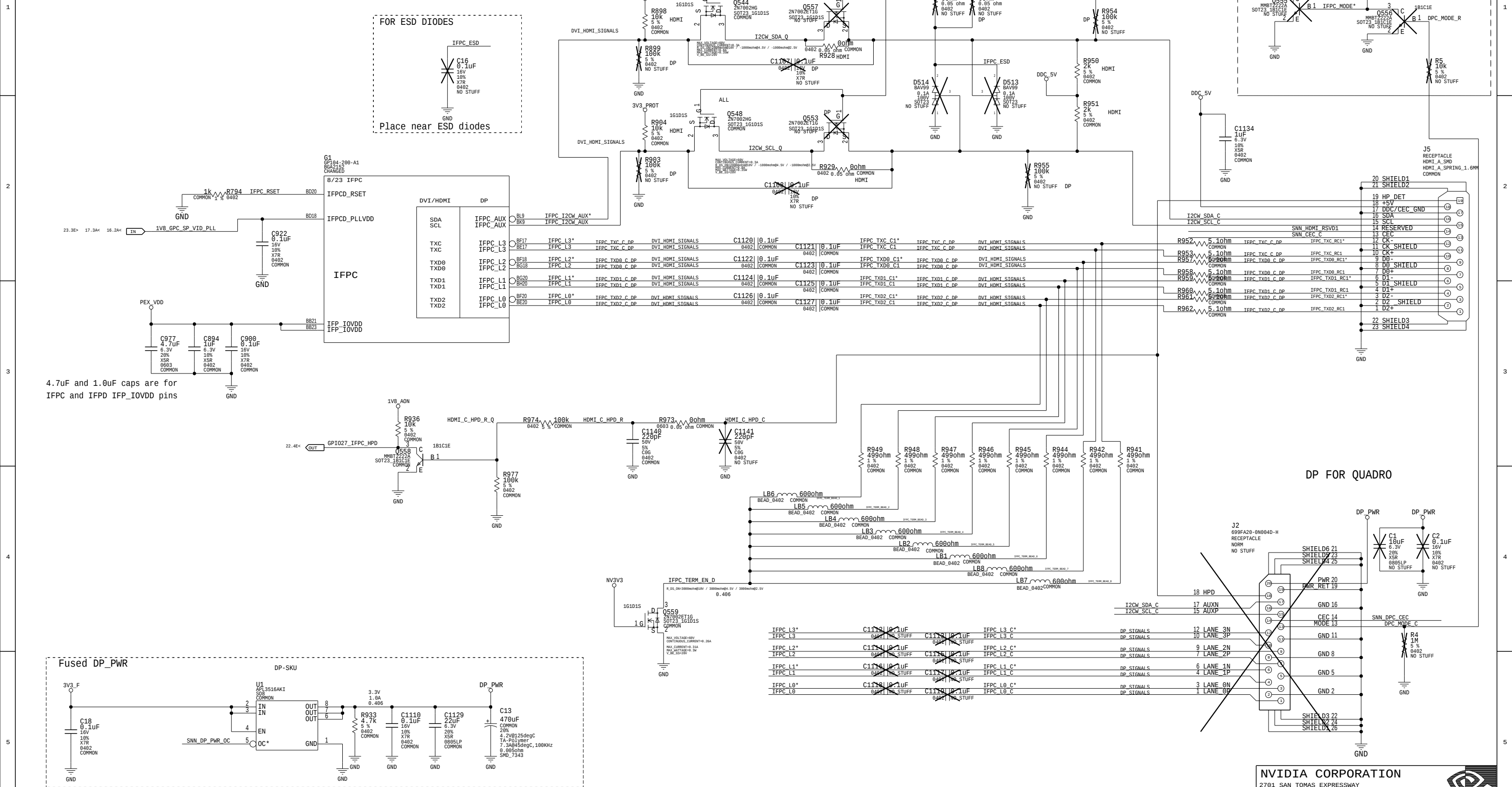


- Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through



- Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through





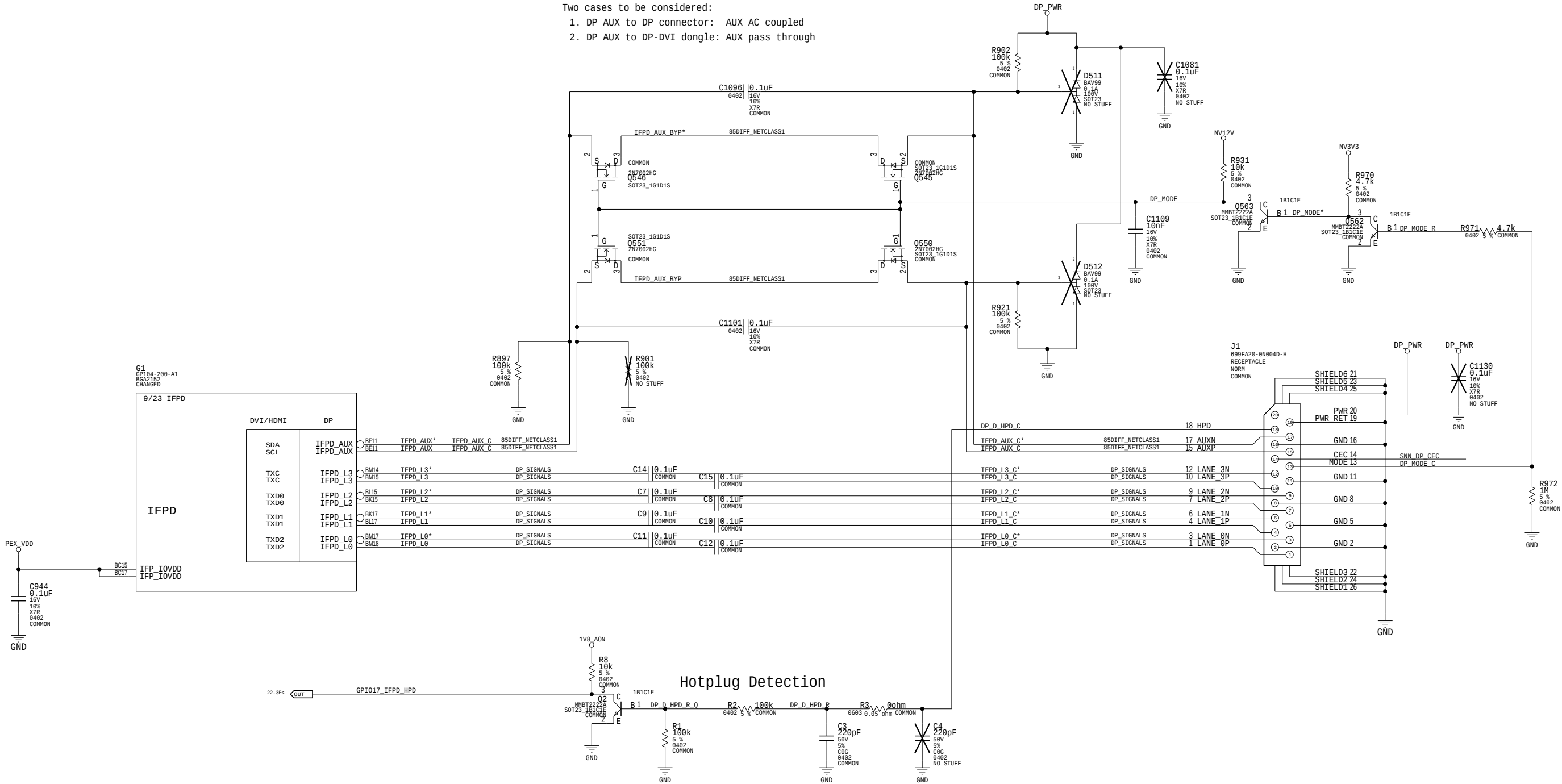
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PAGE DETAIL	IFPC HDMI 2.0/DP

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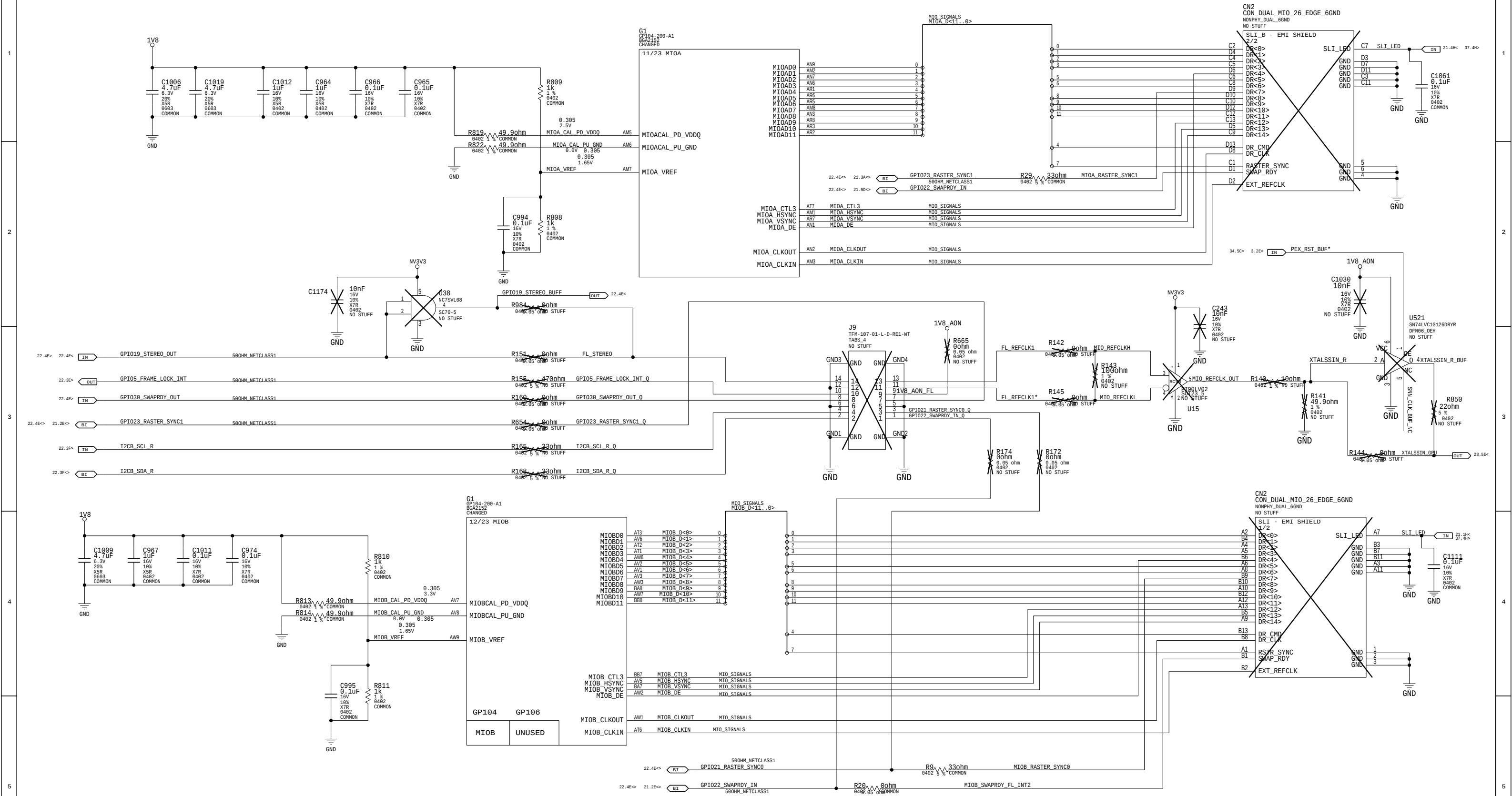
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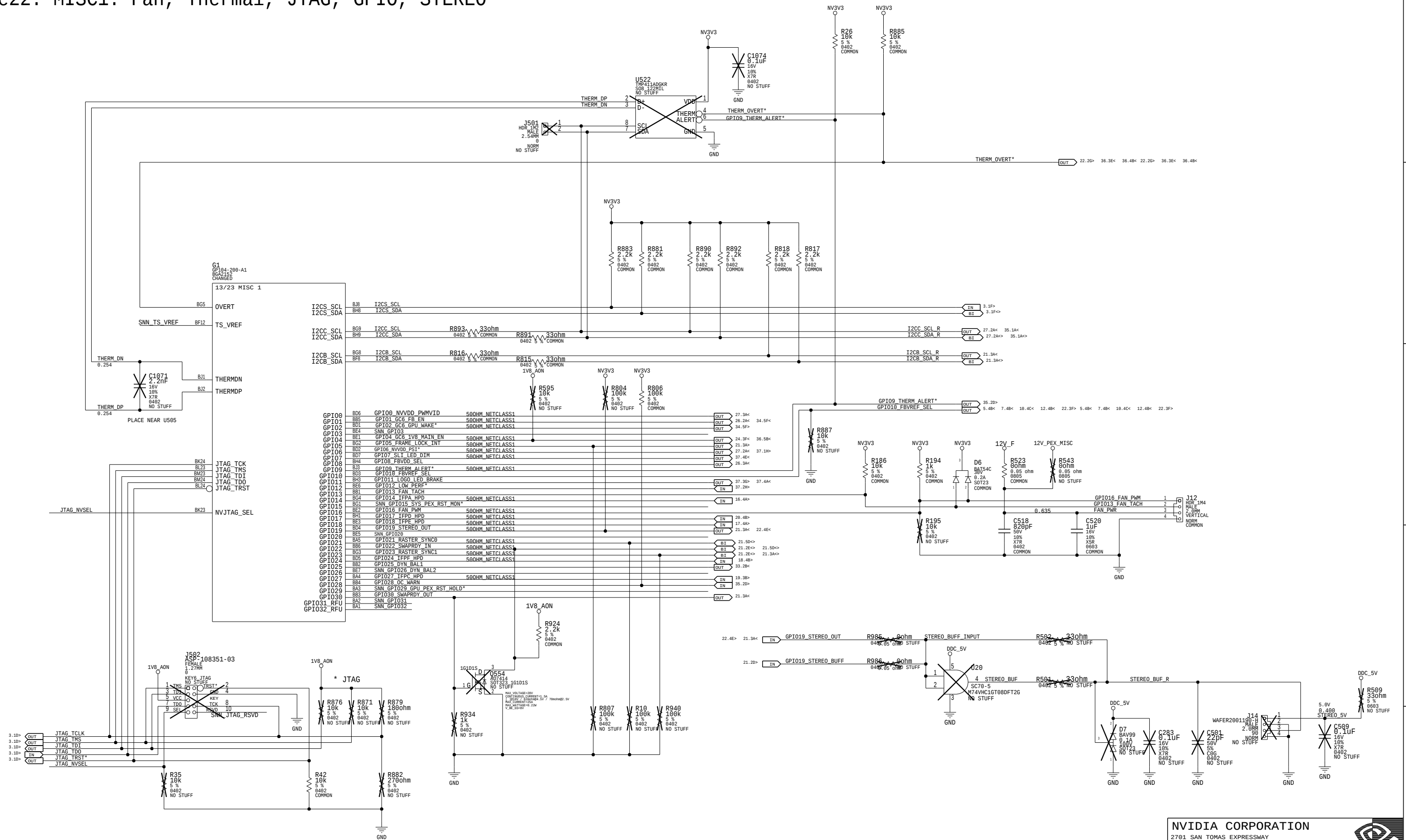


- Two cases to be considered:
- 1. DP AUX to DP connector: AUX AC coupled
 - 2. DP AUX to DP-DVI dongle: AUX pass through



Page21: MIOA/B Interface and FRAME LOCK





Page23: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]		
L	L	L	00000		
L	H	L	00010		
L	H	H	00011		
H	H	L	00110		
H	H	H	00111		
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE	
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE	
L	L	H	1110		
L	H	L	1101		
L	H	H	1100		
H	L	L	1011		
H	L	H	1010		
H	H	L	1001		
H	H	H	1000		
L	L	M	0111		
L	M	L	0110		
L	M	H	0101		
L	H	M	0100		
H	L	M	0011		
H	M	L	0010		
H	M	H	0001		
H	H	M	0000		

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

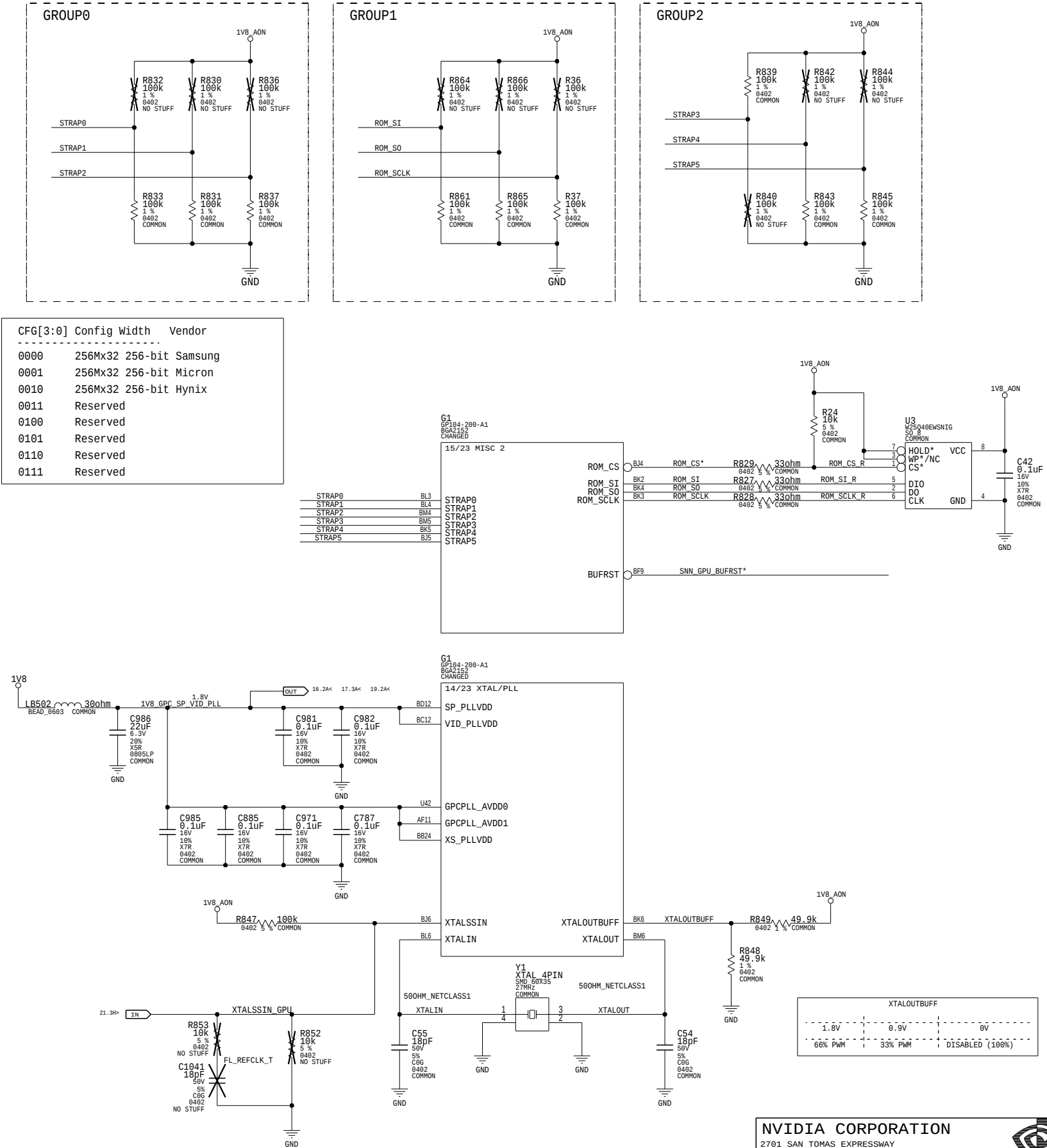
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

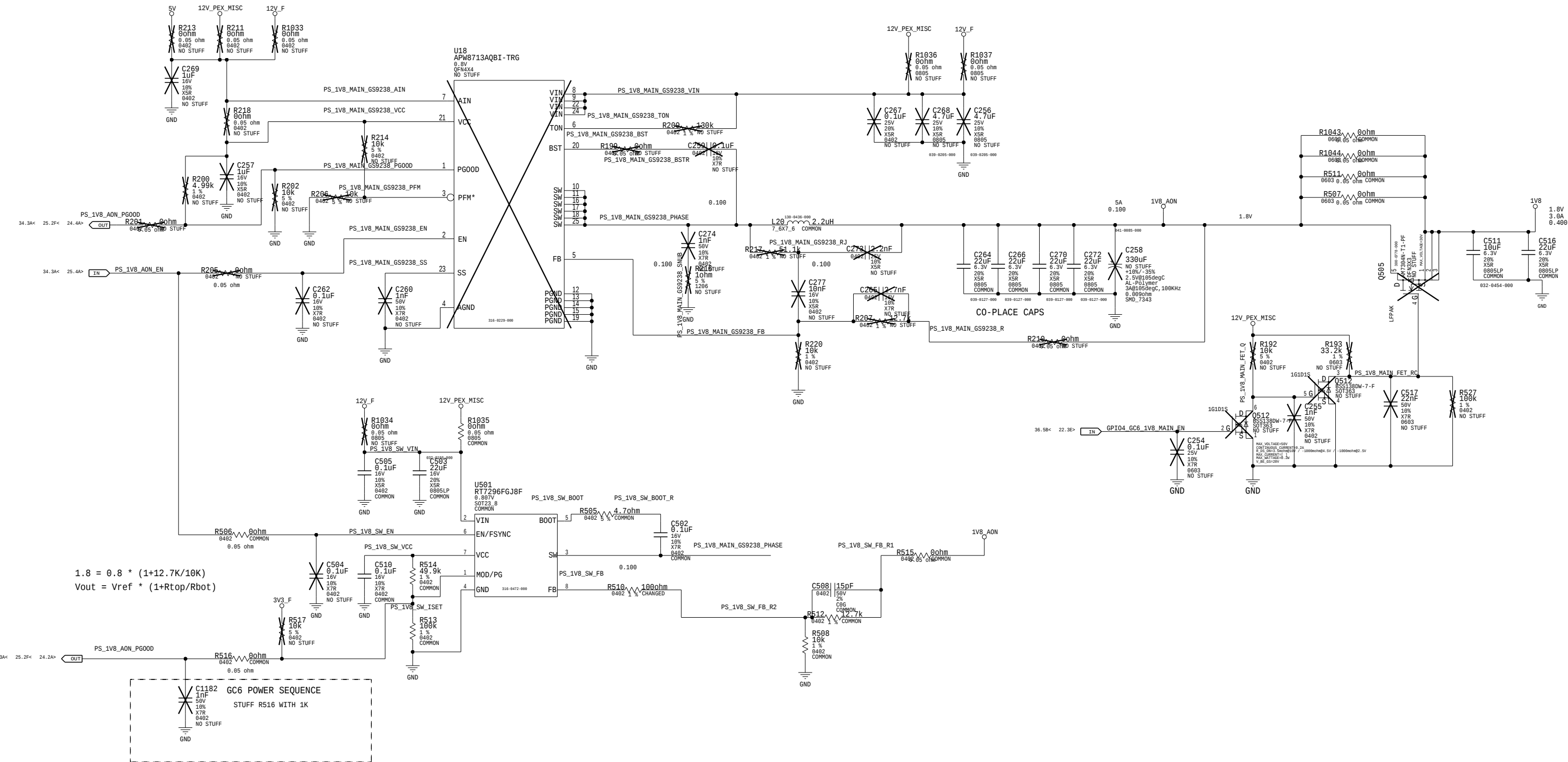
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

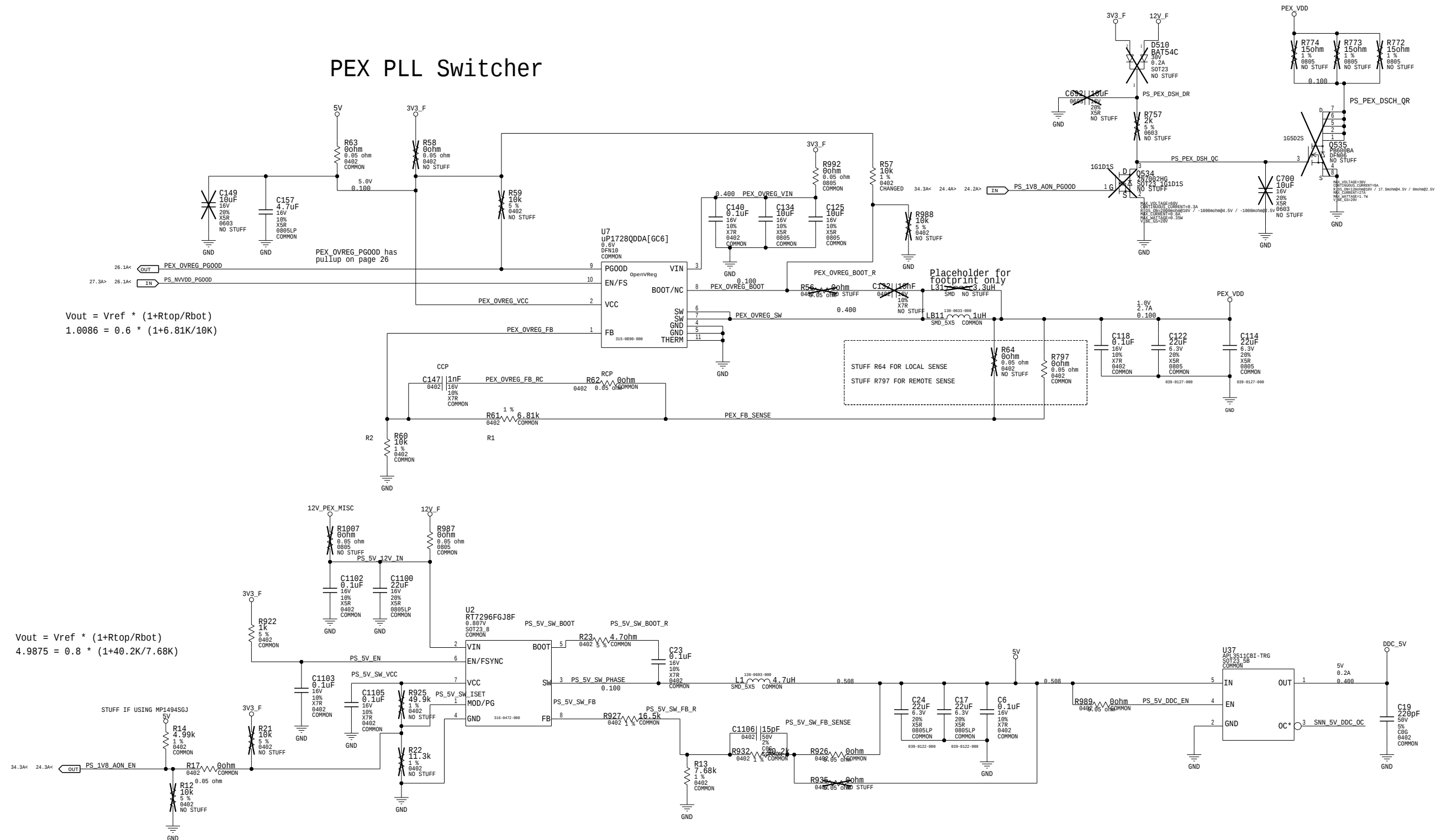
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE





PEX PLL Switcher

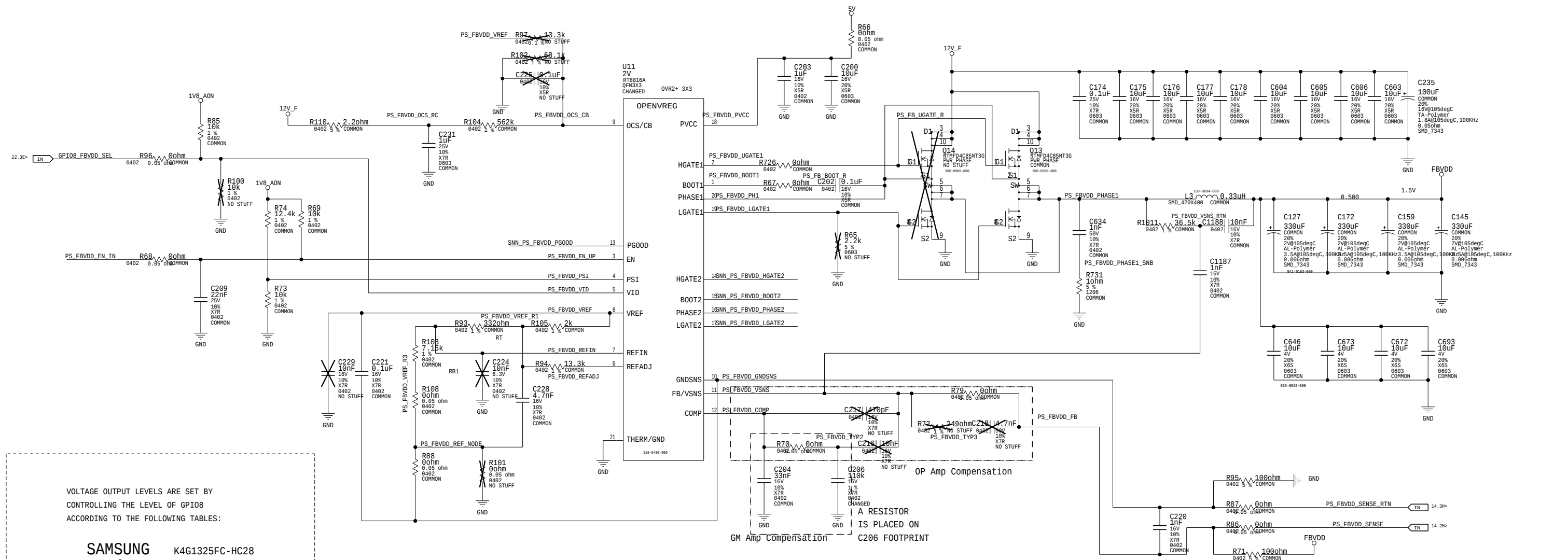
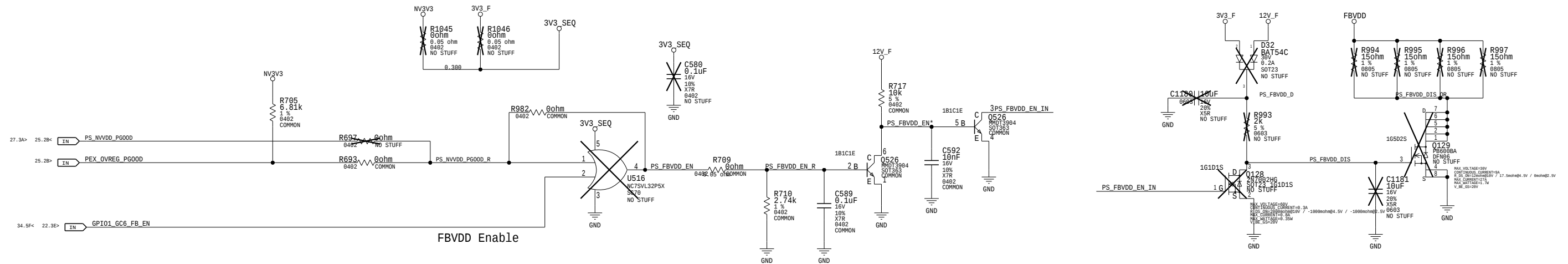


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PAGE DETAIL	PS: 5V, PEX VDD

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Page26: PS: FBVDD



SAMSUNG		K4G1325FC - HC28
GPI08	LEVEL	FBVDD OUTPUT VOLTAGE
0		1.35V
1		1.55V

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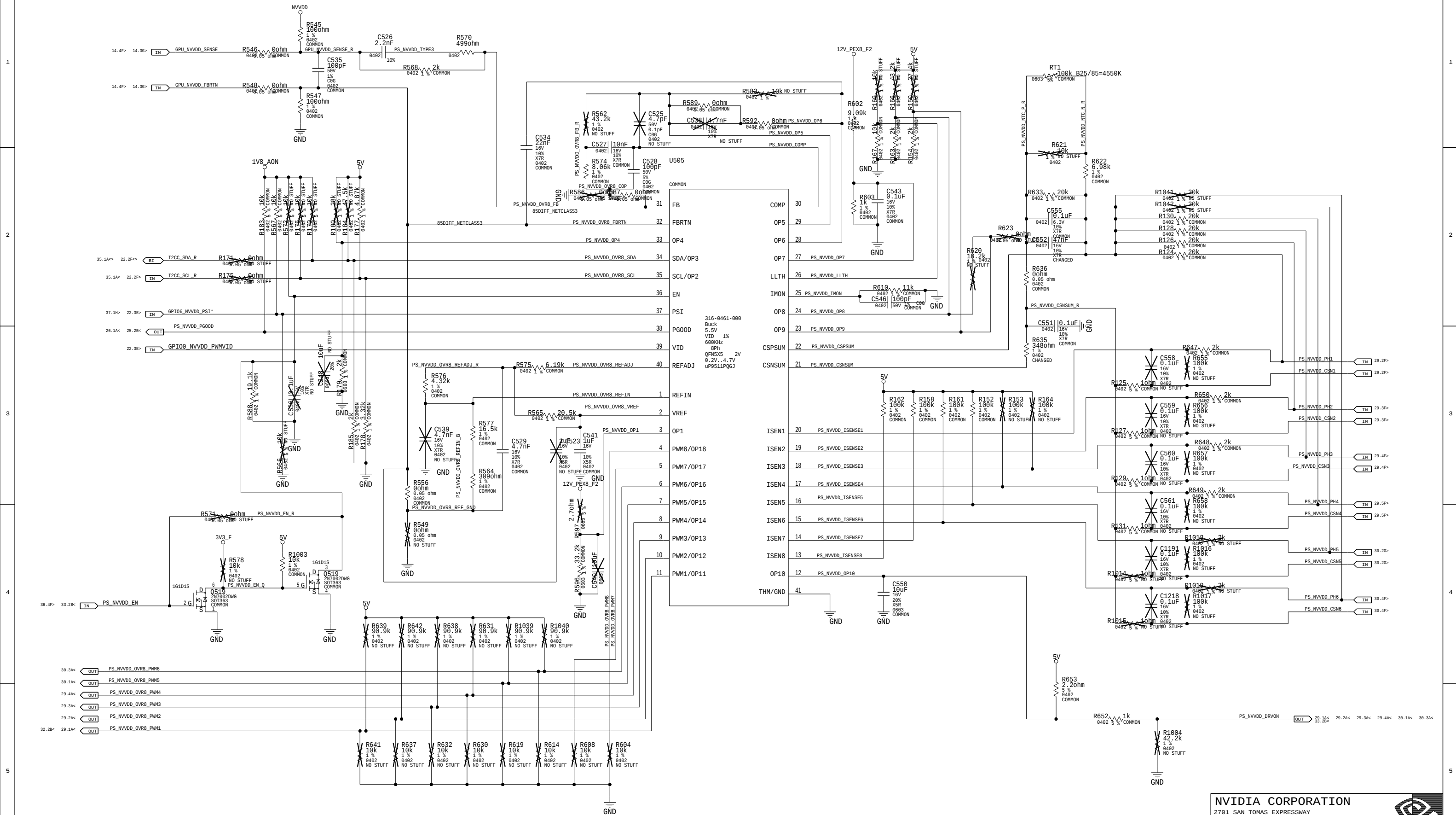
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Page27: PS: NVVDD_OVR8



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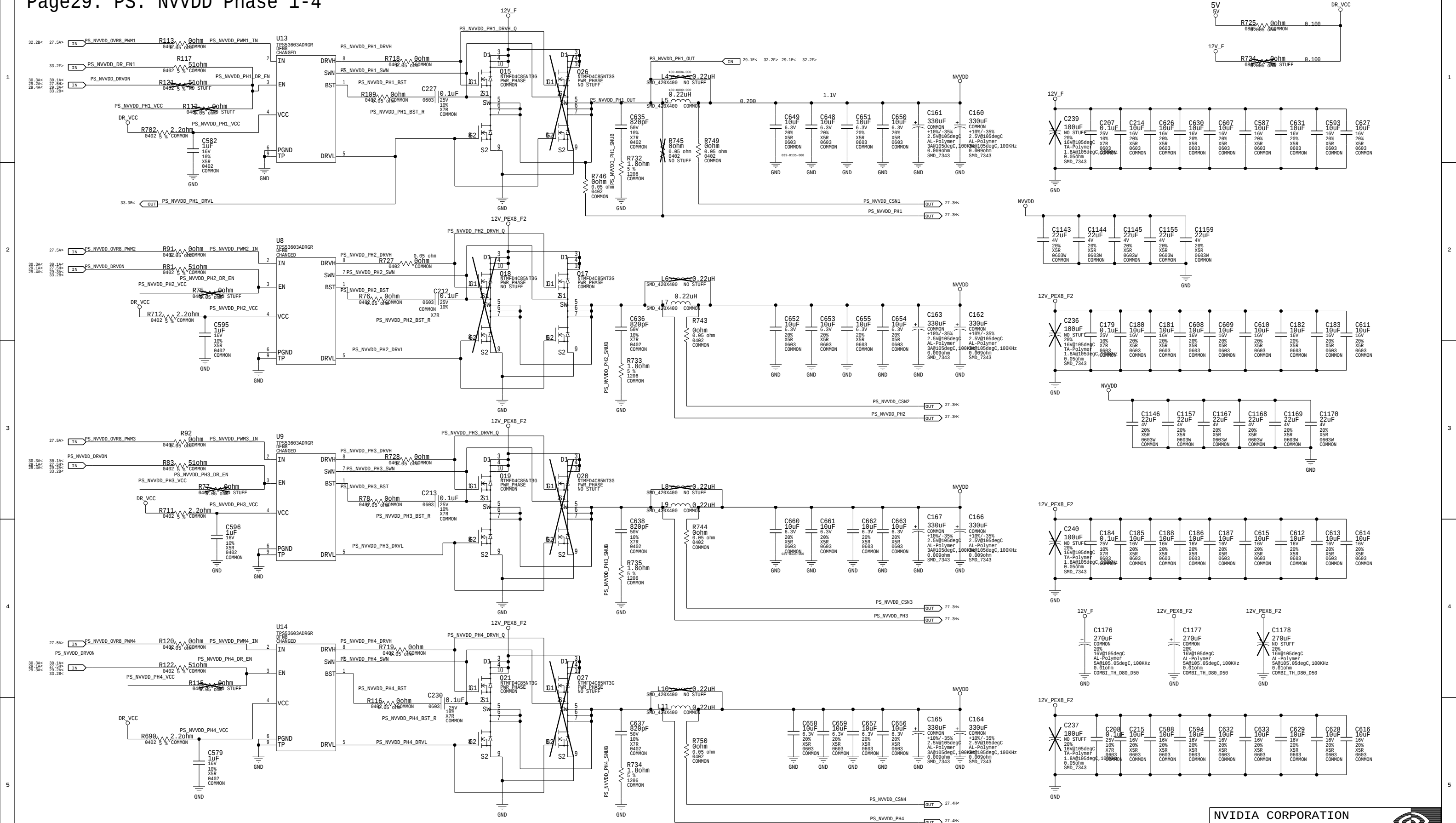
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Page29: PS: NVVDD Phase 1-4



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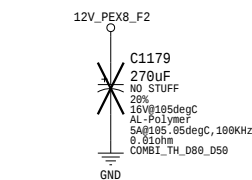
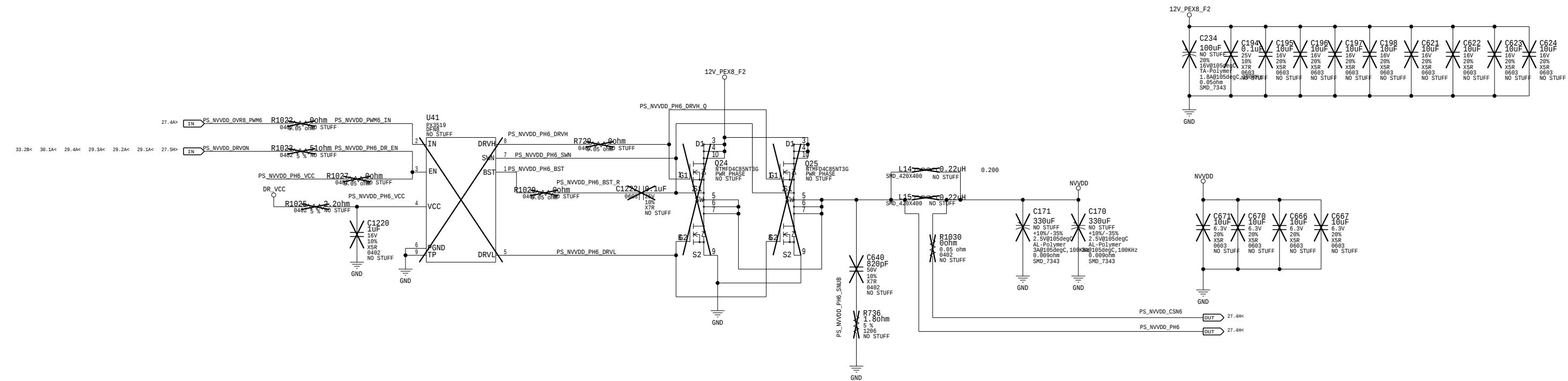
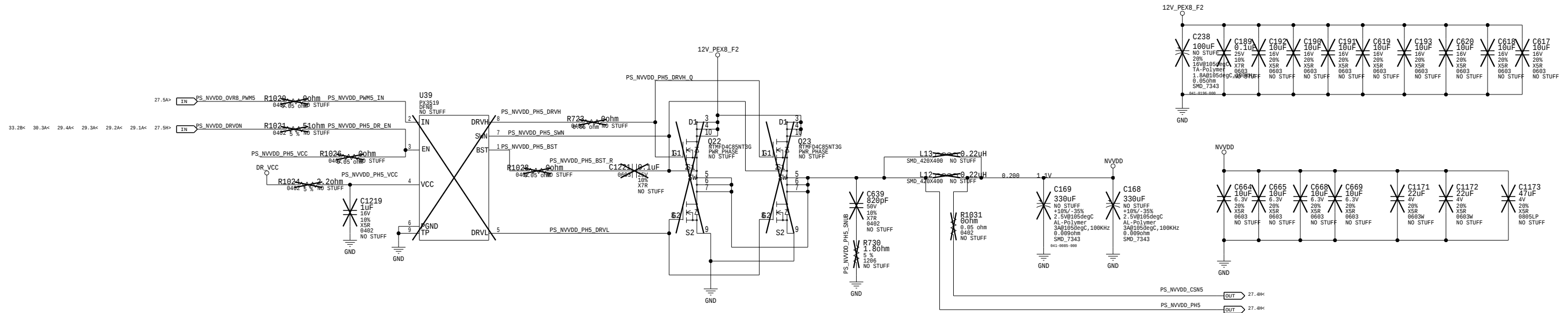
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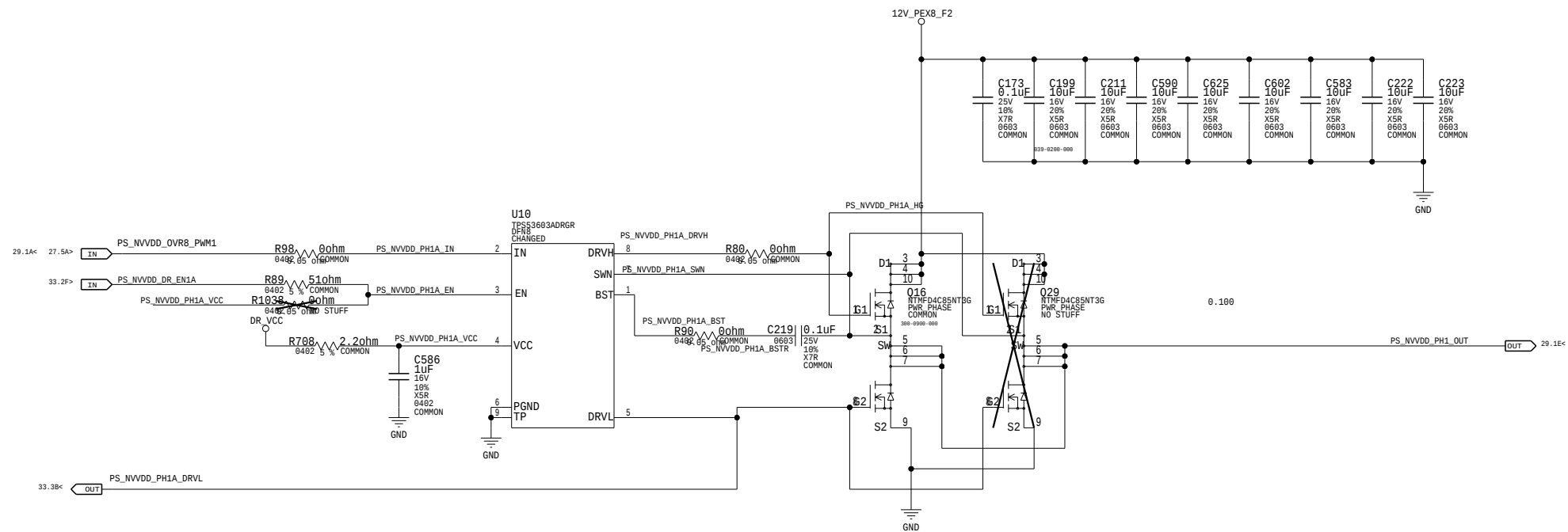
Page30: PS: NVVDD Phase 5 & 6



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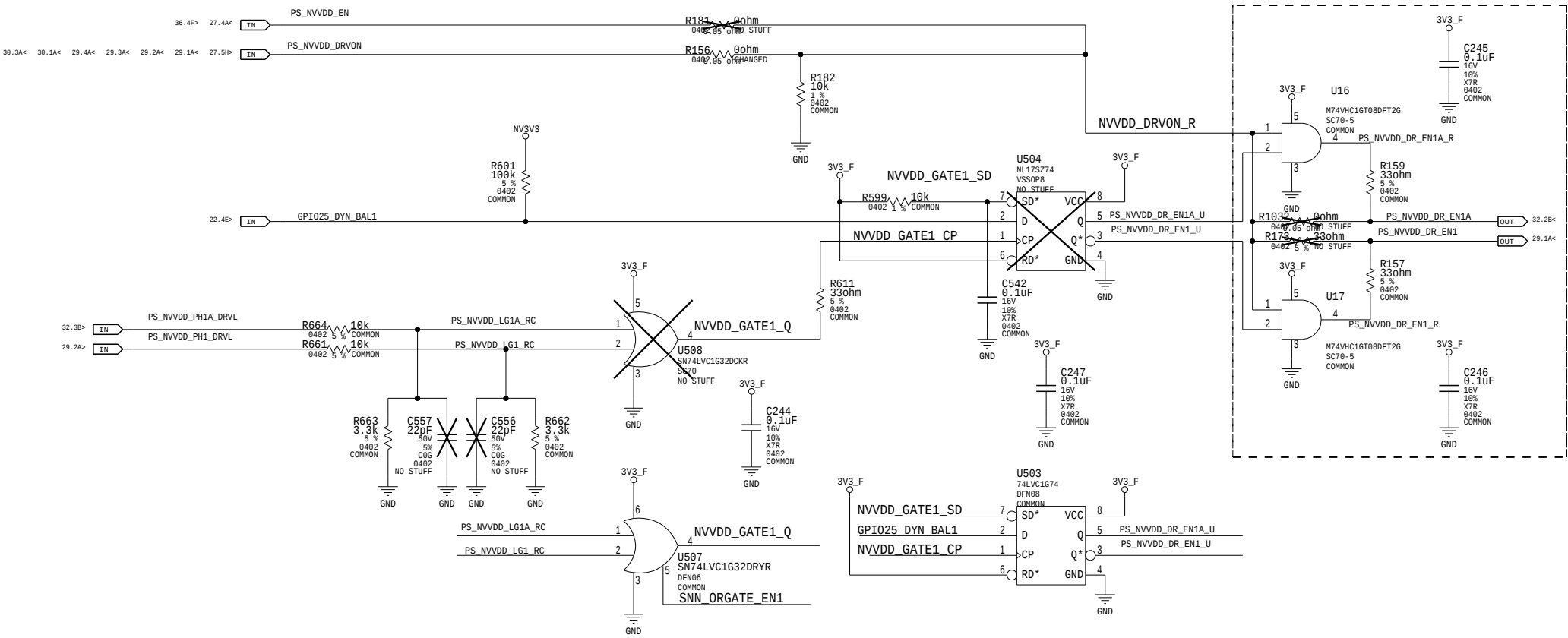
Page32: PS: Dynamic Power Balance Phases



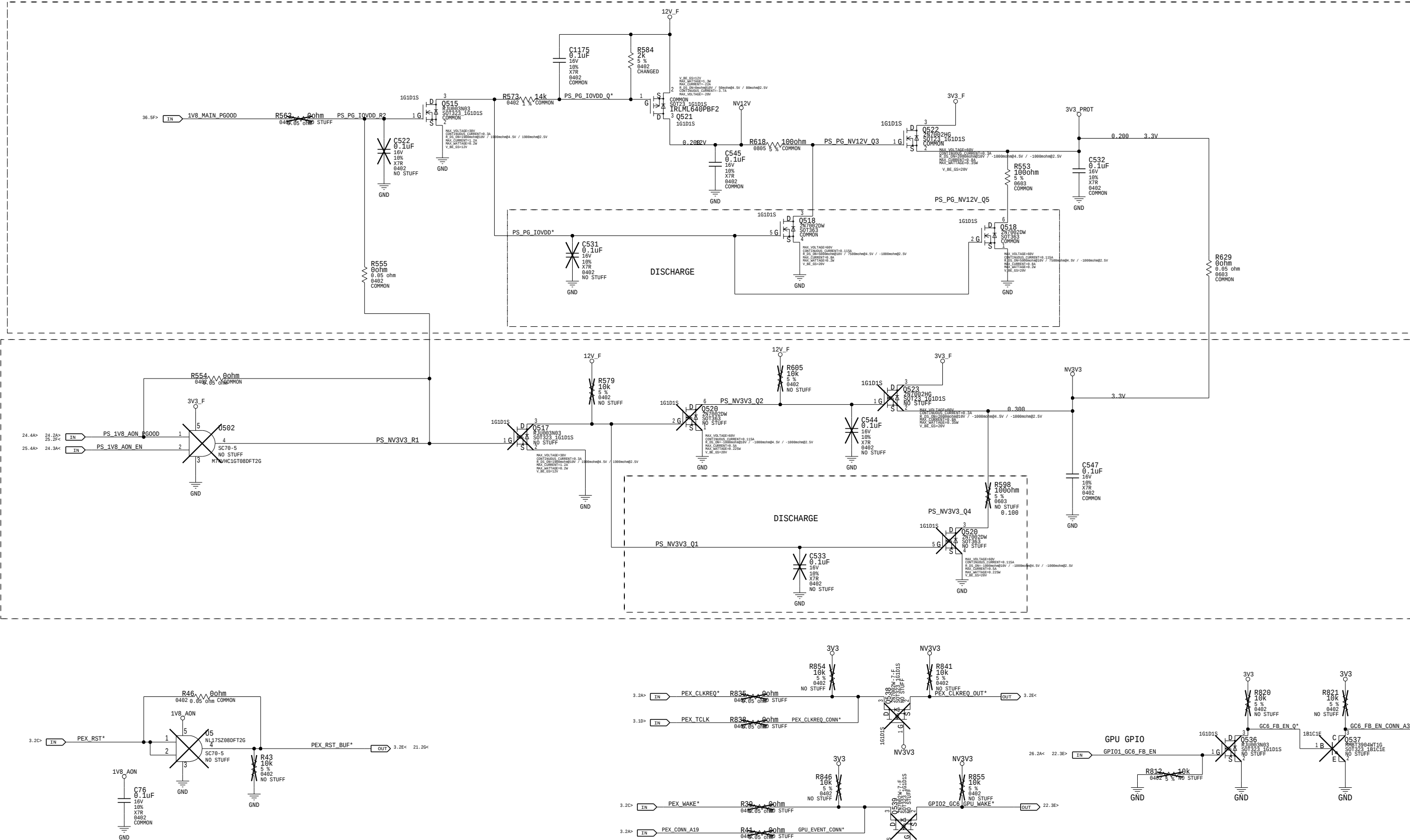
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Page33: PS: Dynamic Power Balance Logic



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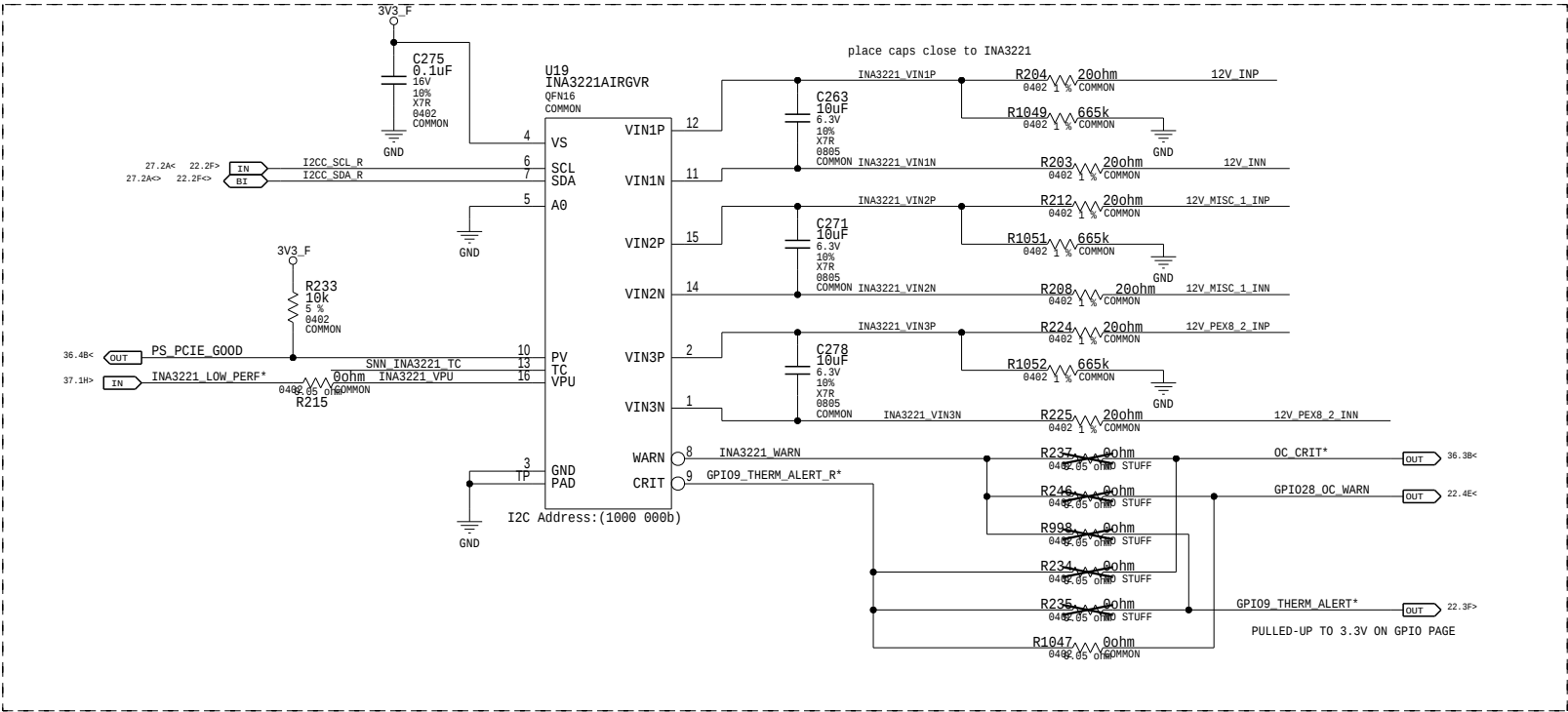
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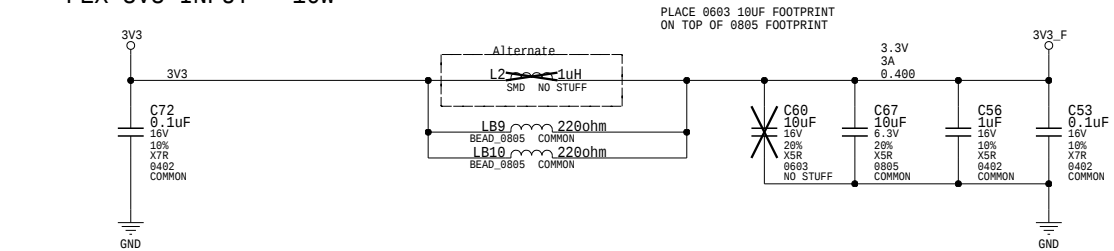
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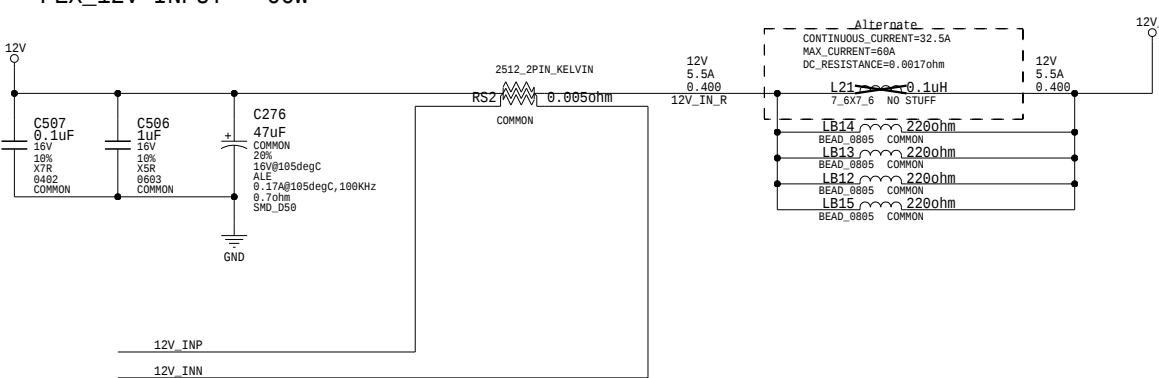
Page35: PS: Inputs, Filtering, and Monitoring



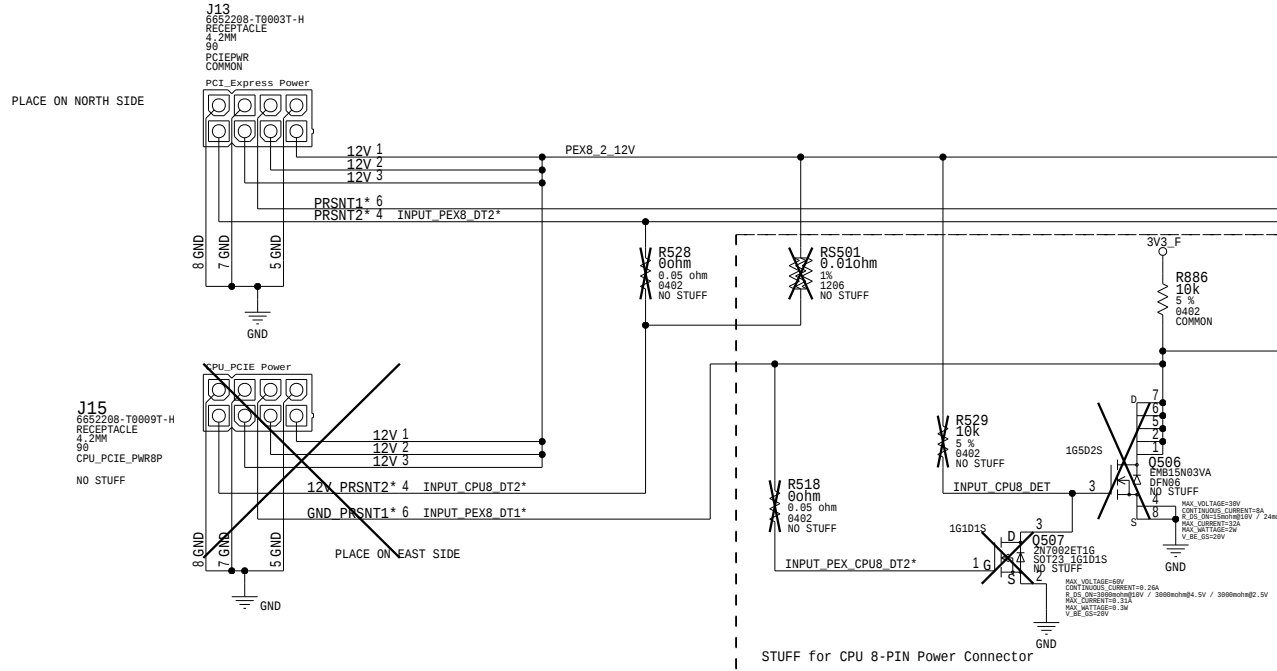
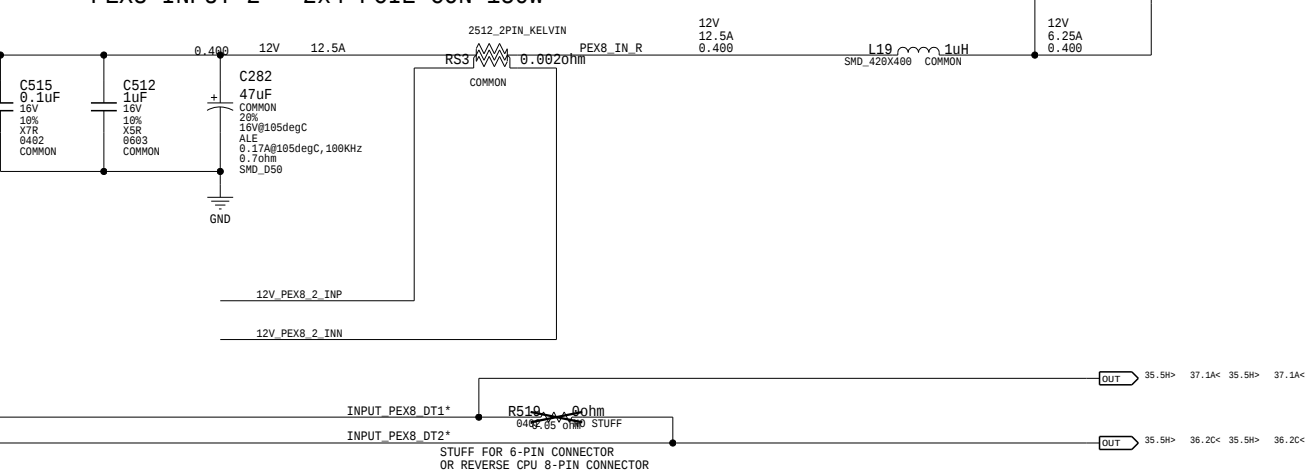
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



PEX8 INPUT 2 - 2x4 PCIE CON 150W



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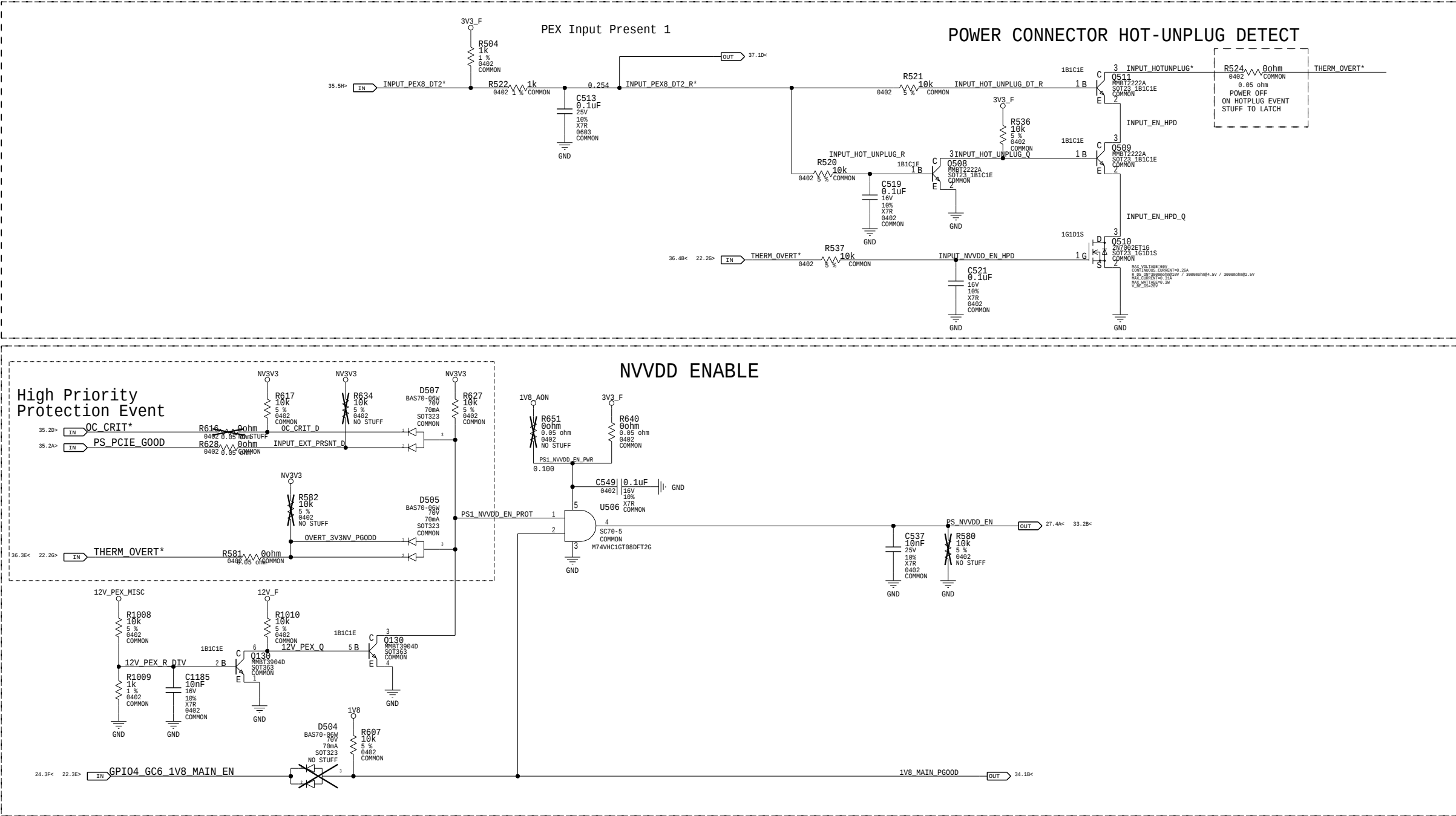
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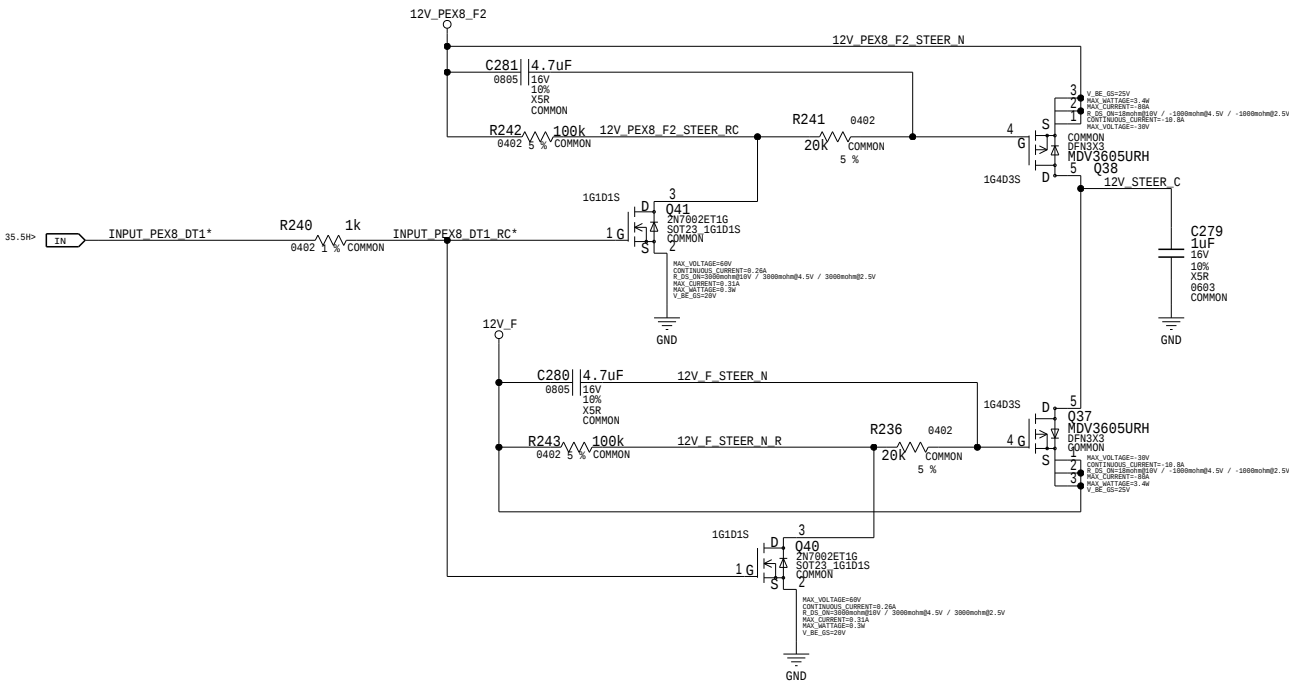
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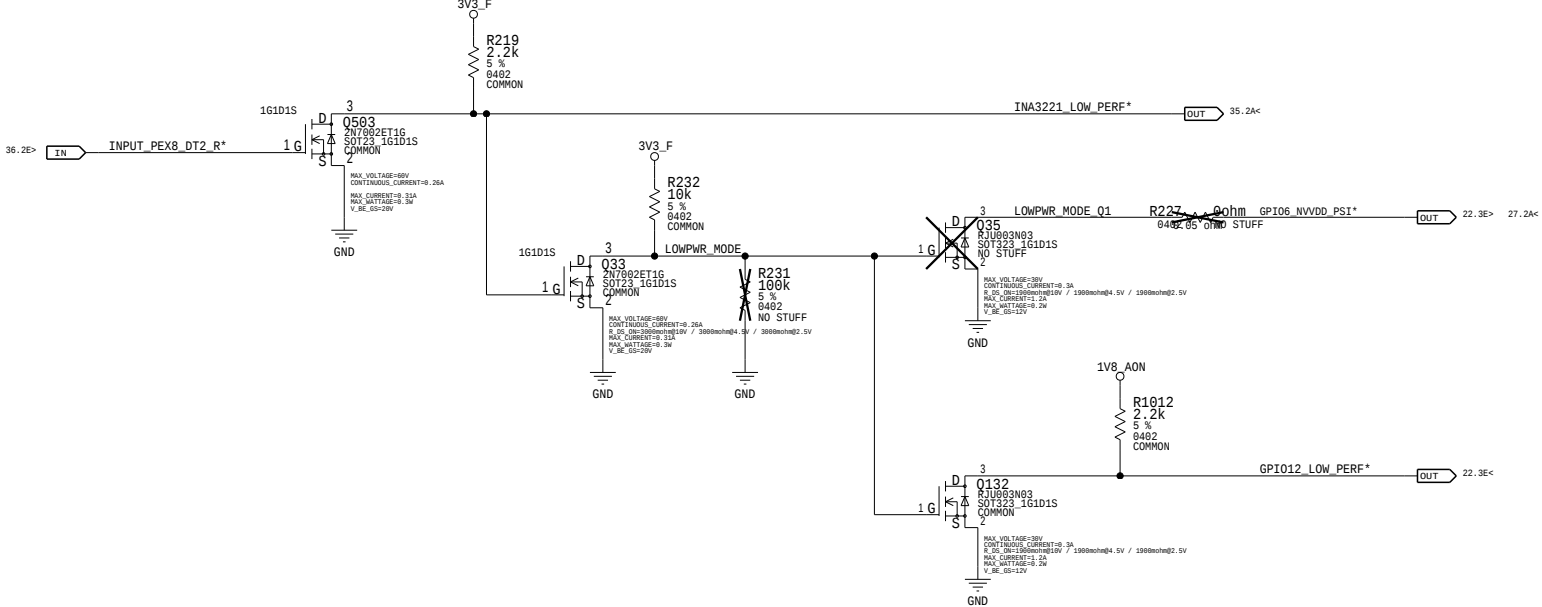
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PEX Input - 12V Current Steering FETs

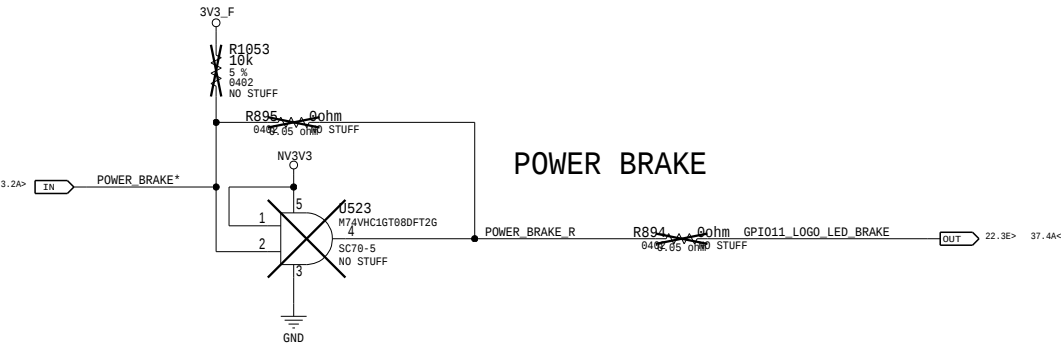


PEX Input - Power Level/PSI* Control



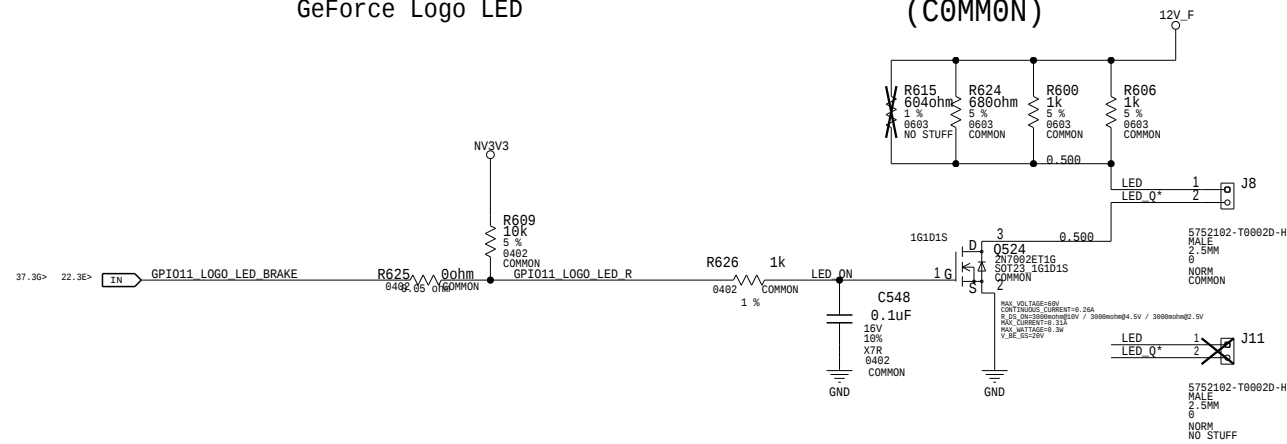
GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

POWER BRAKE

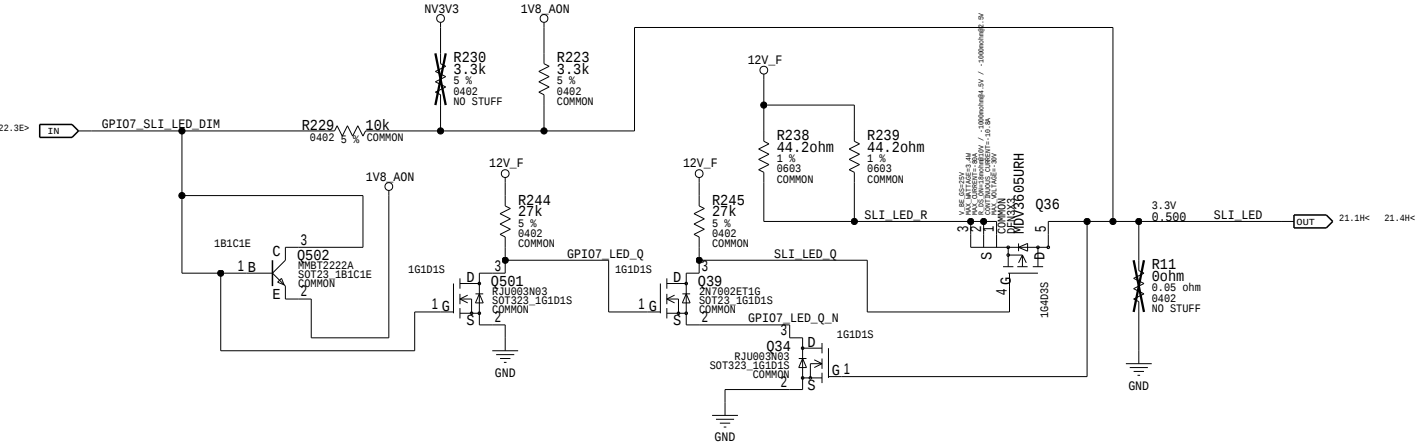


GeForce Logo LED

LED HEADER (COMMON)



SLI LED (GEFORCE ONLY)



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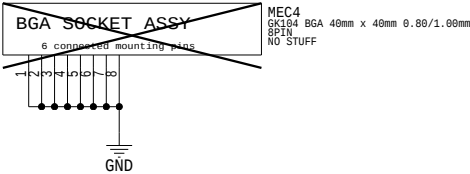
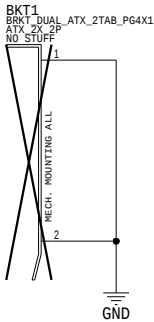


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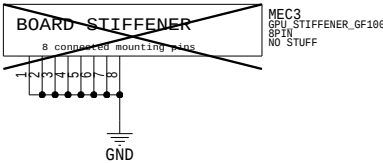
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Mechanical Holes Symbol

