PG411 A01

GP104 - 8GB GDDR5, 256b, 256Mx32
Tall DVI-D + DP + DP + HDMI + DP

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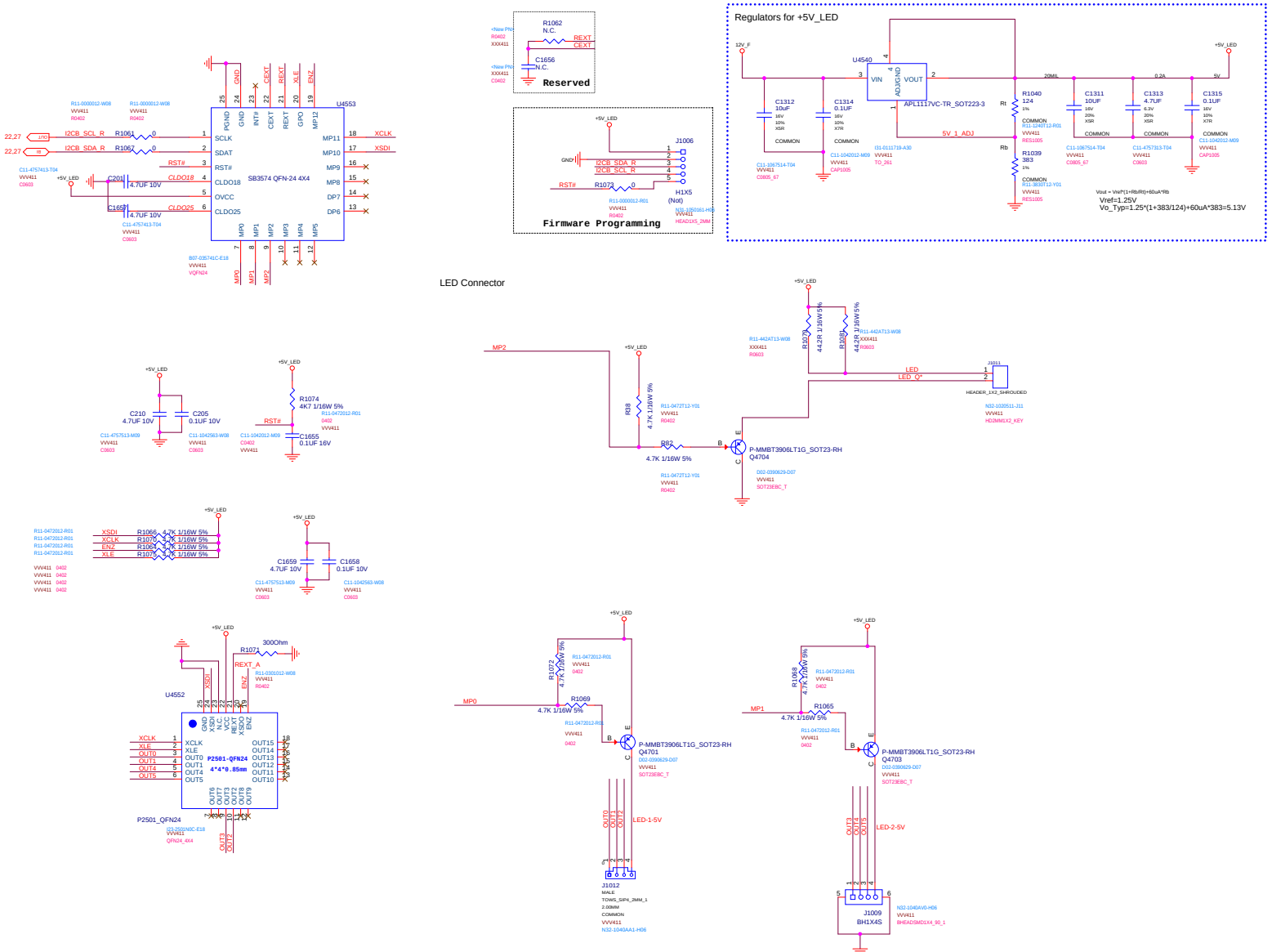

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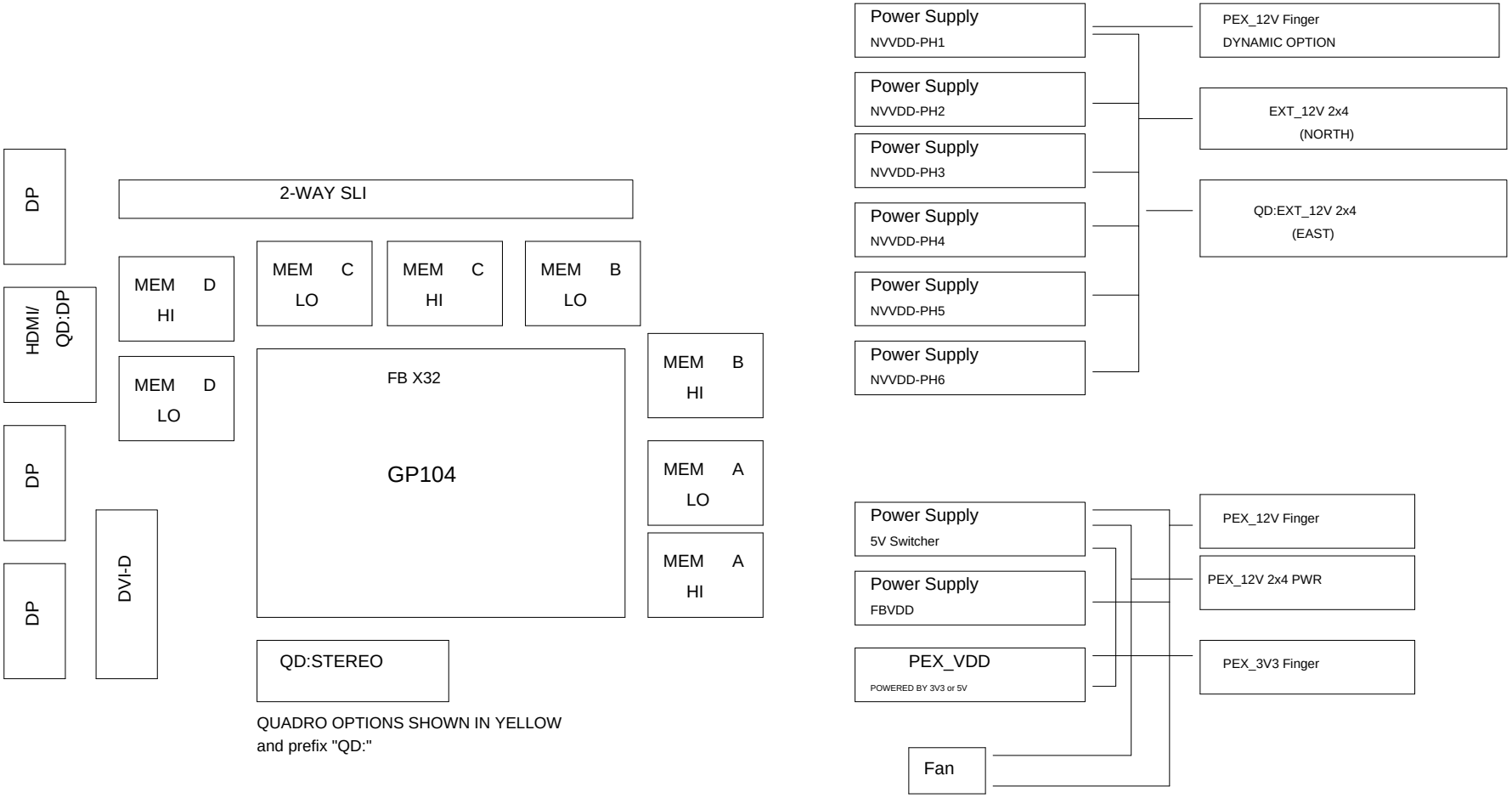
Page2: Block Diagram



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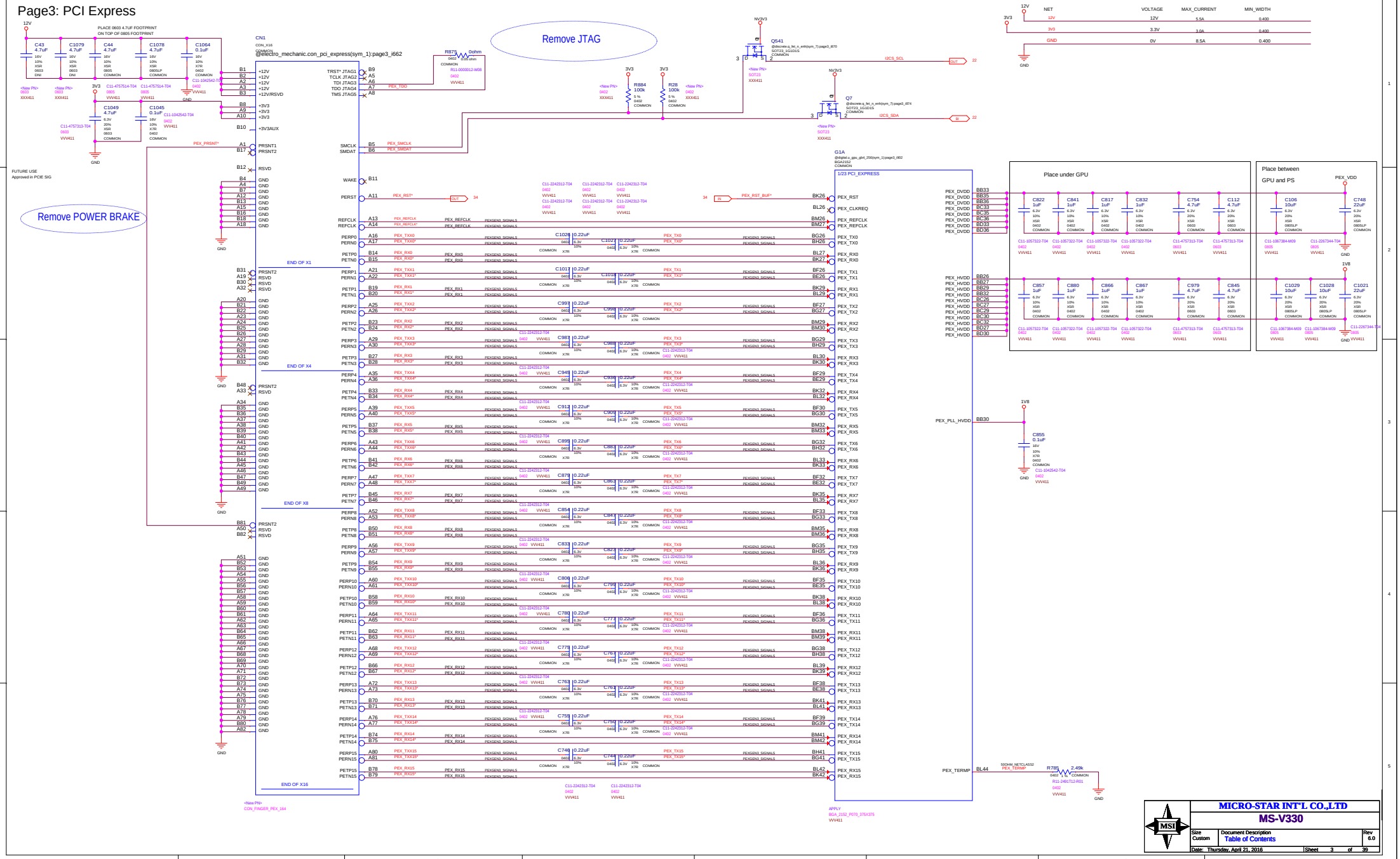
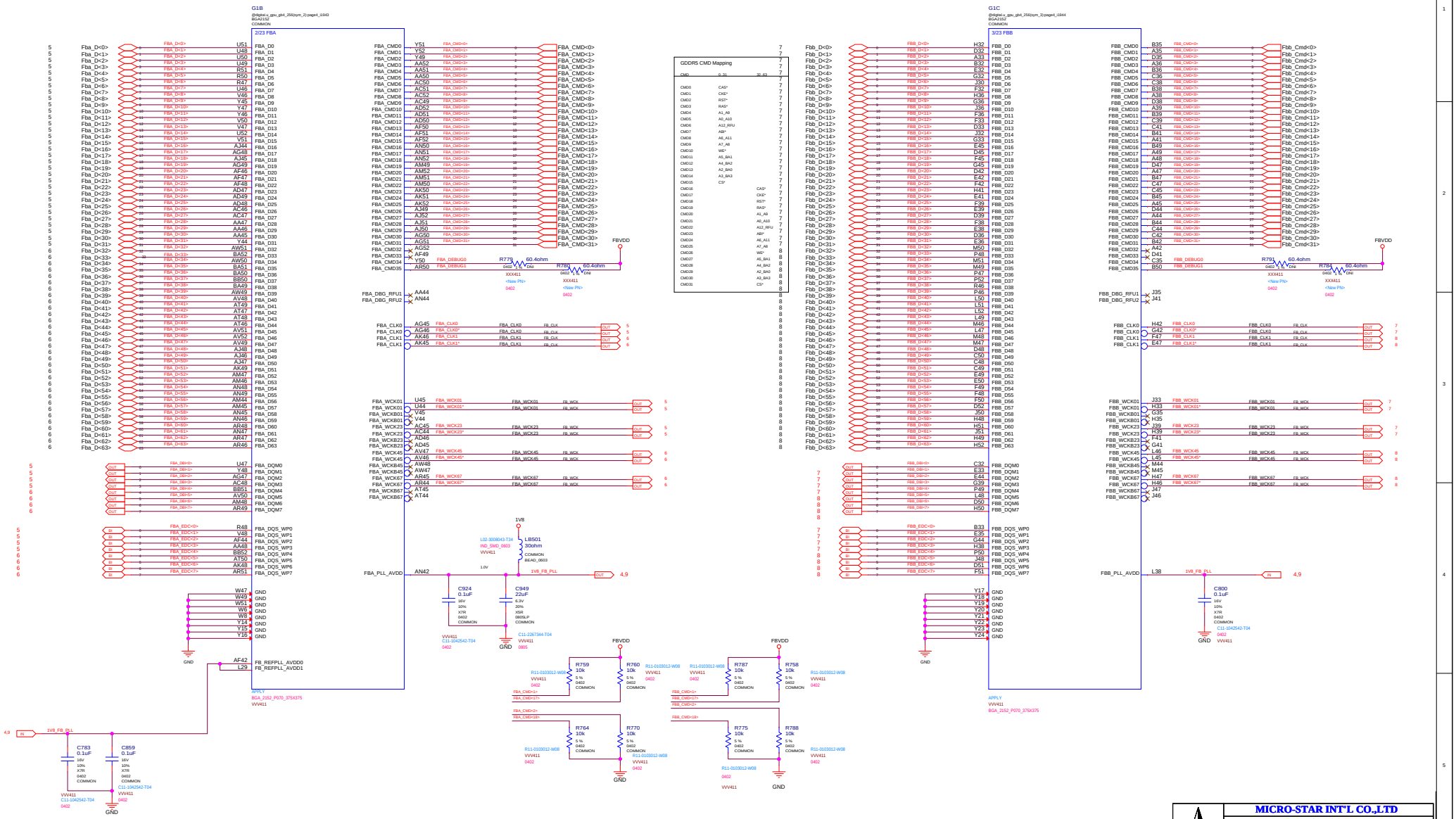
Page3: PCI Express



Page4: MEMORY: GPU Partition A/B



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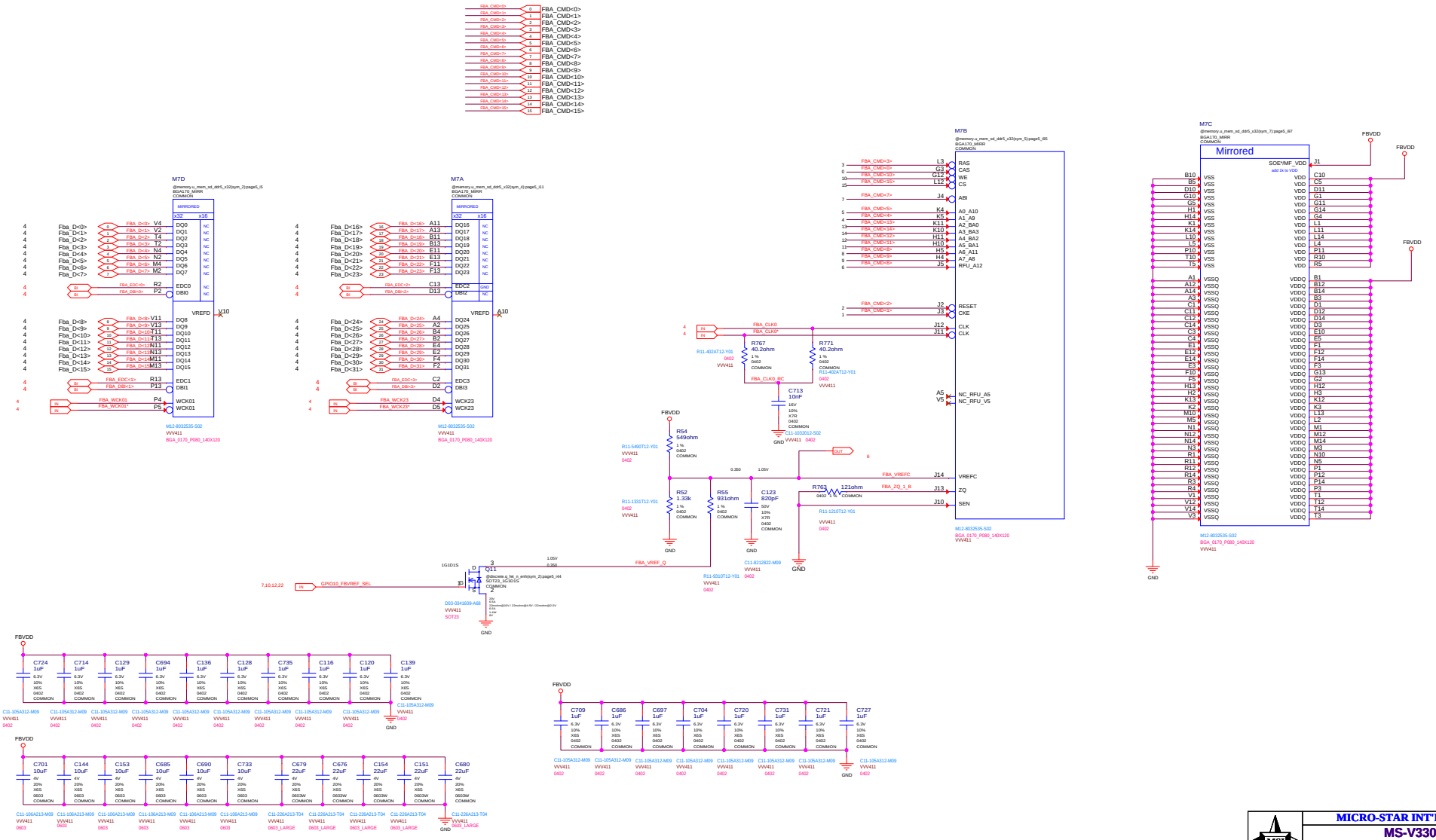
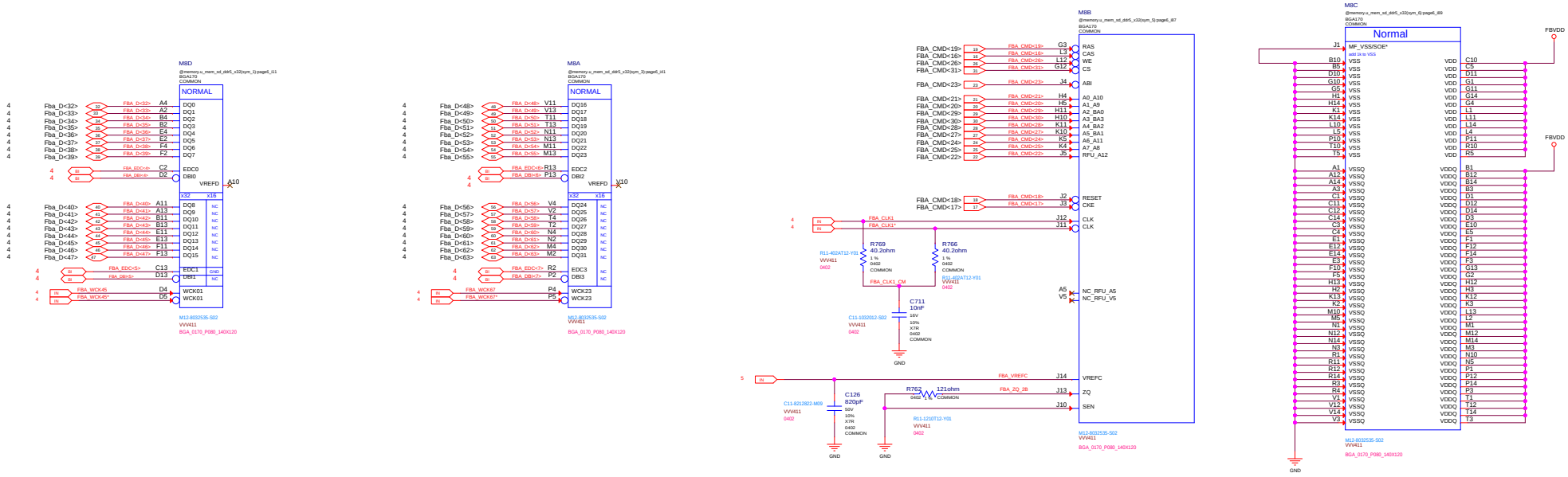
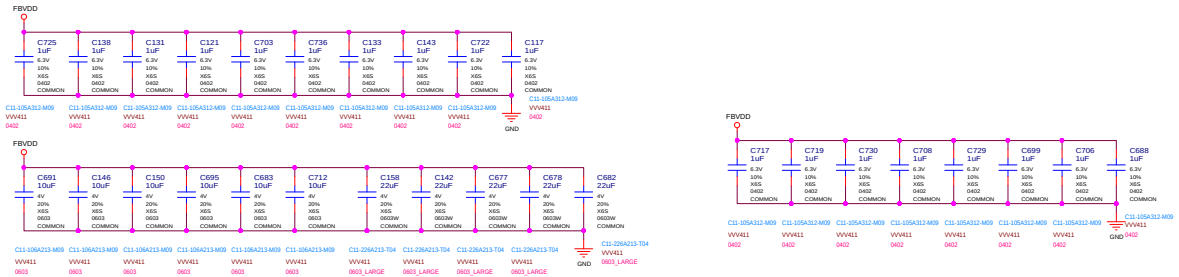
Page5: MEMORY: FBA Partition 31..0



Page6: MEMORY: FBA Partition 63..32





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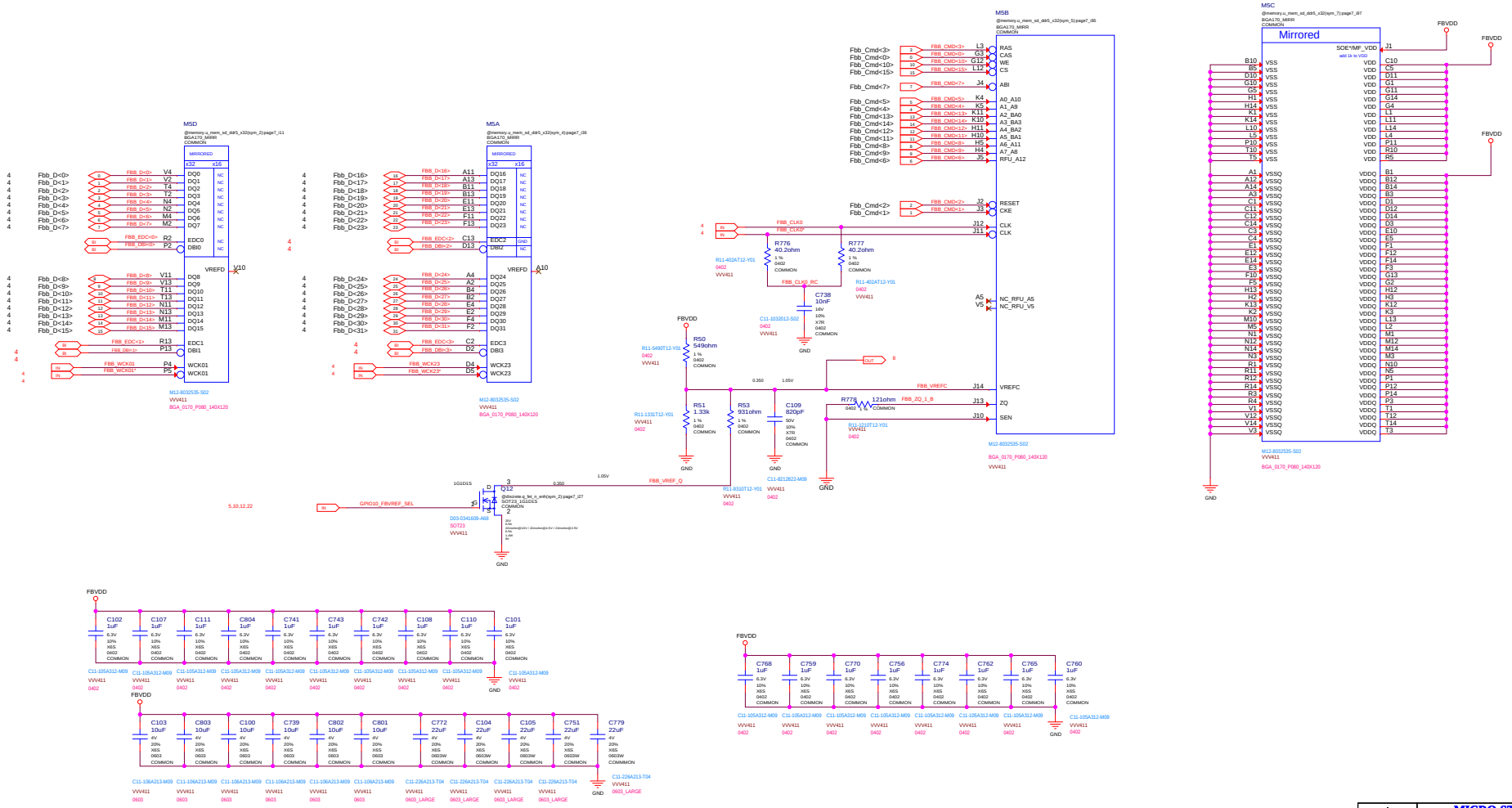
Page7: MEMORY: FBB Partition 31..0



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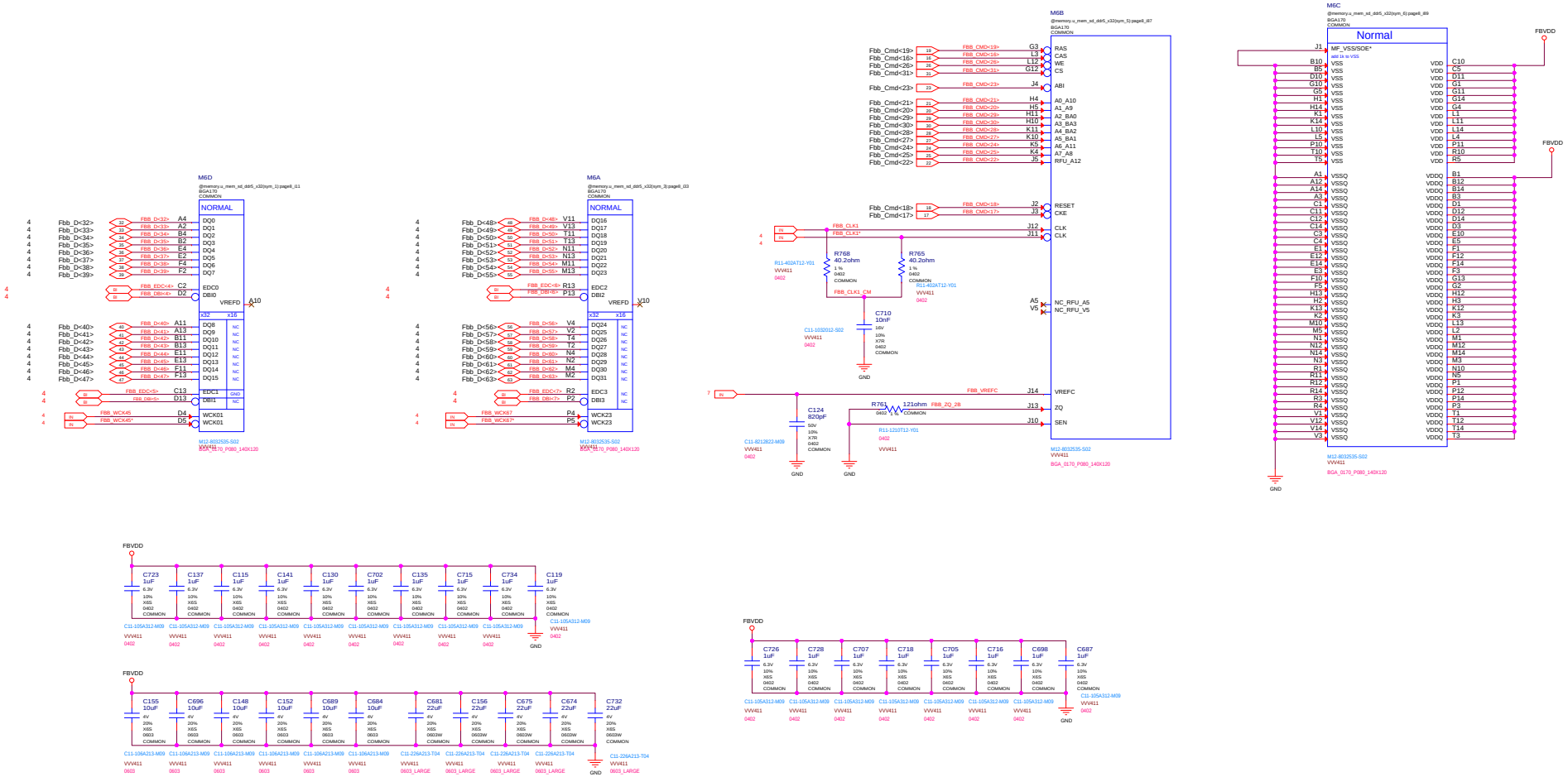
Page8: MEMORY: FBB Partition 63..32



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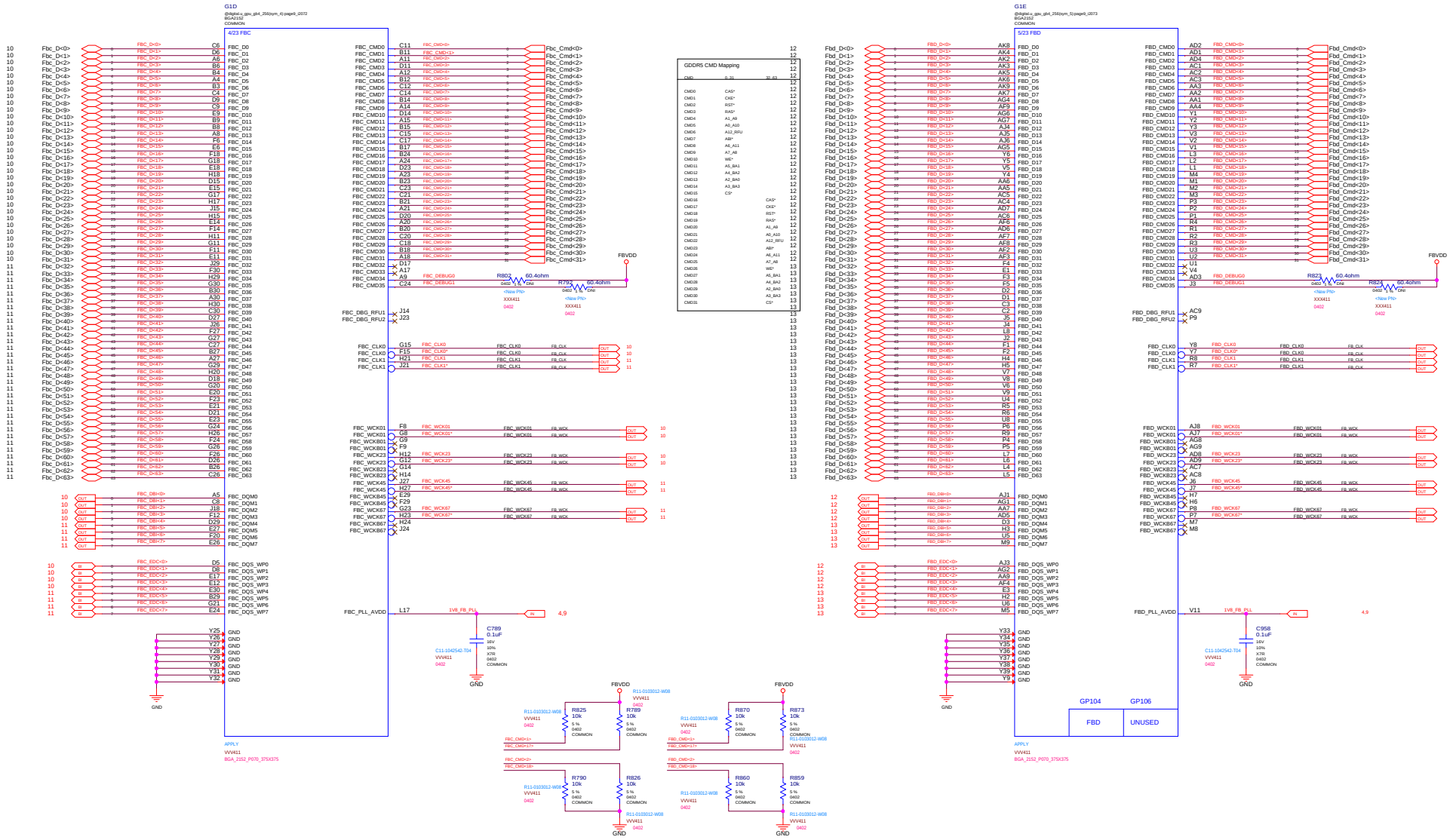
Page9: MEMORY: GPU Partition C/D



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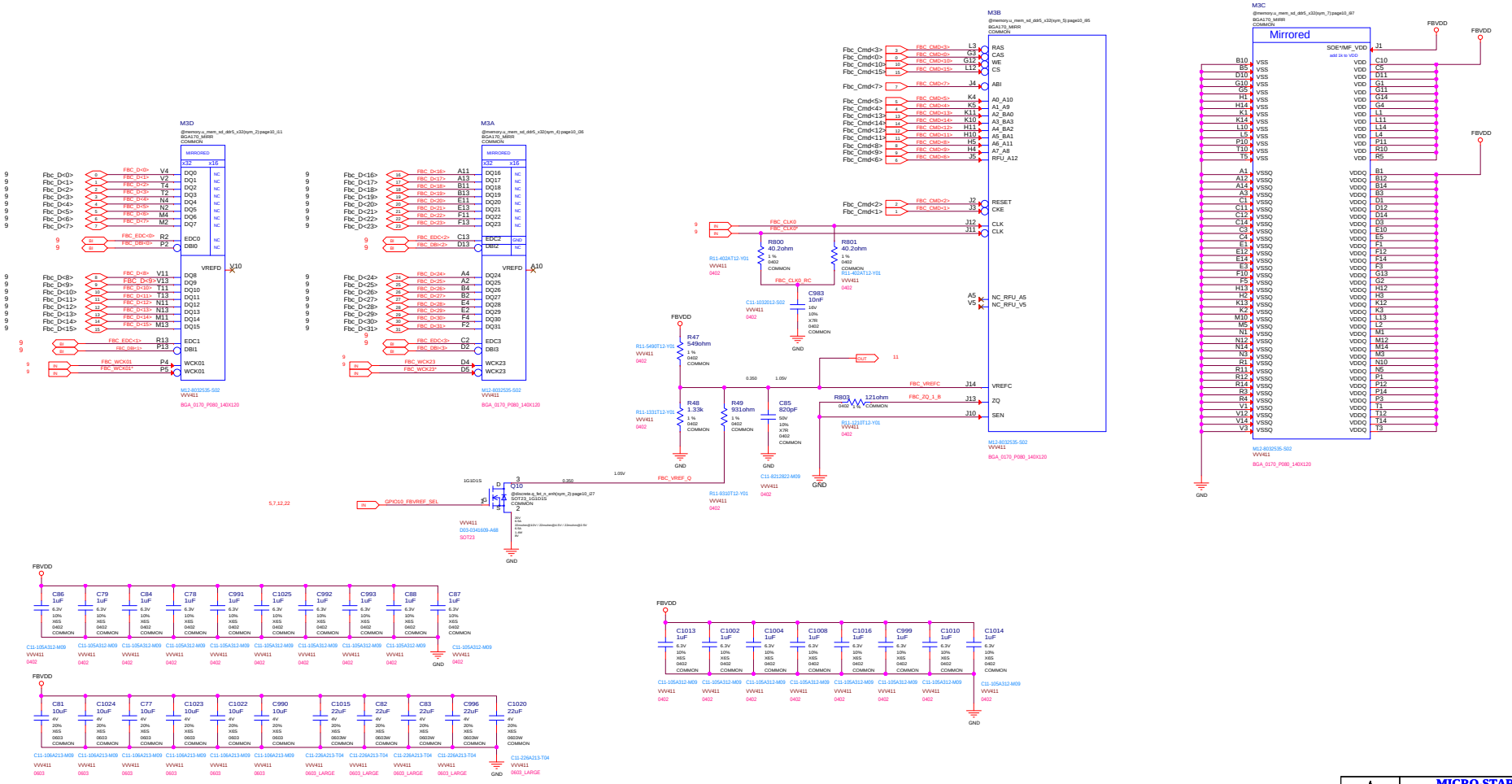
Page10: MEMORY: FBC Partition 31..0



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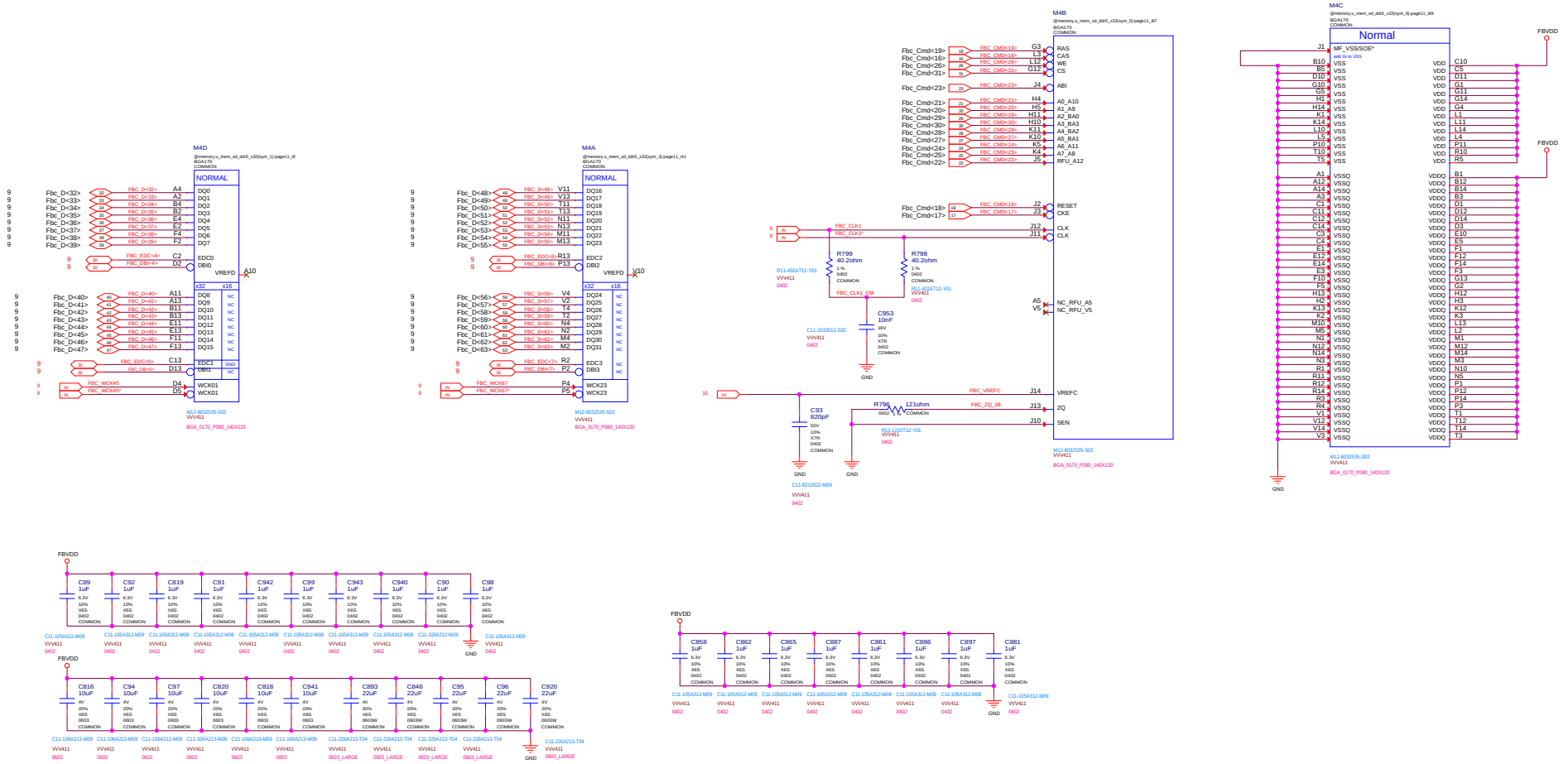
Page11: MEMORY: FBC Partition 63..32



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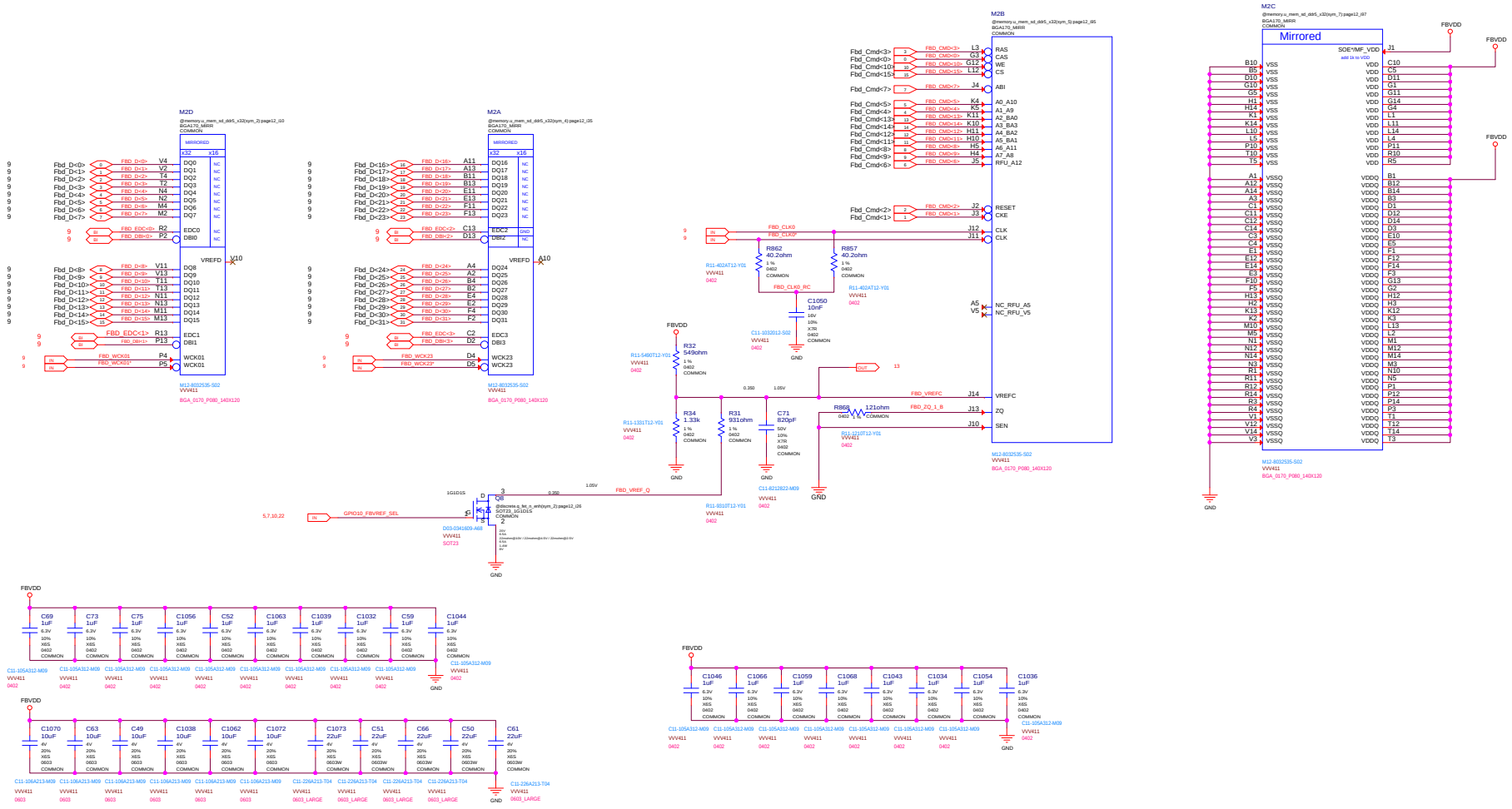
Page12: MEMORY: FBD Partition 31..0



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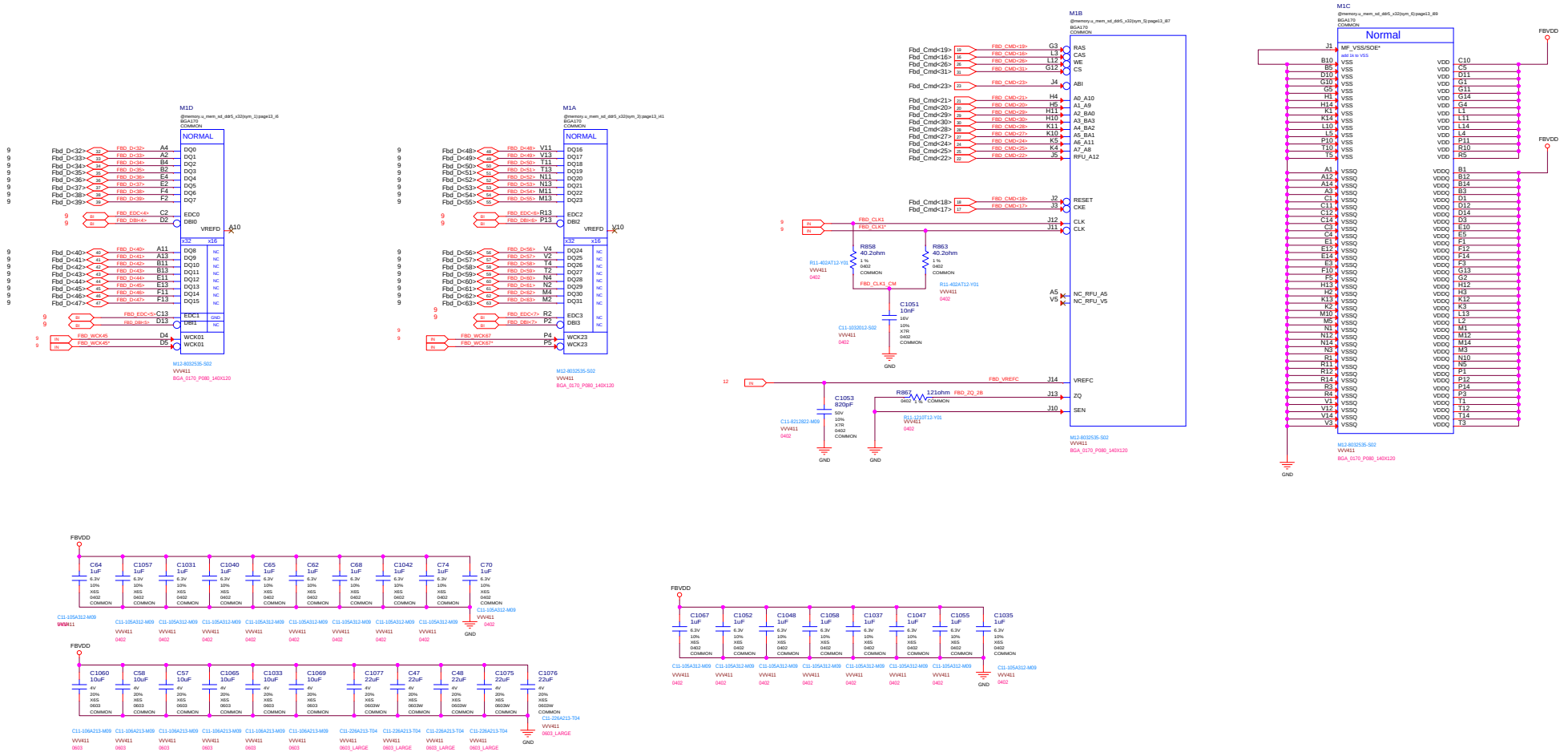
Page13: MEMORY: FBD Partition 63..32



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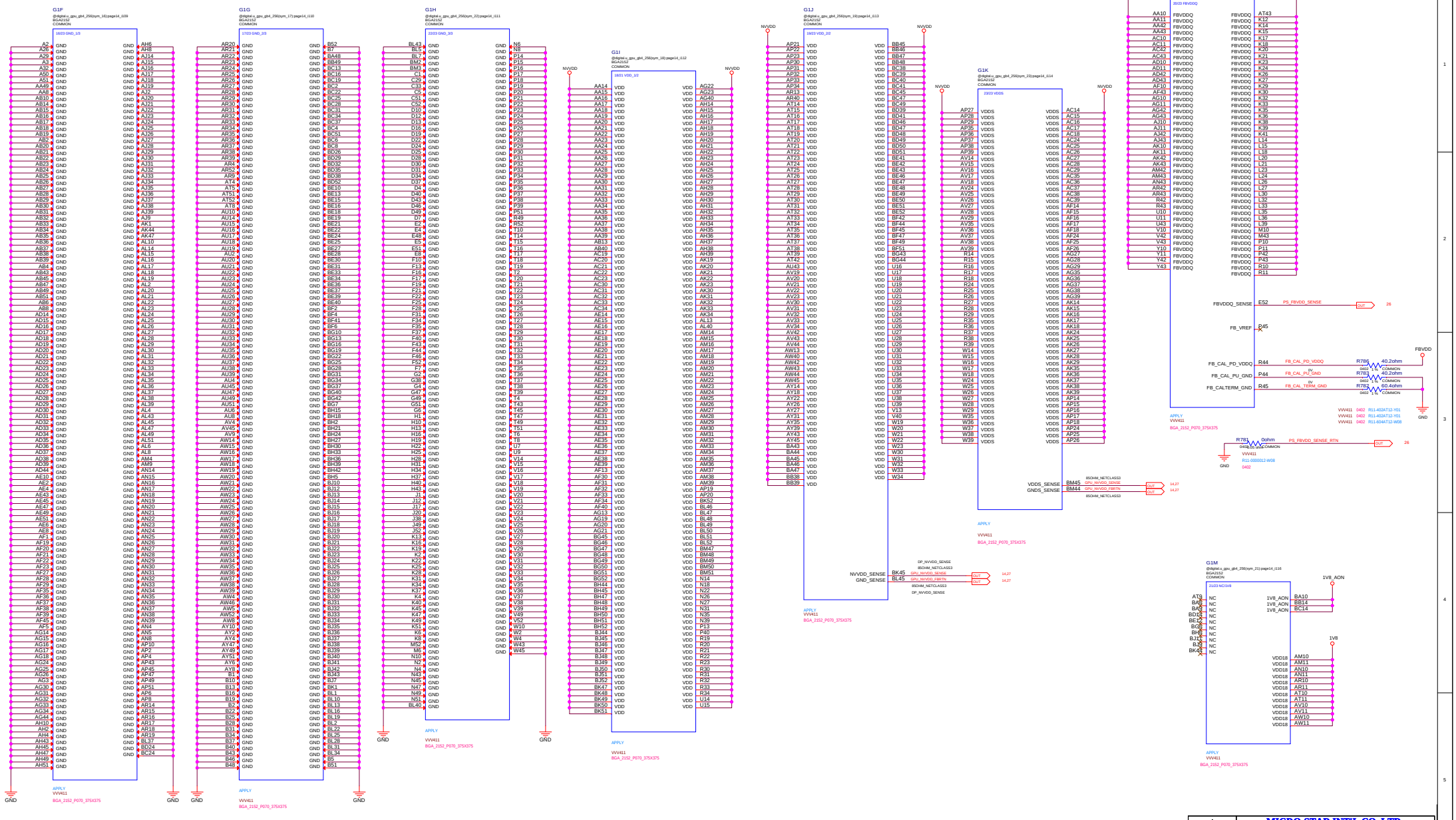
Page14: GPU PWR and GND



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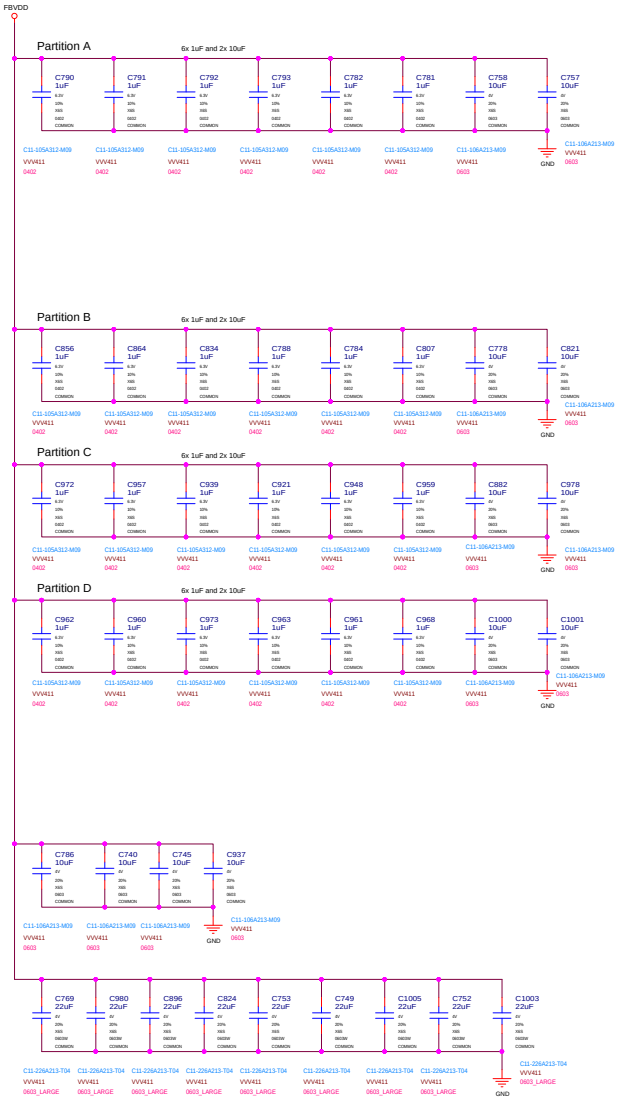
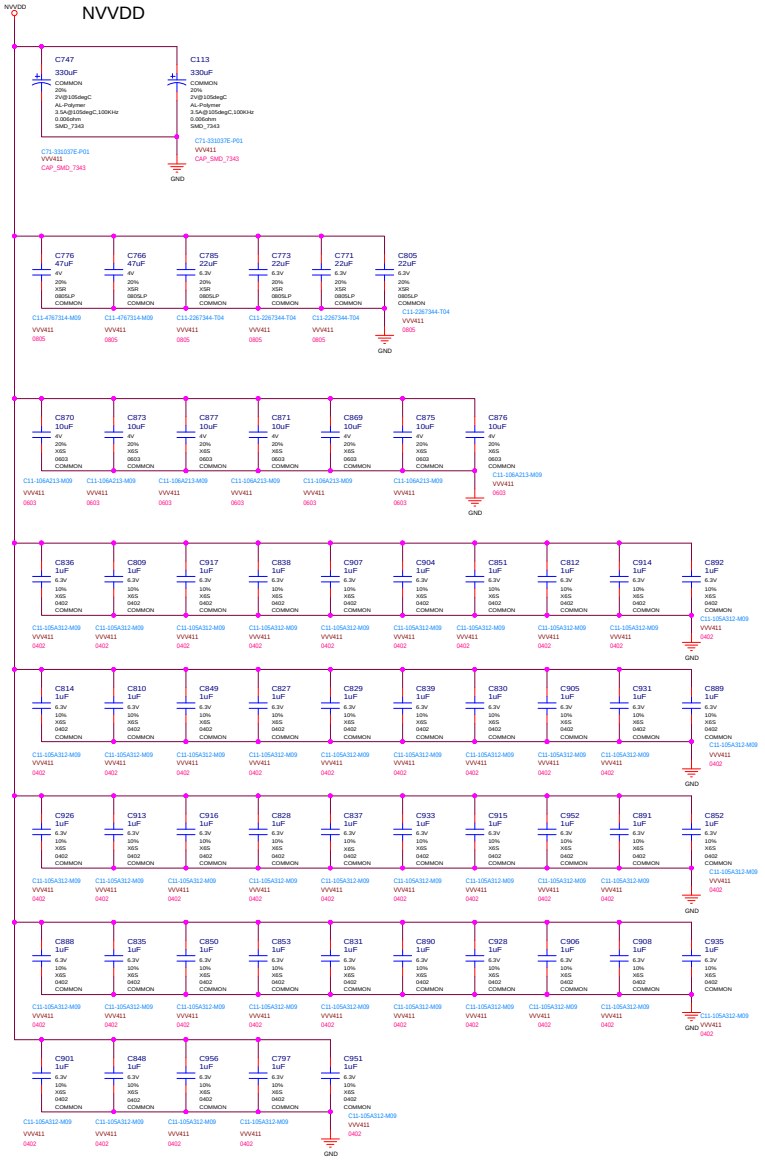
Page15: GPU Decoupling

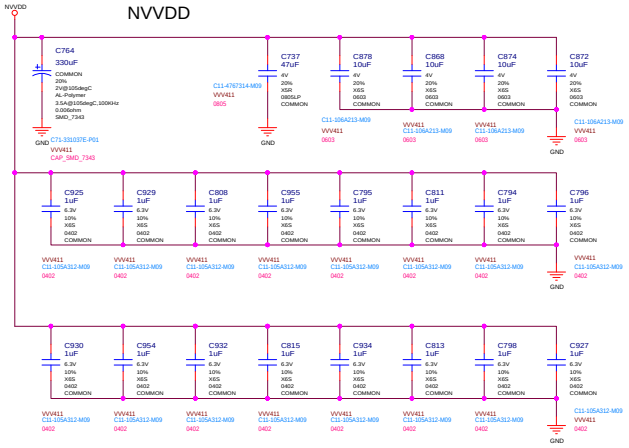
FBVDD

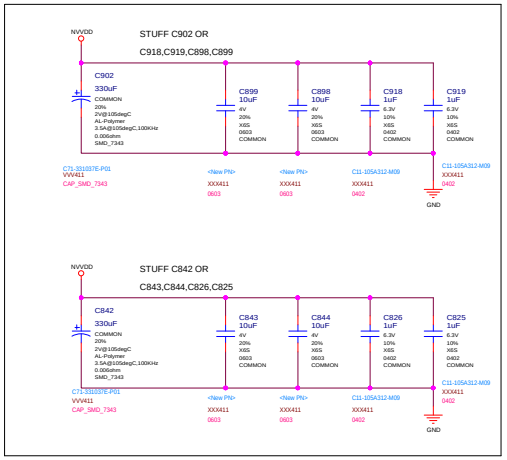


NVVDD

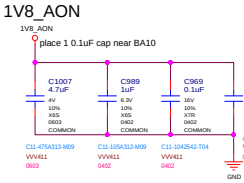


NVVDD



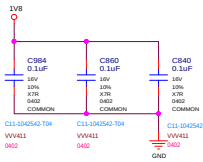


1V8_AON



place 1 0.1uf cap for BB14 and BC14 to share

VDD18



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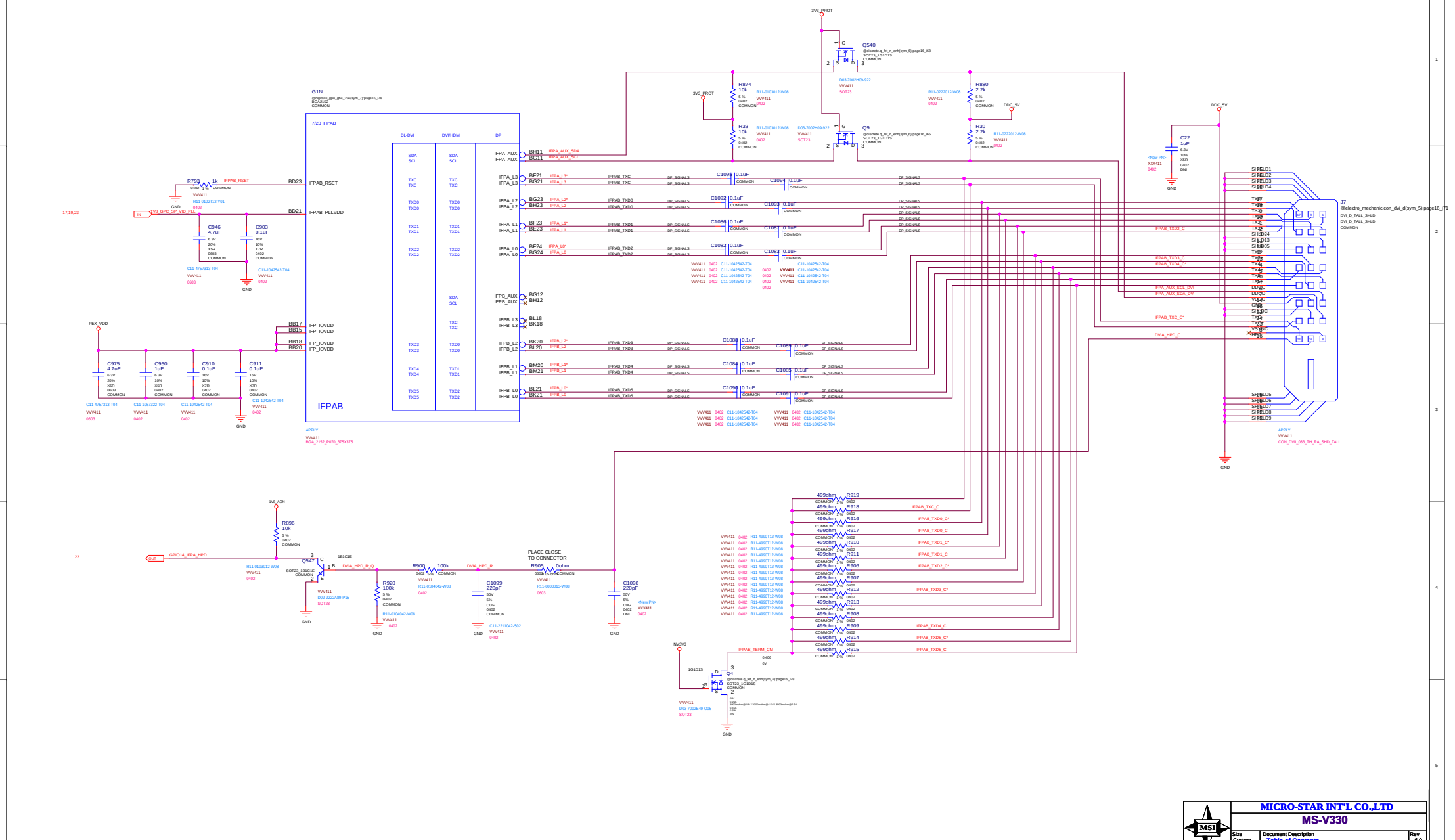
Page16: IFPAB DVI-D-DL



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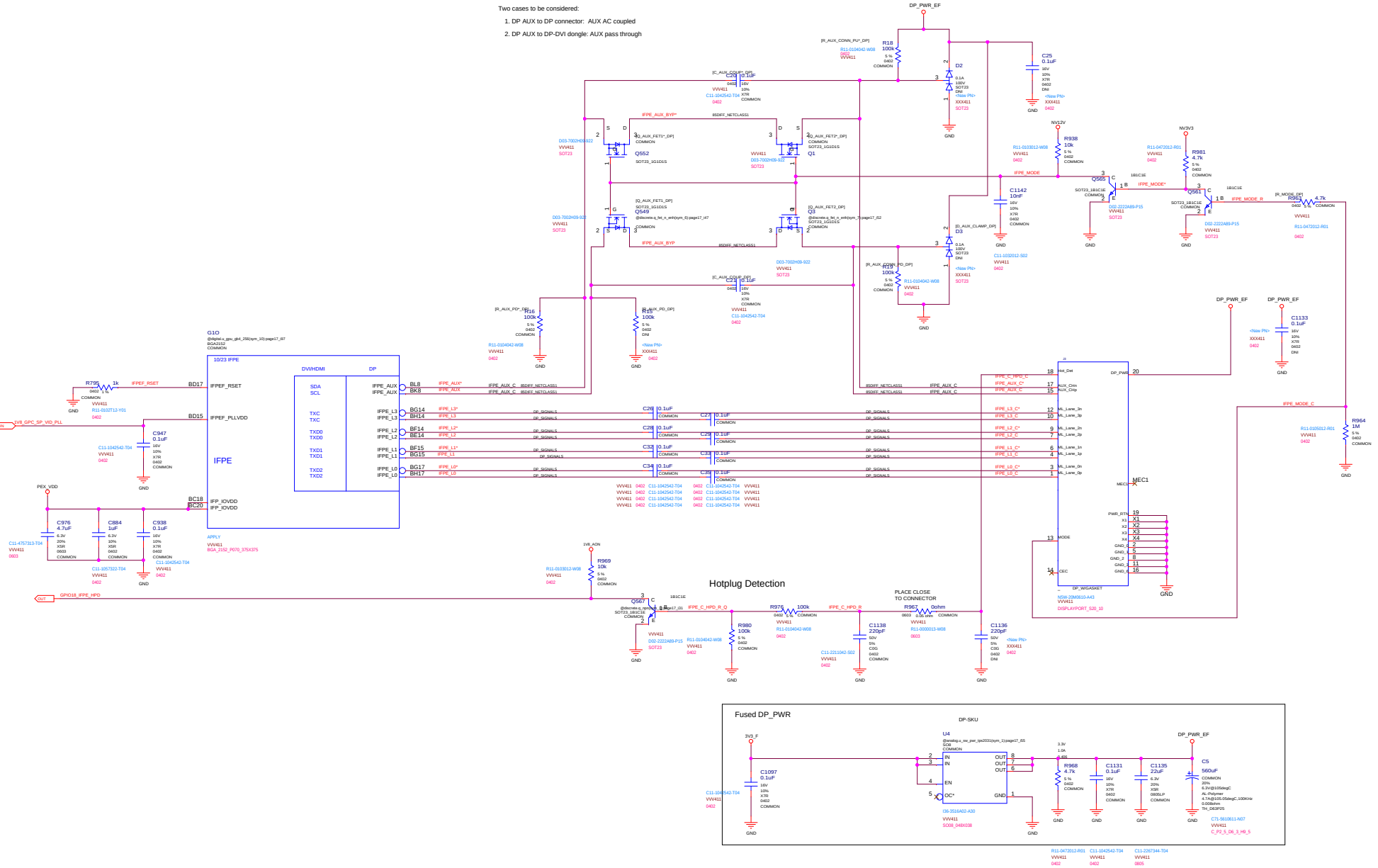
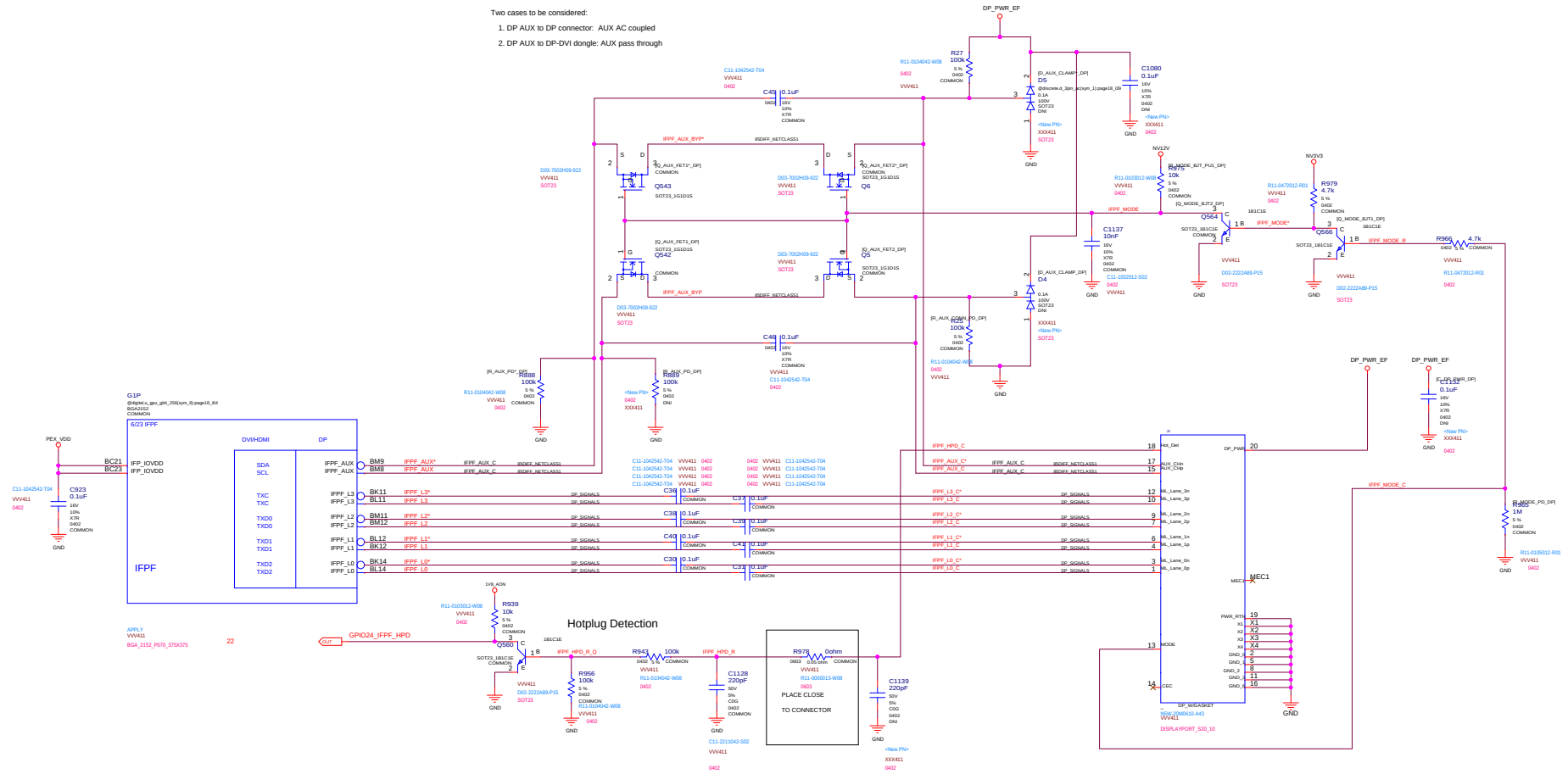
Page17: IFPE DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



Page18: IFPF DP



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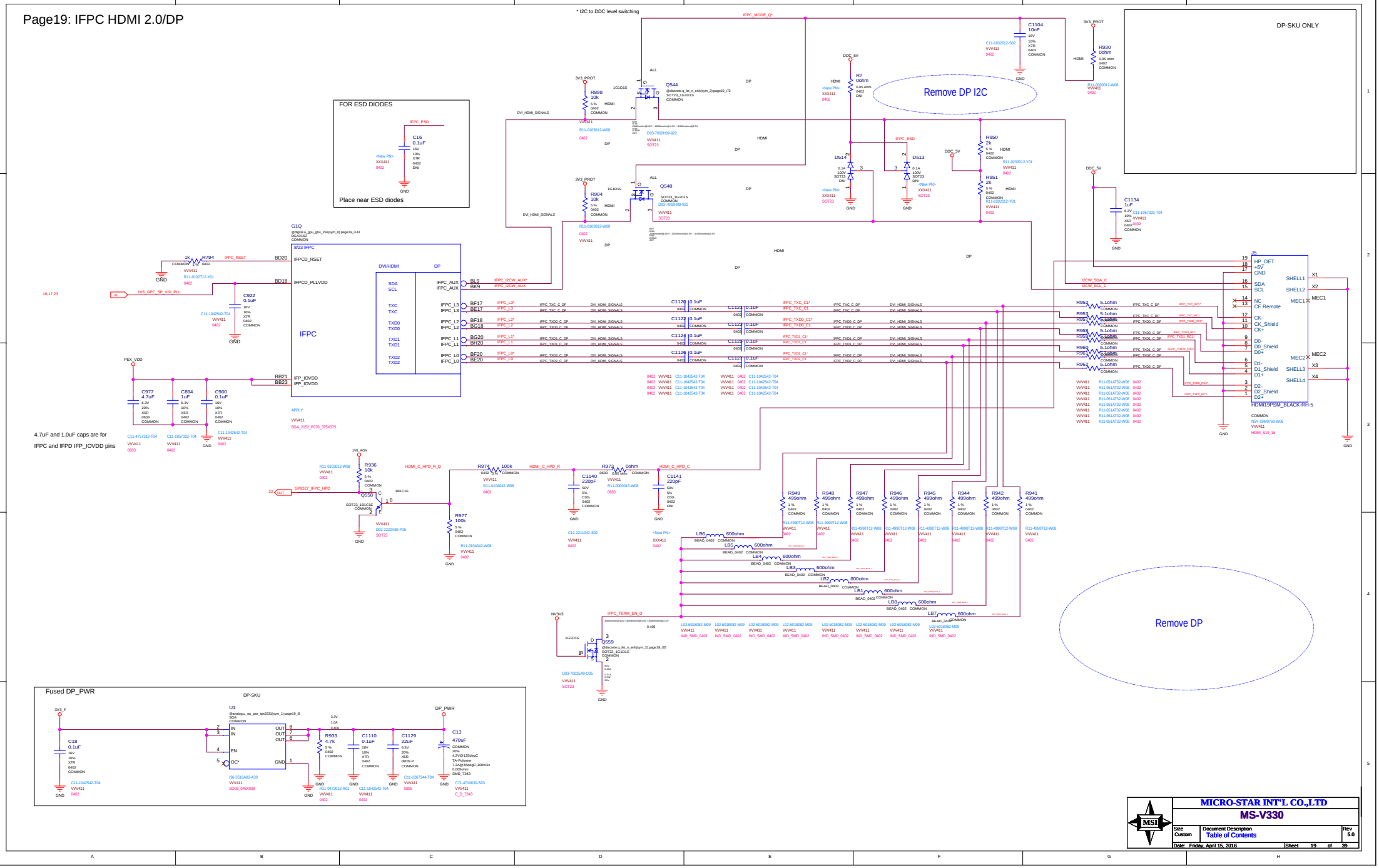
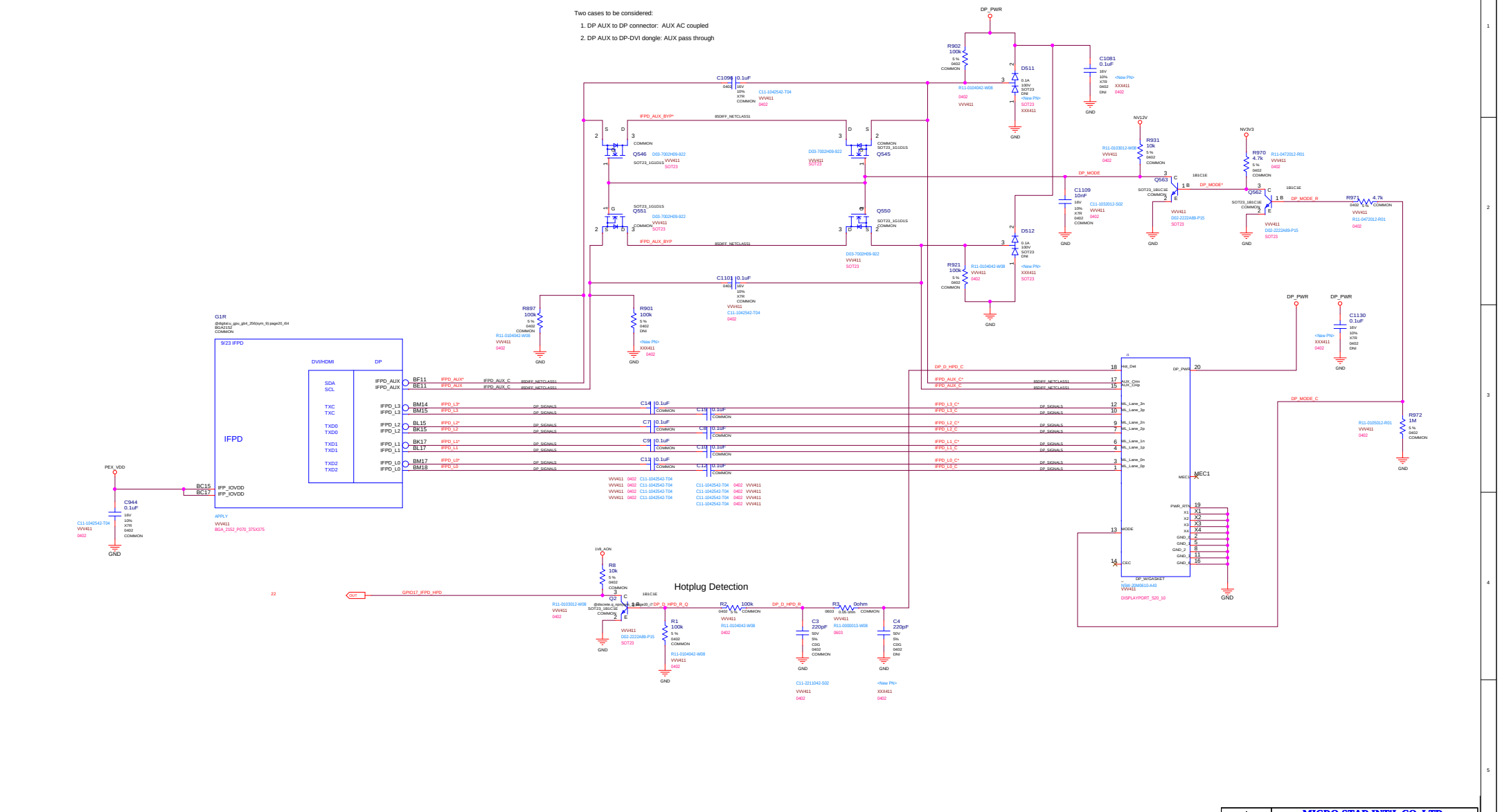
Page19: IFPC HDMI 2.0/DP



Page20: IFPD DP



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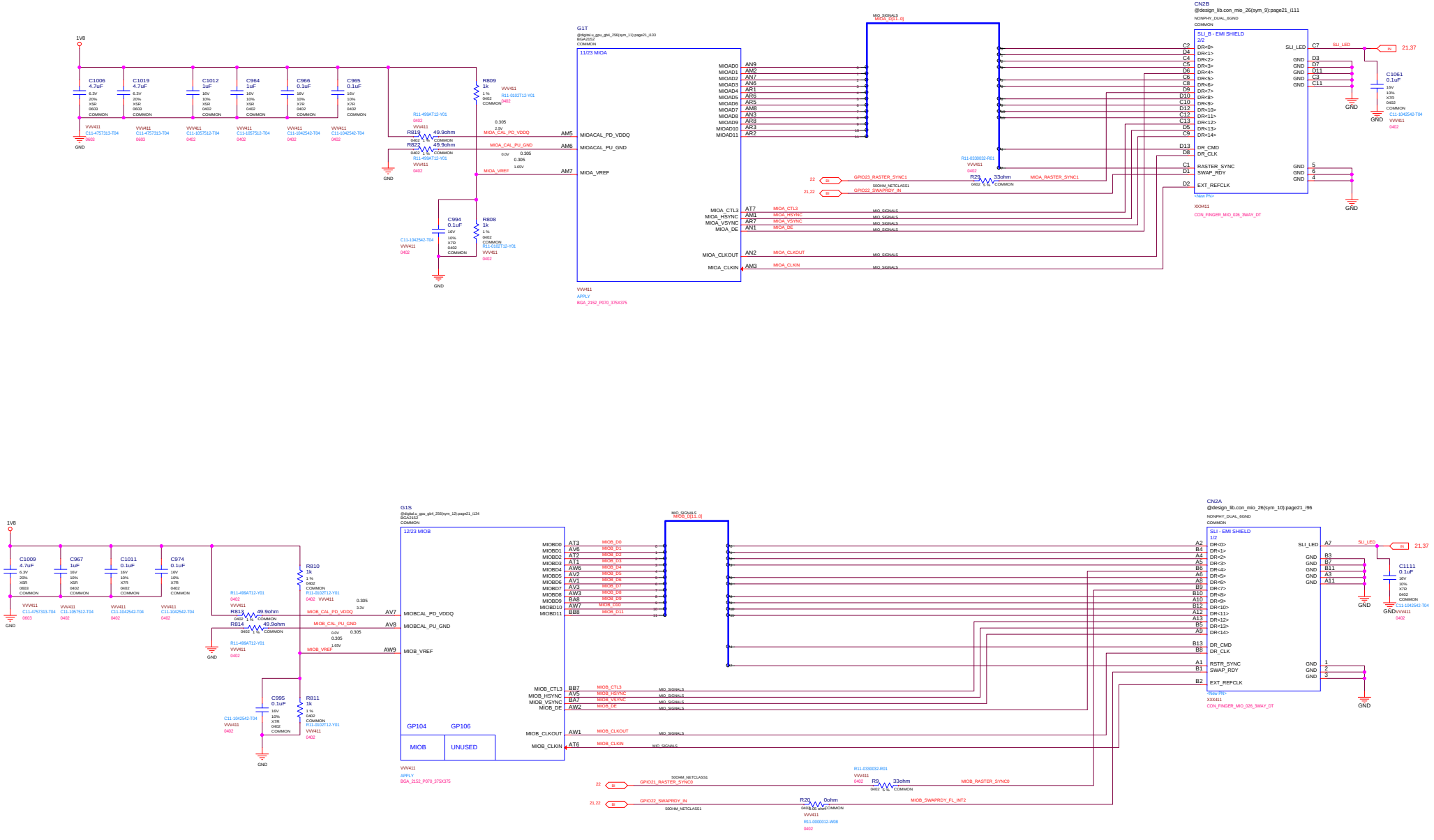
Page21: MIOA/B Interface and FRAME LOCK



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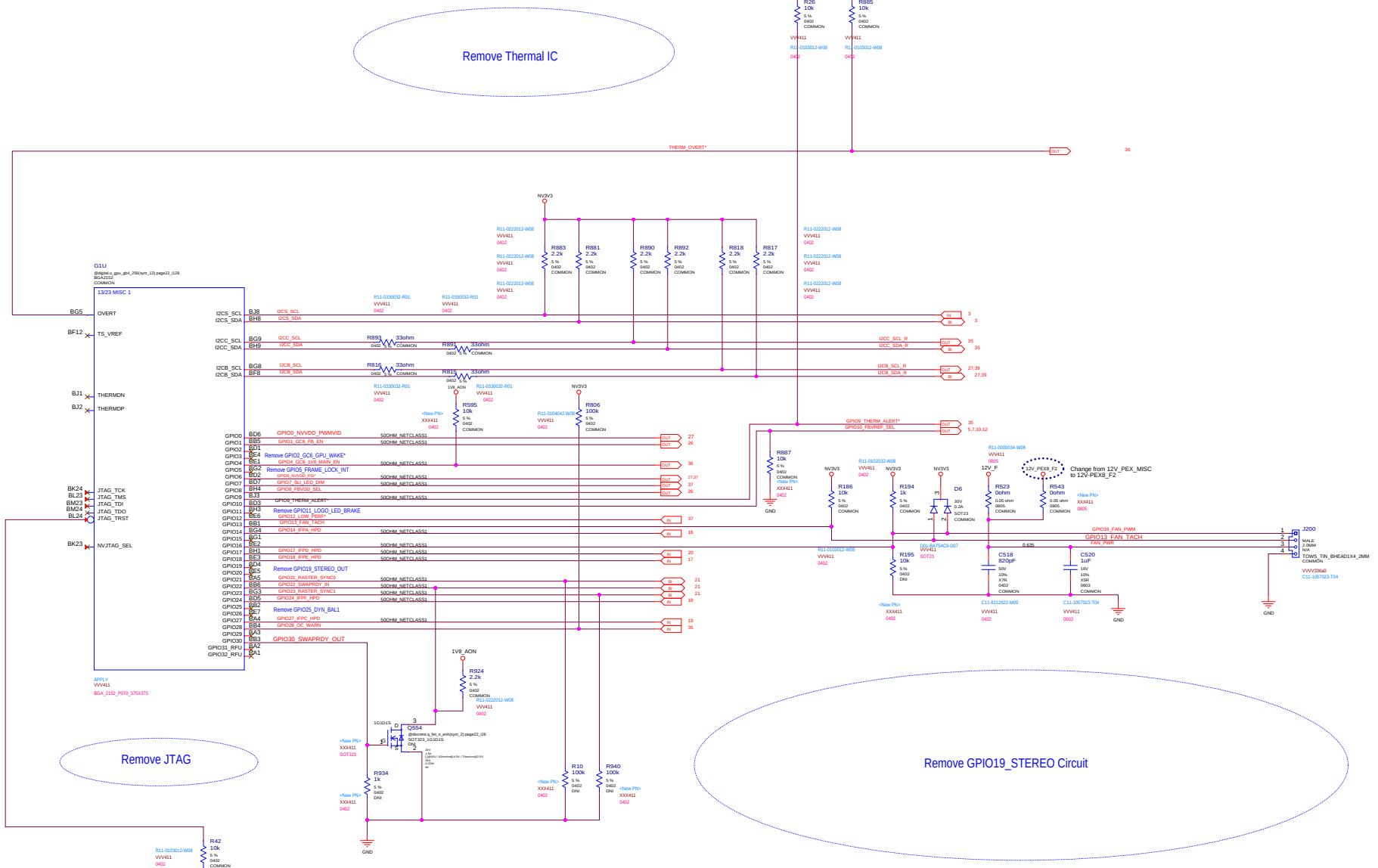
Page22: MISC1: Fan, Thermal, JTAG, GPIO, STEREO



Page23: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

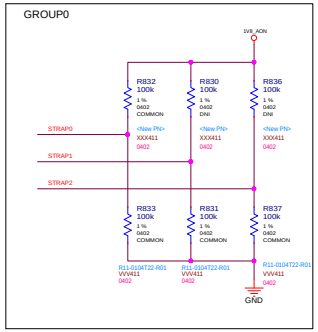
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

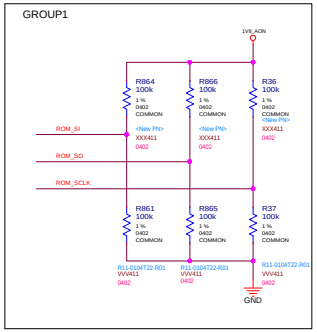
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

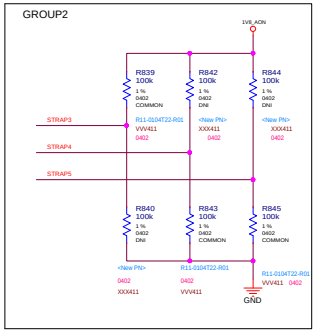
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

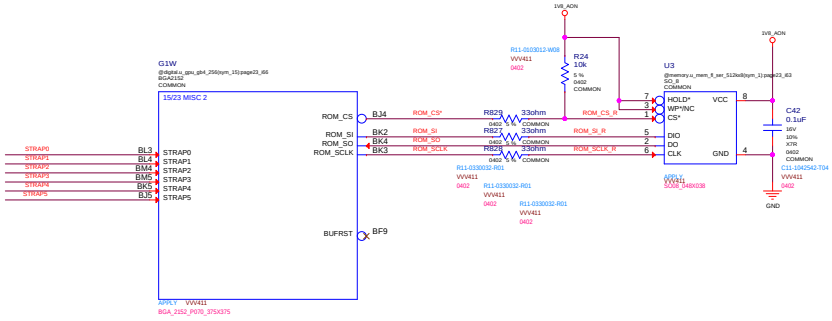
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

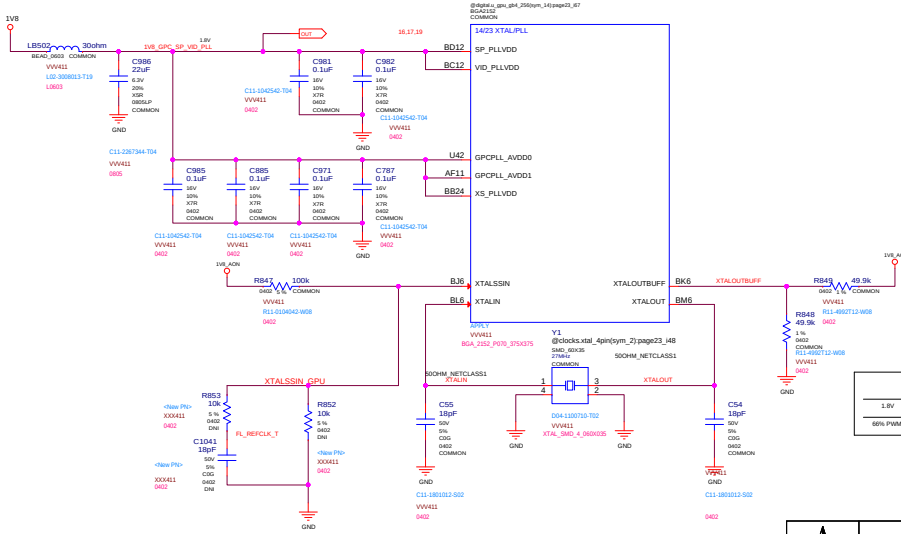






CFG[3:0]	Config Width	Vendor
0000	256Mx32 256-bit Samsung	
0001	256Mx32 256-bit Micron	
0010	256Mx32 256-bit Hynix	
0011	Reserved	
0100	Reserved	
0101	Reserved	
0110	Reserved	
0111	Reserved	





XTALOUTBUFF		
1.8V	0.9V	0V
66% PWM	33% PWM	DISABLED (100%)

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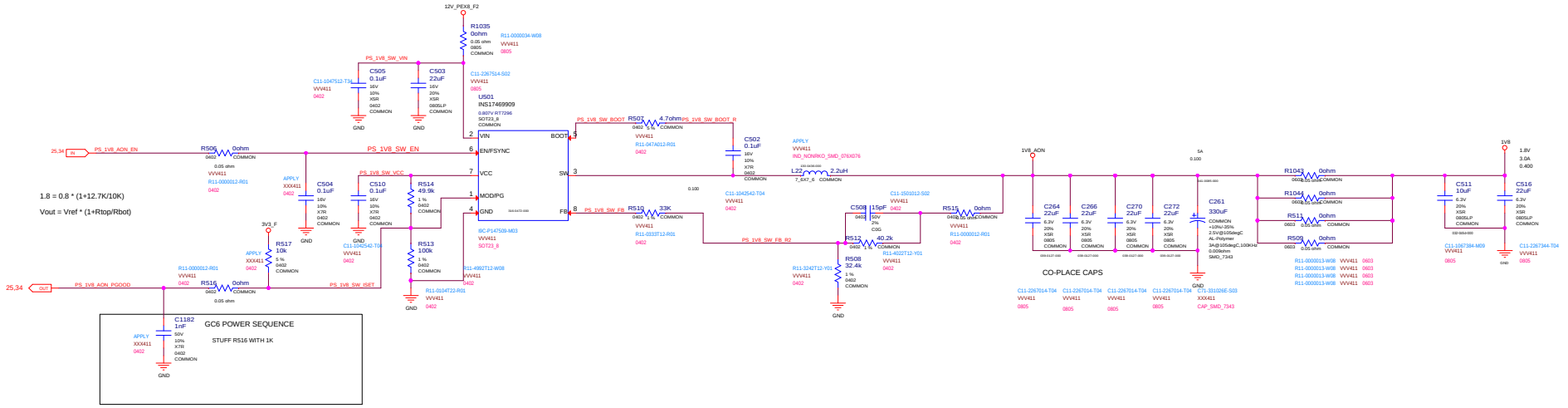

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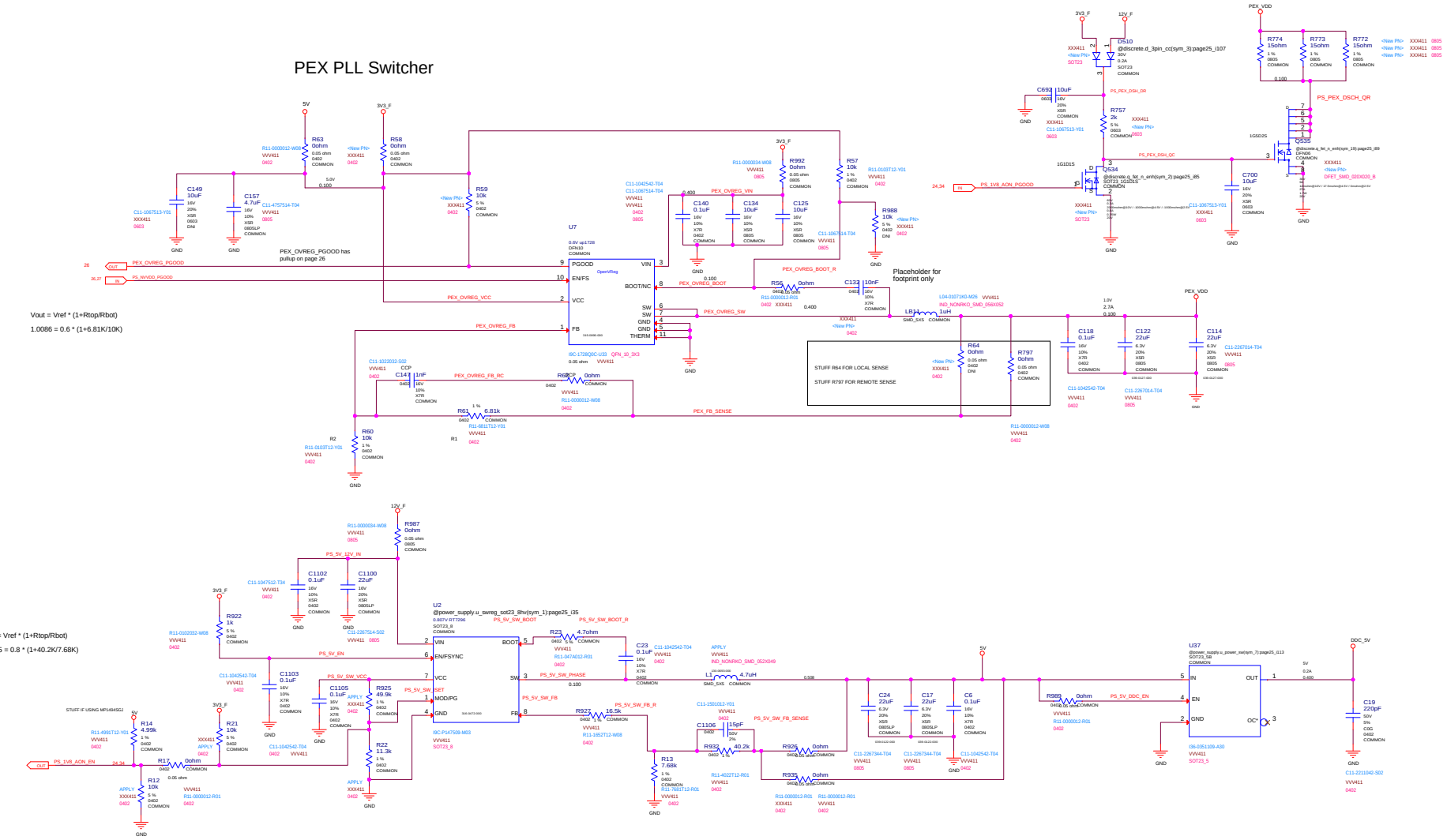
PEX PLL Switcher



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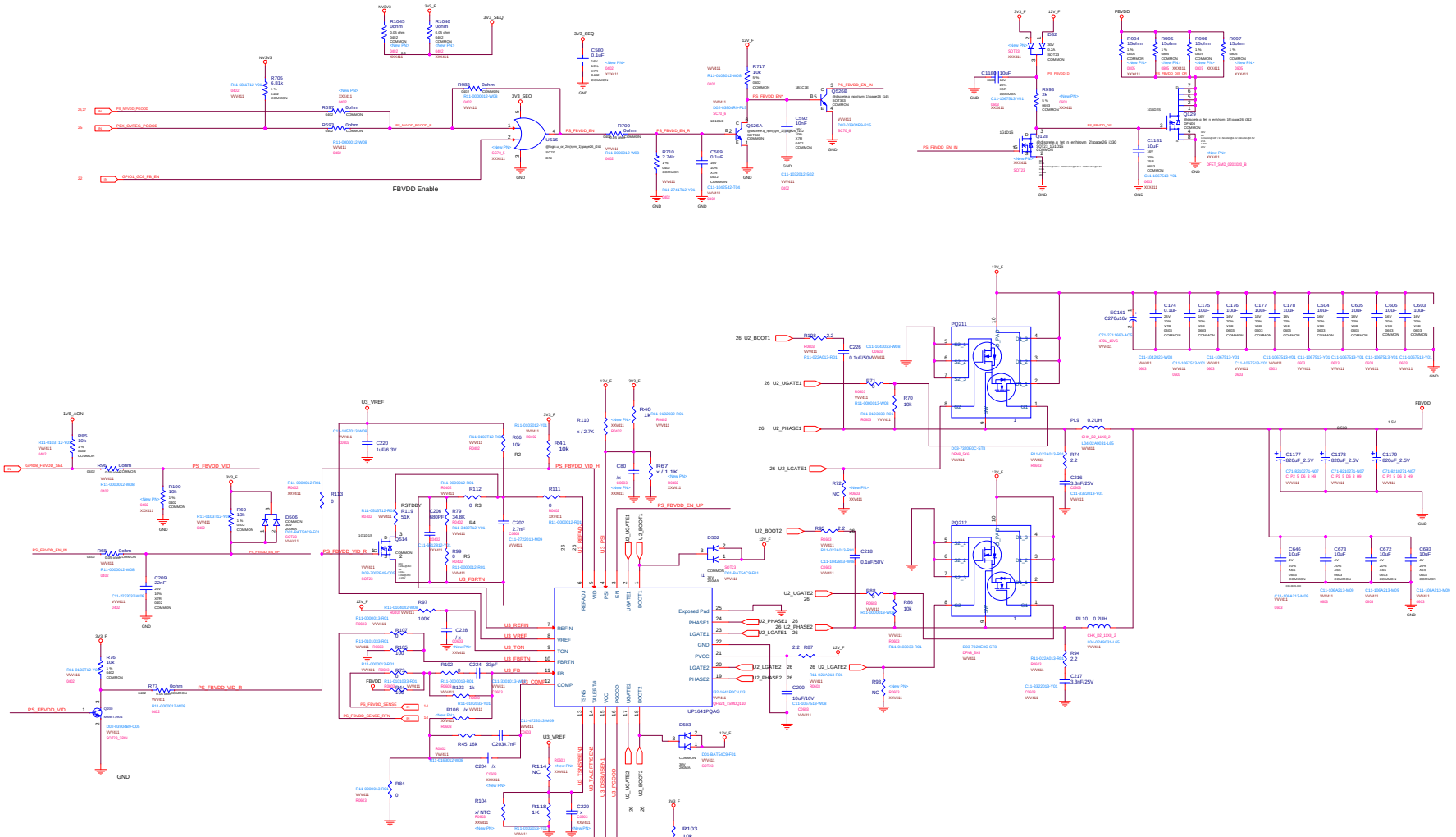
Page26: PS: FBVDD



VOLTAGE OUTPUT LEVELS ARE SET BY
CONTROLLING THE LEVEL OF GPIO8
ACCORDING TO THE FOLLOWING TABLES:

SAMSUNG K4G1325FC-HC28

GPIO8 LEVEL	FBVDD OUTPUT VOLTAGE
0	1.35V
1	1.55V

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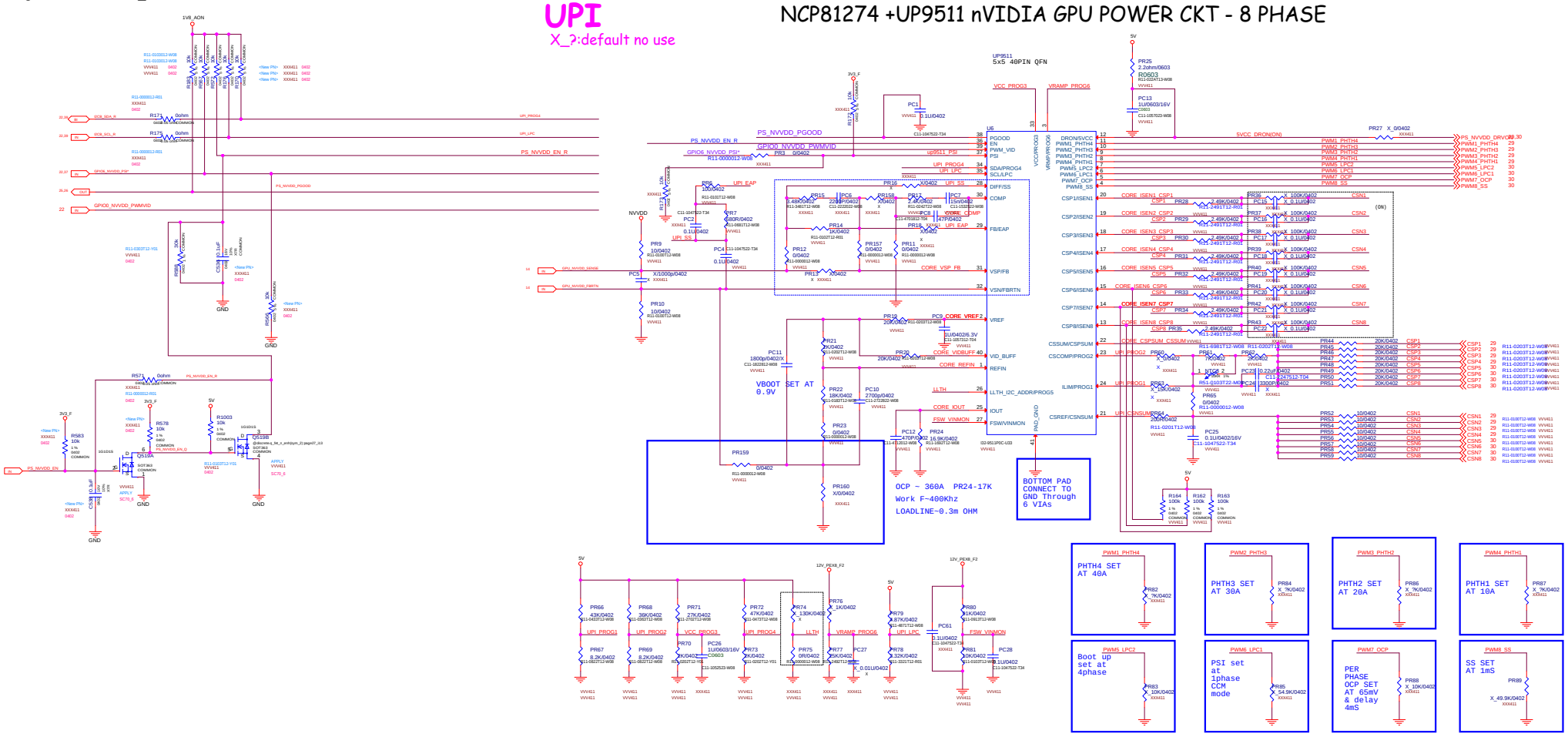
UPI

X_?:default no use

NCP81274 +UP9511 nVIDIA GPU POWER CKT - 8 PHASE



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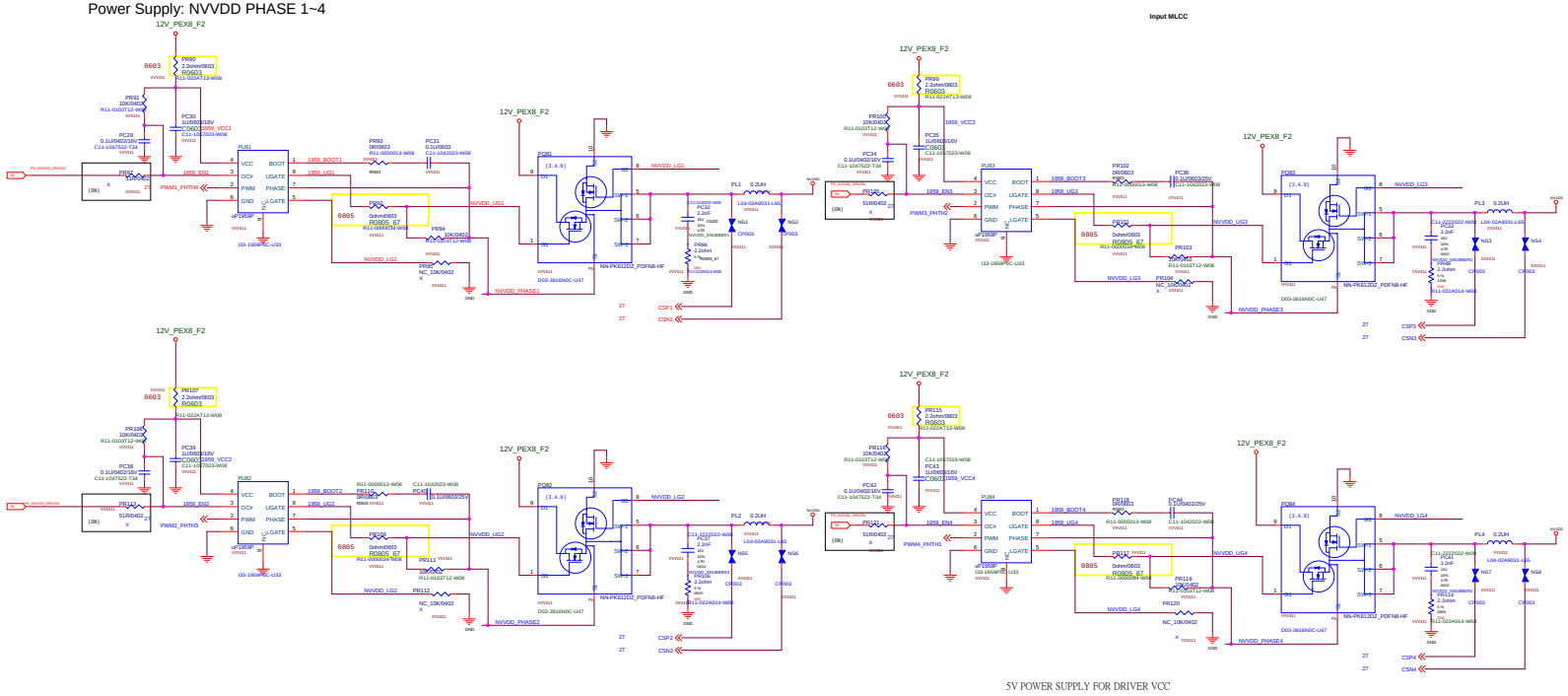
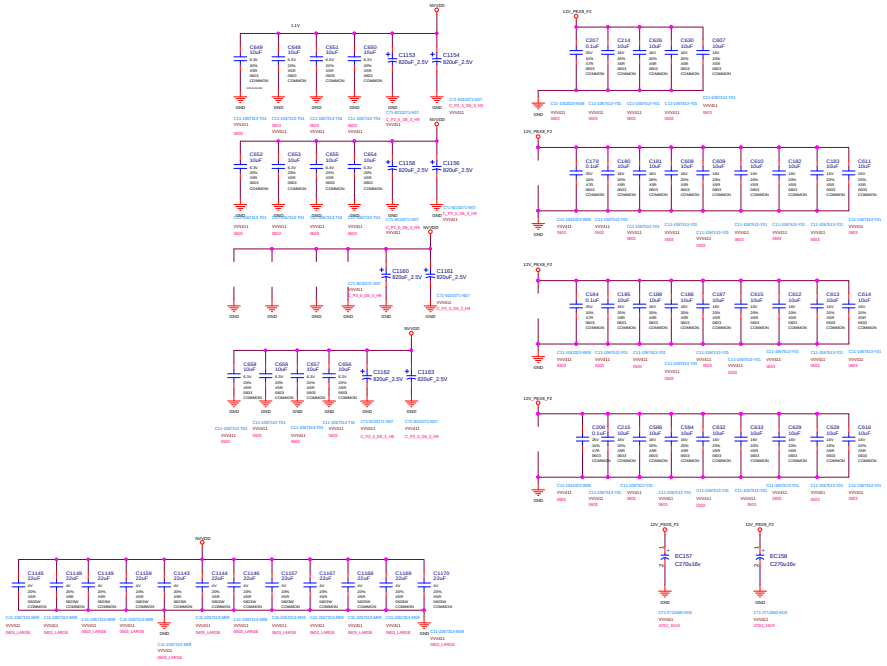
Power Supply: NVVDD PHASE 1~4





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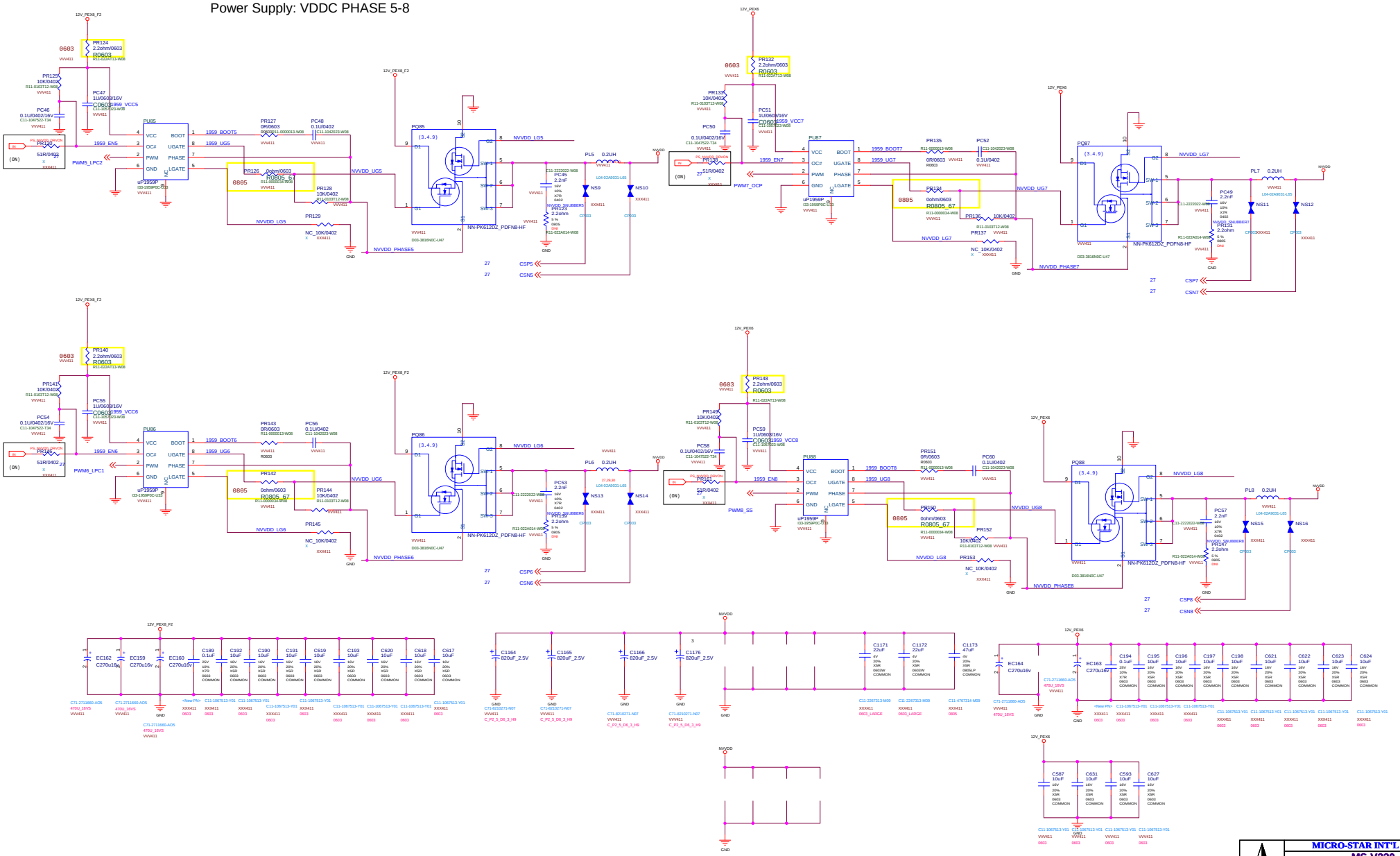
Page30: PS: NVVDD Phase 5 ~8

Power Supply: VDDC PHASE 5-8



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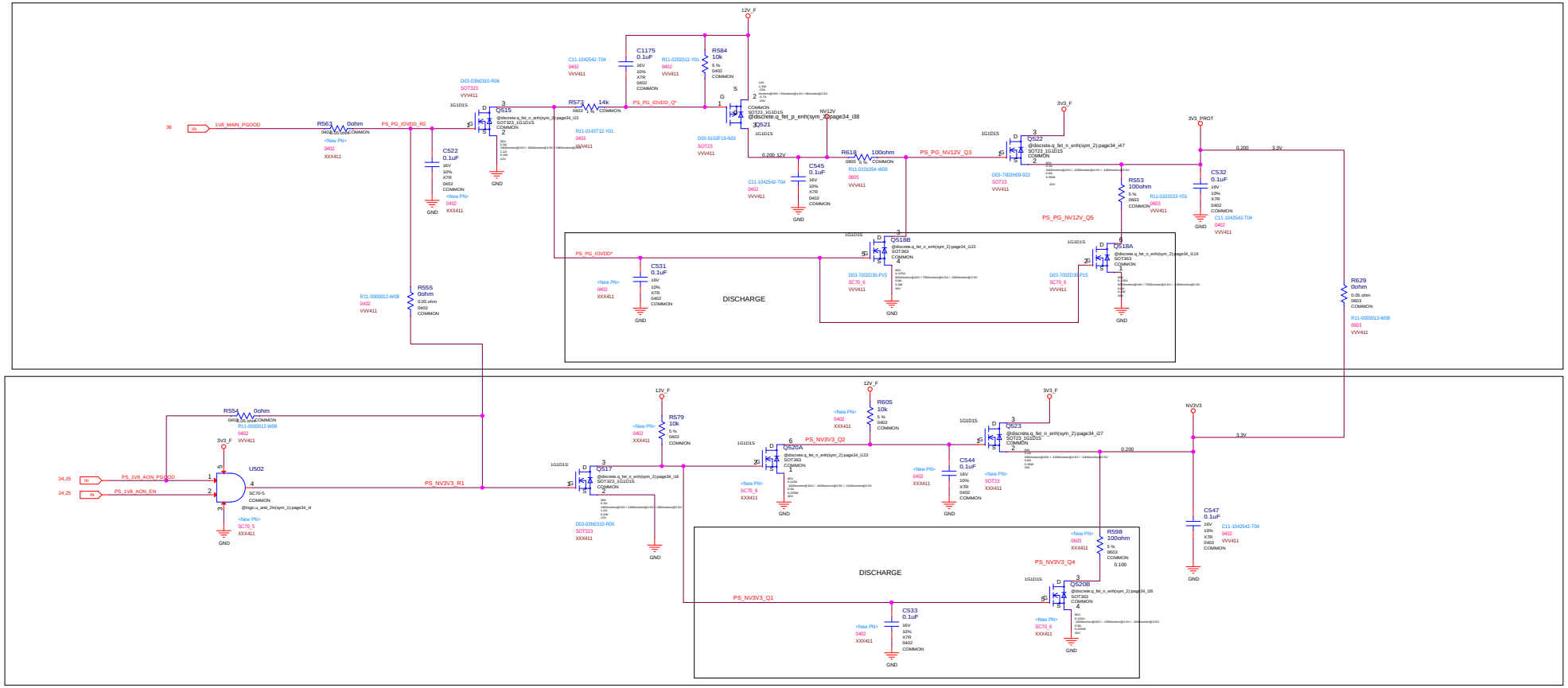
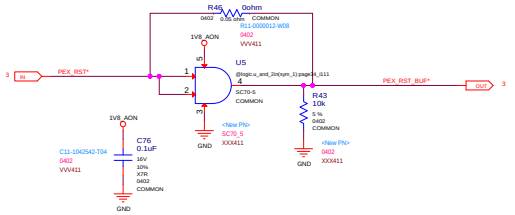
Page32: PS: Dynamic Power Balance Phases

Page33: PS: Dynamic Power Balance Logic

Page34:PS: NV3V3, NV12V





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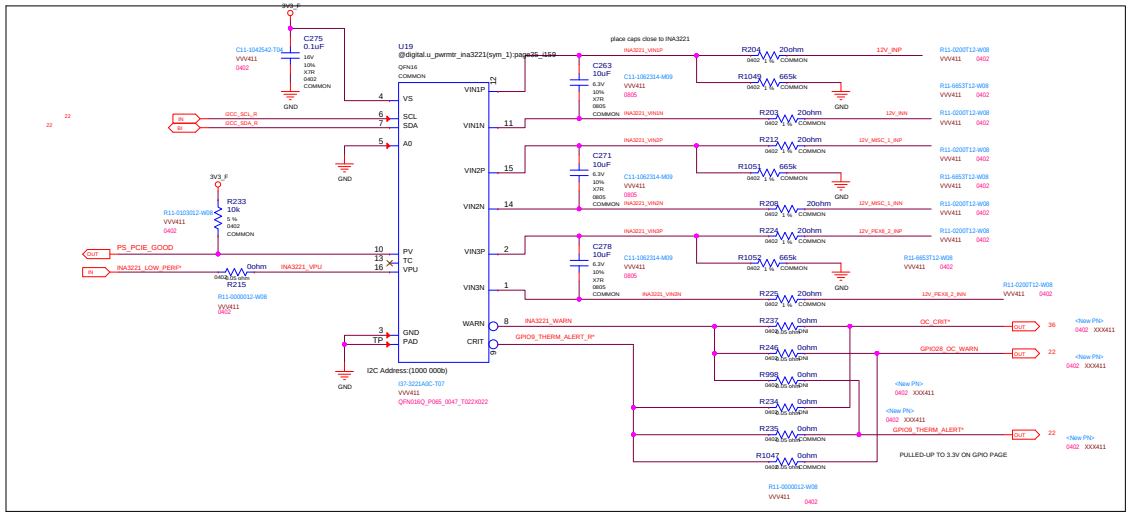
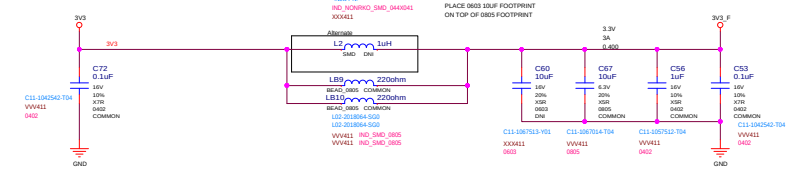
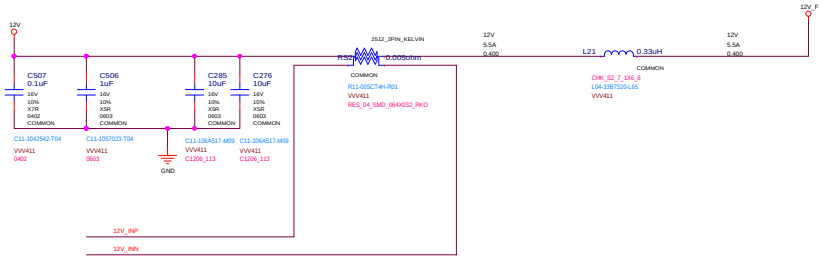
Page35: PS: Inputs, Filtering, and Monitoring

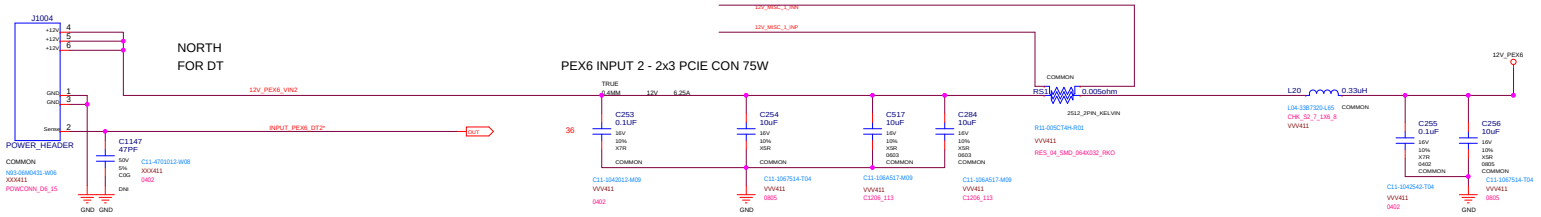


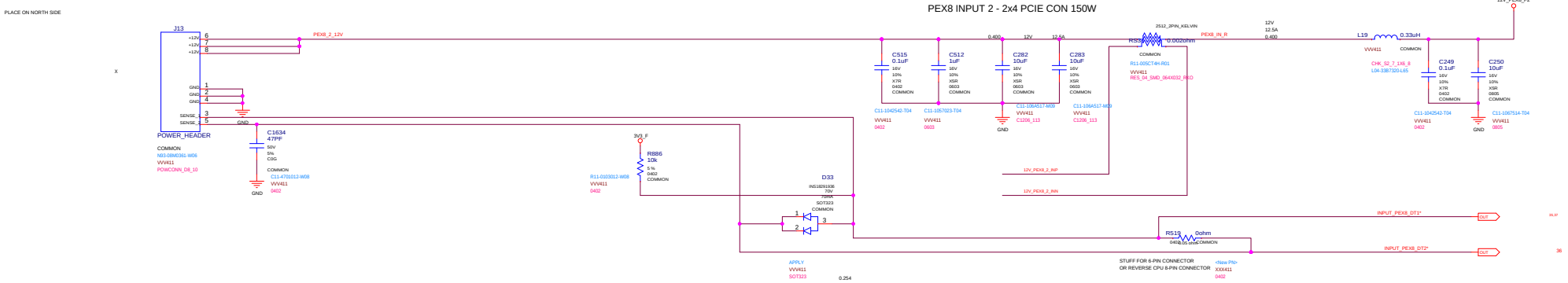
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W







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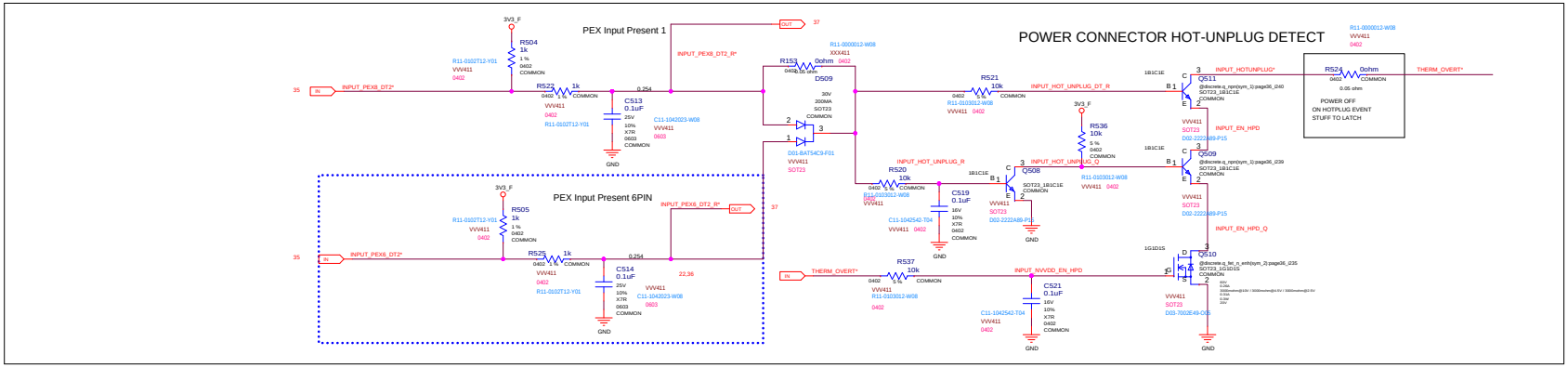
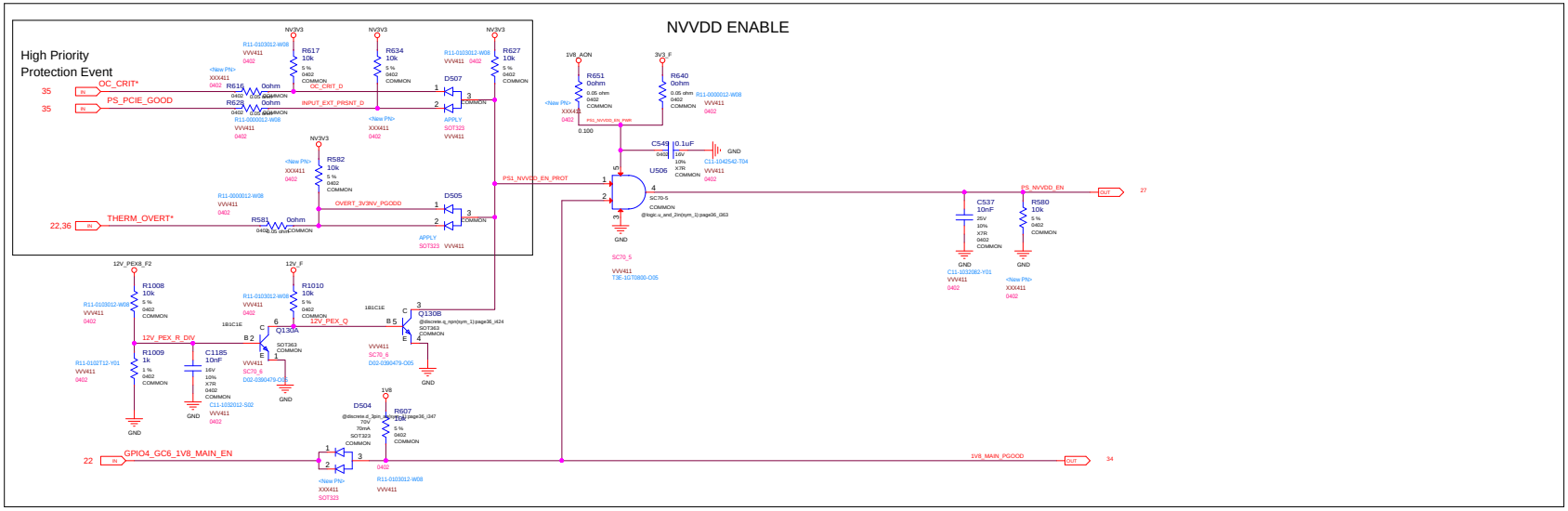
Page36: PS: Shutdown and Sequencing





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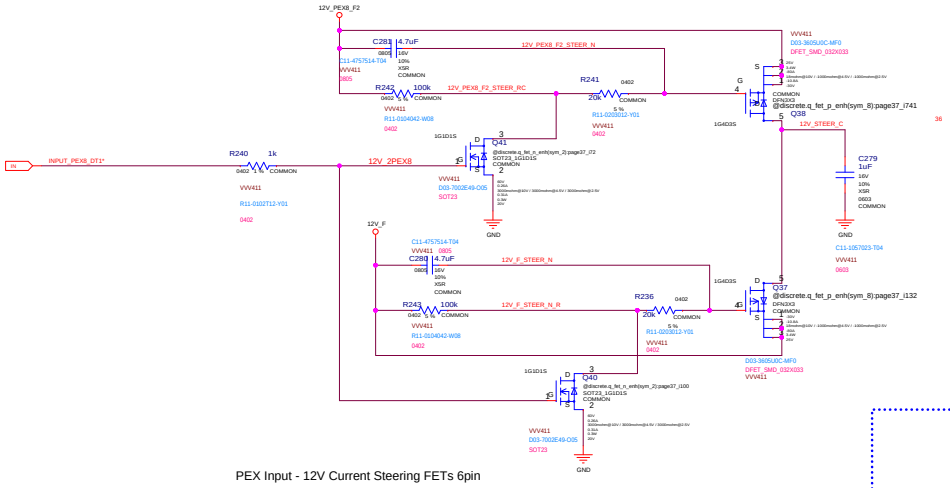
Page37: PS: 12V Current Steering, PSI Control, and LED

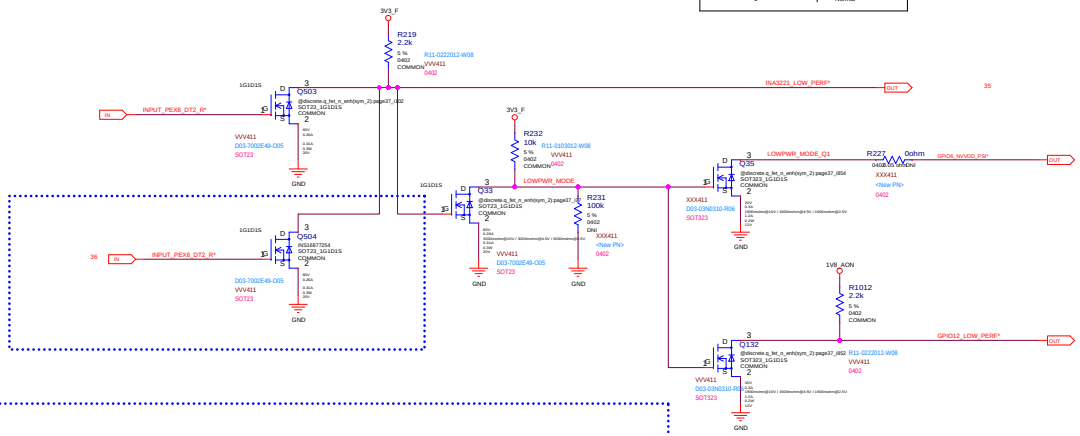
PEX Input - 12V Current Steering FETs 8pin



PEX Input - 12V Current Steering FETs 6pin

PEX Input - Power Level/PSI* Control

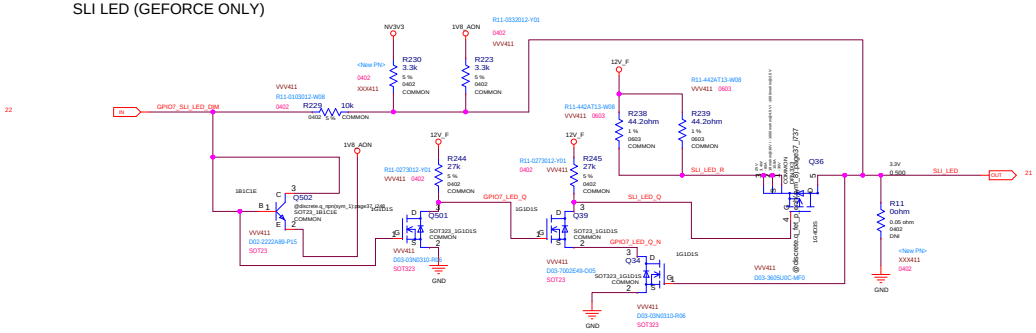
GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal



Remove POWER BRAKE

POWER BRAKE

SLI LED (GEFORCE ONLY)



GeForce Logo LED

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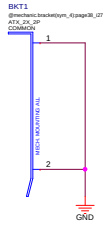
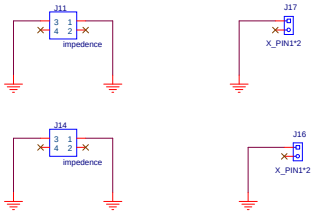
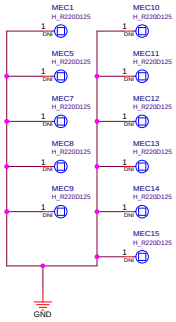
Page38: Mechanical: Bracket/Thermal Solution

Brackets:

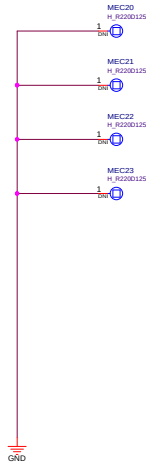


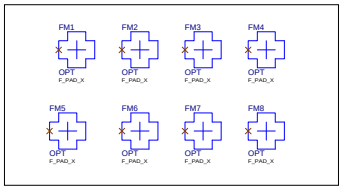


Mechanical Holes Symbol



GPU Stiffner





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