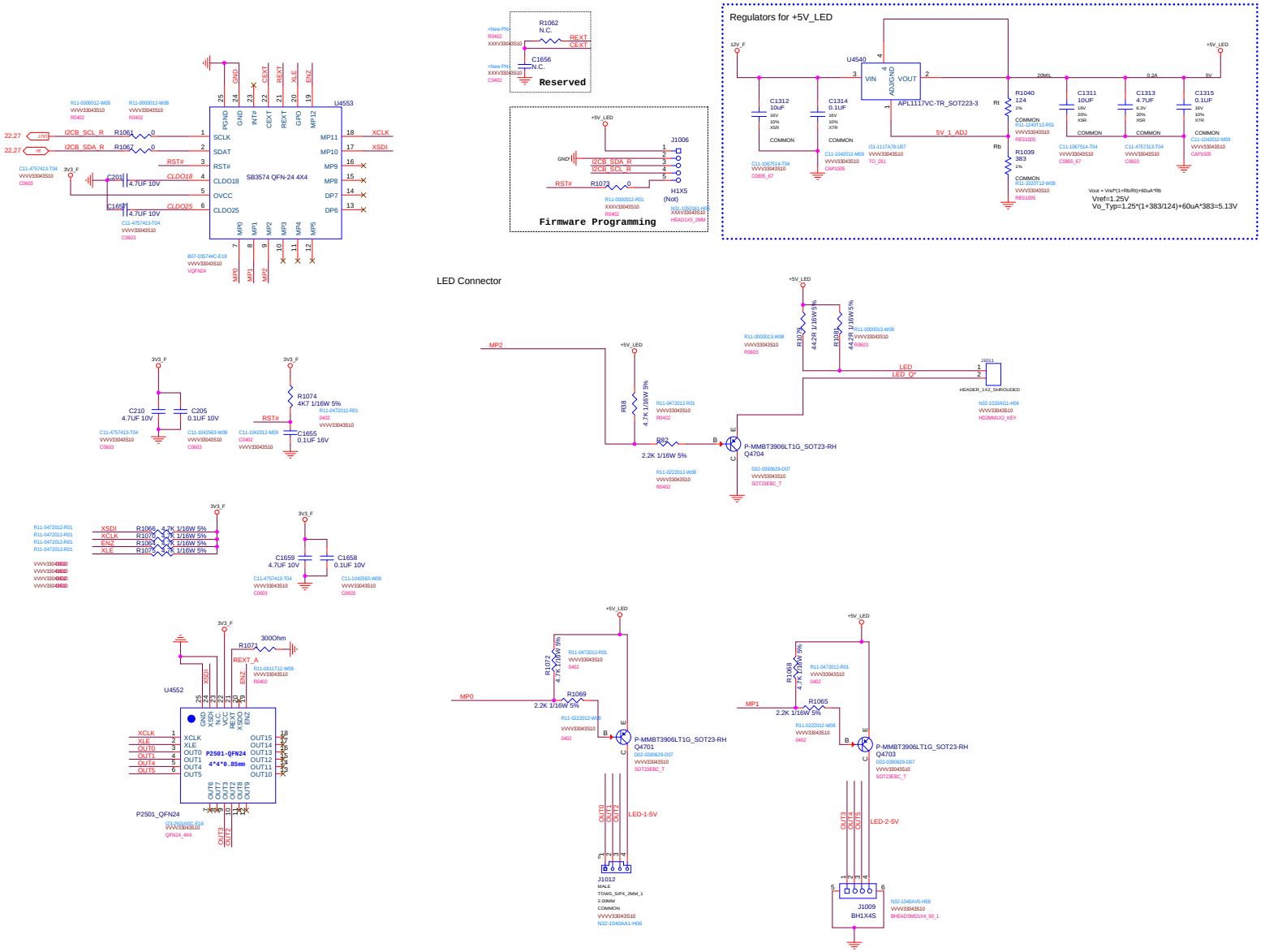
PG411 A01

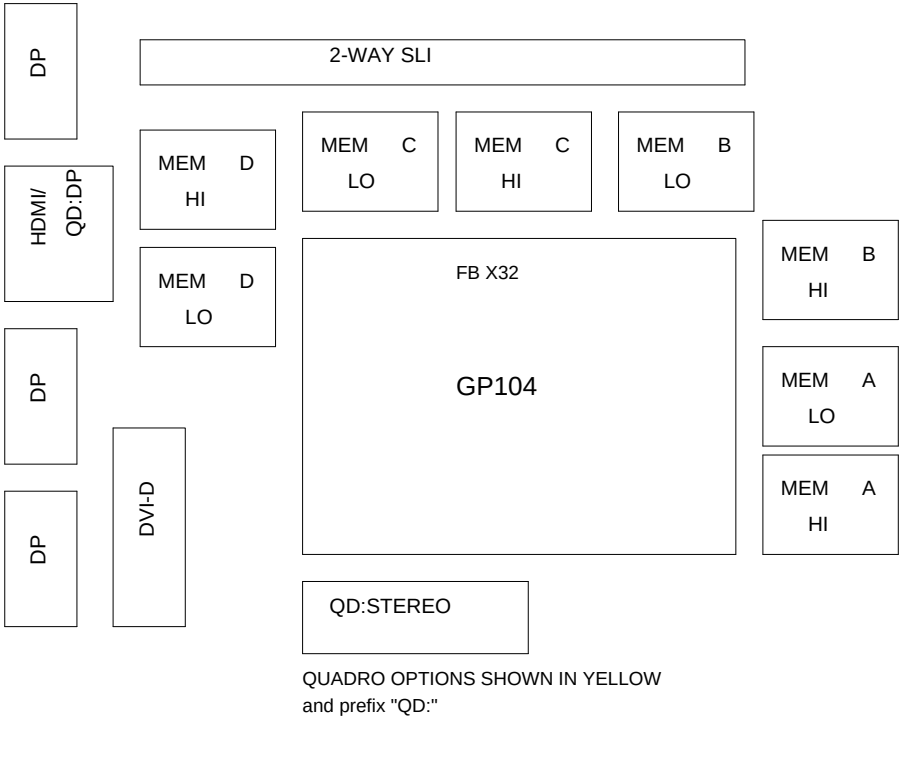
GP104 - 8GB GDDR5, 256b, 256Mx32
Tall DVI-D + DP + DP + HDMI + DP

TABLE OF CONTENTS

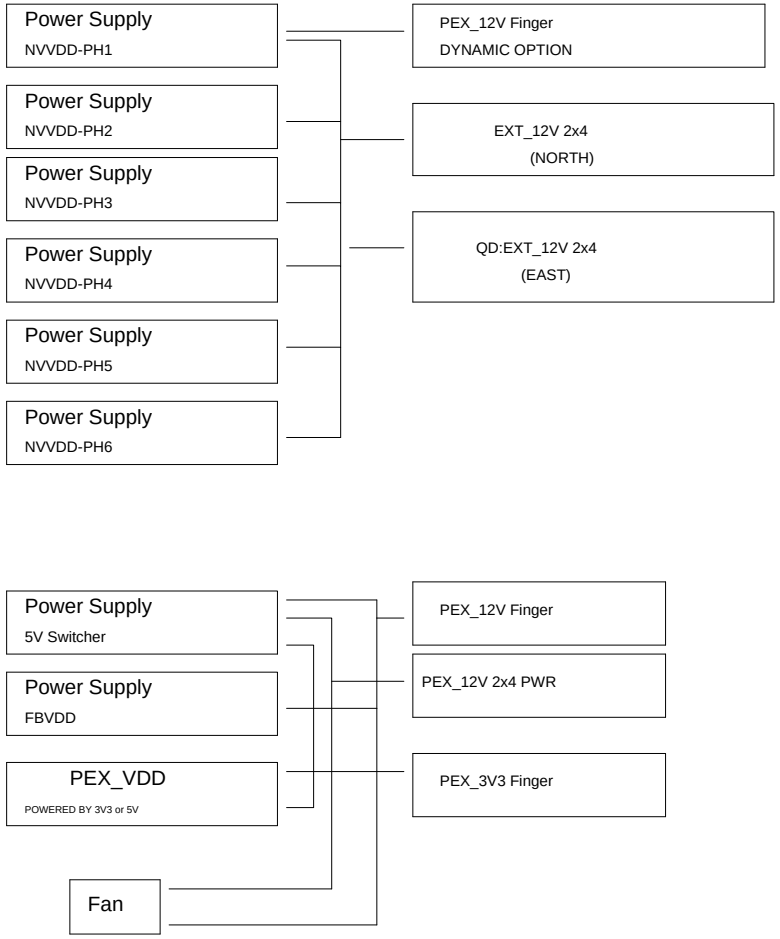
MICRO-STAR INT'L CO.,LTD
MS-V330
Size: Custom | Document Description: Table of Contents | Rev: 6.1
Date: Wednesday, August 10, 2016 | Sheet 1 of 39



MICRO-STAR INT'L CO.,LTD		
MS-V330		
Size: Custom	Document Description: Table of Contents	Rev: 6.1
Date: Wednesday, August 10, 2016	Sheet 39 of 39	

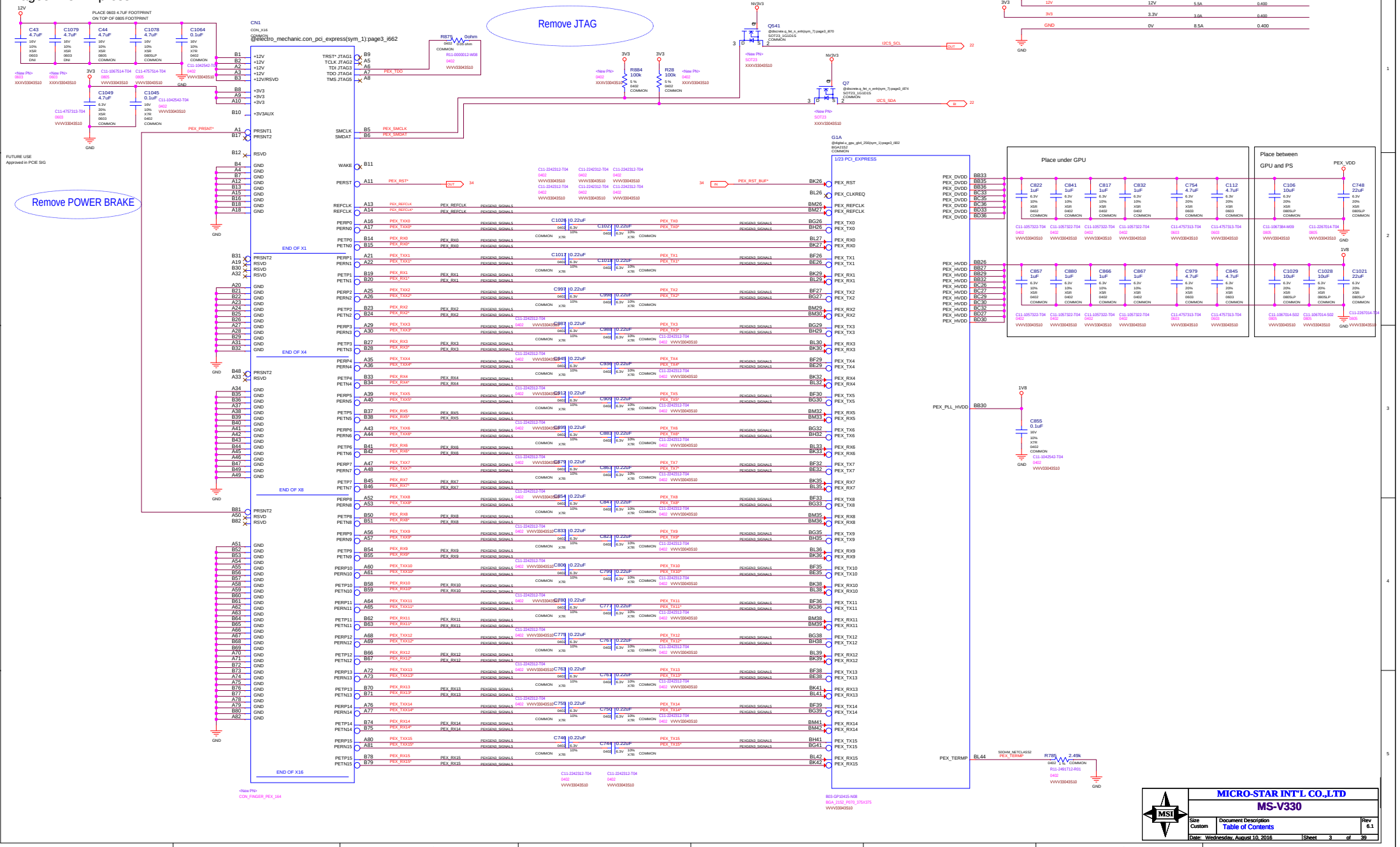


QUADRO OPTIONS SHOWN IN YELLOW
and prefix "QD:"

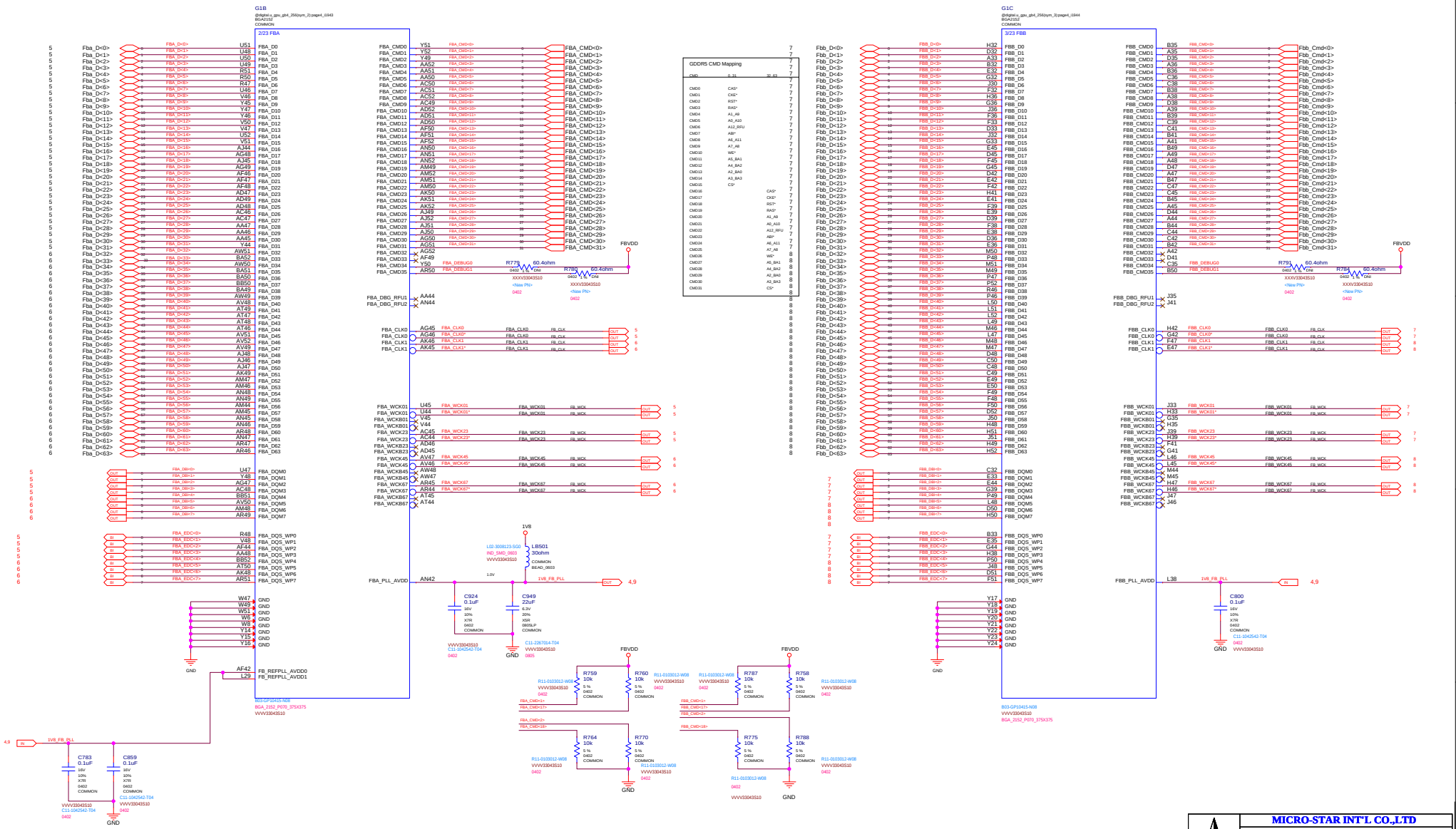


MICRO-STAR INT'L CO.,LTD
MS-V330
Size: Custom | Document Description: Table of Contents | Rev: 6.1
Date: Wednesday, August 10, 2016 | Sheet 2 of 39

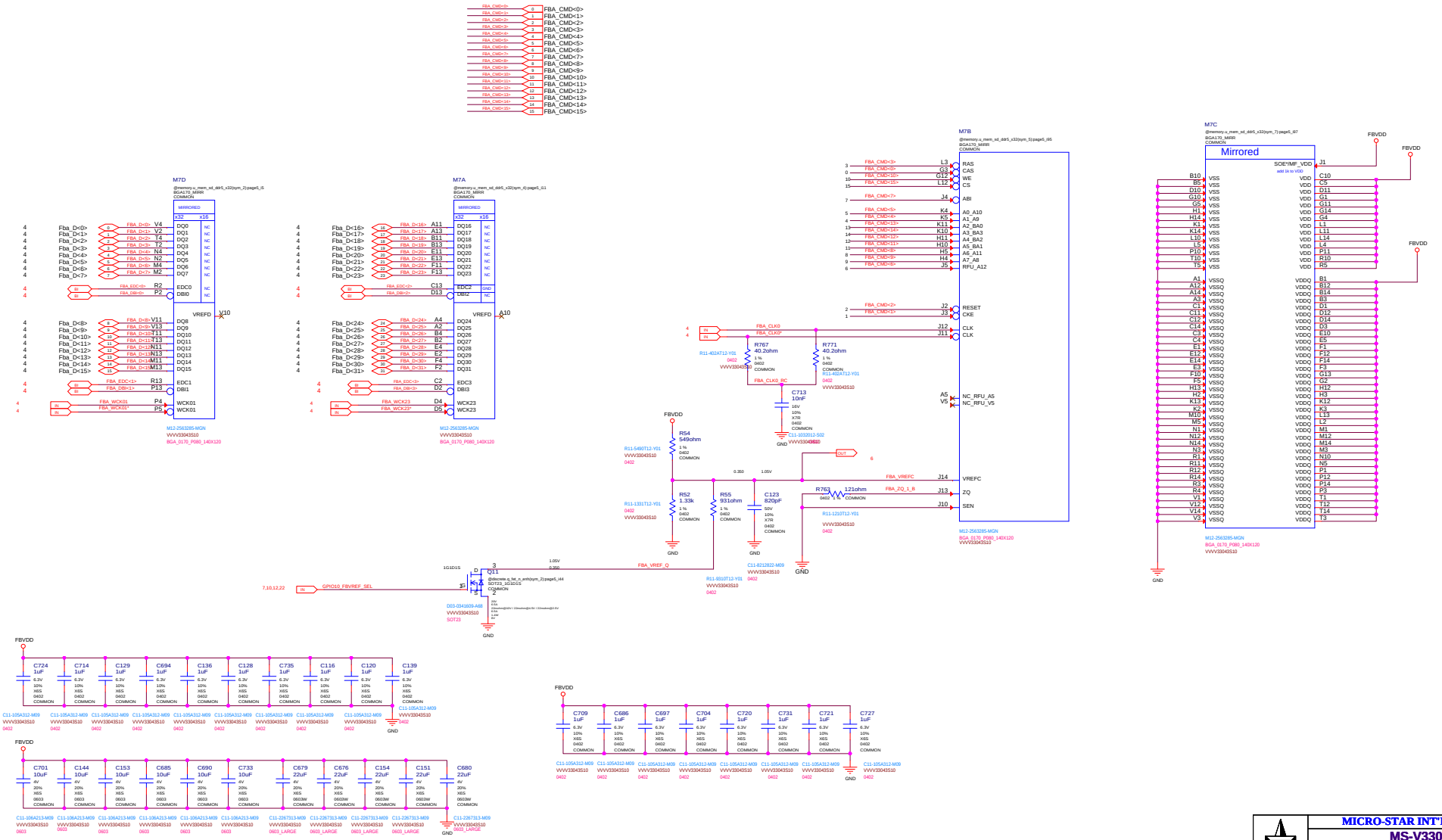
Page3: PCI Express



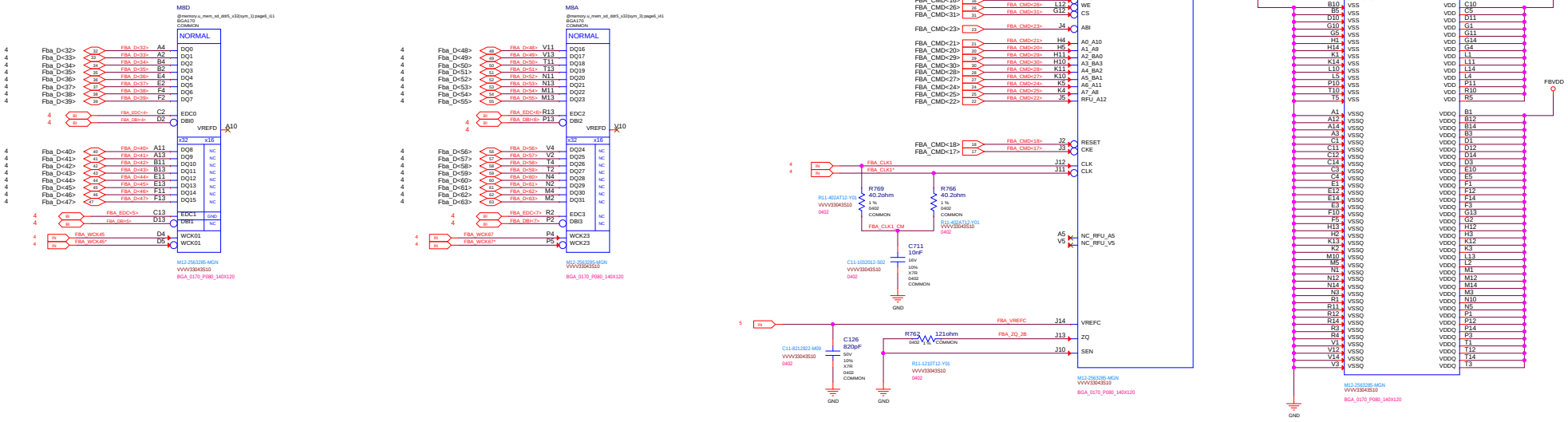
Page4: MEMORY: GPU Partition A/B

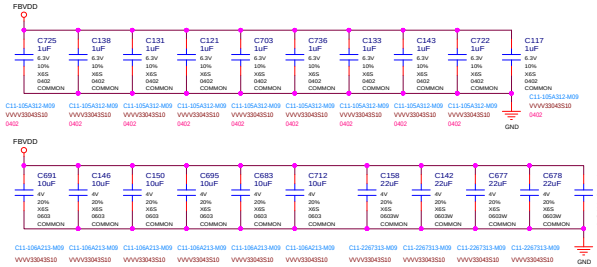


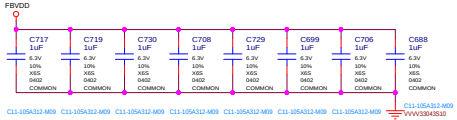
Page5: MEMORY: FBA Partition 31..0



Page6: MEMORY: FBA Partition 63..32

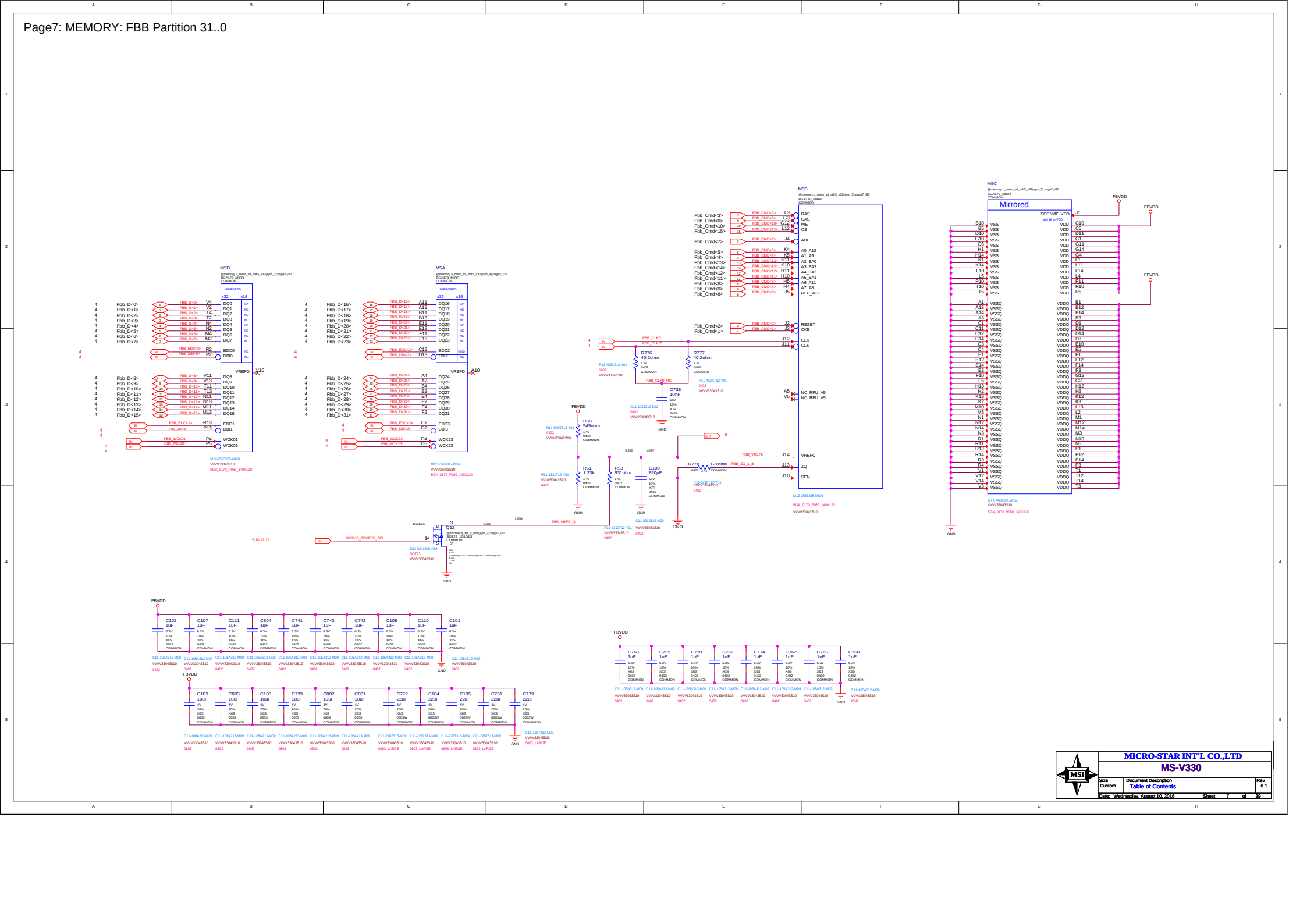




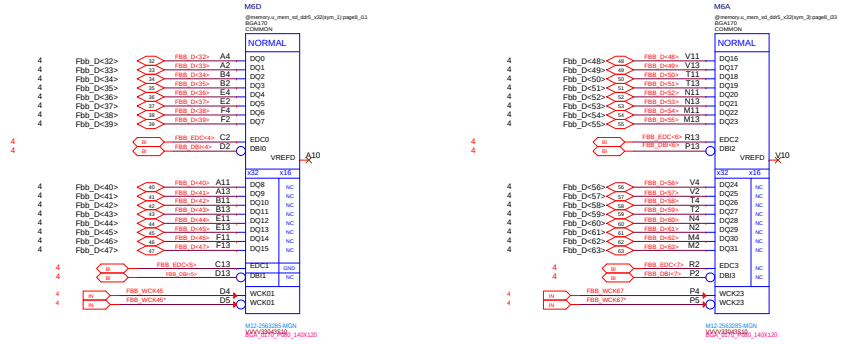


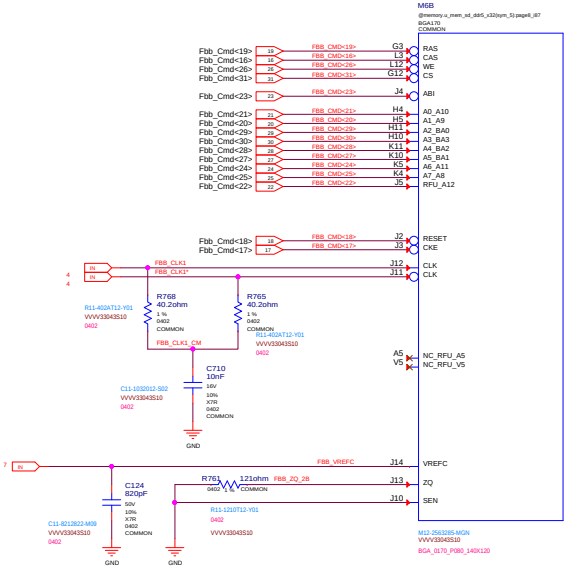
MICRO-STAR INT'L CO.,LTD	
MS-V330	
Size: Custom	Document Description: Table of Contents
Rev: 6.1	
Date: Wednesday, August 10, 2016	Sheet 6 of 39

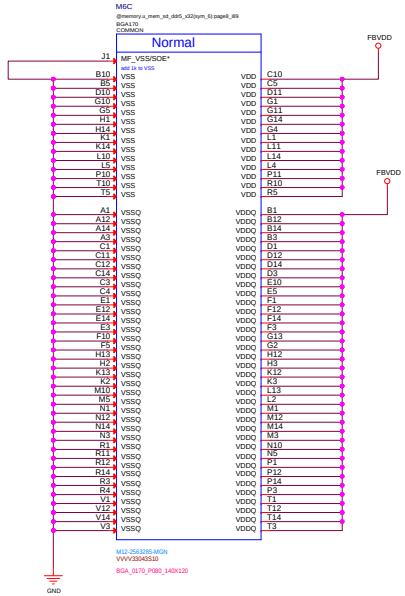
Page7: MEMORY: FBB Partition 31..0

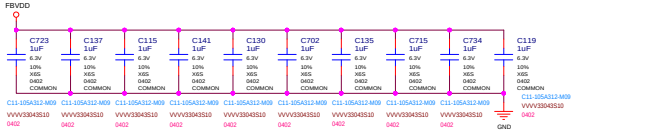


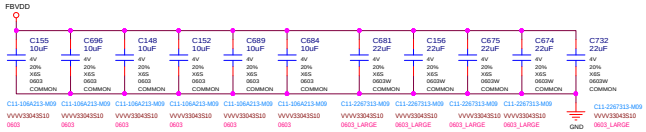
Page8: MEMORY: FBB Partition 63..32

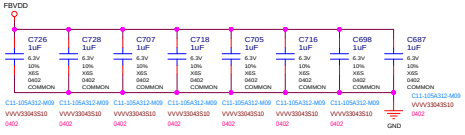












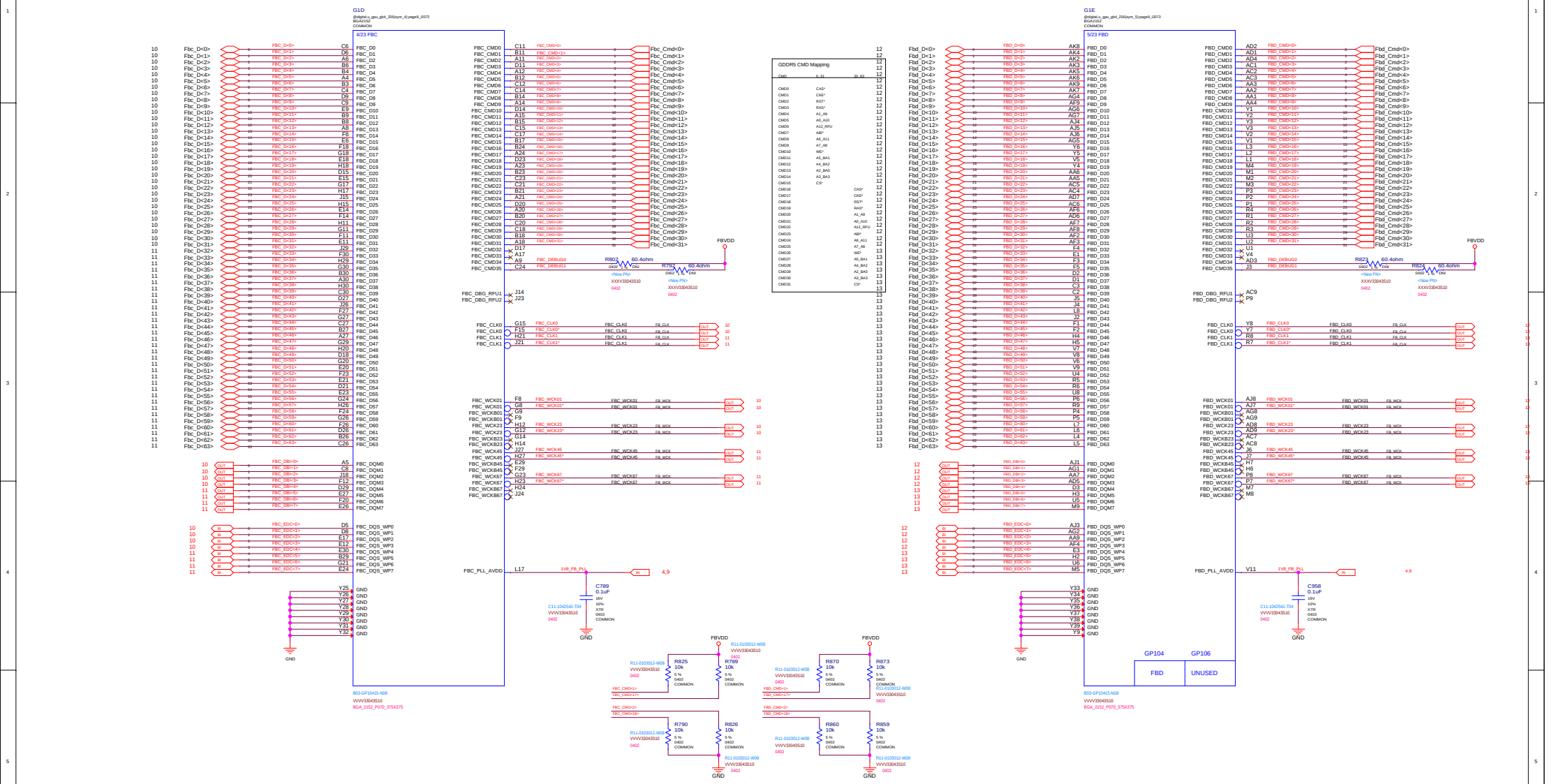
MICRO-STAR INT'L CO.,LTD

MS-V330

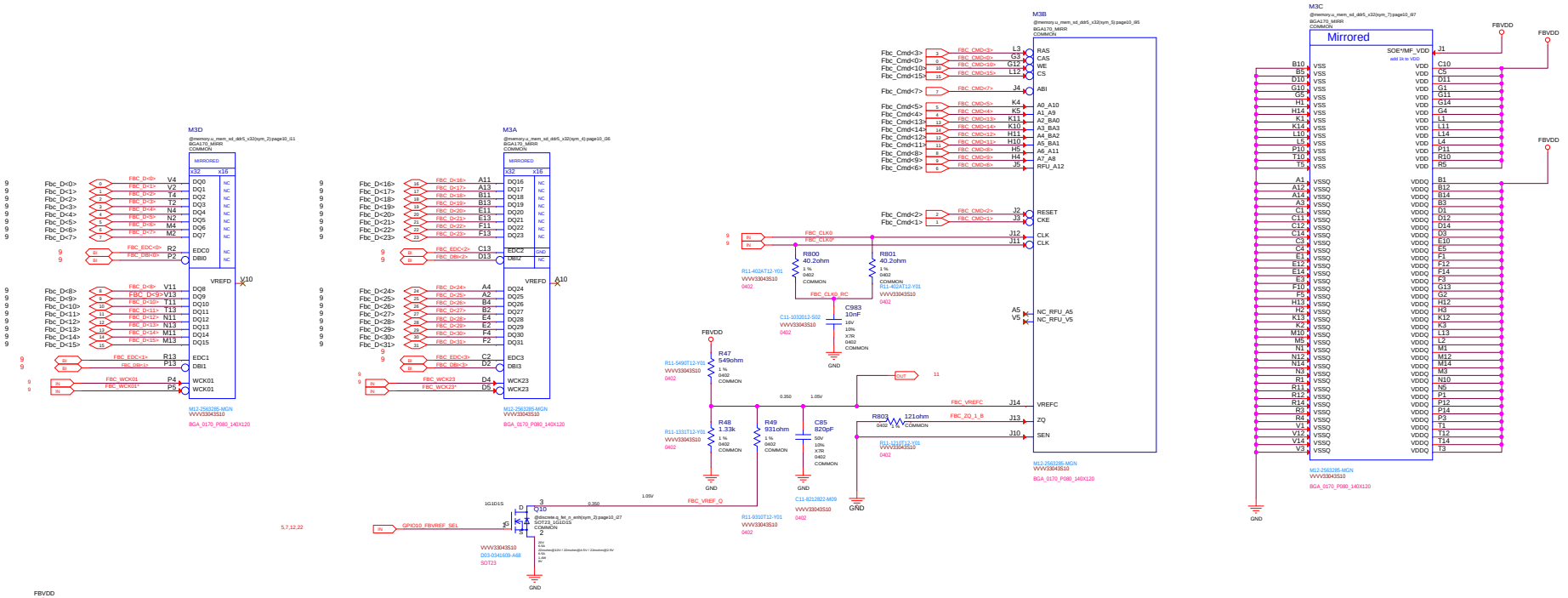
Size	Document Description	Rev
Custom	Table of Contents	6.1

Date: Wednesday, August 10, 2016 Sheet 8 of 39

Page9: MEMORY: GPU Partition C/D

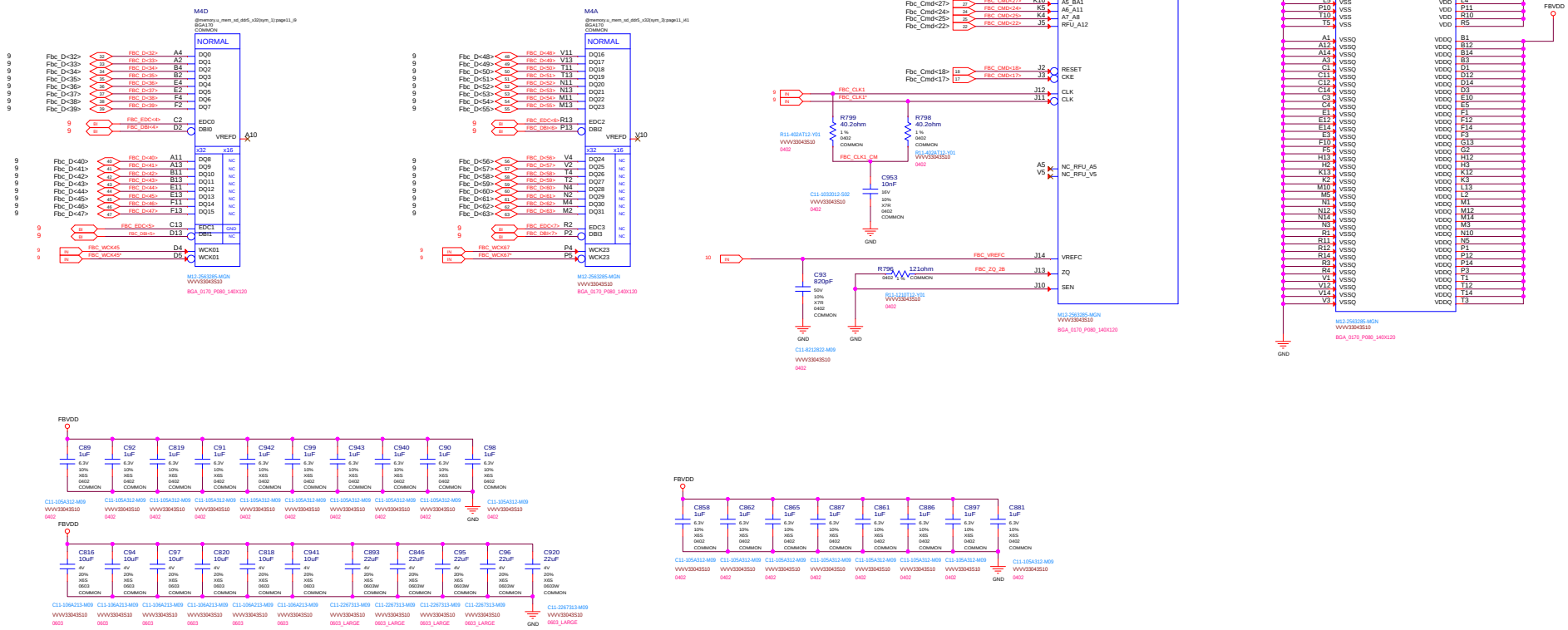


Page10: MEMORY: FBC Partition 31..0

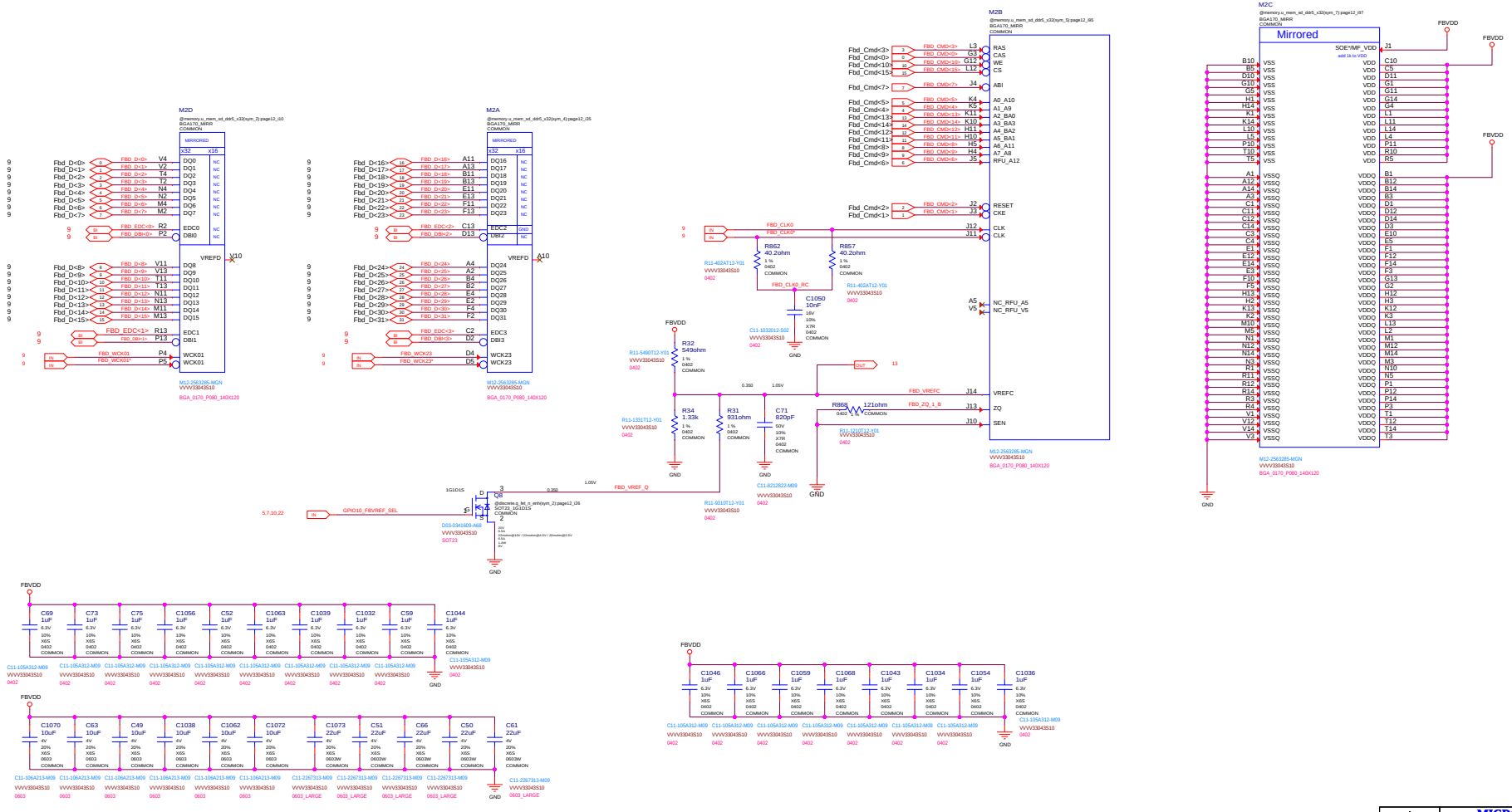


MICRO-STAR INT'L CO.,LTD			
MS-V330			
Size: Custom	Document Description: Table of Contents		Rev: 6.1
Date: Wednesday, August 10, 2016	Sheet 10 of 39		

Page11: MEMORY: FBC Partition 63..32

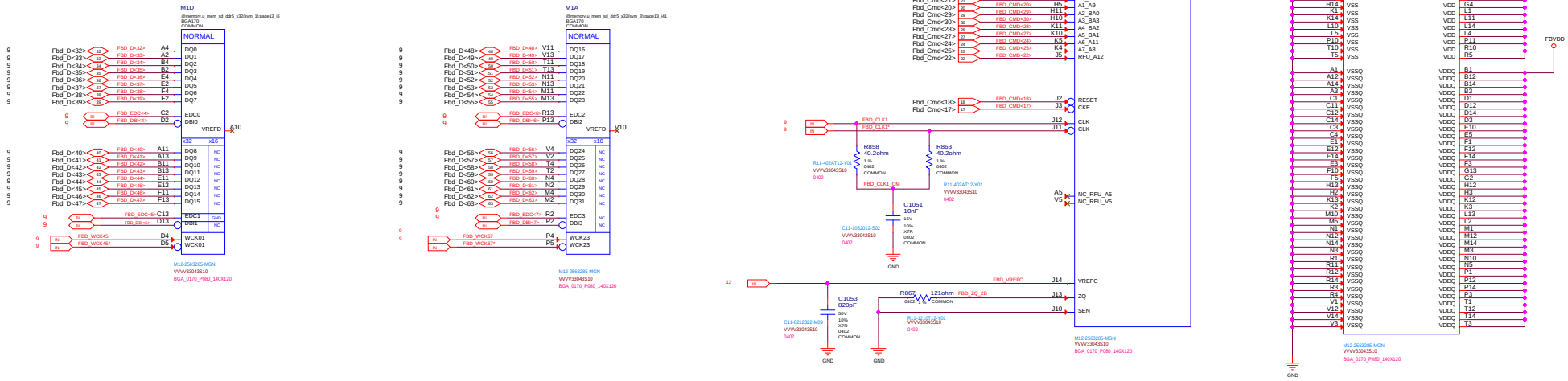


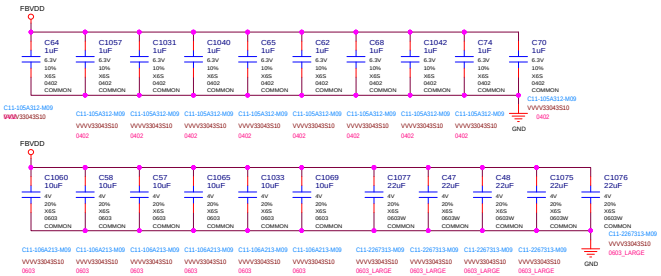
Page12: MEMORY: FBD Partition 31..0

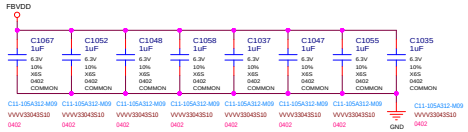


MICRO-STAR INT'L CO.,LTD		
MS-V330		
Size: Custom	Document Description: Table of Contents	Rev: 6.1
Date: Wednesday, August 10, 2016	Sheet 12 of 39	

Page13: MEMORY: FBD Partition 63..32

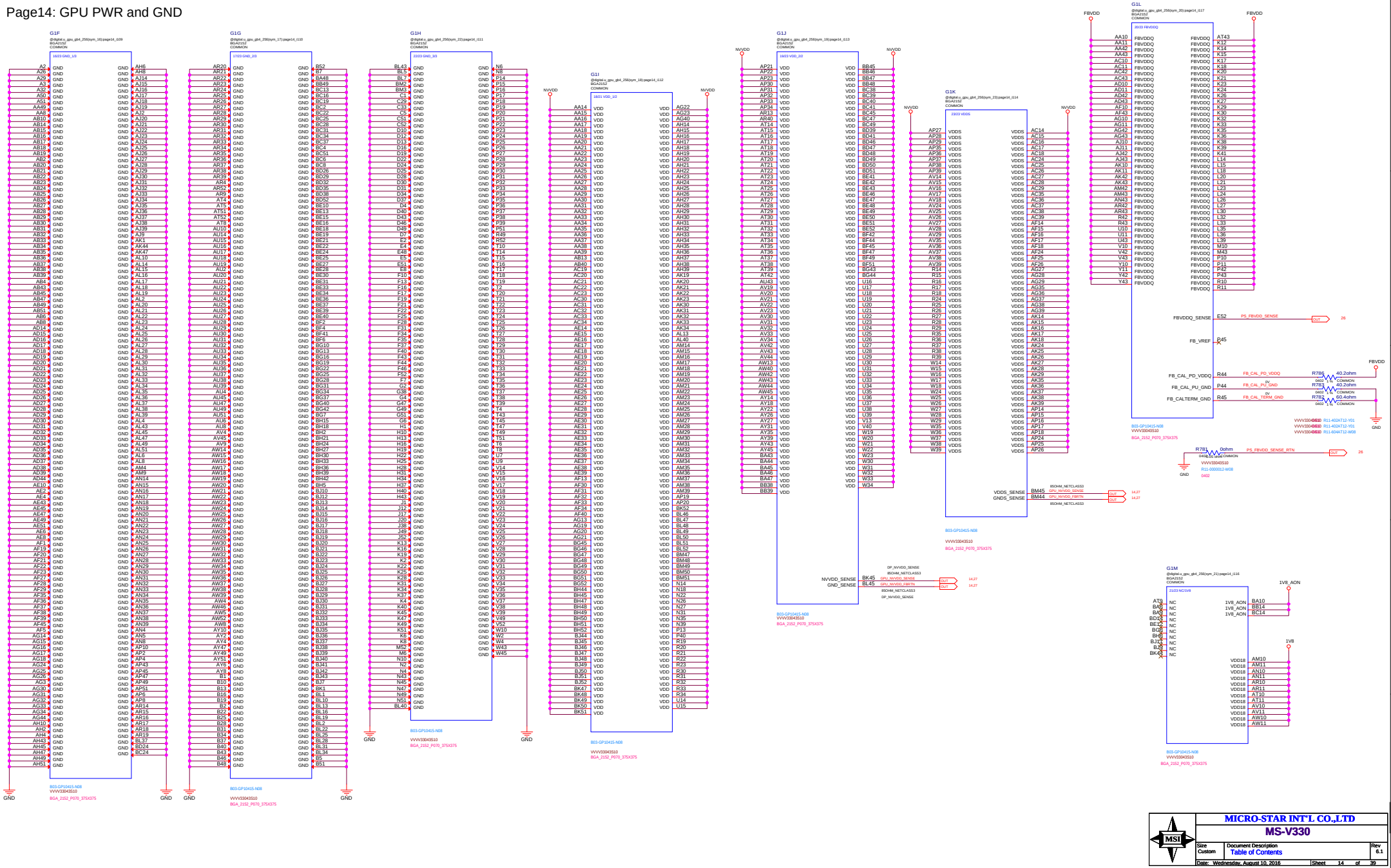






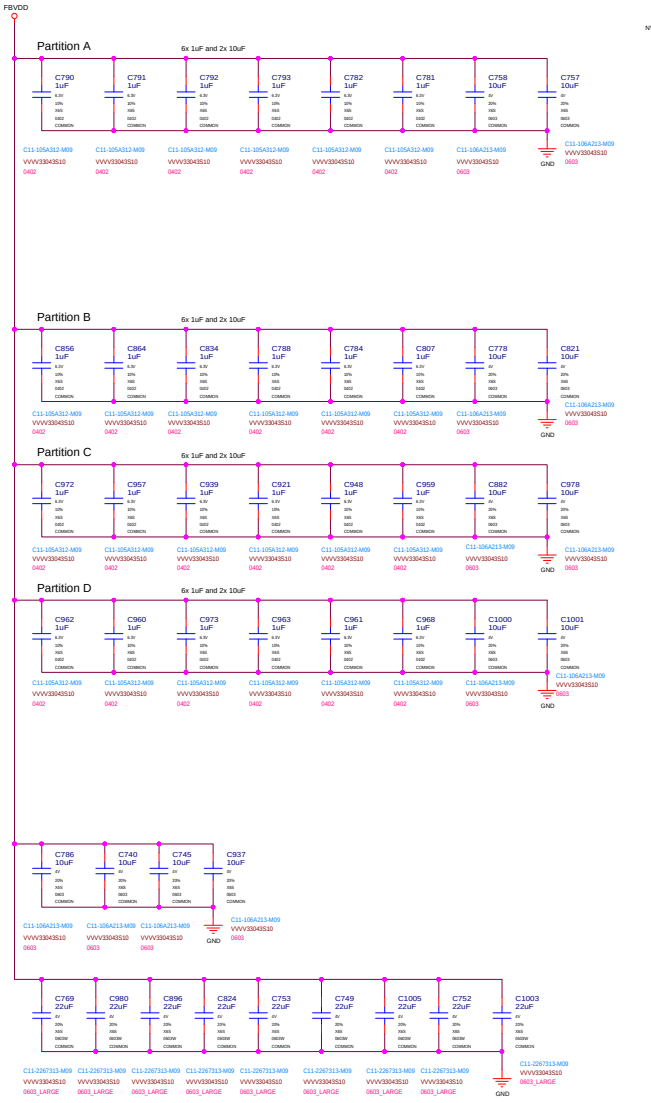
MICRO-STAR INT'L CO.,LTD			
MS-V330			
Size: Custom	Document Description: Table of Contents		Rev: 6.1
Date: Wednesday, August 10, 2016	Sheet 13 of 39		

Page14: GPU PWR and GND

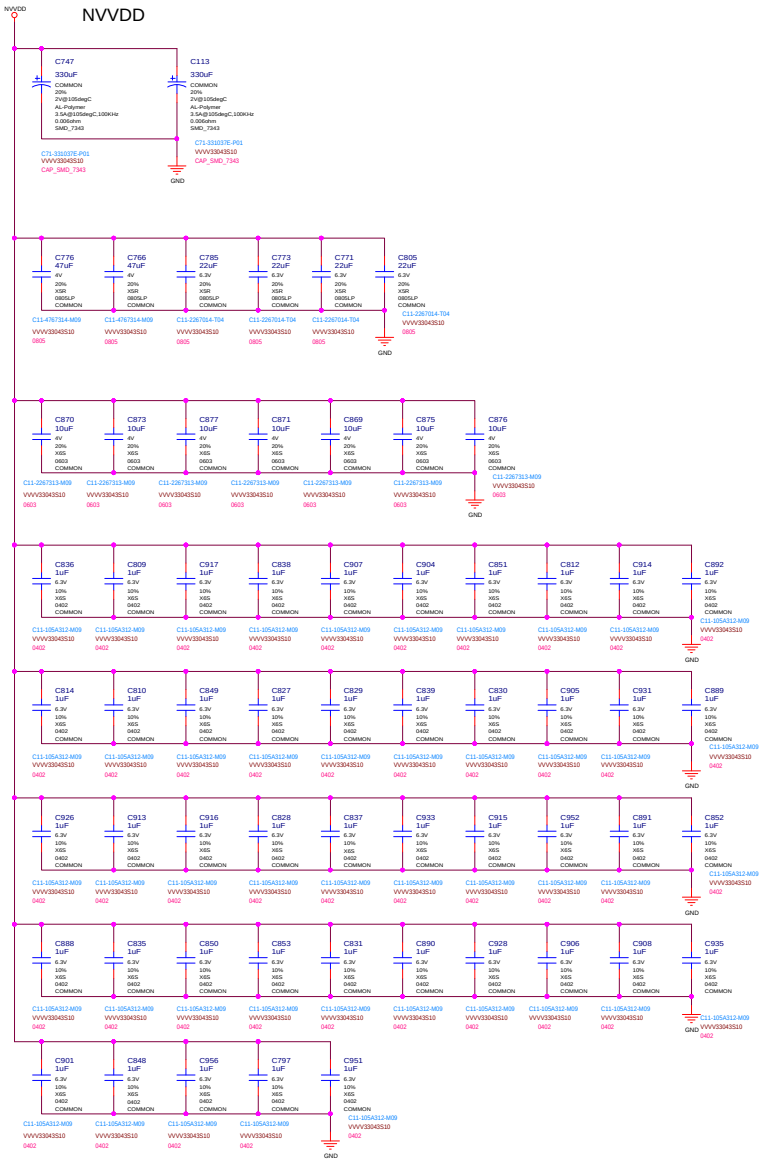


Page15: GPU Decoupling

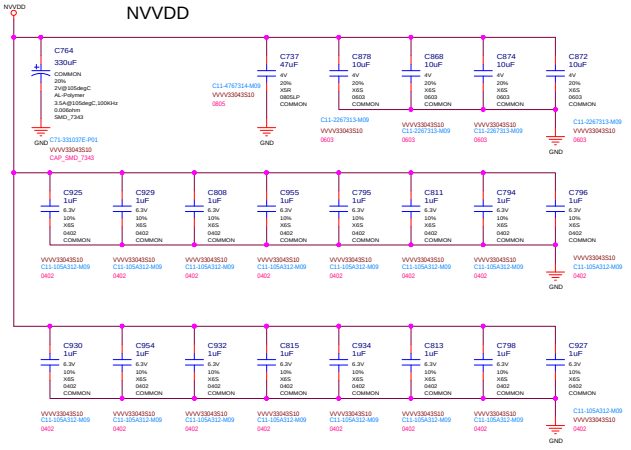
FBVDD

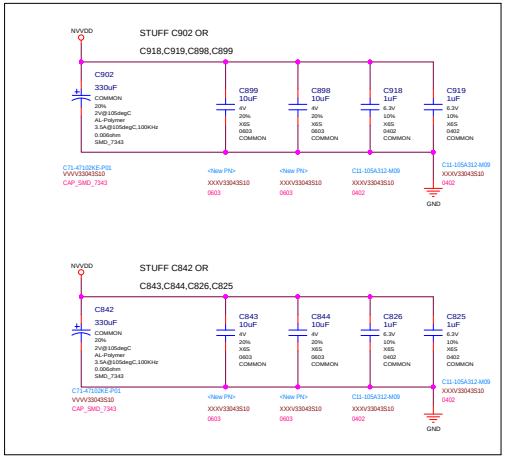


NVVDD

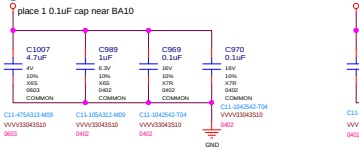


NVVDD



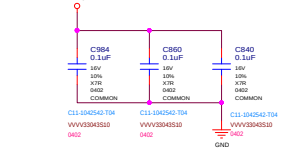


1V8_AON



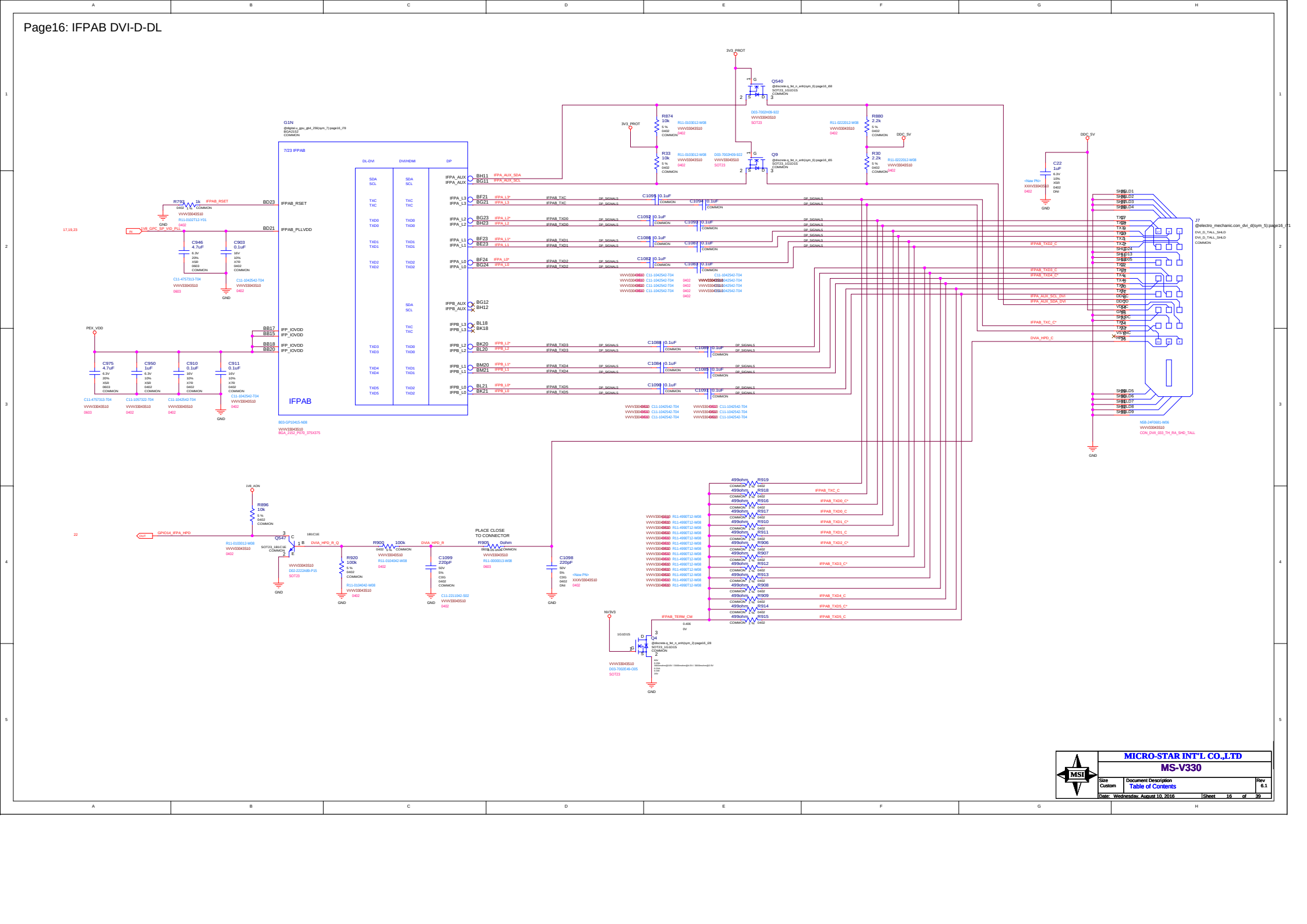
place 1 0.1uf cap for BB14 and BC14 to share

VDD18



MICRO-STAR INT'L CO.,LTD		
MS-V330		
Size: Custom	Document Description: Table of Contents	Rev: 6.1
Date: Wednesday, August 10, 2016	Sheet 15 of 39	

Page16: IFPAB DVI-D-DL



MICRO-STAR INT'L CO.,LTD
MS-V330

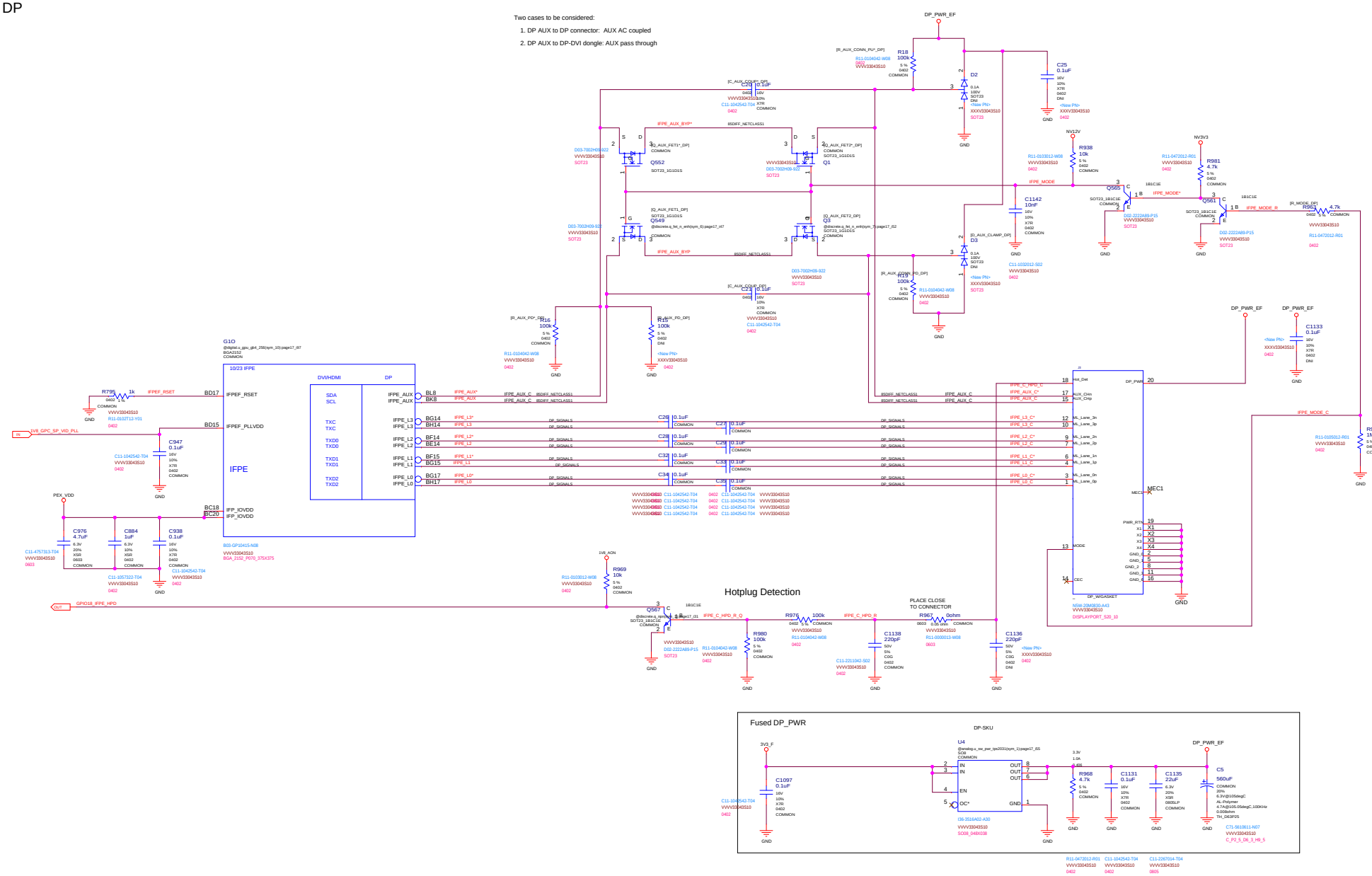
Size	Document Description	Rev
Custom	Table of Contents	6.1

Date: Wednesday, August 10, 2016 Sheet 16 of 39

Page17: IFPE DP

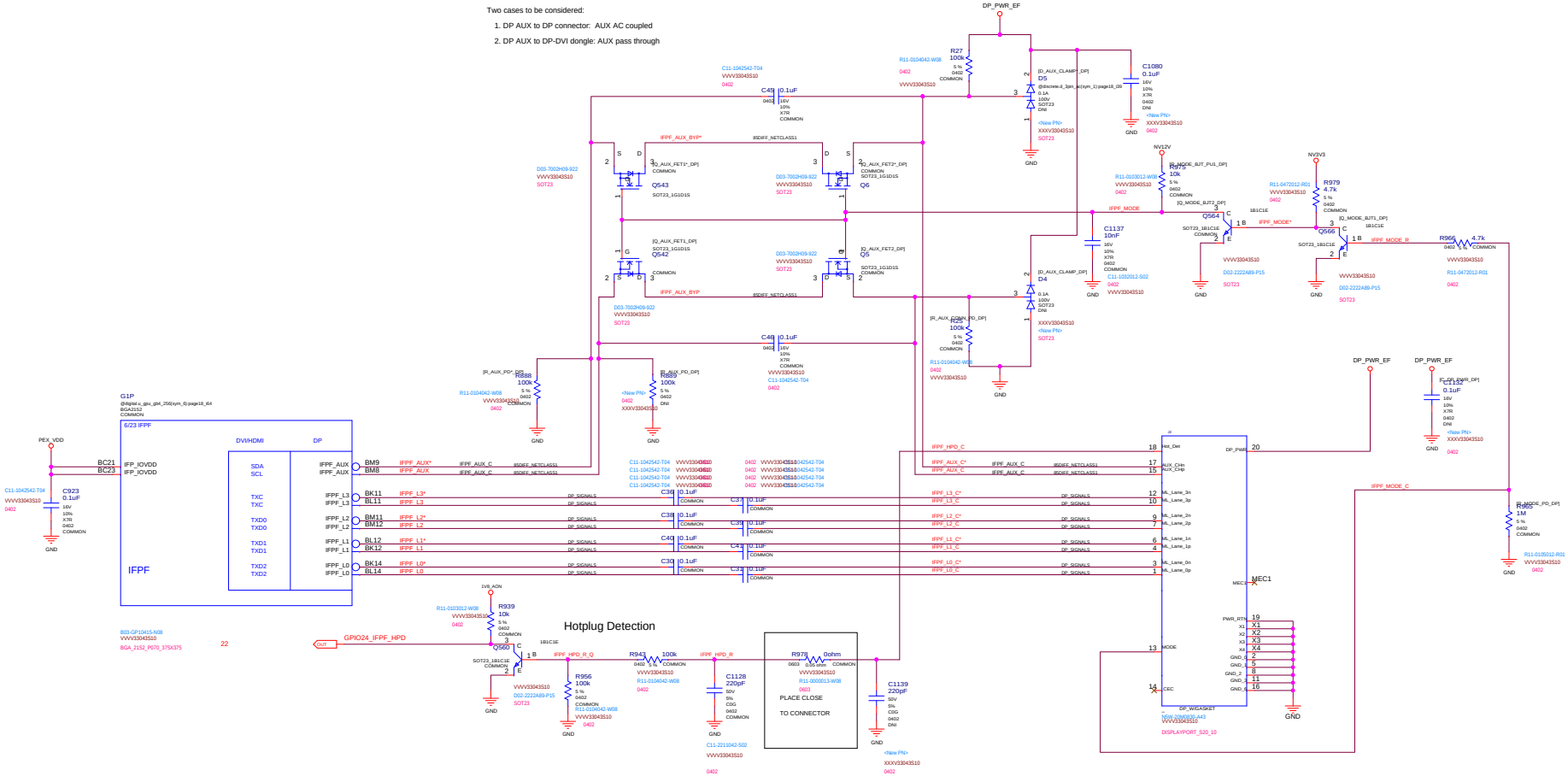
Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



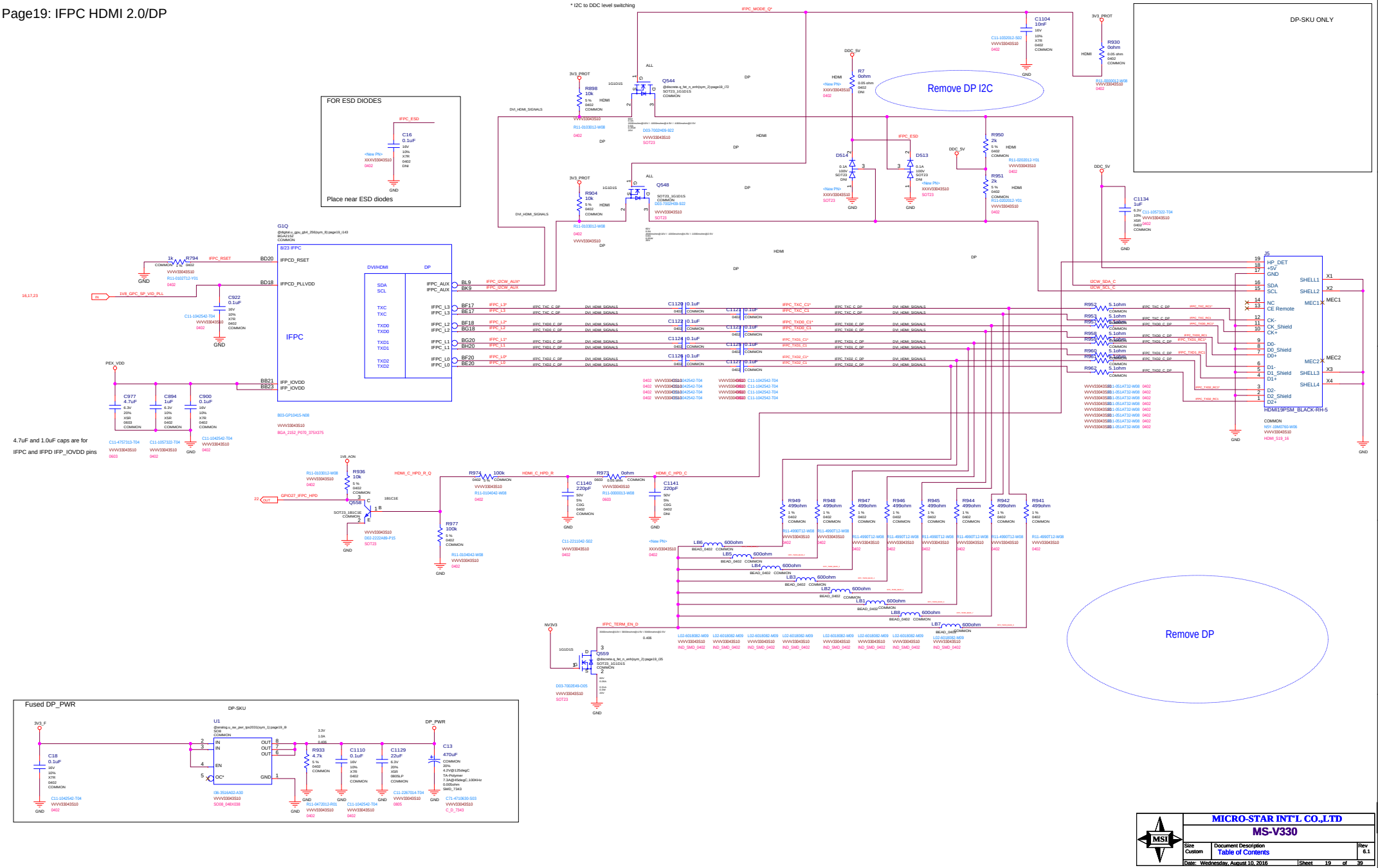
Project	MICRO-STAR INT'L CO.,LTD
	MS-V330
Size	Custom
Document Description	Table of Contents
Rev	6.1
Date:	Wednesday, August 10, 2016
Sheet	17 of 39

Page18: IFPF DP

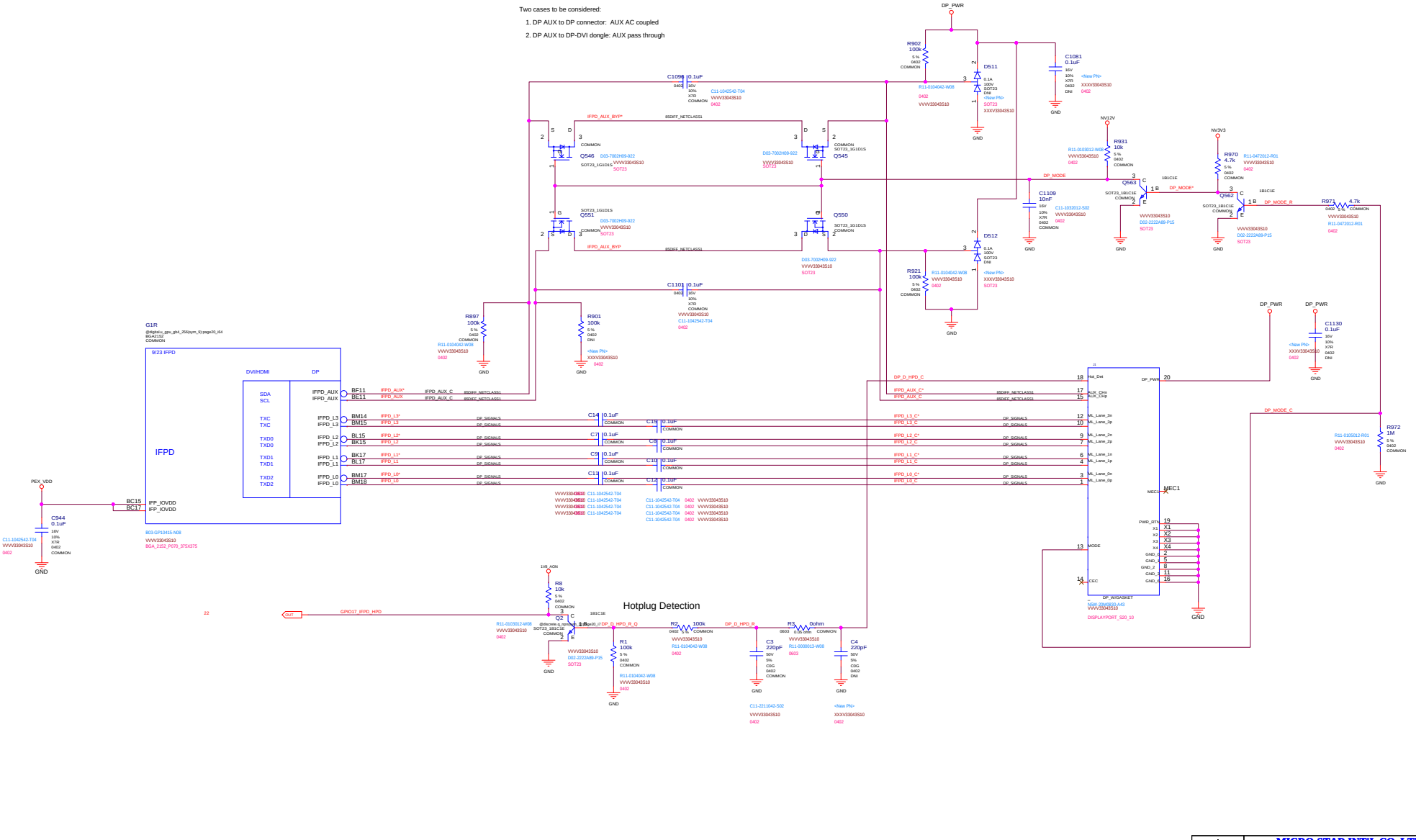


MICRO-STAR INT'L CO.,LTD	
MS-V330	
Size: Custom	Document Description: Table of Contents
Rev: 6.1	
Date: Wednesday, August 10, 2016	Sheet 18 of 39

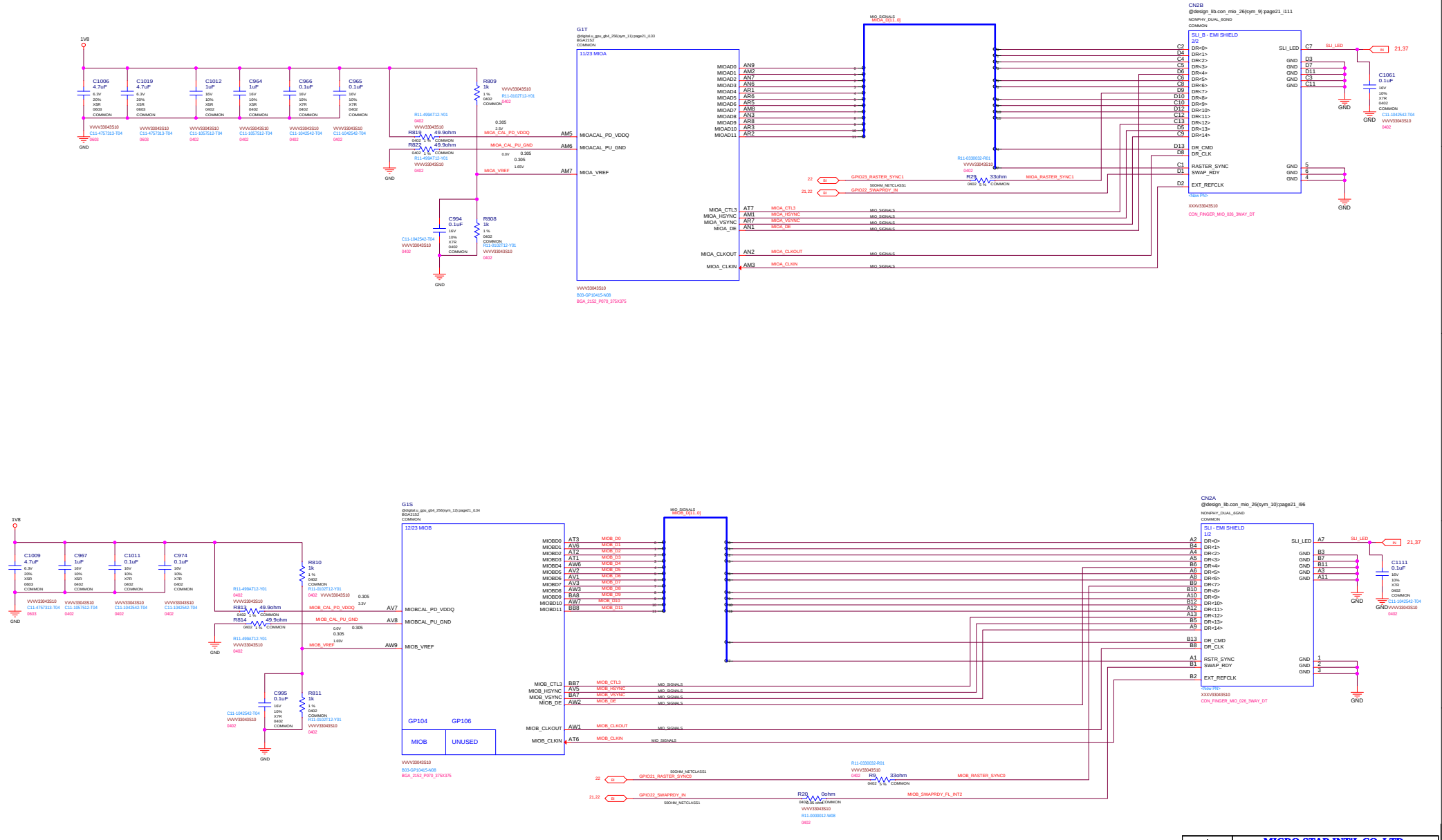
Page19: IFPC HDMI 2.0/DP



Page20: IFPD DP

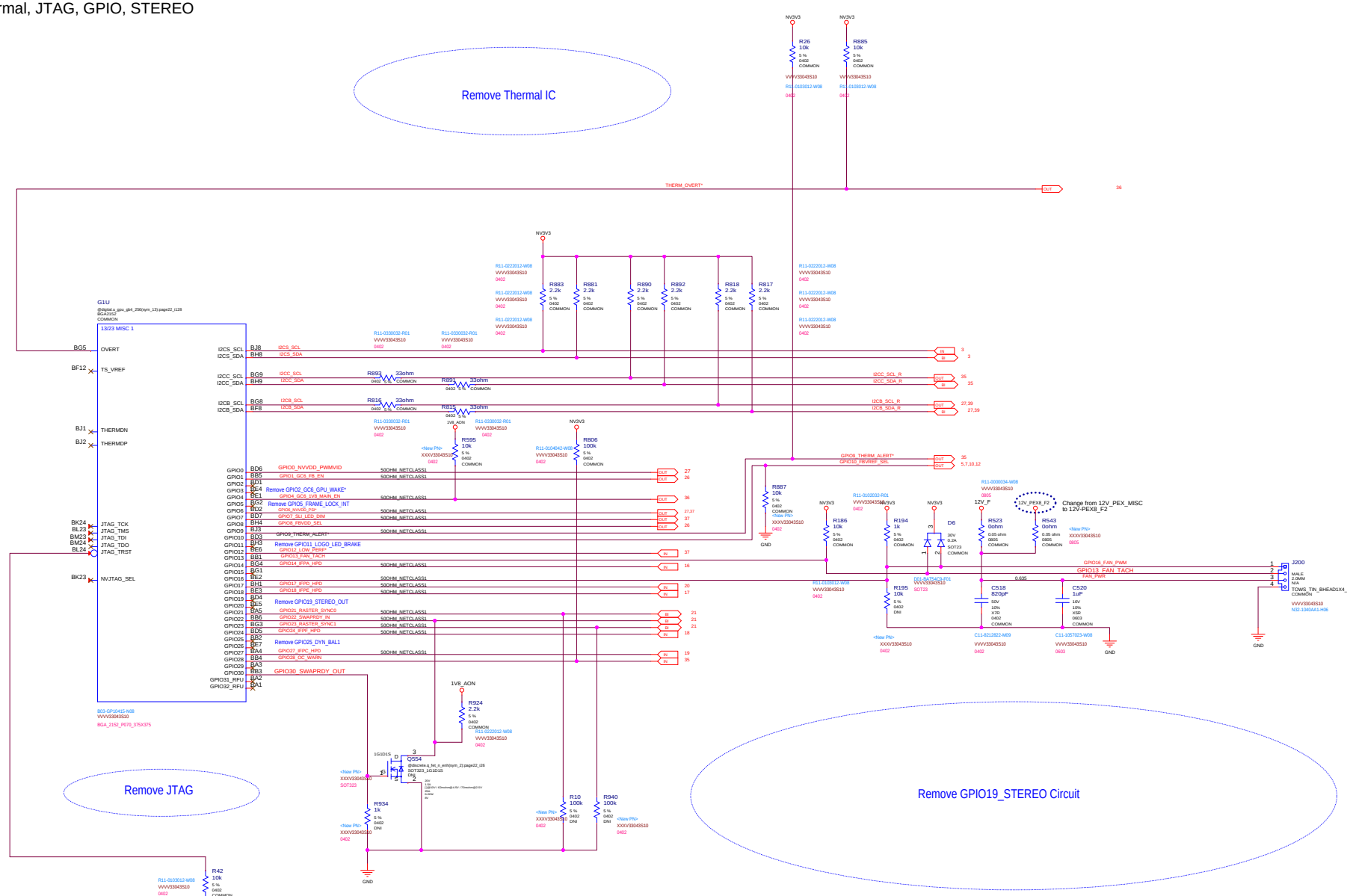


Page21: MIOA/B Interface and FRAME LOCK



MICRO-STAR INT'L CO.,LTD		
MS-V330		
Size: Custom	Document Description: Table of Contents	Rev: 6.1
Date: Wednesday, August 10, 2016	Sheet 21 of 39	

Page22: MISC1: Fan, Thermal, JTAG, GPIO, STEREO



MICRO-STAR INT'L CO.,LTD	
MS-V330	
Size: Custom	Document Description: Table of Contents
Rev: 6.1	
Date: Wednesday, August 10, 2016	Sheet 22 of 39

Page23: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

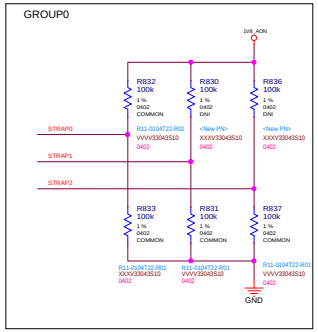
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

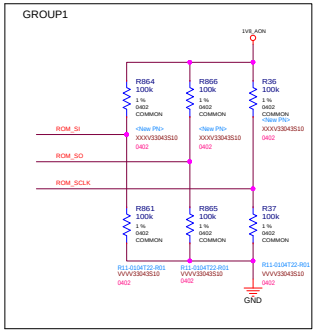
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

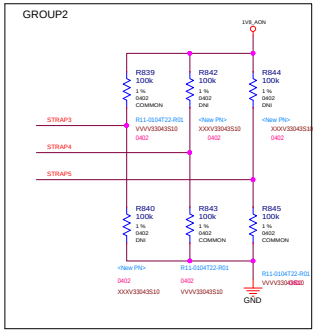
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

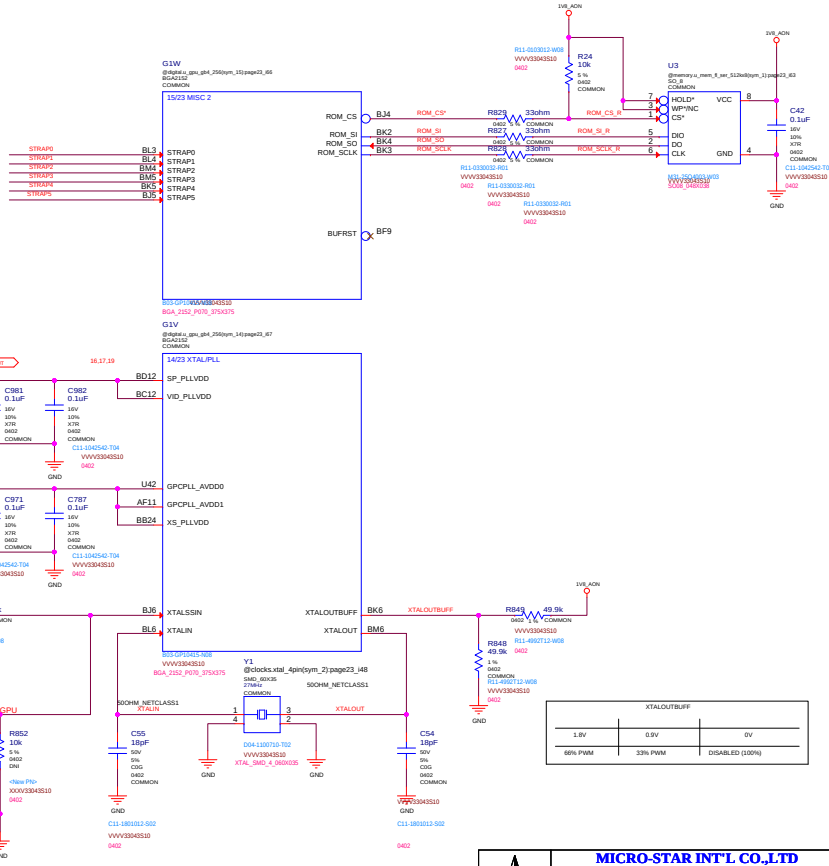
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE





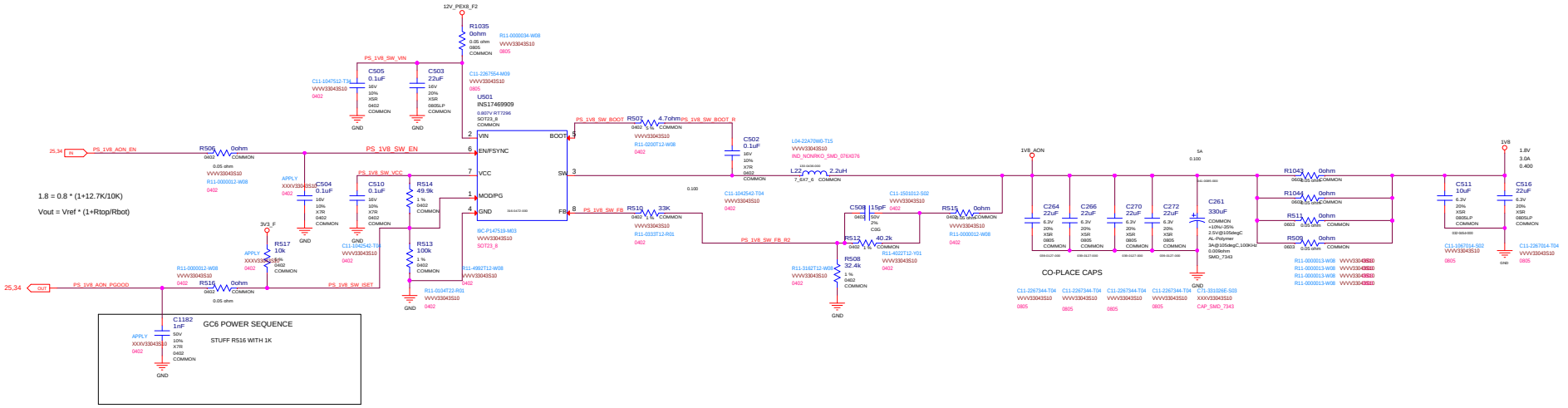


CFG[3:0]	Config Width	Vendor
0000	256Mx32 256-bit	Samsung
0001	256Mx32 256-bit	Micron
0010	256Mx32 256-bit	Hynix
0011	Reserved	
0100	Reserved	
0101	Reserved	
0110	Reserved	
0111	Reserved	

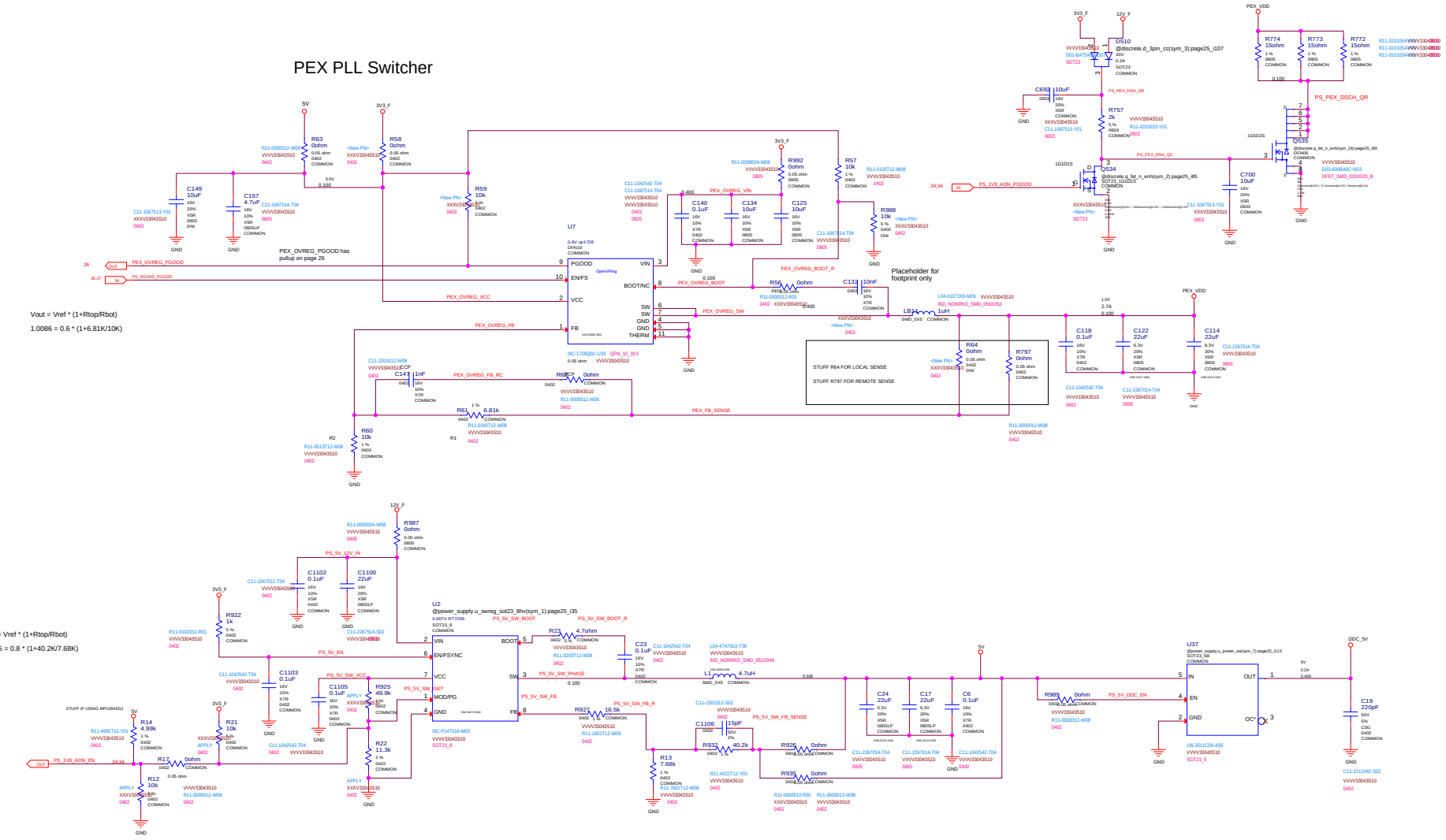


MICRO-STAR INT'L CO.,LTD		
MS-V330		
Size: Custom	Document Description: Table of Contents	Rev: 6.1
Date: Wednesday, August 10, 2016	Sheet 23 of 39	

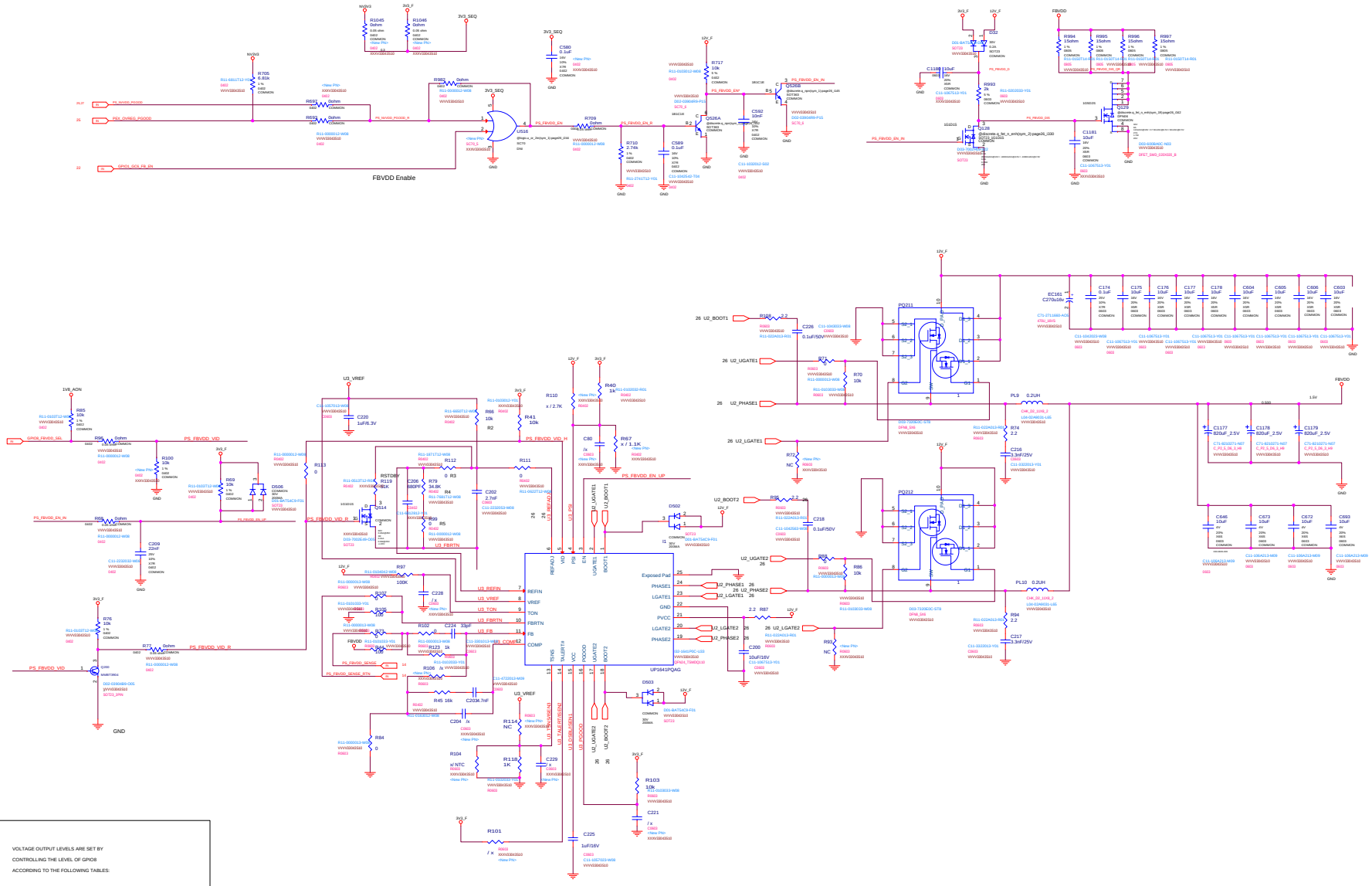
Page24: PS: 1V8, 1V8_AON



MSI	MICRO-STAR INT'L CO.,LTD
	MS-V330
Size: Custom	Document Description: Table of Contents
Rev: 6.1	
Date: Wednesday, August 10, 2016	Sheet 24 of 39


PEX PLL Switcher
Vout = Vref * (1+Rtop/Rbot)
1.0086 = 0.6 * (1+6.81K/10K)
PEX_OVREG_PGOOD has pullup on page 26
Placeholder for footprint only
STUFF R64 FOR LOCAL SENSE
STUFF R797 FOR REMOTE SENSE
Vout = Vref * (1+Rtop/Rbot)
4.9875 = 0.8 * (1+40.2K/7.68K)

Page26: PS: FBVDD



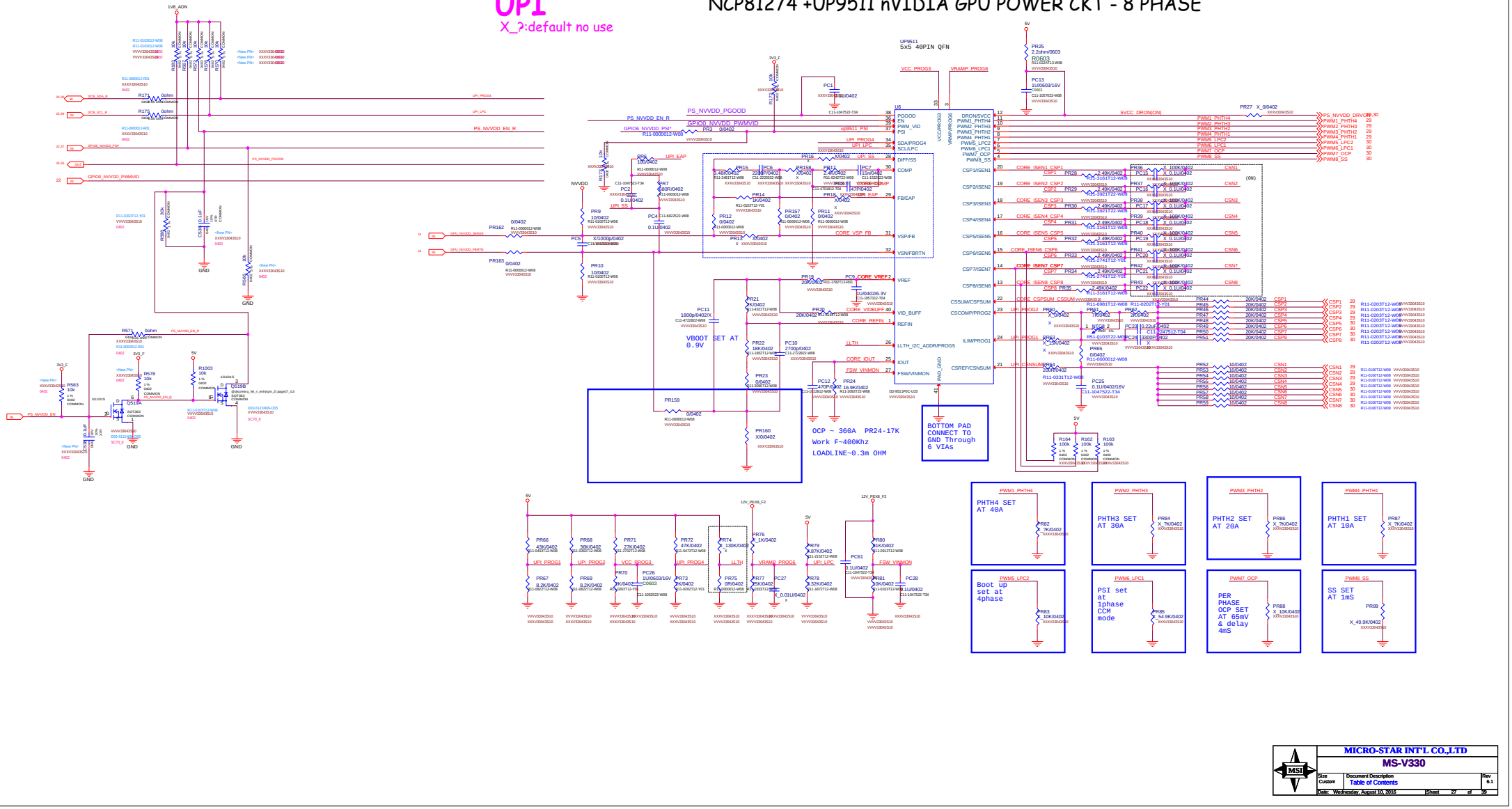
GPIO8 LEVEL	FBVDD OUTPUT VOLTAGE
0	1.35V
1	1.55V

MICRO-STAR INT'L CO.,LTD
MS-V330
Size D
Document Description
Table of Contents
Rev 6.1
Date: Wednesday, August 10, 2016
Sheet 26 of 39

UPI

X_?:default no use

NCP81274 +UP9511 nVIDIA GPU POWER CKT - 8 PHASE

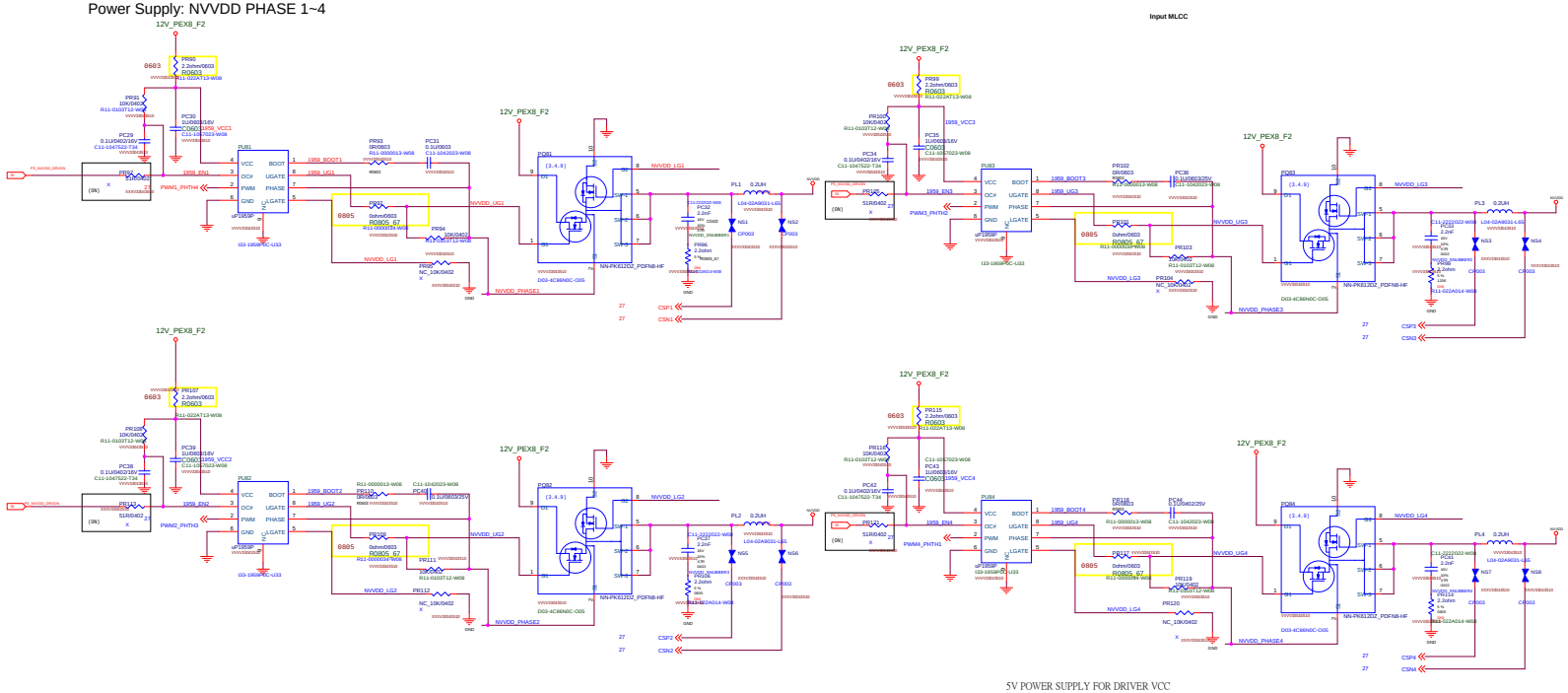


MICRO-STAR INT'L CO.,LTD		
MS-V330		
Size: Custom	Document Description: Table of Contents	Rev: 6.1
Date: Wednesday, August 10, 2016	Sheet: 27 of 39	

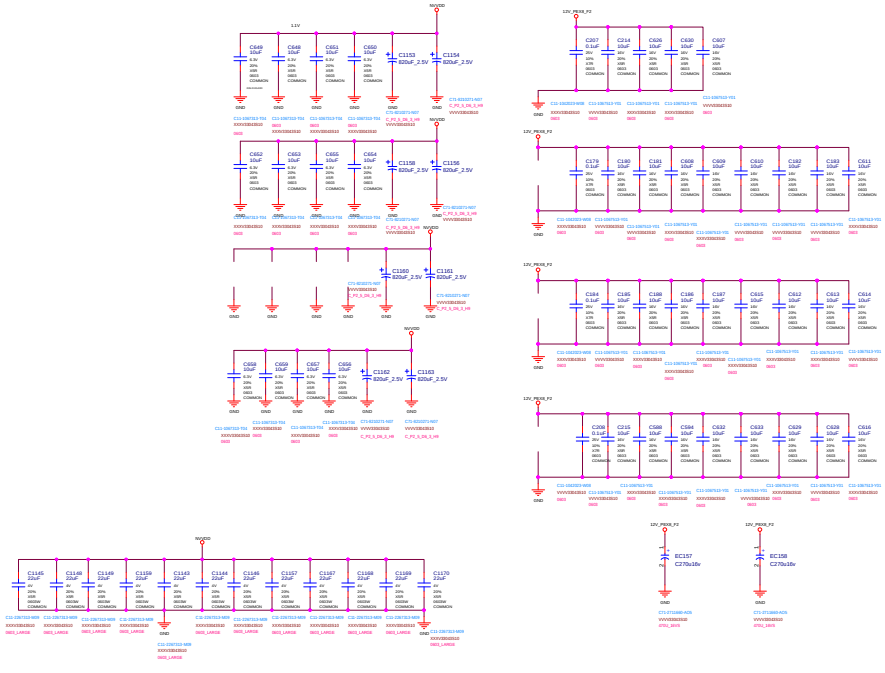
Page28: PS: Blank Page

MICRO-STAR INT'L CO.,LTD	
MS-V330	
Size: Custom	Document Description: Table of Contents
Rev: 6.1	
Date: Wednesday, August 10, 2016	Sheet 28 of 39

Power Supply: NVVDD PHASE 1~4



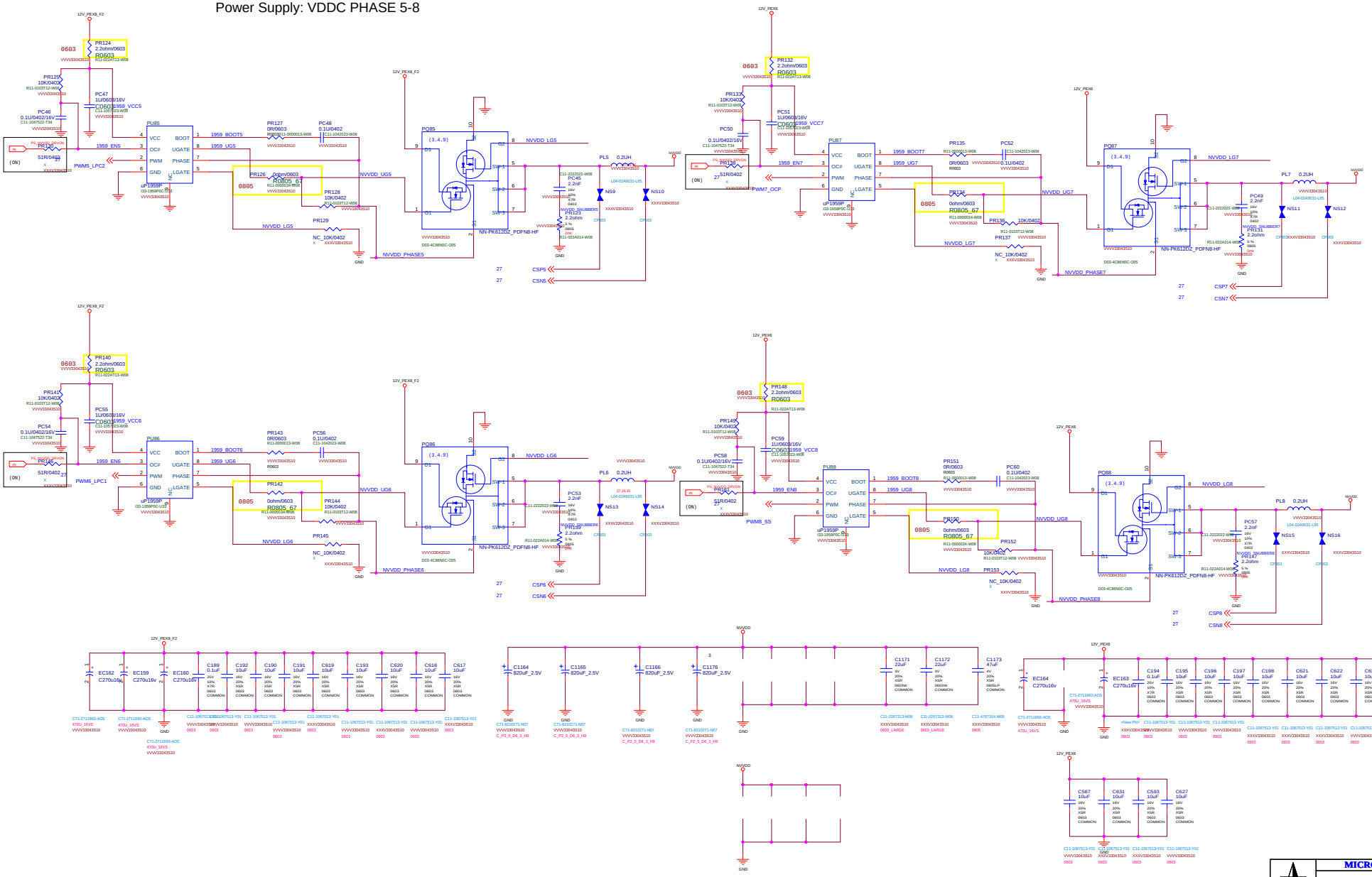
5V POWER SUPPLY FOR DRIVER VCC



MICRO-STAR INT'L CO.,LTD		
MS-V330		
Size: Custom	Document Description: Table of Contents	Rev: 0.1
Date: Wednesday, August 10, 2016	Sheet 29 of 39	

Page30: PS: NVVDD Phase 5 ~8

Power Supply: VDDC PHASE 5-8



MICRO-STAR INT'L CO.,LTD	
MS-V330	
Size: Custom	Document Description: Table of Contents
Rev: 6.1	
Date: Wednesday, August 10, 2016	Sheet 30 of 39

Page31: PS: Blank Page

MICRO-STAR INT'L CO.,LTD	
MS-V330	
Size: Custom	Document Description: Table of Contents
Rev: 6.1	
Date: Wednesday, August 10, 2016	Sheet 31 of 39

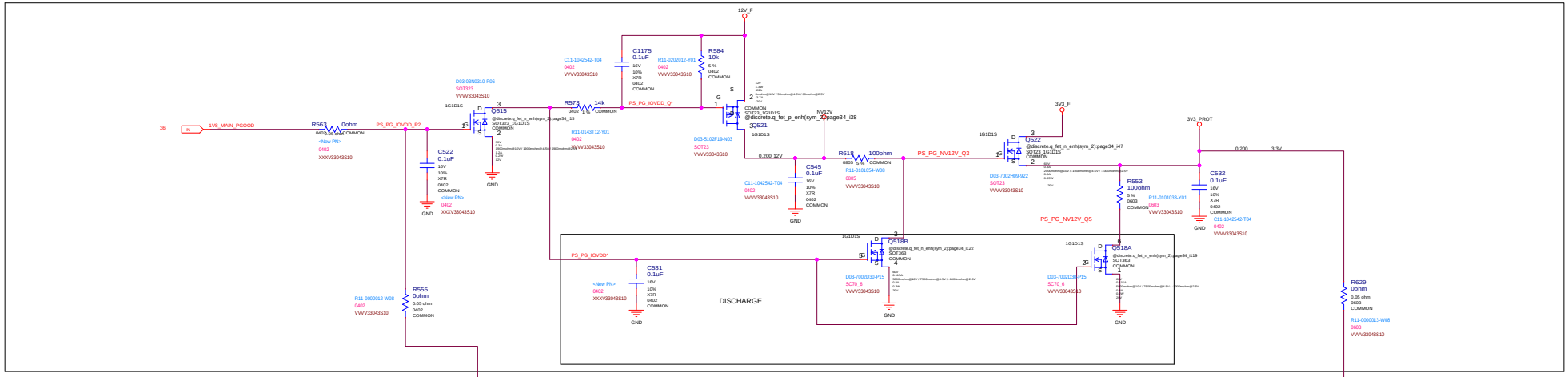
Page32: PS: Dynamic Power Balance Phases

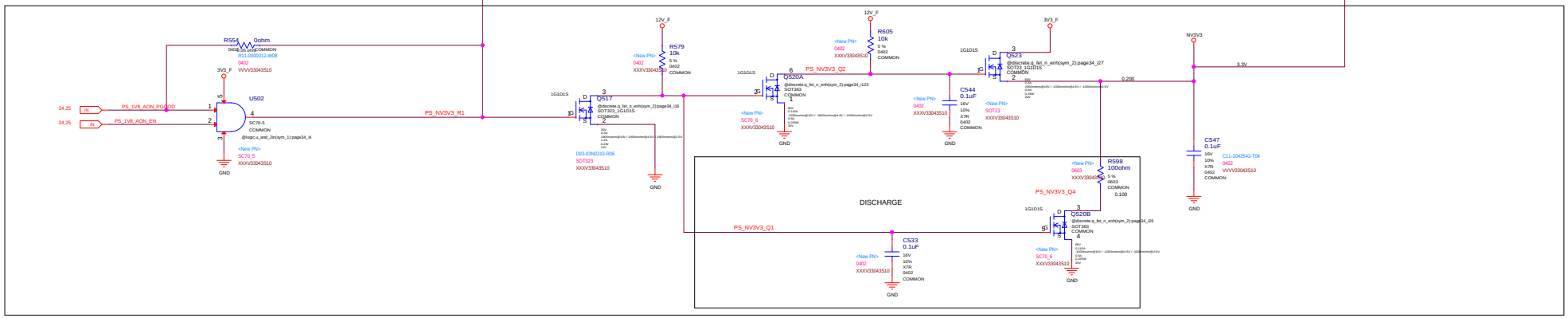
MICRO-STAR INT'L CO.,LTD	
MS-V330	
Size: Custom	Document Description: Table of Contents
Rev: 6.1	
Date: Wednesday, August 10, 2016	Sheet 32 of 39

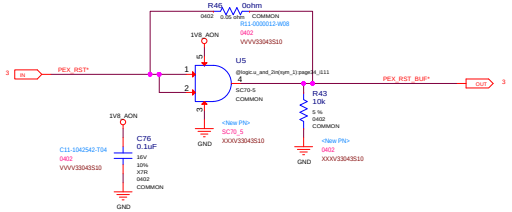
Page33: PS: Dynamic Power Balance Logic

MICRO-STAR INT'L CO.,LTD	
MS-V330	
Size: Custom	Document Description: Table of Contents
Rev: 6.1	
Date: Wednesday, August 10, 2016	Sheet 33 of 39

Page34:PS: NV3V3, NV12V

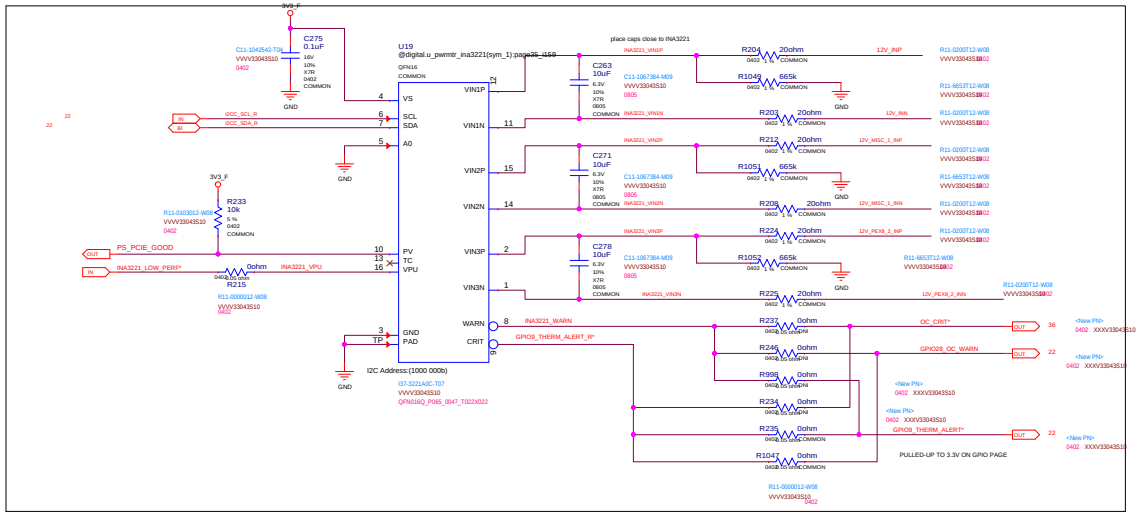




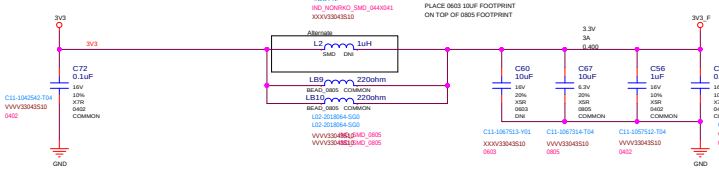


MICRO-STAR INT'L CO.,LTD		
MS-V330		
Size: Custom	Document Description: Table of Contents	Rev: 6.1
Date: Wednesday, August 10, 2016	Sheet 34 of 39	

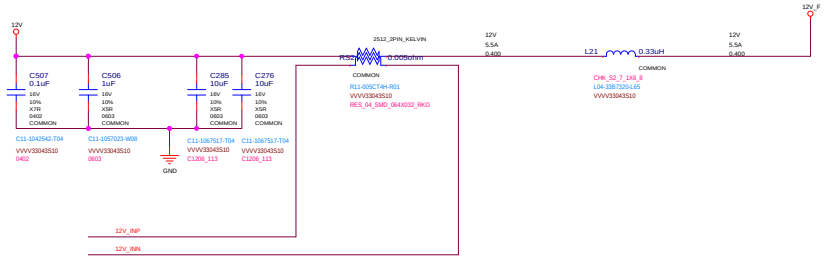
Page35: PS: Inputs, Filtering, and Monitoring



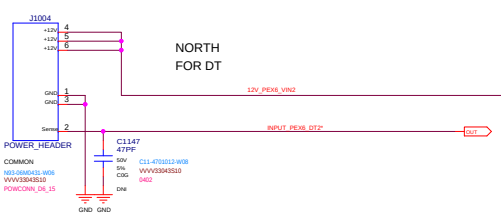
PEX 3V3 INPUT - 10W



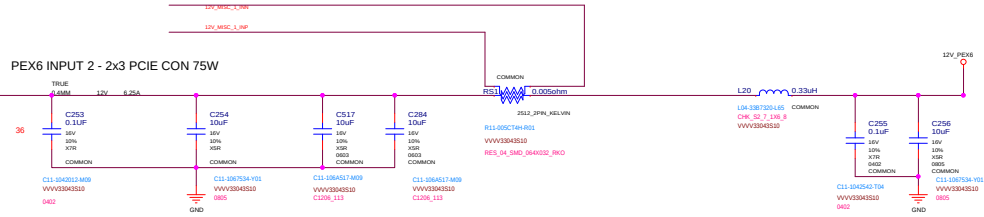
PEX_12V INPUT - 66W



NORTH FOR DT

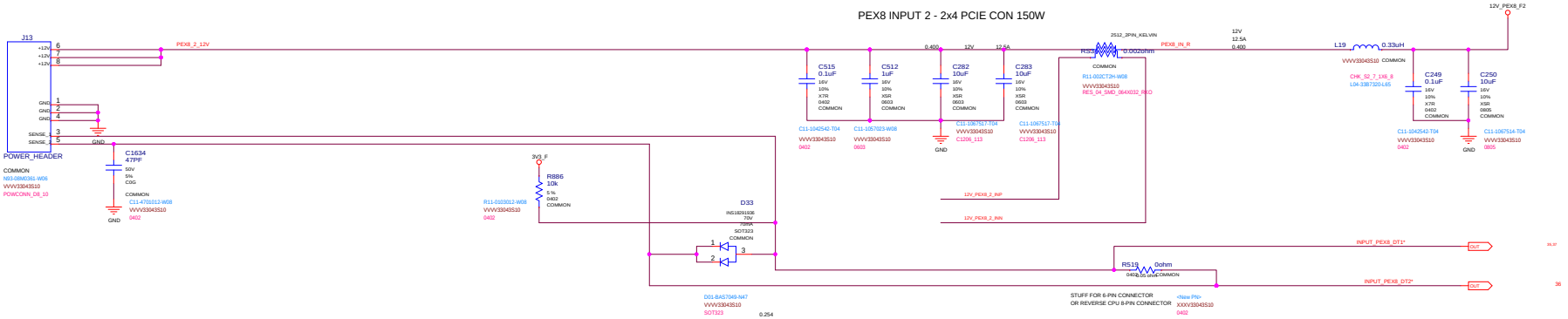


PEX6 INPUT 2 - 2x3 PCIE CON 75W

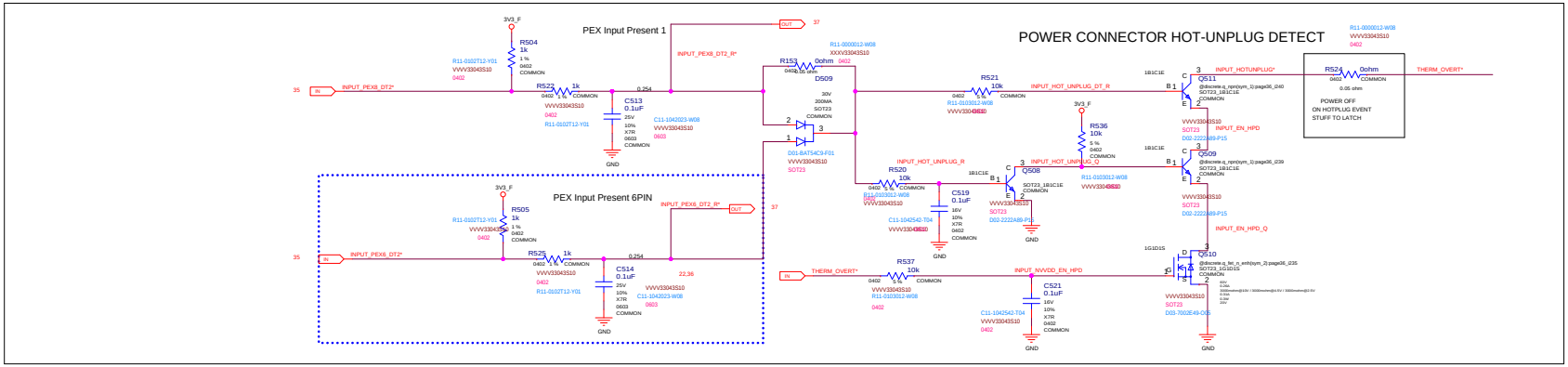


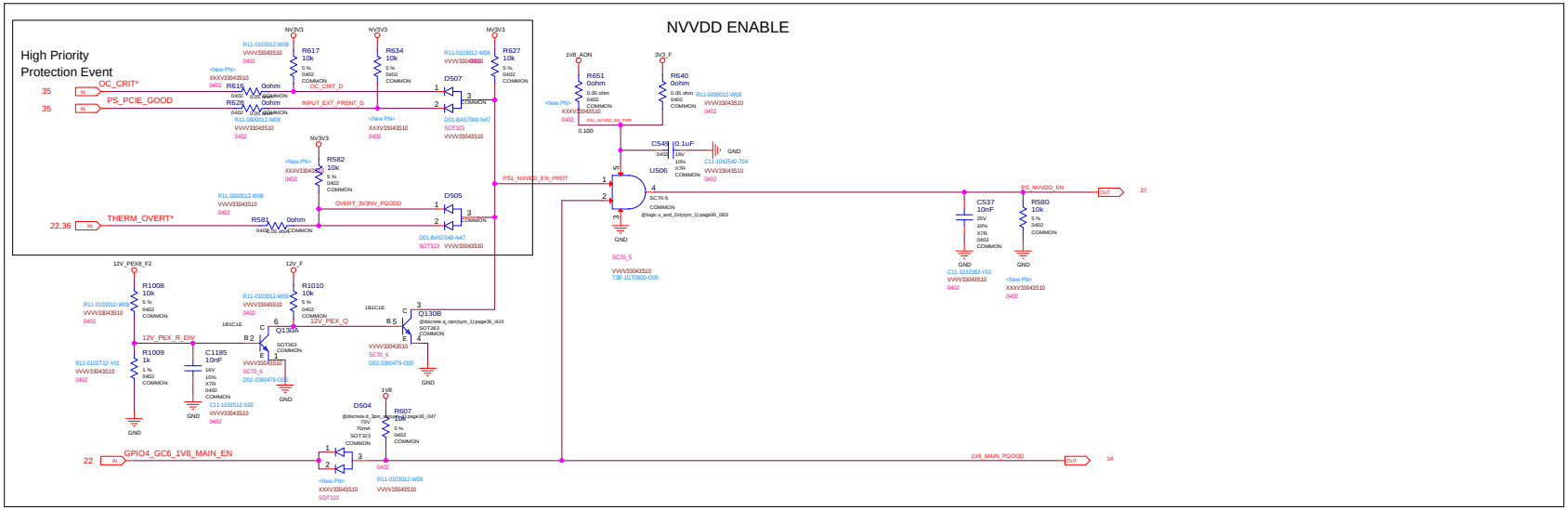
PLACE ON NORTH SIDE

PEX8 INPUT 2 - 2x4 PCIE CON 150W



Page36: PS: Shutdown and Sequencing

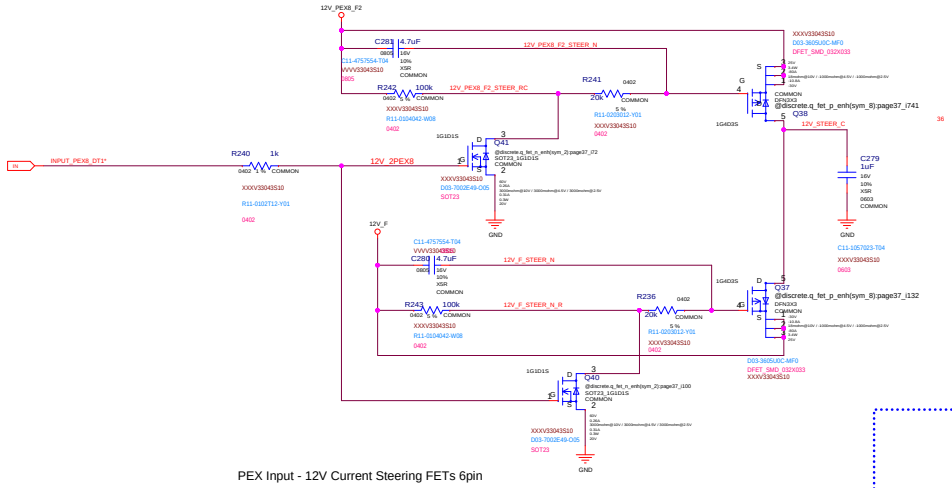




MICRO-STAR INT'L CO.,LTD			
MS-V330			
Size: Custom	Document Description: Table of Contents		Rev: 6.1
Date: Wednesday, August 10, 2016	Sheet 36 of 39		

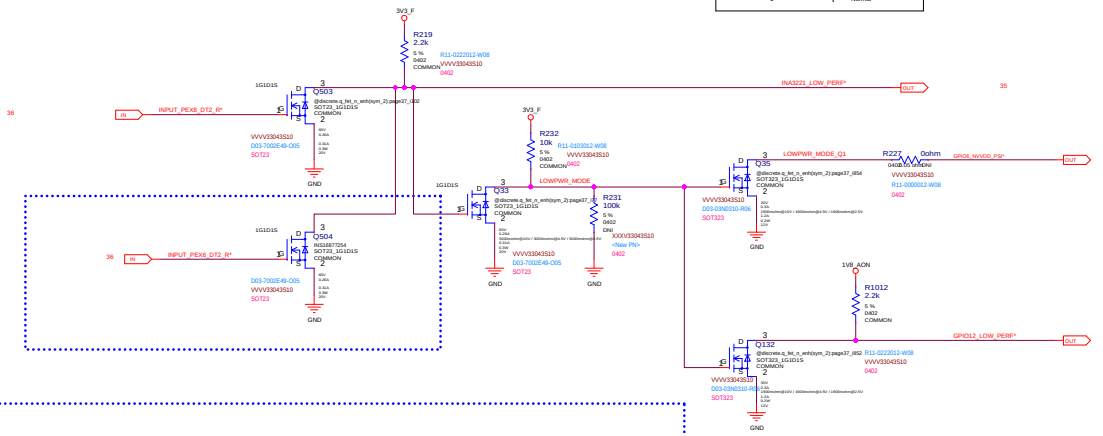
Page37: PS: 12V Current Steering, PSI Control, and LED

PEX Input - 12V Current Steering FETs 8pin



PEX Input - 12V Current Steering FETs 6pin

PEX Input - Power Level/PSI* Control

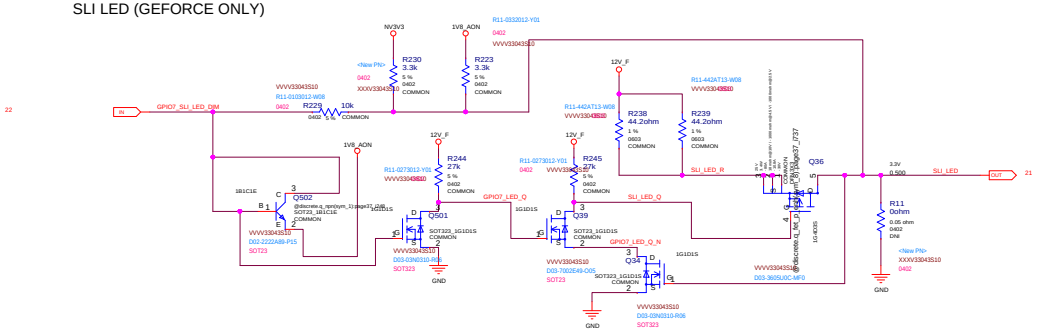


GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

Remove POWER BRAKE

POWER BRAKE

SLI LED (GEFORCE ONLY)



GeForce Logo LED

MICRO-STAR INT'L CO.,LTD

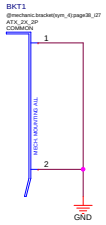
MS-V330

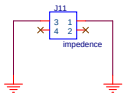
Size	Document Description	Rev
Custom	Table of Contents	6.1

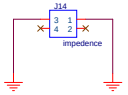
Date: Wednesday, August 10, 2016 Sheet 37 of 39

Page38: Mechanical: Bracket/Thermal Solution

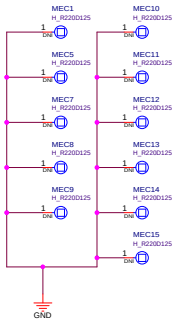
Brackets:



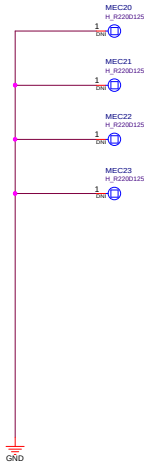


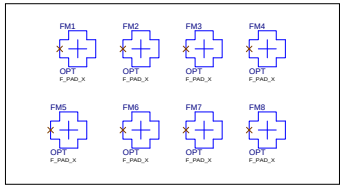


Mechanical Holes Symbol



GPU Stiffner





MICRO-STAR INT'L CO.,LTD		
MS-V330		
Size: Custom	Document Description: Table of Contents	Rev: 6.1
Date: Wednesday, August 10, 2016	Sheet 38 of 39	