PG410 A01

GP106 8GB/4GB GDDR5, 256b, 256Mx32/128MX32
Tall DVI-D + DP + DP + HDMI + HDMI

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V330-7.0 改 PG41 0版
1 增加生手印
2.PEX 改 LDO
3.NVVDD/FBVDD 改
4.改 FP C 为 HDMI

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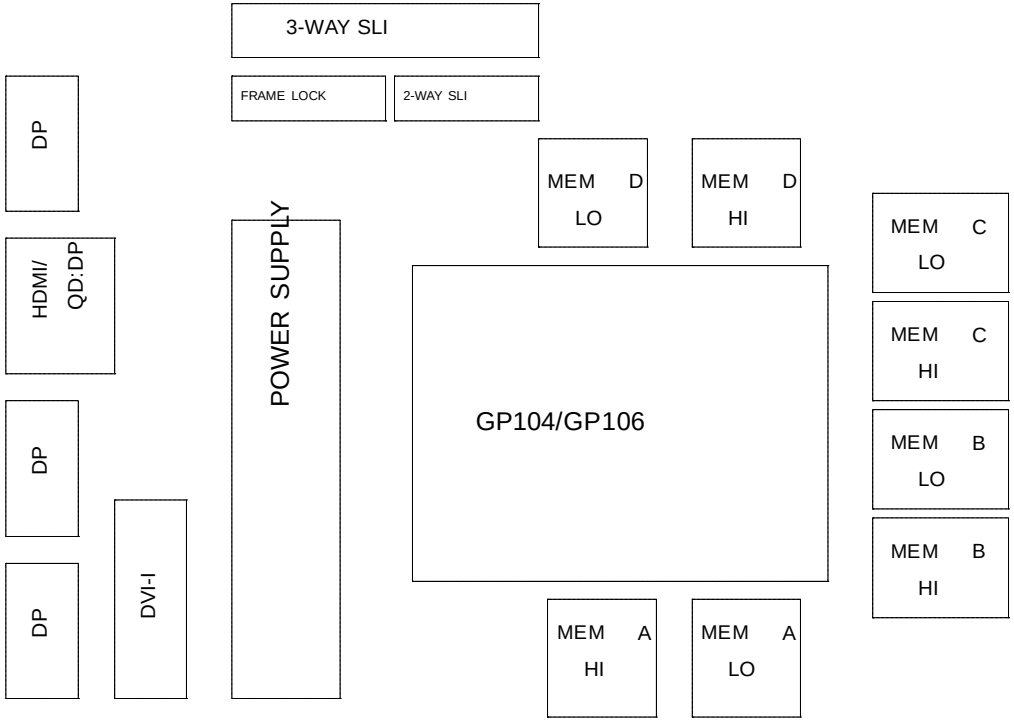
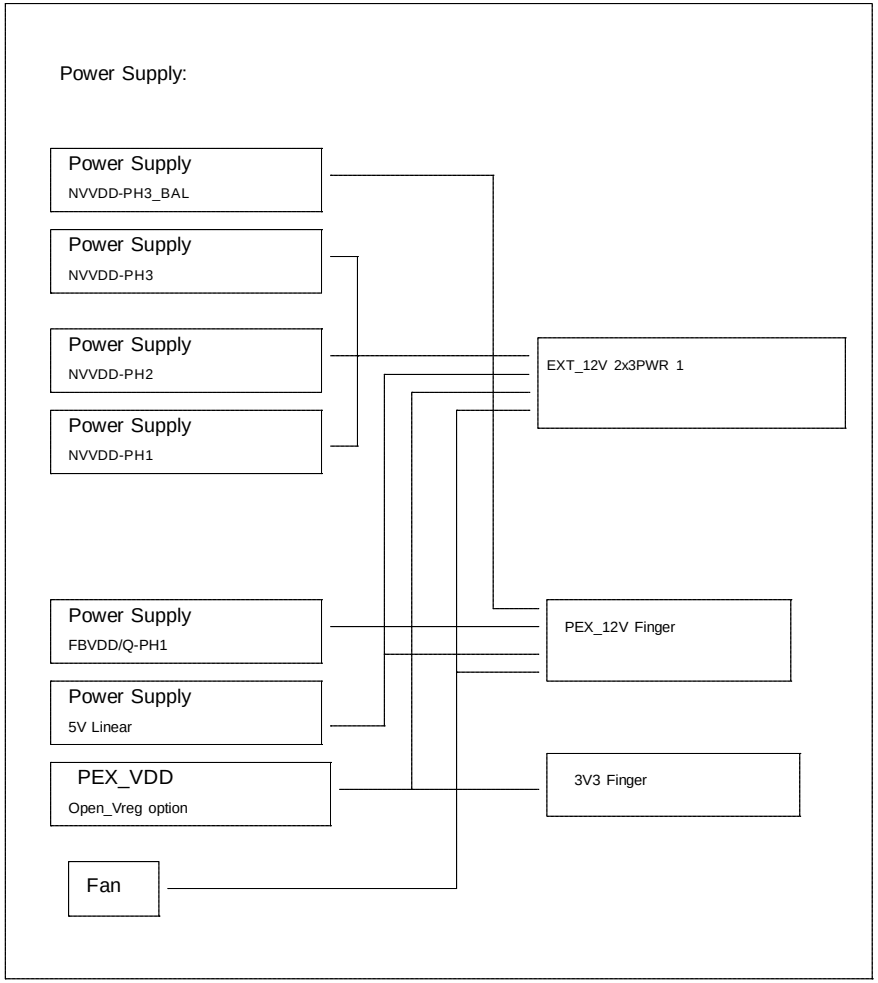
Page2: Block Diagram





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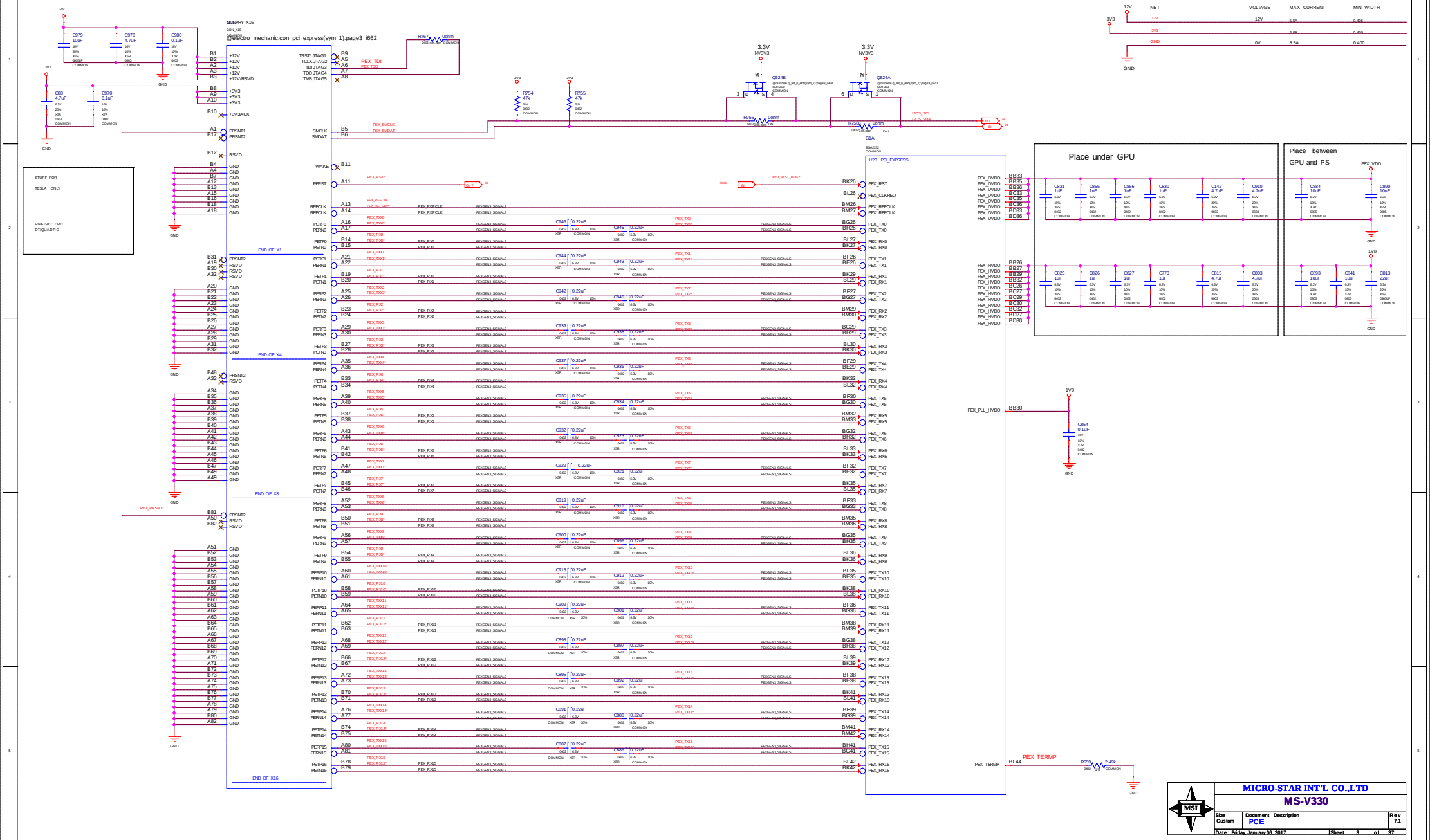
Page3: PCI Express

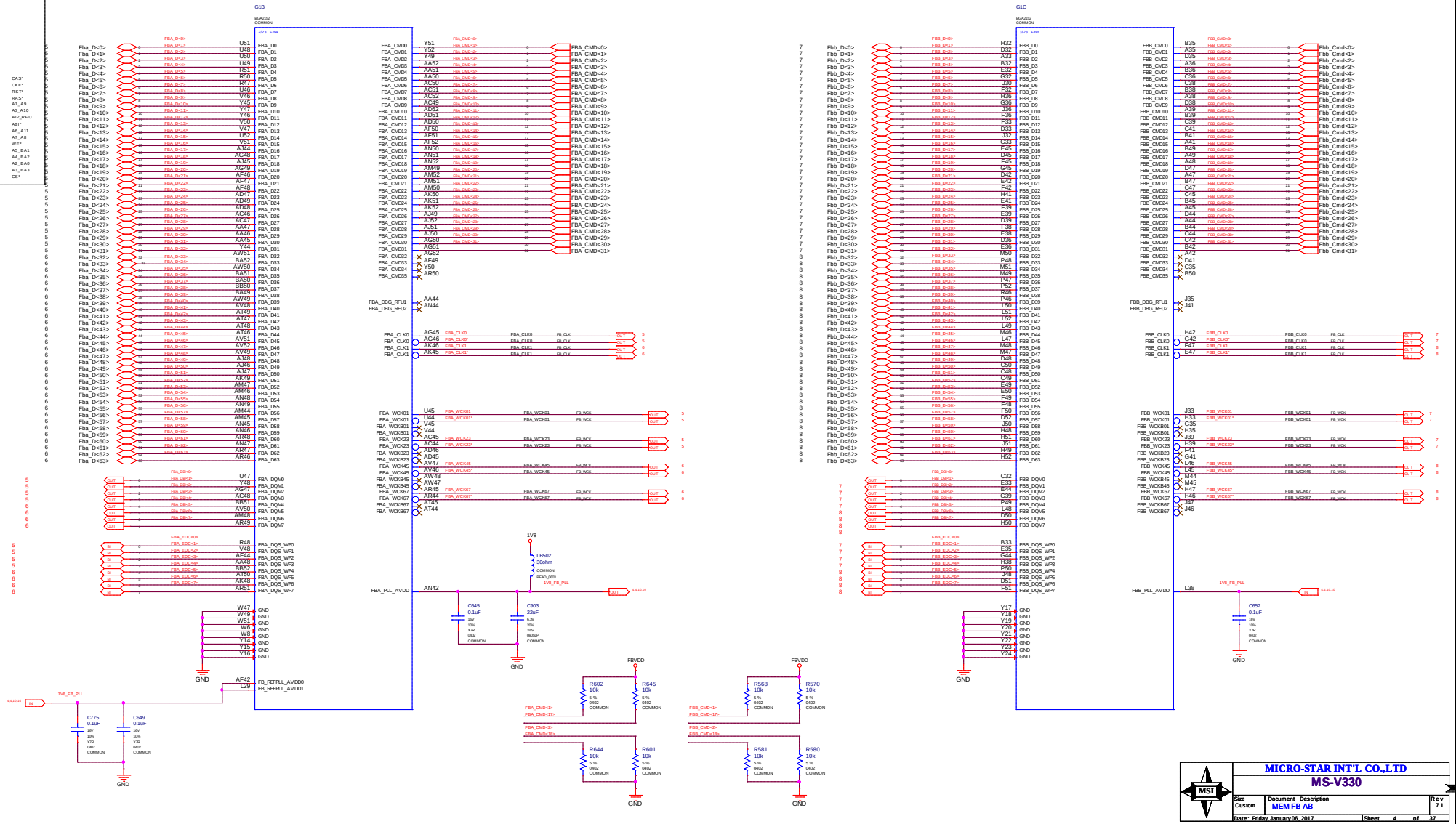


Page4: MEMORY: GPU Partition A/B

Page4: MEMORY: GPU Partition A/B

GDDR5 CMD Mapping

CMD	9_31	32_63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	AB1*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		AB1*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*



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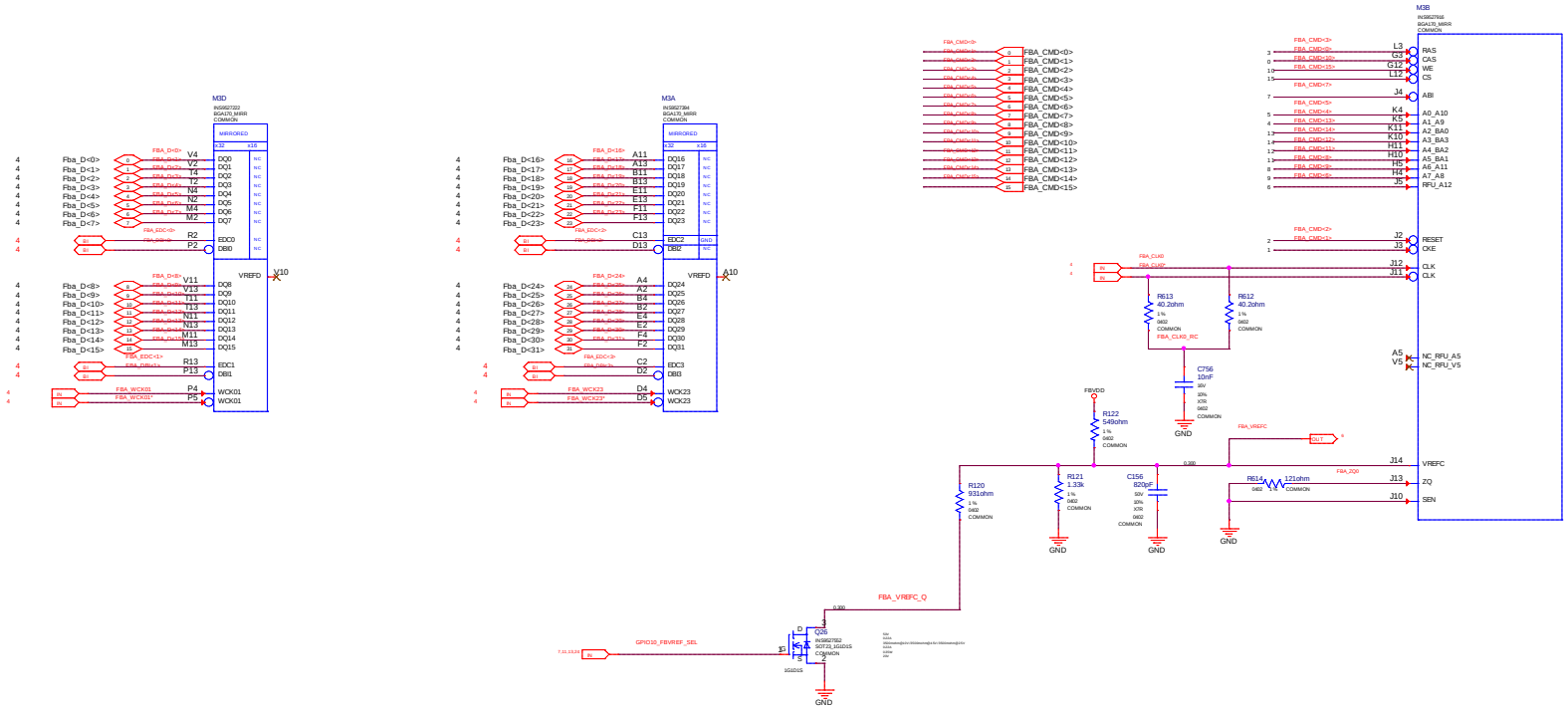
Page5: FRAME BUFFER PARTITION A [31:0]



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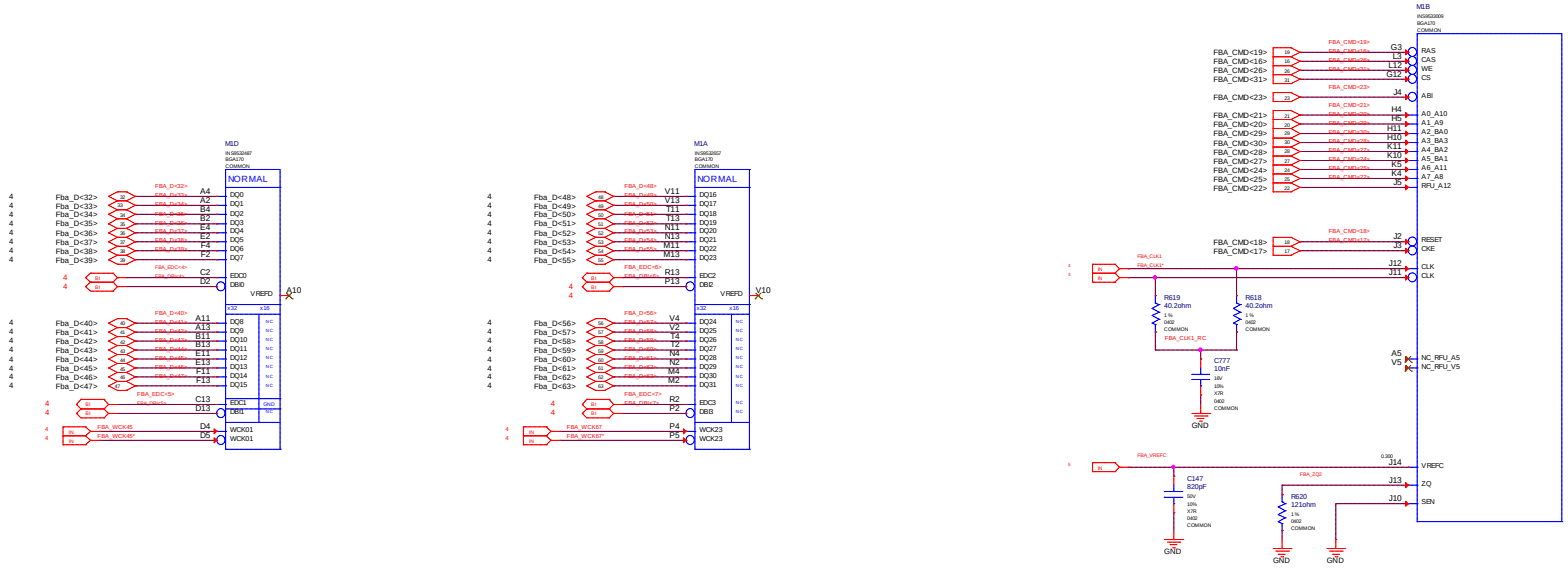
Page6: FRAME BUFFER PARTITION A [63:32]



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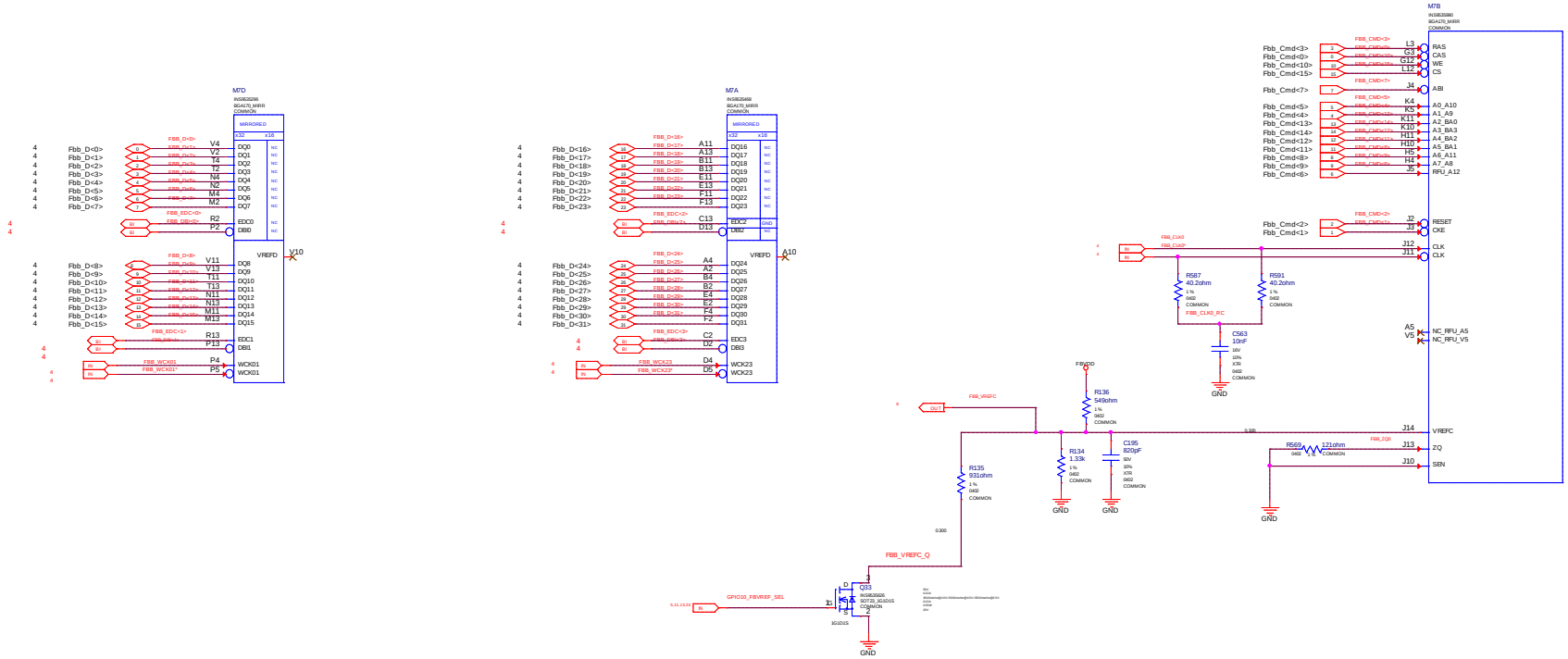
Page7: FRAME BUFFER PARTITION B [31:0]



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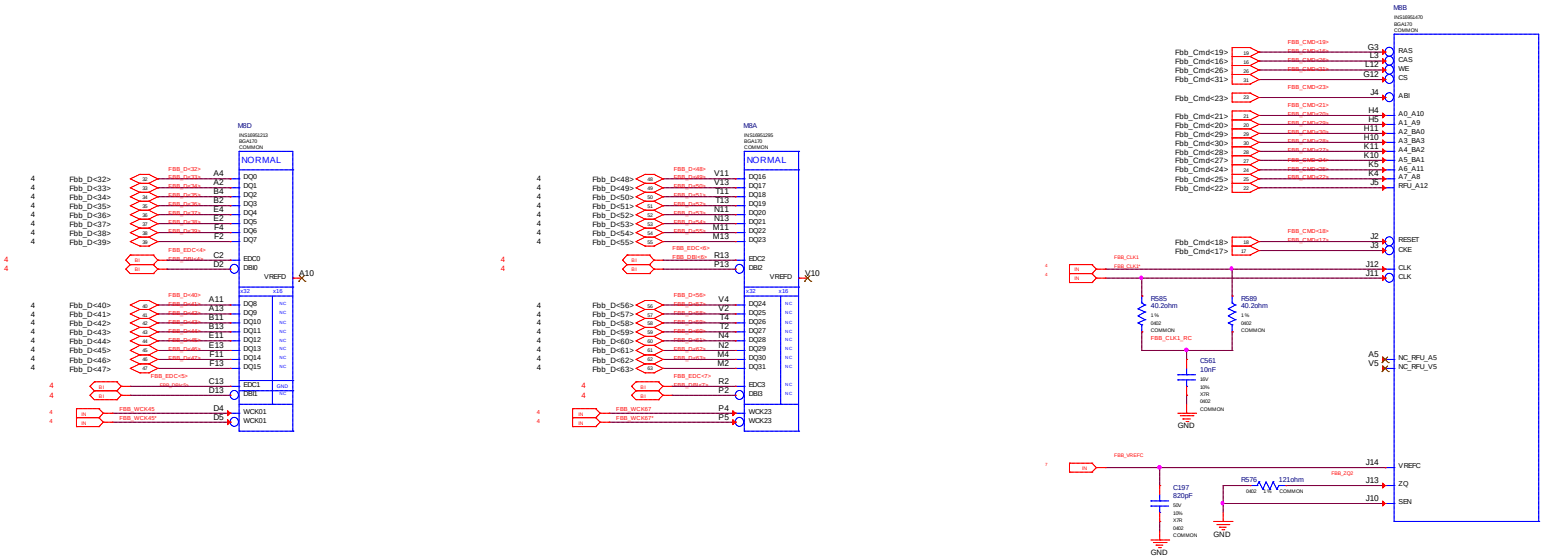
Page8: FRAME BUFFER PARTITION B [63:32]



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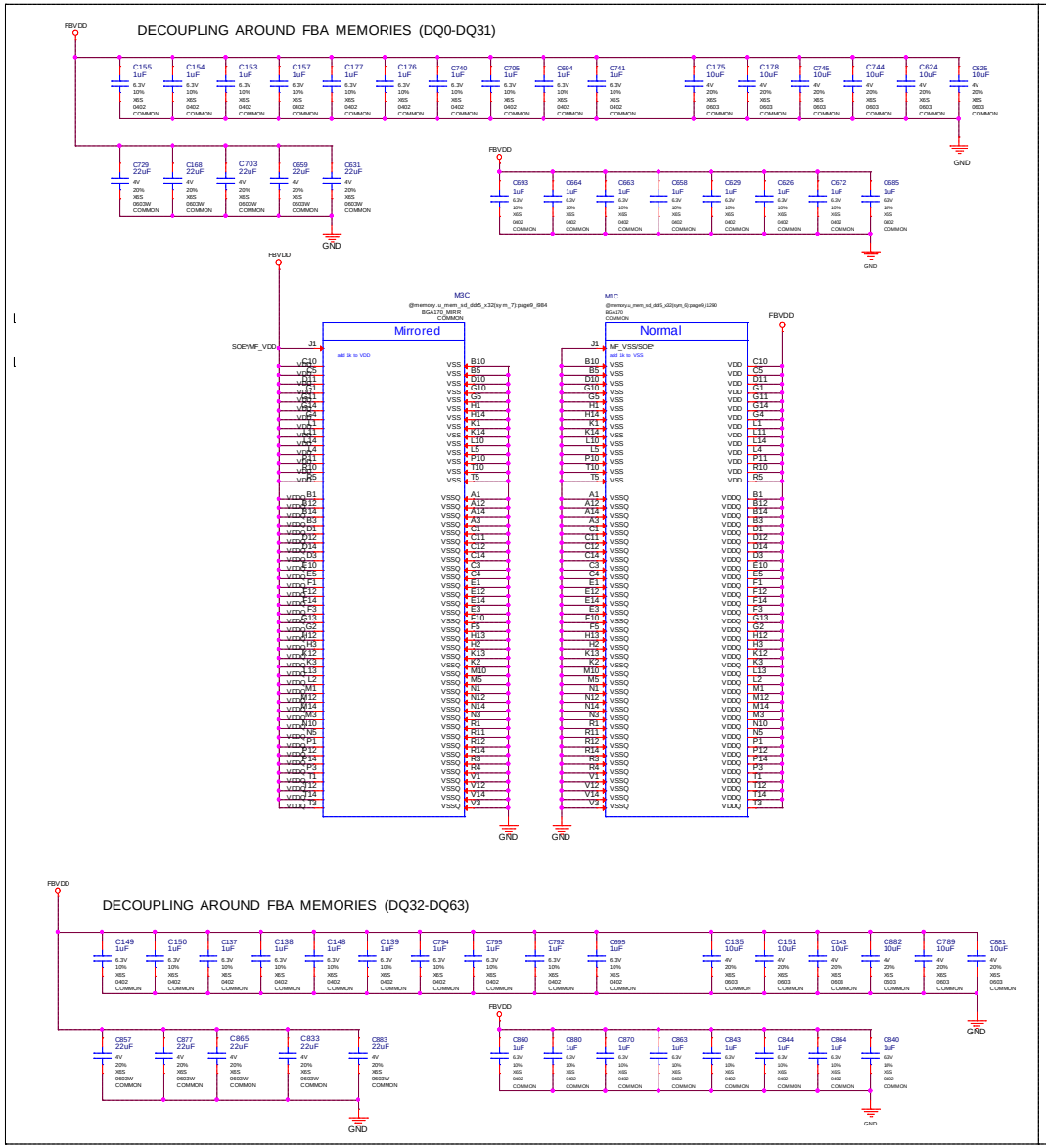
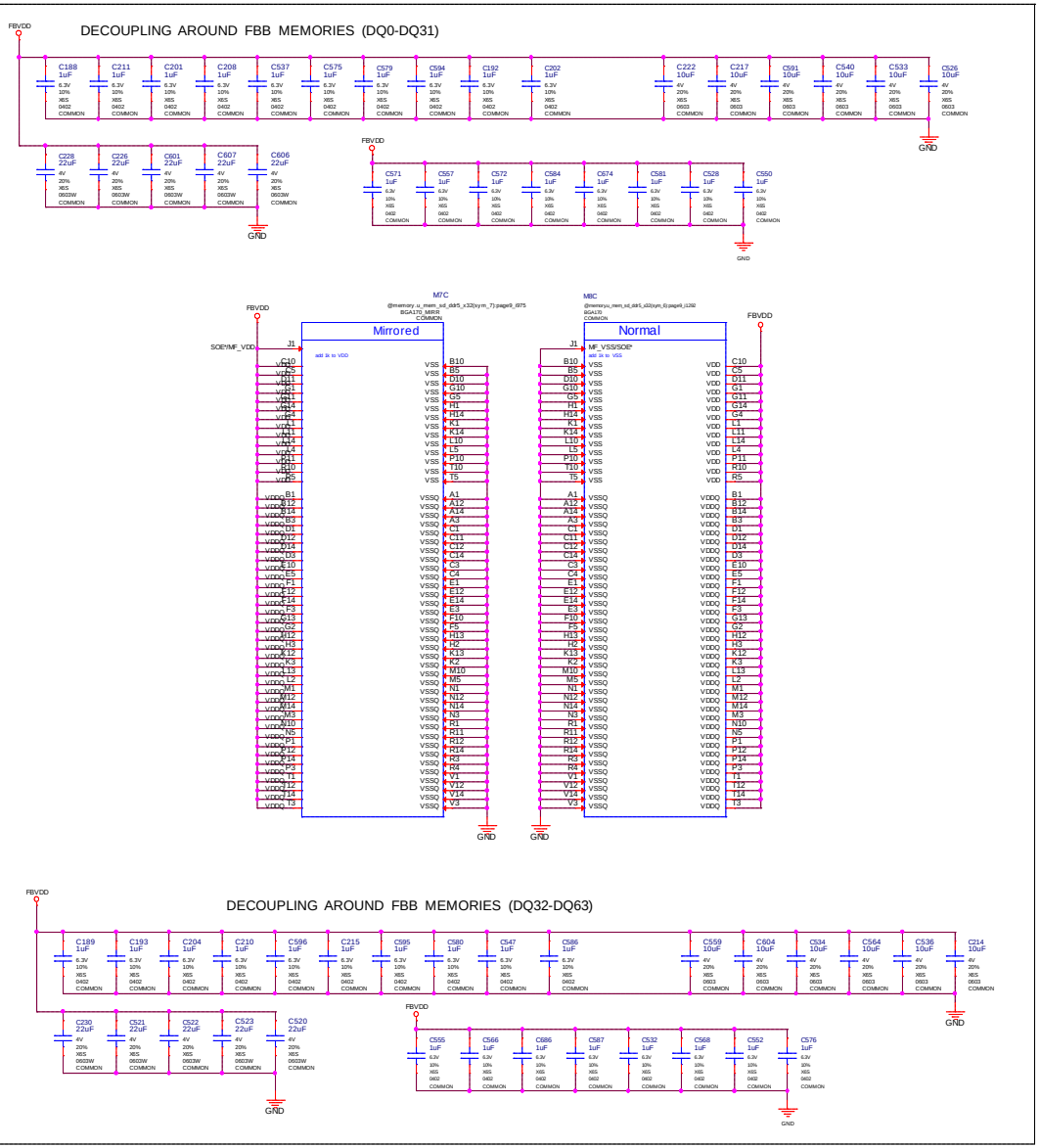
Page9: FRAME BUFFER PARTITION A/B DECOUPLING





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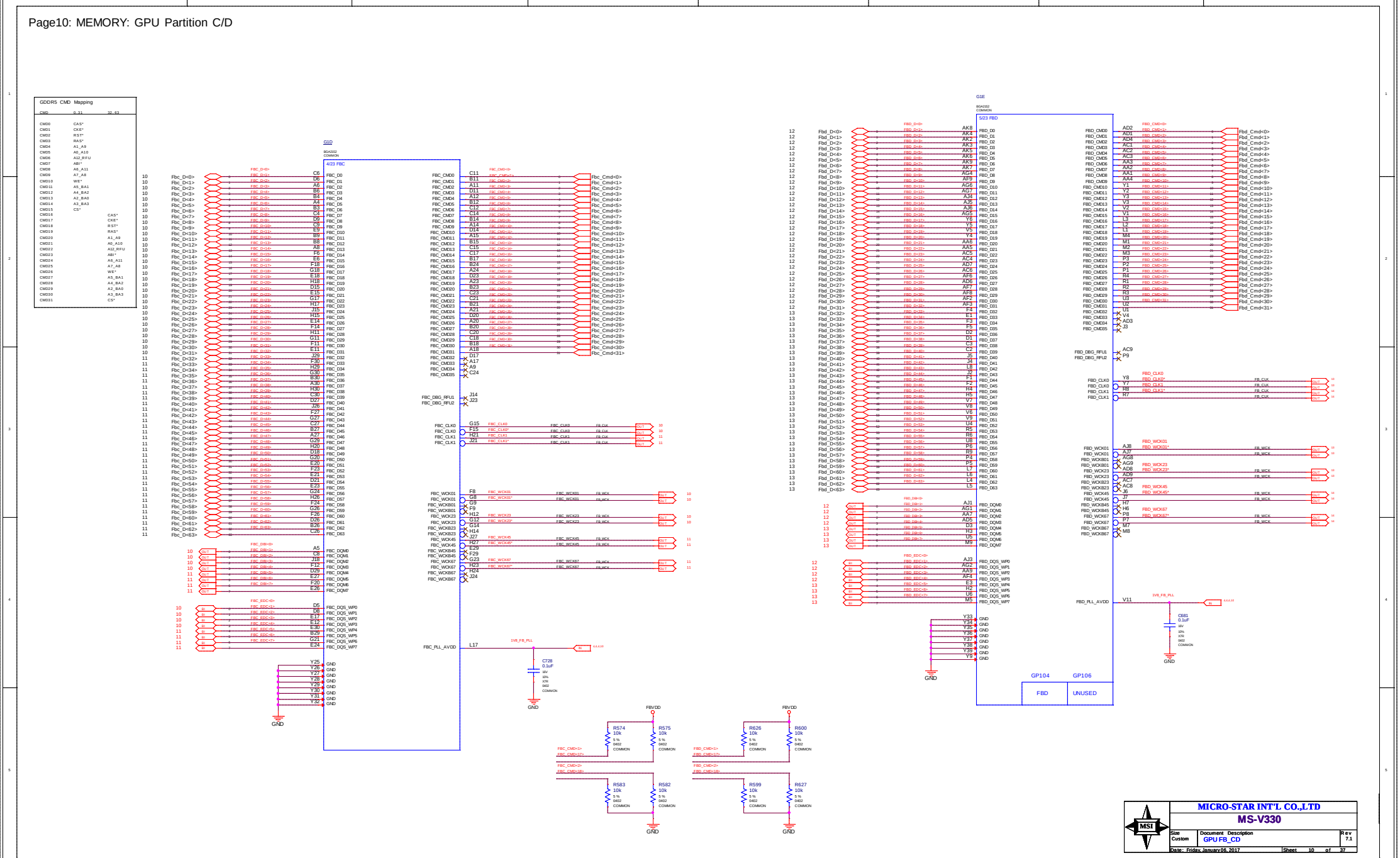
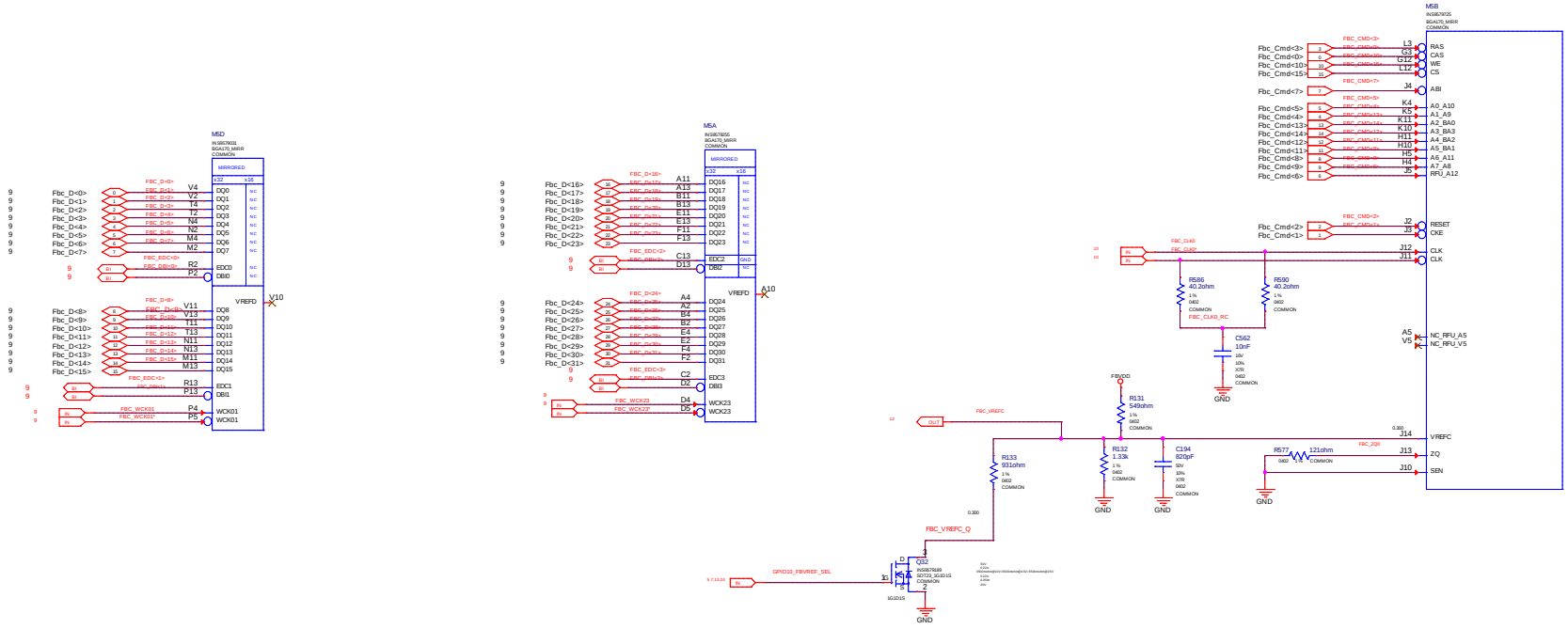
Page10: MEMORY: GPU Partition C/D



Page11: Frame Buffer Partition C [31:0]



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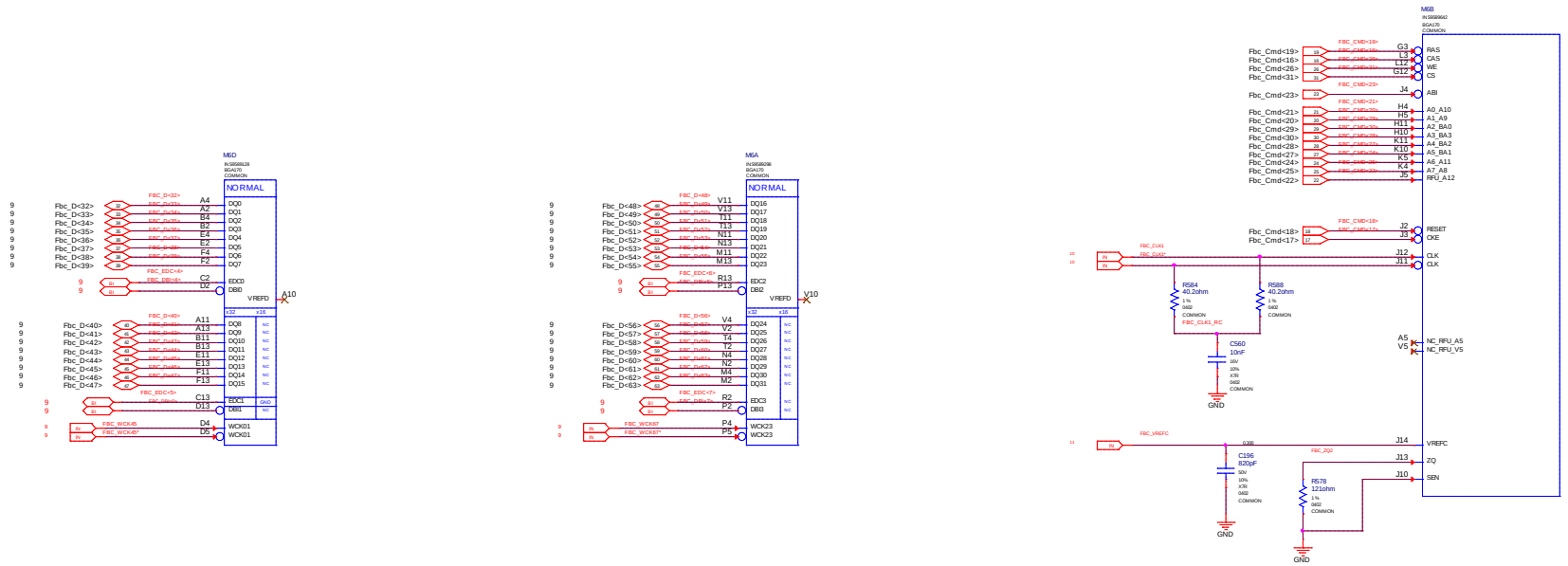
Page12: FRAME BUFFER PARTITION C [63:32]



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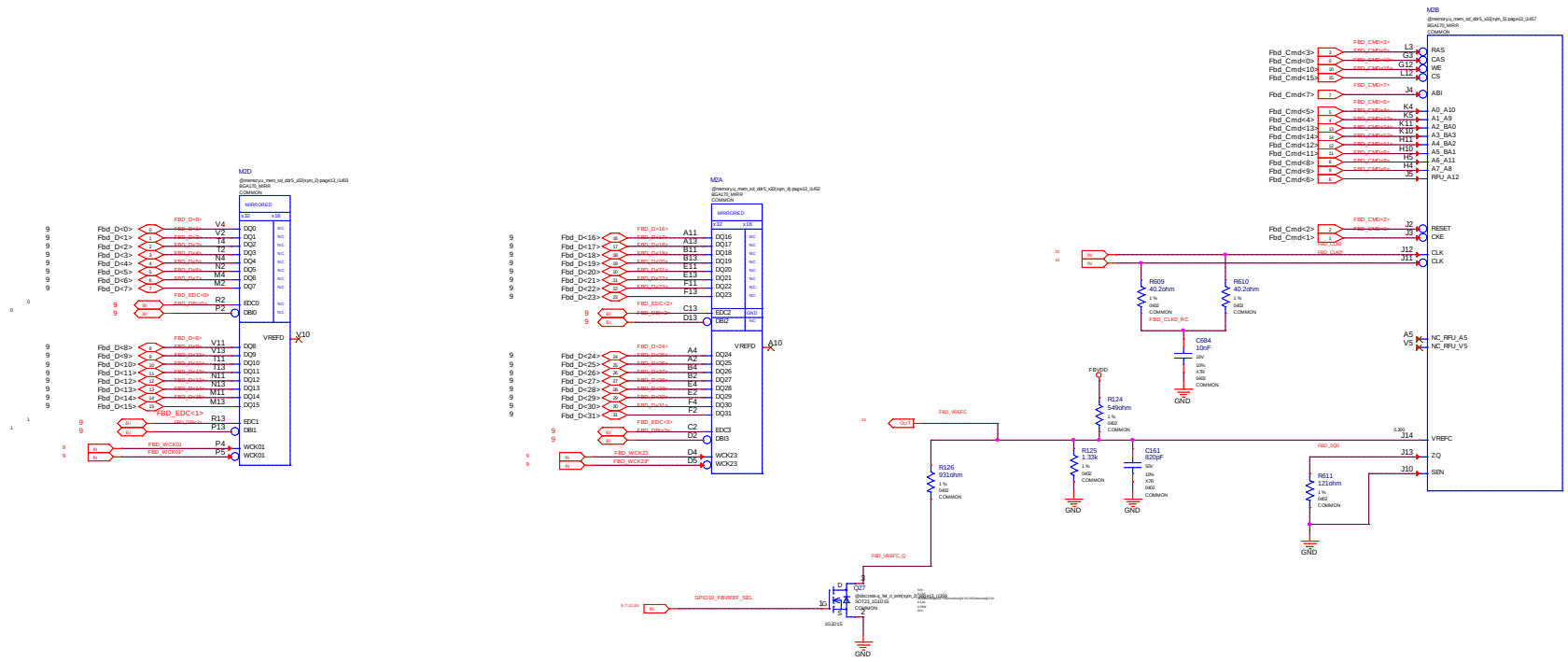
Page13: FRAME BUFFER PARTITION D[31:0]



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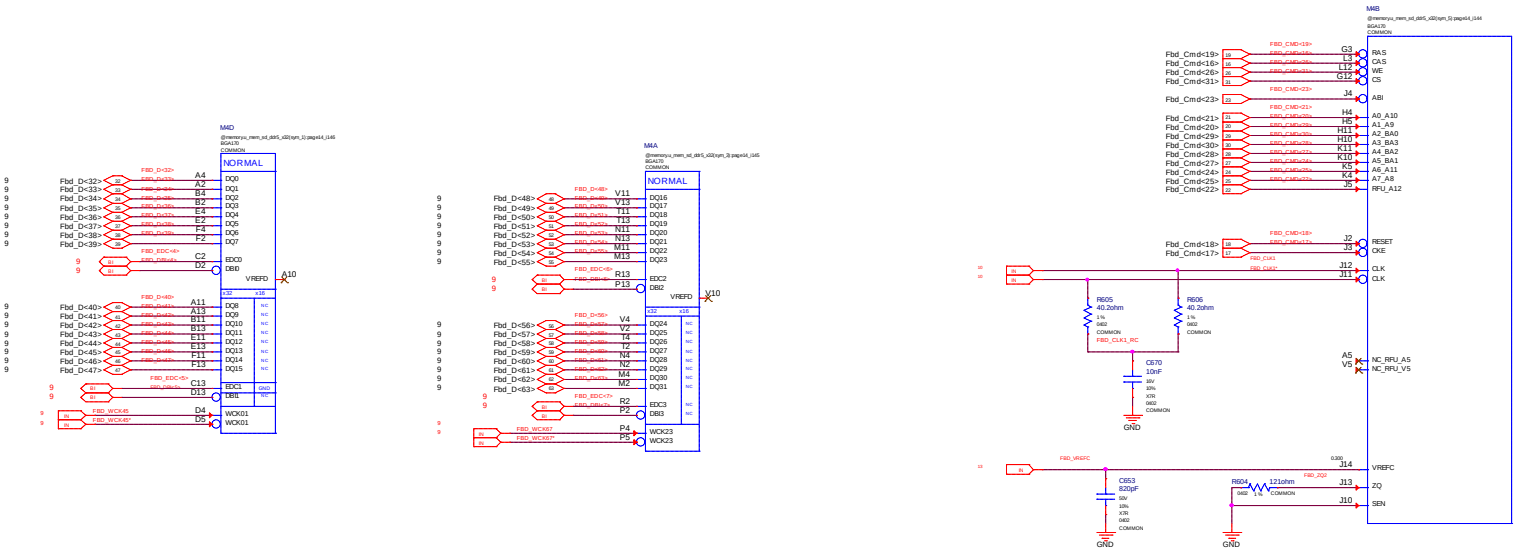
Page14: FRAME BUFFER PARTITION D[63:32]



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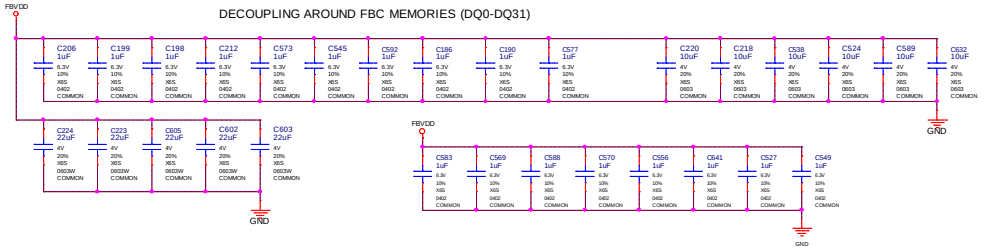
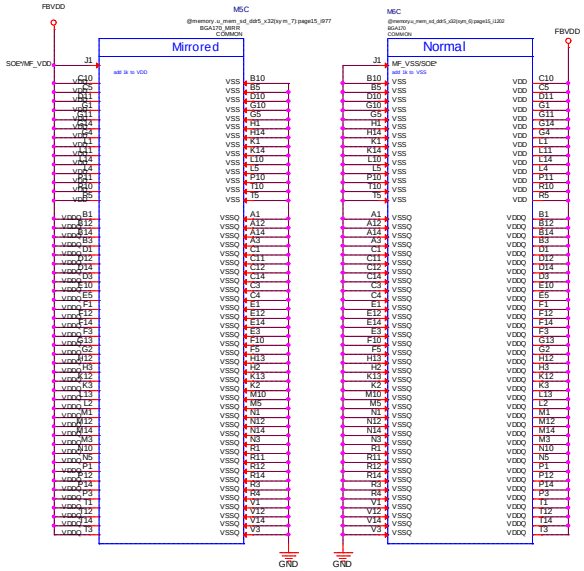
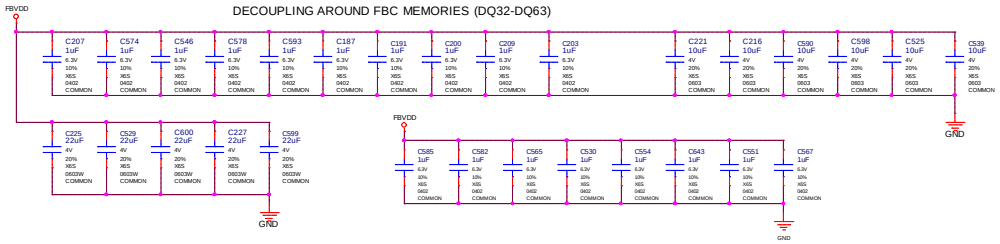
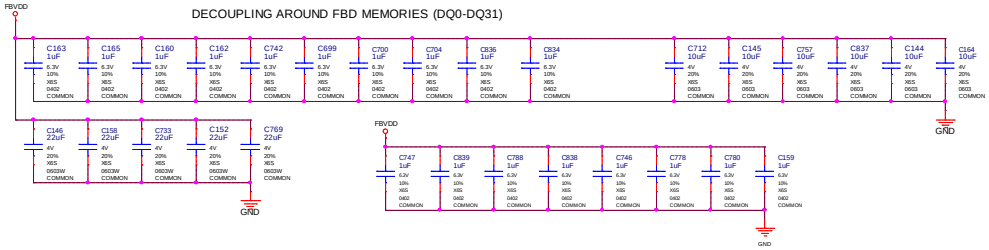
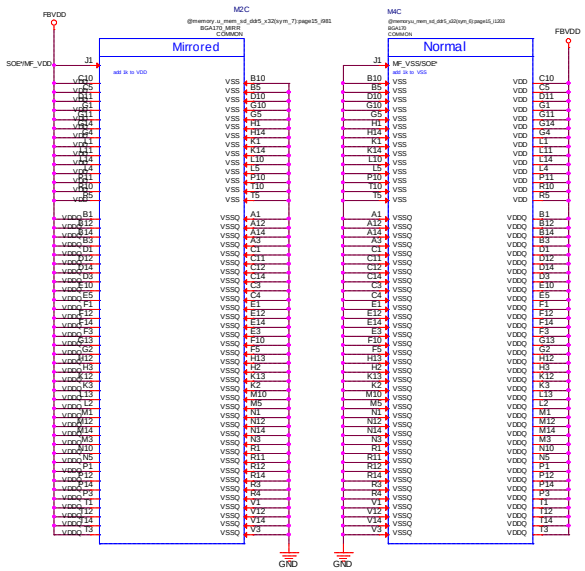
Page15: FRAME BUFFER PARTITION C/D DECOUPLING

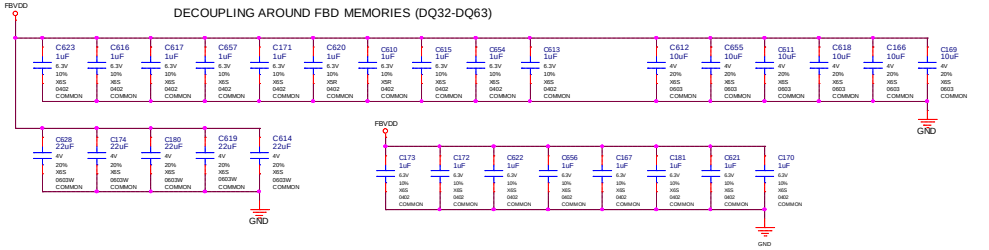












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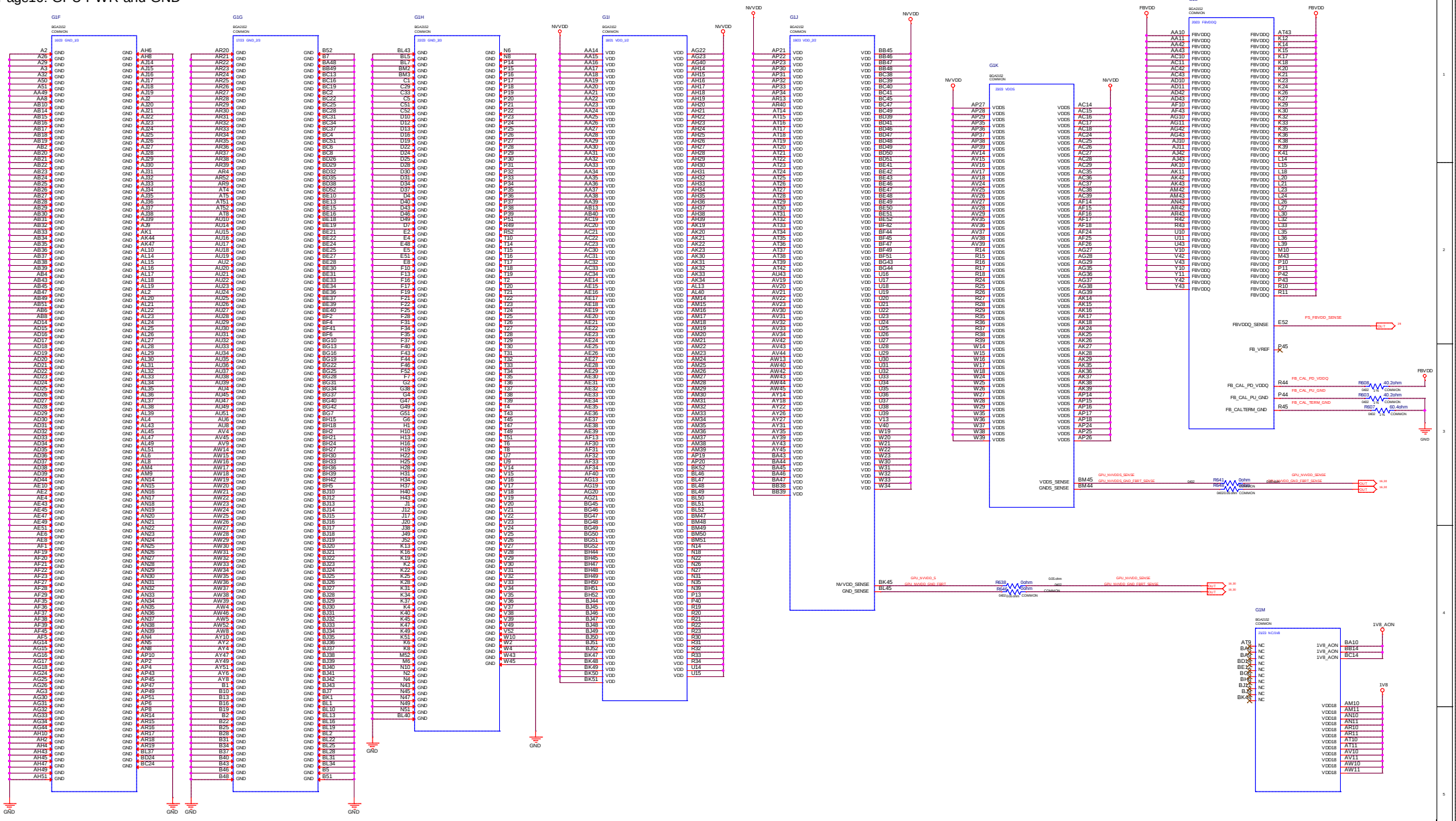
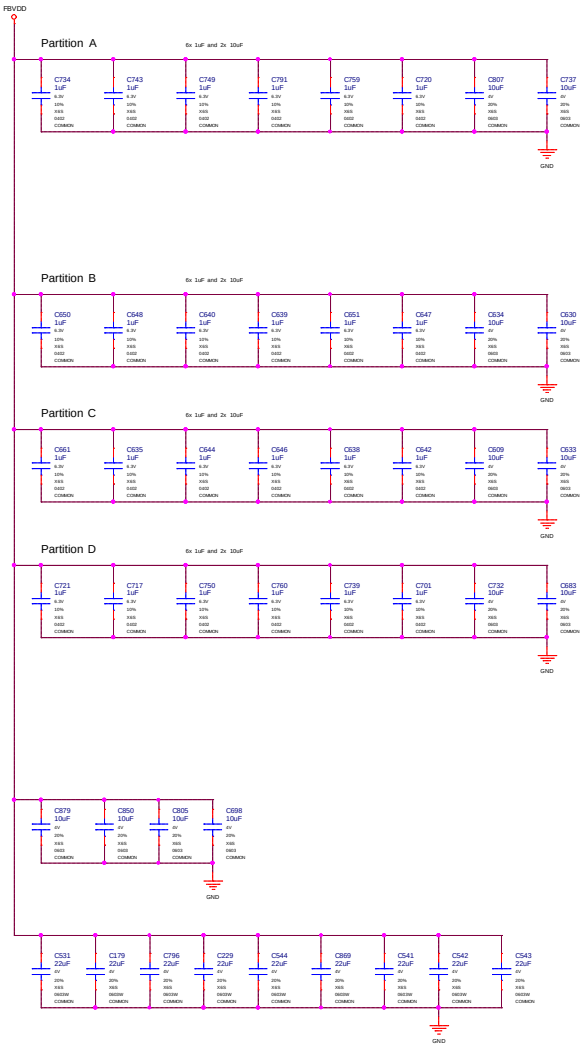
Page16: GPU PWR and GND

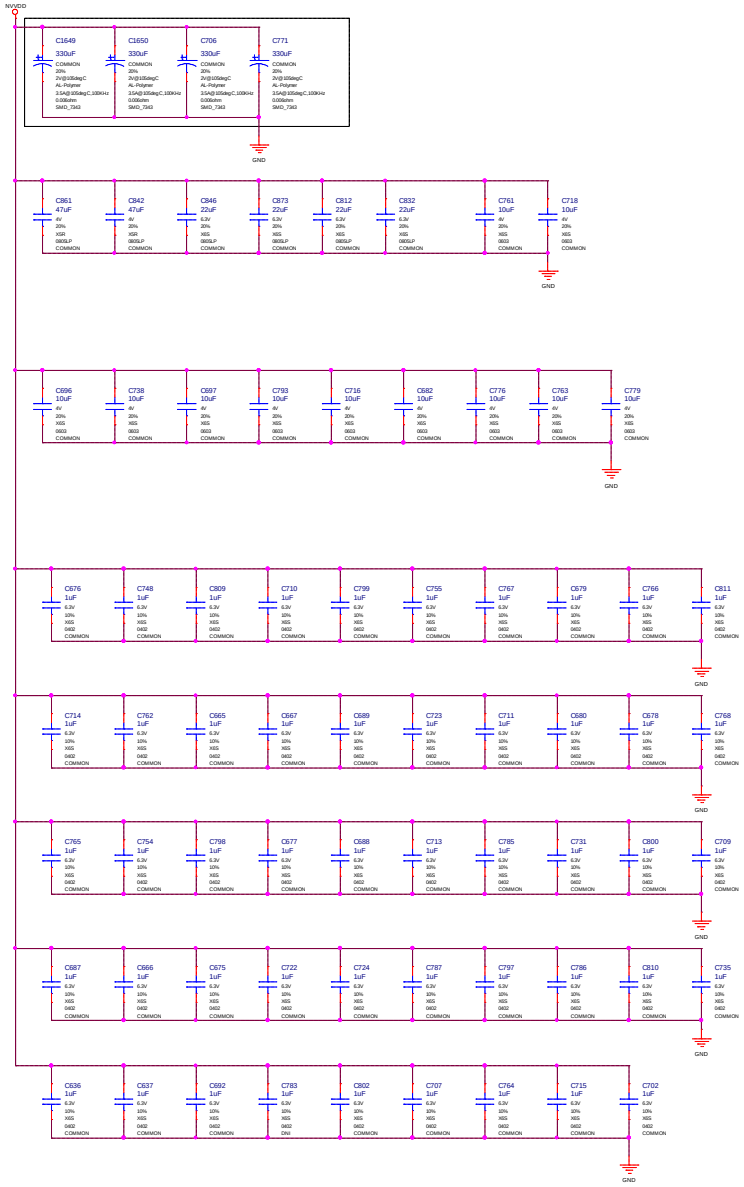


Page17: GPU Decoupling

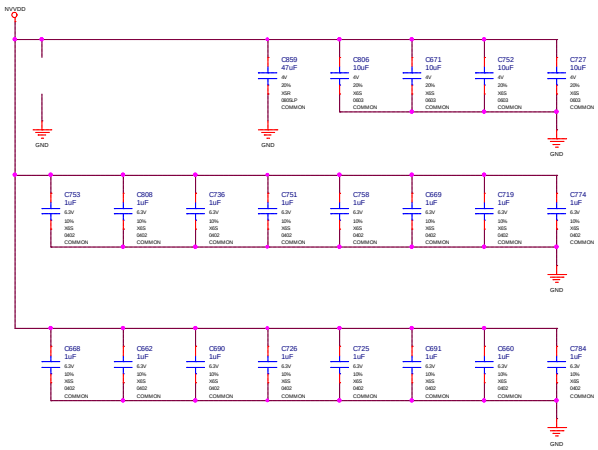
FBVDD



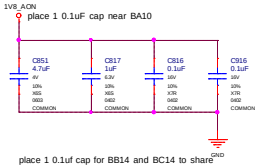
NVVDD



NVVDD

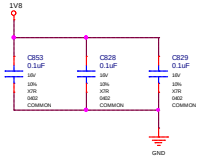


1V8_AON



place 1 0.1uf cap for BB14 and BC14 to share

1V8_MAIN



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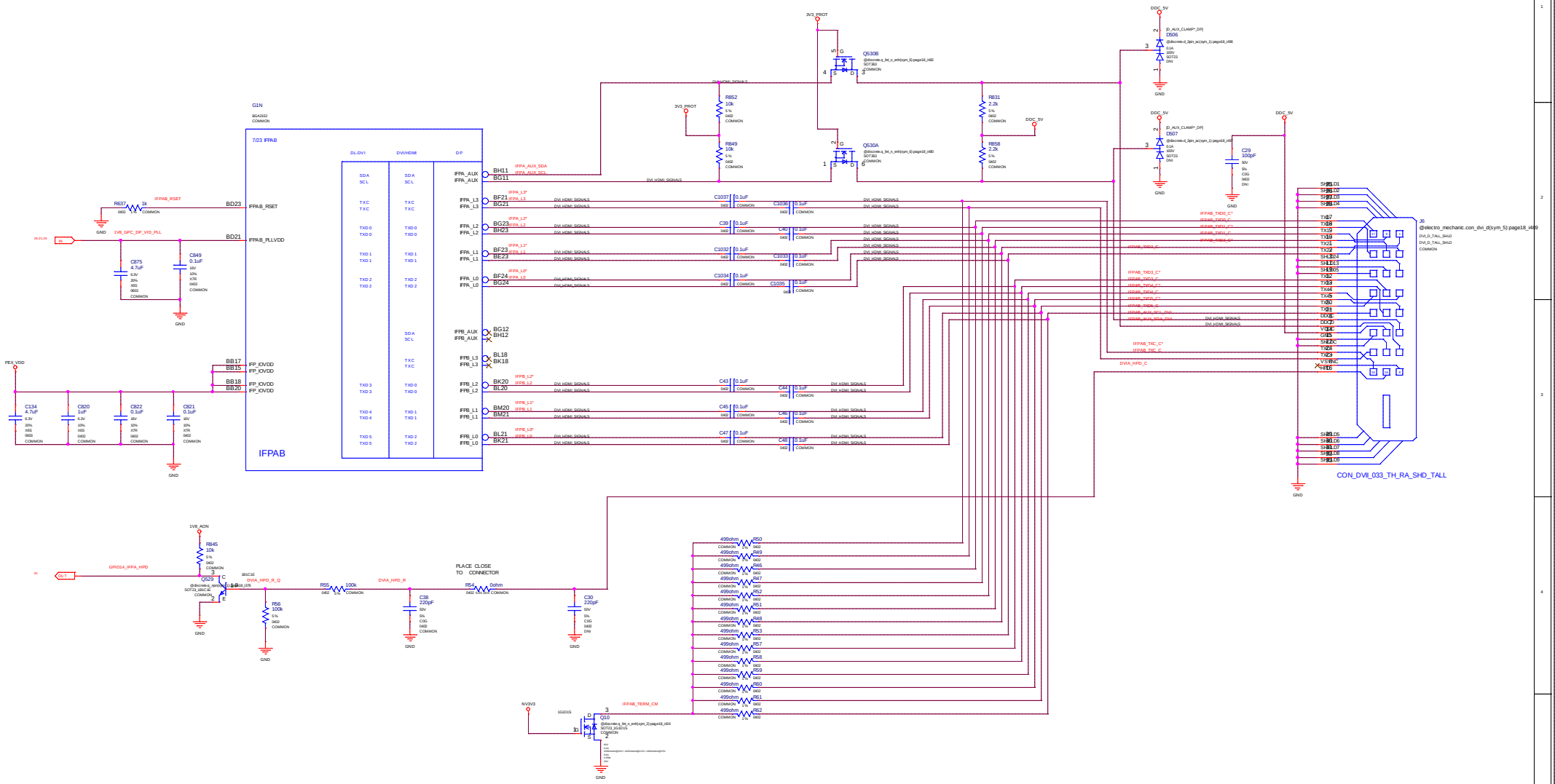
Page18: IFPAB DVI-D-DL



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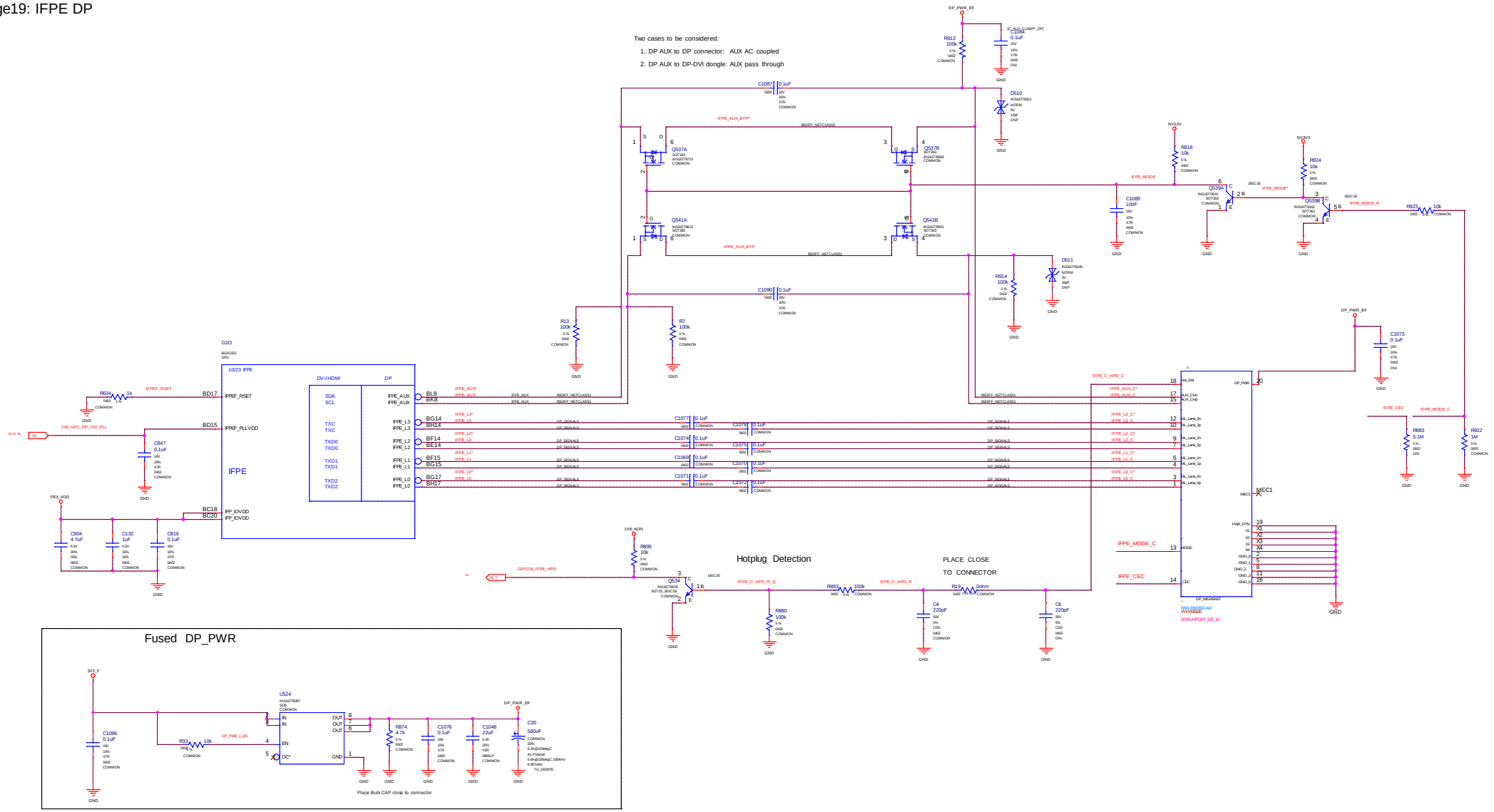
Page19: IFPE DP



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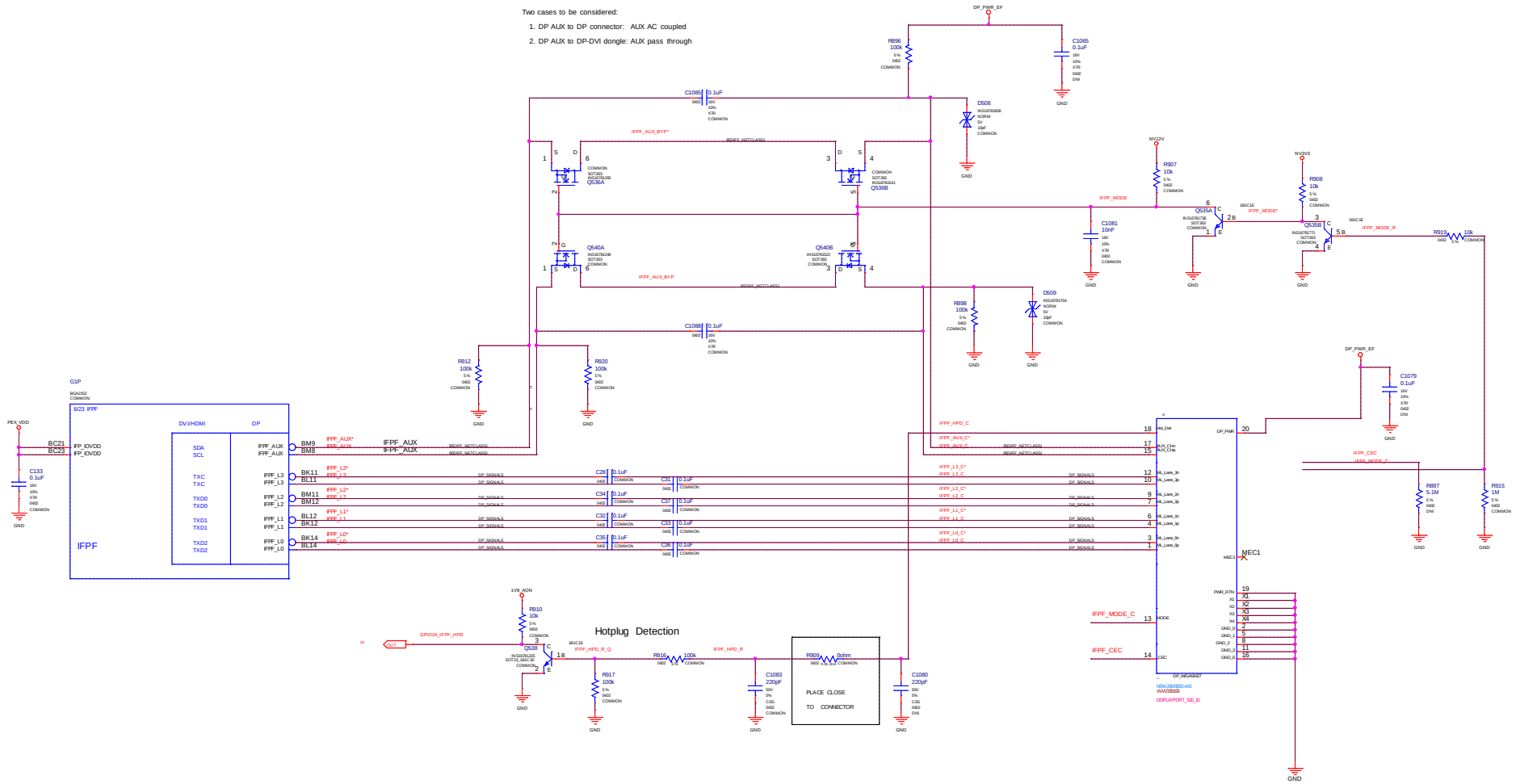
Page 20: IFPF DP



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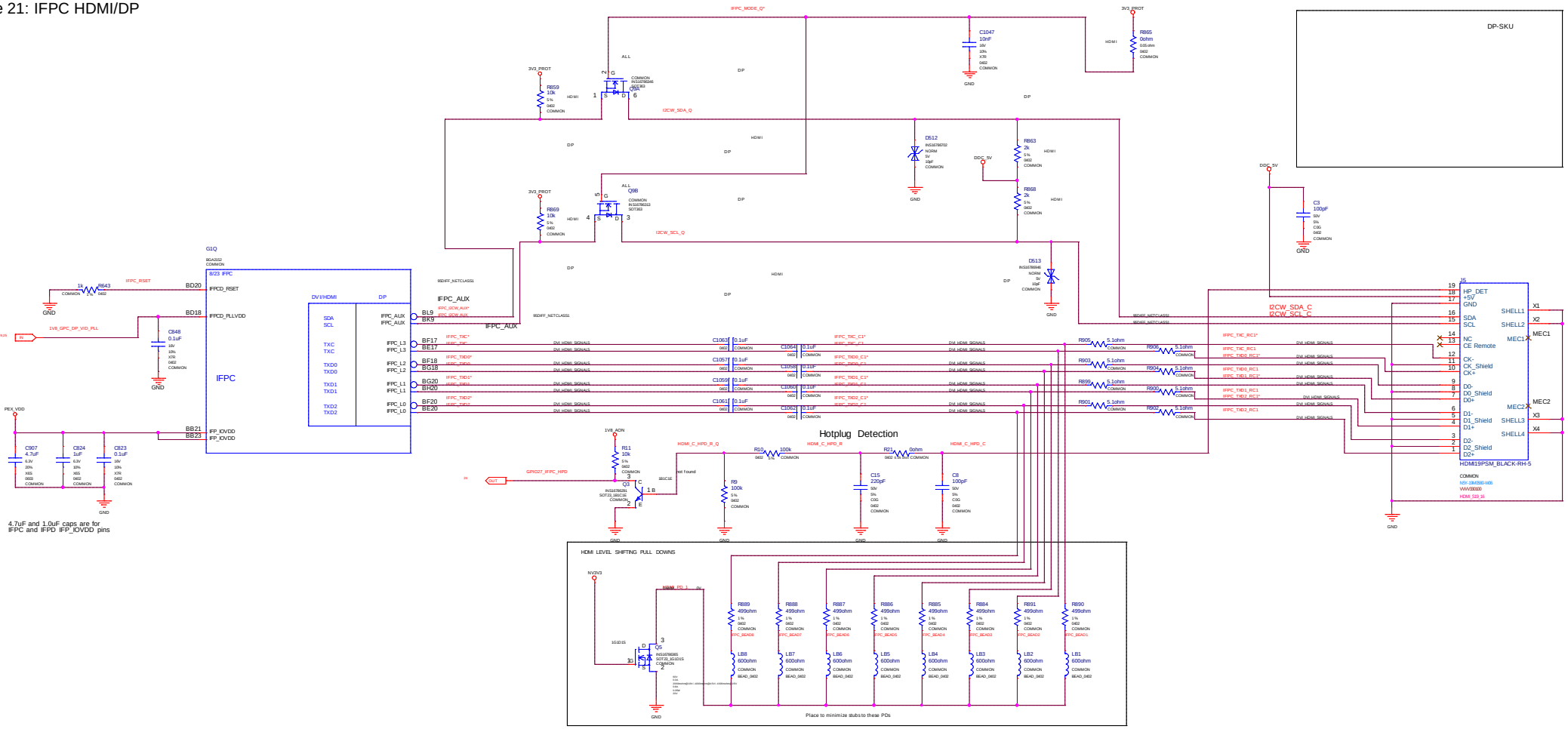
Page 21: IFPC HDMI/DP



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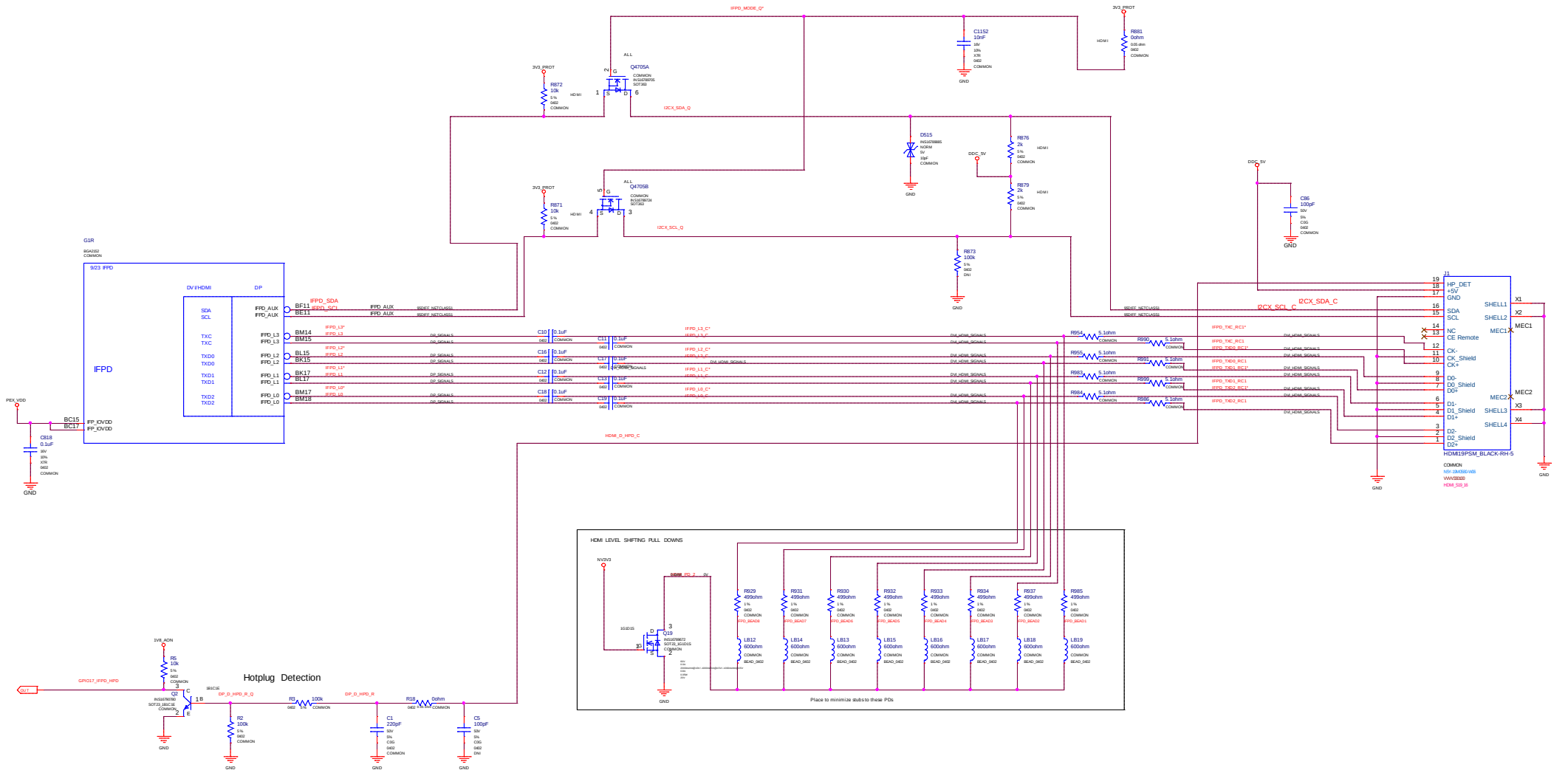
Page 22: IFPD DP



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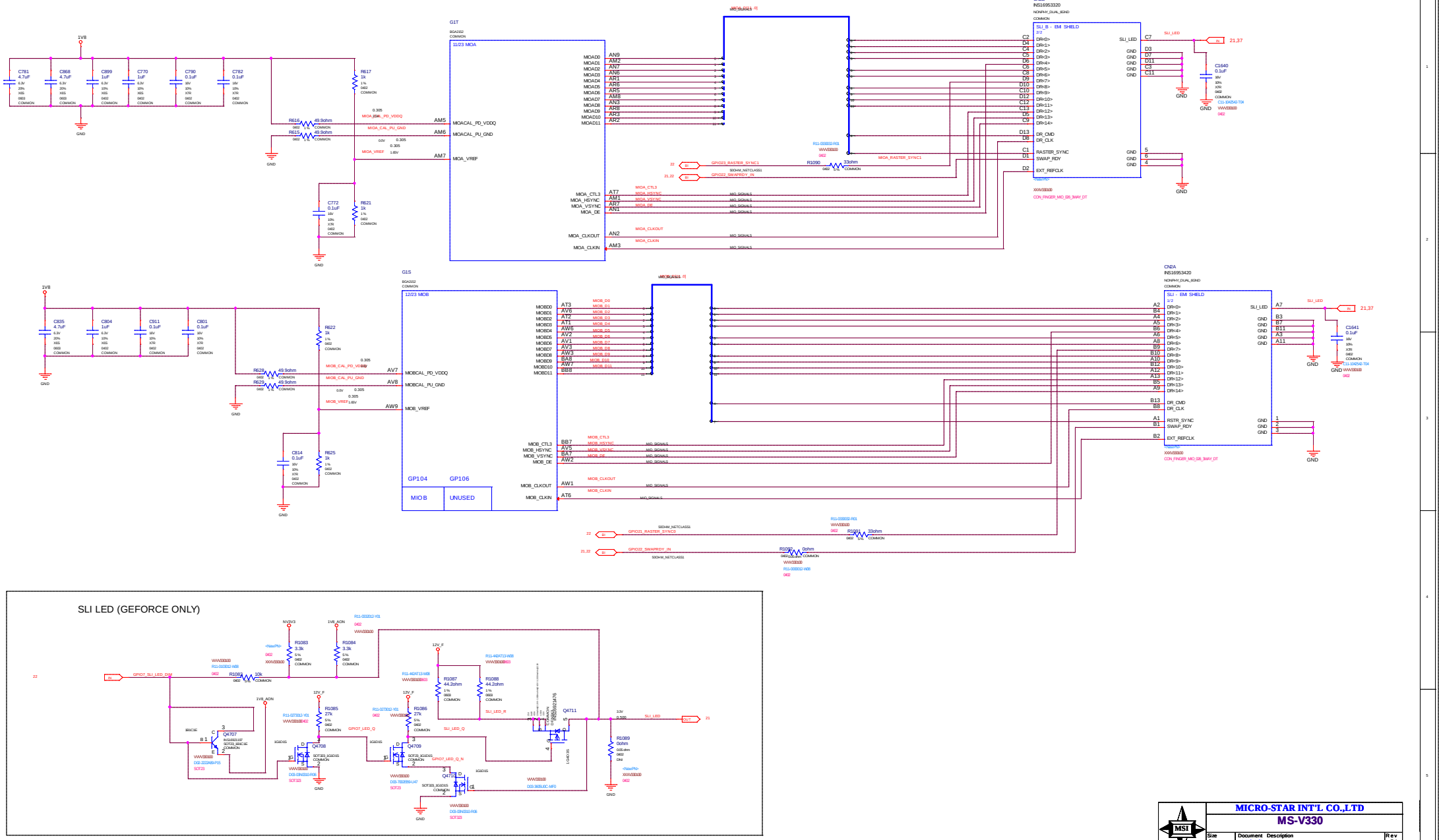
Page 23: MIOA/B Interface and Frame Lock



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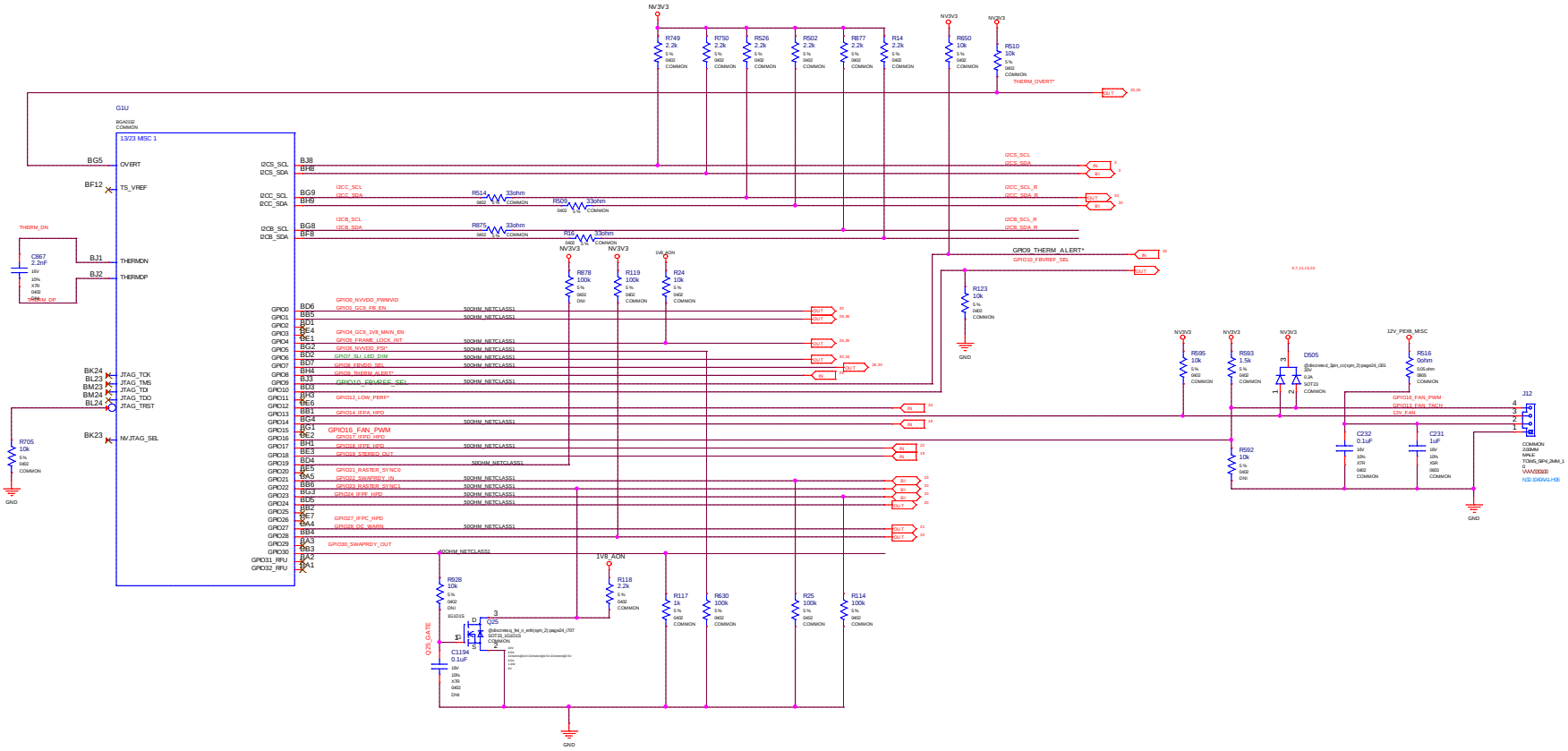
Page 24: MISC1: Fan, Thermal, JTAG, GPIO



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Page25: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

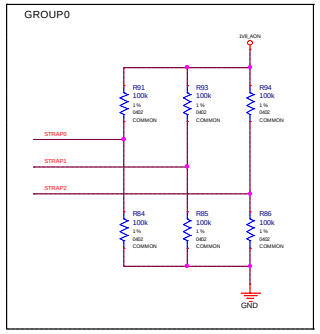
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

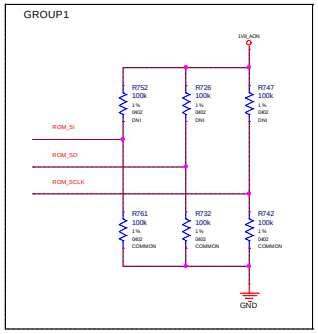
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

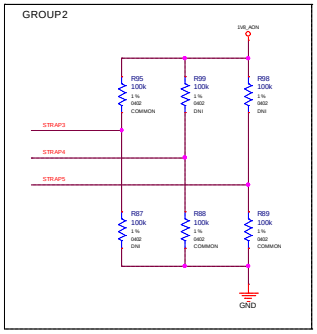
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

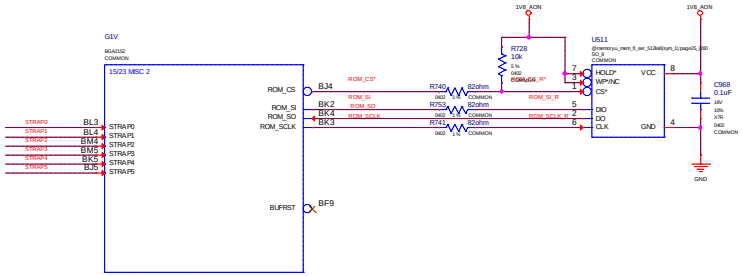
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

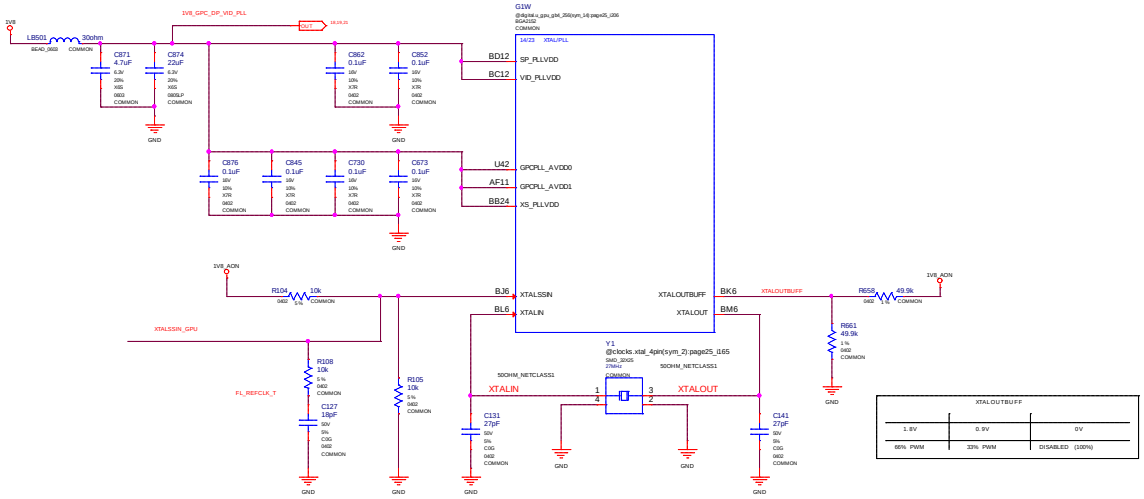






CFG[3:0]	Config Width	Vendor
0000	256Mx32	256-bit Samsung
0001	256Mx32	256-bit Micron
0010	256Mx32	256-bit Hynix
0011	Reserved	
0100	Reserved	
0101	Reserved	
0110	Reserved	
0111	Reserved	





XTALOUTBUFF		
1.8V	0.9V	0V
66% PWM	33% PWM	DISABLED (100%)

MICRO-STAR INT'L CO.,LTD
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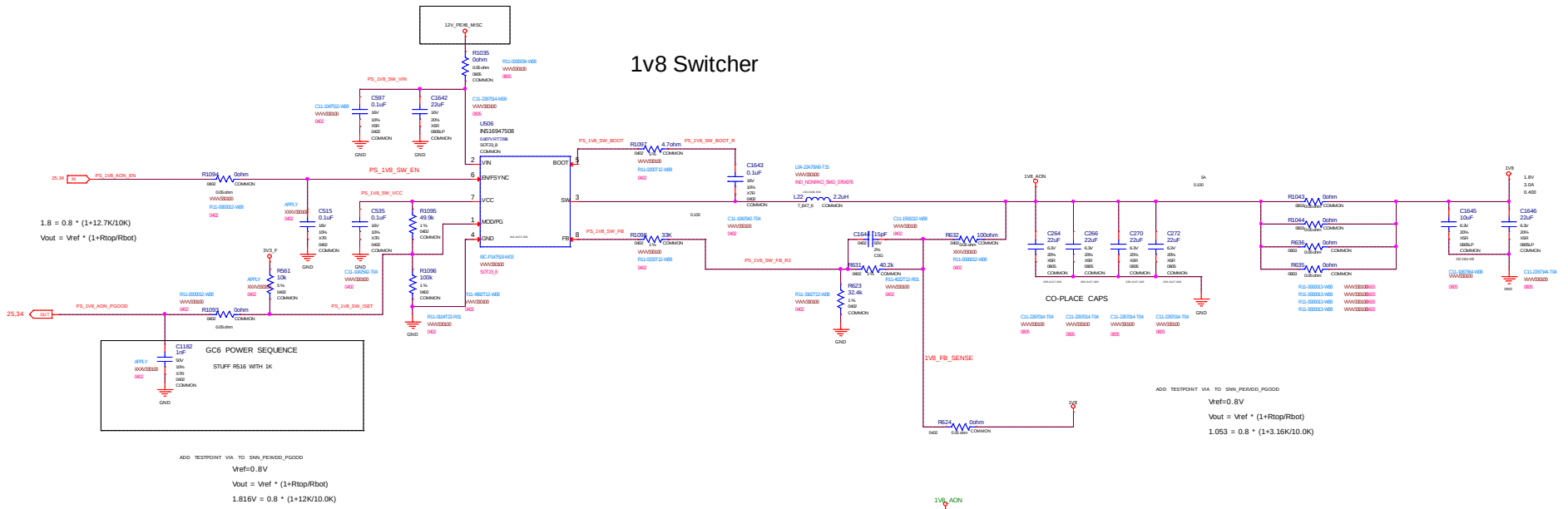
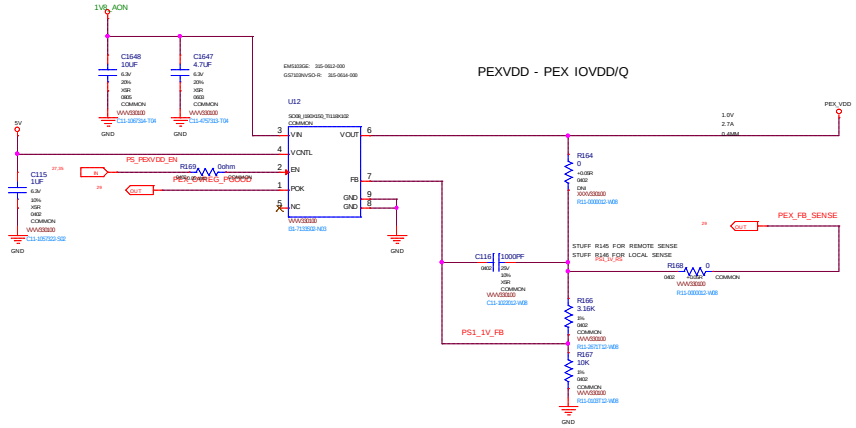
Page26: PS: 1V8 PLL, 1V8_AON





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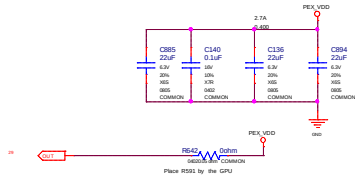
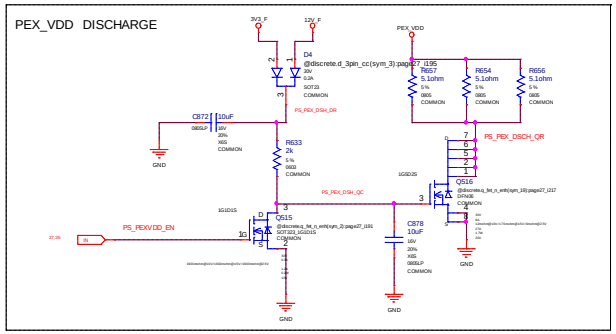
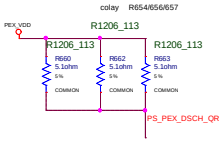
Page27: PS: 5V SWITCHER,PEX VDD

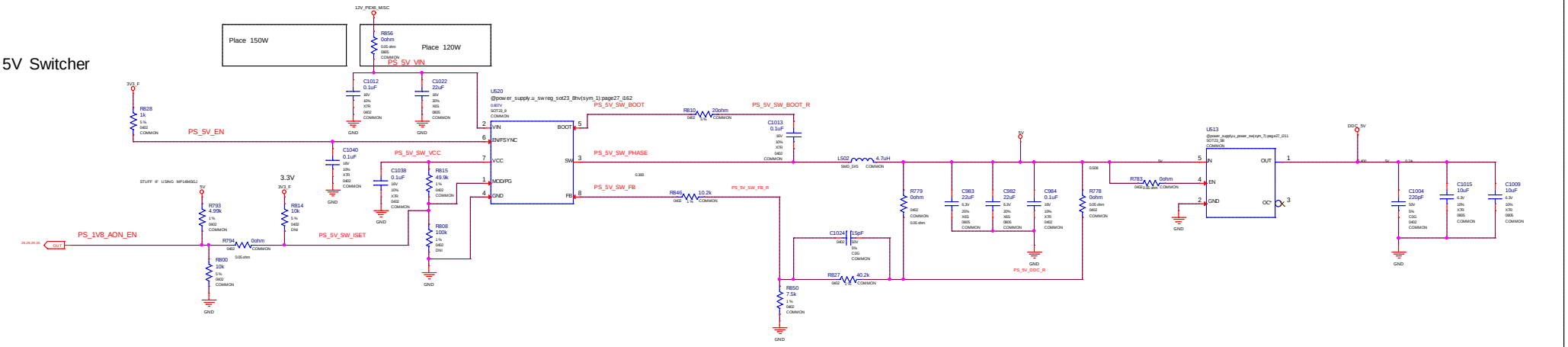
PEX PLL Switcher







5V Switcher



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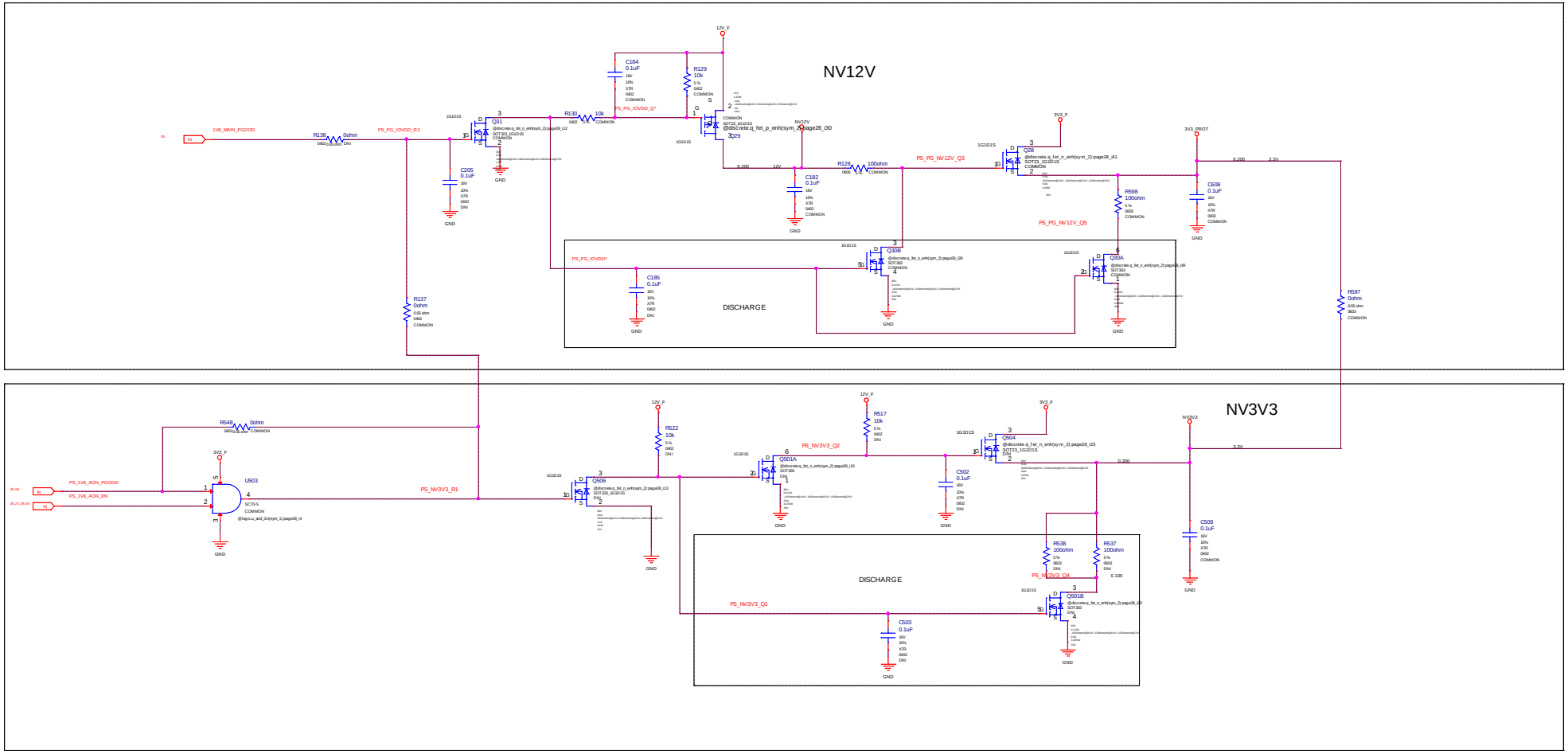

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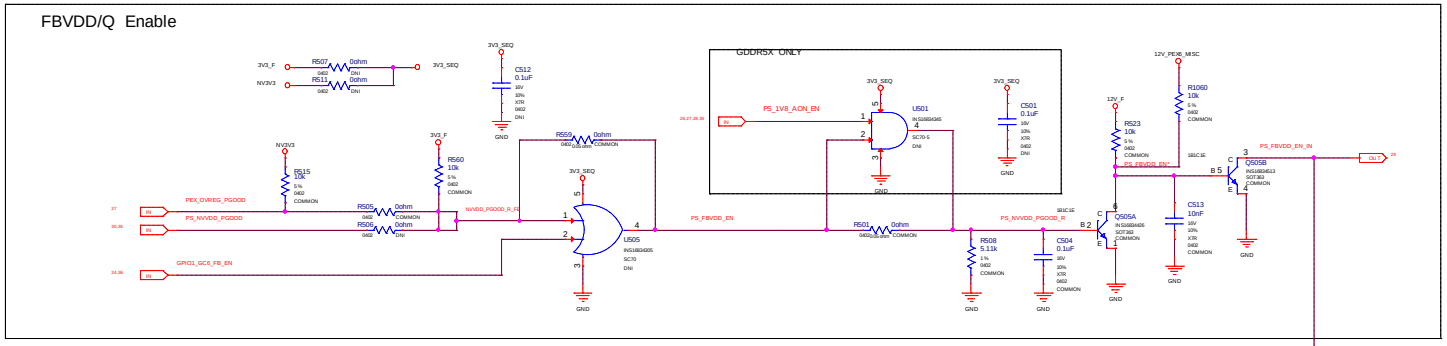
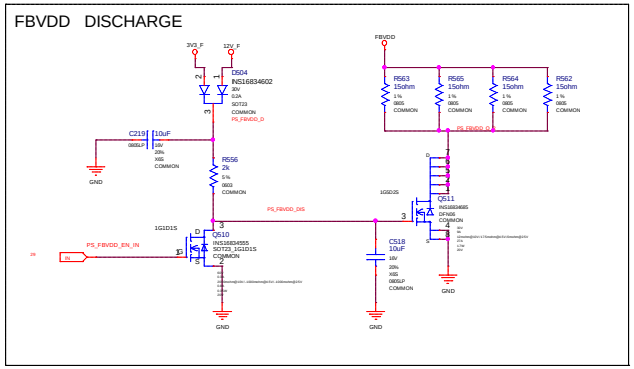
Page29: PS: FBVDDQ

NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
FBVDD			

FBVDD/Q Enable

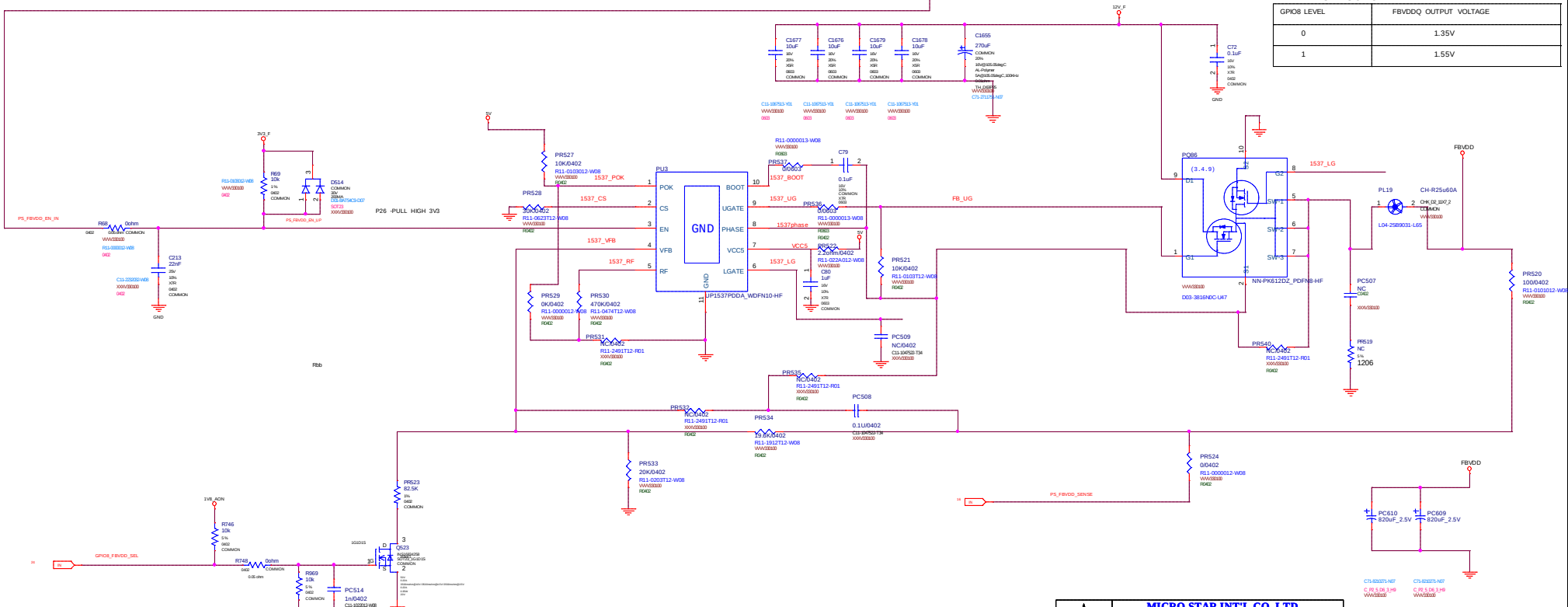


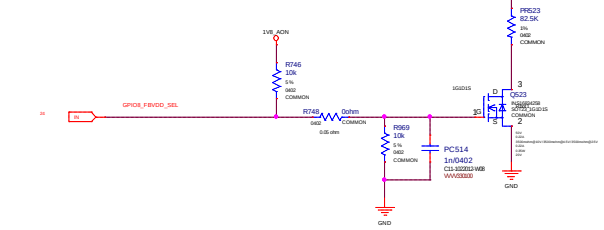
FBVDD DISCHARGE



SAMSUNG

GPIO8 LEVEL	FBVDDQ OUTPUT VOLTAGE
0	1.35V
1	1.55V





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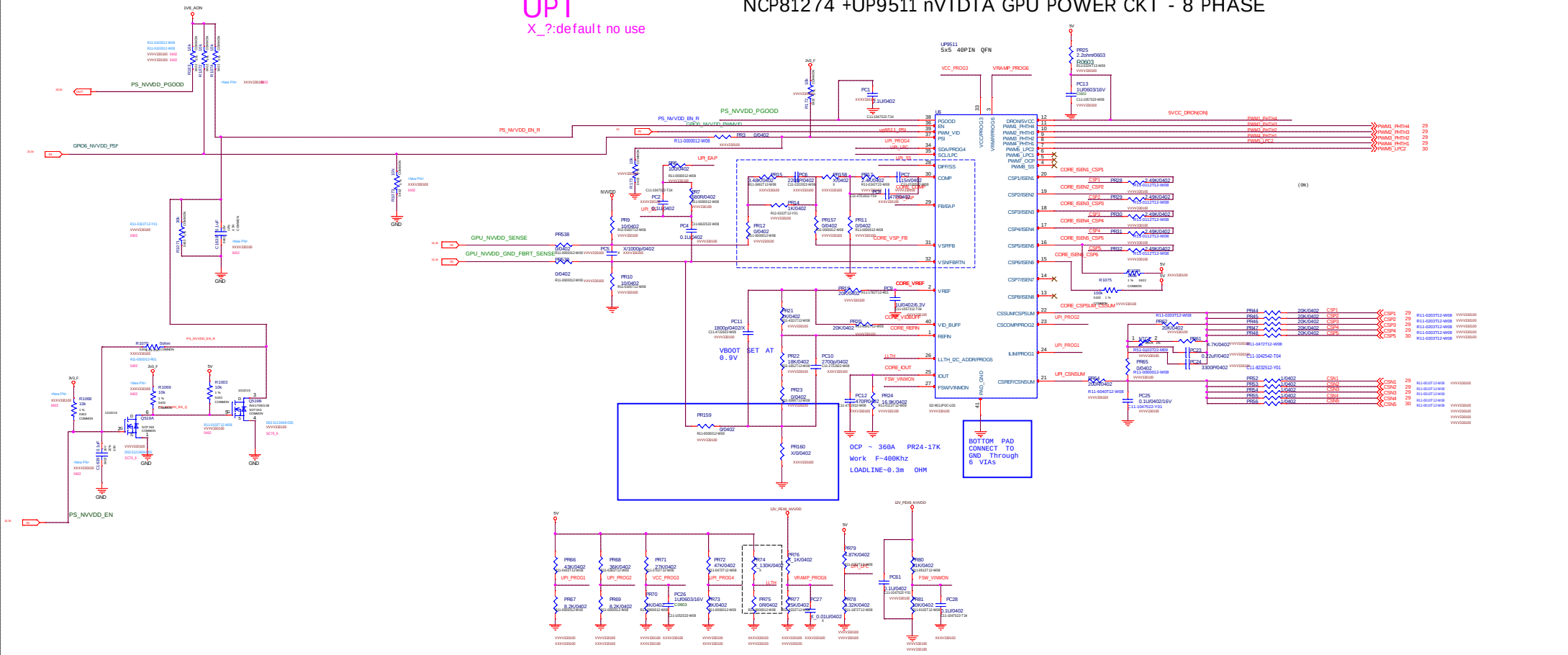
Page27: PS: NVVDD_OVR8

UPI

X_?:default no use

NCP81274 +UP9511 nVIDIA GPU POWER CKT - 8 PHASE



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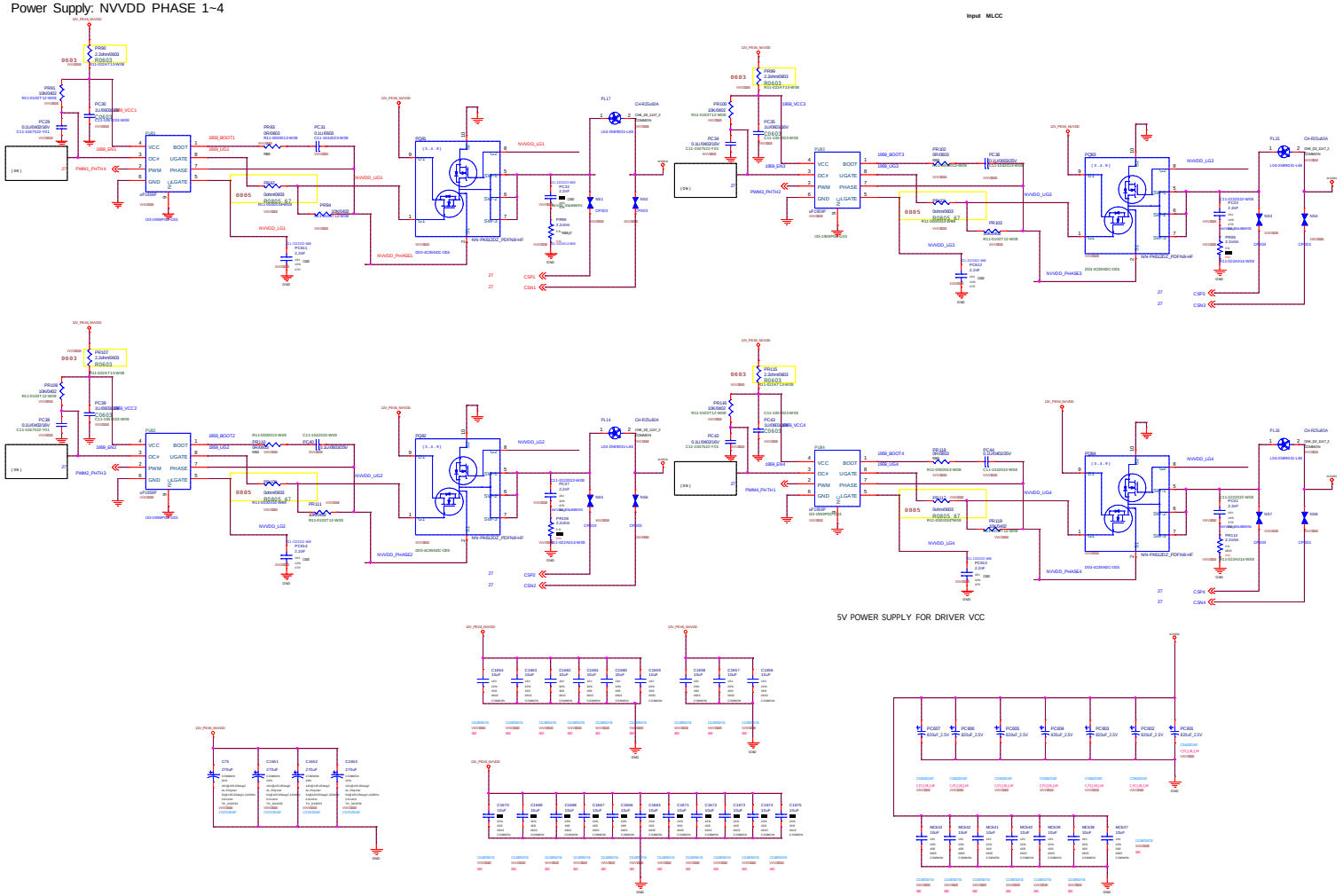
Power Supply: NVVDD PHASE 1~4

Input MLCC



5V POWER SUPPLY FOR DRIVER VCC

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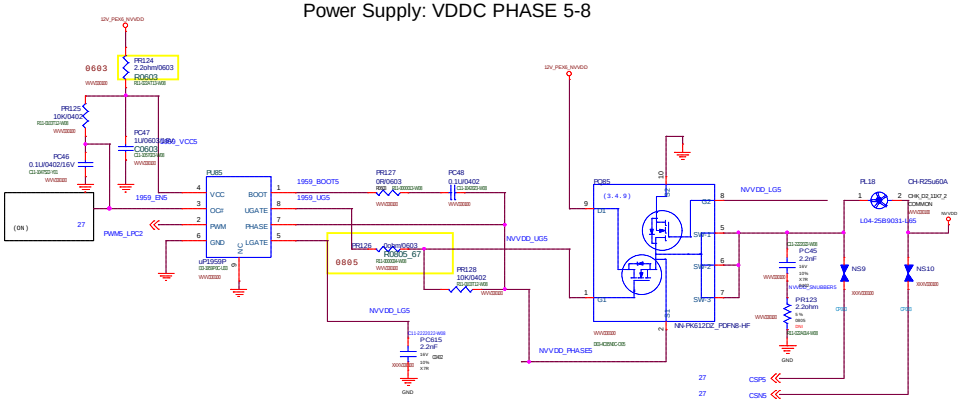
Page30: PS: NVVDD Phase 5 ~8

Power Supply: VDDC PHASE 5-8



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Size: Custom	Document Description: PHASE 5	Rev: 7.1
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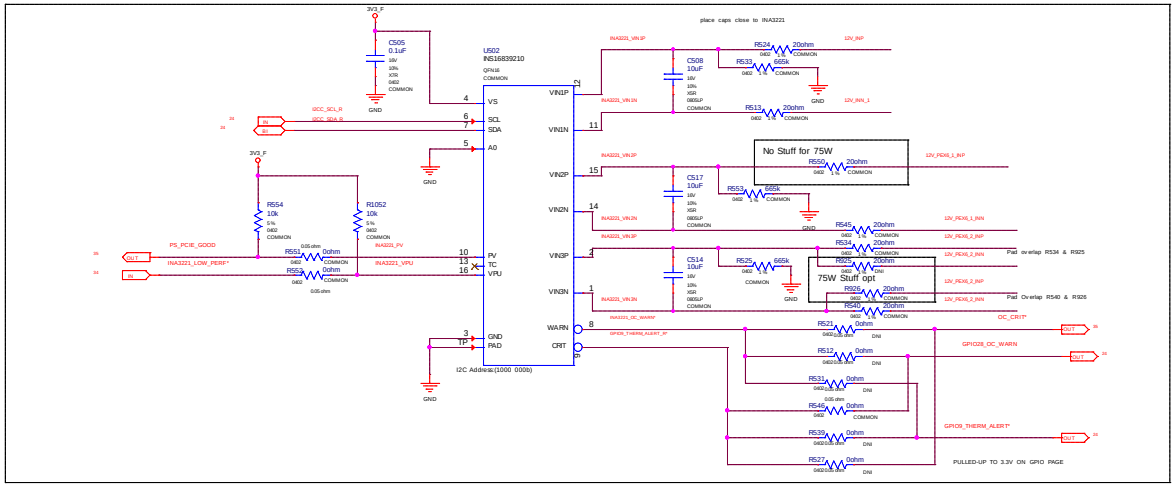
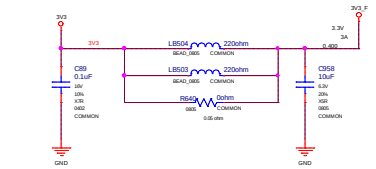
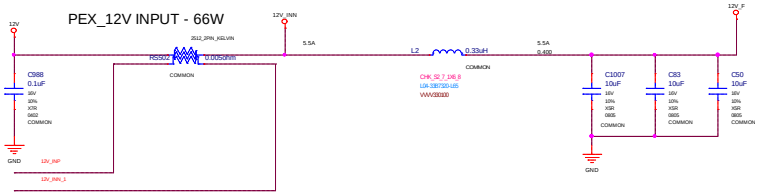
Page33: PS: Inputs, Filtering, and Monitoring



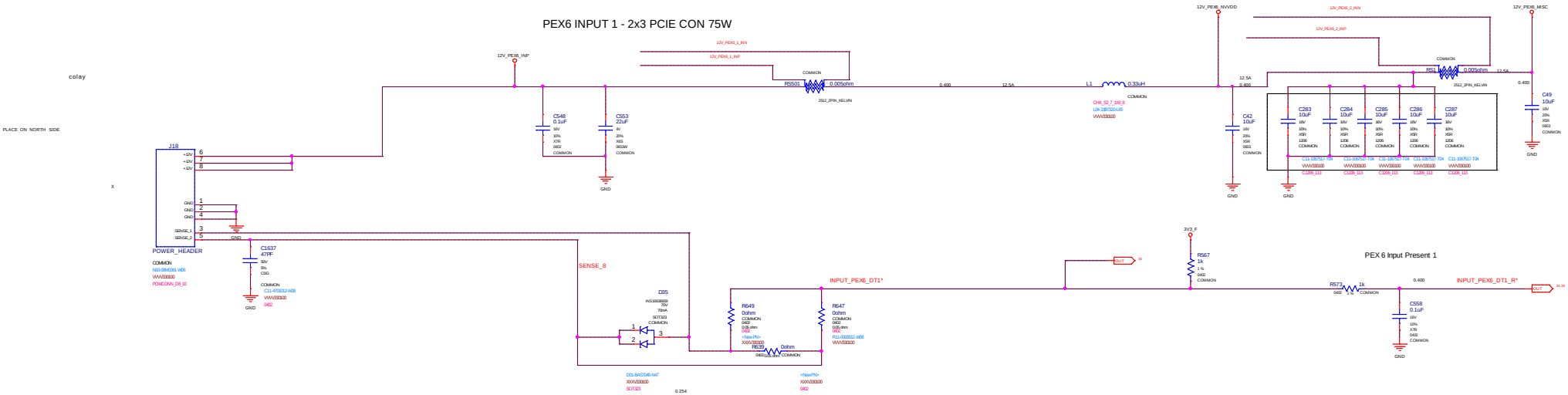
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



PEX6 INPUT 1 - 2x3 PCIE CON 75W



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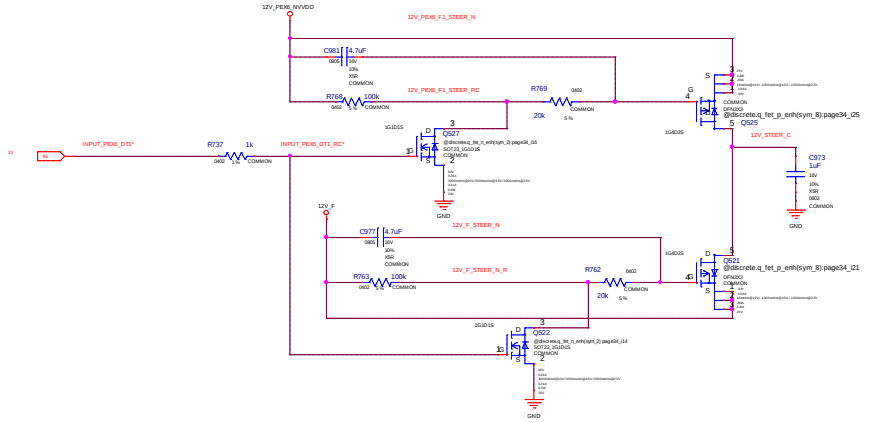
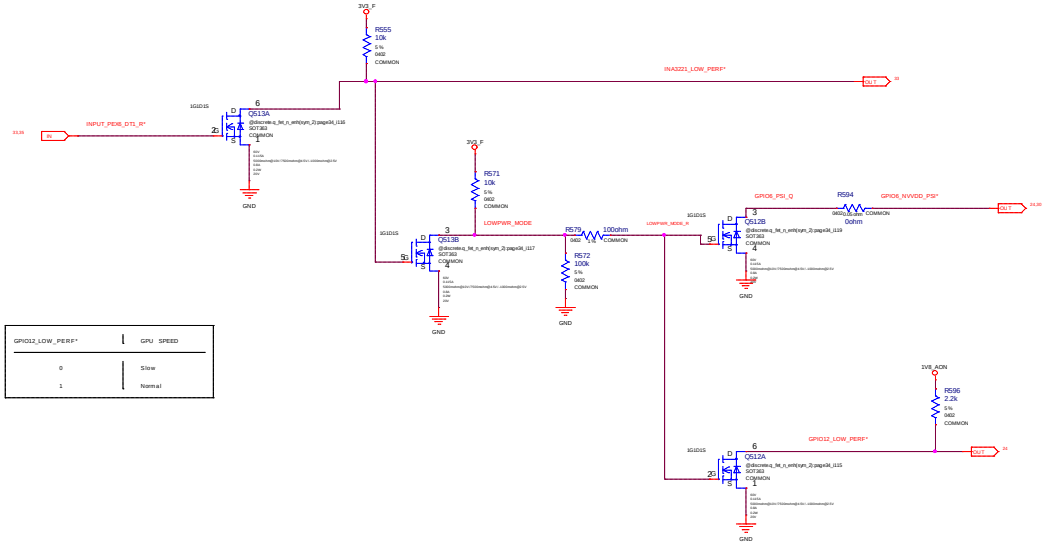
Page34: PS: 12V Current Steering, PSI Control, and LED

12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA



PEX Input - Power Level/PSI* Control



GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

GeForce Logo LED

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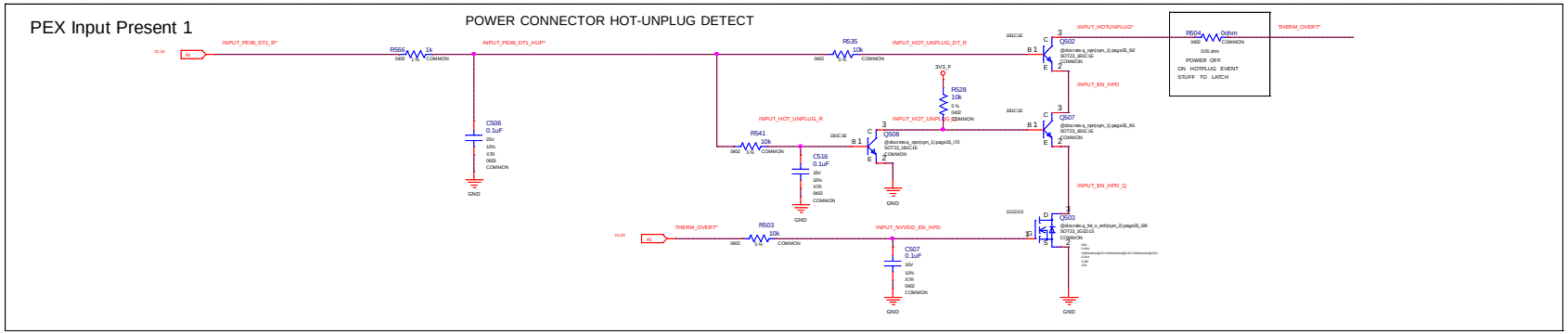
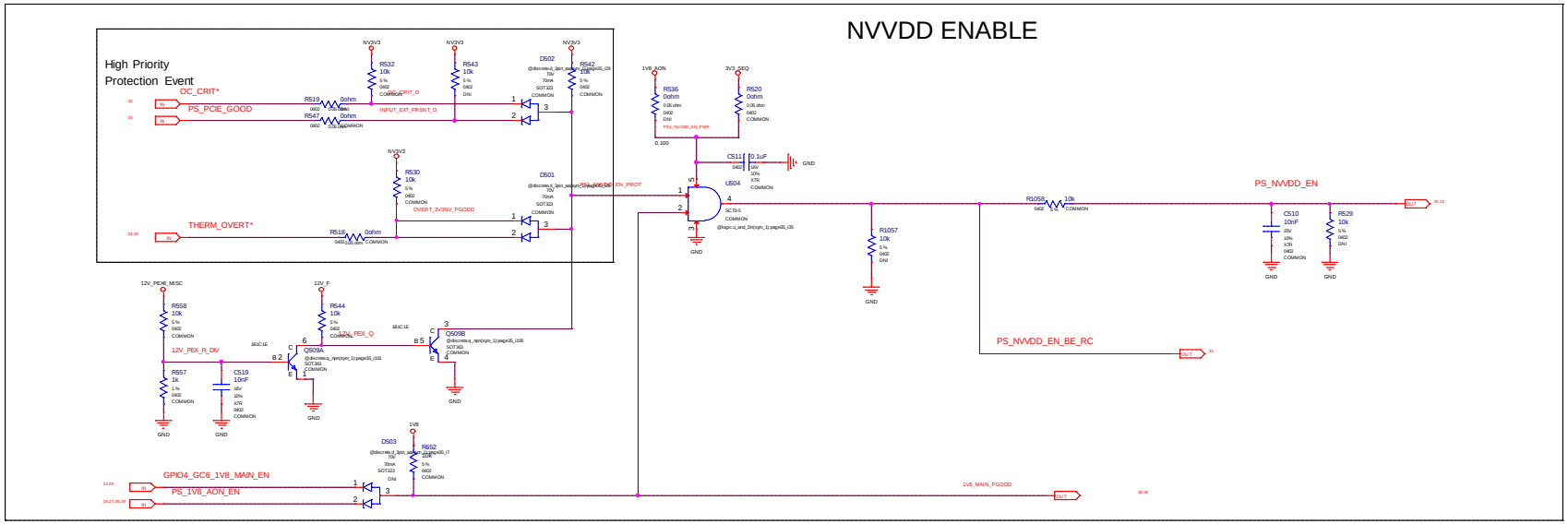
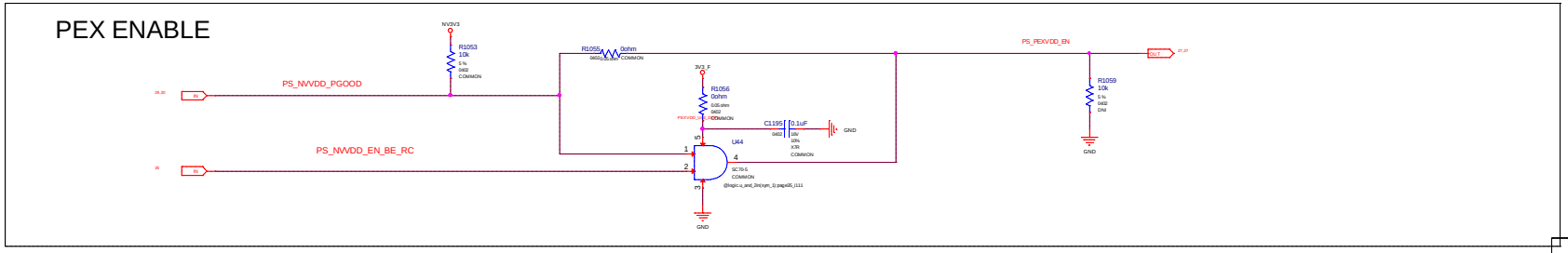
PEX Input Present 1



NVVDD ENABLE



PEX ENABLE



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Page38: GC6 MISC

Accept 3V3 Logic

GC6 FB ENABLE

GPU_EVENT*

PEX_CLKREQ*

PEX_RST# LOGIC

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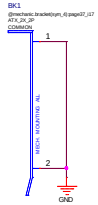
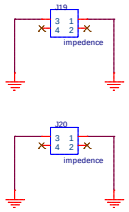
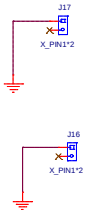
Page40: MECH

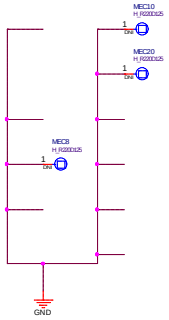
Brackets:



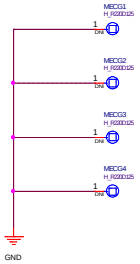


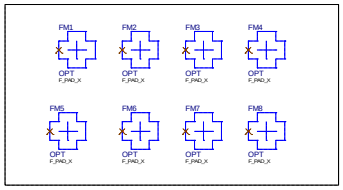


Mechanical Holes Symbol



GPU Stiffner





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