

PG411 A01

GP104 - 8GB GDDR5, 256b, 256Mx32
Tall DVI-D + DP + DP + HDMI + DP

TABLE OF CONTENTS

Page	Description	Page	Description
1	Table of Contents	26	PS: FBVDD
2	Block Diagram	27	PS: NVVDD_OVR8
3	PCI Express	28	PS: Blank Page
4	MEMORY: GPU Partition A/B	29	PS: NVVDD Phase 1-4
5	MEMORY: FBA[31:0]	30	PS: NVVDD Phase 5 & 6
6	MEMORY: FBA[63:32]	31	PS: Blank Page
7	MEMORY: FBB[31:0]	32	PS: Dynamic Power Balance Phases
8	MEMORY: FBB[63:32]	33	PS: Dynamic Power Balance Logic
9	MEMORY: GPU Partition C/D	34	PS: NV3V3, NV12V
10	MEMORY: FBC[31:0]	35	PS: Inputs, Filtering, and Monitoring
11	MEMORY: FBC[63:32]	36	PS: Shutdown and Sequencing
12	MEMORY: FBD[31:0]	37	PS: 12V Current Steering PSI Control and LED
13	MEMORY: FBD[63:32]	38	MECH: Bracket/Thermal
14	GPU PWR and GND		
15	GPU Decoupling		
16	IFPAB DVI-D-DL		
17	IFPE DP		
18	IFPEF DP		
19	IFPC HDMI 2.0/DP		
20	IFPD DP		
21	MIOA/B Interface and Frame Lock		
22	MISC1; Fan, Thermal, JTAG, GPIO, Stereo		
23	MISC2: ROM, XTAL, Straps		
24	PS: 1V8, 1V8_AON		
25	PS: 5V, PEX_VDD		

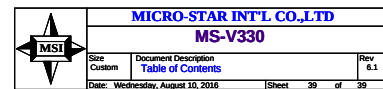
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS." THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

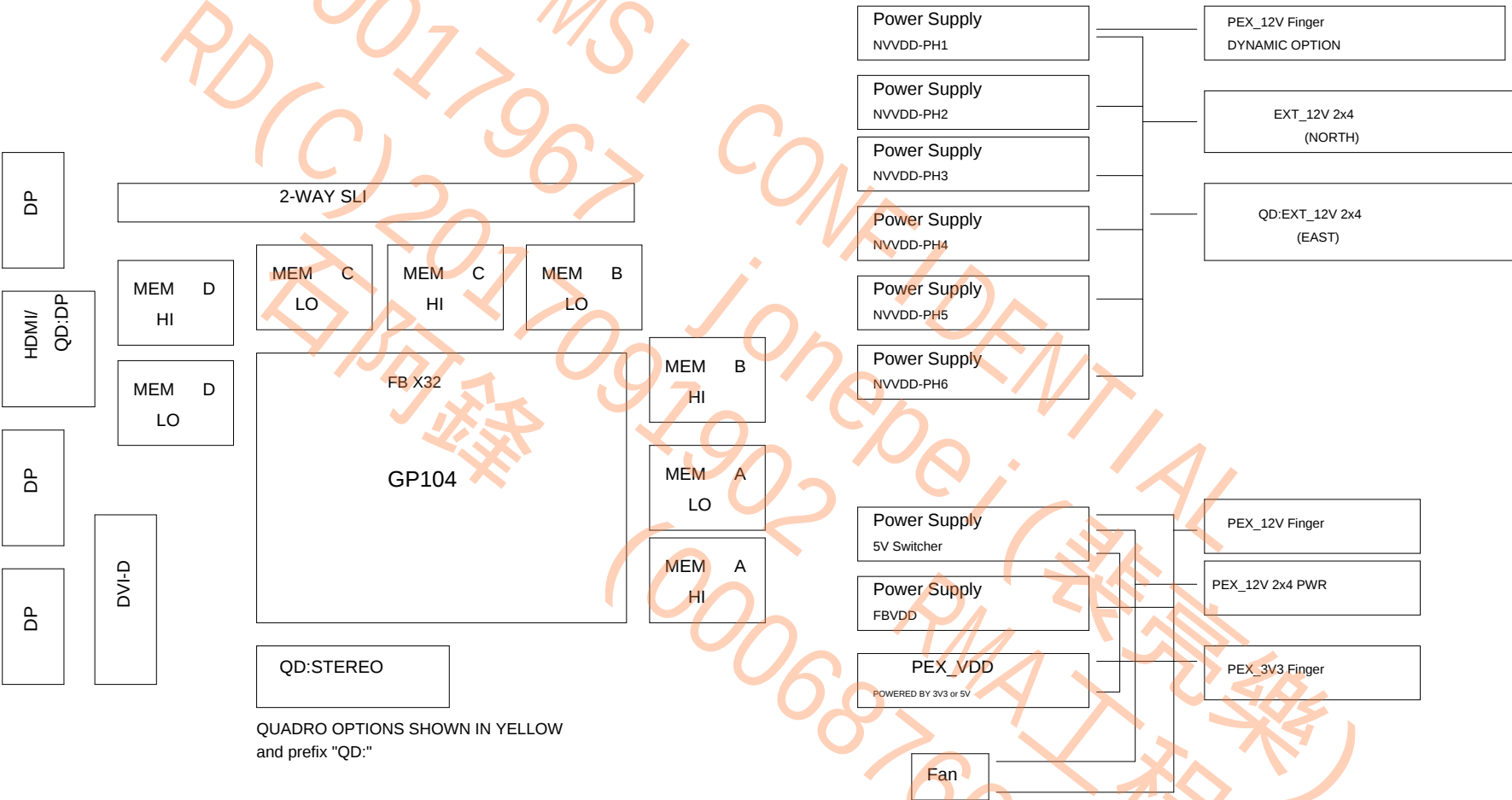


MICRO-STAR INT'L CO.,LTD

MS-V330

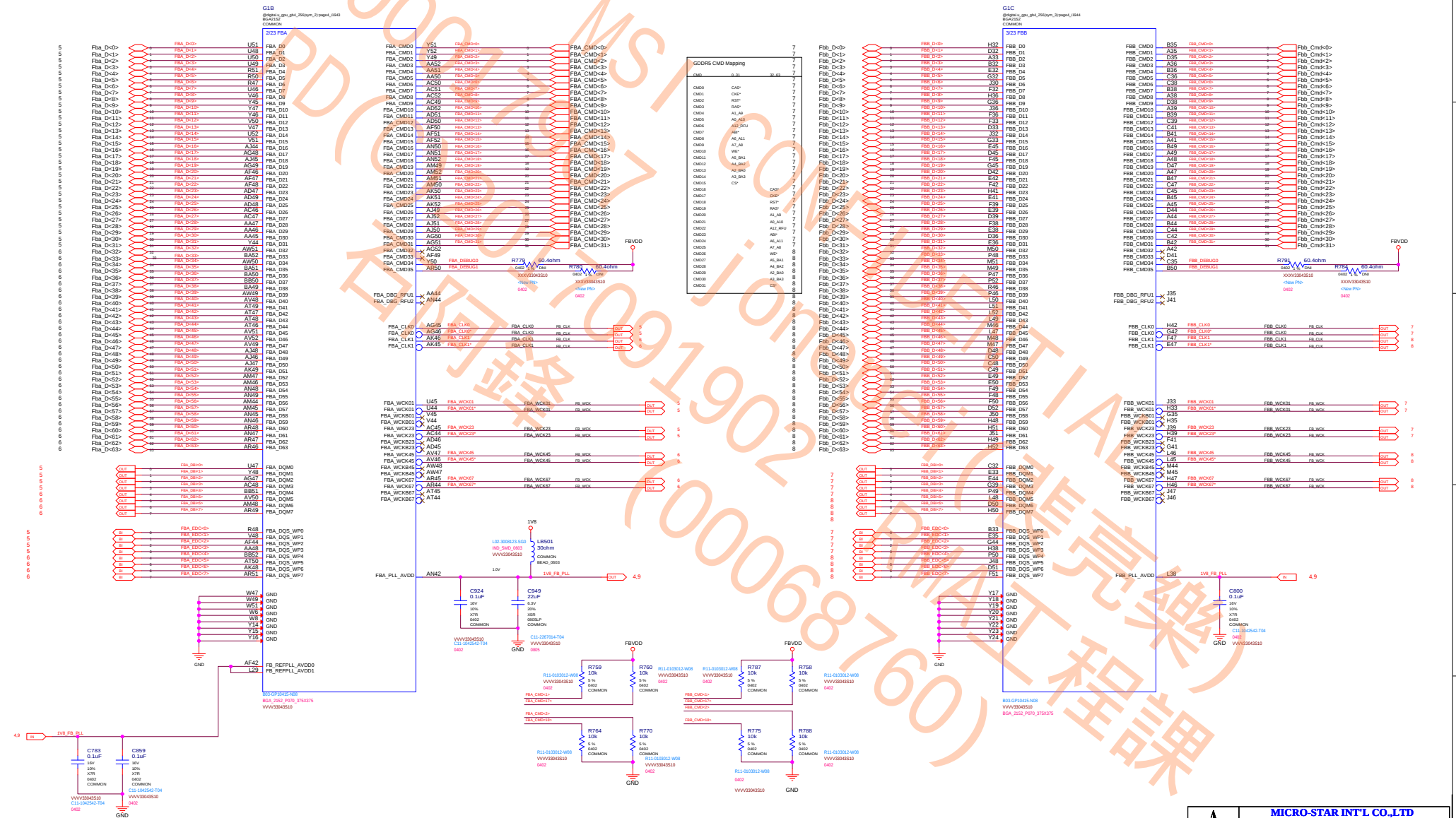
Size	Document Description	Rev
Custom	Table of Contents	6.1
Date: Wednesday, August 16, 2018		Sheet 1 of 39

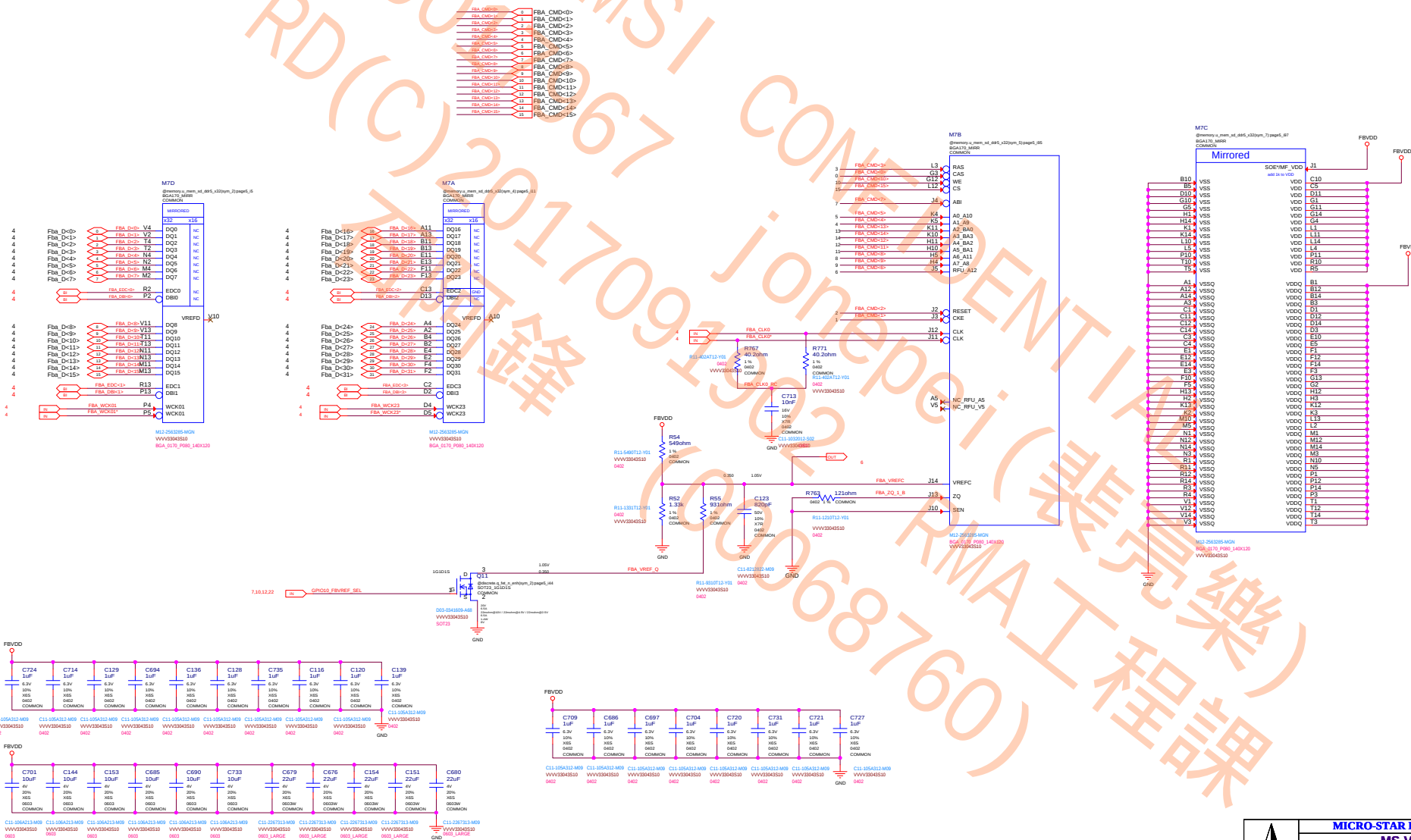


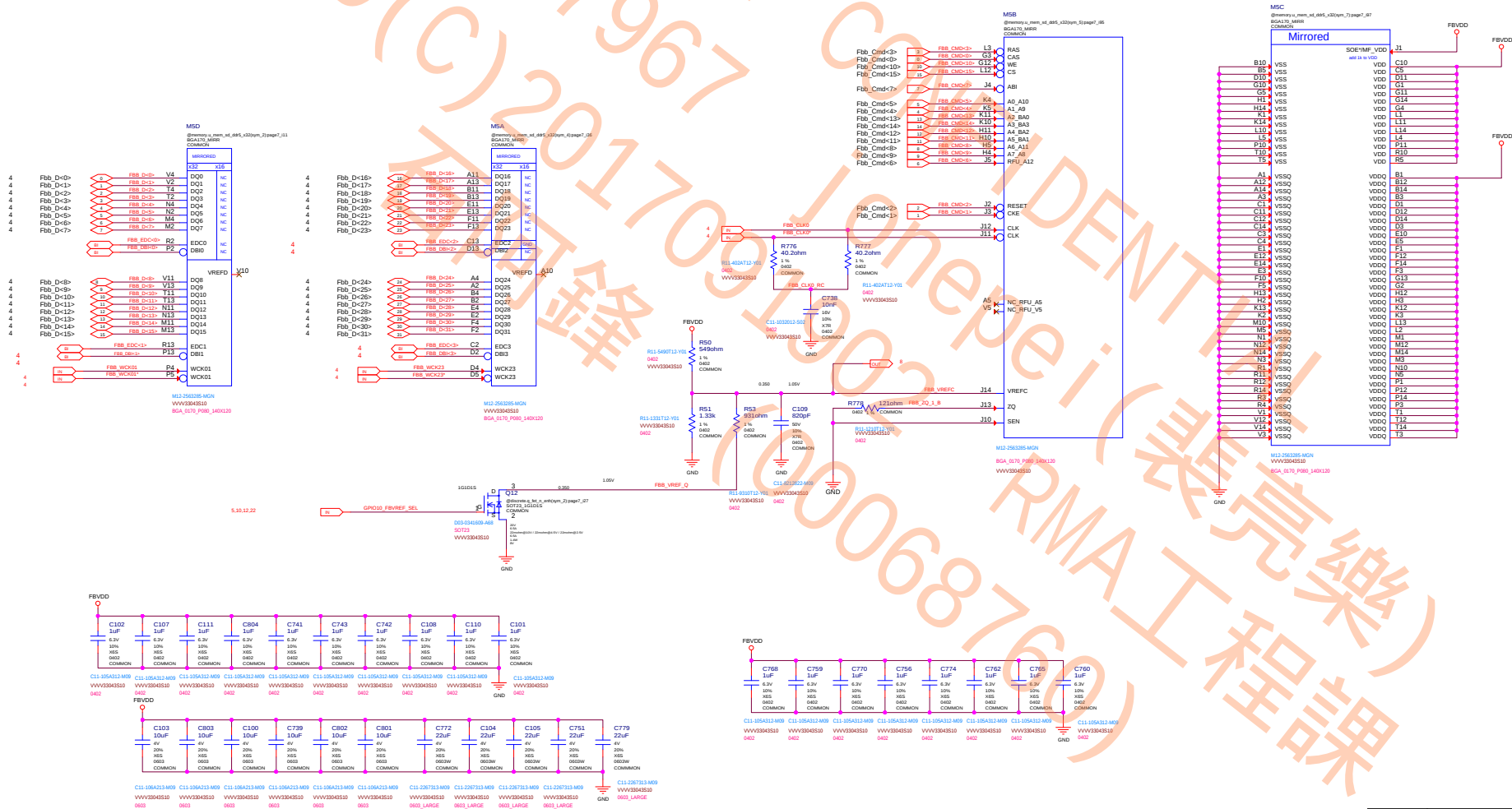


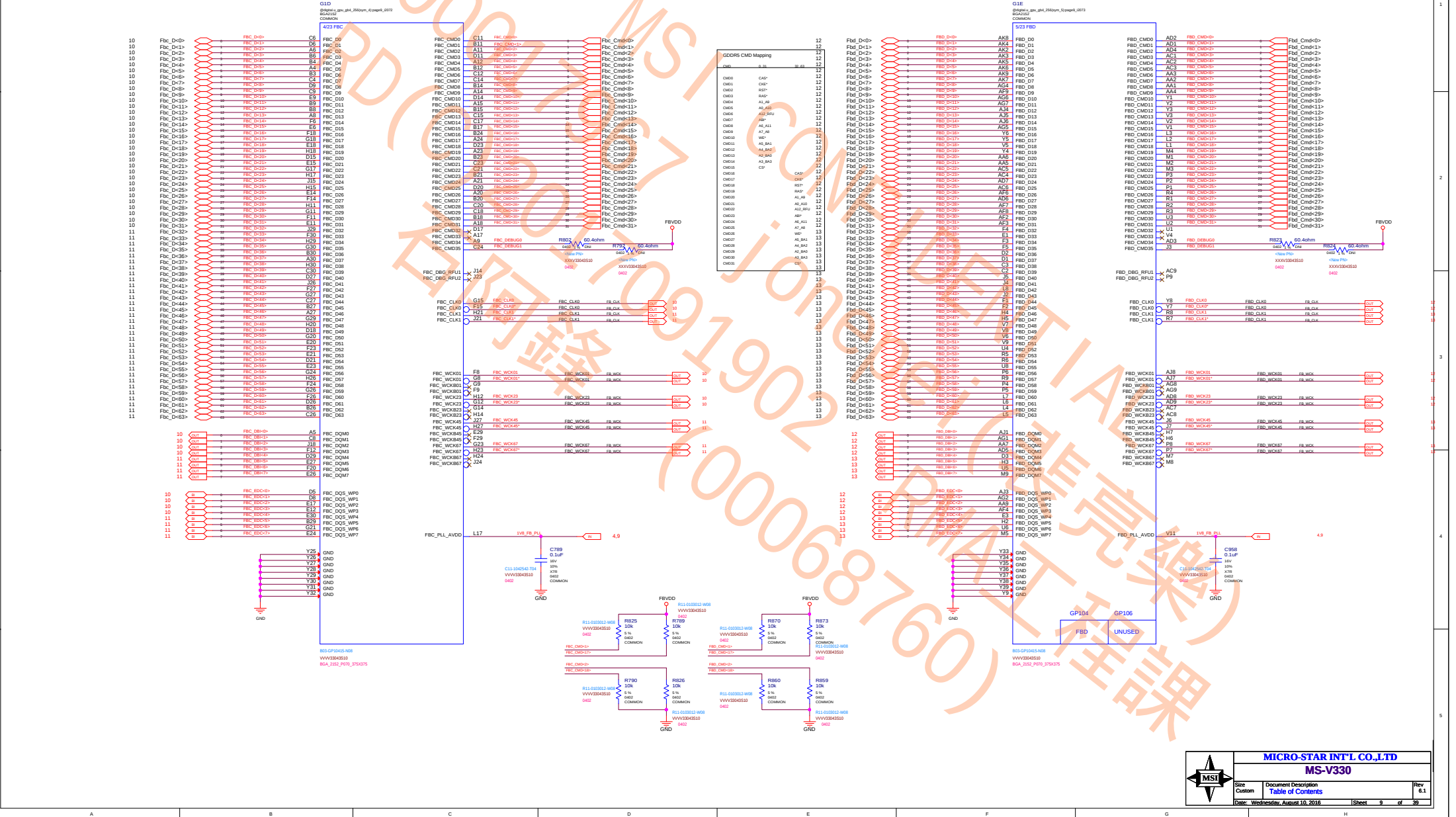
QUADRO OPTIONS SHOWN IN YELLOW
and prefix "QD:"



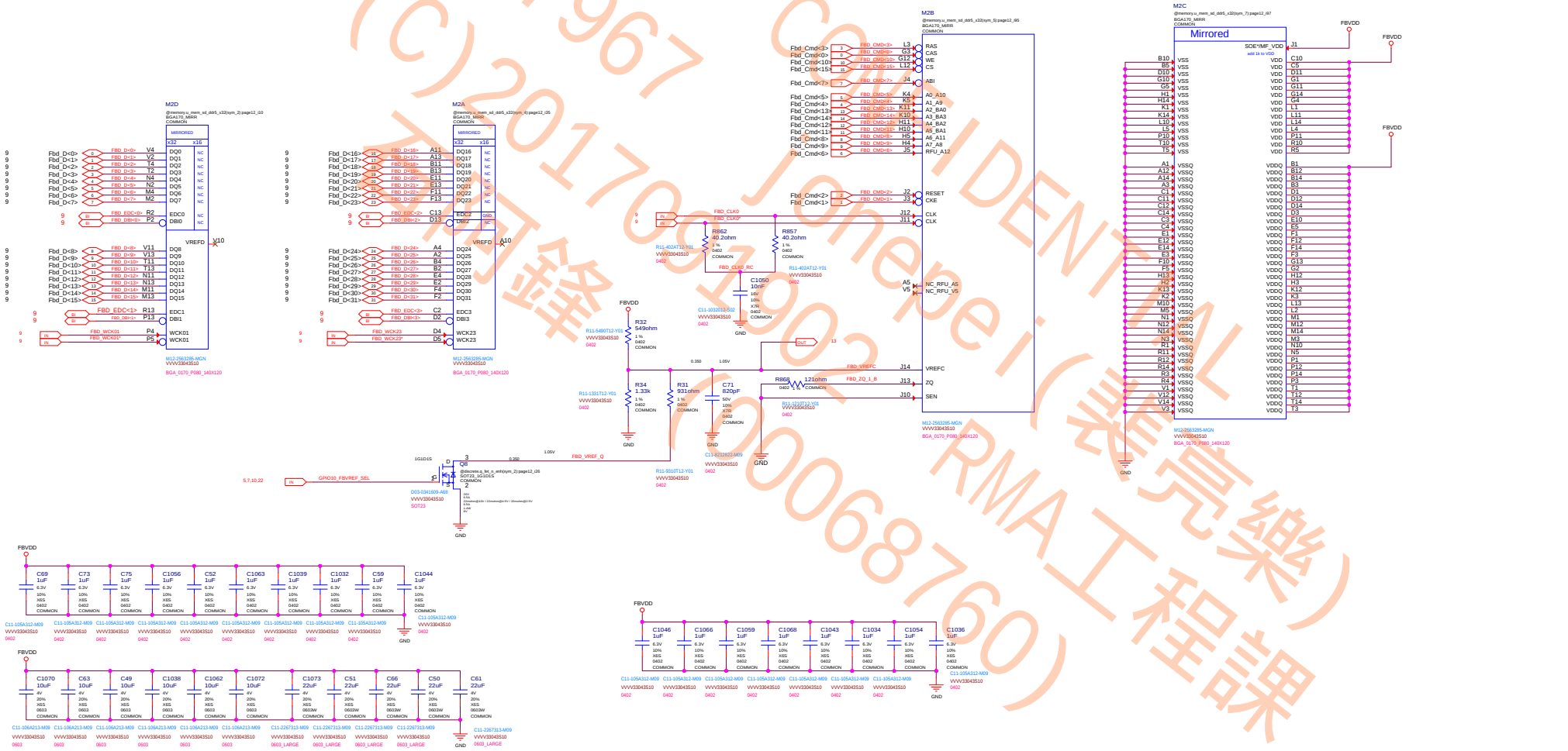














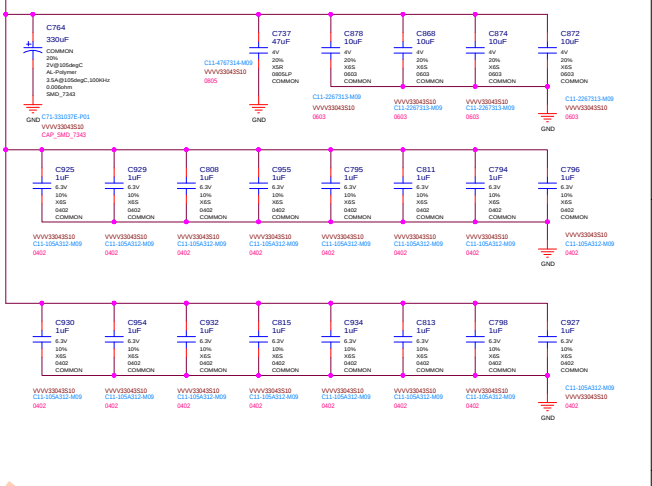
FBVDD



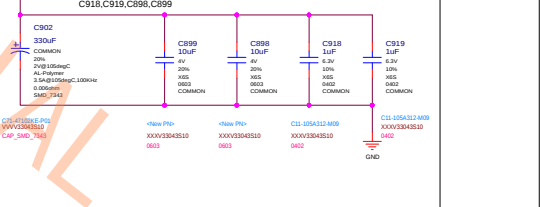
NVVD



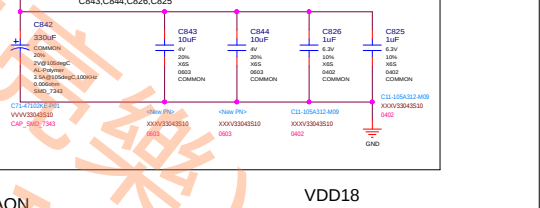
NVVD



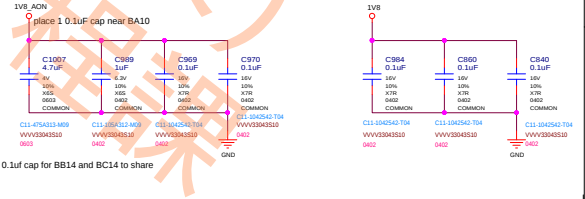
STUFF C902 OR C918,C919,C986,C999



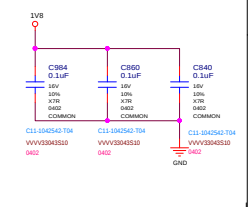
STUFF C842 OR C843,C844,C826,C825



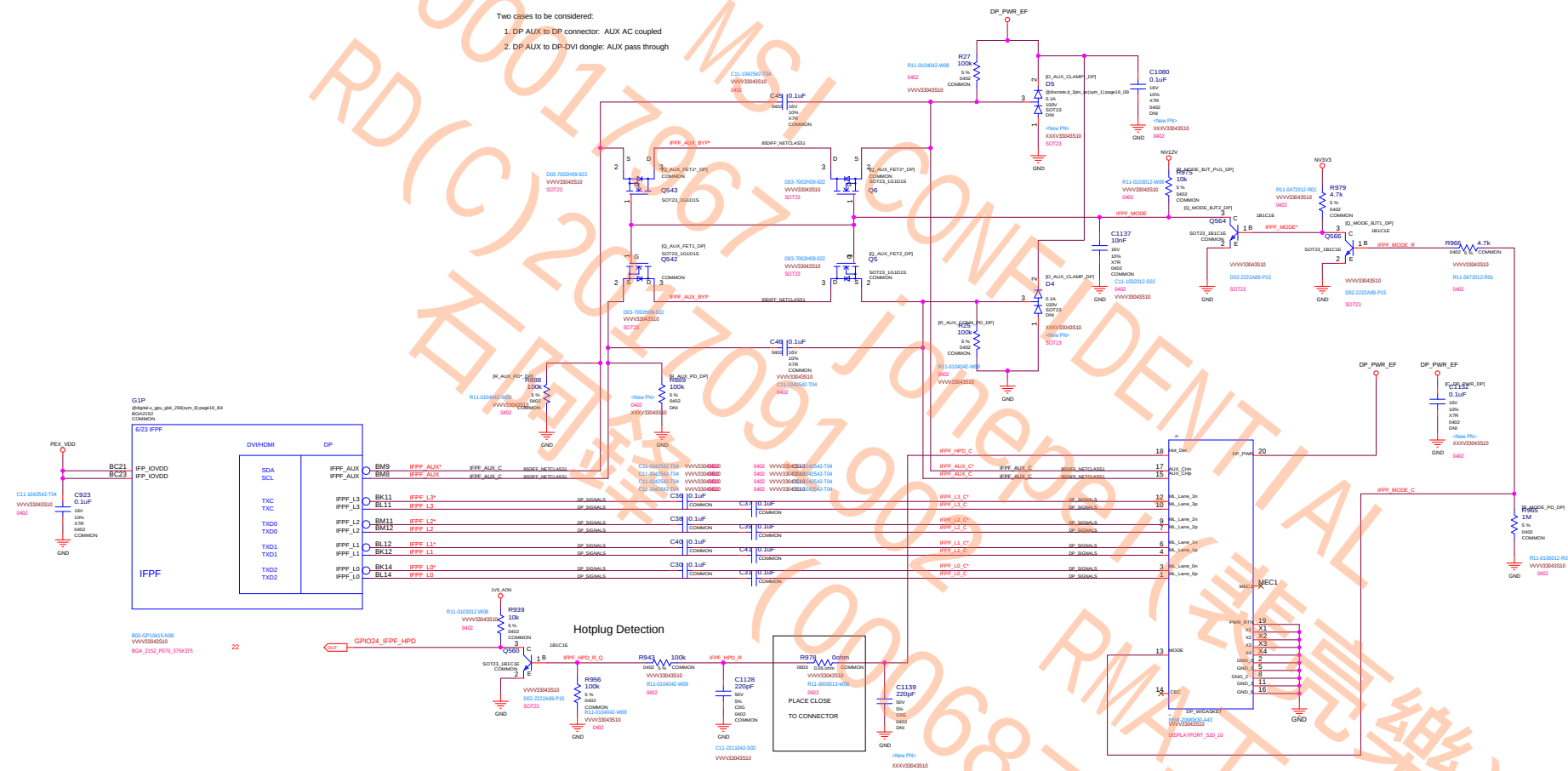
1V8_AON



VDD18

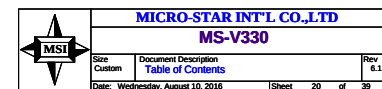
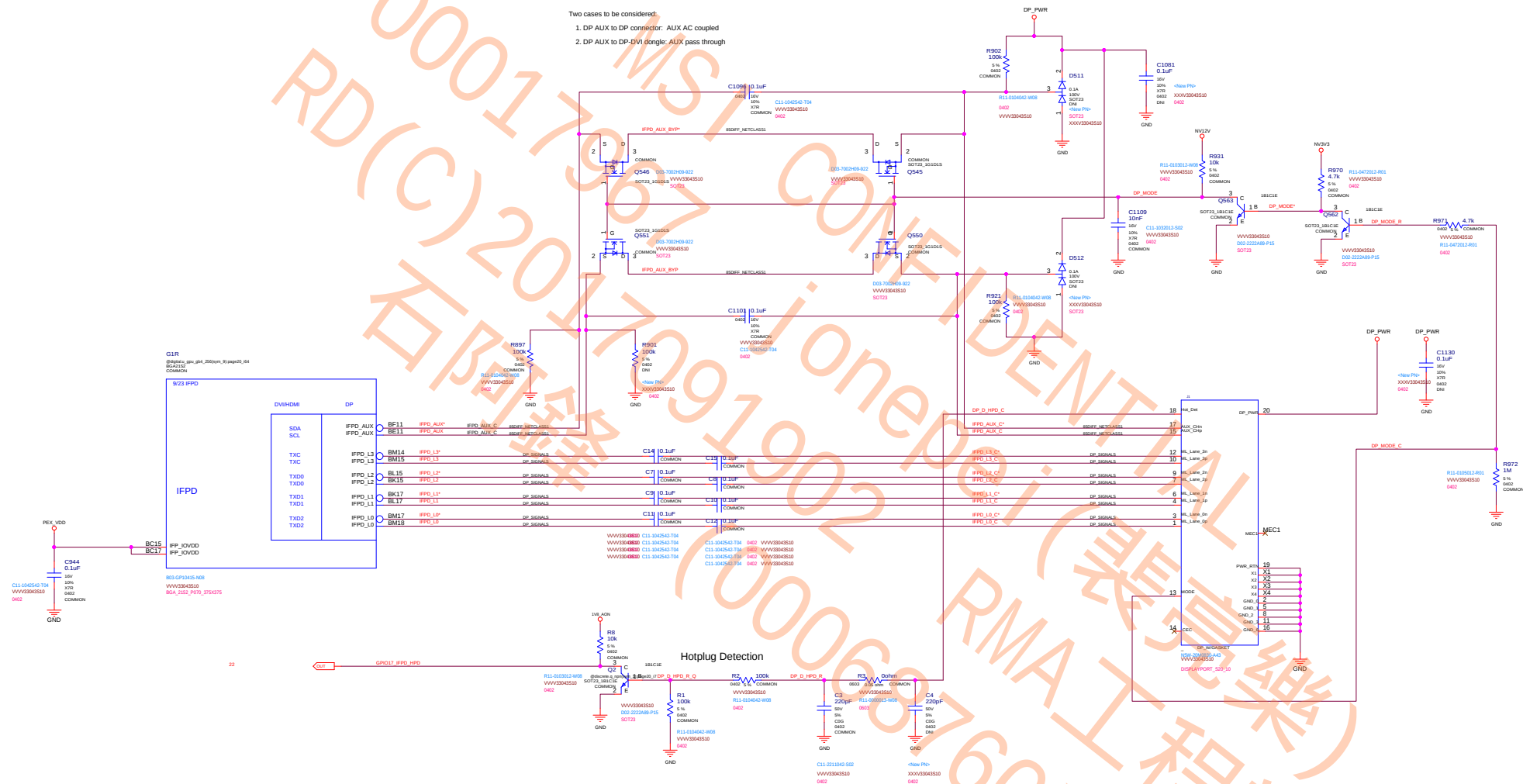


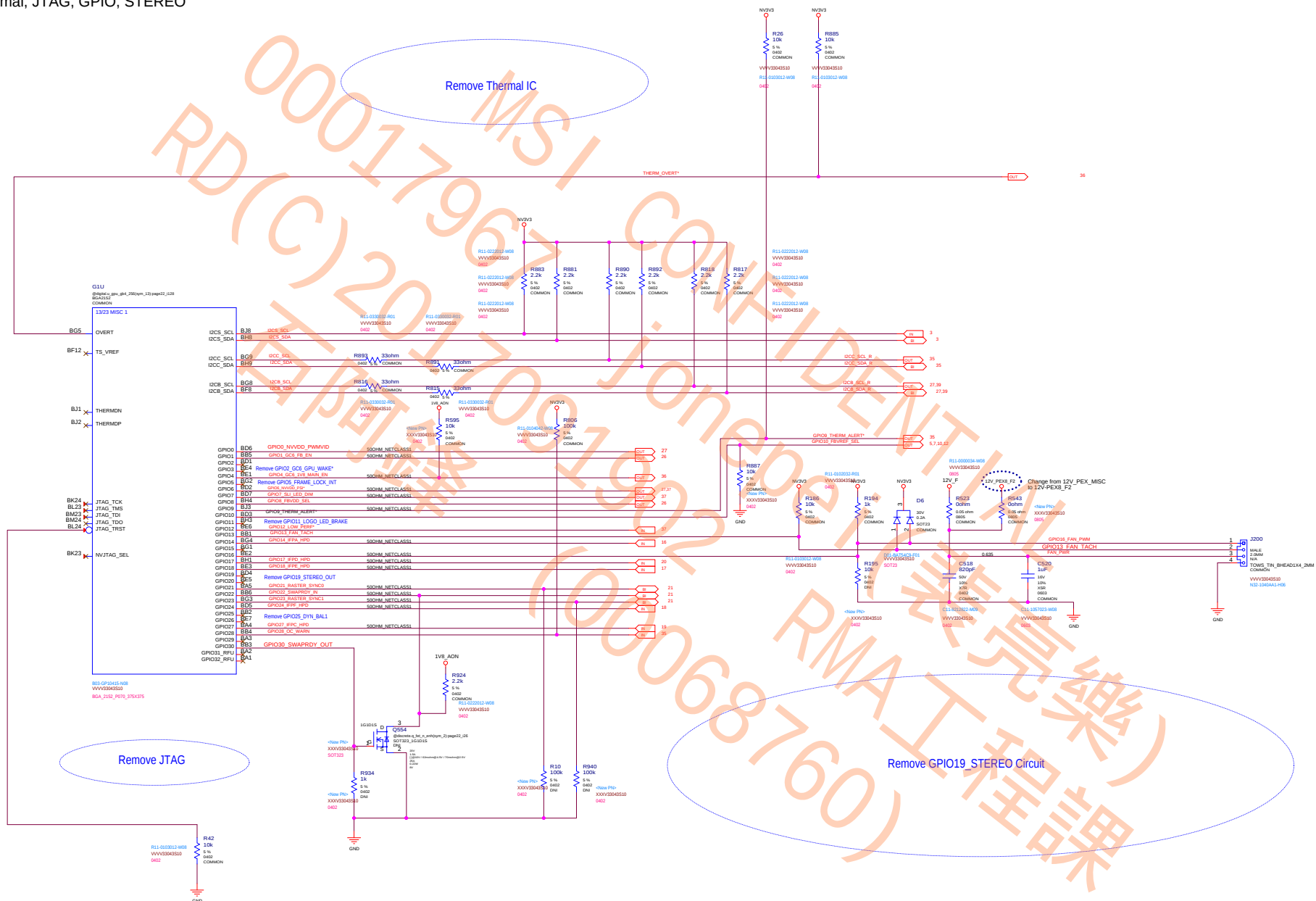
- Two cases to be considered:
- 1. DP AUX to DP connector: AUX AC coupled
 - 2. DP AUX to DP-DVI angle: AUX pass through



Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through





STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
L	L	L	1111 DEFAULT
L	L	H	1110
L	H	L	1101
L	H	H	1100
H	L	L	1011
H	L	H	1010
H	H	L	1001
H	H	H	1000
L	L	M	0111
L	M	L	0110
L	M	H	0101
L	H	M	0100
H	L	M	0011
H	M	L	0010
H	M	H	0001
H	H	M	0000

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

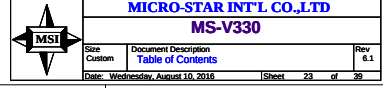
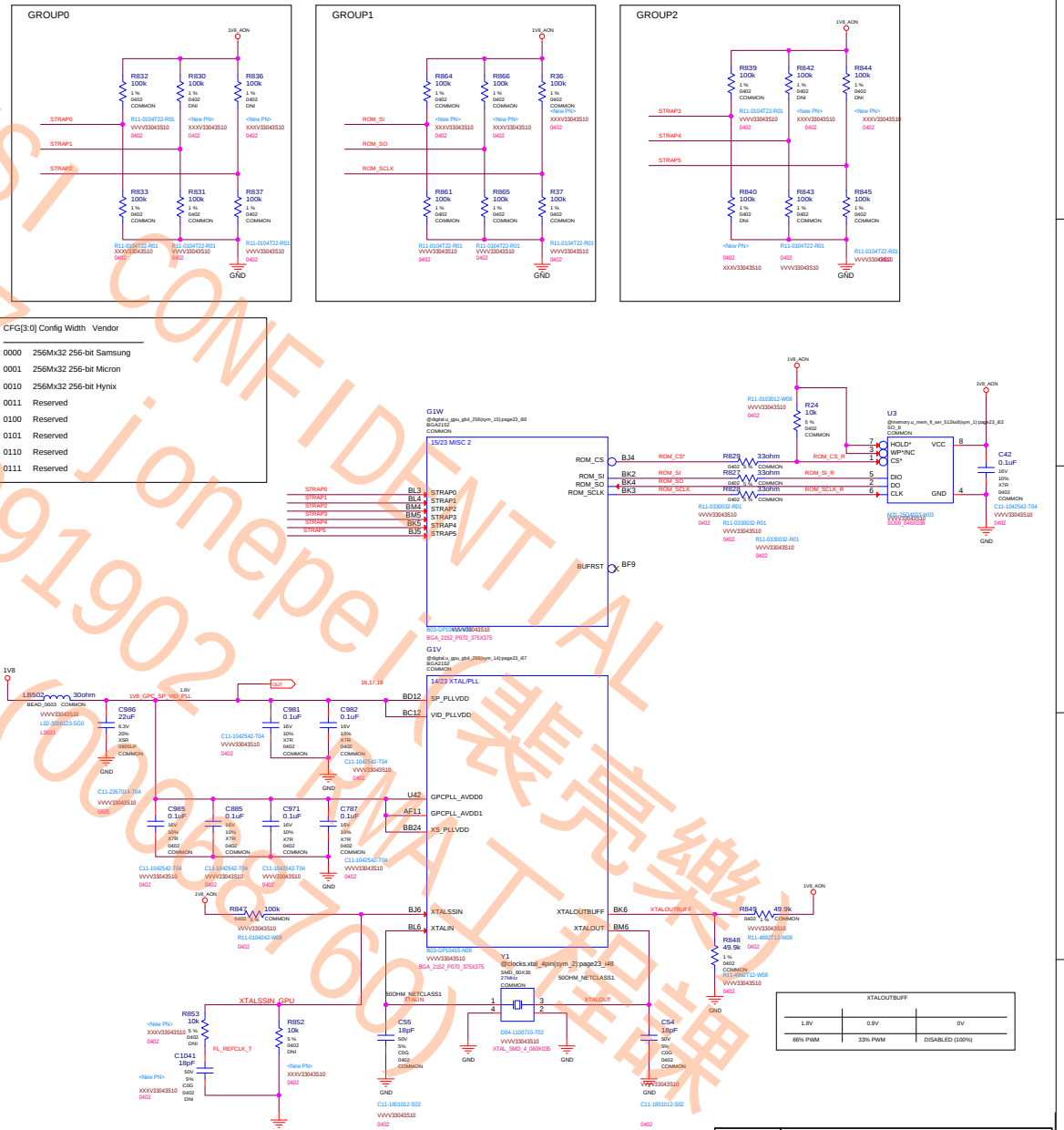
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

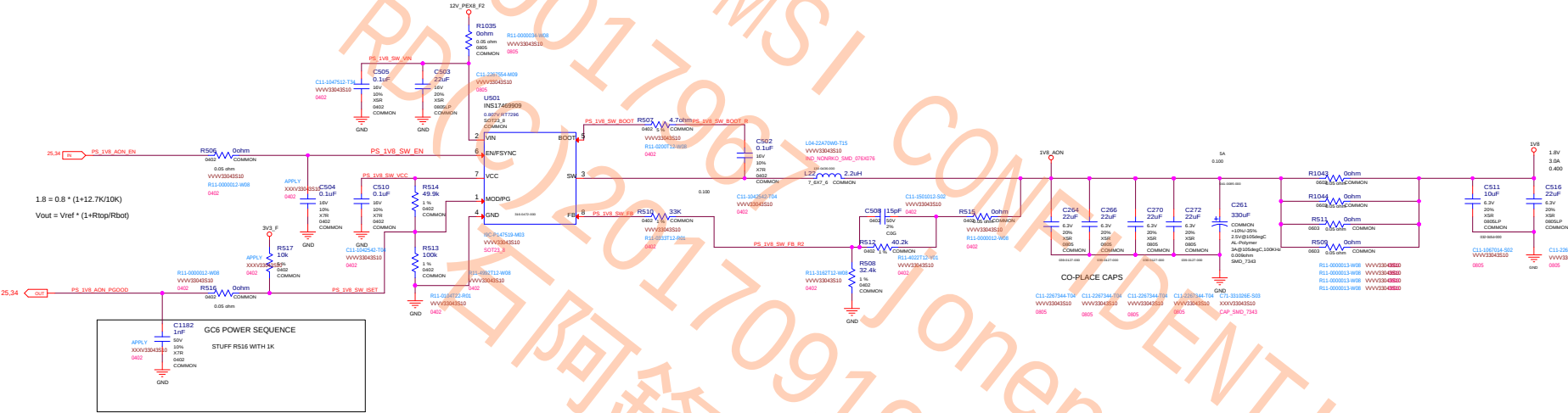
```
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

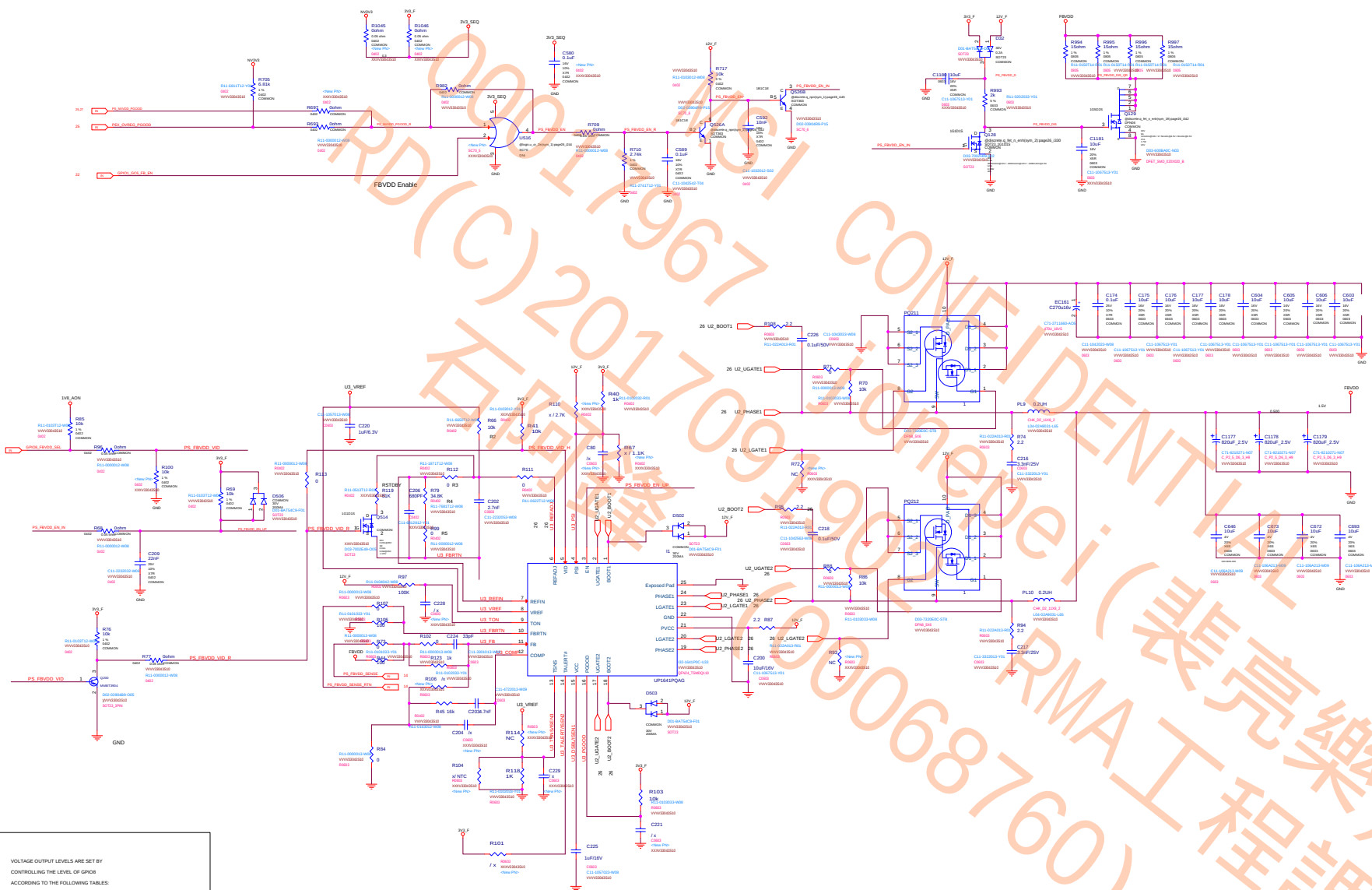
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL
```

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE





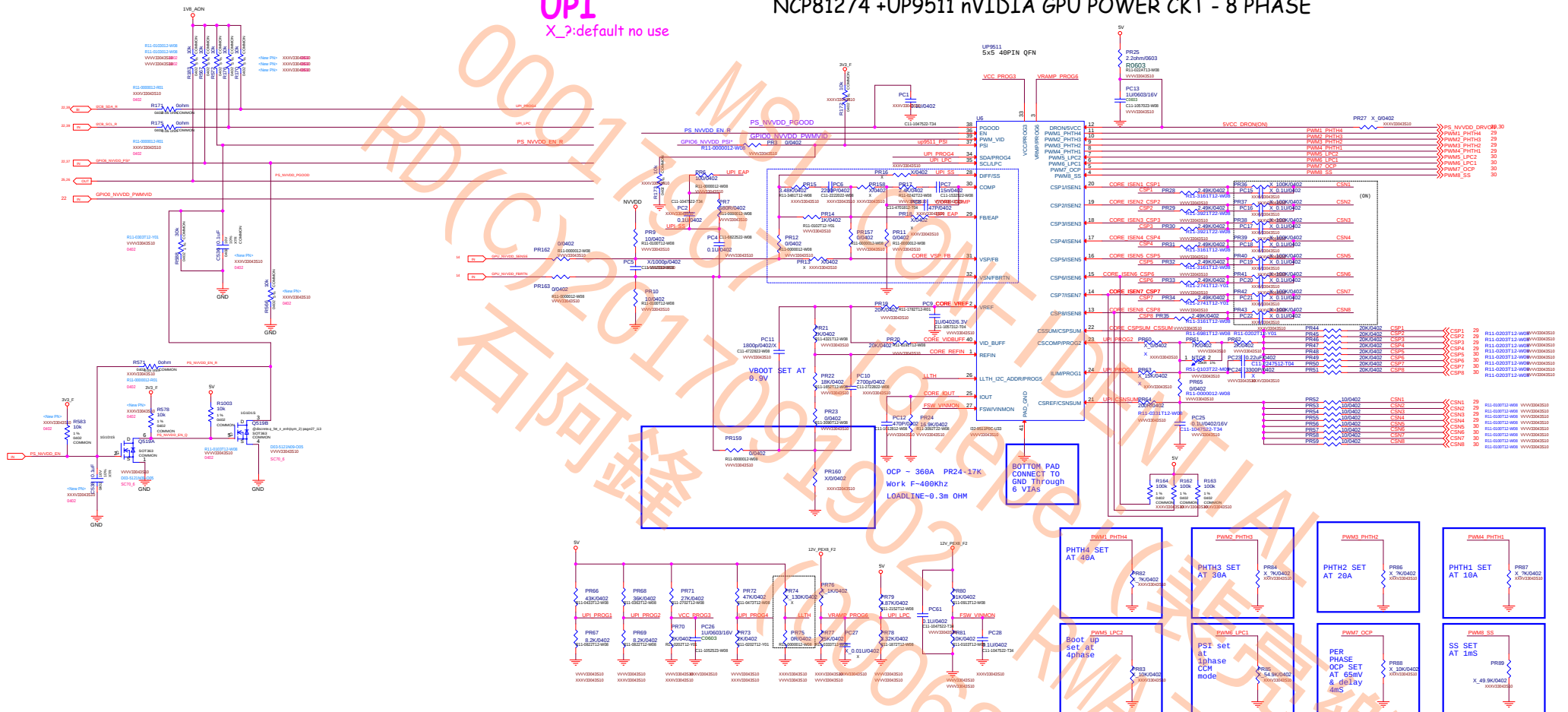


VOLTAGE OUTPUT LEVELS ARE SET BY
CONTROLLING THE LEVEL OF GPIOB
ACCORDING TO THE FOLLOWING TABLE

SAMSUNG K4G1325FC-HC28

GPIO8 LEVEL	FBVDD OUTPUT VOLTAGE
0	1.35V
1	1.55V

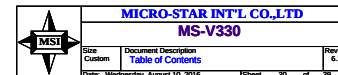
NCP81274 +UP9511 nVIDIA GPU POWER CKT - 8 PHASE



	MICRO-STAR INT'L CO.,LTD		
	MS-V330		
	Size Custom	Document Description <u>Table of Contents</u>	Rev 6.1
	Date: Wednesday, August 16, 2016		Sheet 27 of 39

MSI CONFIDENTIAL
00017967 jonepei (裴亮樂)
RD(C)2017091902 RMA工程課
石阿鋒 (00068760)

MICRO-STAR INT'L CO.,LTD		
MS-V330		
Size	Document Description	Rev
Custom	Table of Contents	6.1
Date: Wednesday, August 16, 2018		Sheet 28 of 39



MSI CONFIDENTIAL
00017967 jonepei (裴亮樂)
RD(C)2017091902 RMA工程課
石阿鋒 (00068760)

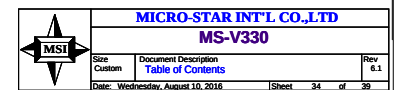
MICRO-STAR INT'L CO.,LTD		
MS-V330		
Size	Document Description	Rev
Custom	Table of Contents	6.1
Date: Wednesday, August 16, 2018		Sheet 31 of 39

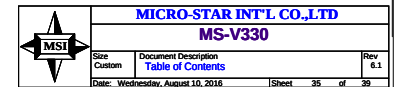
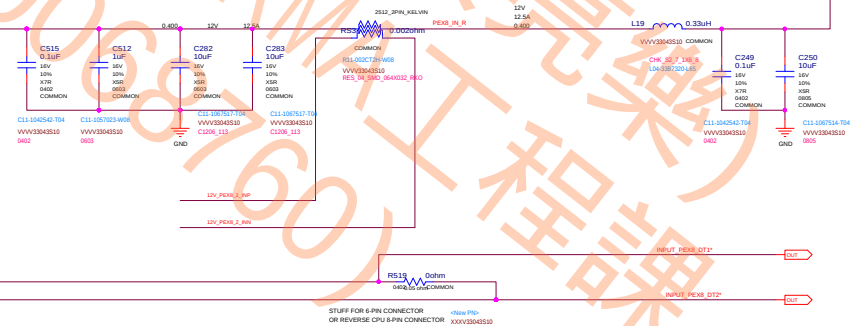
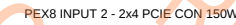
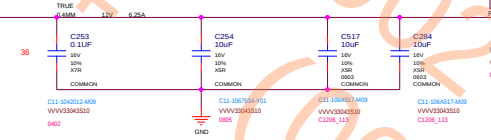
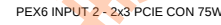
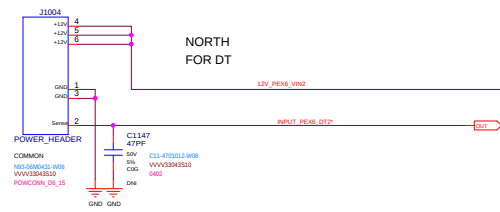
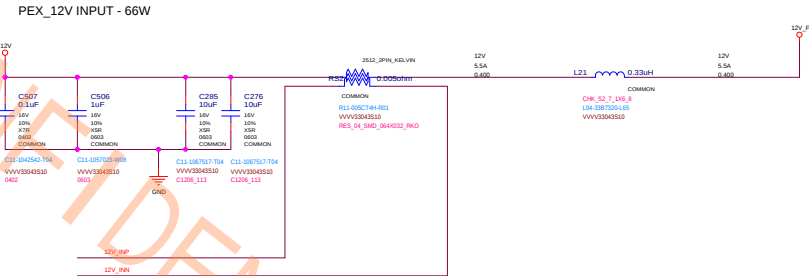
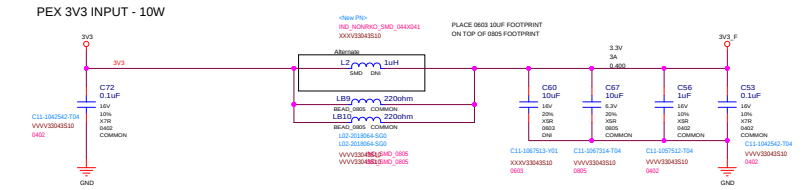
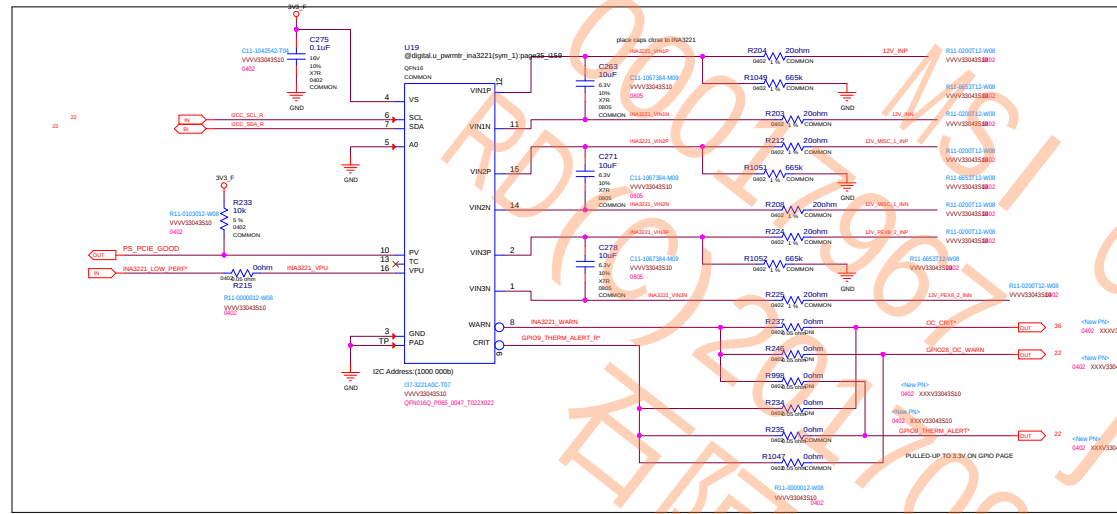
MSI CONFIDENTIAL
00017967 jonepei (裴亮樂)
RD(C)2017091902 RMA工程課
石阿鋒 (00068760)

MICRO-STAR INT'L CO.,LTD		
MS-V330		
Size	Document Description	Rev
Custom	Table of Contents	6.1
Date: Wednesday, August 16, 2018		Sheet 32 of 39

MSI CONFIDENTIAL
00017967 jonepei (裴亮樂)
RD(C)2017091902 RMA工程師
石阿鋒 (00068760)

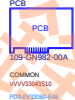
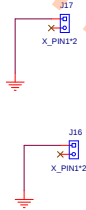
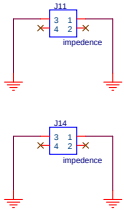
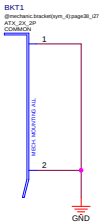
MICRO-STAR INT'L CO.,LTD		
MS-V330		
Size	Document Description	Rev
Custom	Table of Contents	6.1
Date: Wednesday, August 16, 2018		Sheet 33 of 39



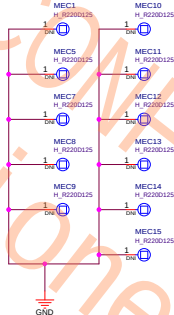




Brackets:



Mechanical Holes Symbol



GPU Stiffner

