PG301 A02

Comanche 192b GDDR5, <150W, 2-way SLI

Tall DVI-I + DP + DP + DP/HDMI + DP

TABLE OF CONTENTS

V320-2.0 change item:

Page15:DVI add esd

Page18:remove DP colay

Page20:HDMI add esd

Page21:4pin housing colay 6pin housing

Page25:NVVDD enable phase4

Page27:Add phase4

Page29:remove colay NVVDD power solution

Page30: 12V input bead change to choke
6pin power con colay 8pin con
remove 0603 MLCC colay

Page32:stuff logo LED

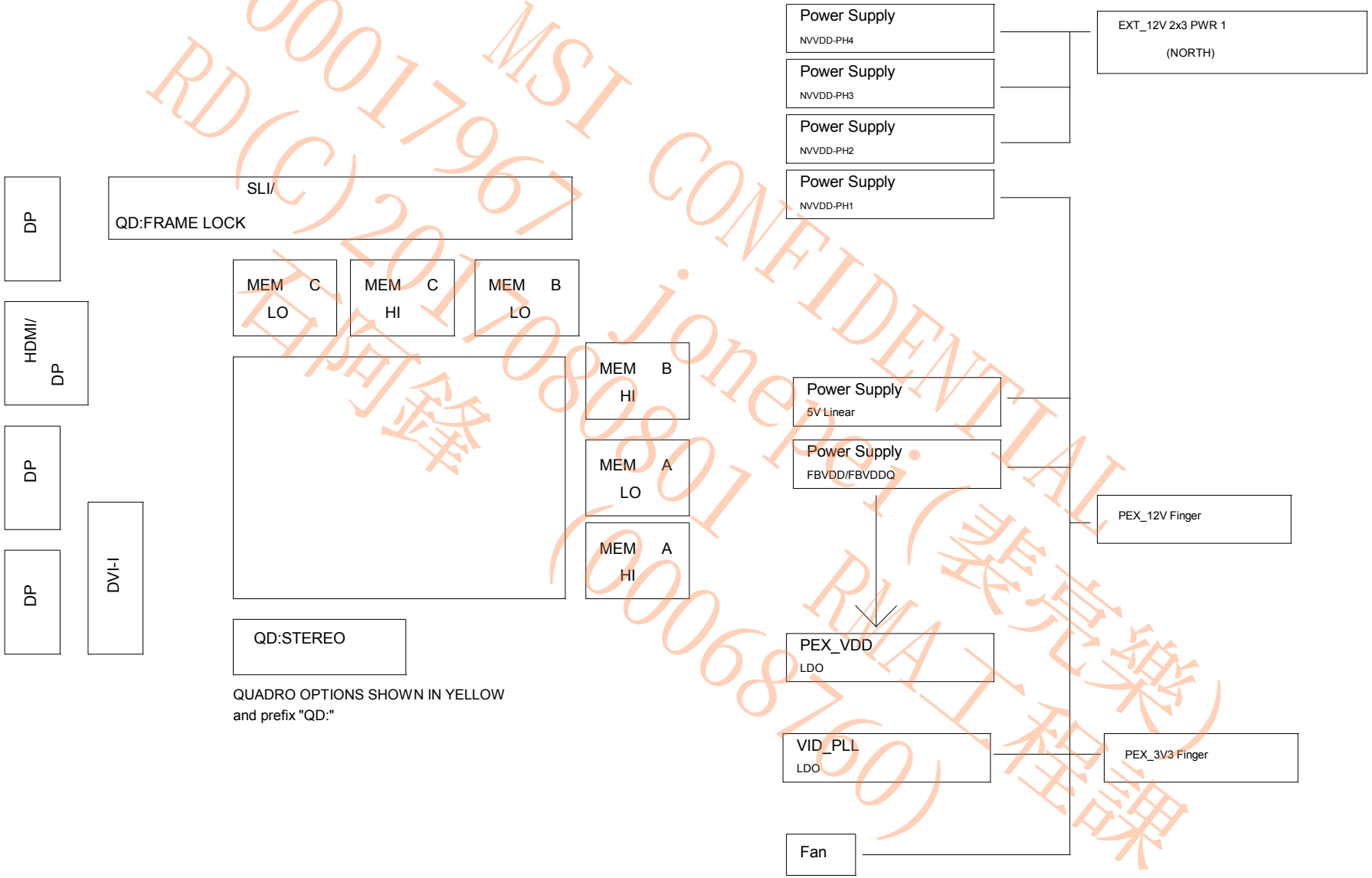
V330-1.0 change item:

All IOVDD/NV3V3 change to 3V3_F

Page03 : 1.Remoce JATG circuit
2.Remoce U502/Q518/R1669/R1670/R663
Page09 : Remove MEMORY_ GPU Partition C
Page10 : Remove MEMORY_ FBC[31_0]
Page11 : Remove MEMORY_ FBC[63_32]
Page14 : Remove R176 and connect to FB_PLLVDD
Page15 : 1. Remove LB502/R173/R174 and connect to FB_PLLVDD
2. Remove R171
3. Change J6 footprint
Page16 : 1.GPU pin AT8 connector to FB_PLLVDD
2.Remove IFPE DP circuit
Page17 : Remove IFPF DP circuit
Page18 : GPU pin AT13 connector to FB_PLLVDD
Page19 : GPU pin AT9 connector to FB_PLLVDD
Page20 : Remove FRAMELOCK circuit
Page21 : 1.Remove R183/R185/Q32
2.Remove R641/R642/R595/R555
3.Remove I2CB/GPIO4/GPIO8/GPIO11/GPIO18/GPIO19
4.Remove I2CC/I2CB/GPIO6/GPIO12/GPIO9 level shift
5.Remove JTAG

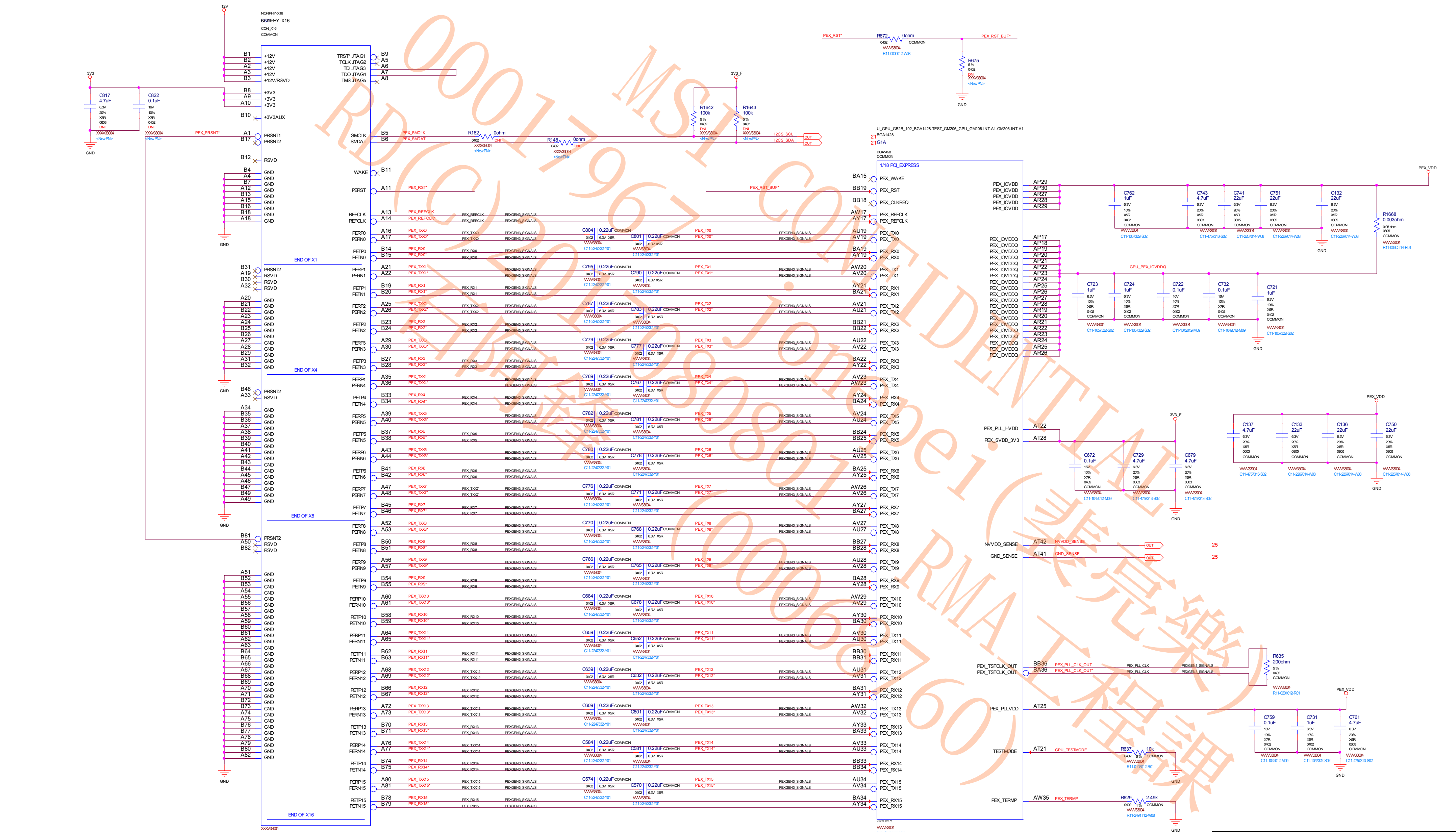
Page22 : 1.Remoce R628/R1641/R638/C740
2.Remoce GPU BUFRST*
Page23 : 1.Co-lay U12
2.C753 connector to PS1_1V_RS
Page24 : Change MOS and Choke
Page26 : Change MOS
Page27 : Change MOS
Page30 : 1.Change L20/L21 footprint
2.Add 12V Current Steering circuit
3.Remove some input MLCC
Page31 : Remove R147/R151/R142/R143/R145
Page32 : 1.Remove Logo LED circuit
2.Remove IFP_IOVDD circuit
3.Remove R2/DS1
Page33 : 1.Remove IOVDD Regulator circuit
2.Remove R585/R581/R9
Page34 : Change BKT1 footprint

Block Diagram



MICRO-STAR INT'L CO.,LTD
MS-V330
Size: Custom | Document Description: 02_Block Diagram | Rev: 2.1
Date: Tuesday, February 02, 2016 | Sheet 2 of 35

PCI Express



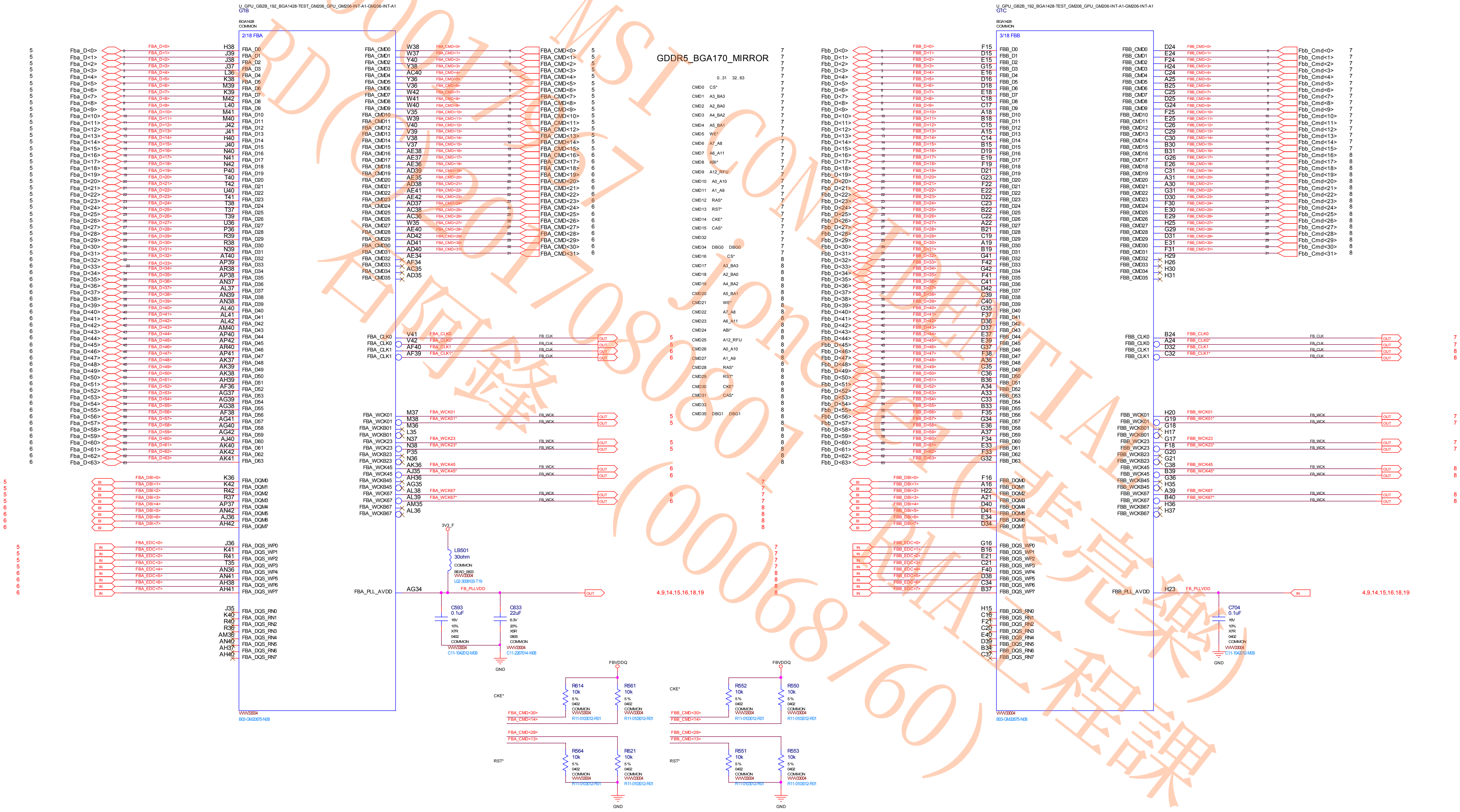
MICRO-STAR INT'L CO.,LTD

MS-V330

Size	Document Description	Rev
Custom	03_PCI Express	2.1

Date: Tuesday, February 02, 2016 | Sheet 3 of 35

MEMORY: GPU Partition A/B



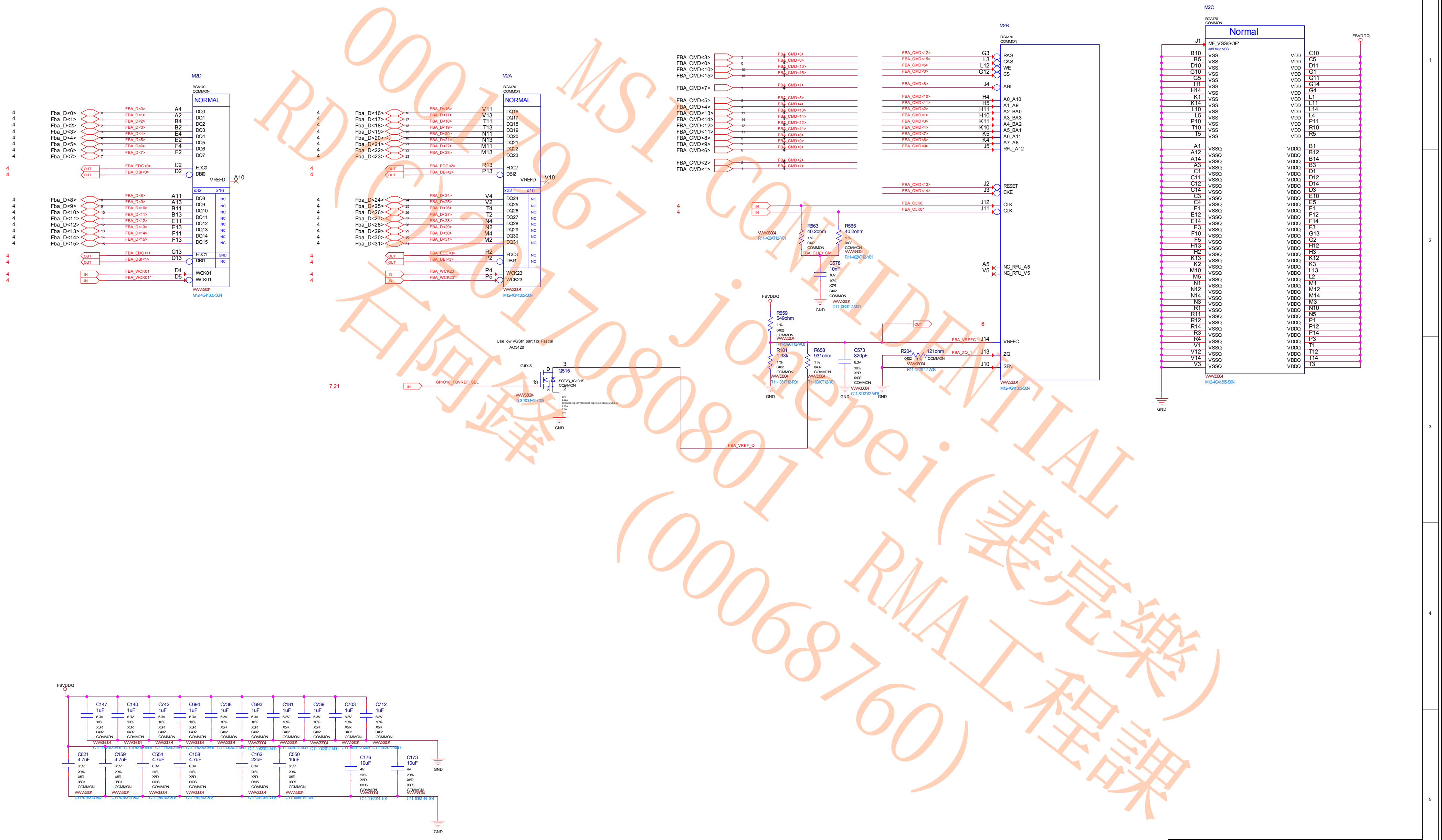
MICRO-STAR INT'L CO.,LTD

MS-V330

Size	Document Description	Rev
Custom	04_MEMORY_GPU Partition A_B	2.1

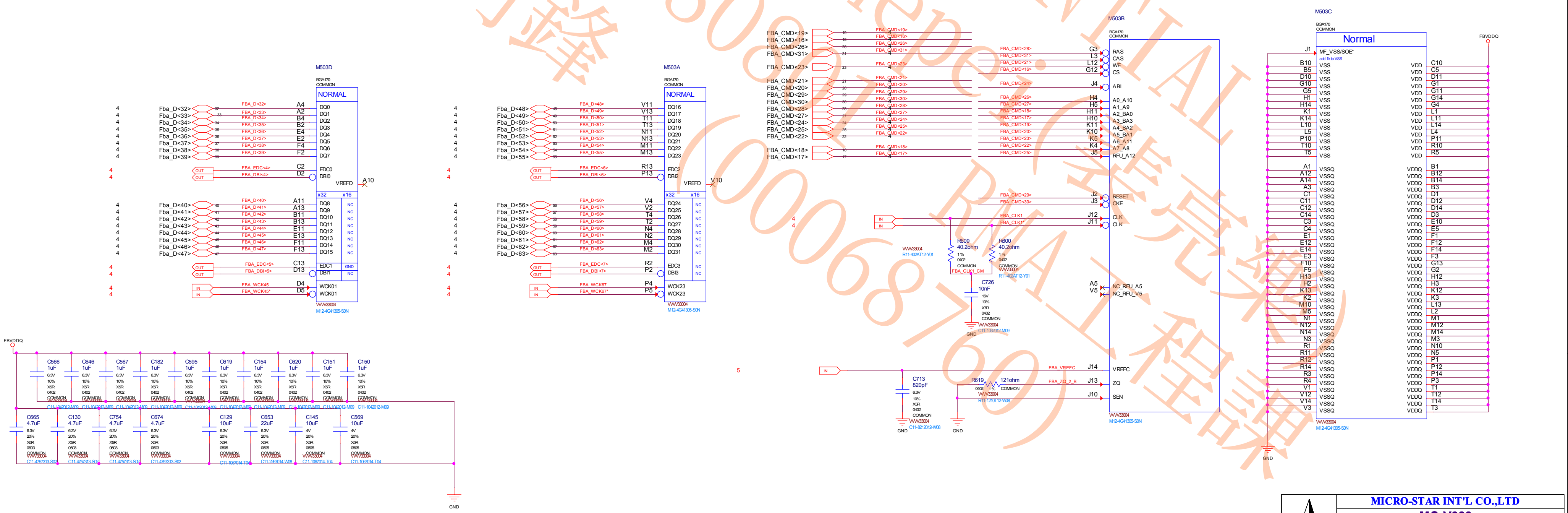
Date: Tuesday, February 02, 2016 Sheet 4 of 35

MEMORY: FBA Partition 31..0



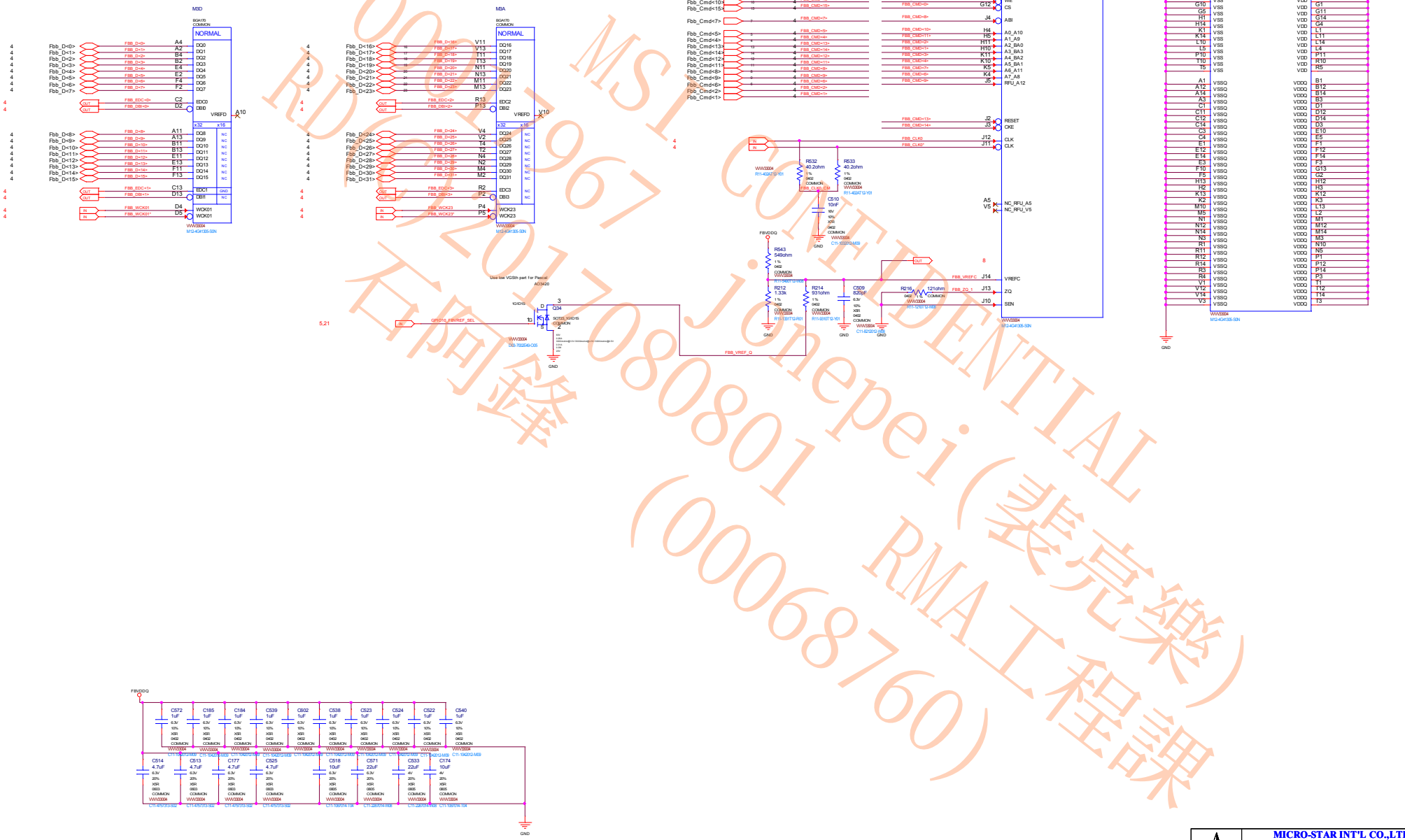
MICRO-STAR INT'L CO.,LTD			
MS-V330			
Size: Custom	Document Description: 05_MEMORY_FBA[31_0]		Rev: 2.1
Date: Tuesday, February 02, 2016		Sheet 5 of 35	

MEMORY: FBA Partition 63..32

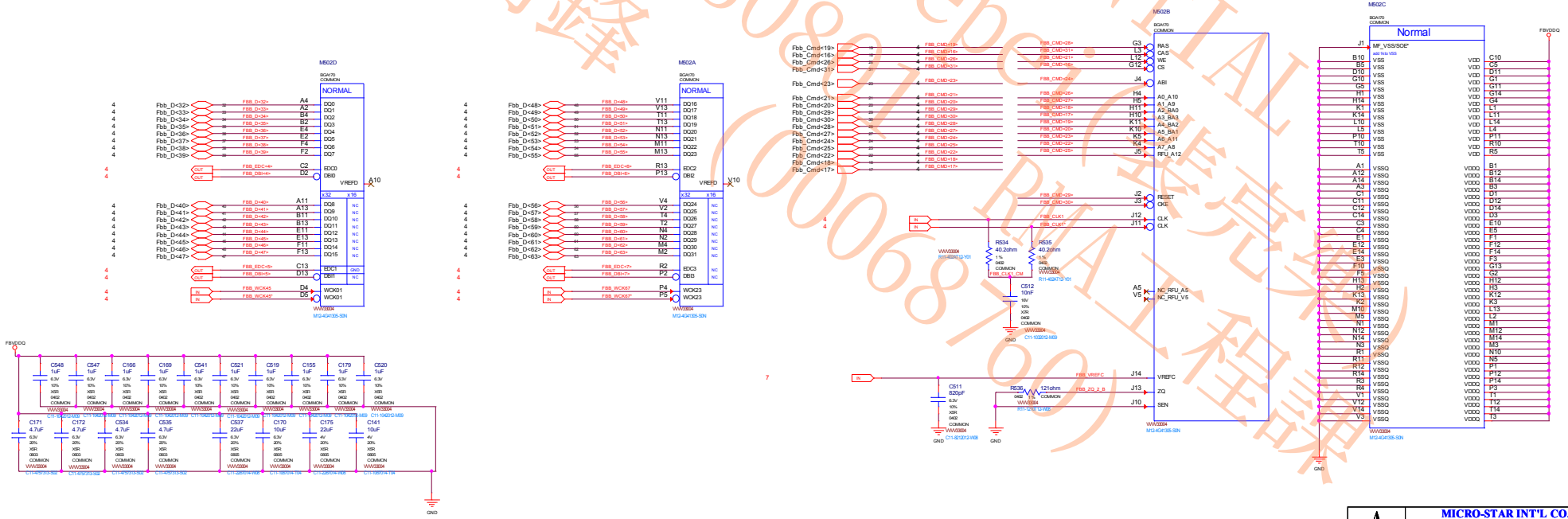


MICRO-STAR INT'L CO.,LTD		
MS-V330		
Size: Custom	Document Description: 06_MEMORY_FBA[63_32]	Rev: 2.1
Date: Tuesday, February 02, 2016	Sheet 6 of 35	

MEMORY: FBB Partition 31..0



MEMORY: FBB Partition 63..32



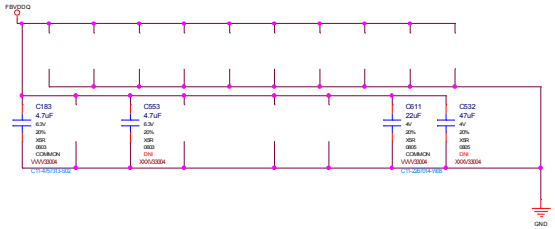
MICRO-STAR INT'L CO.,LTD		
MS-V330		
Size: Custom	Document Description: 08_MEMORY_FBB[63_32]	Rev: 2.1
Date: Tuesday, February 02, 2016	Sheet 8 of 35	

MEMORY: GPU Partition C/D

GDDR5_BGA170_MIRROR

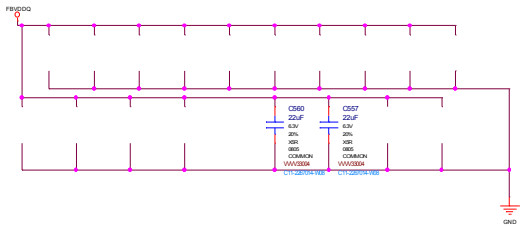
MICRO-STAR INT'L CO.,LTD		
MS-V330		
Size: Custom	Document Description: 09_MEMORY_GPU Partition C	Rev: 2.1
Date: Tuesday, February 02, 2016	Sheet 9 of 35	

MEMORY: FBC Partition 31..0



MSI	MICRO-STAR INT'L CO.,LTD		
	MS-V330		
Size: Custom	Document Description: 10_MEMORY_FBC[31_0]		Rev: 2.1
Date: Tuesday, February 02, 2016		Sheet 10 of 35	

MEMORY: FBC Partition 63..32

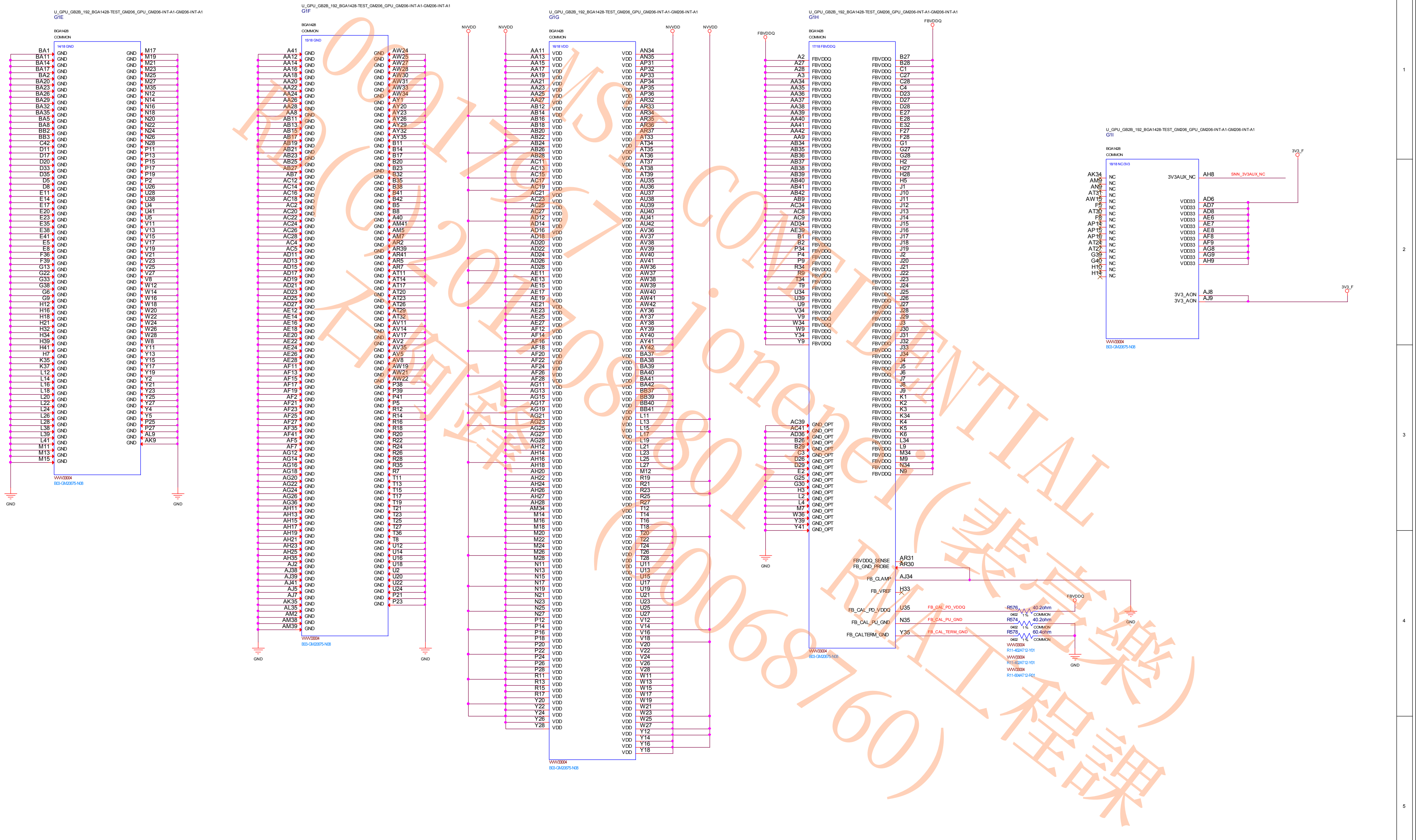


MICRO-STAR INT'L CO.,LTD
MS-V330

Size	Document Description	Rev
Custom	11_MEMORY_FBC[63_32]	2.1

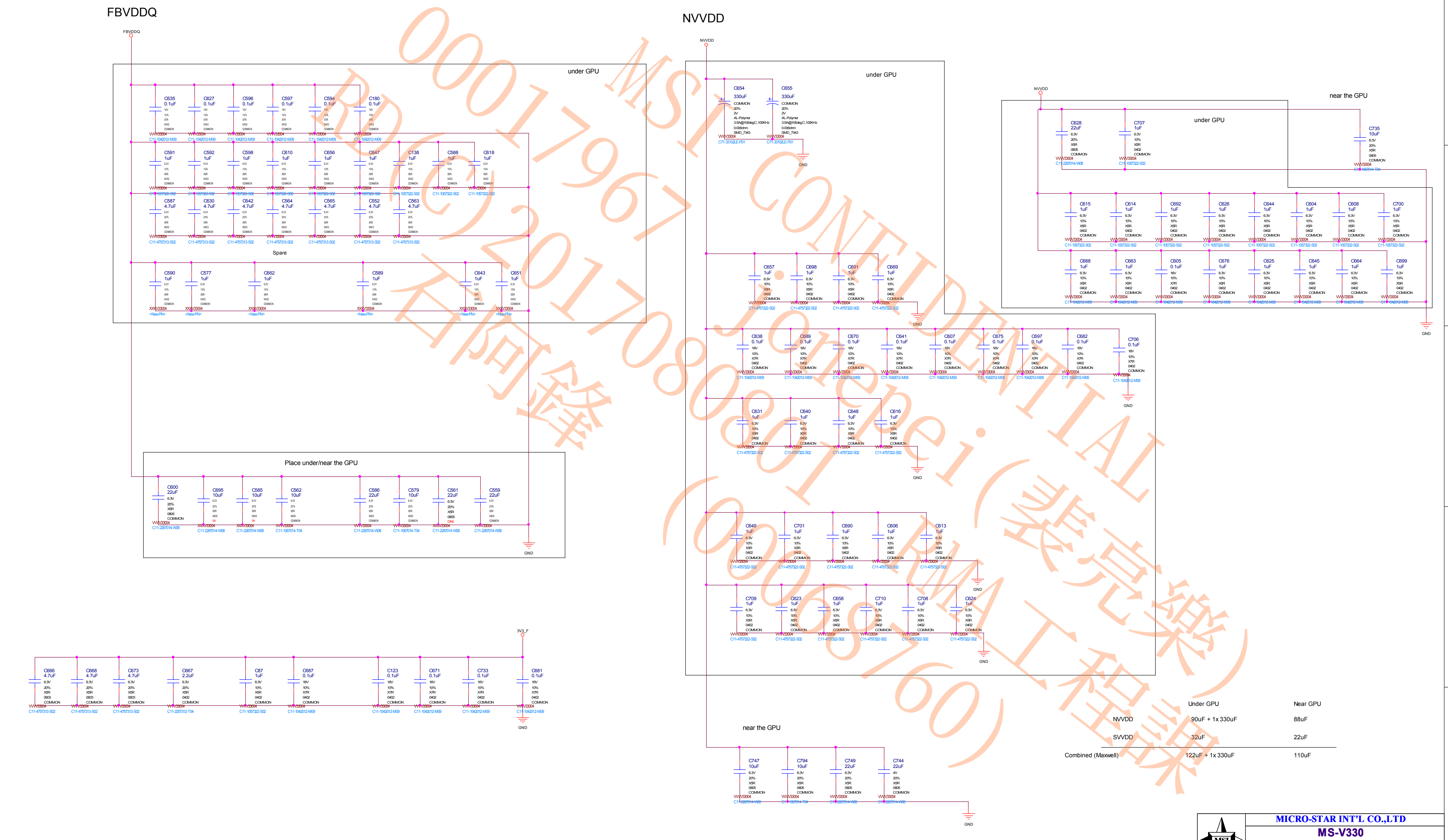
Date: Tuesday, February 02, 2016 Sheet 11 of 35

GPU PWR and GND



MICRO-STAR INT'L CO.,LTD		
MS-V330		
Size: Custom	Document Description: 12_GPU PWR and GND	Rev: 2.1
Date: Tuesday, February 02, 2016	Sheet 12 of 35	

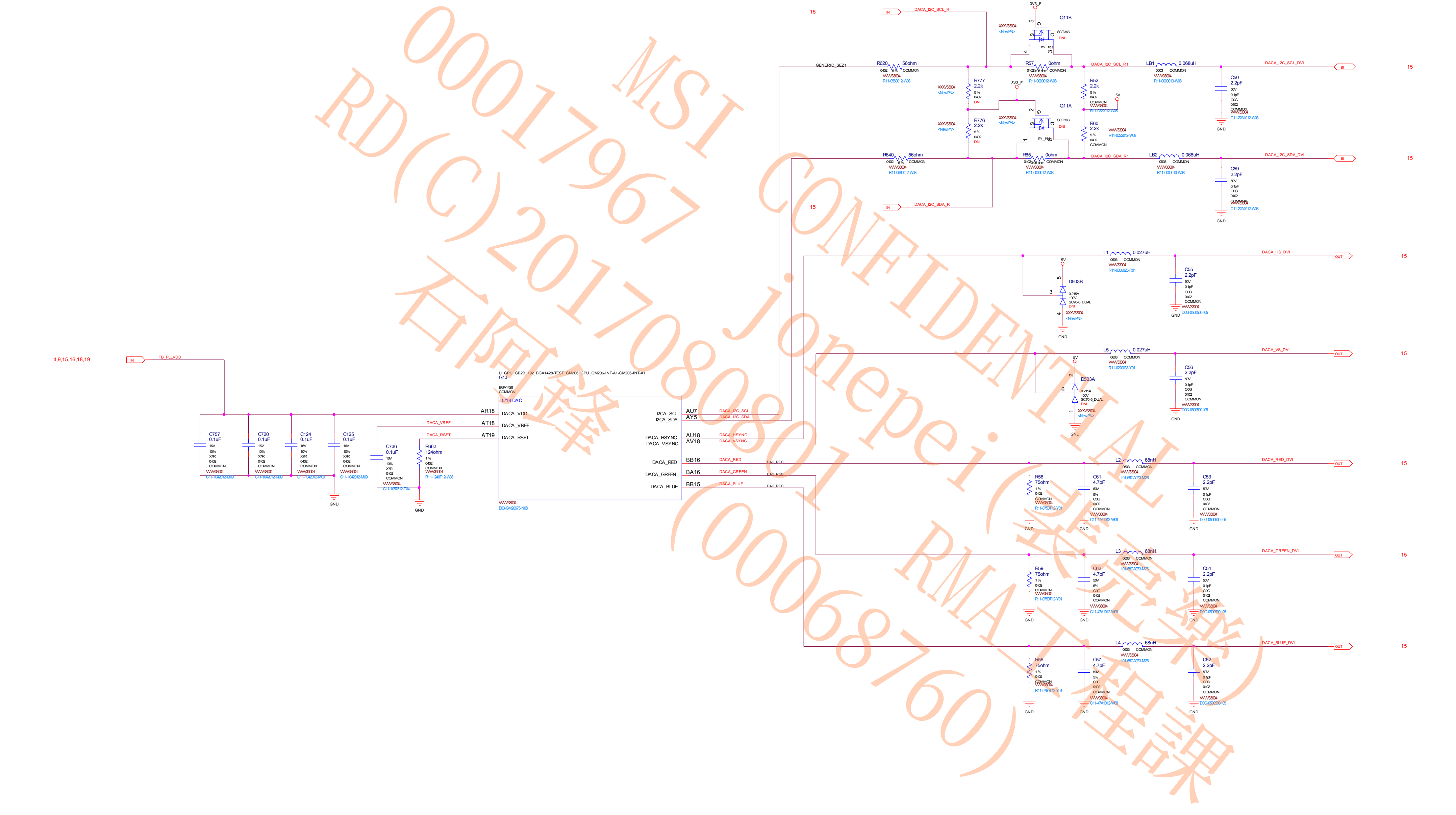
GPU Decoupling



	Under GPU	Near GPU
NVVDD	90uF + 1x 330uF	88uF
SVVDD	32uF	22uF
Combined (Maxwell)	122uF + 1x 330uF	110uF

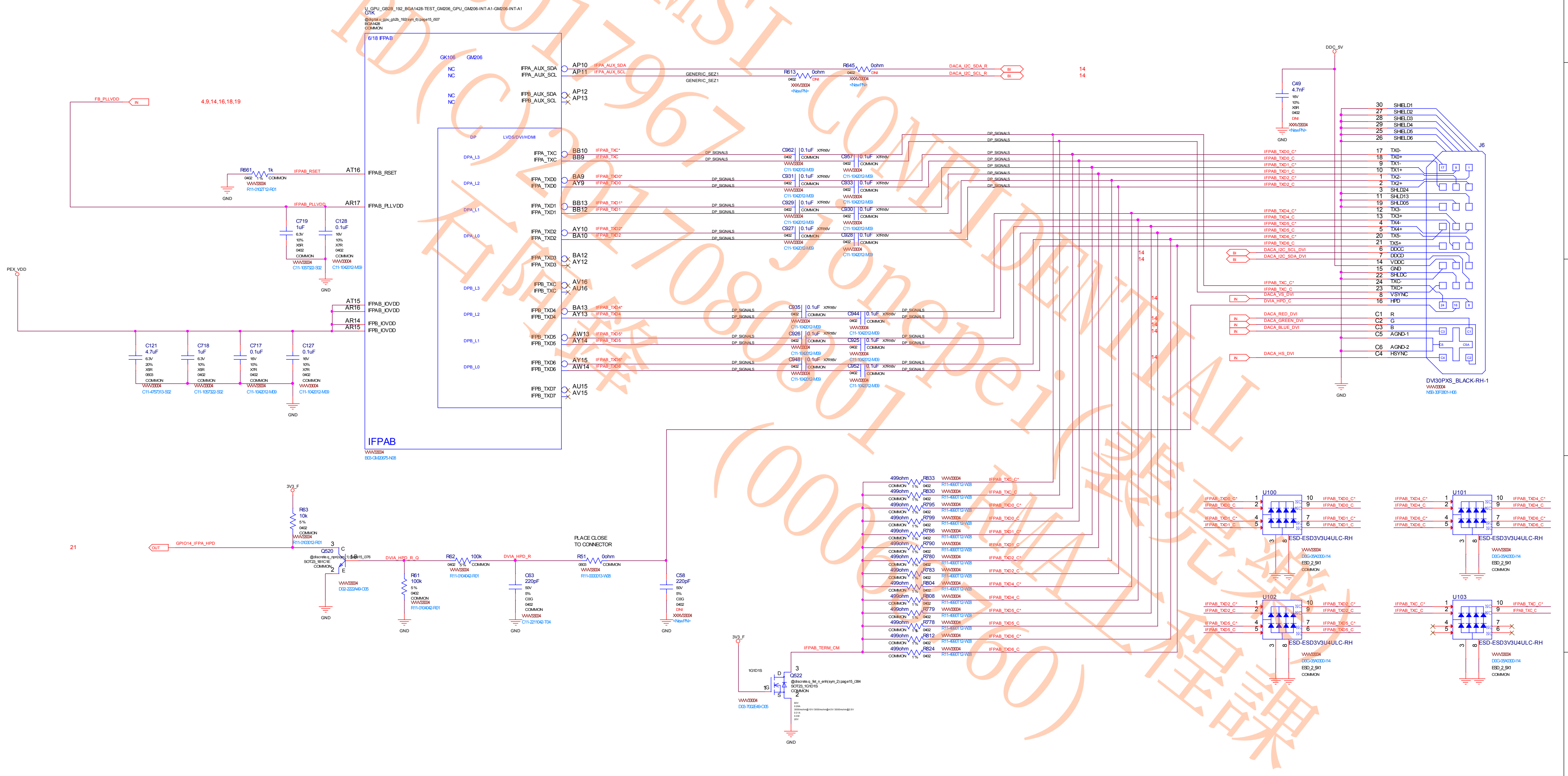
MICRO-STAR INT'L CO.,LTD		
MS-V330		
Size: Custom	Document Description: 13_GPU Decoupling	Rev: 2.1
Date: Tuesday, February 02, 2016	Sheet 13 of 35	

DACA Interface



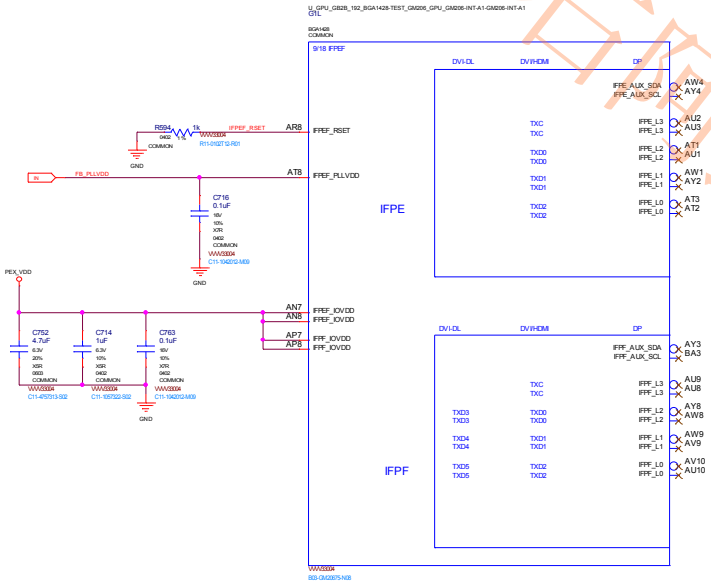
MICRO-STAR INT'L CO.,LTD	
MS-V330	
Size: Custom	Document Description: 14_DACA Interface	Rev: 2.1
Date: Tuesday, February 02, 2016	Sheet 14 of 35

IFPAB DVI-I-DL



MICRO-STAR INT'L CO.,LTD		
MS-V330		
Size: Custom	Document Description: 15_IFPAB DVI-I-DL	Rev: 2.1
Date: Tuesday, February 02, 2016	Sheet 15 of 35	

Page18: IFPEF with IFPE DP



17ci203

MICRO-STAR INT'L CO.,LTD

MS-V330

Size: Custom | Document Description: 16_IFPEF with IFPE DP | Rev: 2.1

Date: Tuesday, February 02, 2016 | Sheet 16 of 35

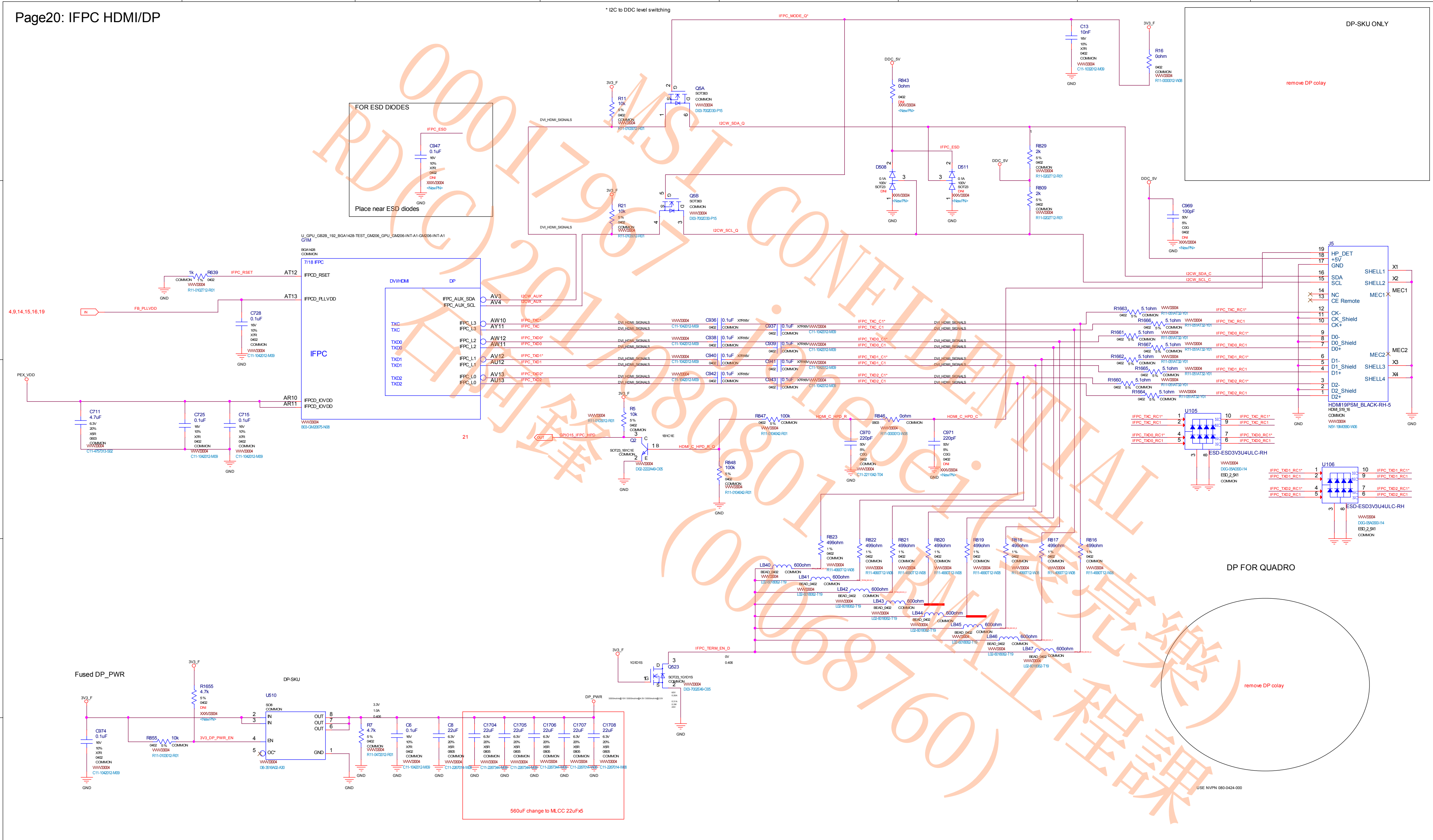
IFPF DP

MICRO-STAR INT'L CO.,LTD
MS-V330

Size	Document Description	Rev
Custom	17_IFPF DP	2.1

Date: Tuesday, February 02, 2016 Sheet 17 of 35

Page20: IFPC HDMI/DP

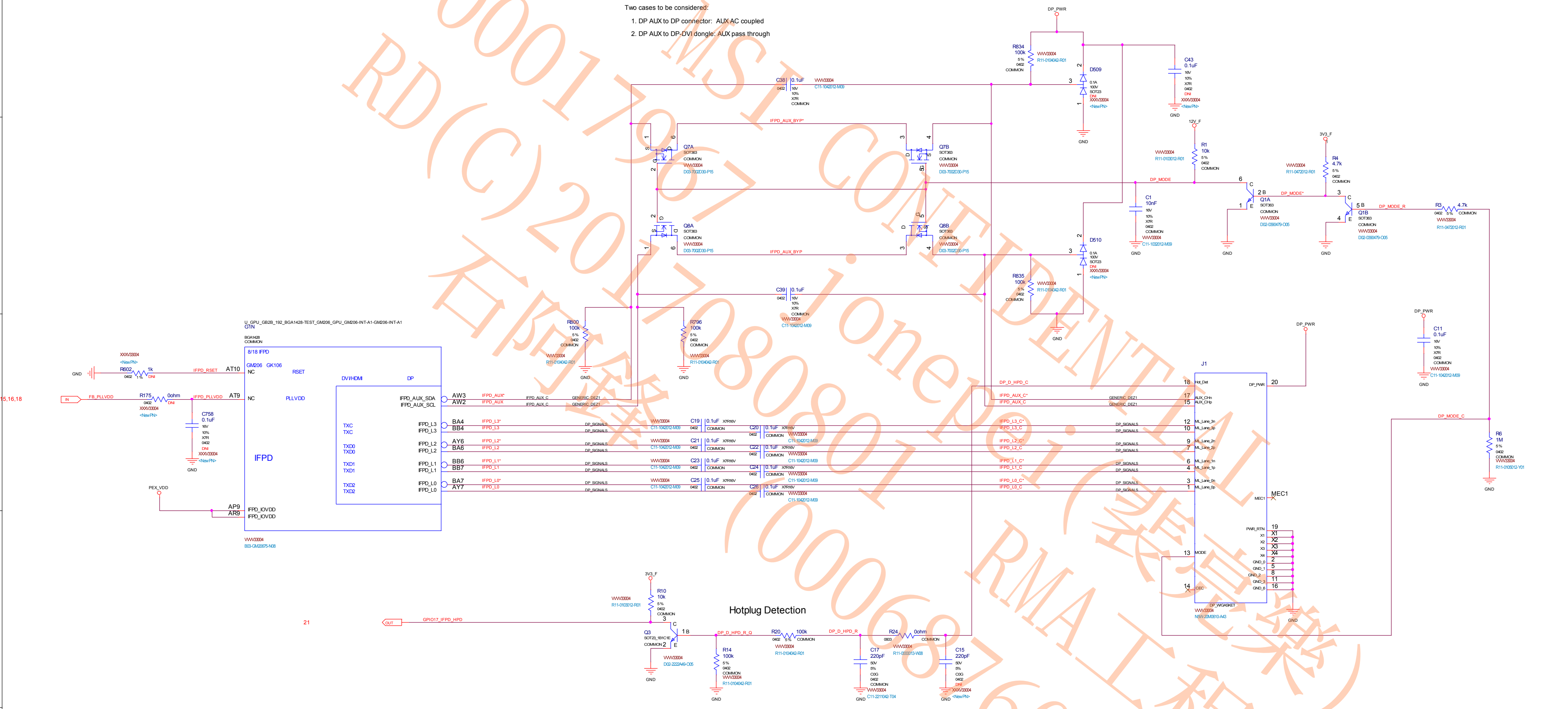


MICRO-STAR INT'L CO.,LTD
MS-V330

Size	Document Description	Rev
Custom	18_IFPC HDMI_DP	2.1

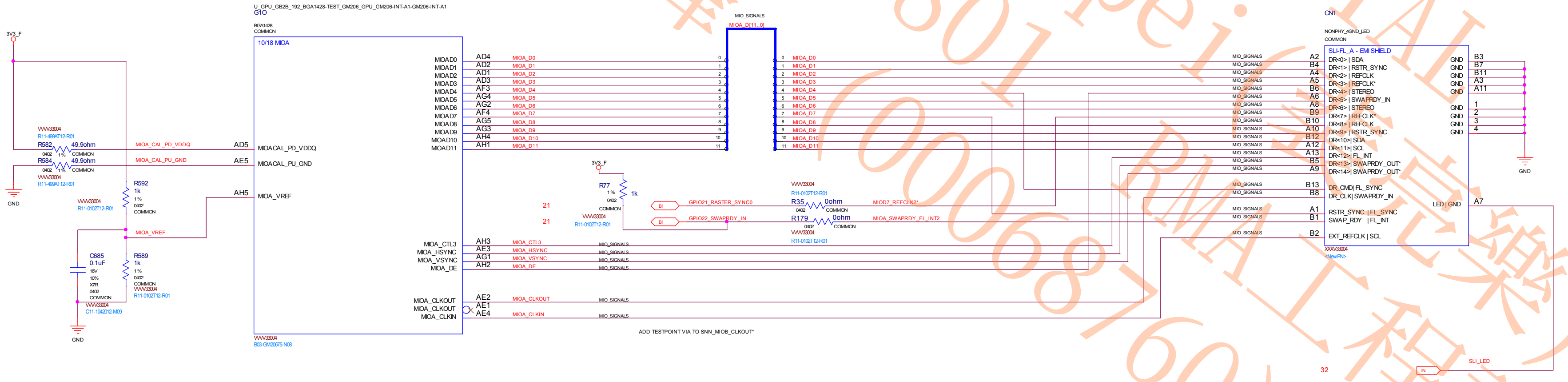
Date: Tuesday, February 02, 2016 | Sheet 18 of 35

IFPD DP



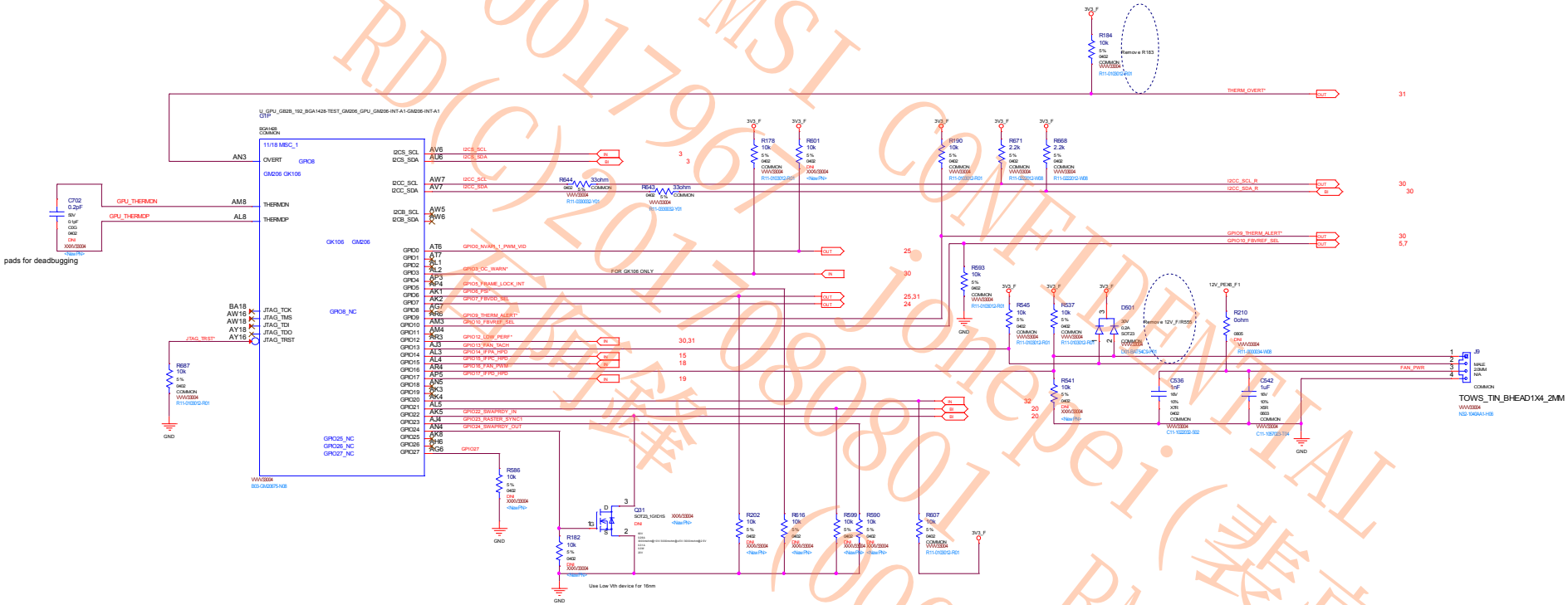
MICRO-STAR INT'L CO.,LTD	
MS-V330	
Size: Custom	Document Description: 19_IFPD DP
Rev: 2.1	
Date: Tuesday, February 02, 2016	Sheet 19 of 35

MIOA/SLI Interface



MICRO-STAR INT'L CO.,LTD		
MS-V330		
Size Custom	Document Description 20_MIOA	Rev 2.1
Date: Tuesday, February 02, 2016	Sheet 20 of 35	

MISC1: Fan, Thermal, JTAG, GPIO

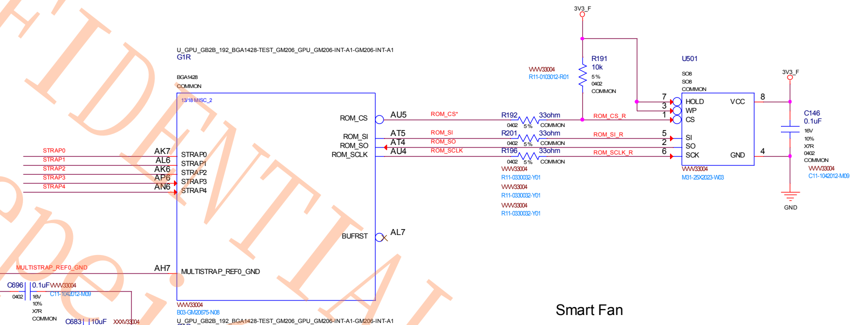


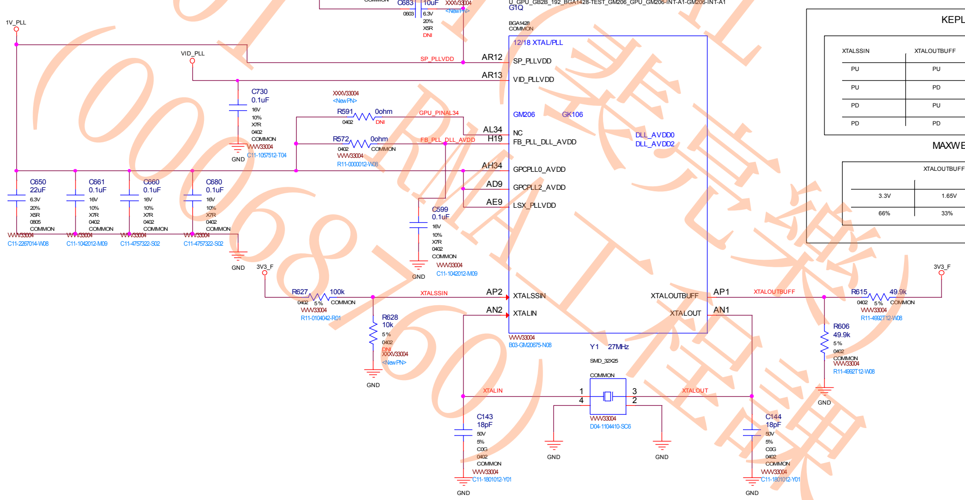
MICRO-STAR INT'L CO.,LTD			
MS-V330			
Size: Custom	Document Description: 21_MISC1_Fan, Thermal, JTAG,		Rev: 2.1
Date: Tuesday, February 02, 2016	Sheet 21 of 35		

MISC2: ROM, XTAL, Straps

	KEPLER	MAXWELL
STRAP0	USER_BIT [3:0]*	
STRAP1	3GIO_PADCFG_LUT_ADR*	
STRAP2	PCI_DEVID [3:0]*	
STRAP3	SOR_EXPOSED [3:0]*	
STRAP4	DP_PLL_VDD_33V*	
	PEX_MAX_SPEED*	
	PEX_SPD_CHANGE_GEN3*	
	*	
ROM_SI	RAMCFG[0]*	RAMCFG[0]*
	RAMCFG[1]*	RAMCFG[1]*
	RAMCFG[2]*	RAMCFG[2]*
	RAMCFG[3]*	RAMCFG[3]*
ROM_SO	VGA_DEVICE*	VGA_DEVICE*
	SMB_ALT_ADDR*	SMB_ALT_ADDR*
	FB[0]_APERTURE_SIZE*	PCIE_CFG*
	FB[1]_APERTURE_SIZE*	DEVID_SEL*
ROM_SCLK	PEX_PLL_EN_TERM100*	SOR0_EXPOSED*
	PCI_DEVID_EXT[5]*	SOR1_EXPOSED*
	SUB_VENDOR*	SOR2_EXPOSED*
	PCI_DEVID_EXT[4]*	SOR3_EXPOSED*

	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111





Smart Fan

KEPLER

XTALSSIN	XTALOUTBUFF	Inverted PWM %
PU	PU	66 (33% HIGH)
PU	PD	50 (50% HIGH)
PD	PU	33 (66% HIGH)
PD	PD	0 (100% HIGH)

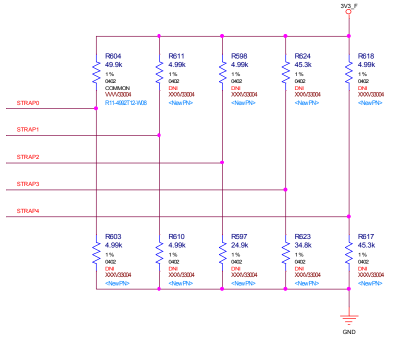
MAXWELL

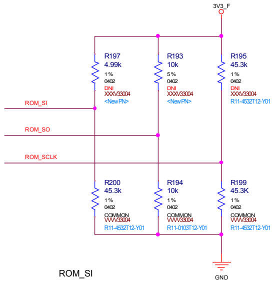
XTALOUTBUFF		
3.3V	1.65V	0V
66%	33%	DISABLED

MULTI_STRAP_REF0_GND	
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	40.2k 1% TO GND

MAXWELL

STRAP0		
3.3V	1.65V	0V
GC6+ ISLAND ENABLED	GC6+ DEBUG MODE	GC6+ ISLAND DISABLED





ROM_SI

SAMSUNG	HYNIX	ELPIDA
45.3k PD	34.8k PD	30.1k PD

17ci203

MICRO-STAR INT'L CO.,LTD

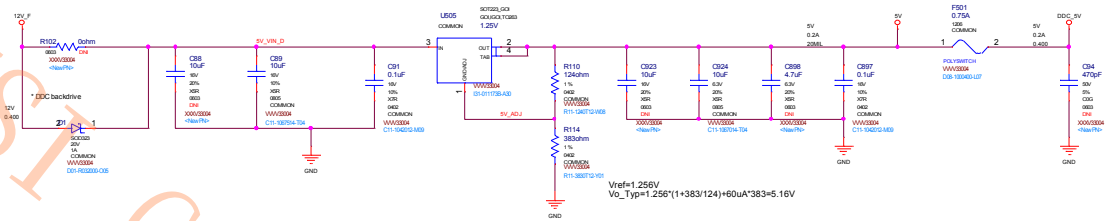
MS-V330

Size	Document Description	Rev
Custom	22_MISC2_ ROM, XTAL, Straps	2.1

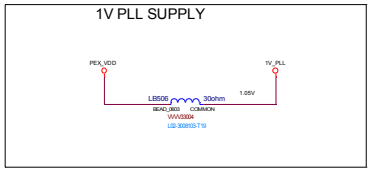
Date: Tuesday, February 02, 2016 Sheet 22 of 35

PS: 5V, PEX_VDD

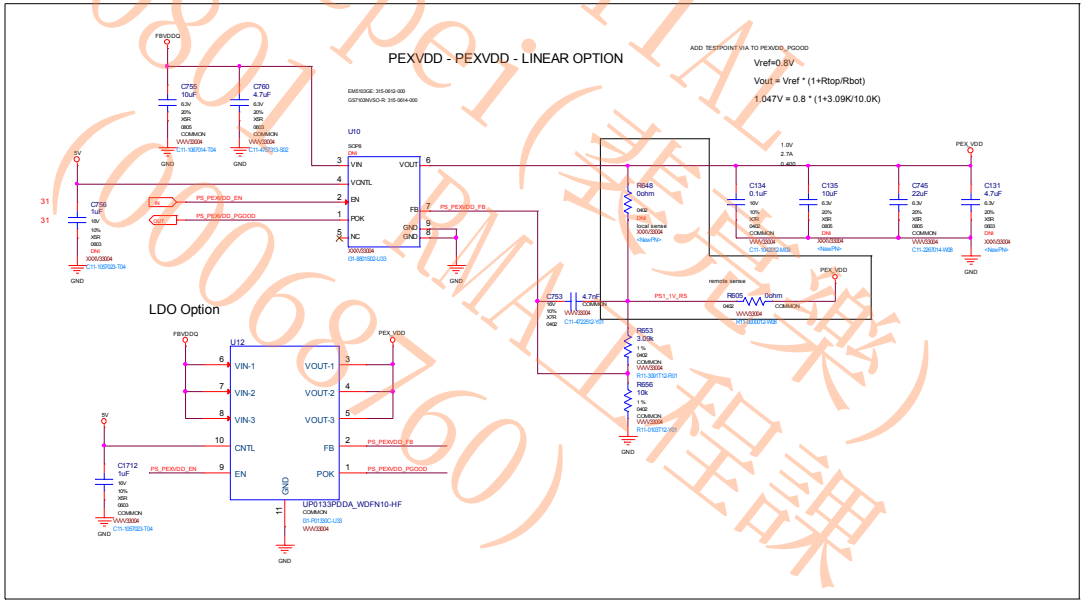
5V / DDC SUPPLY



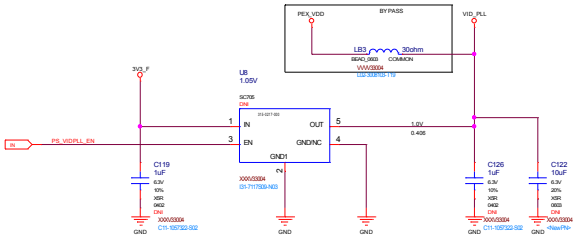
1V PLL SUPPLY



PEXVDD - PEXVDD - LINEAR OPTION



VID PLL SUPPLY



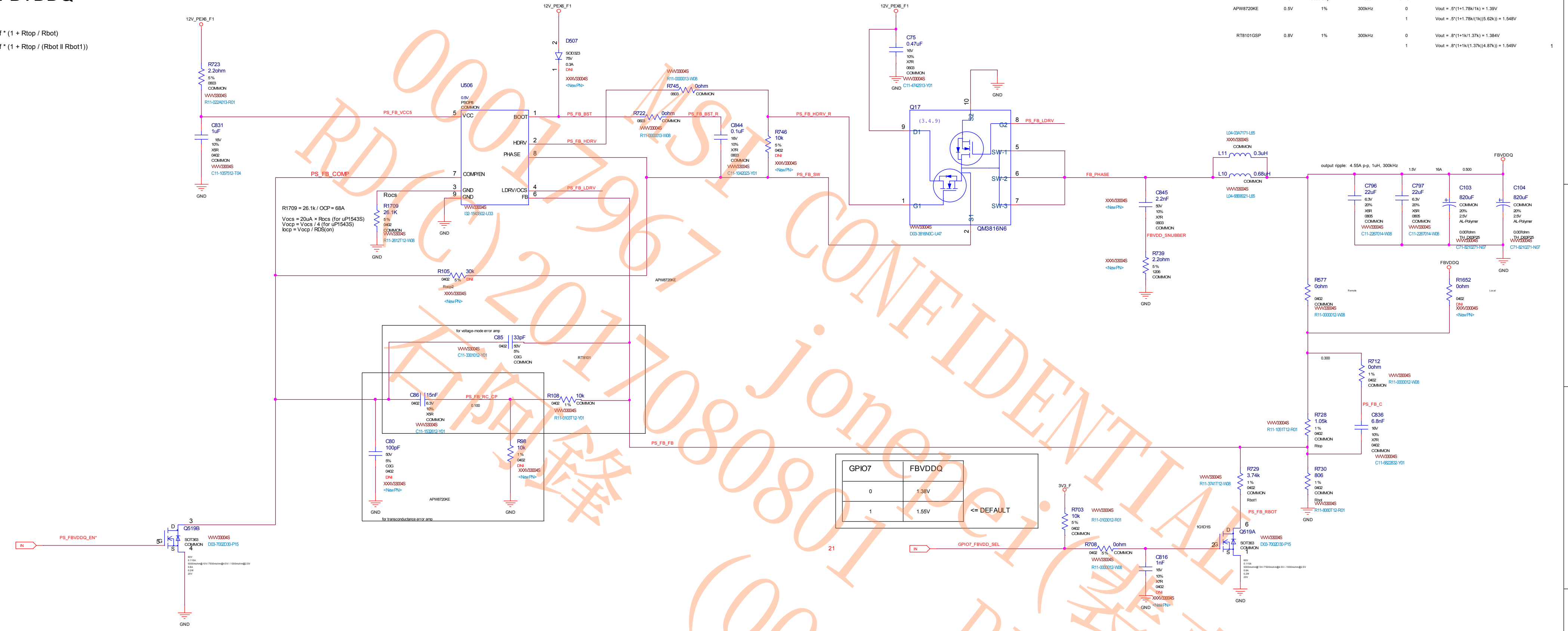
MICRO-STAR INT'L CO.,LTD	
MS-V330	
Size: Custom	Document Description: 23_PS_ 5V, PEX_VDD, VID_PLL
Rev: 2.1	
Date: Tuesday, February 02, 2016	Sheet 23 of 35

PS: FBVDDQ

Vout = Vref * (1 + Rtop / Rbot)

Vout = Vref * (1 + Rtop / (Rbot ll Rbot1))

	Vref	Vref accuracy	Fosc	GPIO7	
APW8720KE	0.5V	1%	300kHz	0	Vout = .5*(1+1.78k/1k) = 1.39V
				1	Vout = .5*(1+1.78k/(1k||5.62k)) = 1.548V
RT8101GSP	0.8V	1%	300kHz	0	Vout = .8*(1+1k/1.37k) = 1.384V
				1	Vout = .8*(1+1k/(1.37k||4.87k)) = 1.549V



GPIO7	FBVDDQ	
0	1.38V	
1	1.55V	<= DEFAULT

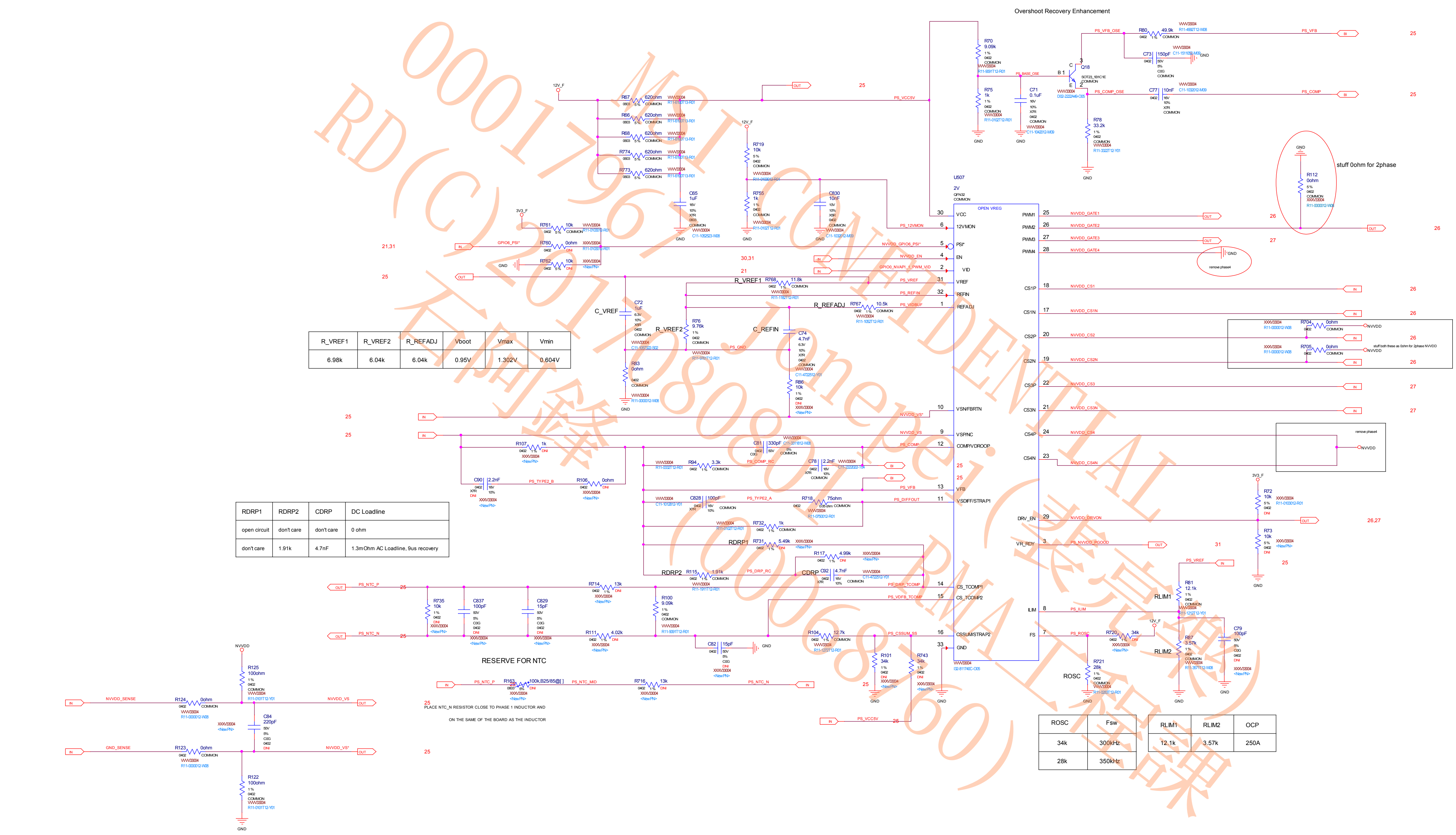
MICRO-STAR INT'L CO.,LTD

MS-V330

Size	Document Description	Rev
Custom	24_PS_FBVDD_Q	2.1

Date: Tuesday, February 02, 2016 Sheet 24 of 35

PS: NVVDD Controller



R_VREF1	R_VREF2	R_REFADJ	Vboot	Vmax	Vmin
6.98k	6.04k	6.04k	0.95V	1.302V	0.604V

RDRP1	RDRP2	CDRP	DC Loadline
open circuit	don't care	don't care	0 ohm
don't care	1.91k	4.7nF	1.3mOhm AC Loadline, 9us recovery

ROSC	Fsw
34k	300kHz
28k	350kHz

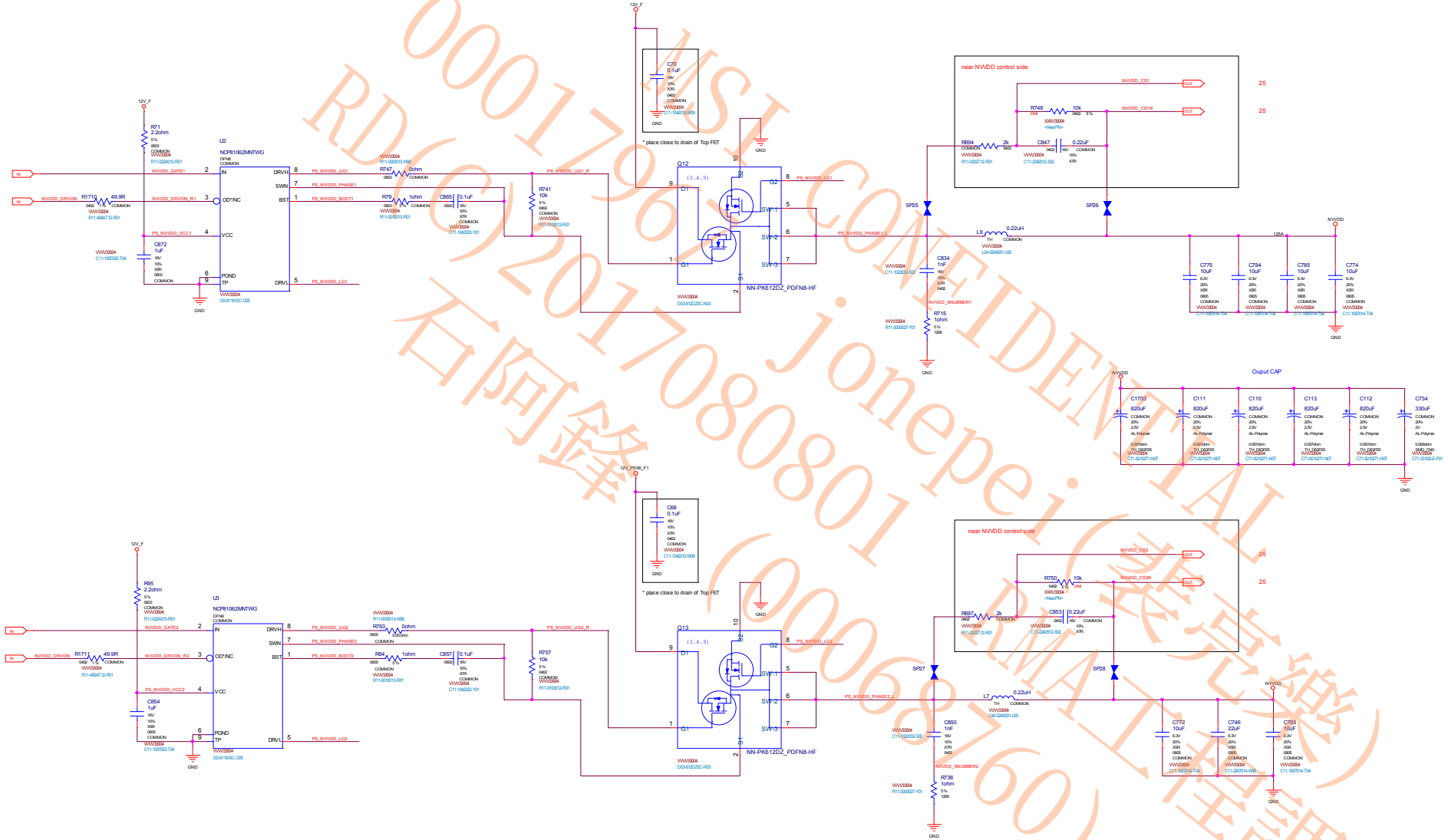
RLIM1	RLIM2	OCP
12.1k	3.57k	250A

MICRO-STAR INT'L CO.,LTD

MS-V330

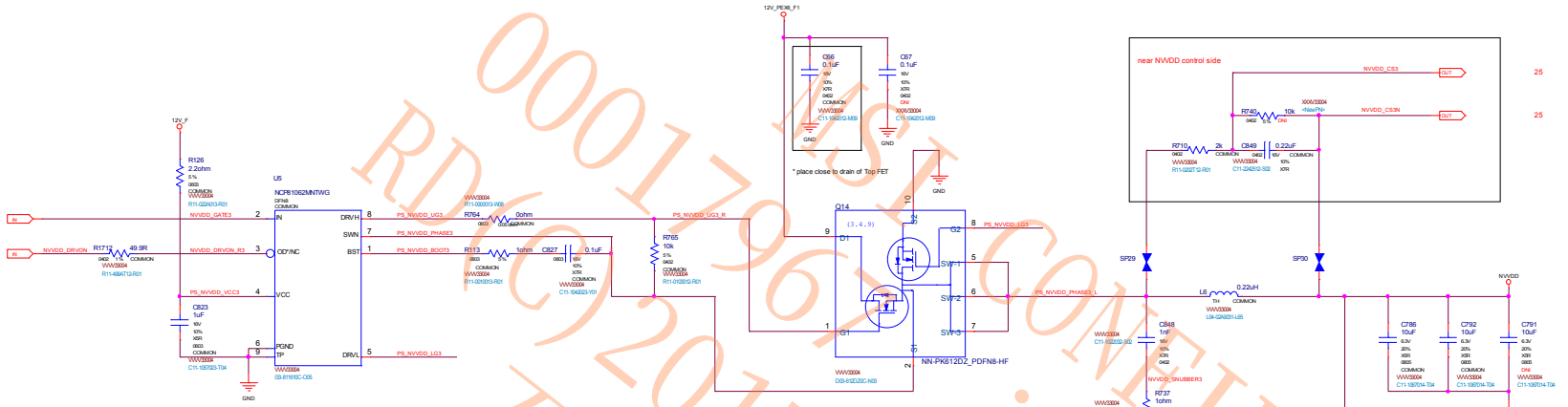
Size	Document Description	Rev
Custom	25_PS_NVVDD Controller OVR4	2.1

PS: NVVDD Phase 1,2



MICRO-STAR INT'L CO.,LTD		
MS-V330		
Size: Custom	Document Description: 26_PS_ NVVDD Phase 1,2	Rev: 2.1
Date: Tuesday, February 02, 2016	Sheet 26 of 35	

PS: NVVDD Phase 3,4



remove phase4

MICRO-STAR INT'L CO.,LTD	
MS-V330	
Size: Custom	Document Description: 27_PS_ NVVDD Phase 3,4
Rev: 2.1	
Date: Tuesday, February 02, 2016	Sheet 27 of 35

[RESERVED]

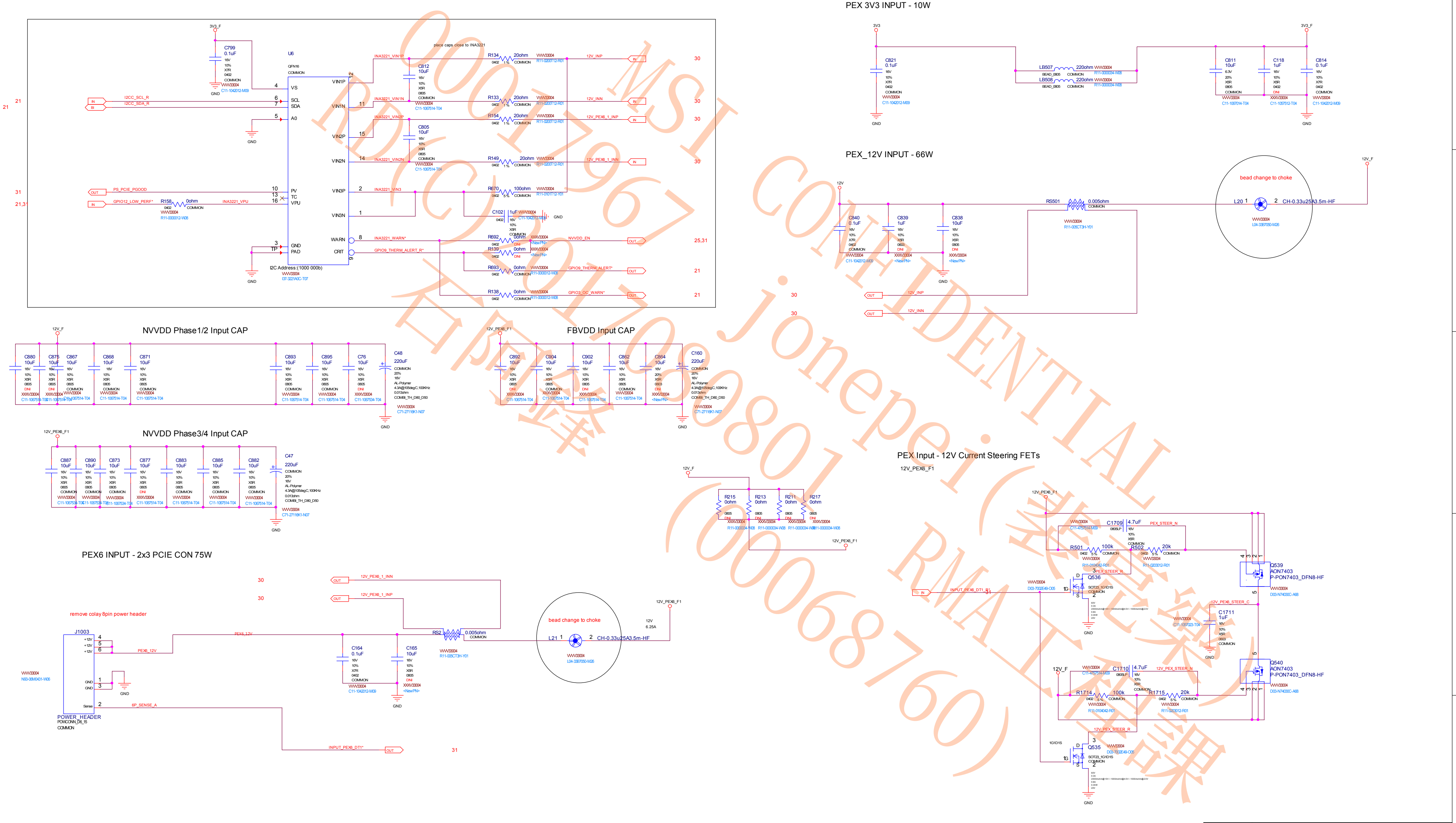
17ci203

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V330	
Size: Custom	Document Description: 28_[RESERVED]	Rev: 2.1
Date: Tuesday, February 02, 2016	Sheet 28 of 35	

PS: NVVDD OVR2+1 POWER

MSI	MICRO-STAR INT'L CO.,LTD
	MS-V330
Size: Custom	Document Description: 29_PS_ NVVDD OVR2+1 option
Rev: 2.1	
Date: Tuesday, February 02, 2016	Sheet 29 of 35

PS: Inputs, Filtering, Monitoring and 12V Current Steering



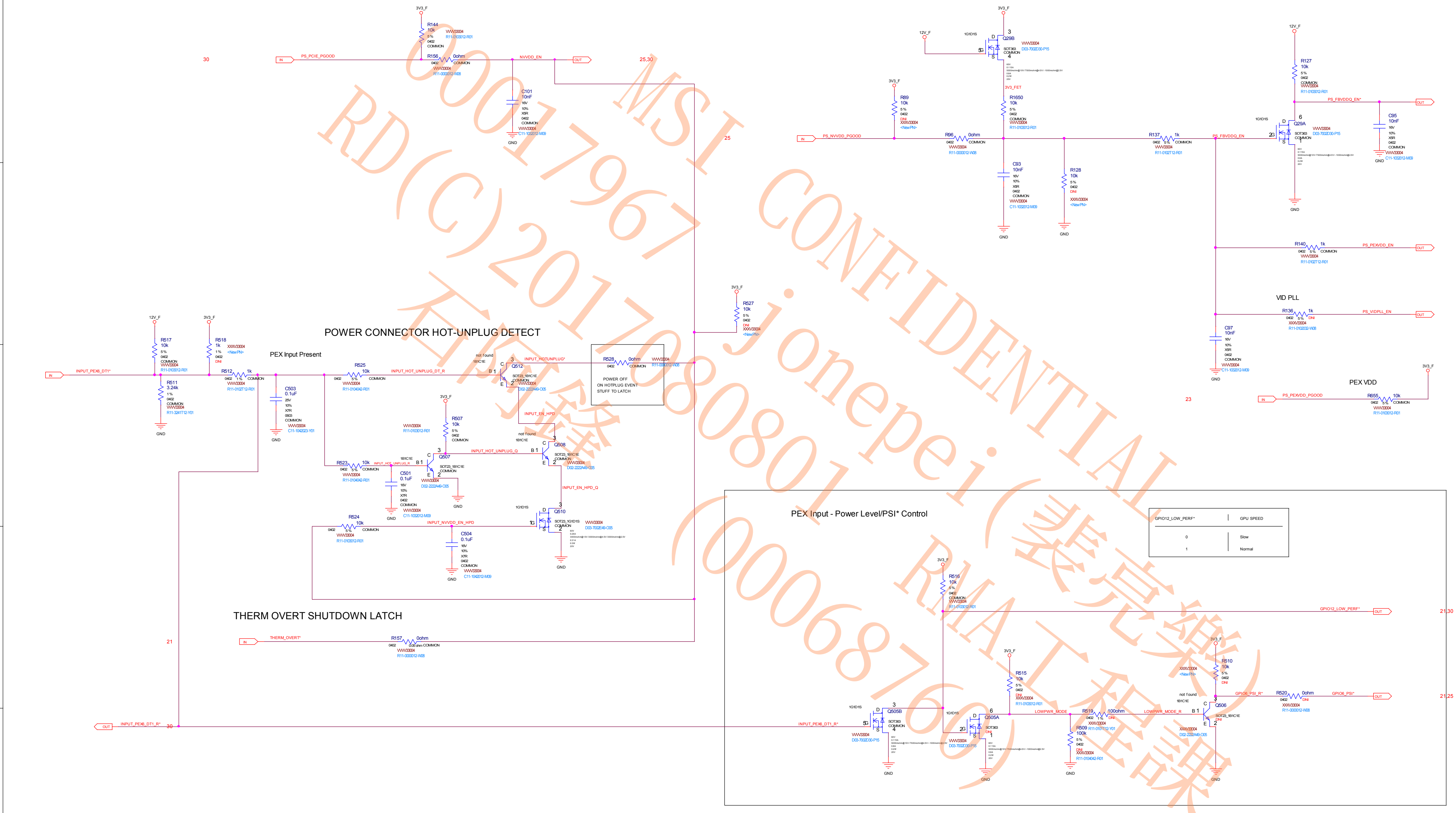
MICRO-STAR INT'L CO.,LTD

MS-V330

Size	Document Description	Rev
Custom	30_PS_ Inputs, Filtering, Monitoring and 12V Current Steering	2.1

Date: Tuesday, February 02, 2016 Sheet 30 of 35

PS: Sequence and Shutdown



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

MICRO-STAR INT'L CO.,LTD

MS-V330

Size	Document Description	Rev
Custom	31_PS_ Sequence and Shutdown	2.1

Date: Tuesday, February 02, 2016 | Sheet 31 of 35

LEDs

IFP_IOVDD (backdrive prevention)

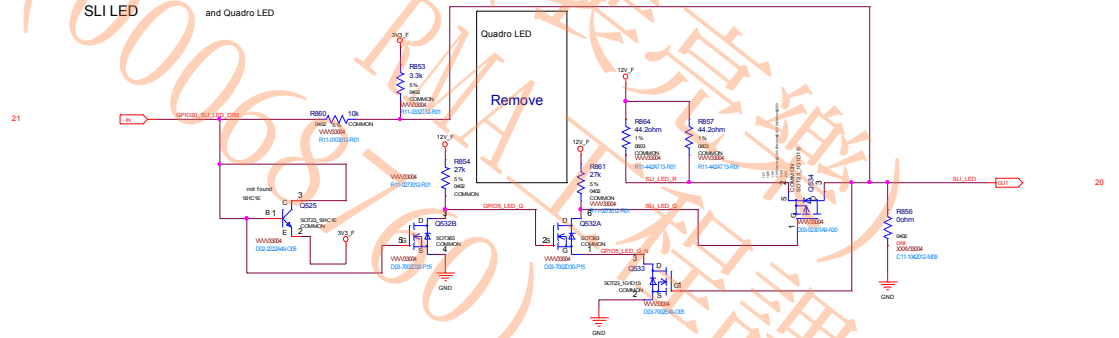
Kepler Only

Remove

SLI LED and Quadro LED

Quadro LED

Remove



MICRO-STAR INT'L CO.,LTD		
MS-V330		
Size: Custom	Document Description: 32_LEDs	Rev: 2.1
Date: Tuesday, February 02, 2016	Sheet 32 of 35	

PS: IOVDD, NV3V3, NV12V

OVR0 1.8V REGULATOR. STUFF FOR 16nm

Remove

Special Note:
1. Place [C_OUT] close to [L_OUT]
2. Use local FB sense (refer to design guide for details)
3. Place PLL/IO filter ferrite bead to the same position as FB local sense point

BYPASS. STUFF FOR 28nm

Remove

Gated rails required for 16nm

Remove

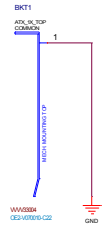
MICRO-STAR INT'L CO.,LTD
MS-V330

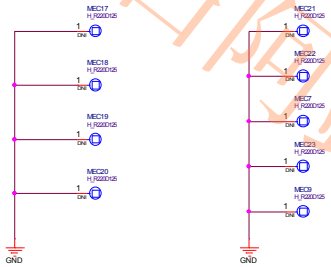
Size	Document Description	Rev
Custom	33_PS_ IOVDD Regulator	2.1

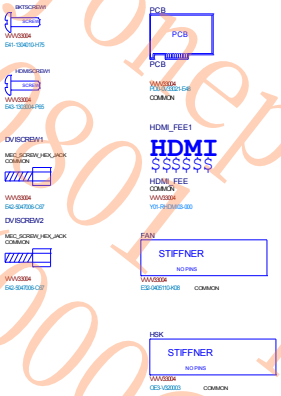
Date: Tuesday, February 02, 2016 Sheet 33 of 35

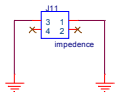
Mechanical: Bracket/Thermal Solution

Brackets:

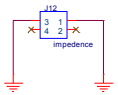




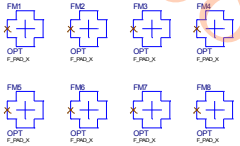




L1_D_0.12/0.101 80ohm



L4_D_0.1/0.12 90ohm



L1_S_0.126 47ohm

L4_S_0.102 52ohm

MICRO-STAR INT'L CO.,LTD		
MS-V330		
Size: Custom	Document Description: 34_MECH_Bracket_Thermal	Rev: 2.1
Date: Tuesday, February 02, 2016	Sheet 34 of 35	

Note:

2015/11/23	
page: 20	Remove_SLI net
page:21	ADD GPIO11_LOGO_LED NET / Remove_SLI net
page:24	預留 FBVDDQ convertor : NB685
page:25	移除第四相線路,預留關閉二相線路
page:27	移除第四相線路
page:32	新增Logo LED線路/移除SLI LED線路

MICRO-STAR INT'L CO.,LTD
MS-V330
Size: Custom | Document Description: Remark | Rev: 2.1
Date: Tuesday, February 02, 2016 | Sheet 35 of 35