

PG410 A01

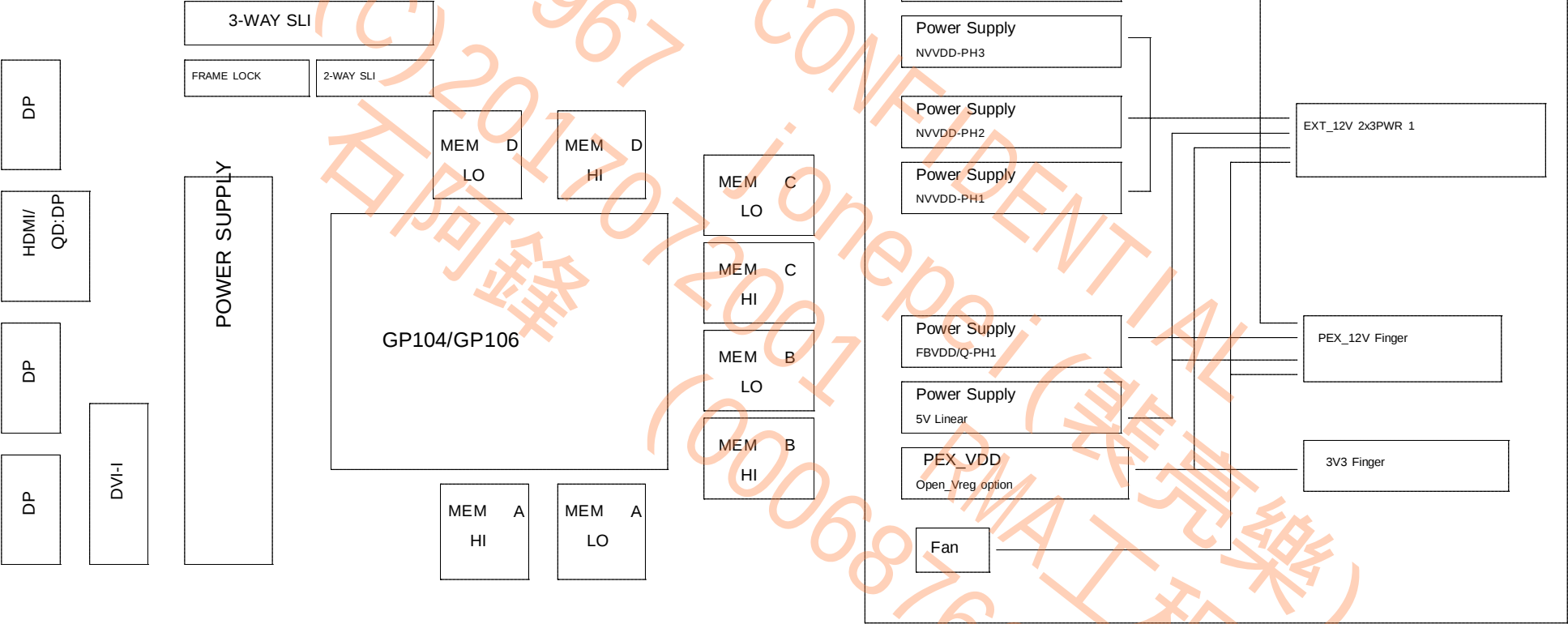
GP106 8GB/4GB GDDR5, 256b, 256Mx32/128MX32
Tall DVI-D + DP + DP + HDMI + HDMI

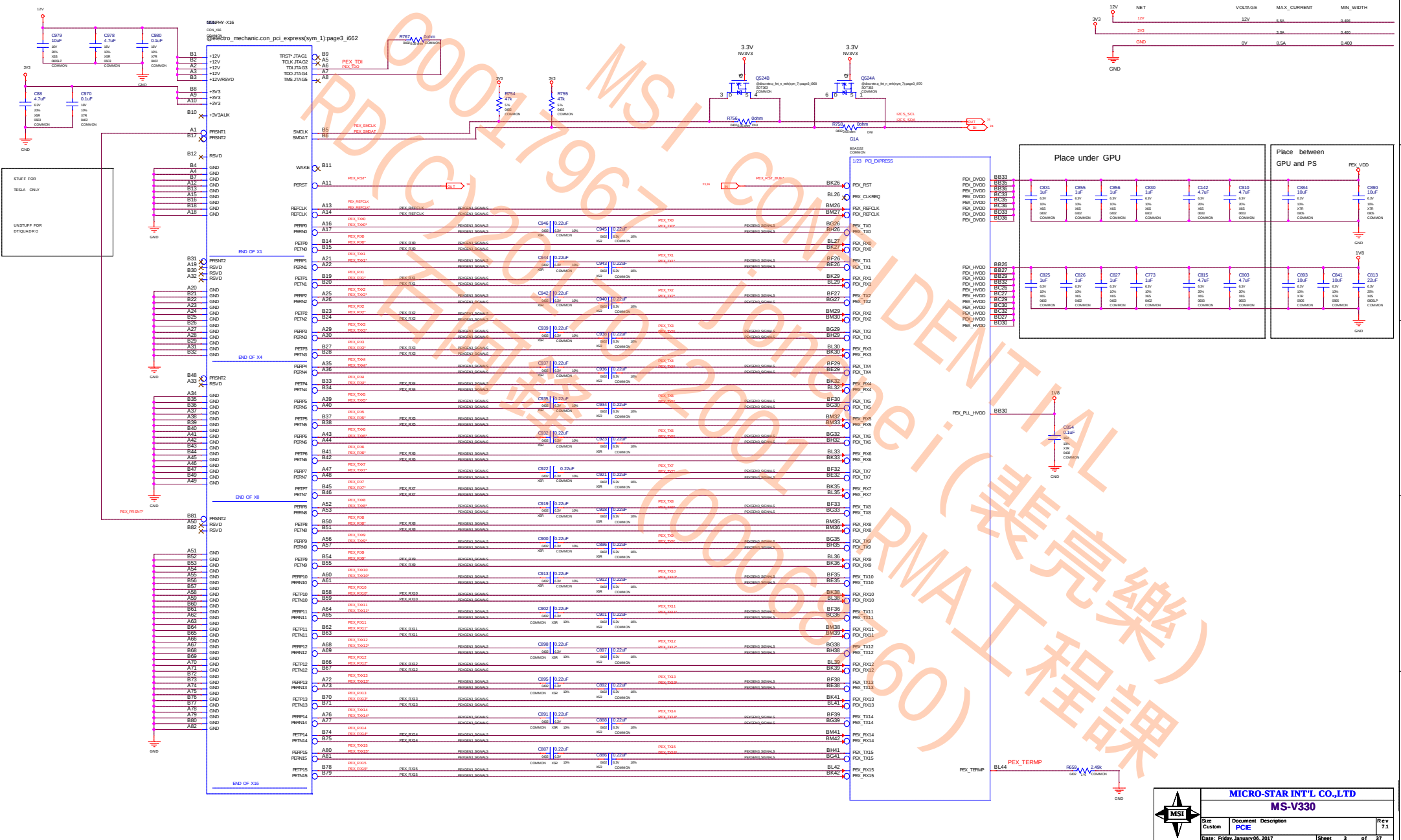
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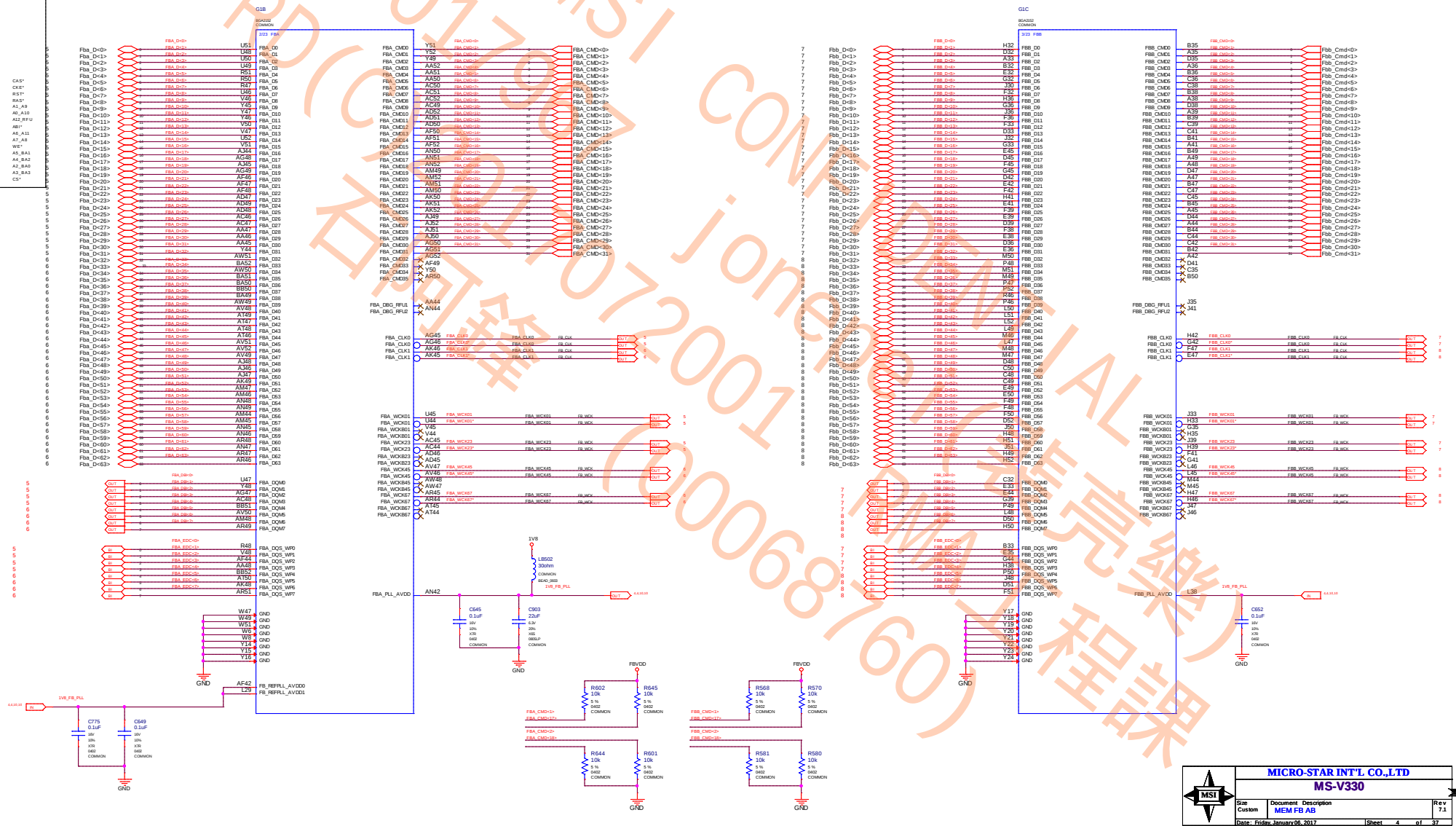
V330-T 0 頁 PG41 00
1 - 規格書
2 - 規格書
3 - 規格書
4 - 規格書

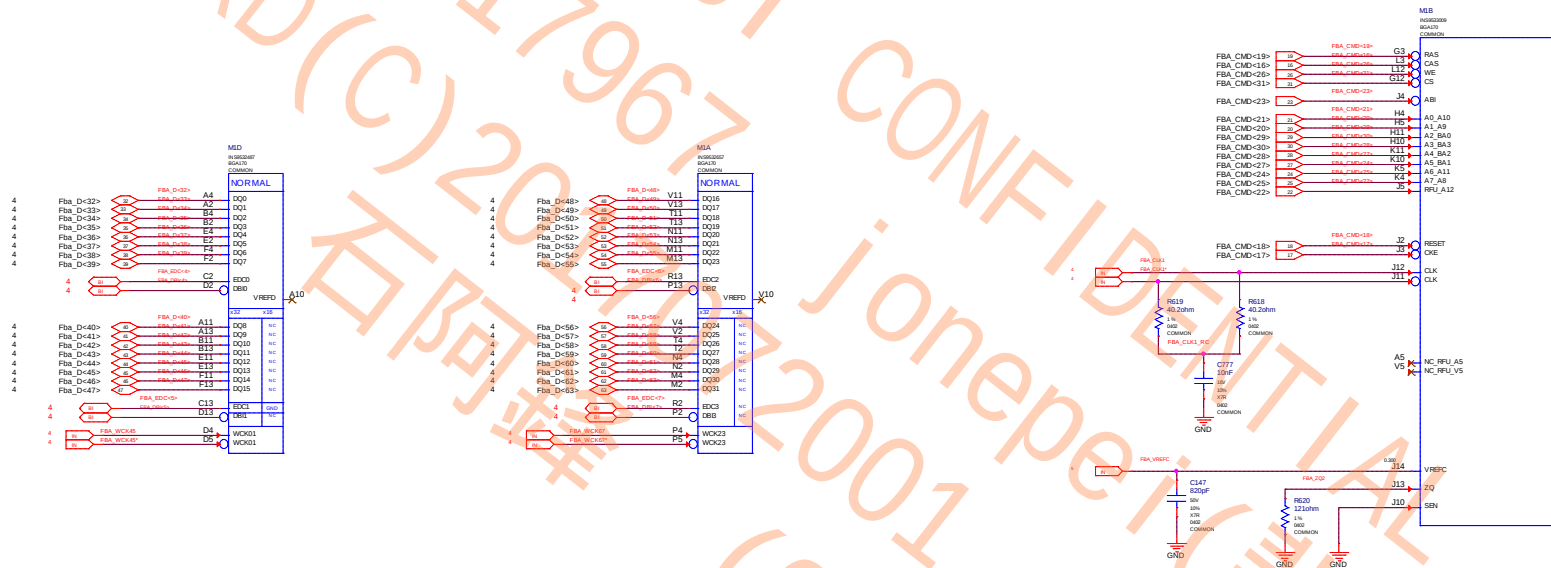
MICRO-STAR INT'L CO.,LTD			
MS-V330			
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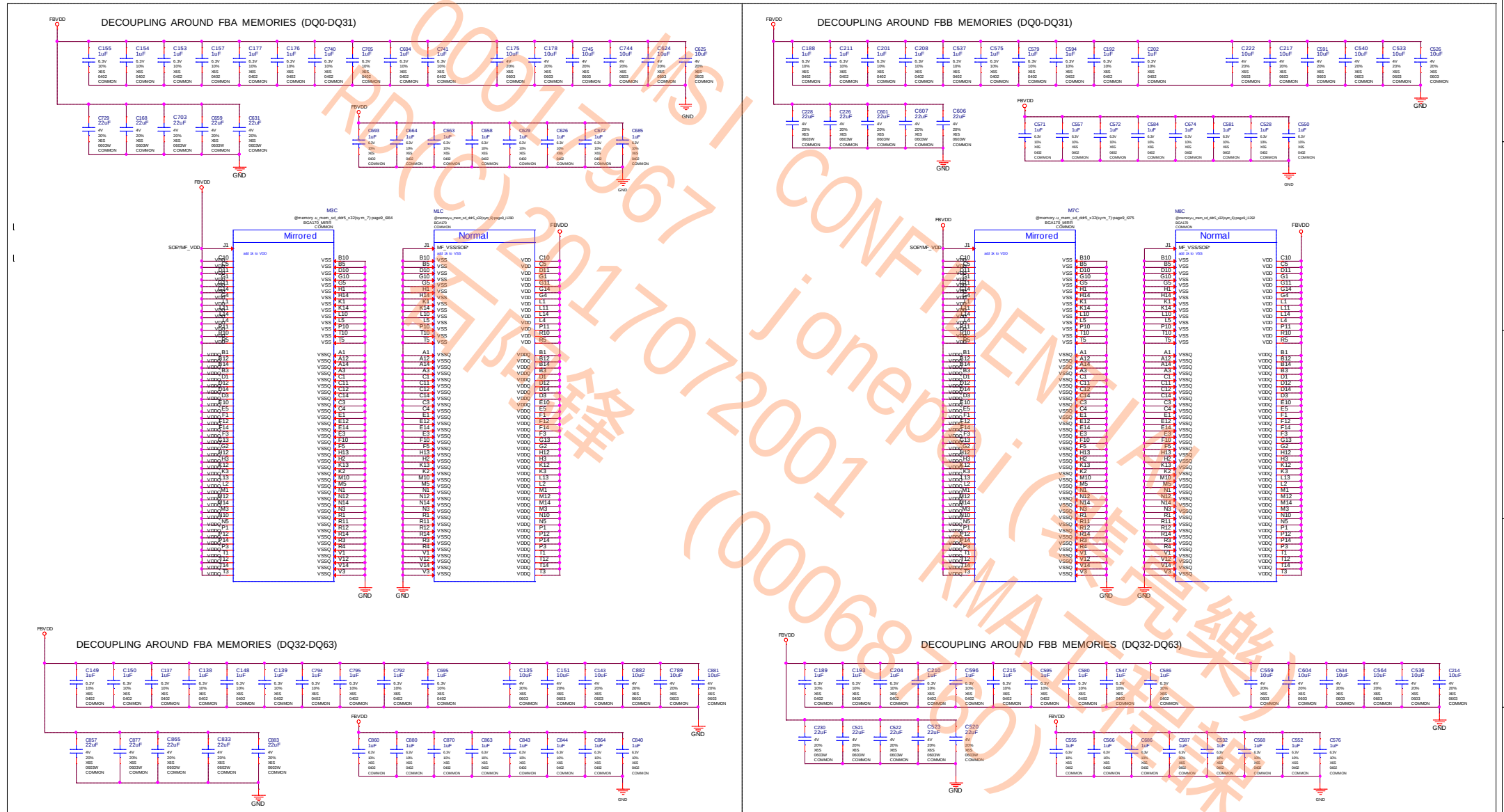




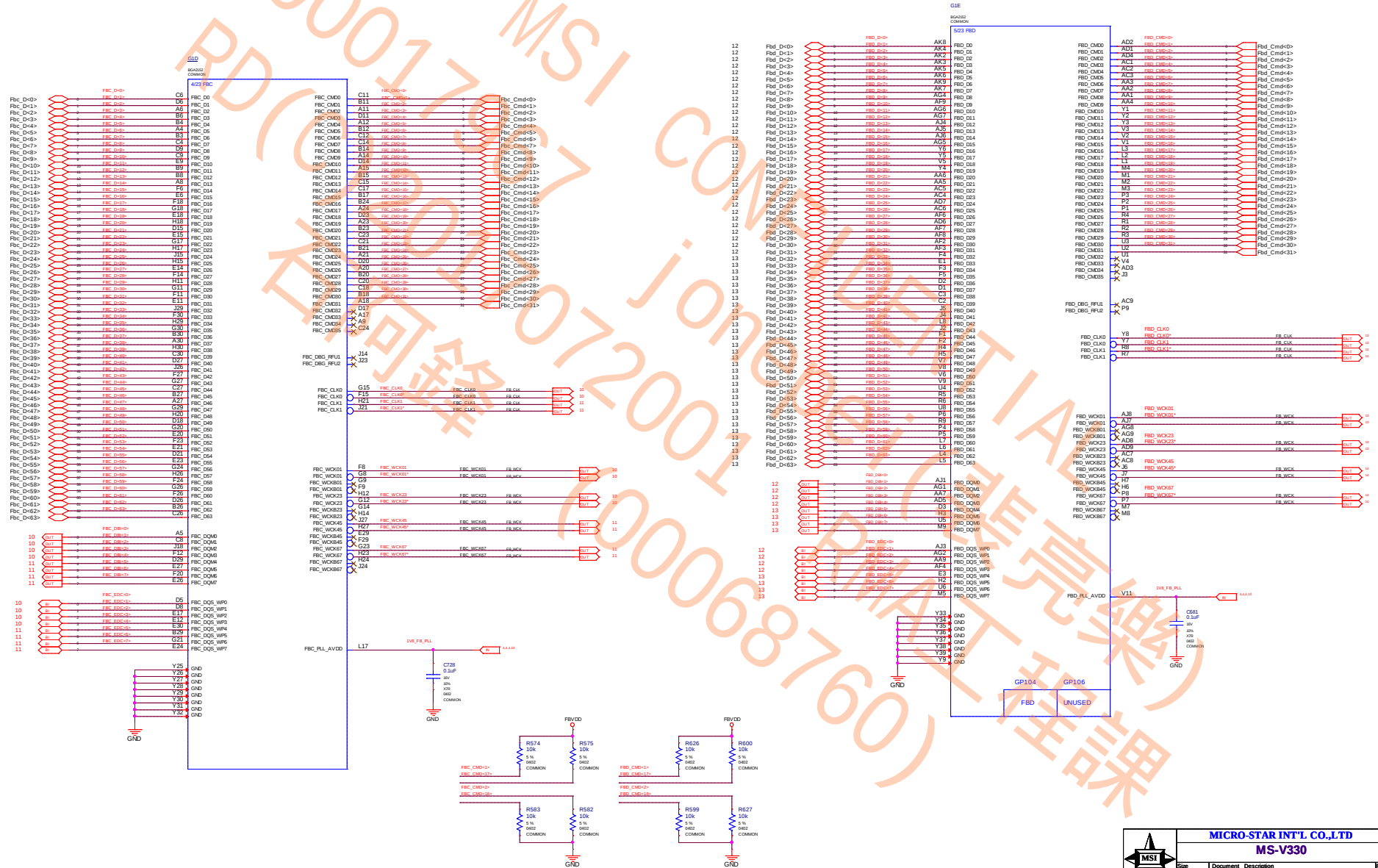
GDSCR CMD Mapping		
CMD	A-21	A-42
CM00	CAS*	
CM01	CAS*	
CM02	RST*	
CM03	BS†	
CM04	A3, A8	
CM05	A2, A10	
CM06	A12, RFU	
CM07	AB†	
CM08	A8, A11	
CM09	A7, A8	
CM10	WE*	
CM11	A5, BA1	
CM12	A4, BA2	
CM13	A2, BA0	
CM14	A3, BA3	
CM15	CS*	
CM16		CAS*
CM17		CSE*
CM18		BS†
CM19		BA5*
CM20		A1, A9
CM21		AB, A10
CM22		A12, RFU
CM23		AB†
CM24		A8, A11
CM25		A7, A8
CM26		WE*
CM27		A5, BA1
CM28		AB, BA2
CM29		A2, BA0
CM30		A3, BA3
CM31		CS*

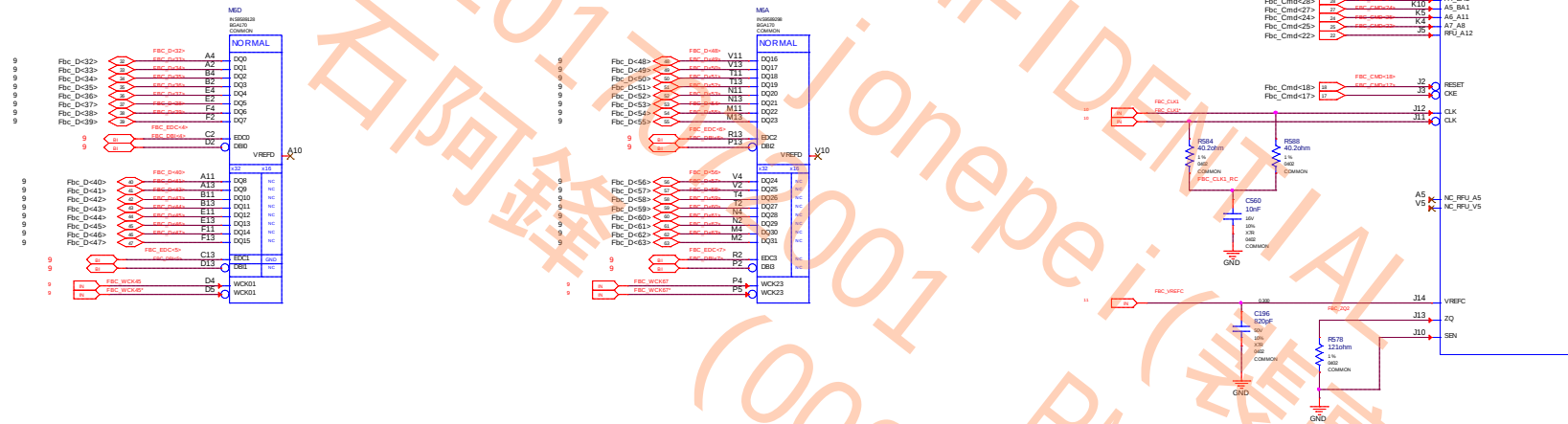


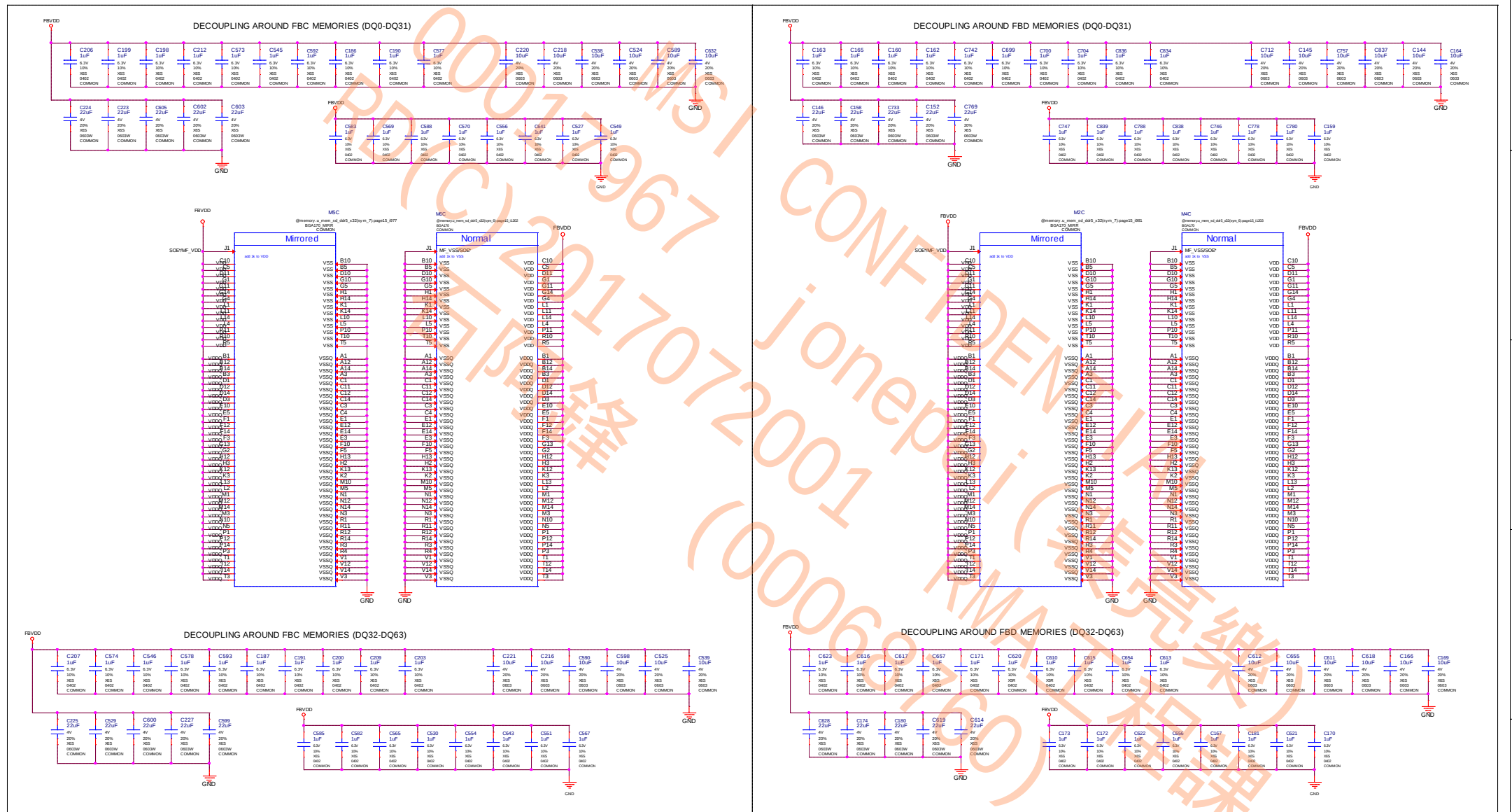




QDDR5 CMD Mapping		
Cmd	QDDR5	32-Bit
CMDS0	CAS*	
CMDS1	CAS*	
CMDS2	RST*	
CMDS3	RAS*	
CMDS4	A1, A8	
CMDS5	A0, A10	
CMDS6	A2, BFU	
CMDS7	ABT*	
CMDS8	A0, A11	
CMDS9	A7, A8	
CMDS10	WE*	
CMDS11	A0, BA1	
CMDS12	A1, BA2	
CMDS13	A2, BA0	
CMDS14	A3, BA3	
CMDS15	C*	
CMDS16	CAS*	
CMDS17	RST*	
CMDS18	A0, BA1	
CMDS19	RAS*	
CMDS20	A0, A10	
CMDS21	A2, BFU	
CMDS22	ABT*	
CMDS23	A0, A11	
CMDS24	A7, A8	
CMDS25	WE*	
CMDS26	A0, BA1	
CMDS27	A1, BA2	
CMDS28	A2, BA0	
CMDS29	A3, BA3	
CMDS30	C*	



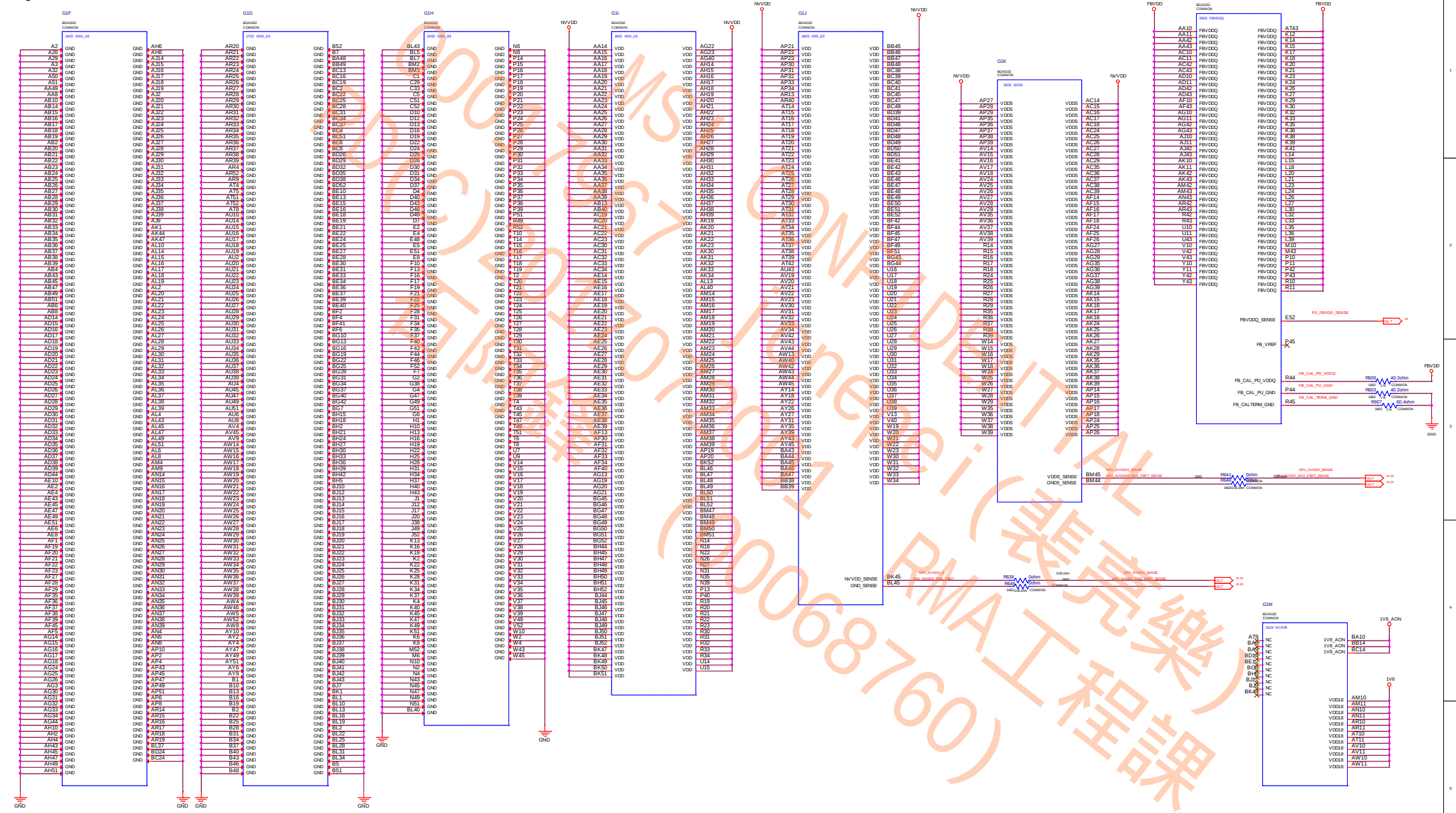




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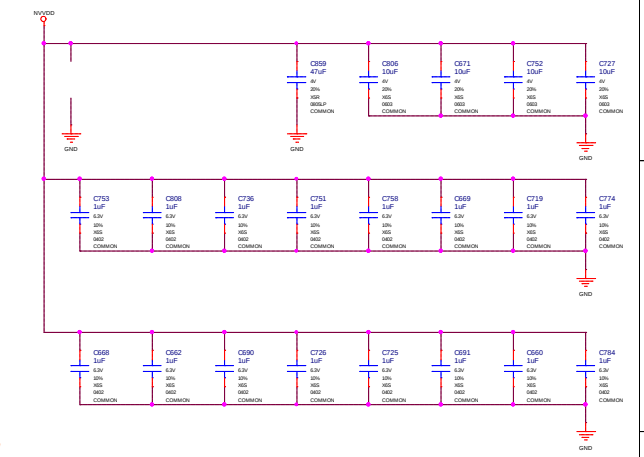
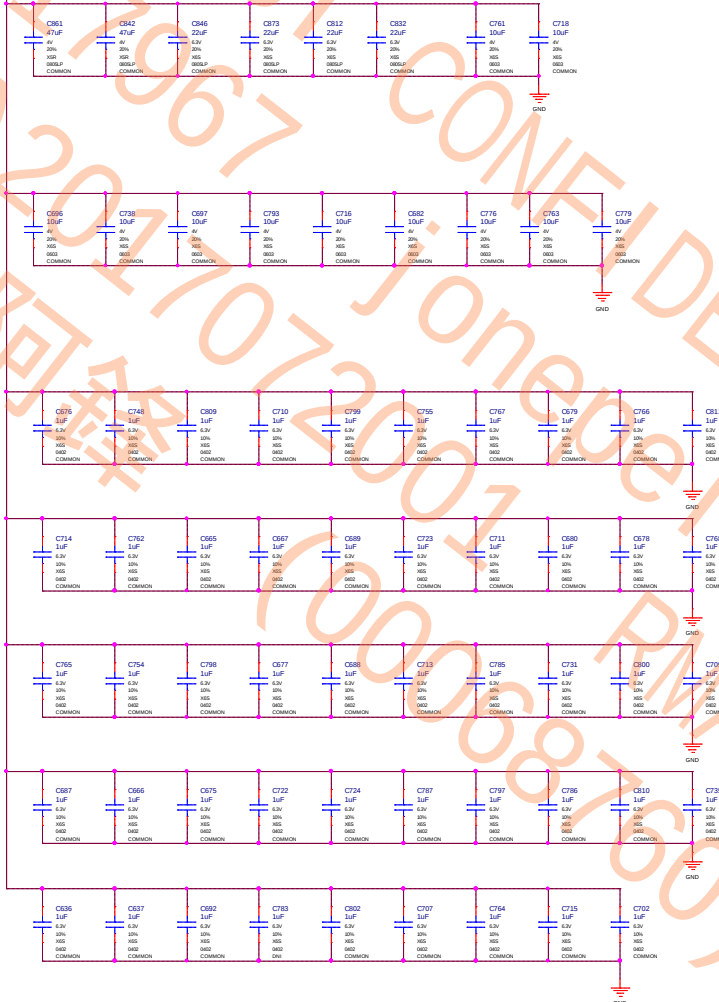
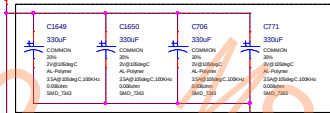
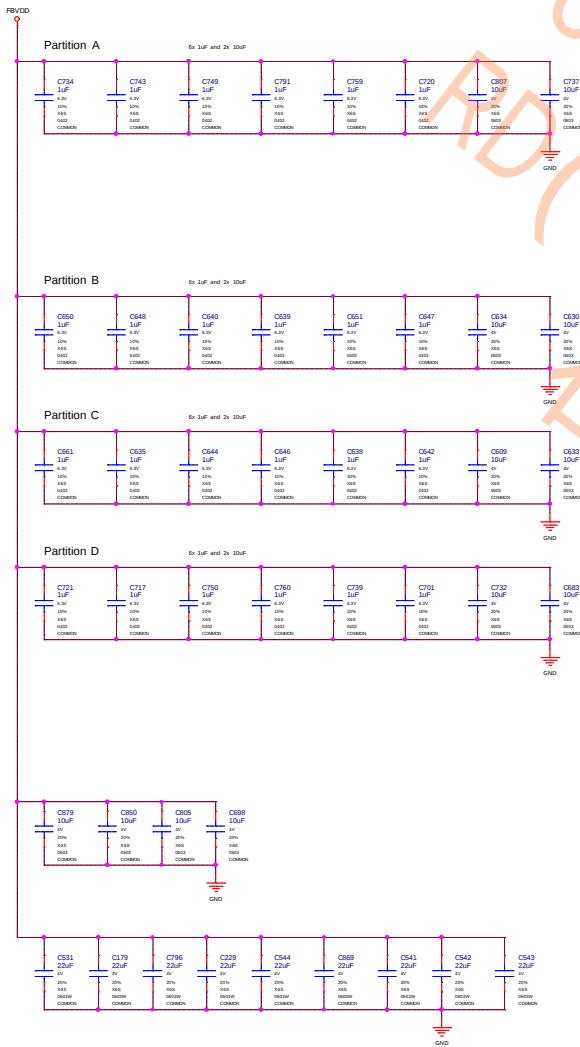
Rev	Docum	Description	Rev
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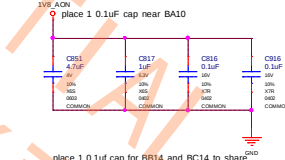
FBVDD

NVDD

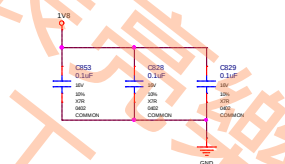
NVDD

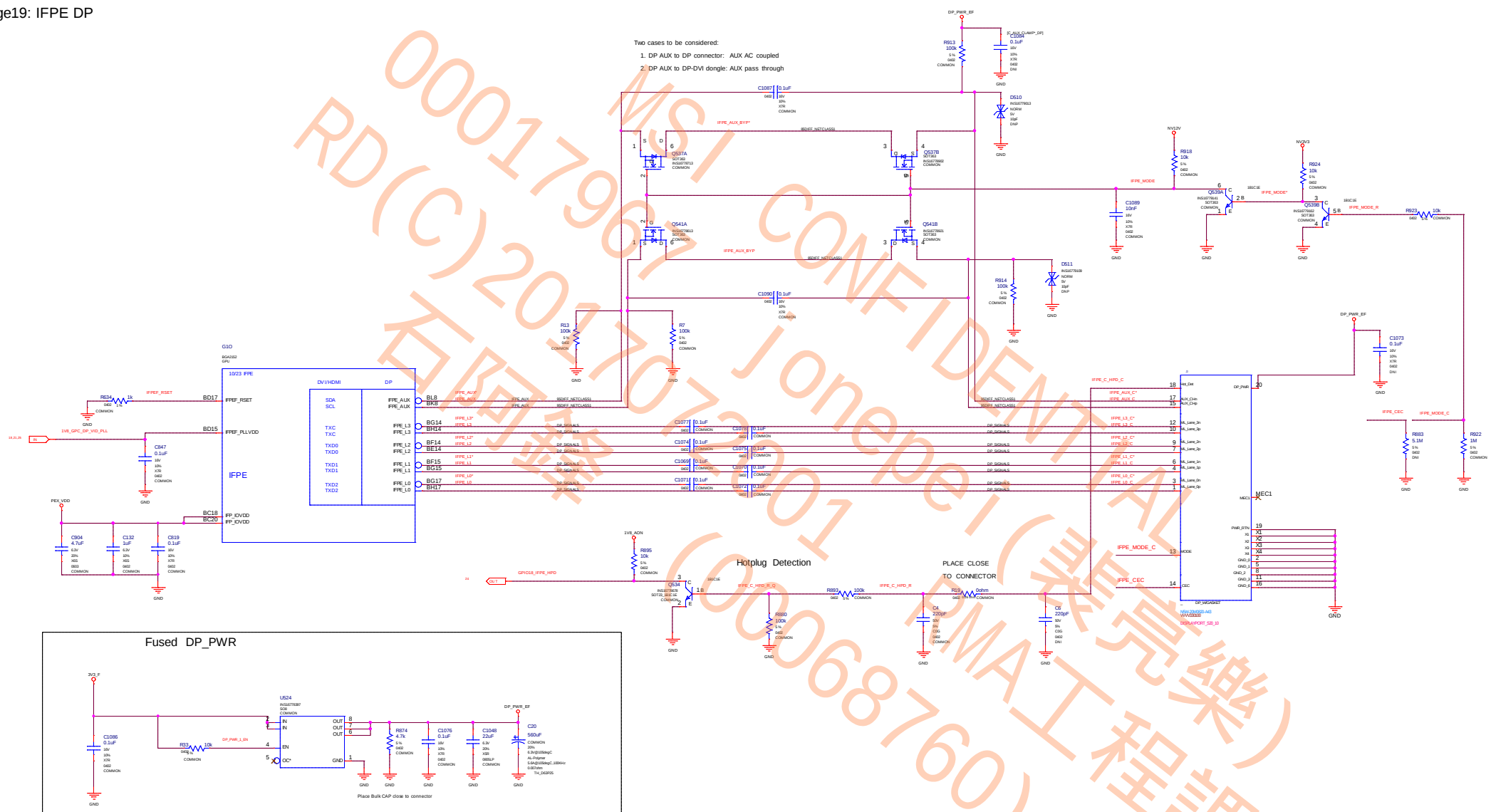


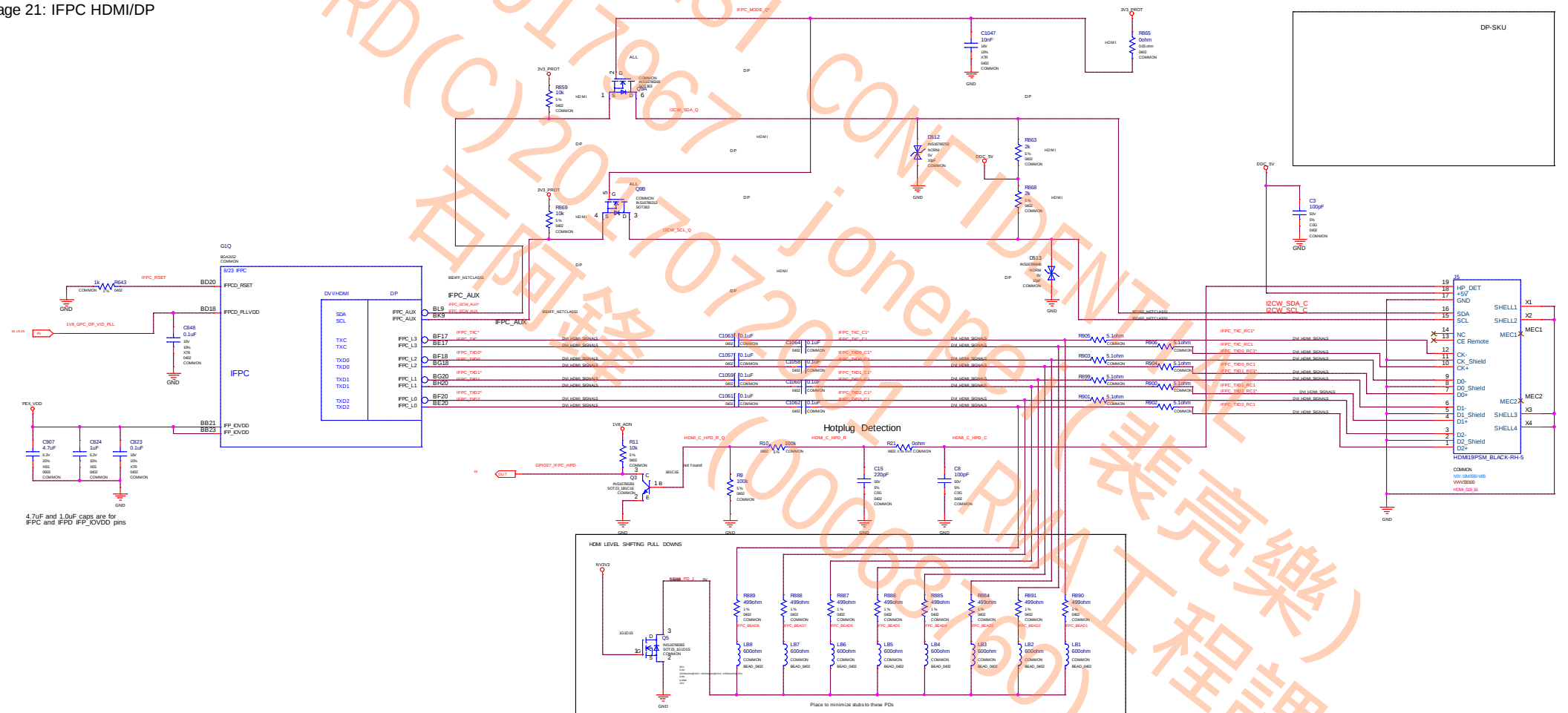
1V8_AON



1V8_MAIN







STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111	DEFAULT
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

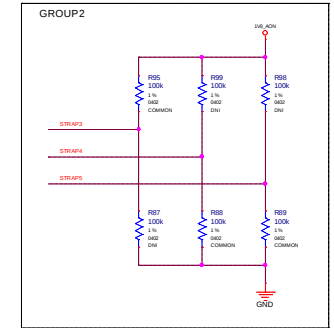
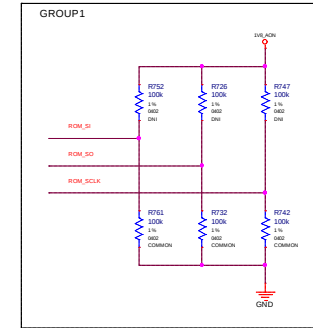
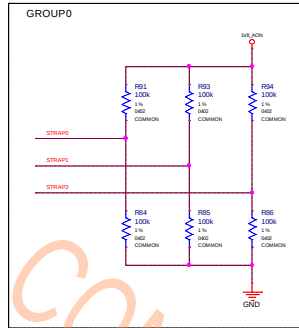
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

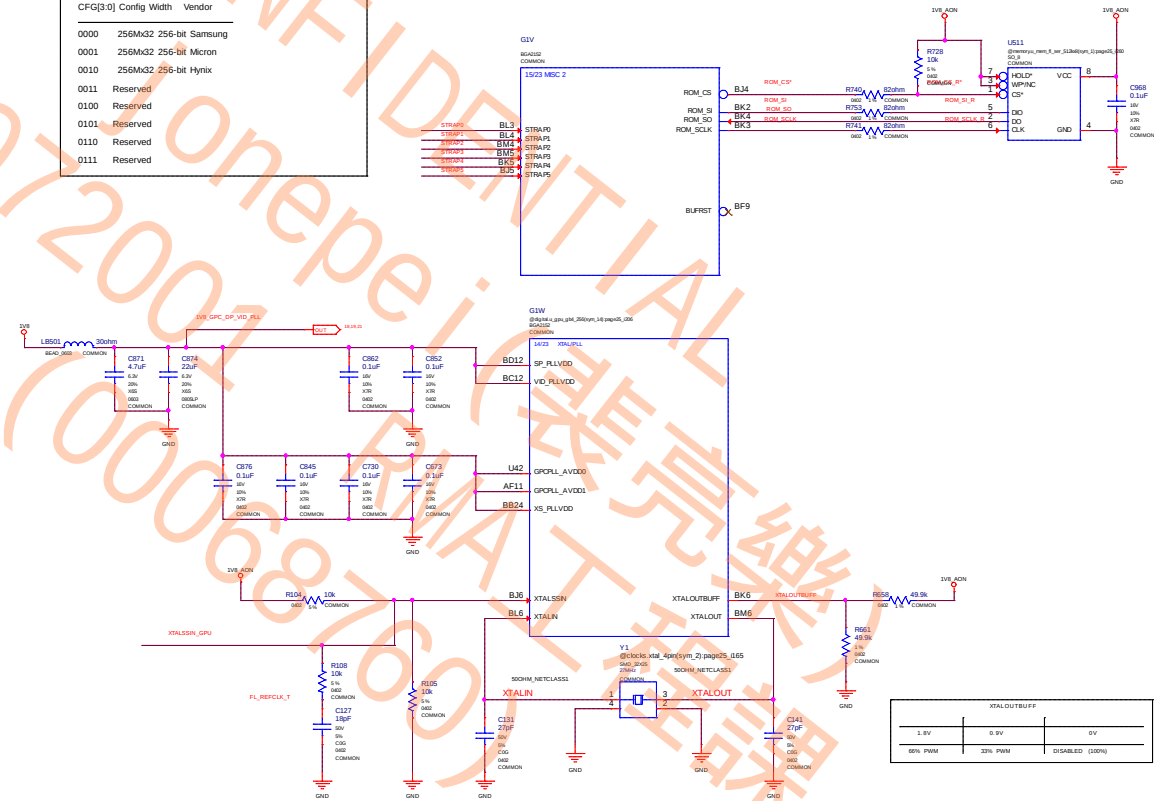
1:DEVID_SEL REBRAND
0:DEVID_SEL ORGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



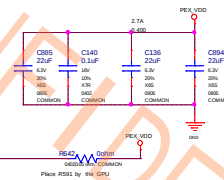
CFG(3:0)	Config	Width	Vendor
0000	256Mx32	256-bit	Samsung
0001	256Mx32	256-bit	Micron
0010	256Mx32	256-bit	Hynix
0011	Reserved		
0100	Reserved		
0101	Reserved		
0110	Reserved		
0111	Reserved		



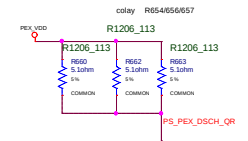
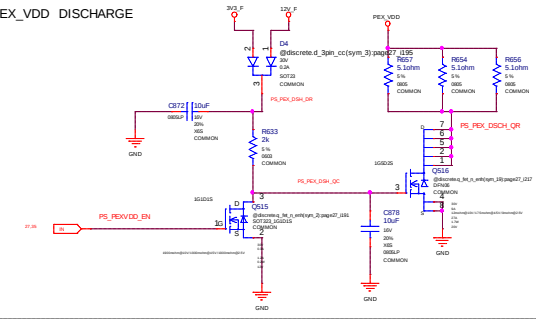
XTALOUTBUFF		
1.8V	0.9V	0V
80% PWM	20% PWM	DISABLED (2070)

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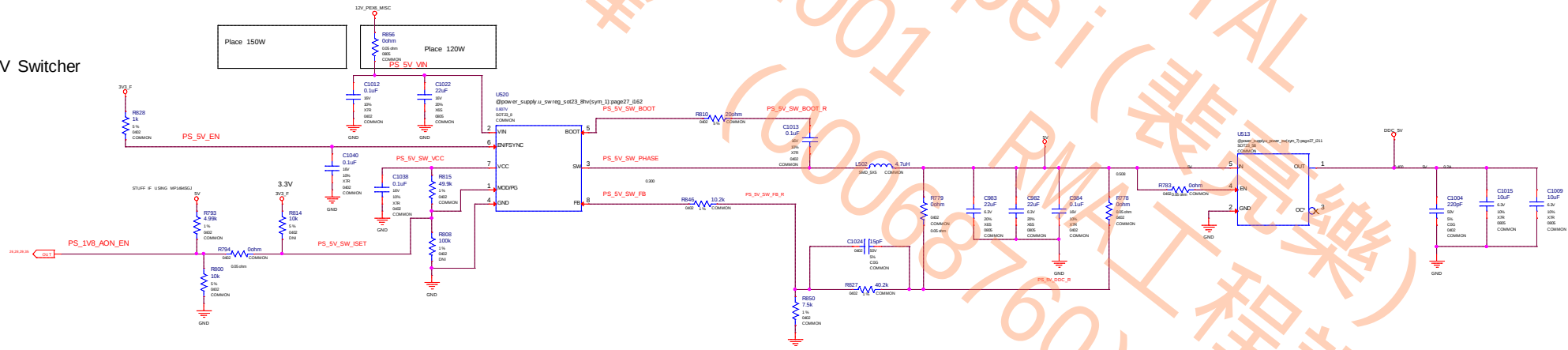
PEX PLL Switcher



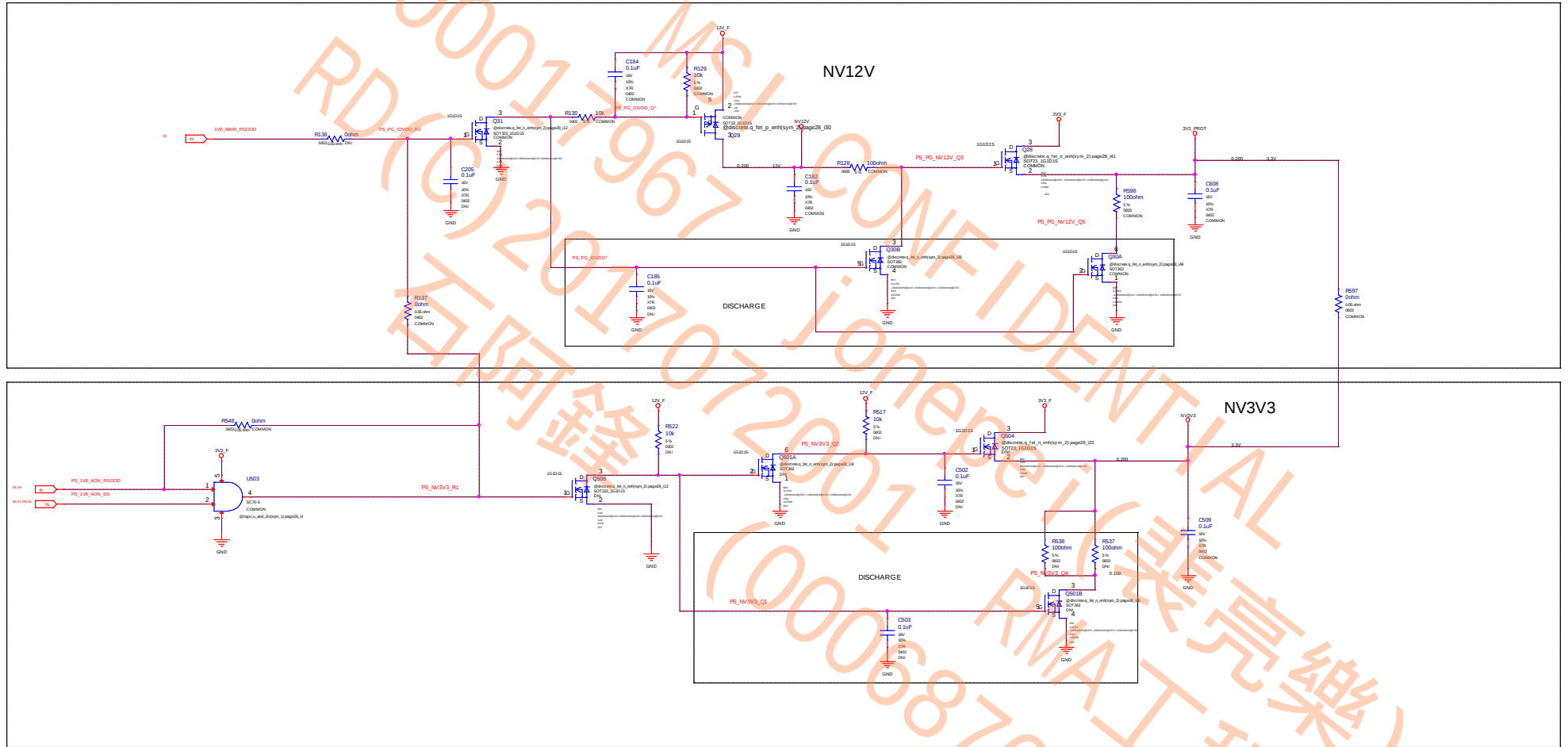
PEX_VDD DISCHARGE



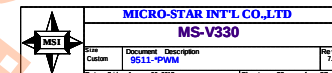
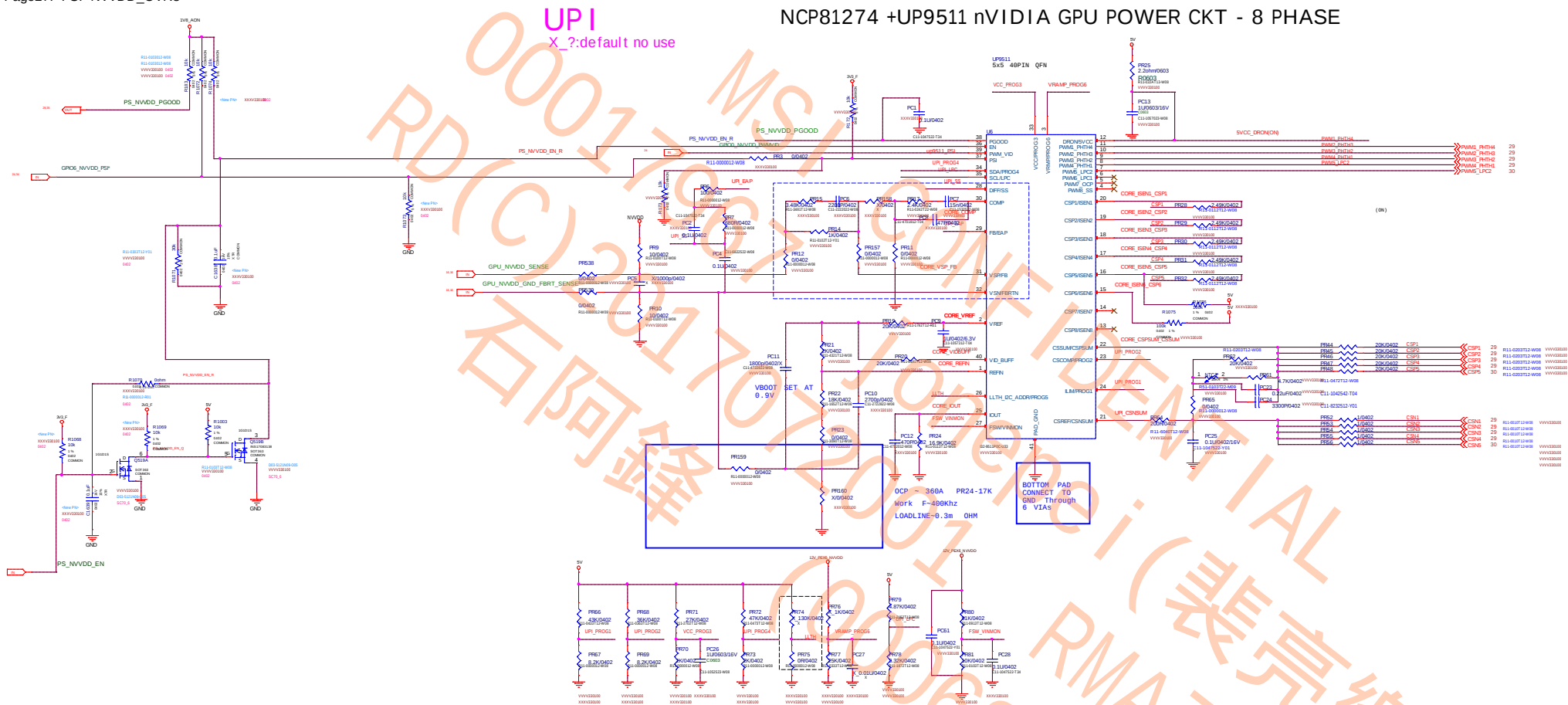
5V Switcher



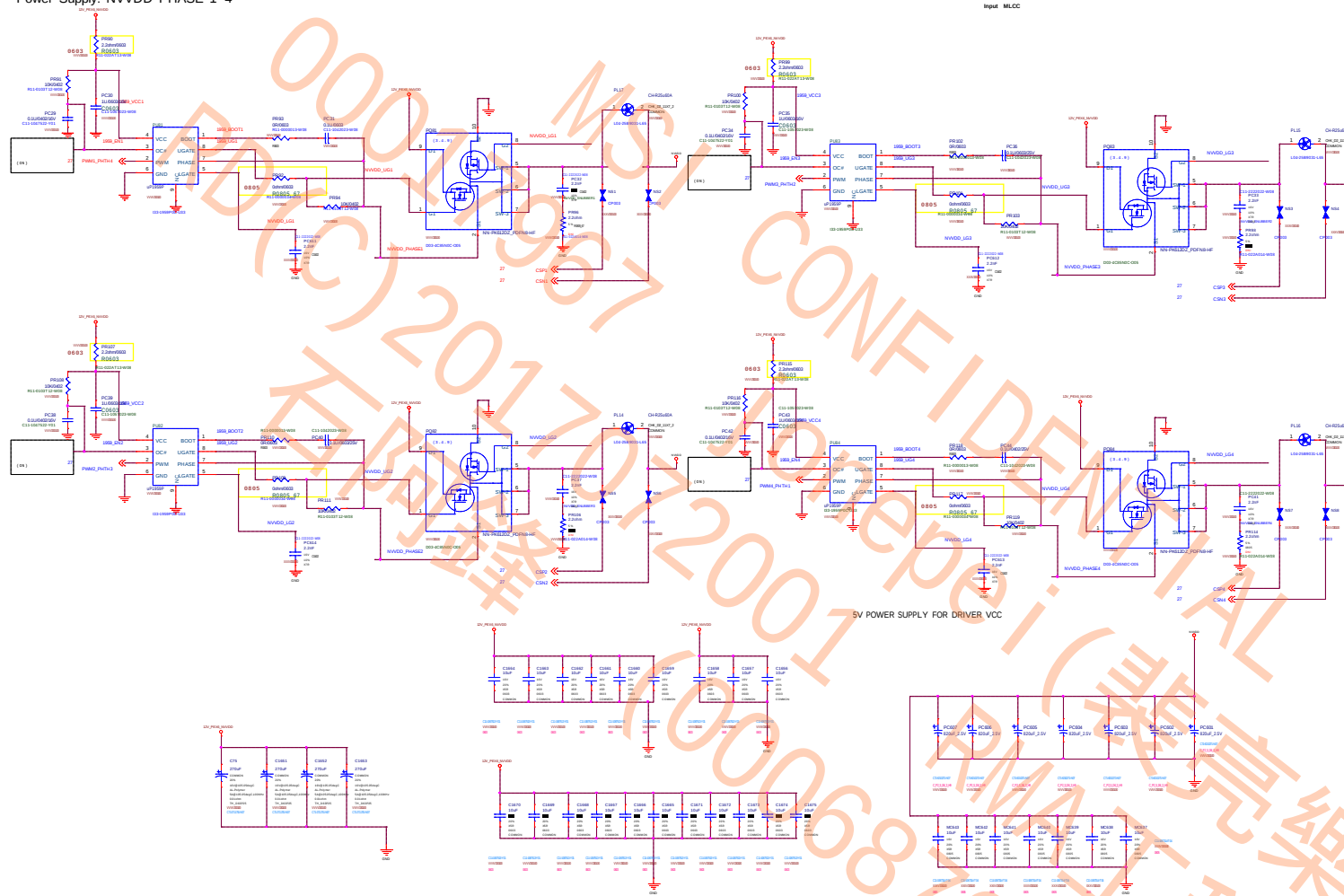
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Custom	5V		7.1
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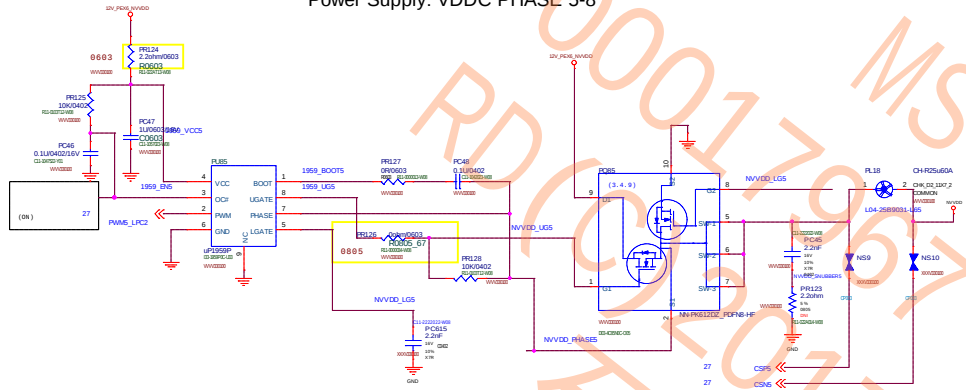
NCP81274 +UP9511 nVIDIA GPU POWER CKT - 8 PHASE



Power Supply: NVVDD PHASE 1~4

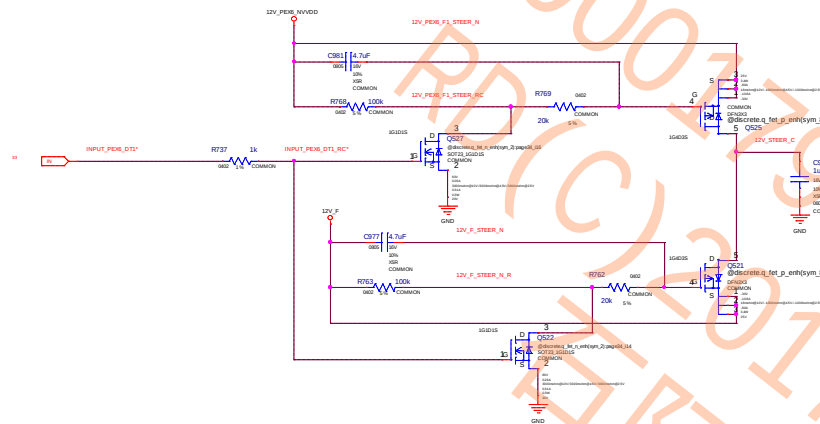


Power Supply: VDDC PHASE 5-8

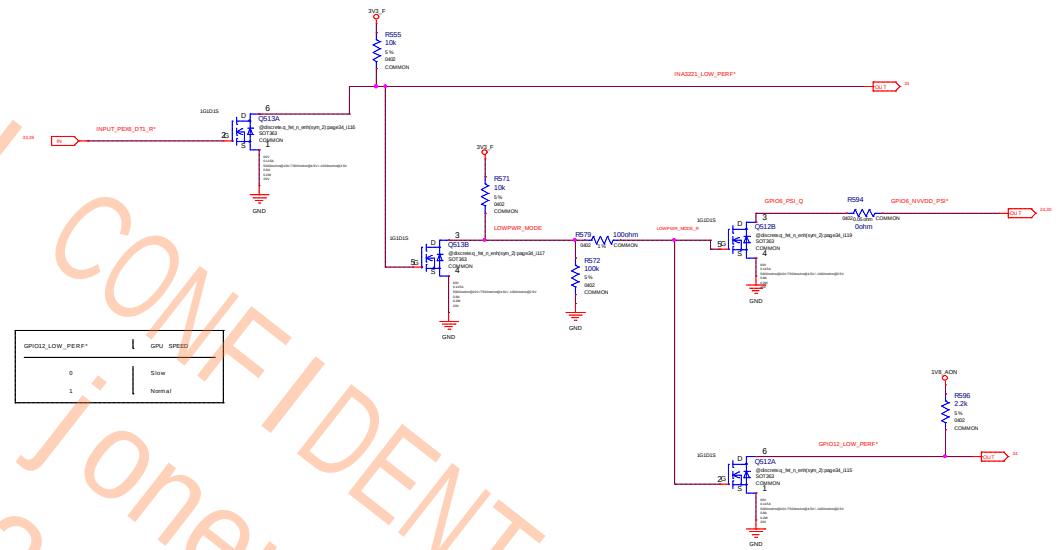


12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA

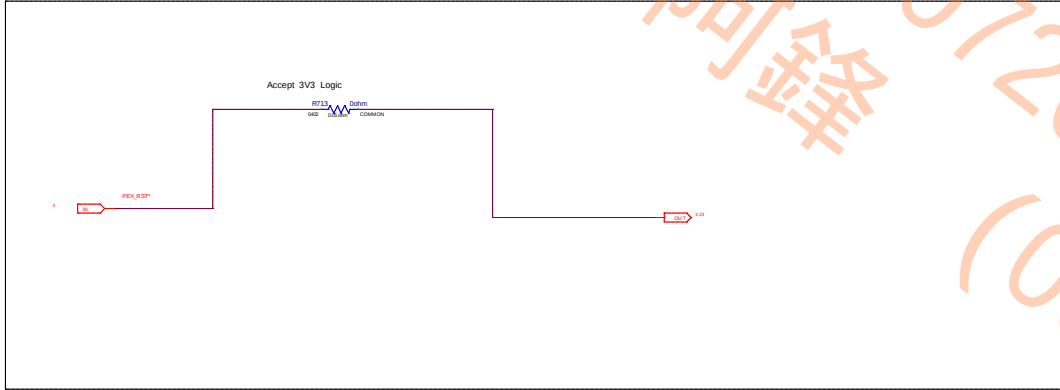


PEX Input - Power Level/PSI* Control



GeForce Logo LED

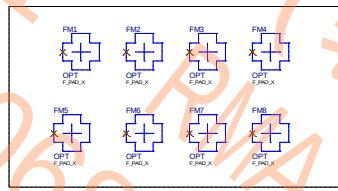
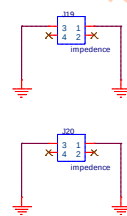
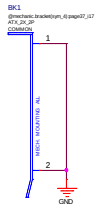
00017967 MSI CONFIDENTIAL
RD(C)20170720 jonepei (裴亮樂)
石阿鋒 (00068760) RMA工程師



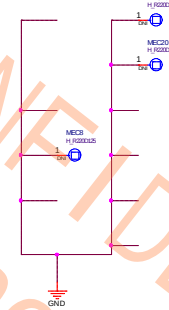
GC6 FB ENABLE
GPU_EVENT*
PEX_CLKREQ*
PEX_RST# LOGIC

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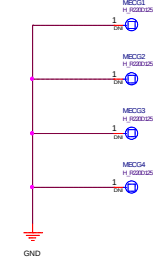
Brackets:



Mechanical Holes Symbol



GPU Stiffner



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Custom	MECH		7.2	
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