PG411 A01

GP104 - 8GB GDDR5, 256b, 256Mx32
Tall DVI-D + DP + DP + HDMI + DP

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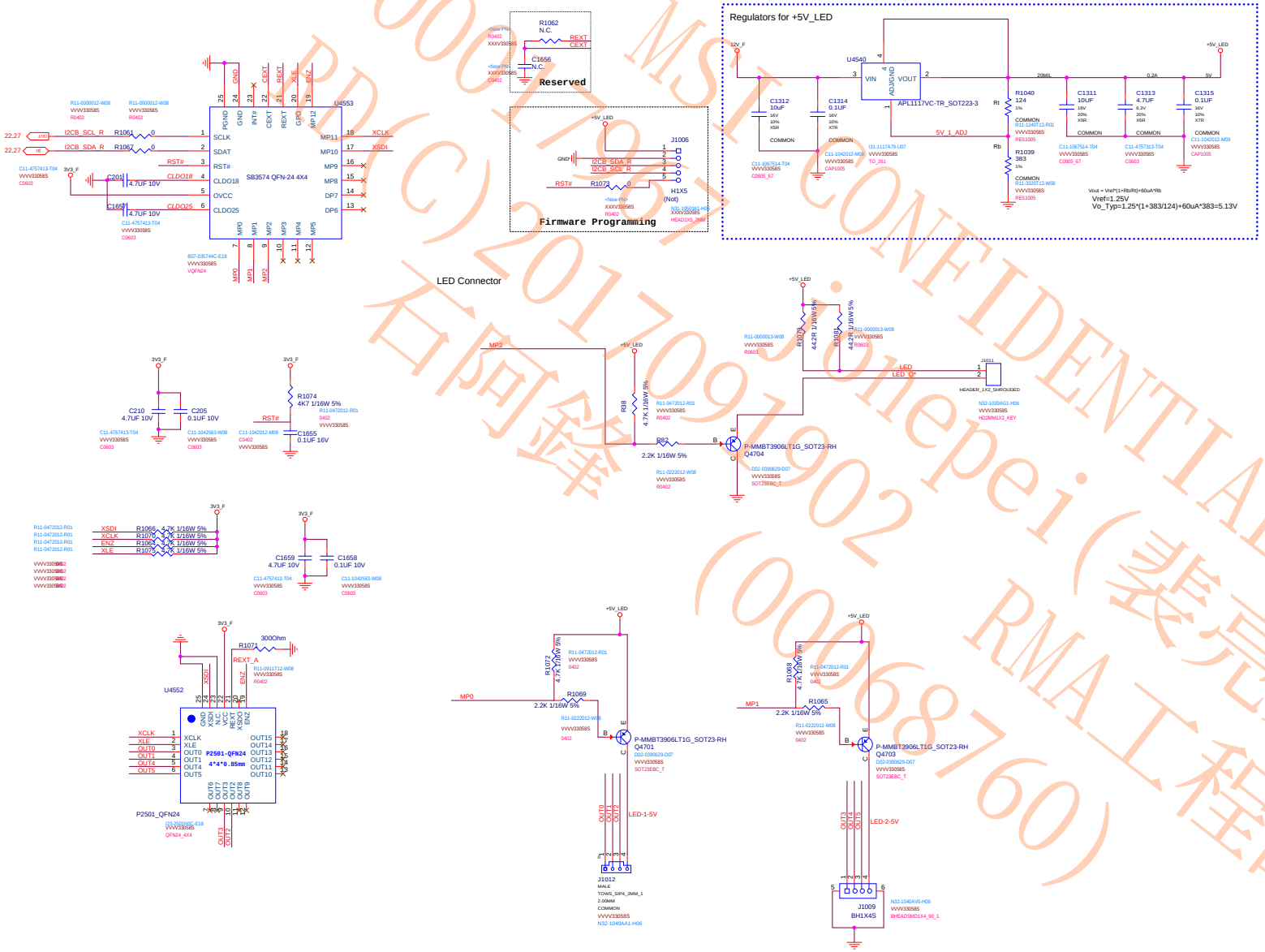

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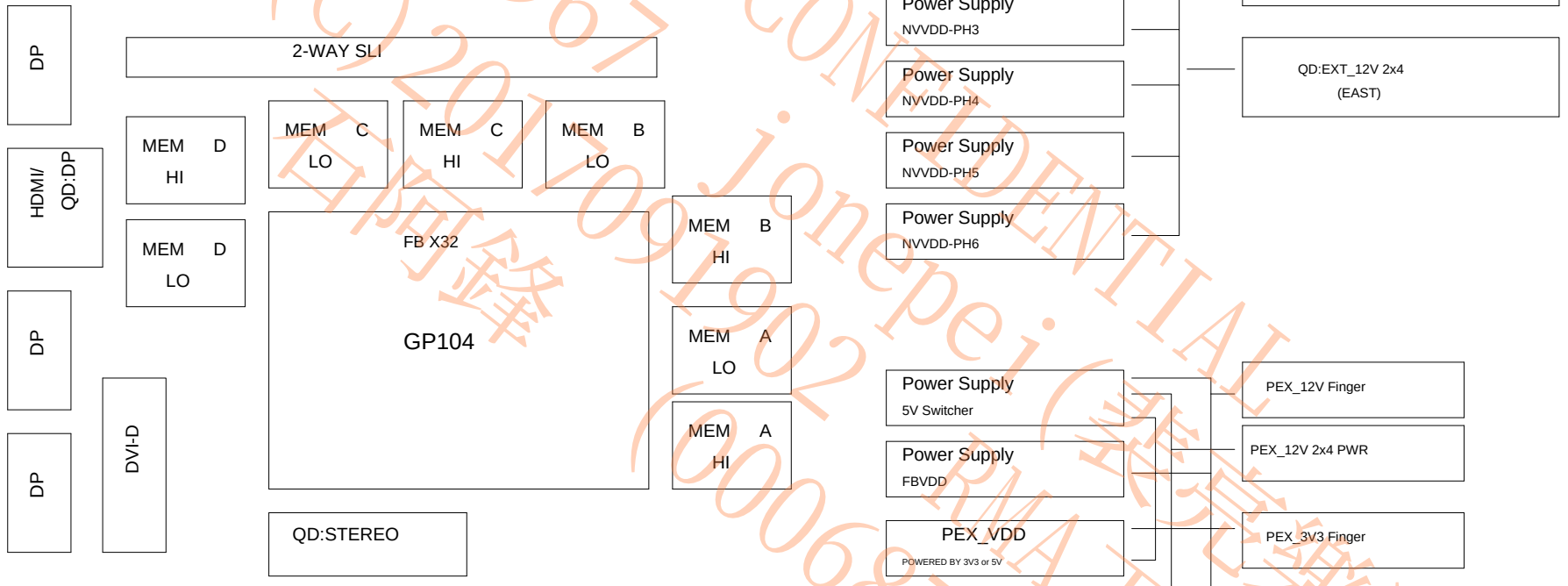
Page2: Block Diagram



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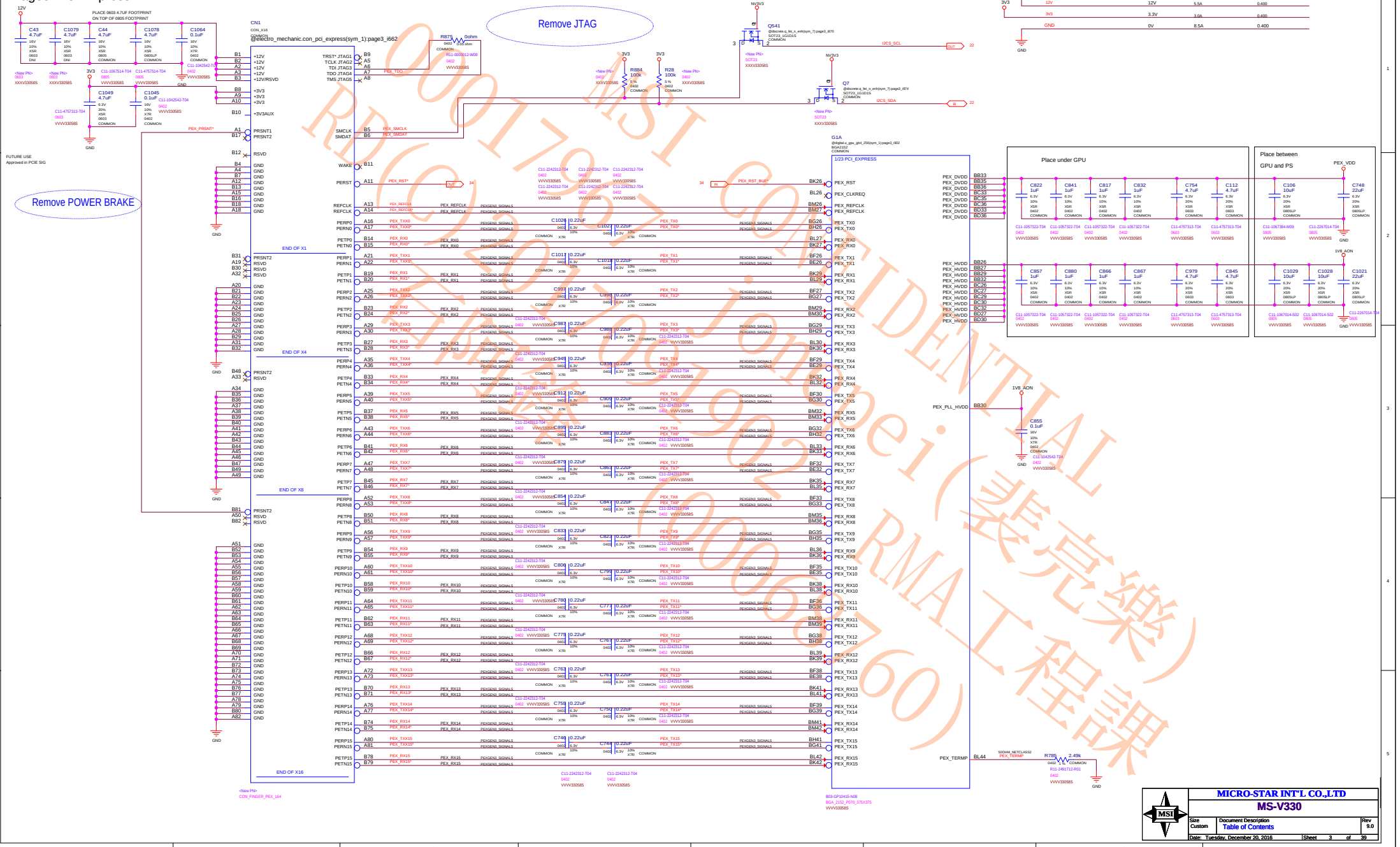
Page3: PCI Express



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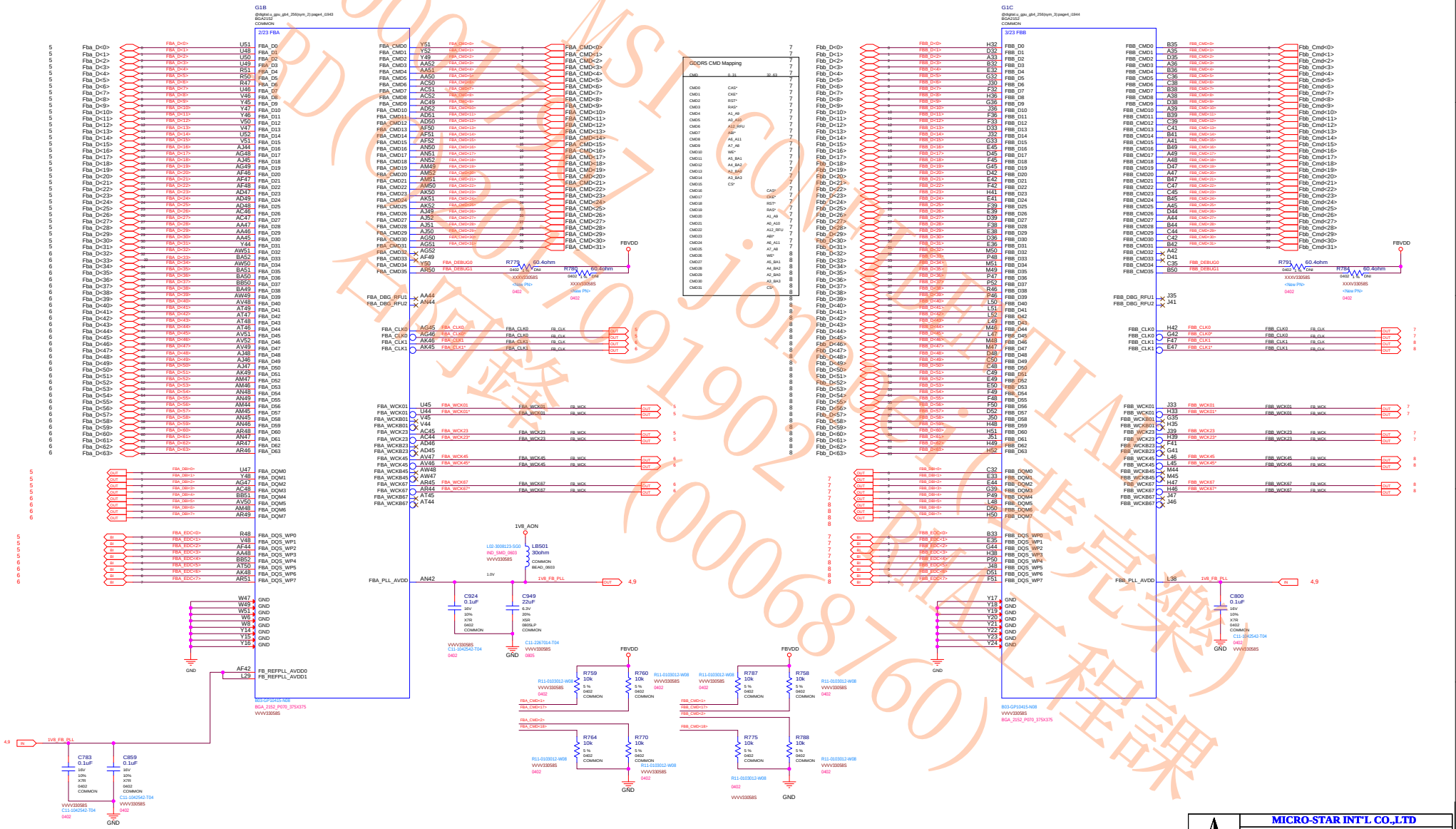
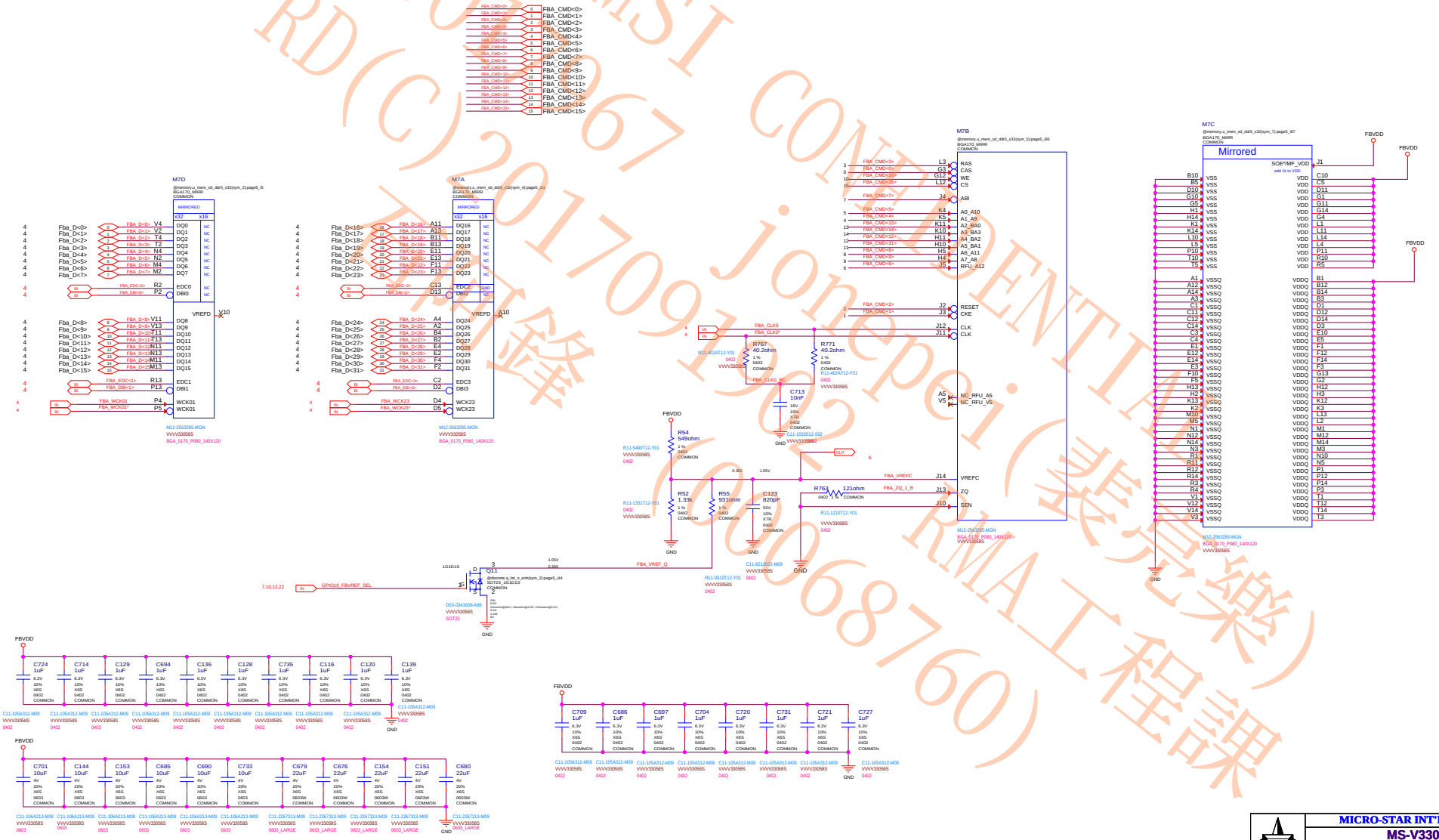
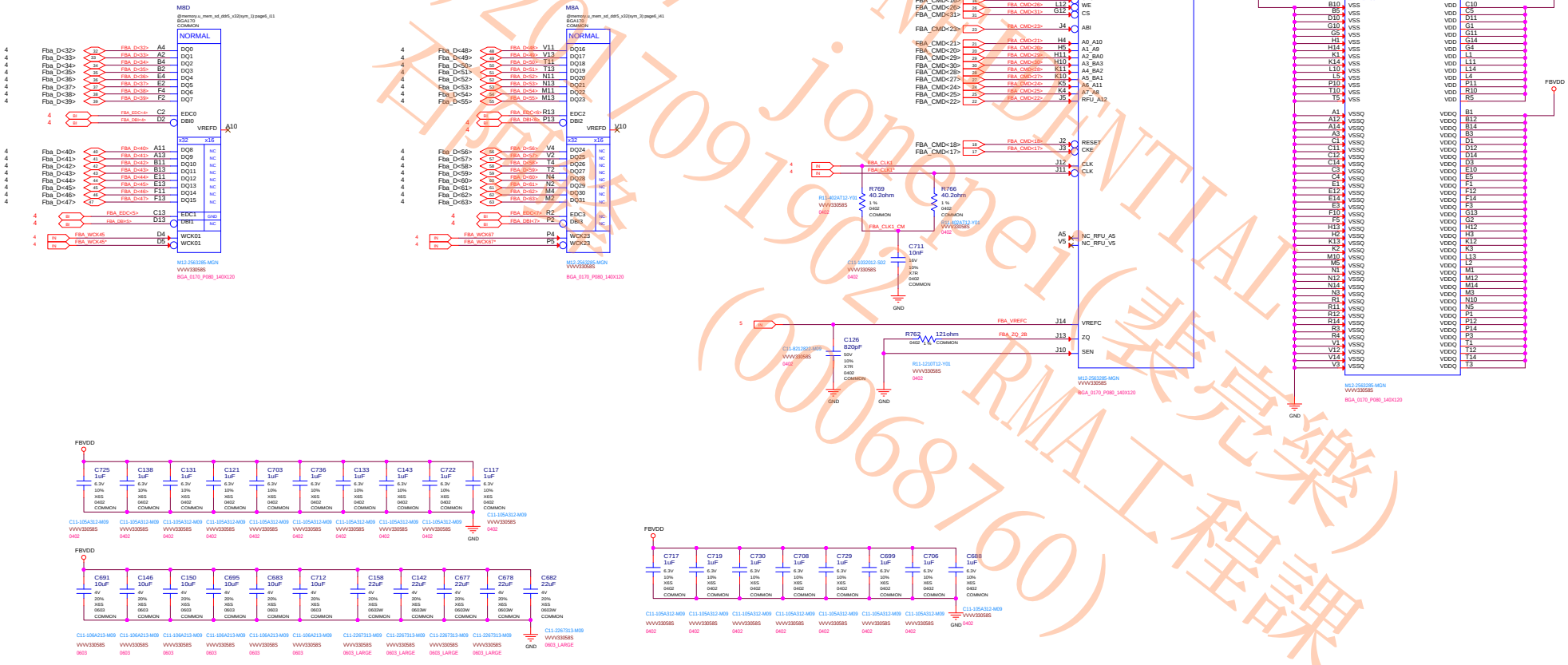




Page6: MEMORY: FBA Partition 63..32



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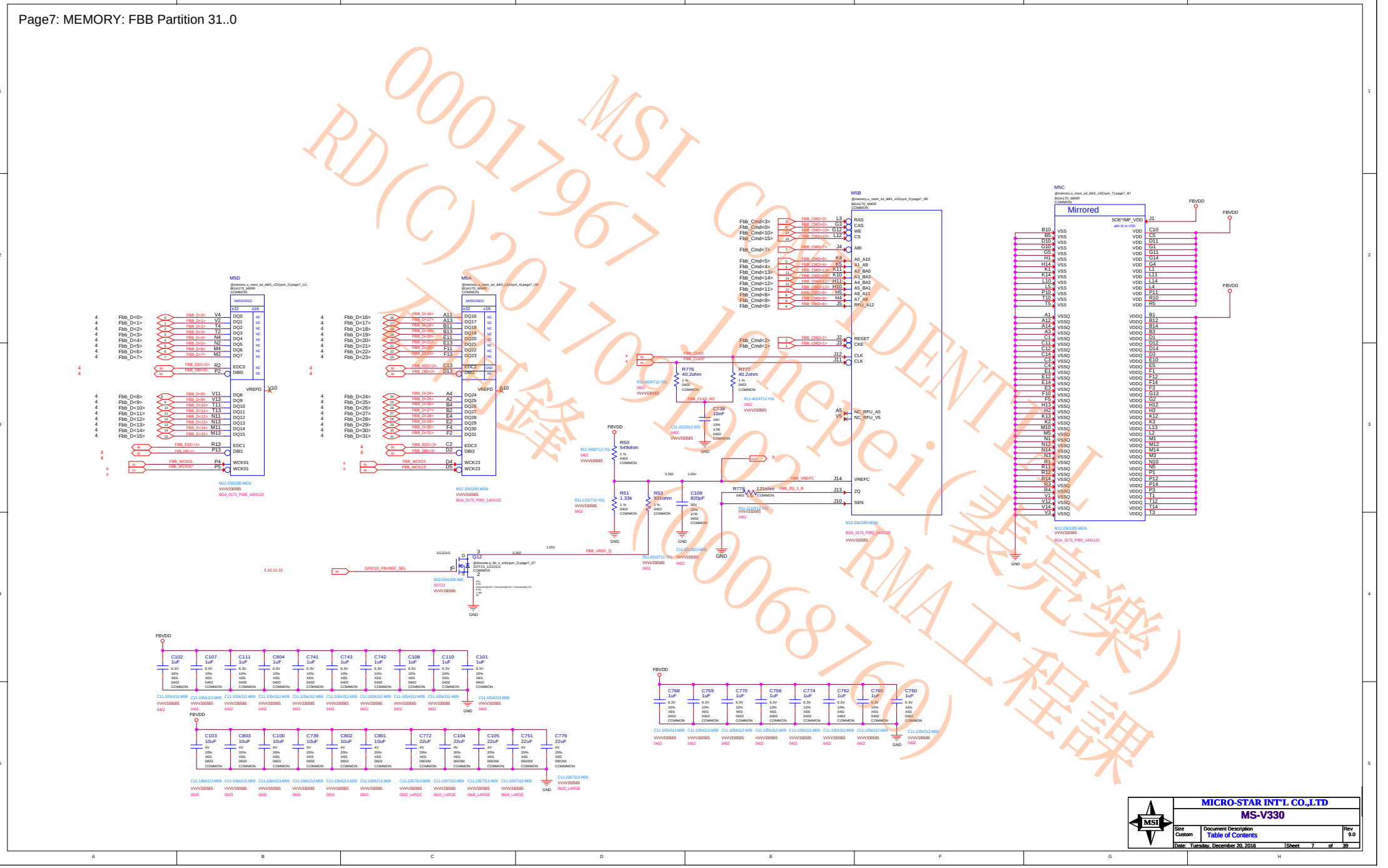
Page7: MEMORY: FBB Partition 31..0



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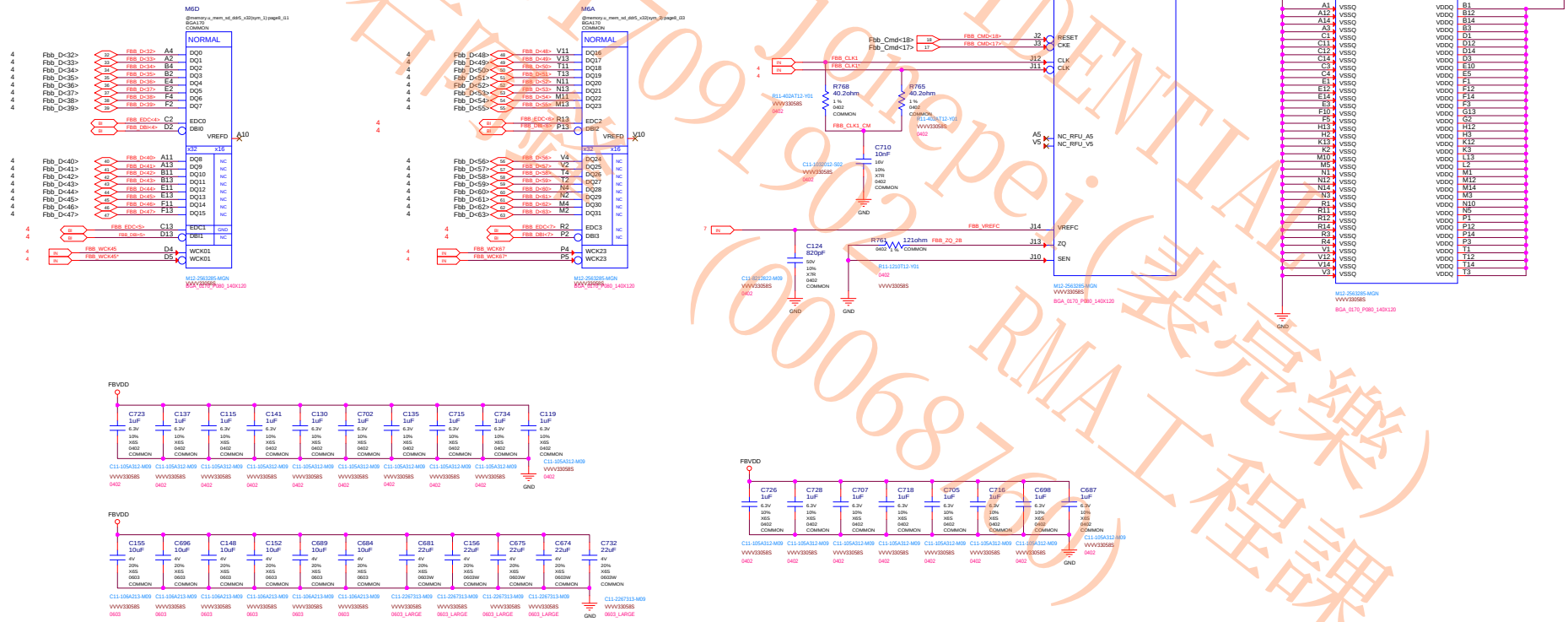

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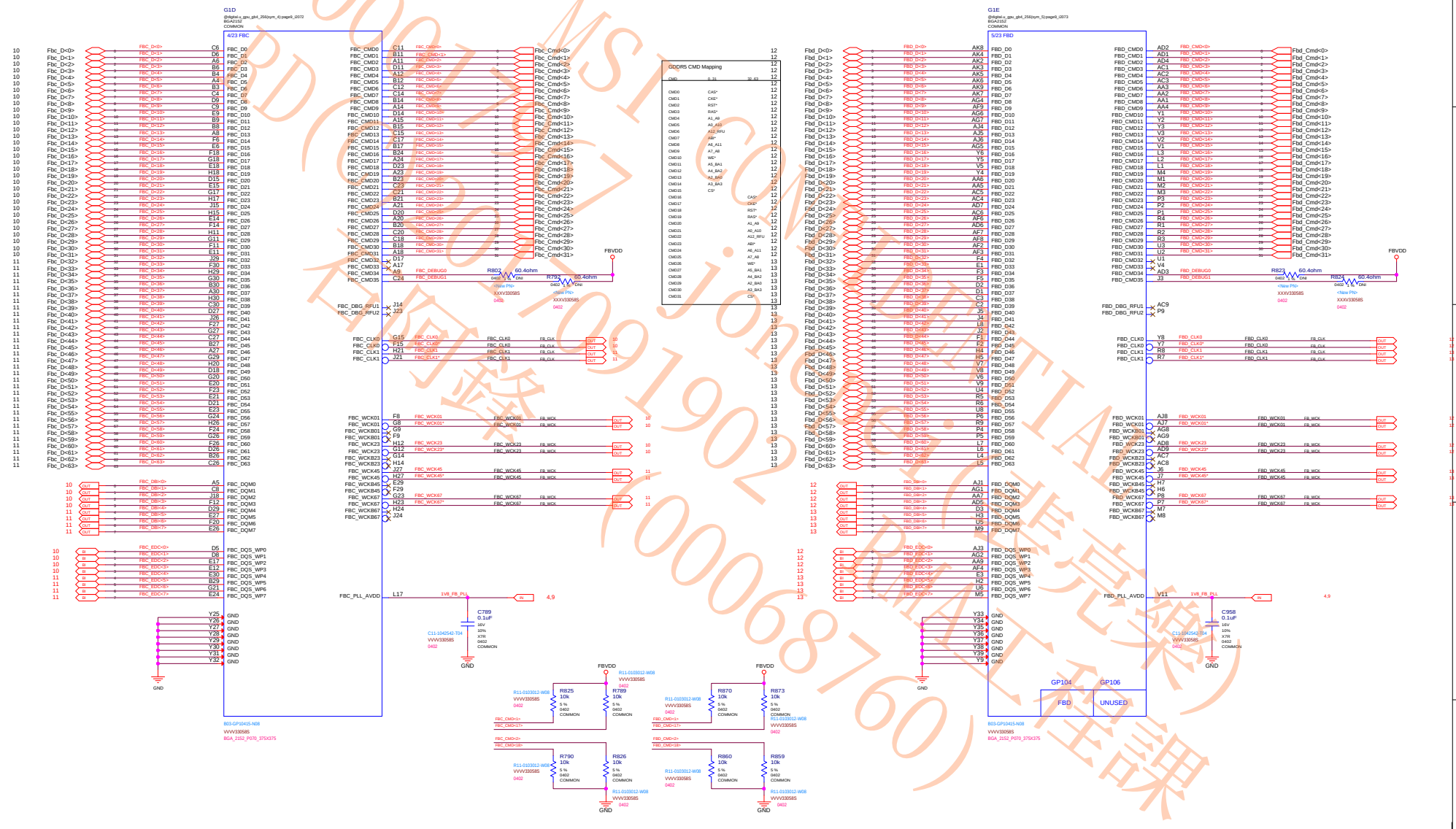

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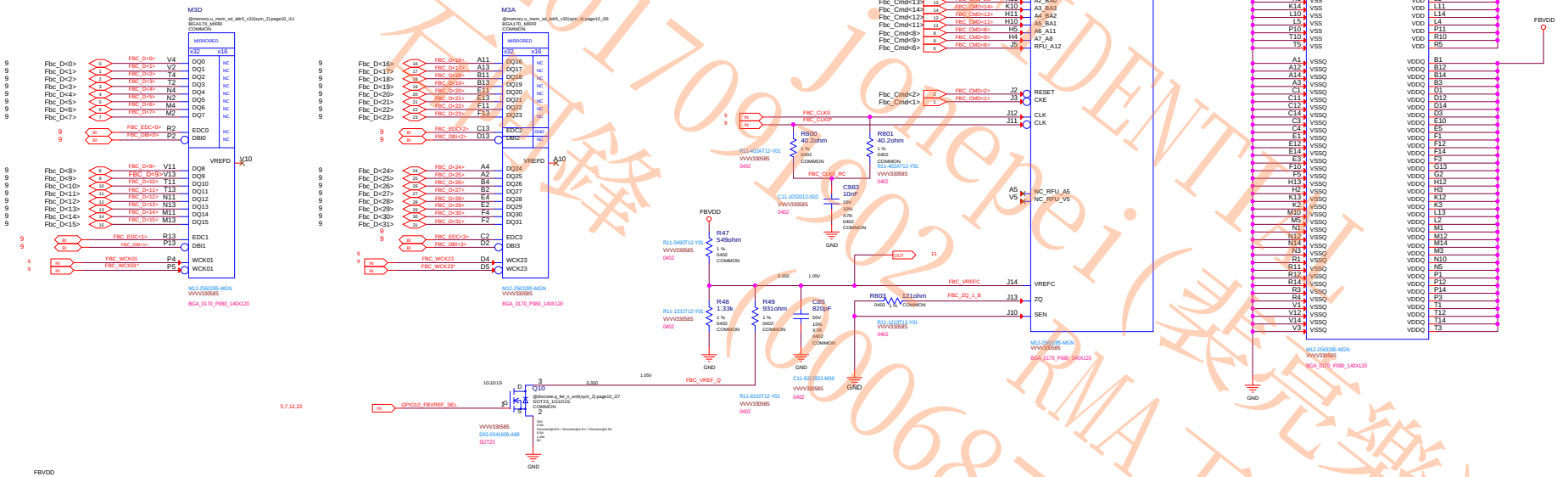

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Page11: MEMORY: FBC Partition 63..32

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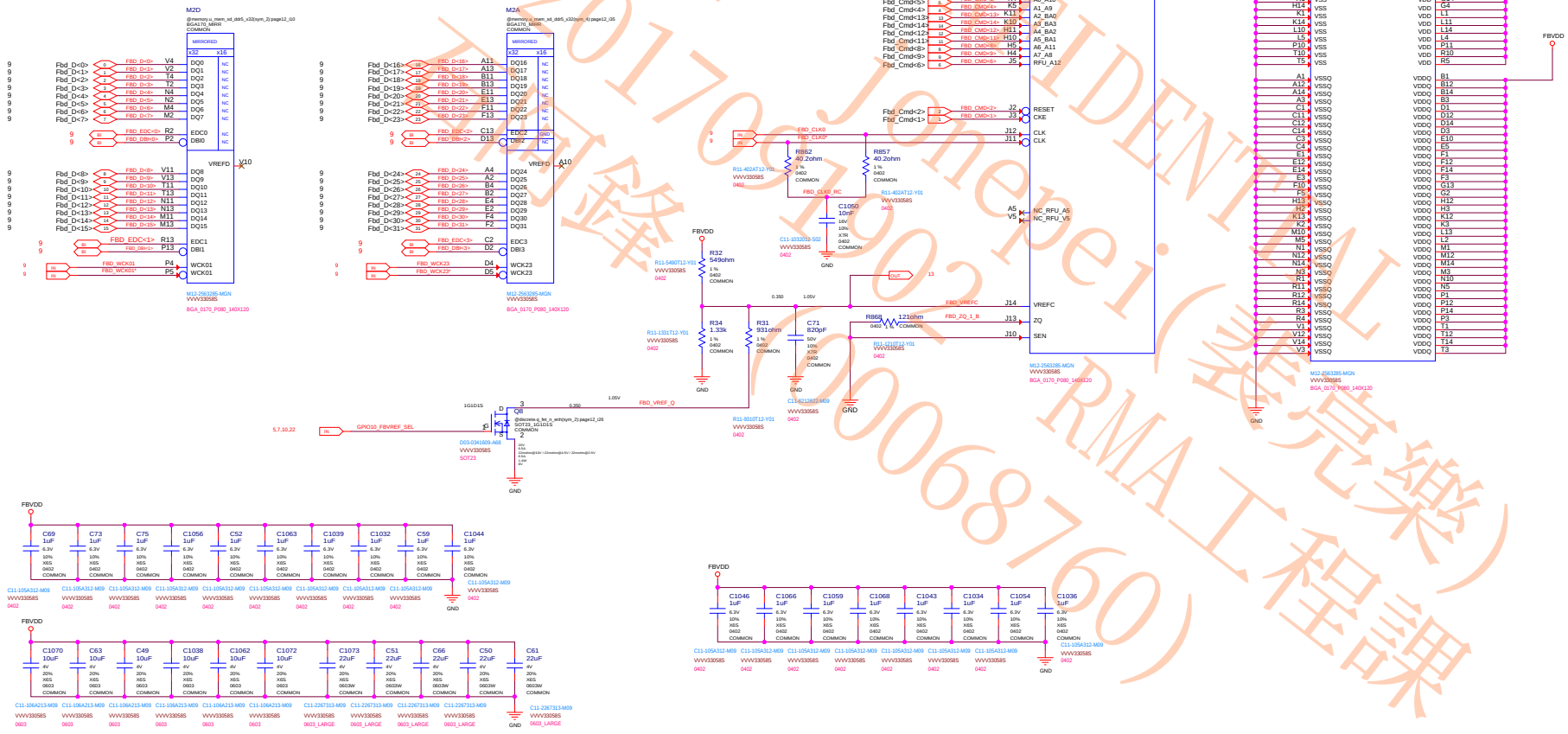

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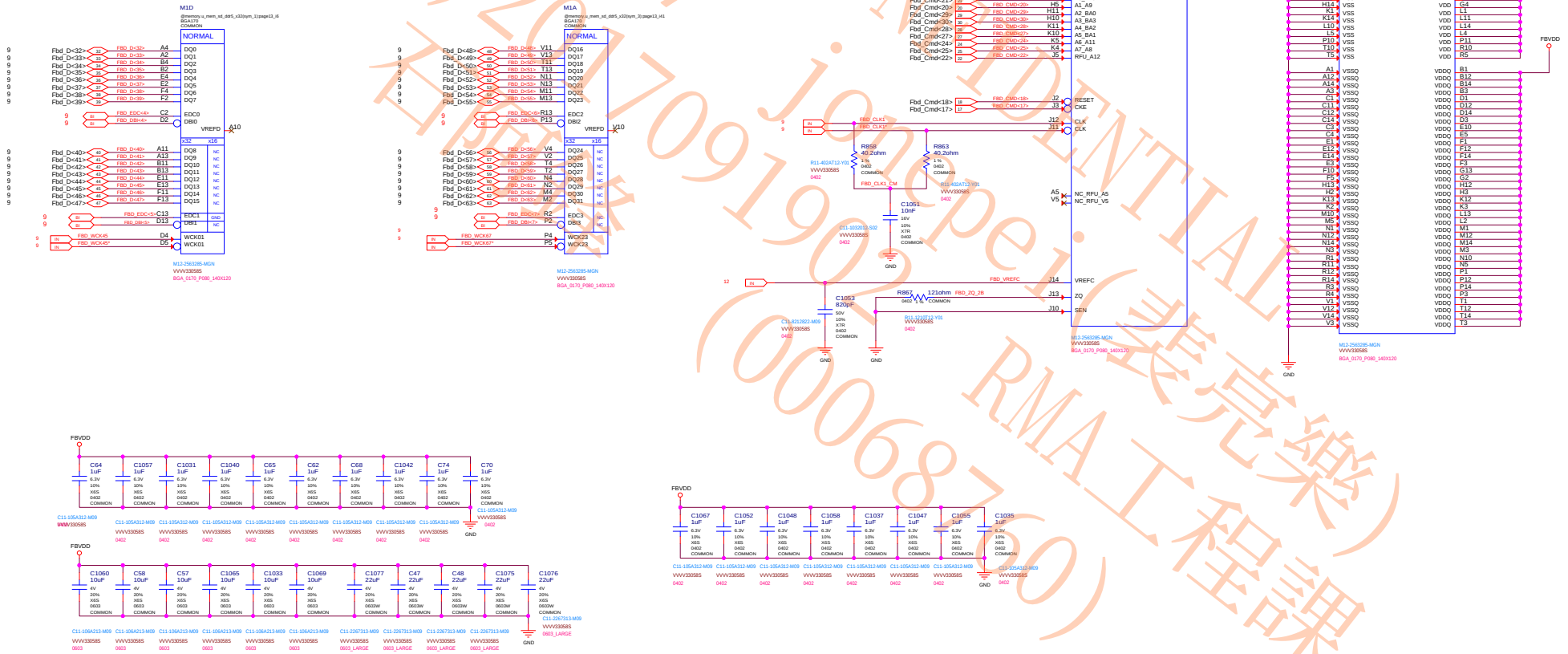
Page13: MEMORY: FBD Partition 63..32



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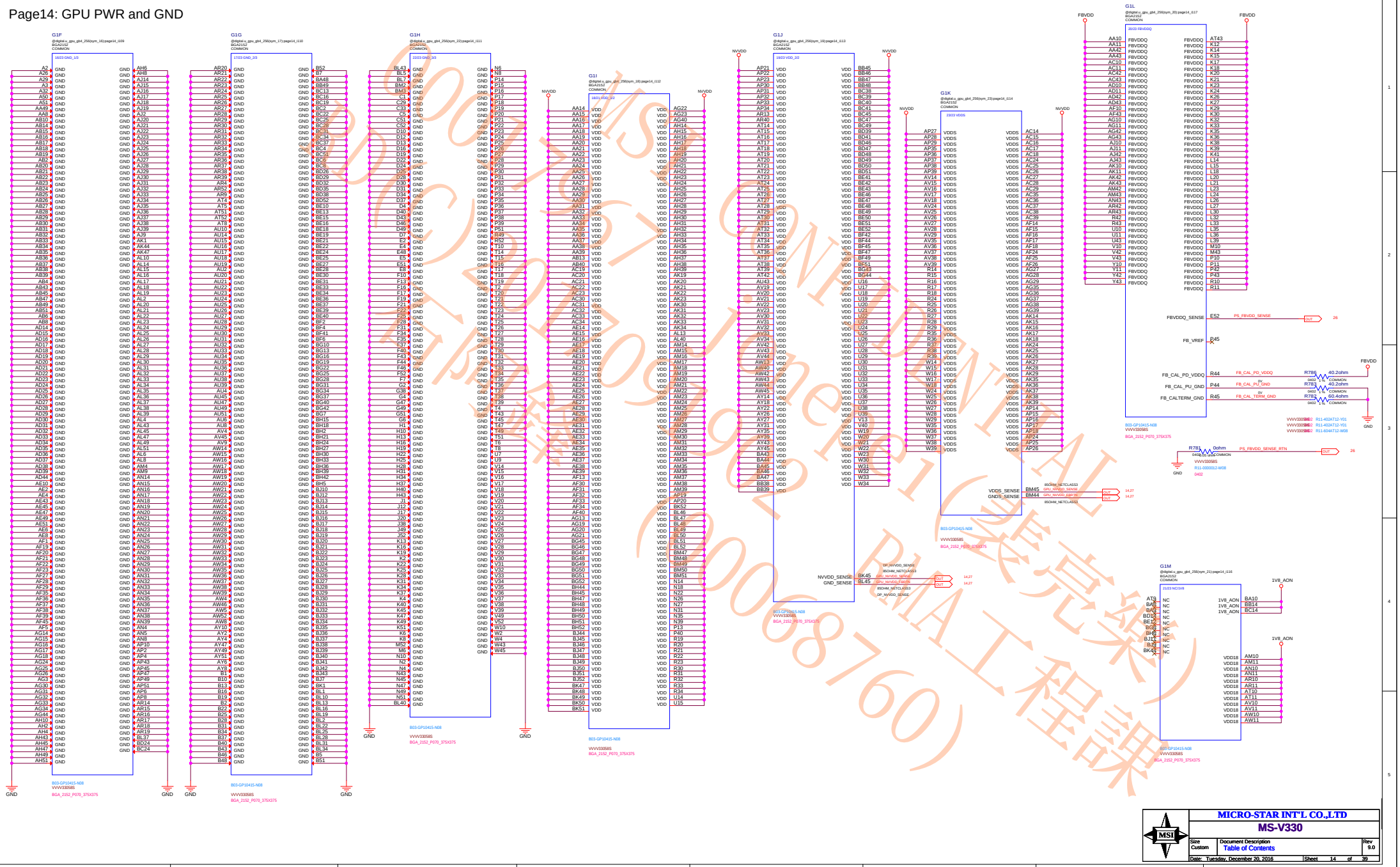
Page14: GPU PWR and GND



Page15: GPU Decoupling

FBVDD

FBVDD

Partition A — 6x 1uF and 2x 10uF

C790 1uF, C791 1uF, C792 1uF, C793 1uF, C782 1uF, C781 1uF, C758 10uF, C757 10uF

Partition B — 6x 1uF and 2x 10uF

C856 1uF, C864 1uF, C834 1uF, C788 1uF, C784 1uF, C807 1uF, C778 1uF, C821 10uF

Partition C — 6x 1uF and 2x 10uF

C972 1uF, C957 1uF, C939 1uF, C921 1uF, C948 1uF, C959 1uF, C882 10uF, C978 10uF

Partition D — 6x 1uF and 2x 10uF

C962 1uF, C960 1uF, C973 1uF, C963 1uF, C961 1uF, C968 1uF, C1000 10uF, C1001 10uF

C786 10uF, C740 10uF, C745 10uF, C937 10uF

C769 22uF, C980 22uF, C896 22uF, C824 22uF, C753 22uF, C749 22uF, C1005 22uF, C752 22uF, C1003 22uF

NVVDD

NVVDD

C747 330uF COMMON 20% 2V@105degC AL-Polymer 3.5A@105degC,100KHz 0.006ohm SMD_7343 — C71-331037E-P01 VVV330S8S CAP_SMD_7343

C113 330uF COMMON 20% 2V@105degC AL-Polymer 3.5A@105degC,100KHz 0.006ohm SMD_7343 — C71-331037E-P01 VVV330S8S CAP_SMD_7343

C776 47uF, C766 47uF, C785 22uF, C773 22uF, C771 22uF, C805 22uF

C870 10uF, C873 10uF, C877 10uF, C871 10uF, C869 10uF, C875 10uF, C876 10uF

C836 1uF, C809 1uF, C917 1uF, C838 1uF, C907 1uF, C904 1uF, C851 1uF, C812 1uF, C914 1uF, C892 1uF

C814 1uF, C810 1uF, C849 1uF, C827 1uF, C829 1uF, C839 1uF, C830 1uF, C905 1uF, C931 1uF, C889 1uF

C926 1uF, C913 1uF, C916 1uF, C828 1uF, C837 1uF, C933 1uF, C915 1uF, C952 1uF, C891 1uF, C852 1uF

C888 1uF, C835 1uF, C850 1uF, C853 1uF, C831 1uF, C890 1uF, C928 1uF, C906 1uF, C908 1uF, C935 1uF

C901 1uF, C848 1uF, C956 1uF, C797 1uF, C951 1uF

NVVDD

NVVDD

C764 330uF COMMON 20% 2V@105degC AL-Polymer 3.5A@105degC,100KHz 0.006ohm SMD_7343 — C71-331037E-P01 VVV330S8S CAP_SMD_7343

C737 47uF, C878 10uF, C868 10uF, C874 10uF, C872 10uF

C925 1uF, C929 1uF, C808 1uF, C955 1uF, C795 1uF, C811 1uF, C794 1uF, C796 1uF

C930 1uF, C954 1uF, C932 1uF, C815 1uF, C934 1uF, C813 1uF, C798 1uF, C927 1uF

STUFF C902 OR C918,C919,C898,C899

C902 330uF COMMON 20% 2V@105degC AL-Polymer 3.5A@105degC,100KHz 0.006ohm SMD_7343 — C71-471306E-P01 CAP_SMD_7343

C899 10uF, C898 10uF, C918 1uF, C919 1uF

STUFF C842 OR C843,C844,C826,C825

C842 330uF COMMON 20% 2V@105degC AL-Polymer 3.5A@105degC,100KHz 0.006ohm SMD_7343 — C71-470306E-P01 CAP_SMD_7343

C843 10uF, C844 10uF, C826 1uF, C825 1uF

1V8_AON

1V8_AON

place 1 0.1uF cap near BA10

C1007 4.7uF, C989 1uF, C969 0.1uF, C970 0.1uF

place 1 0.1uf cap for BB14 and BC14 to share

VDD18

1V8_AON

C984 0.1uF, C860 0.1uF, C840 0.1uF

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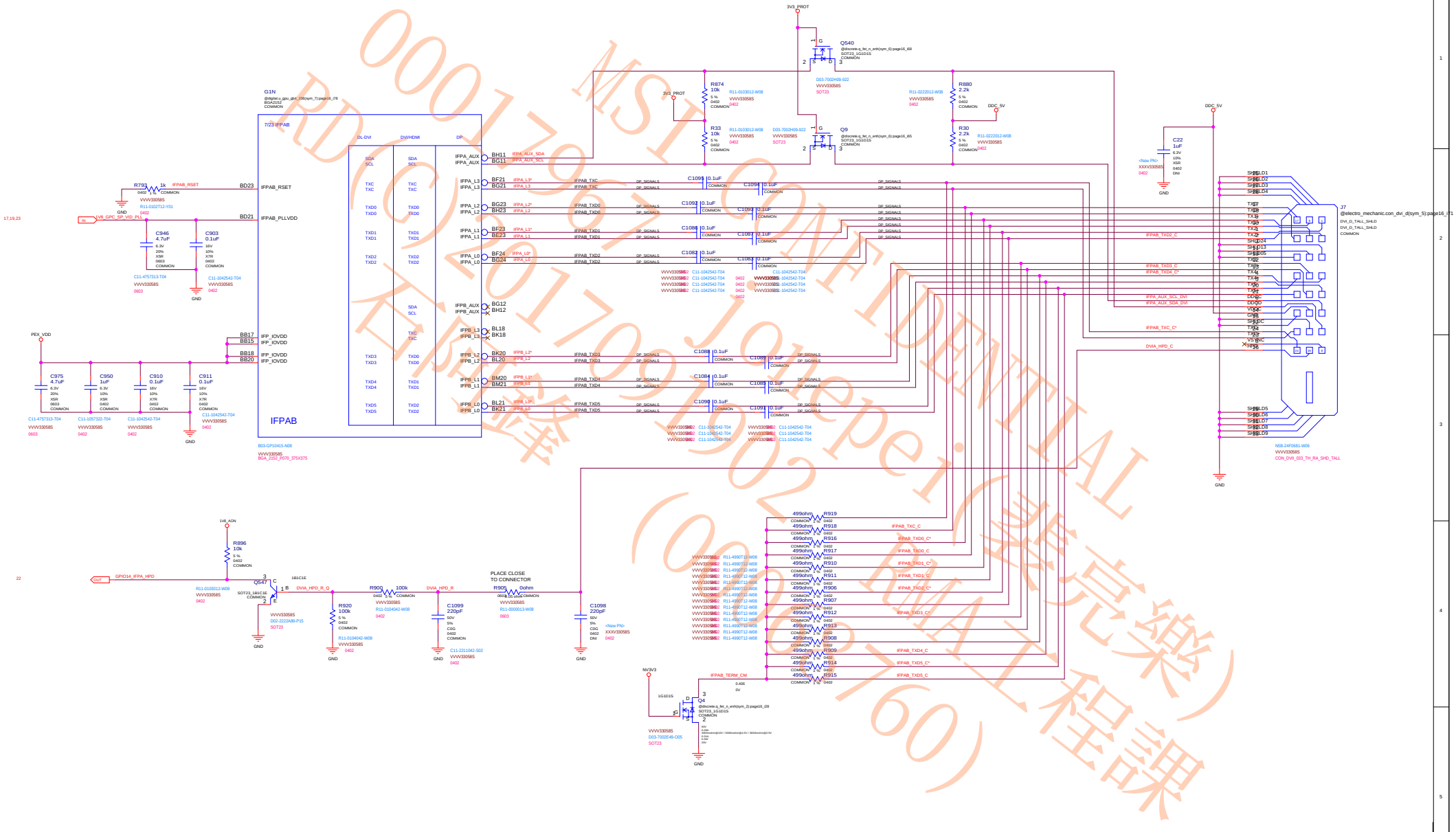

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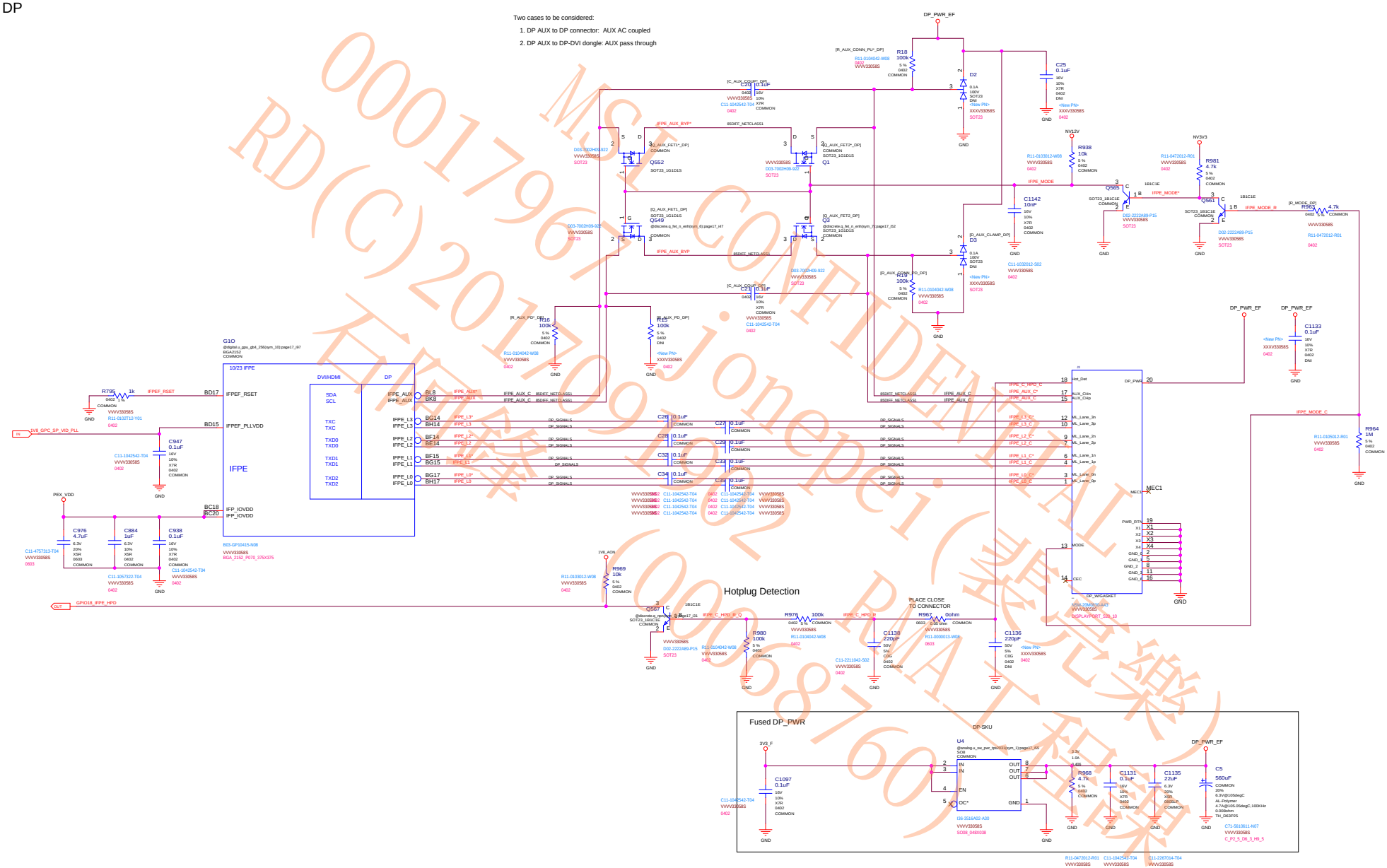
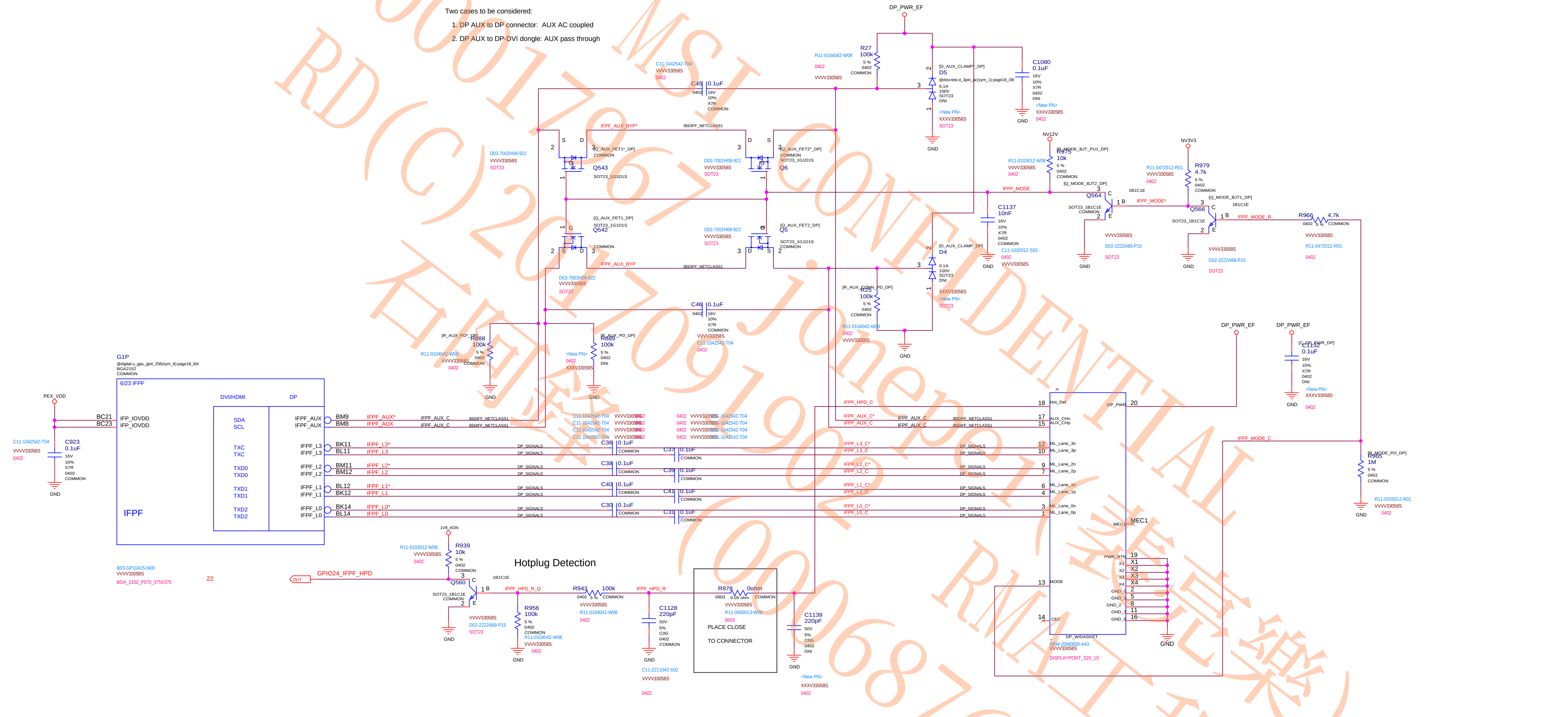
Page17: IFPE DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



Page18: IFPF DP



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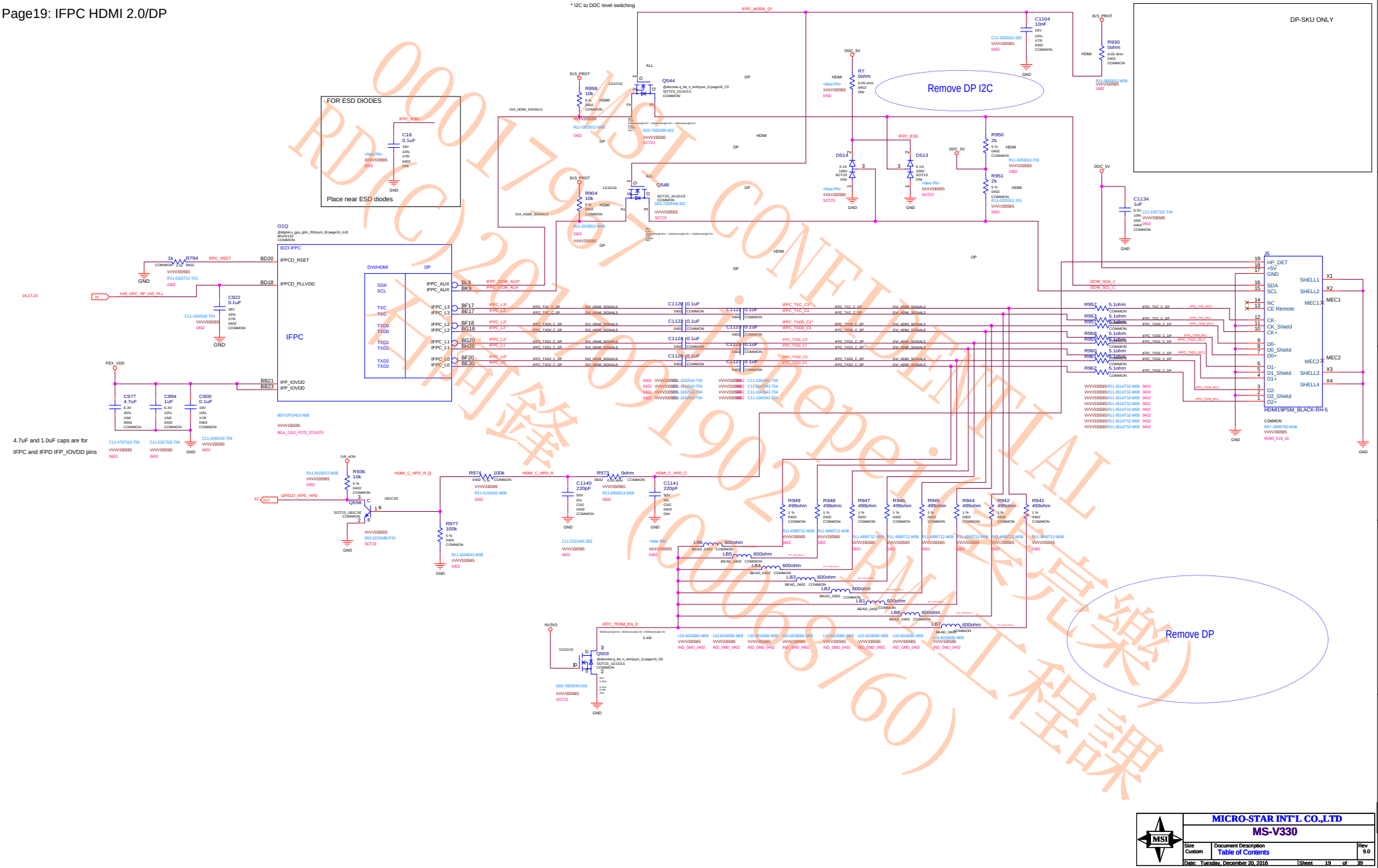
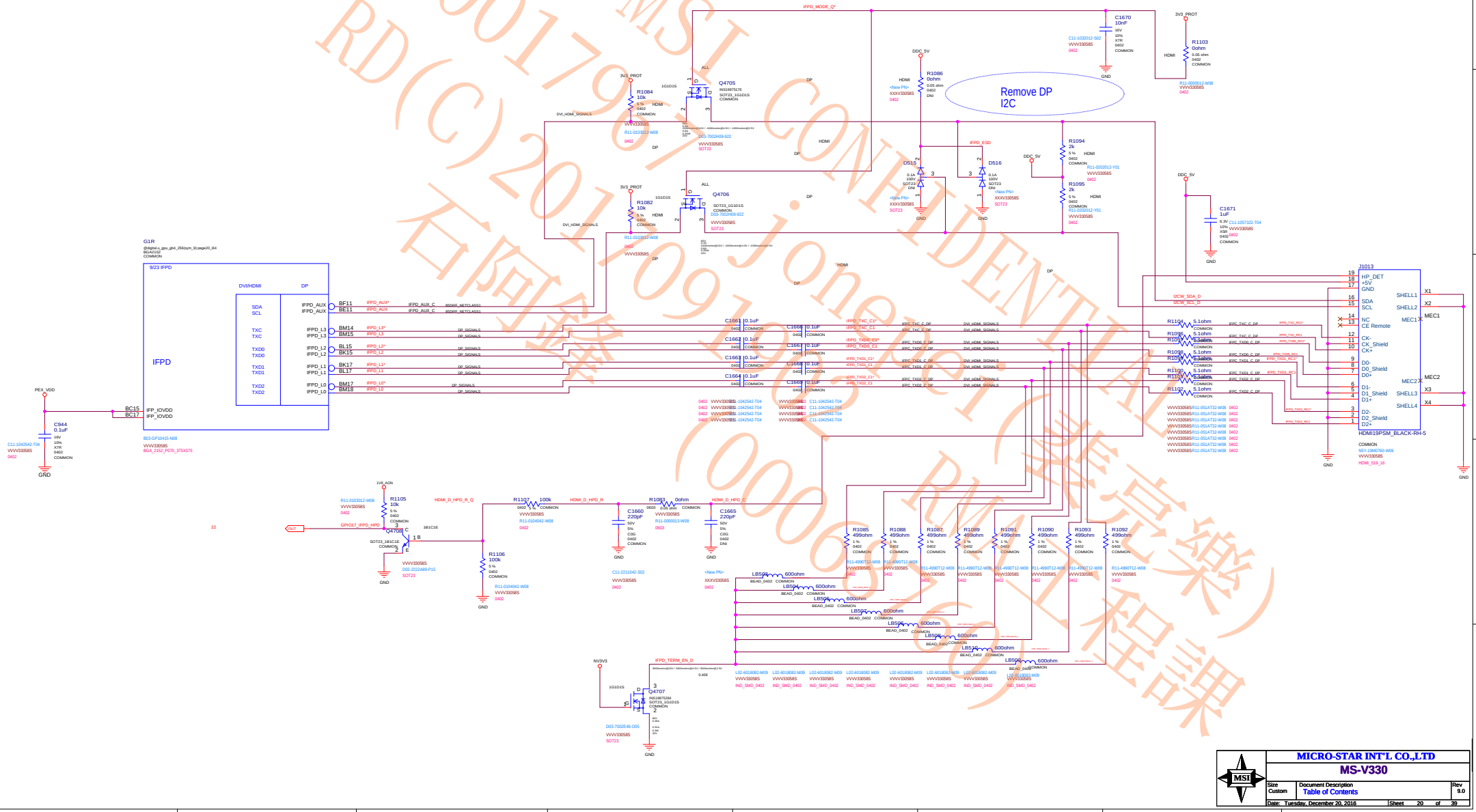
Page19: IFPC HDMI 2.0/DP



Page20: IFPD DP



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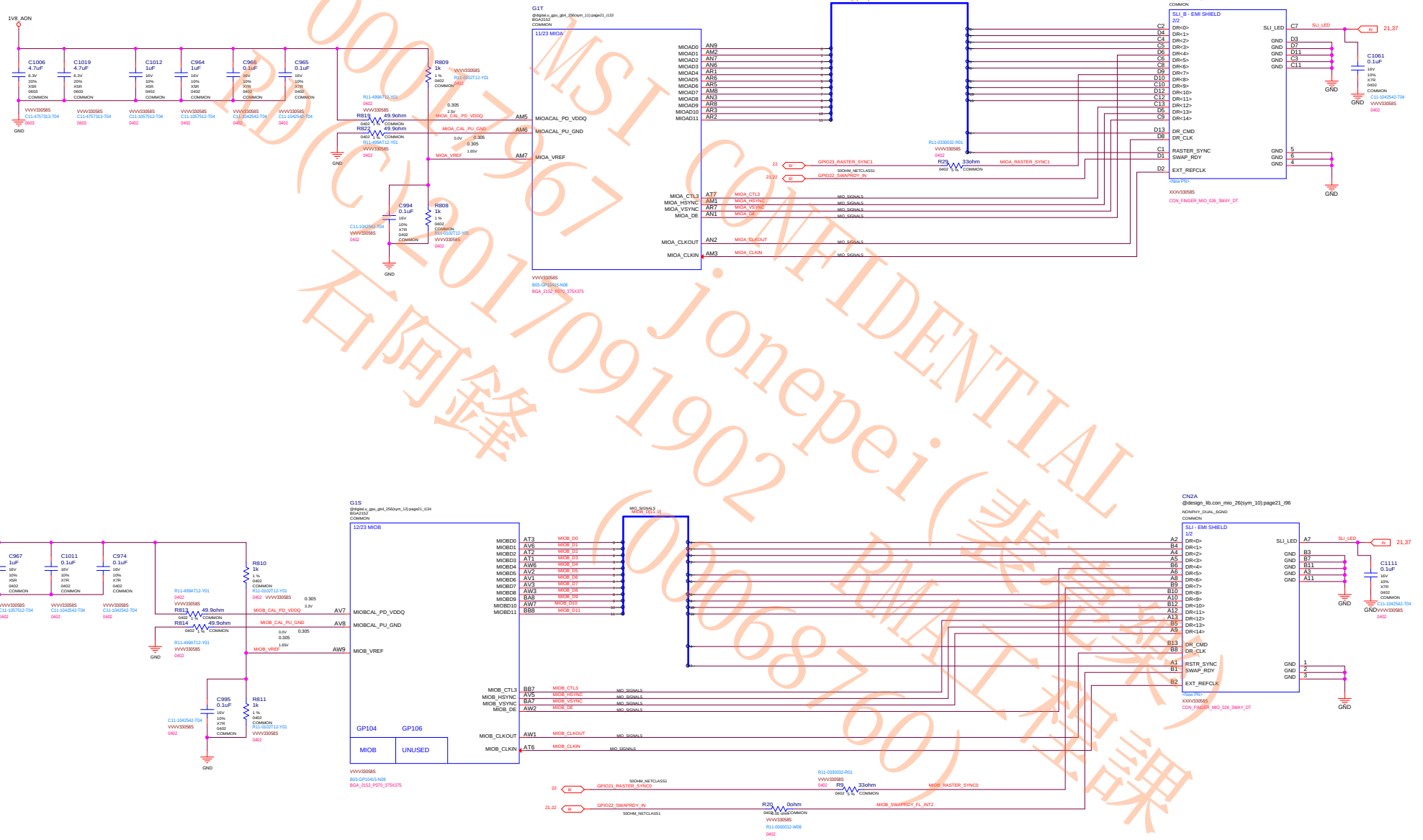
Page21: MIOA/B Interface and FRAME LOCK



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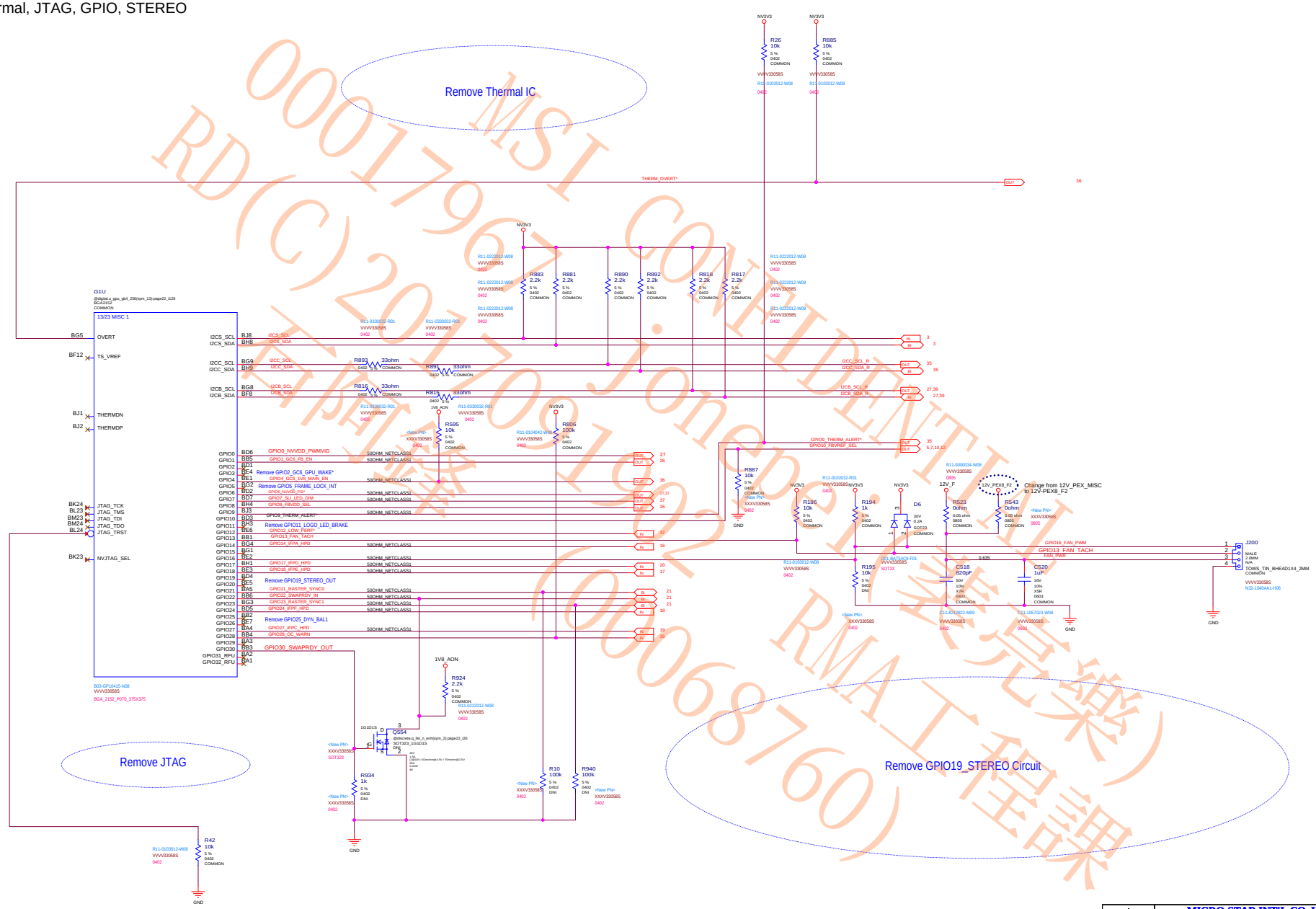
Page22: MISC1: Fan, Thermal, JTAG, GPIO, STEREO



Page23: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	
L	H	L	00010	
L	H	H	00011	
H	H	L	00110	
H	H	H	00111	
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

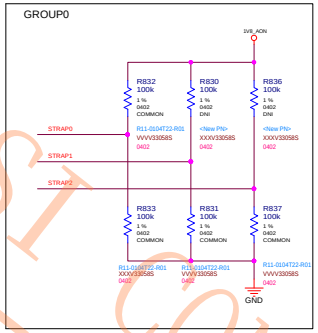
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

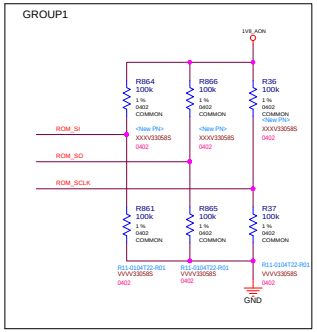
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

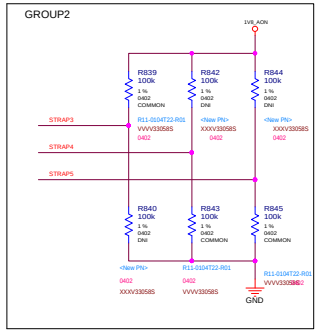
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

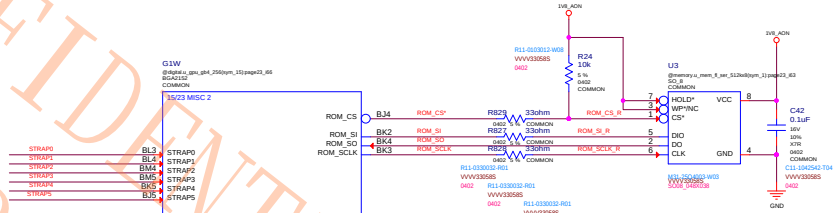
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

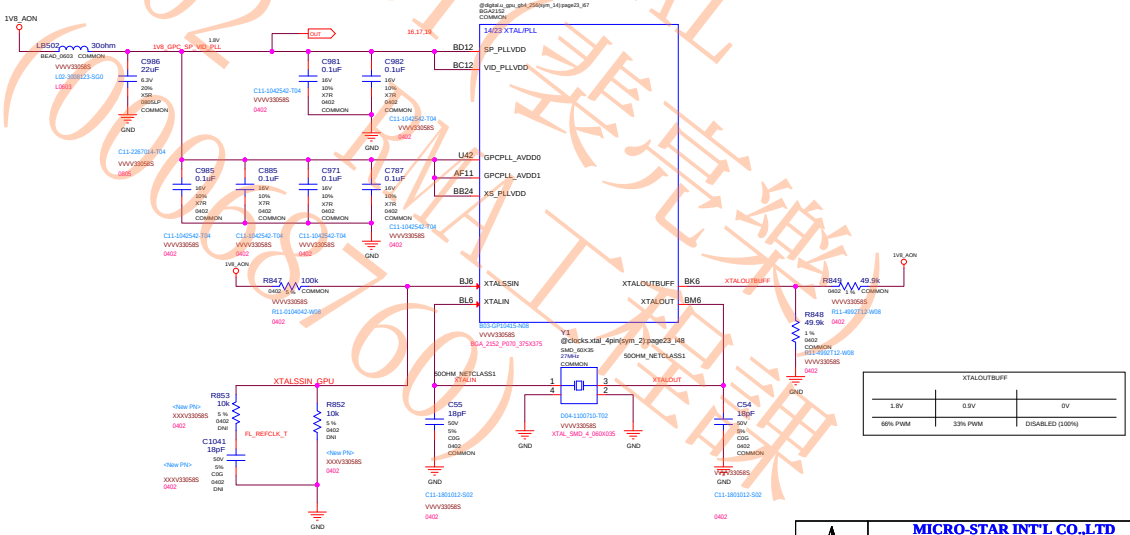






CFG[3:0]	Config Width	Vendor
0000	256Mx32 256-bit	Samsung
0001	256Mx32 256-bit	Micron
0010	256Mx32 256-bit	Hynix
0011	Reserved	
0100	Reserved	
0101	Reserved	
0110	Reserved	
0111	Reserved	





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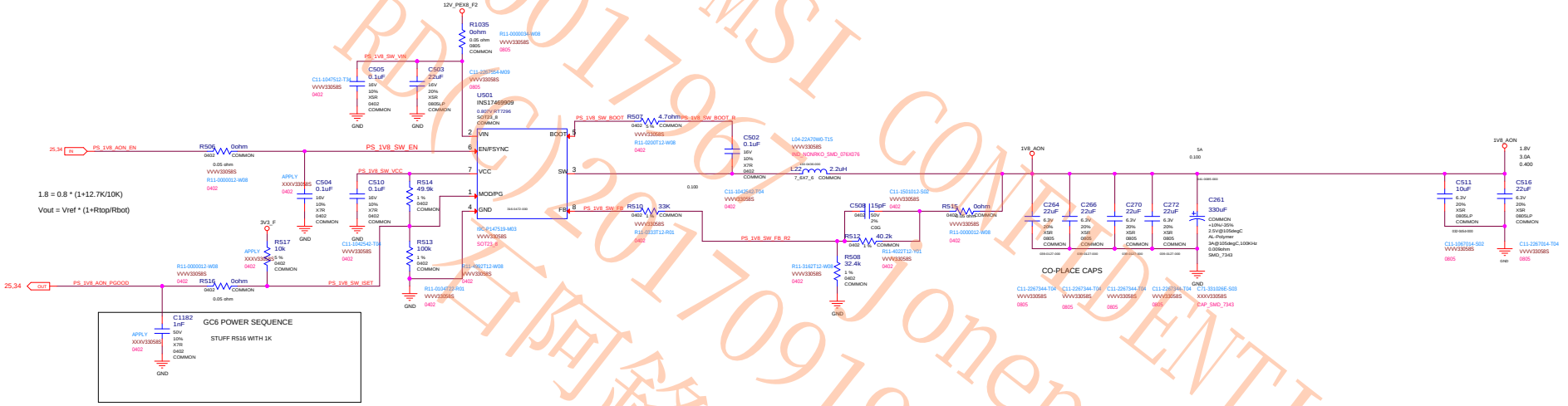
Page24: PS: 1V8, 1V8_AON



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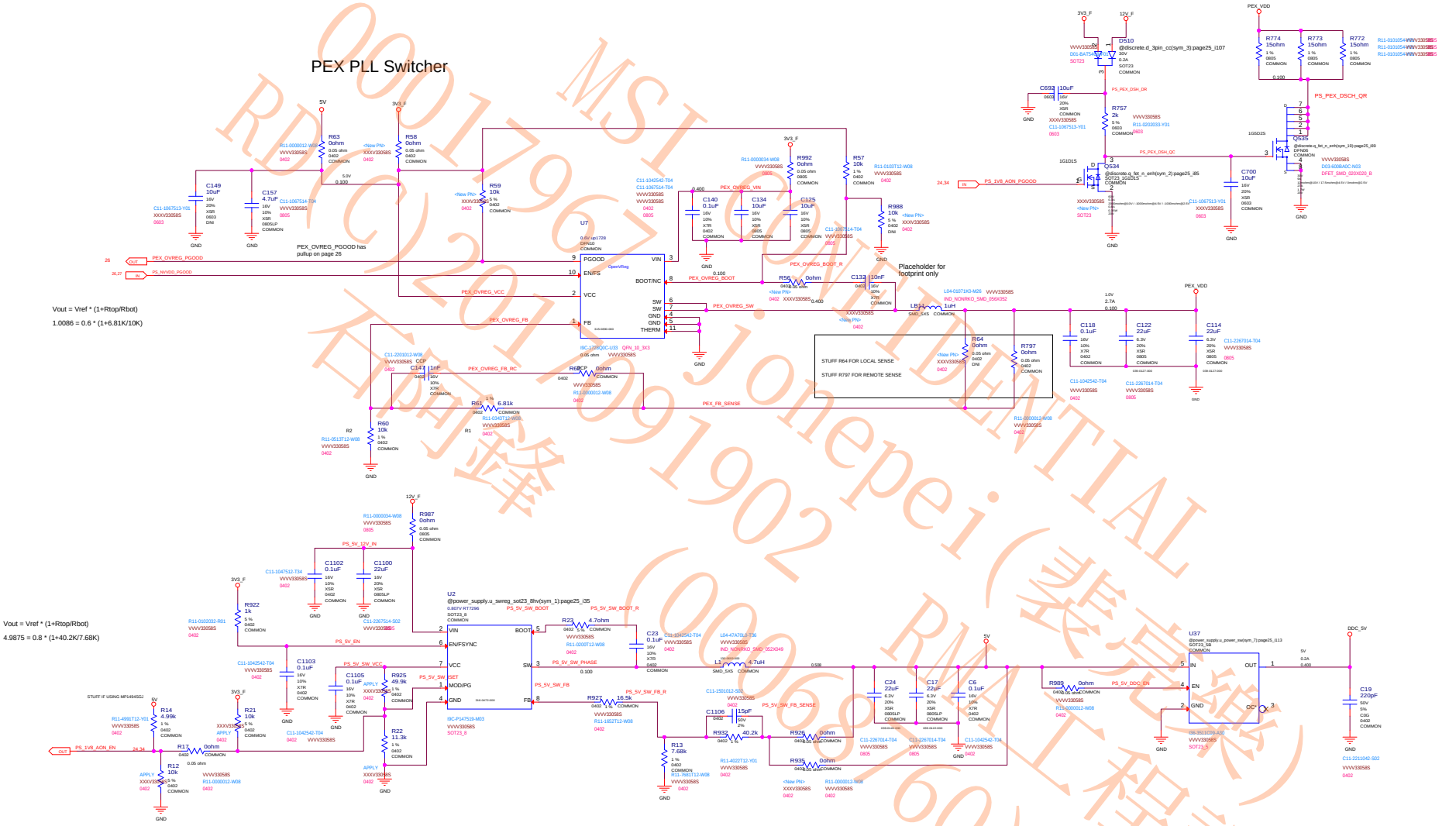

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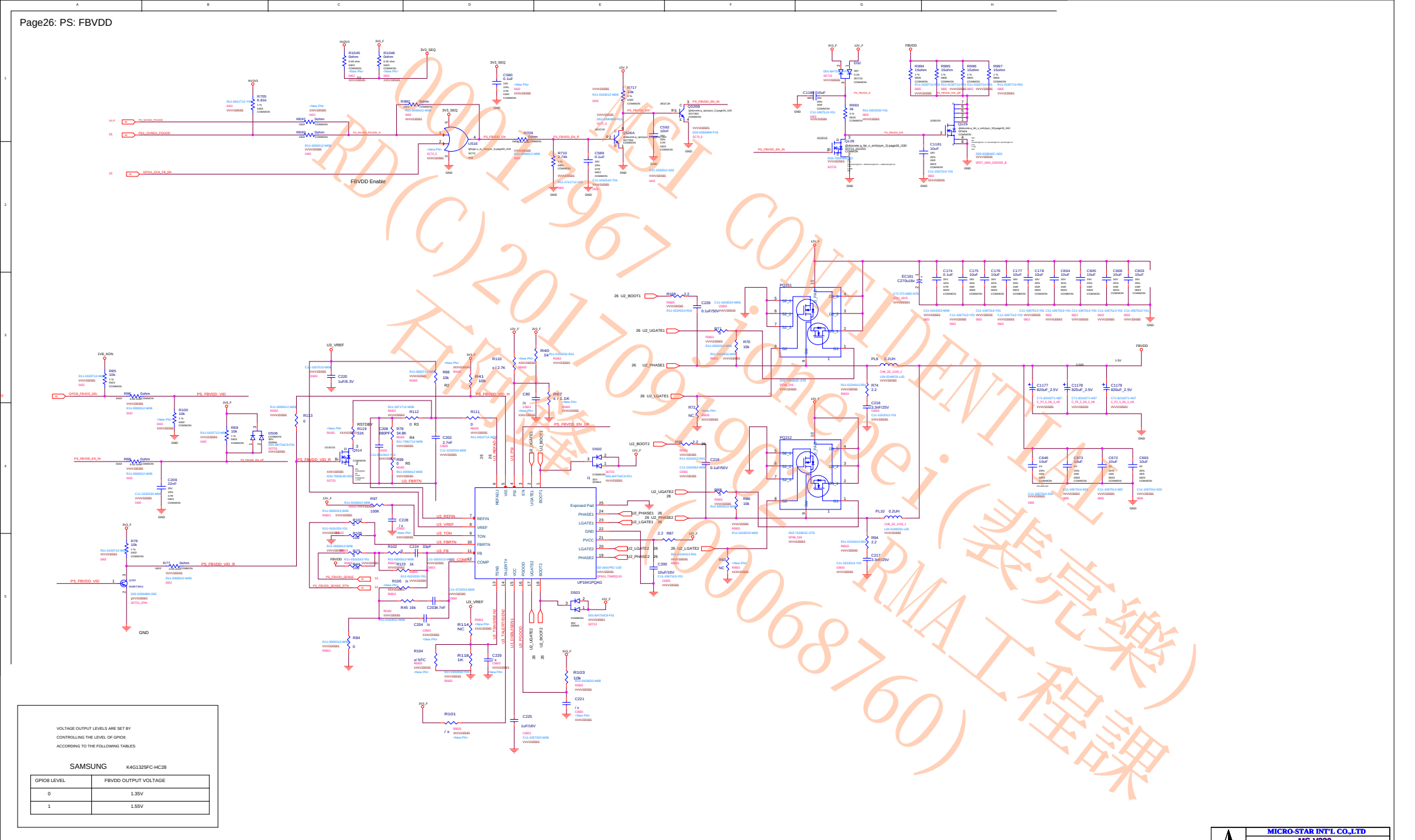

VOLTAGE OUTPUT LEVELS ARE SET BY
CONTROLLING THE LEVEL OF GPIO8
ACCORDING TO THE FOLLOWING TABLES:

SAMSUNG K4G1325FC-HC28

GPIO8 LEVEL	FBVDD OUTPUT VOLTAGE
0	1.35V
1	1.55V

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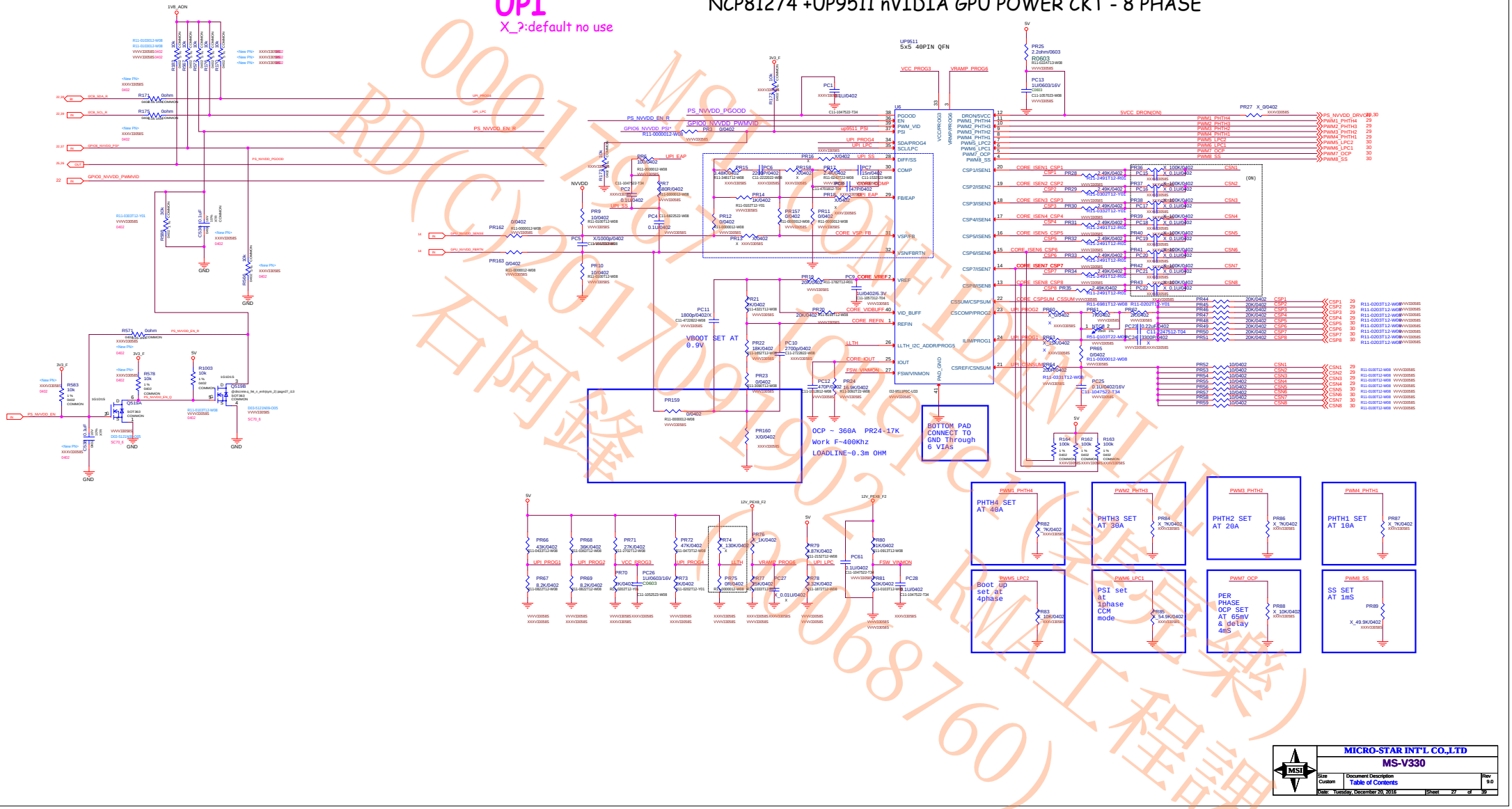
UPI

X_?:default no use

NCP81274 +UP9511 nVIDIA GPU POWER CKT - 8 PHASE



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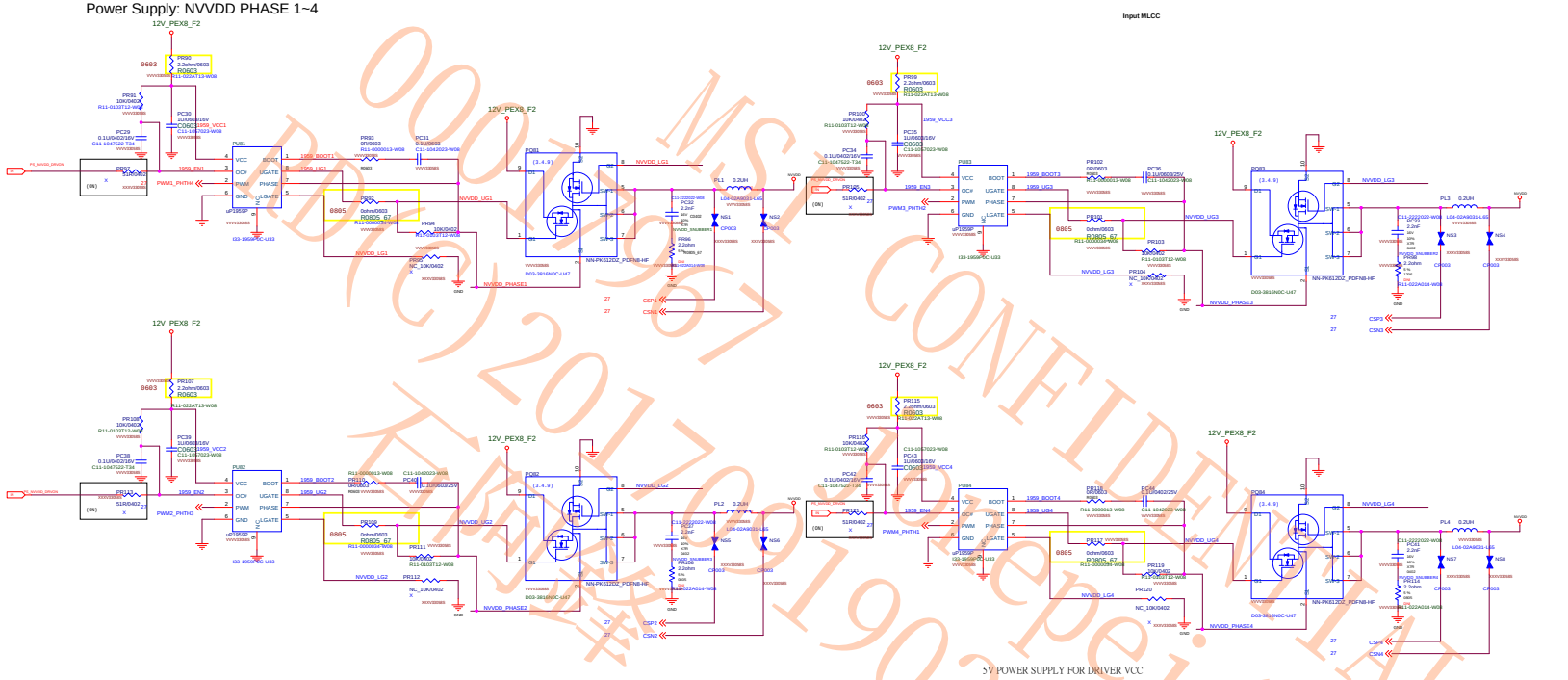
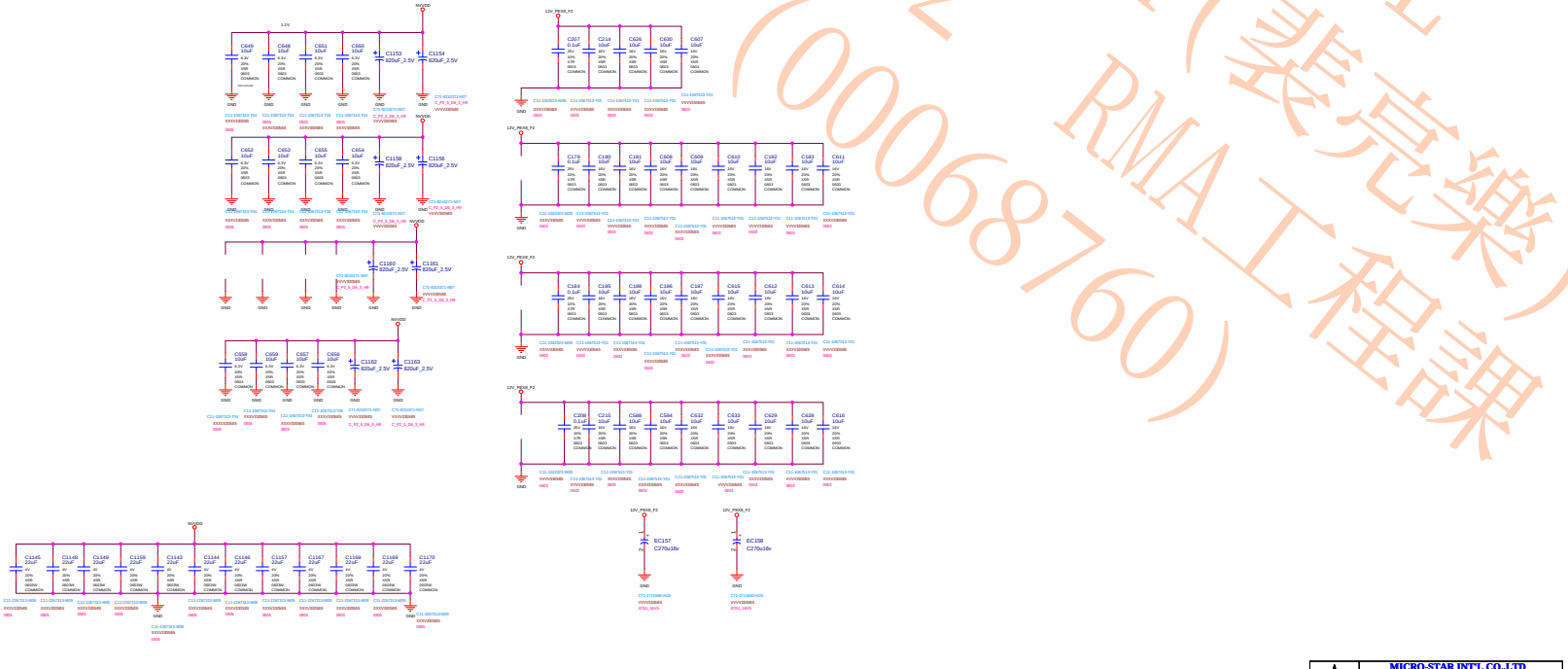
Power Supply: NVVDD PHASE 1~4



5V POWER SUPPLY FOR DRIVER VCC



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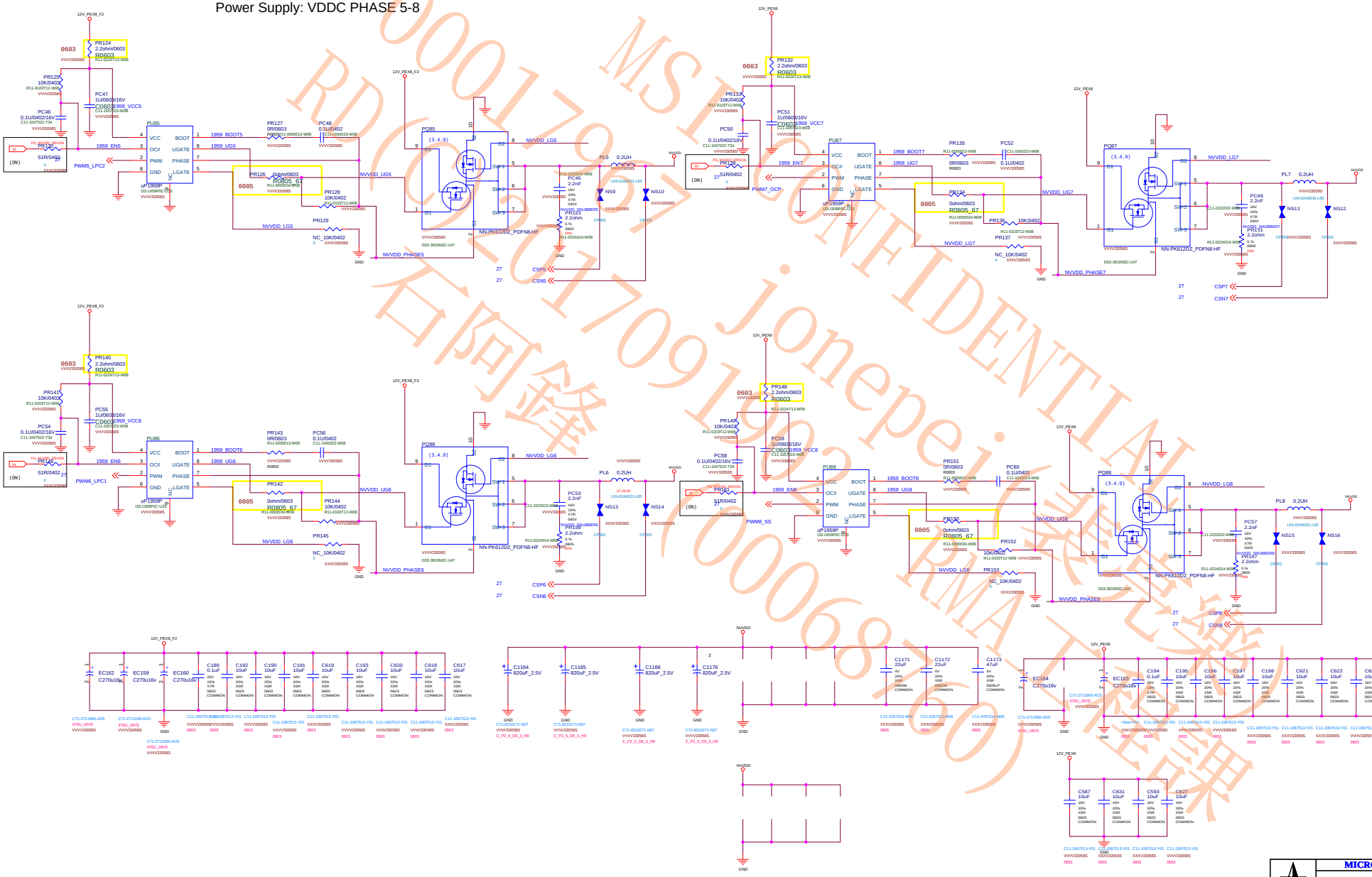
Page30: PS: NVVDD Phase 5 ~8

Power Supply: VDDC PHASE 5-8



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Page31: PS: Blank Page

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Page32: PS: Dynamic Power Balance Phases

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Page33: PS: Dynamic Power Balance Logic

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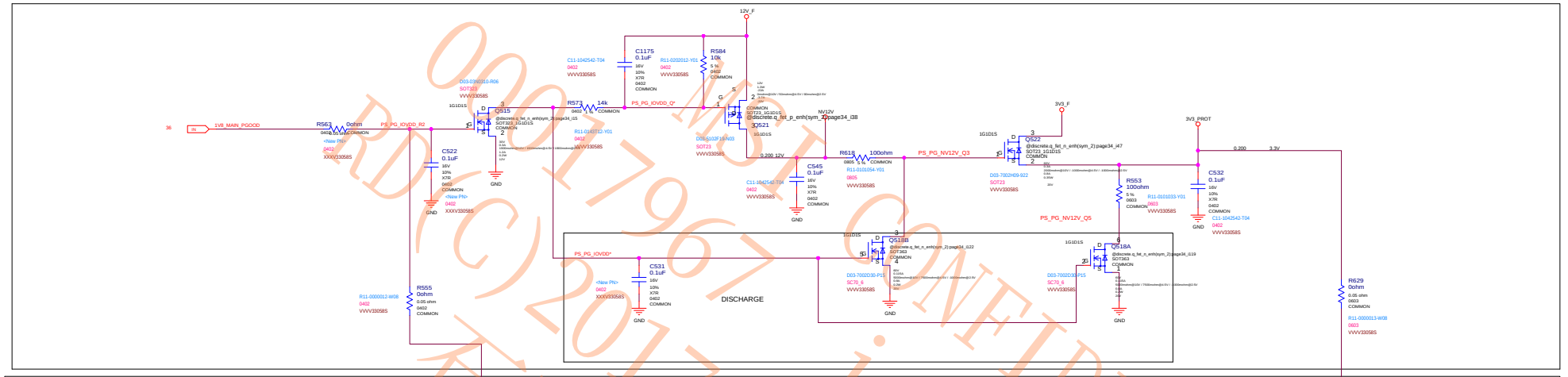
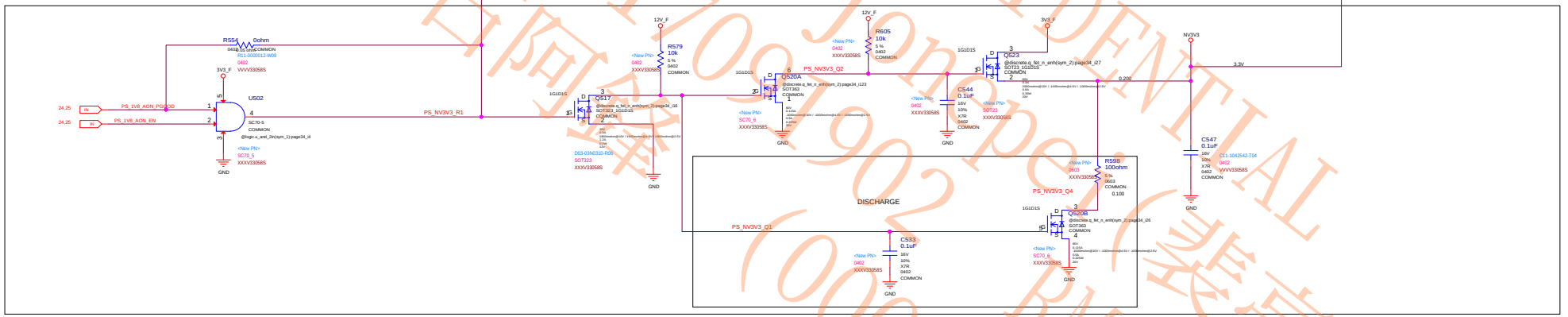
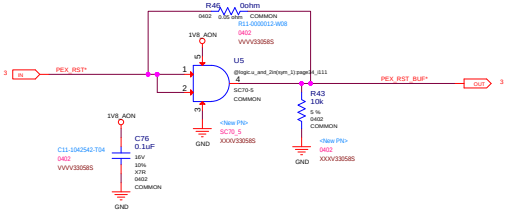
Page34:PS: NV3V3, NV12V







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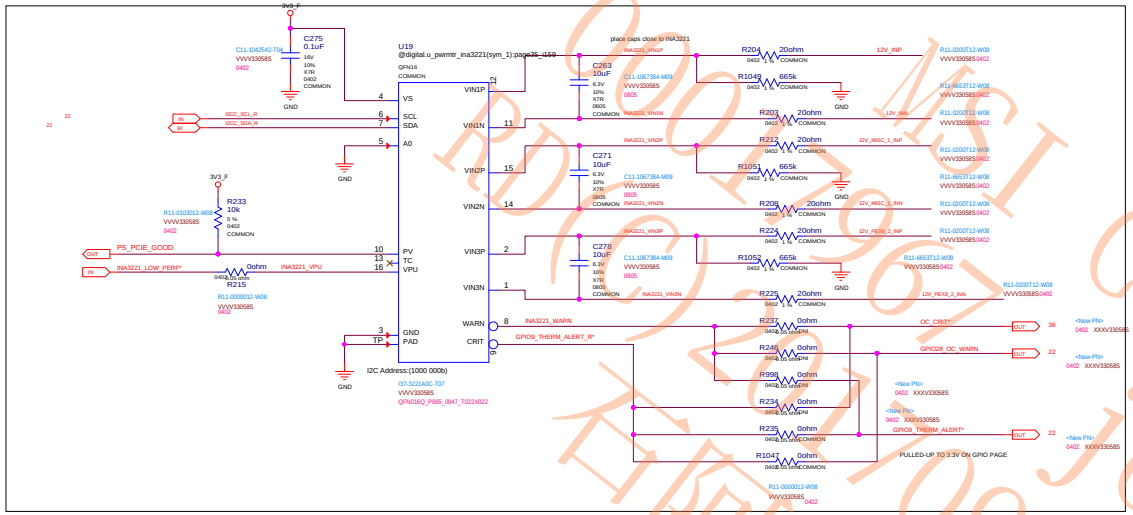
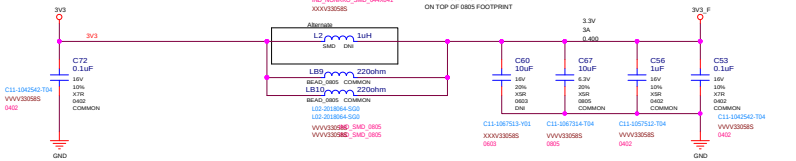
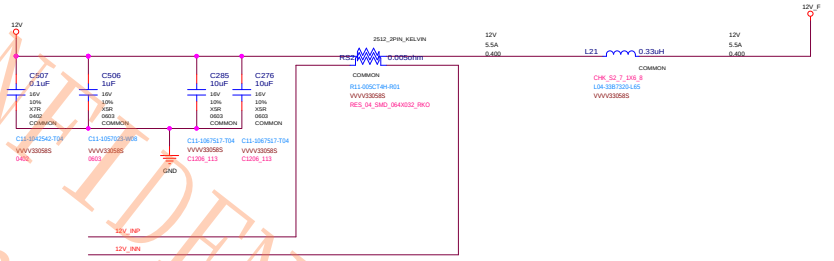
Page35: PS: Inputs, Filtering, and Monitoring



PEX 3V3 INPUT - 10W

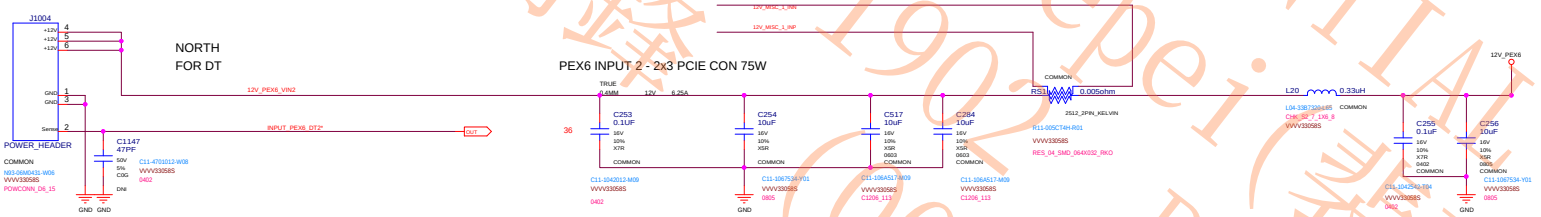


PEX_12V INPUT - 66W

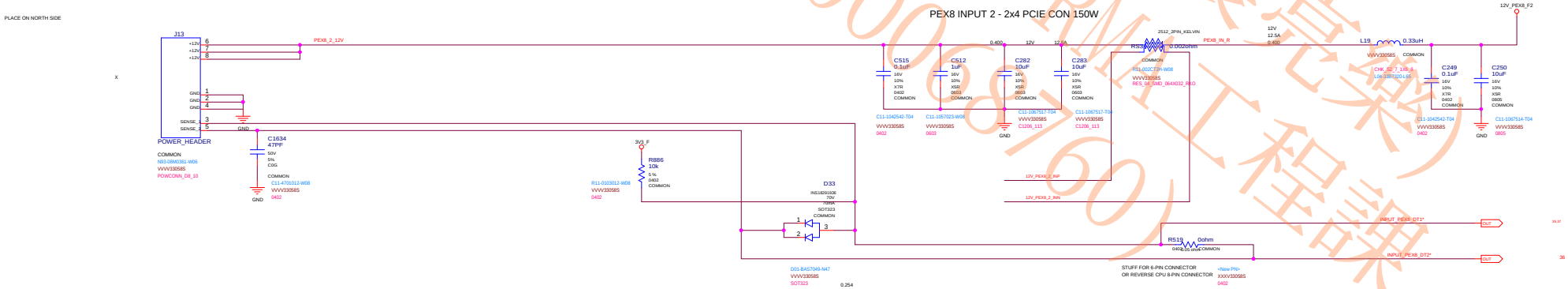


NORTH FOR DT

PEX6 INPUT 2 - 2x3 PCIE CON 75W



PEX8 INPUT 2 - 2x4 PCIE CON 150W



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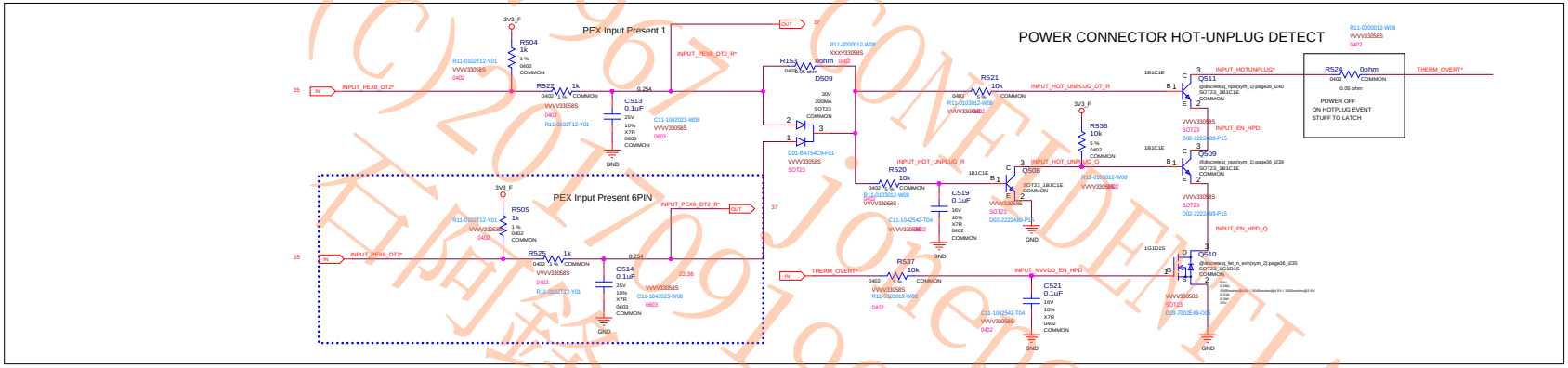
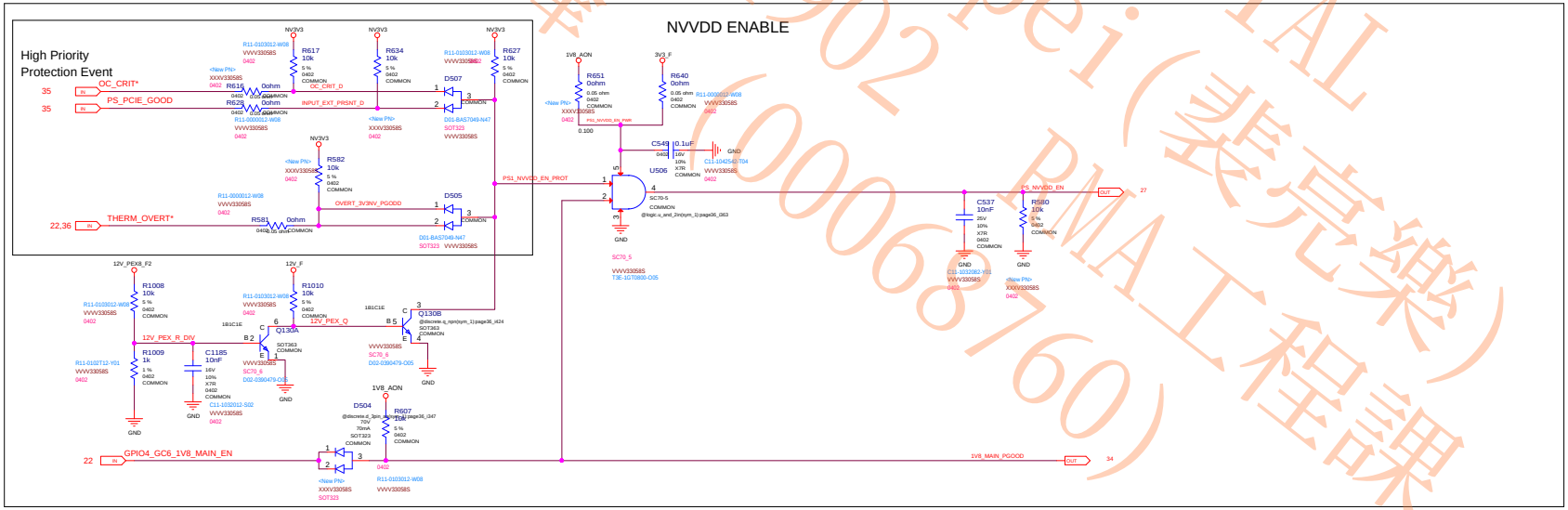
Page36: PS: Shutdown and Sequencing





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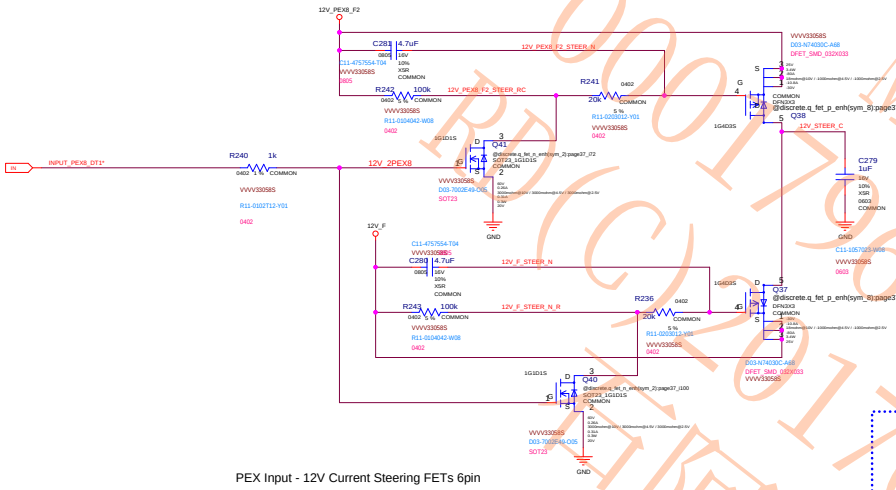
Page37: PS: 12V Current Steering, PSI Control, and LED

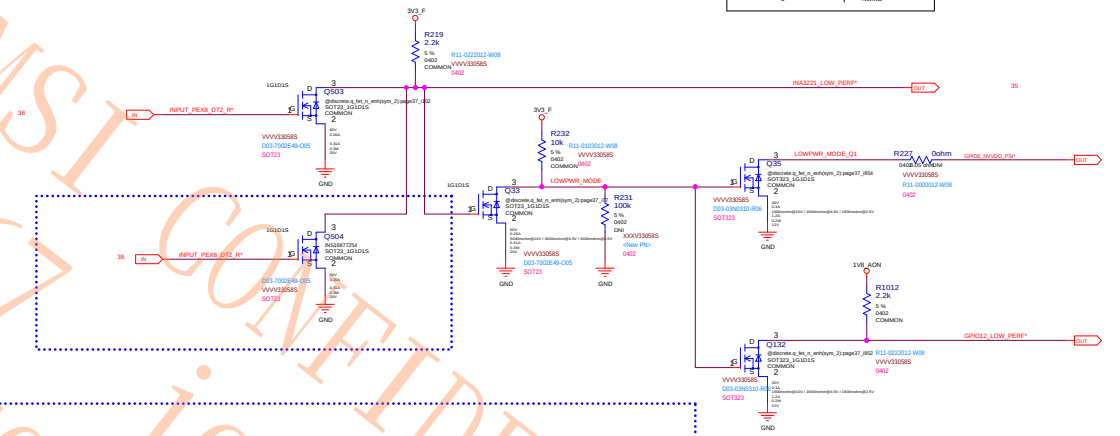
PEX Input - 12V Current Steering FETs 8pin



PEX Input - 12V Current Steering FETs 6pin

PEX Input - Power Level/PSI* Control

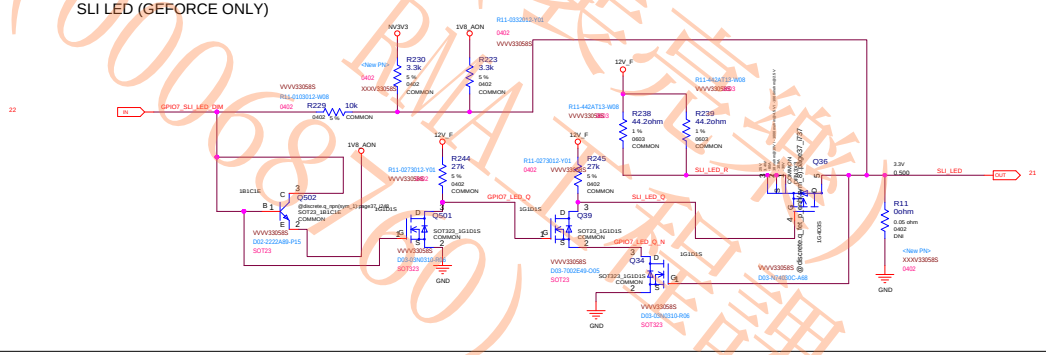
GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal



Remove POWER BRAKE

POWER BRAKE

SLI LED (GEFORCE ONLY)



GeForce Logo LED

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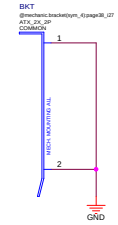
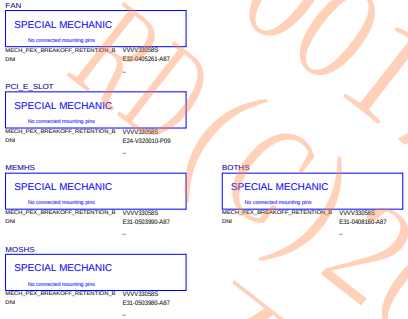
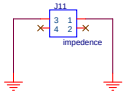
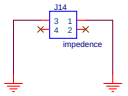
Page38: Mechanical: Bracket/Thermal Solution

Brackets:

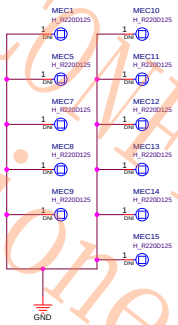




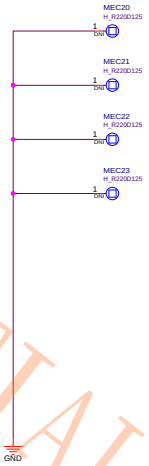


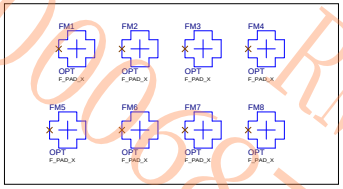


Mechanical Holes Symbol



GPU Stiffner





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