PG611 A00

12GB GDDR5X, 384b, 256Mx32
TALL DVI-D + DP + DP + HDMI/DP + DP

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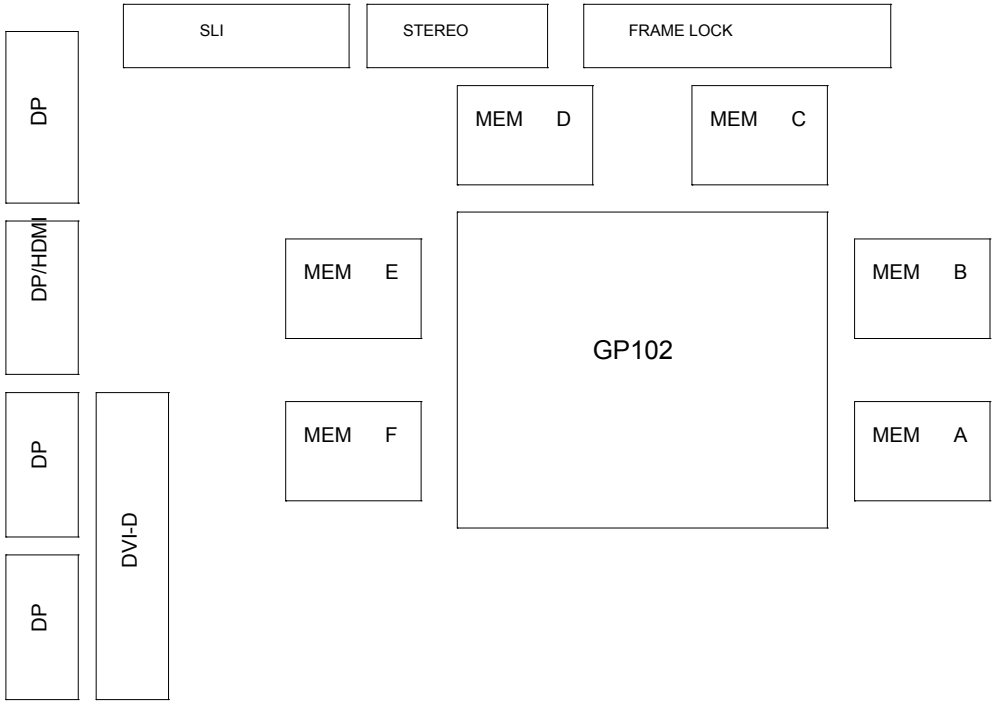

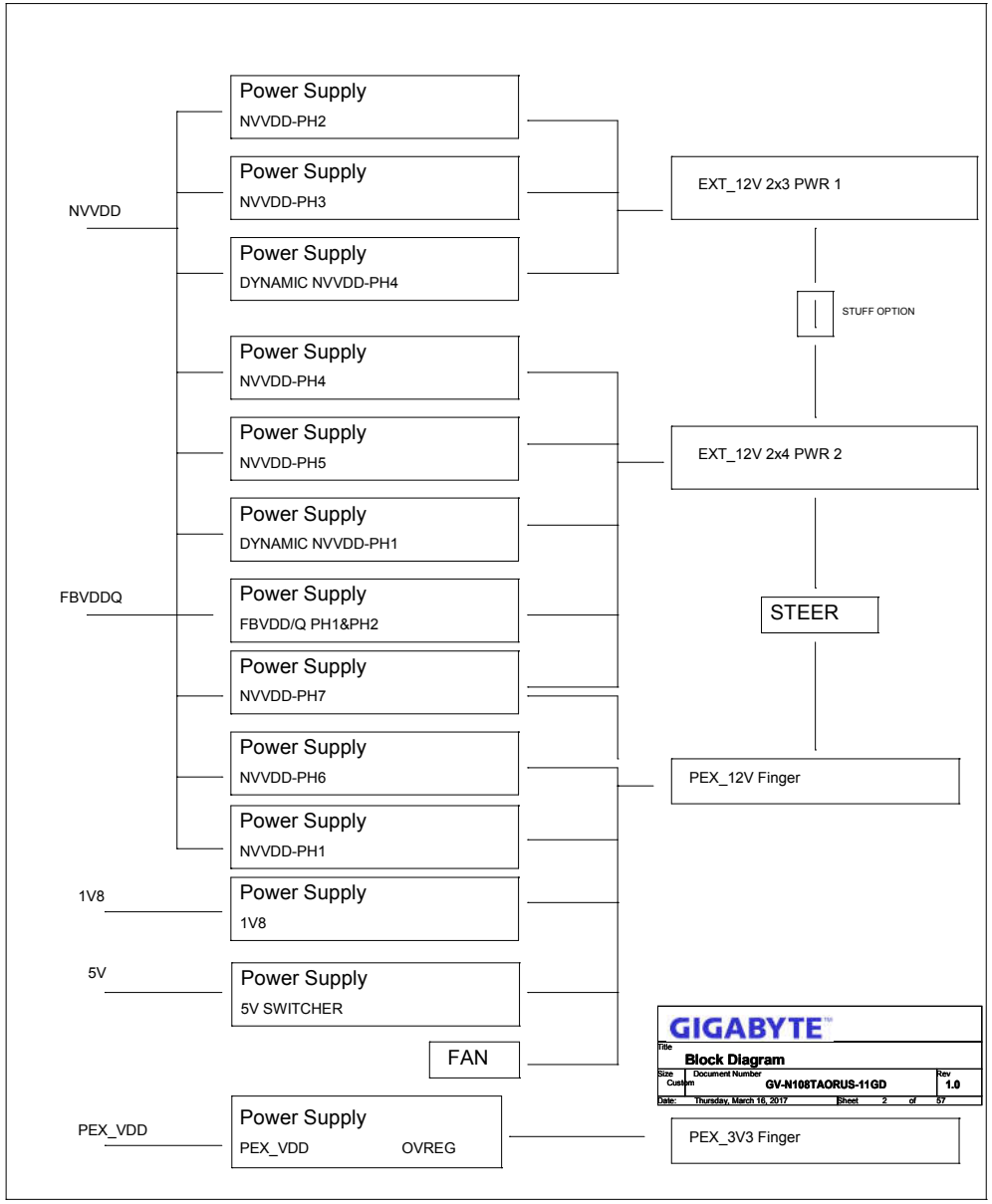

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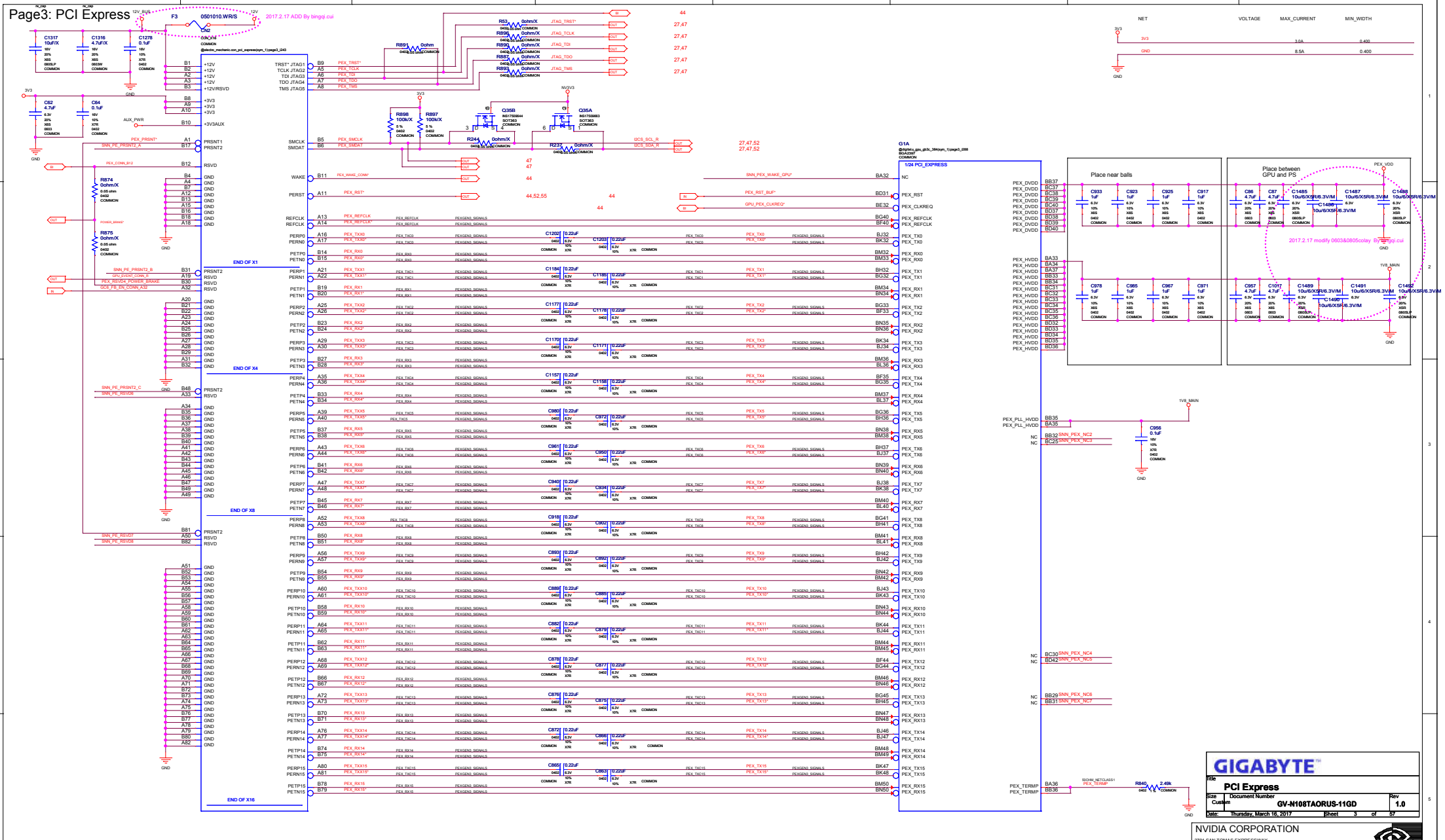

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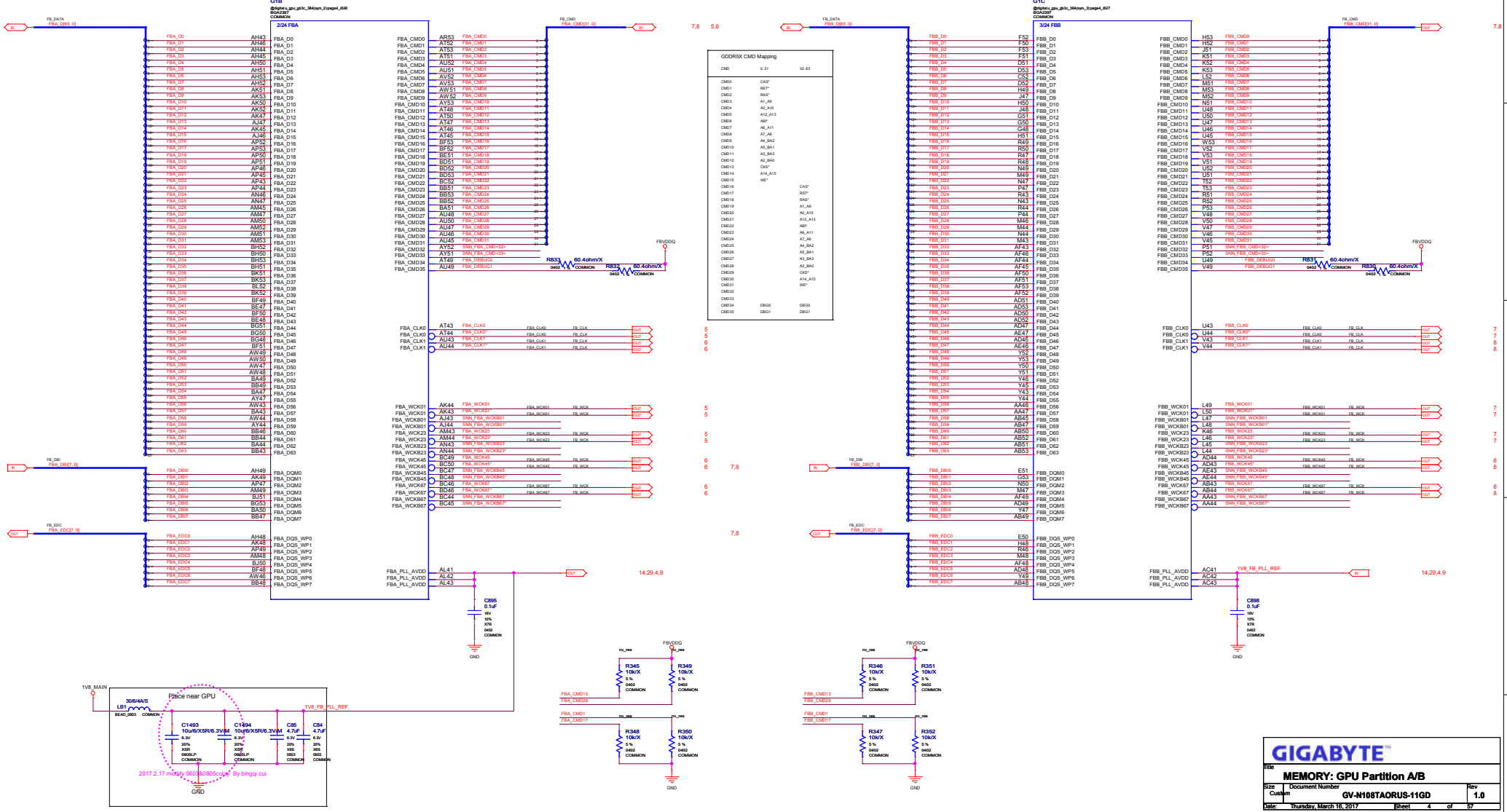

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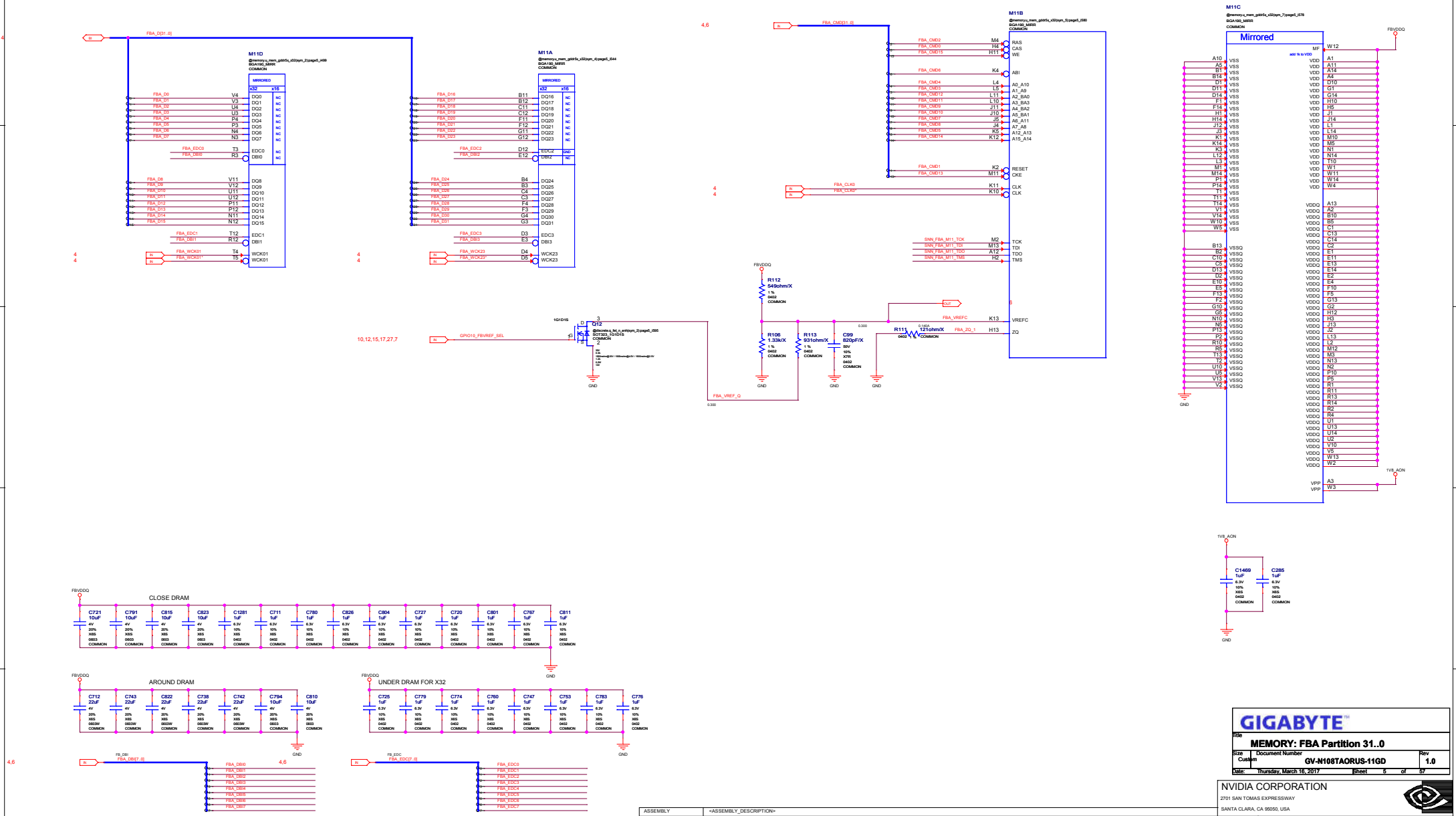

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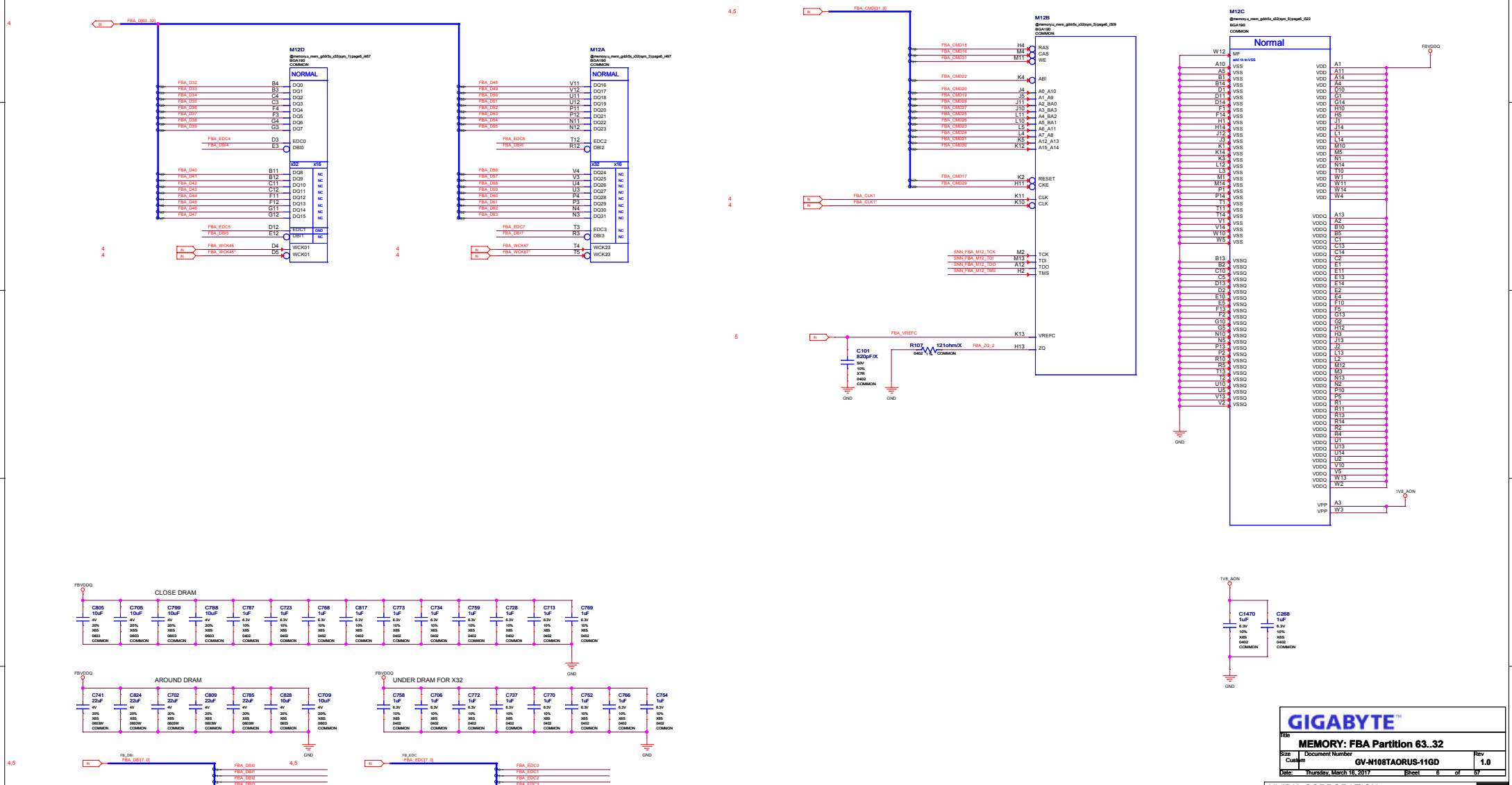

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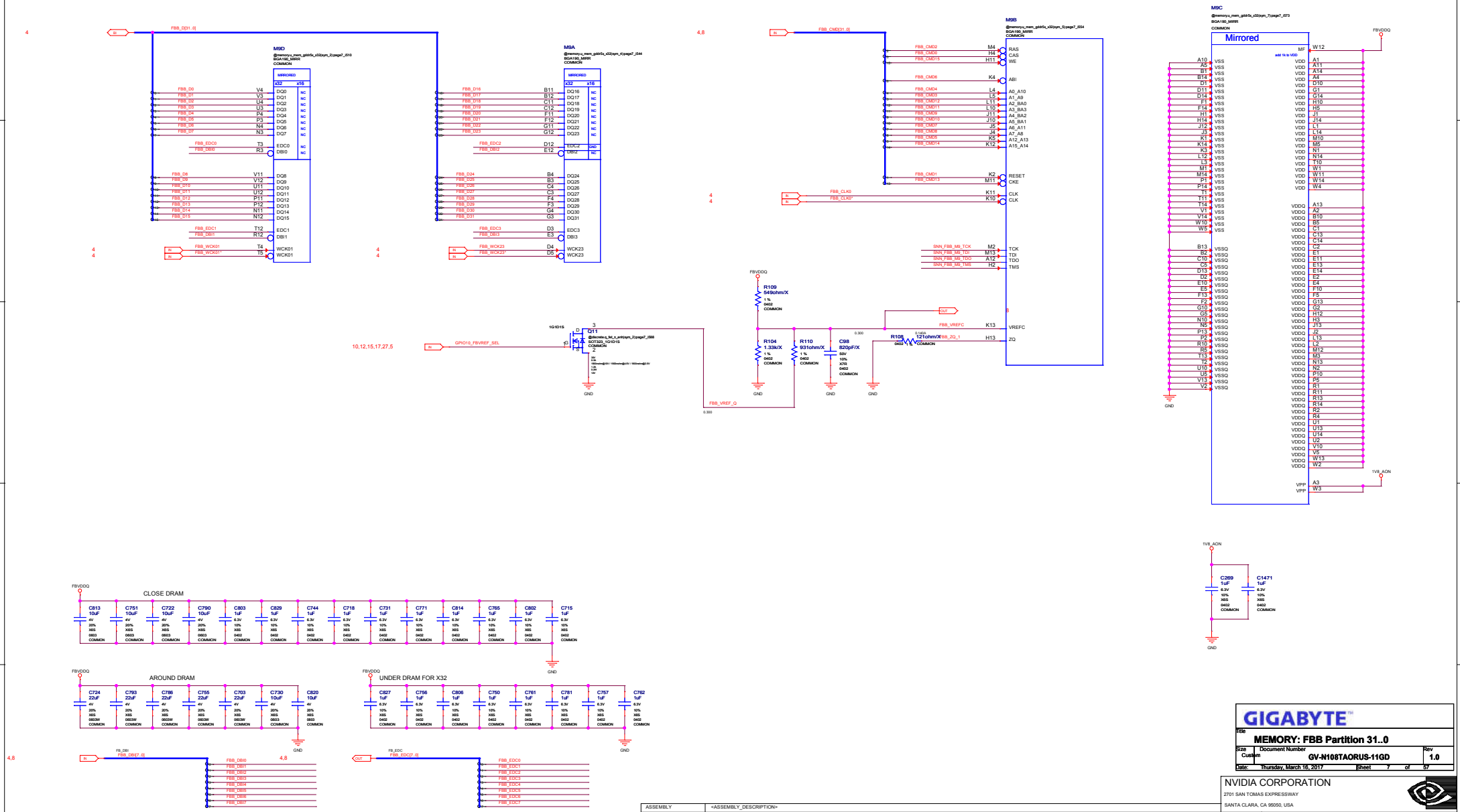

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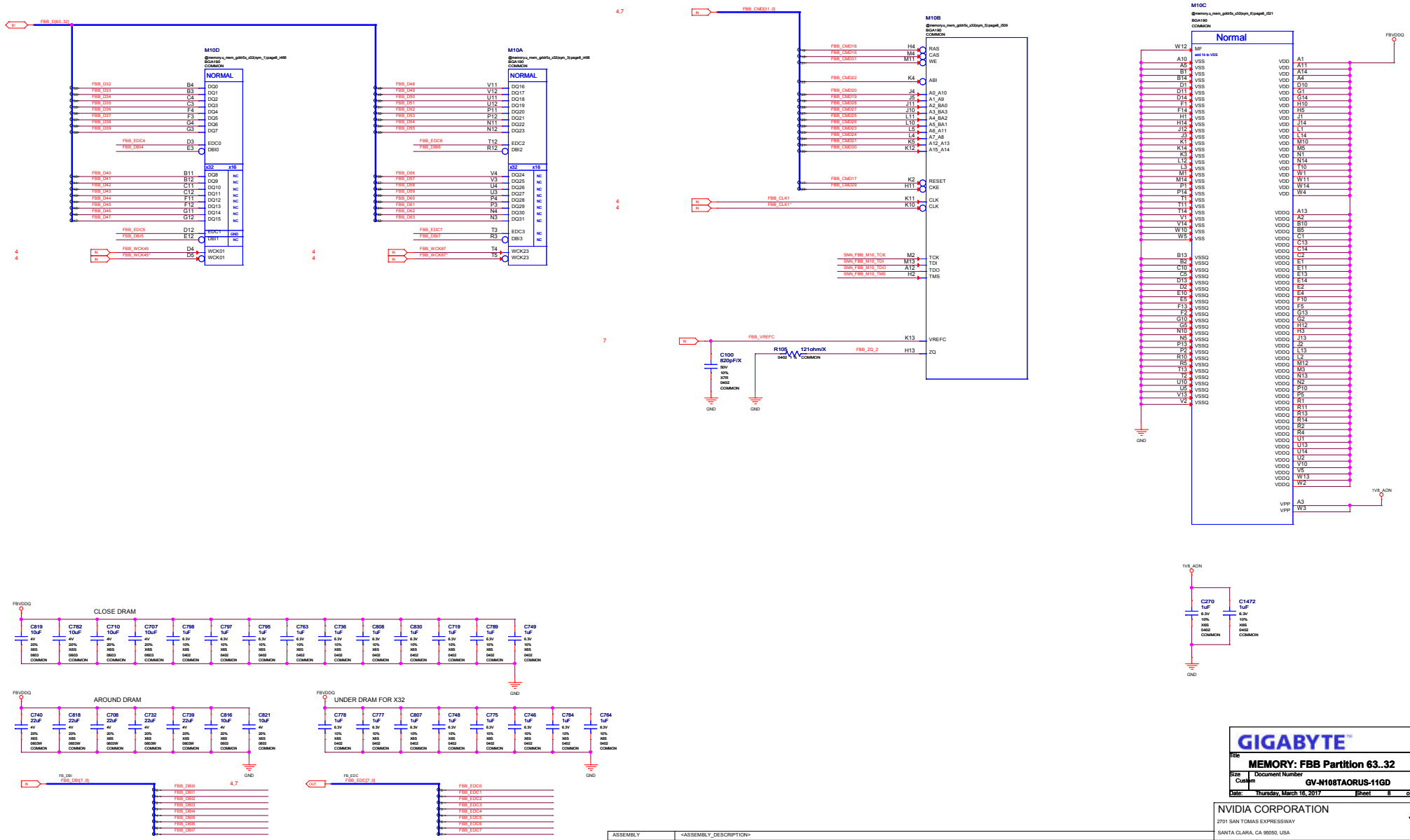

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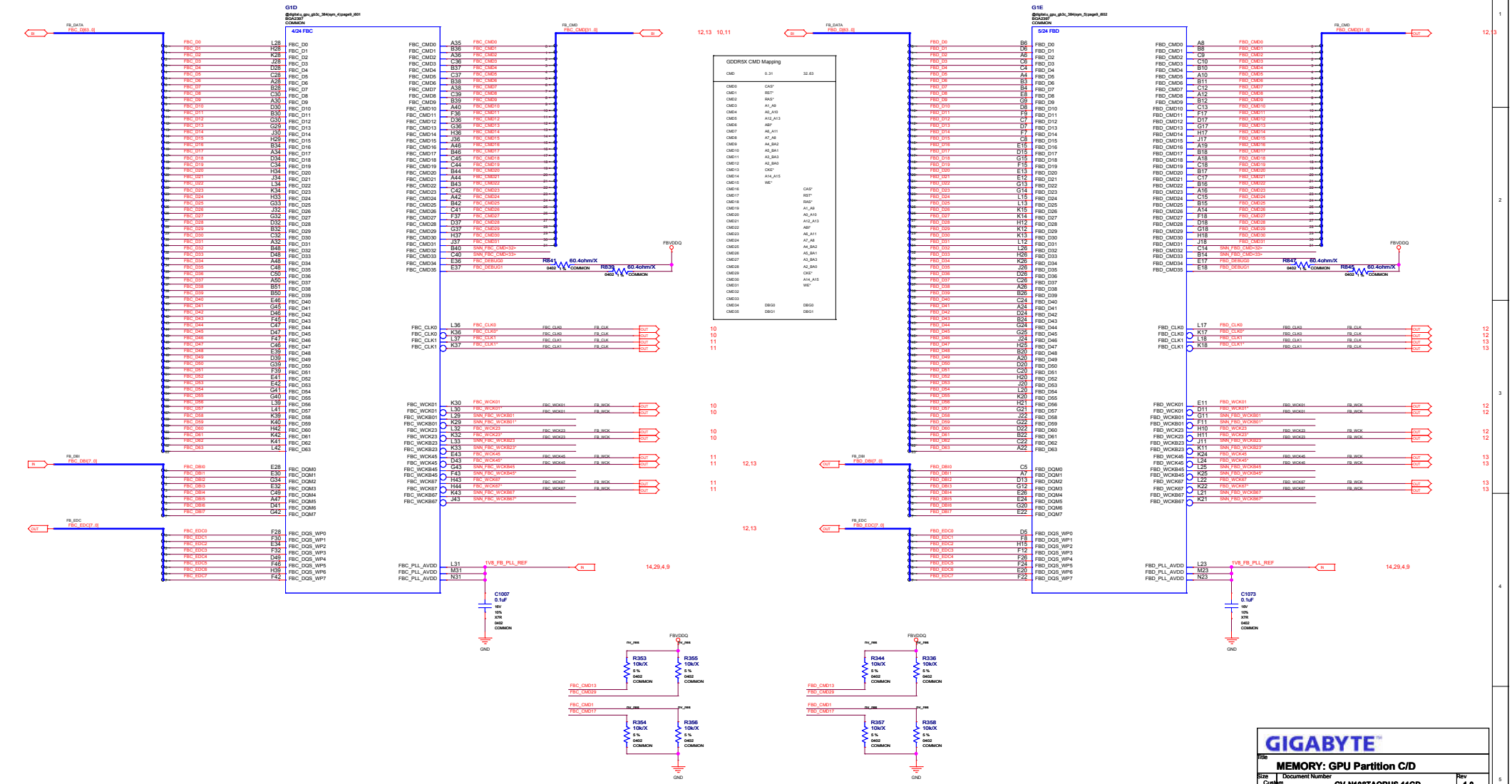

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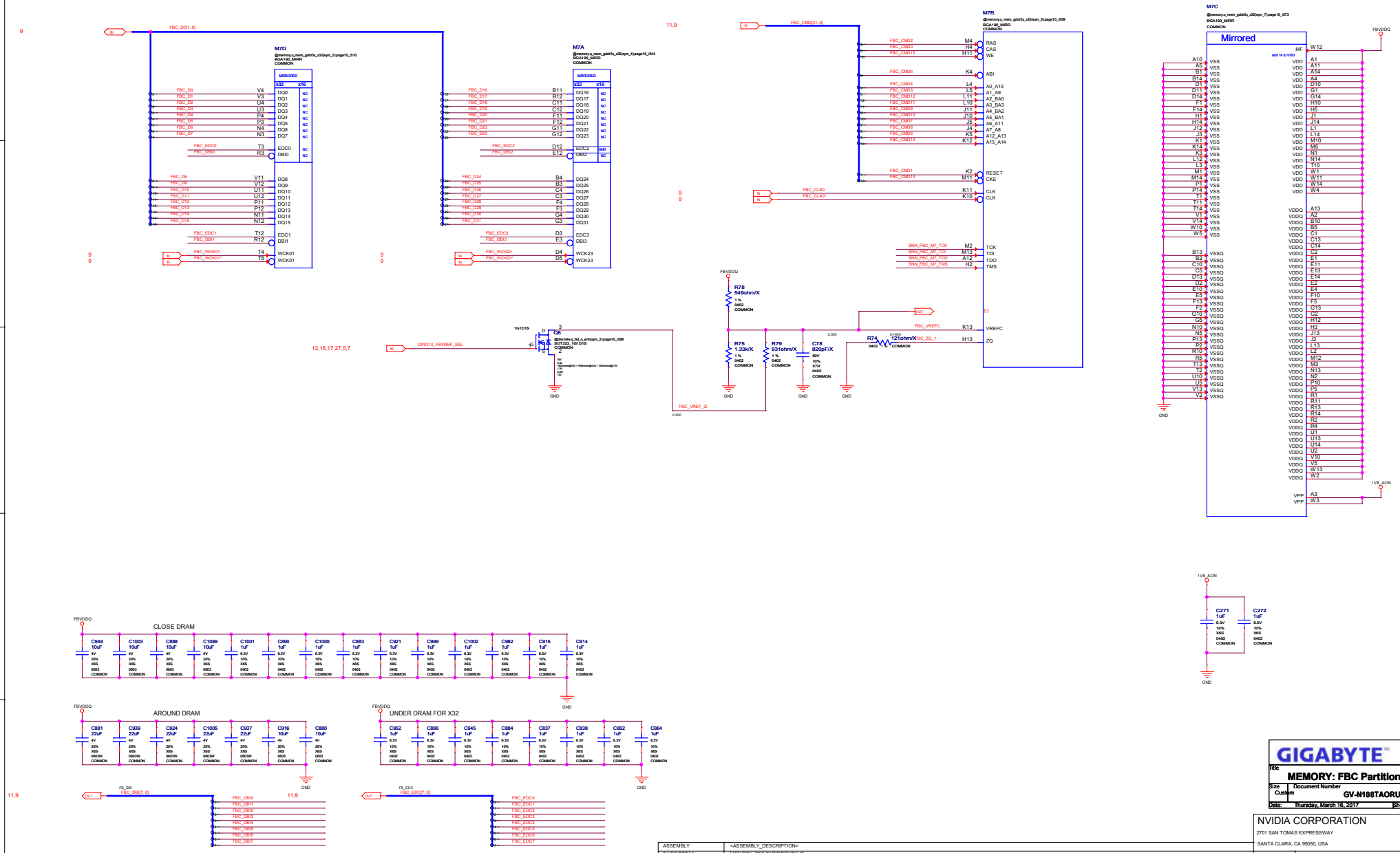

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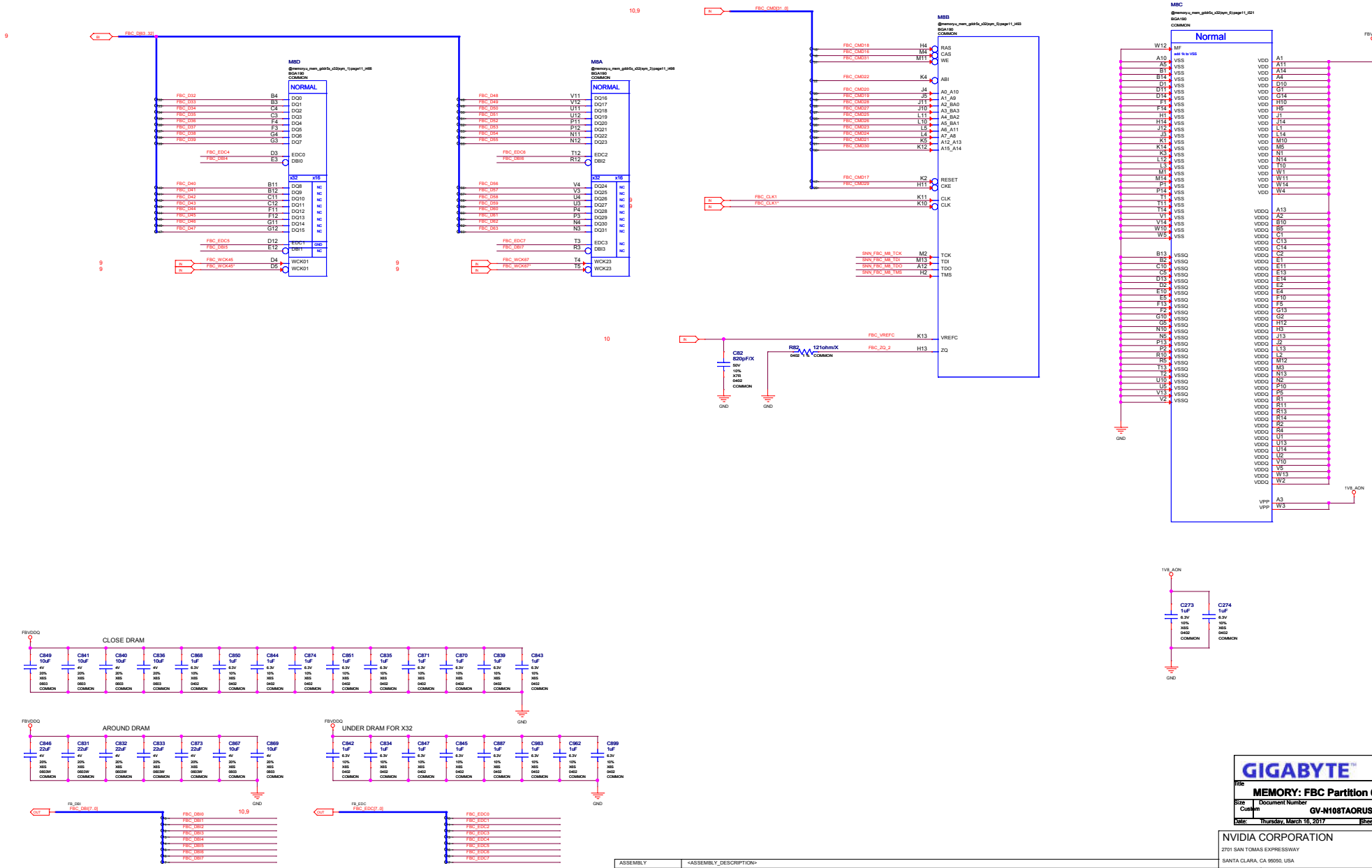

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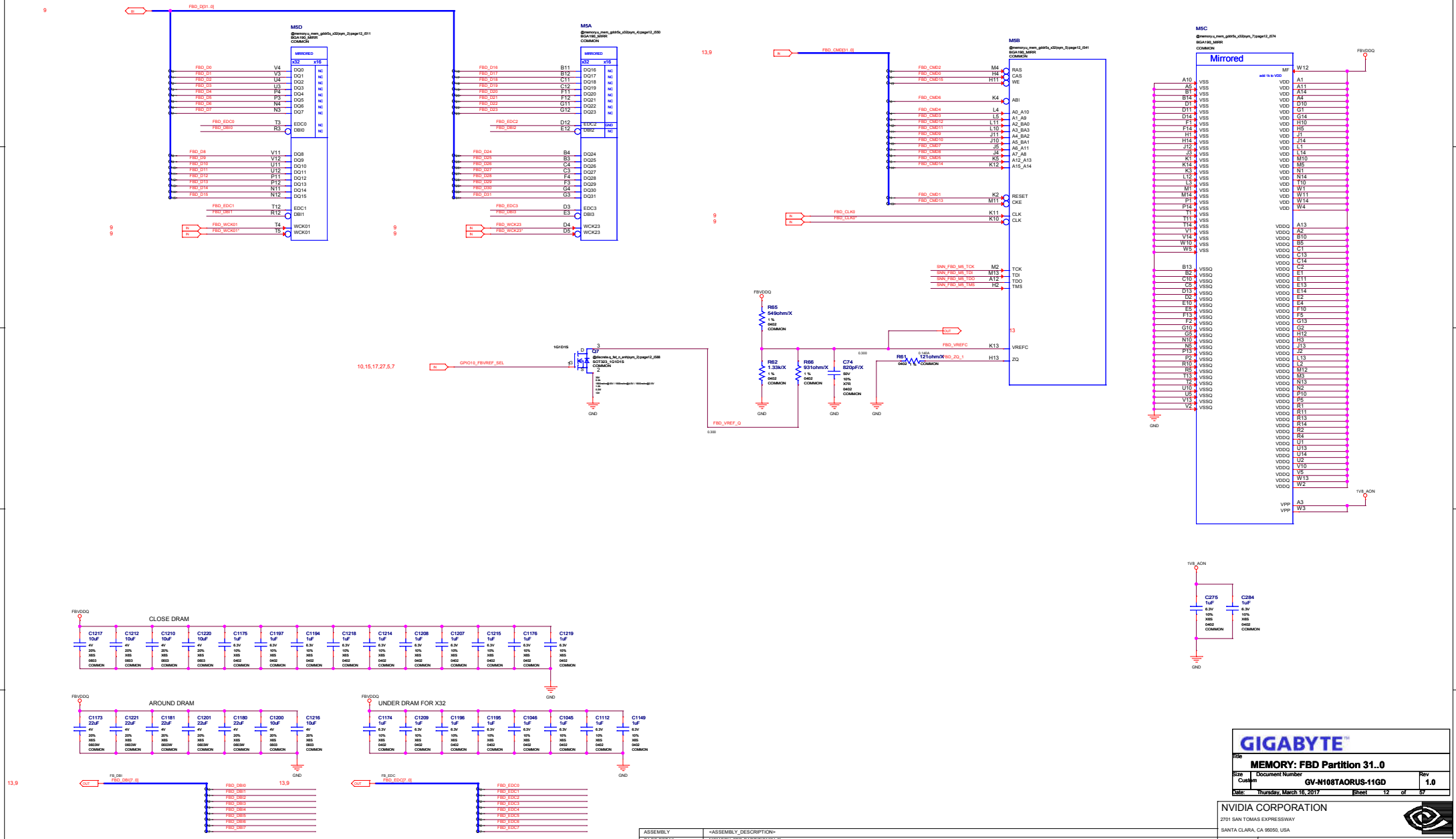

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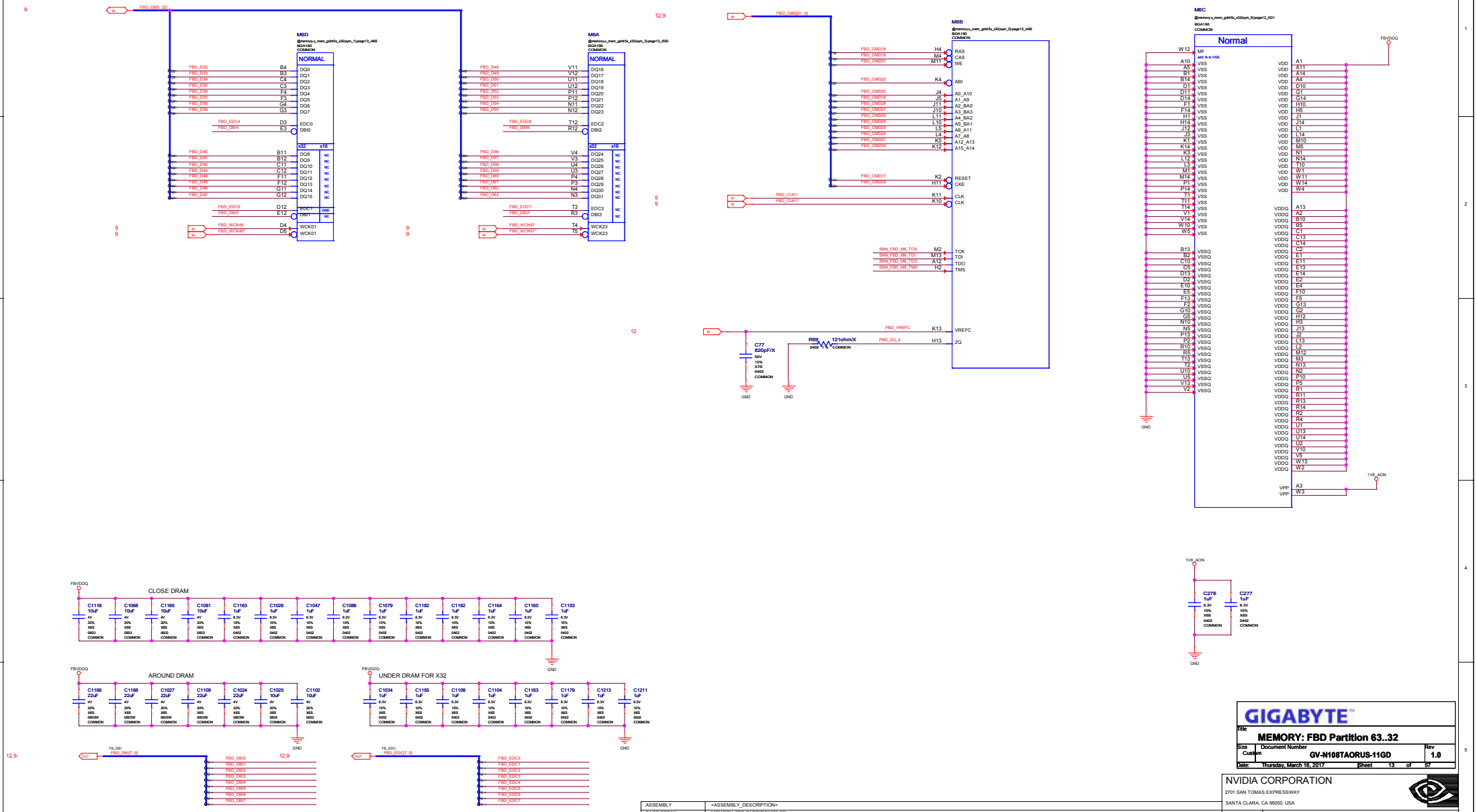

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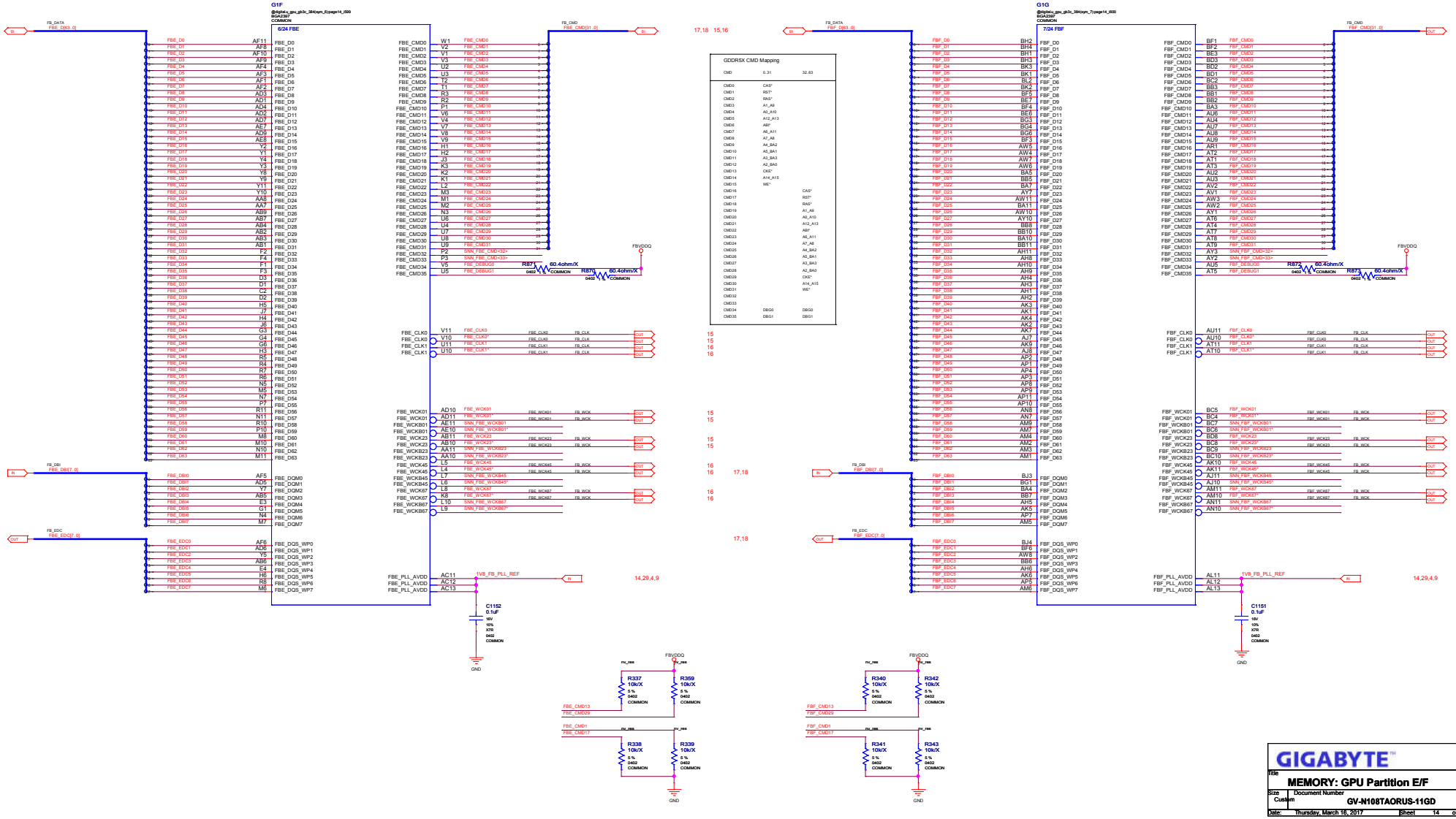

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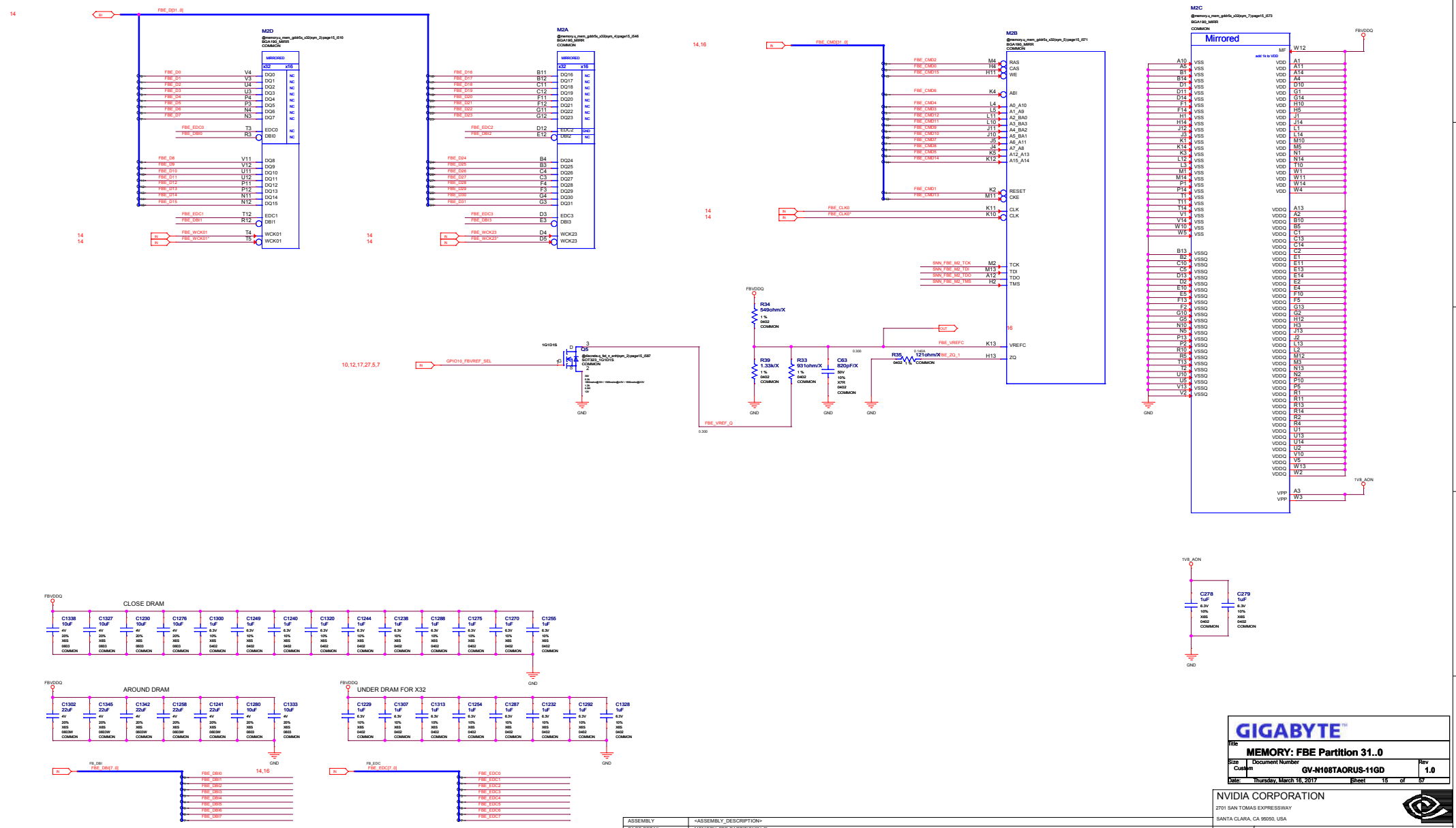
Page15: MEMORY: FBE Partition 31..0



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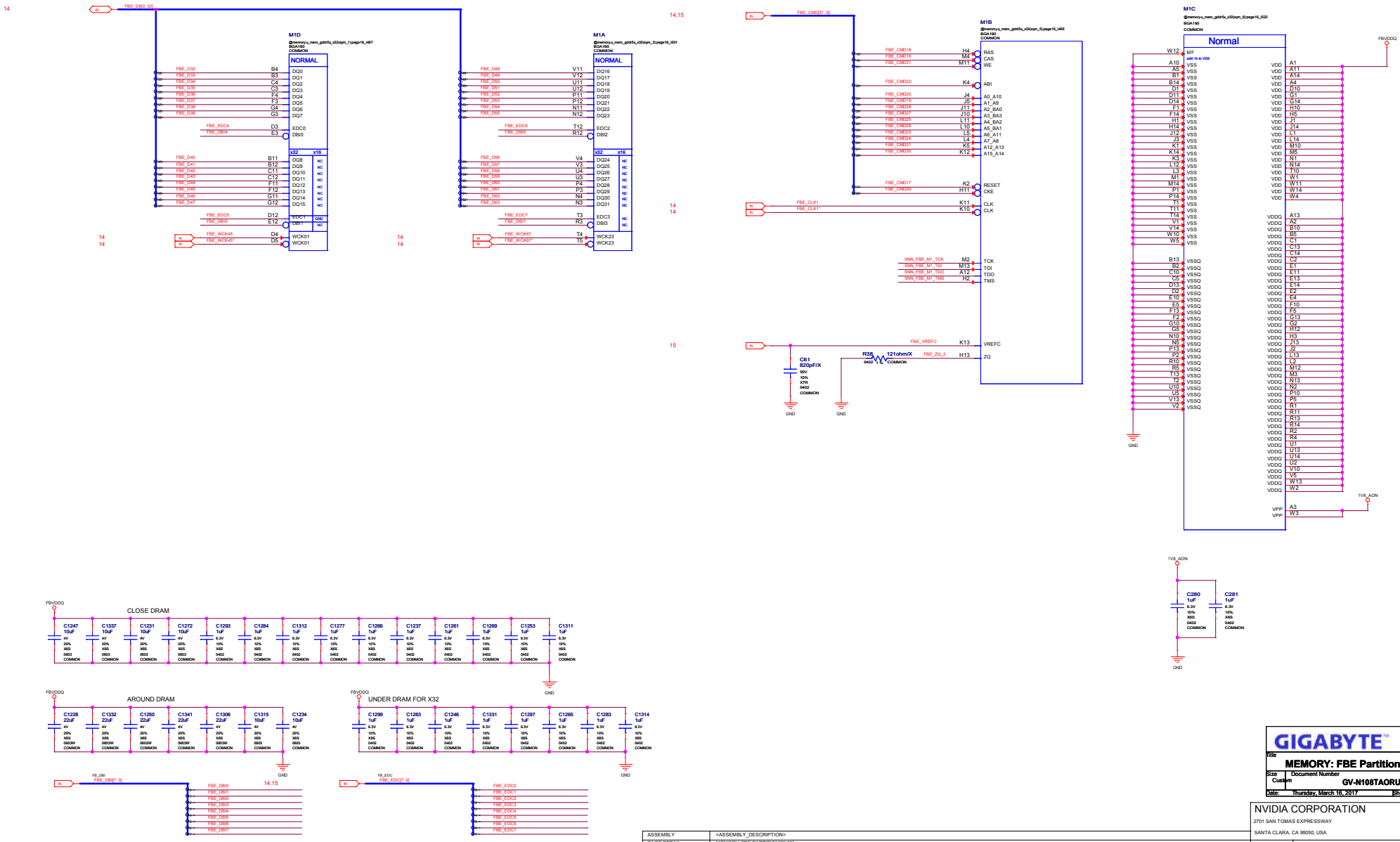
Page16: MEMORY: FBE Partition 63..32



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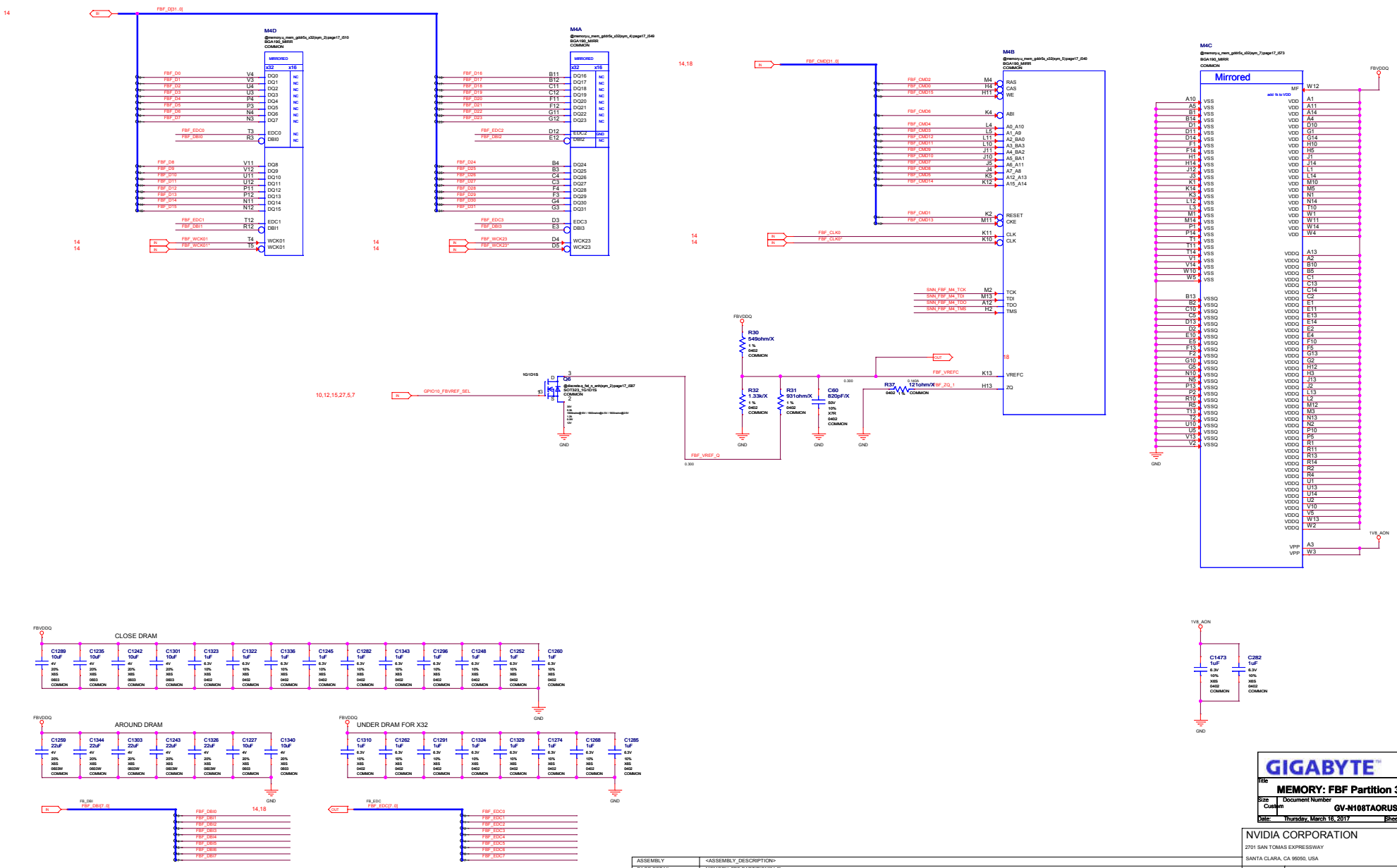
Page17: MEMORY: FBF Partition 31..0



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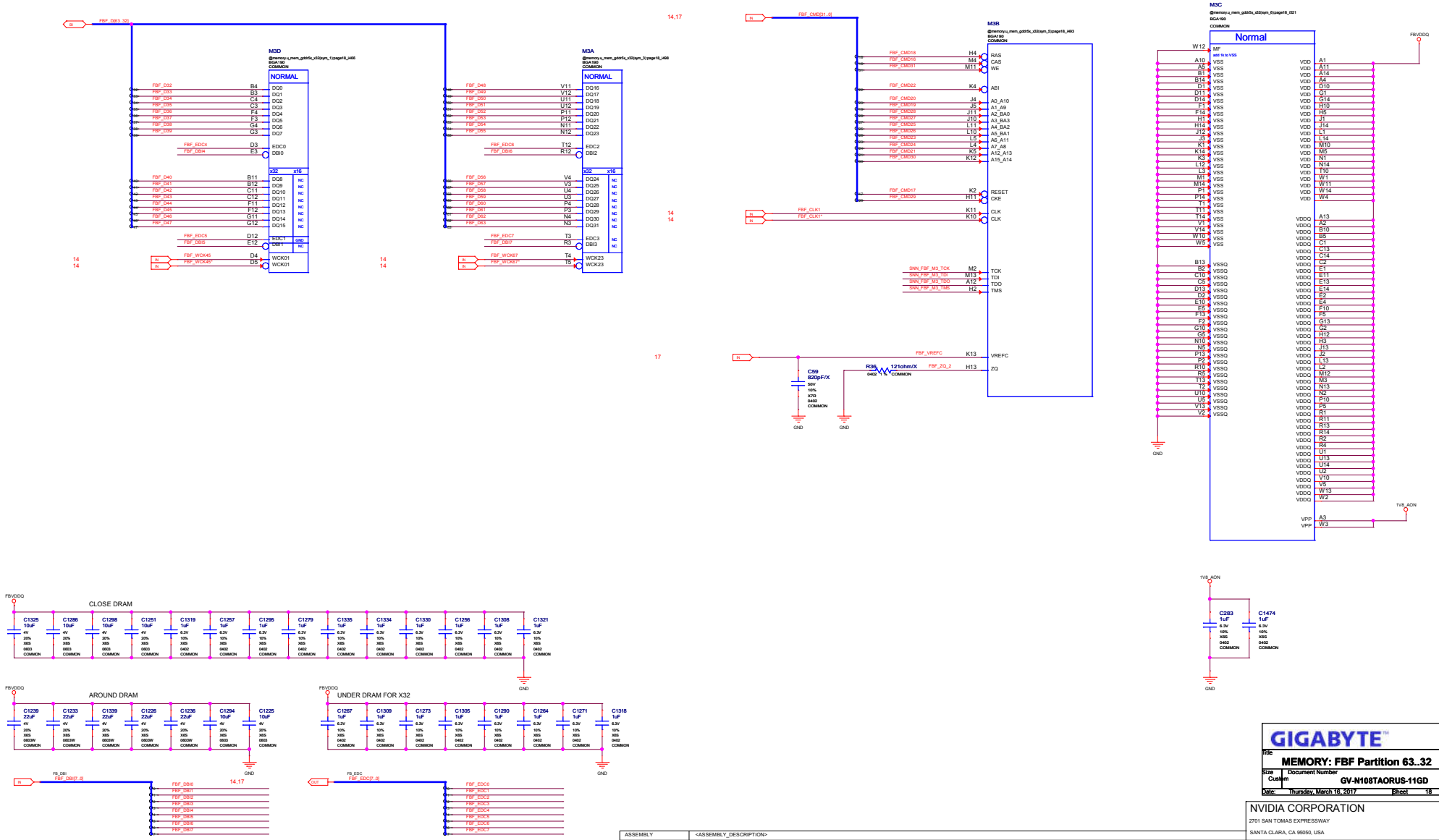
Page18: MEMORY: FBF Partition 63..32



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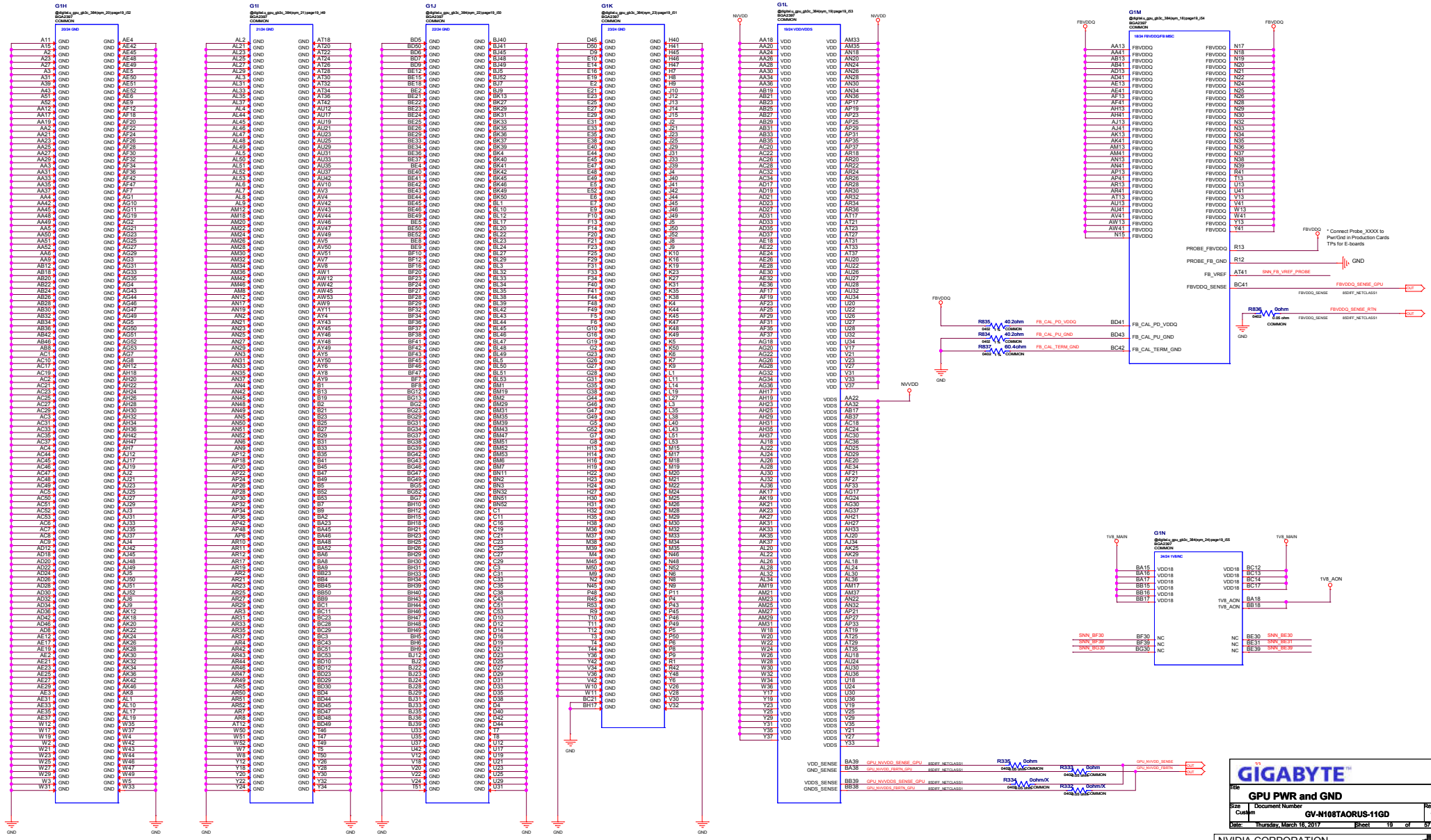
Page19: GPU PWR and GND



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PAGE DETAIL	GPU PWR AND GND

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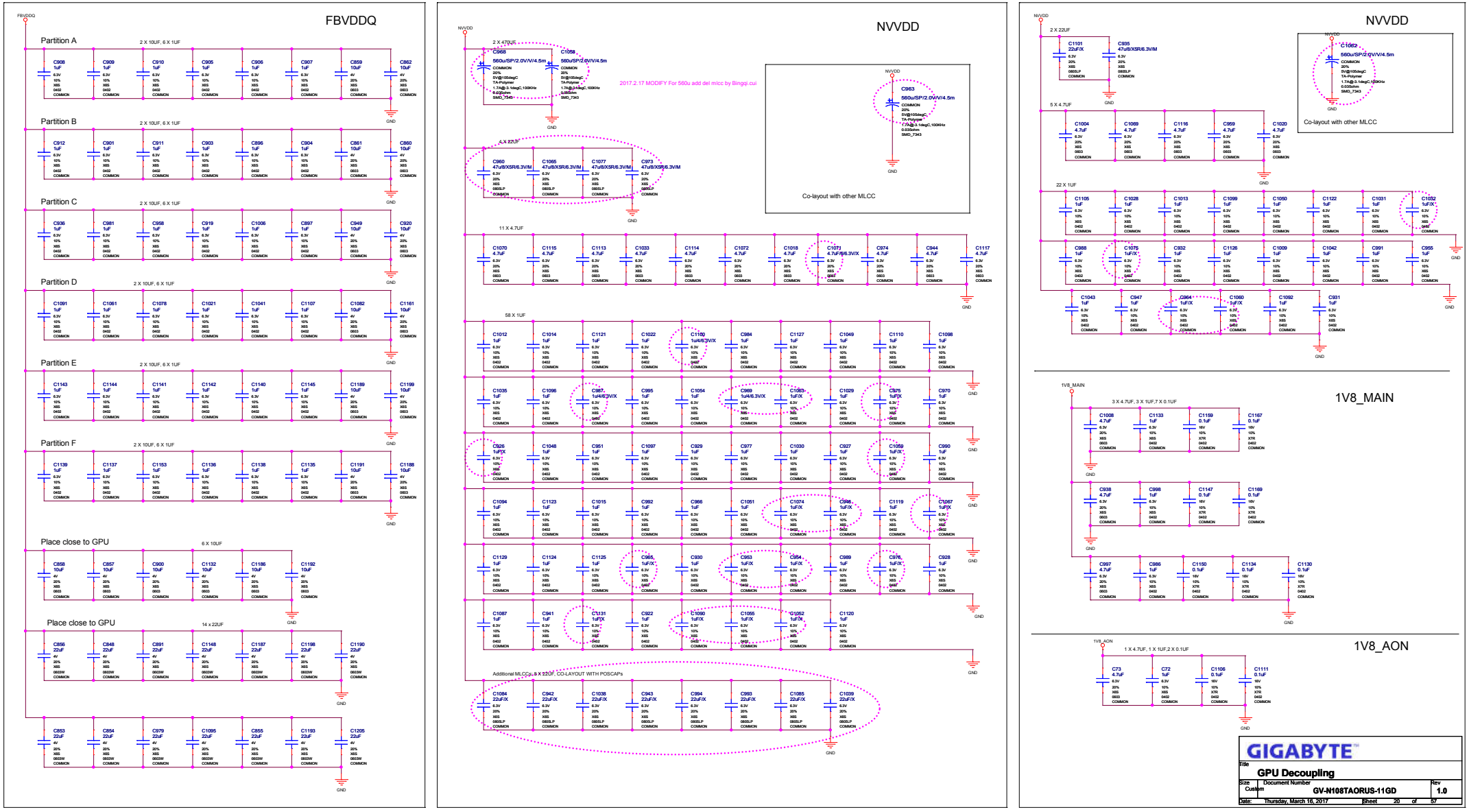
Page20: GPU Decoupling



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PAGE DETAIL	GPU DECOUPLING

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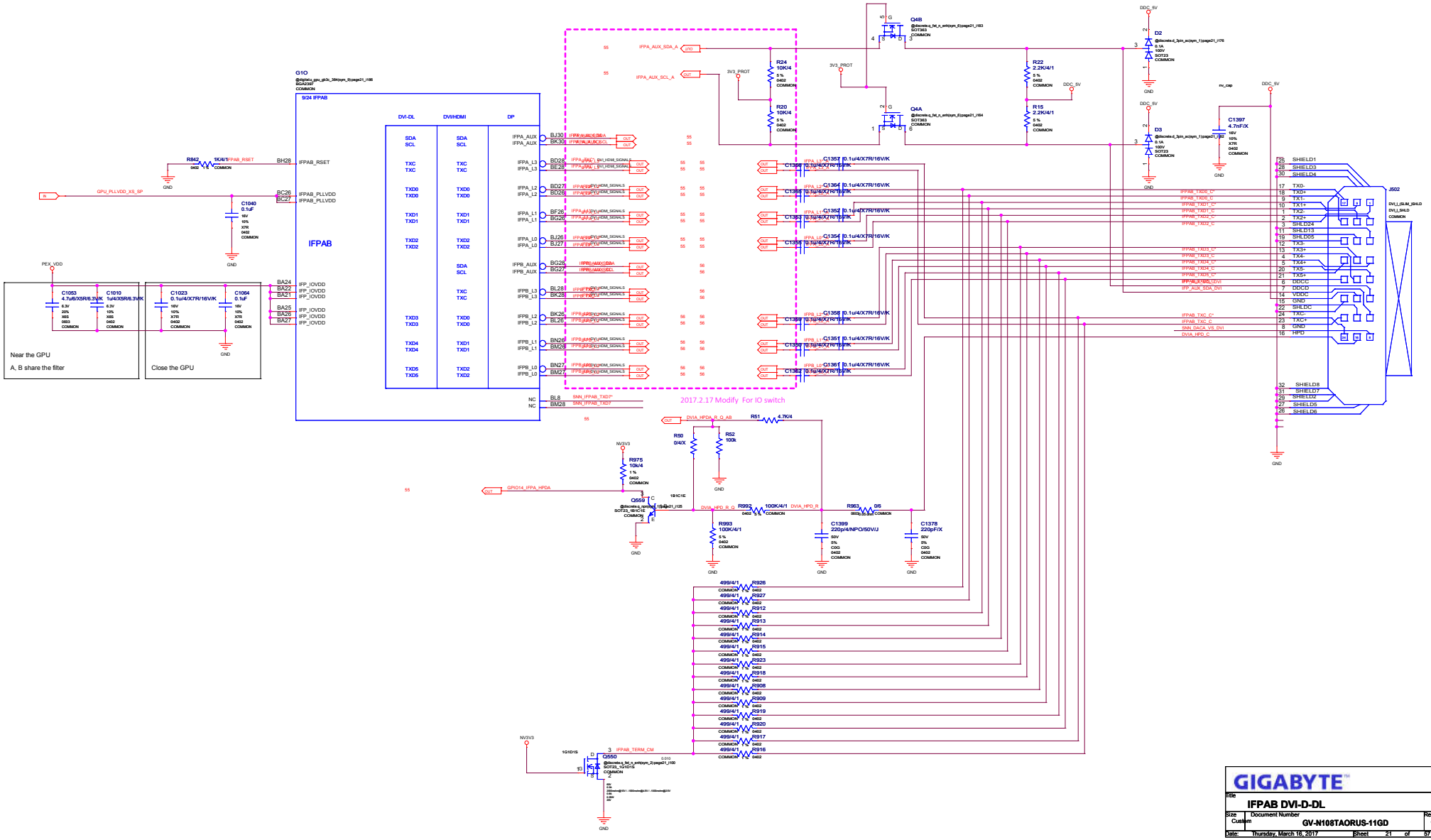
Page21: IFPAB DVI-D-DL



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Title	IFPAB DVI-D-DL
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPAB DVI-D-DL

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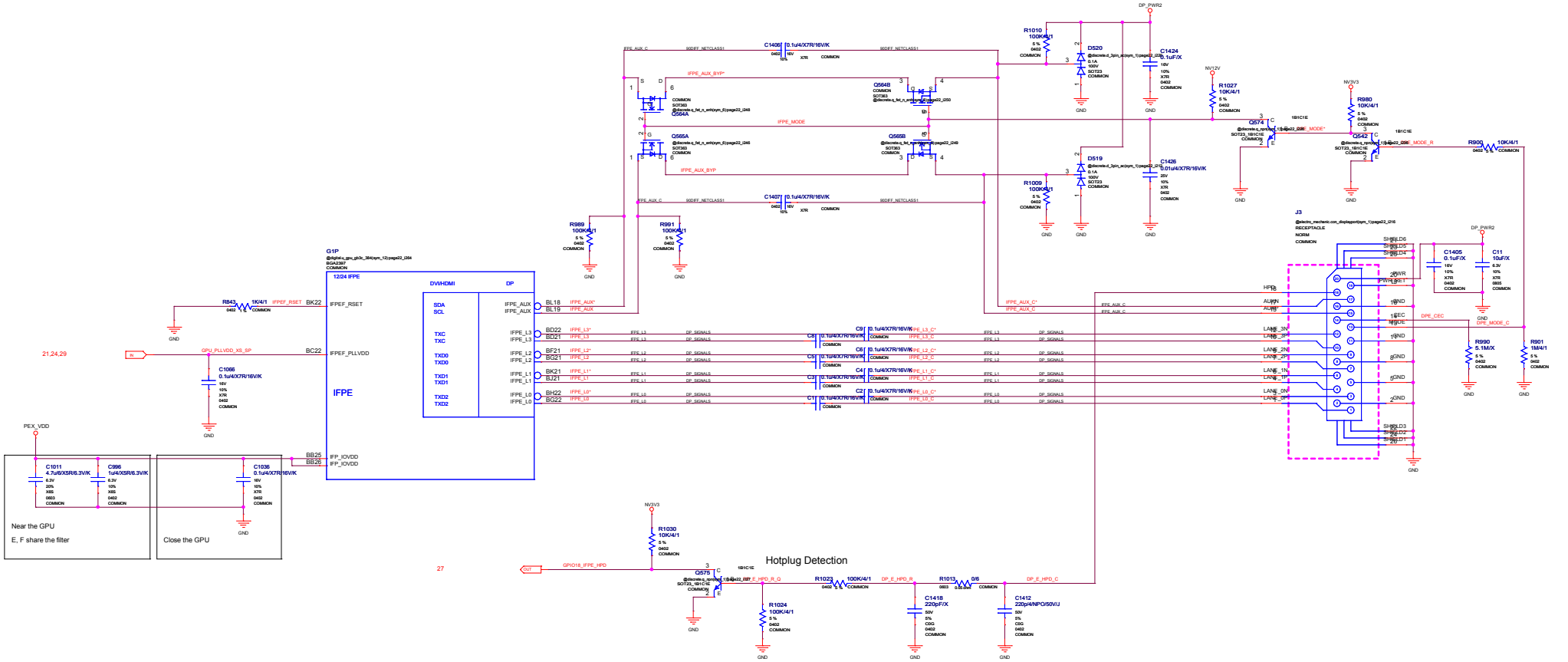
Page22: IFPE DP



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PAGE DETAIL	IFPE DP

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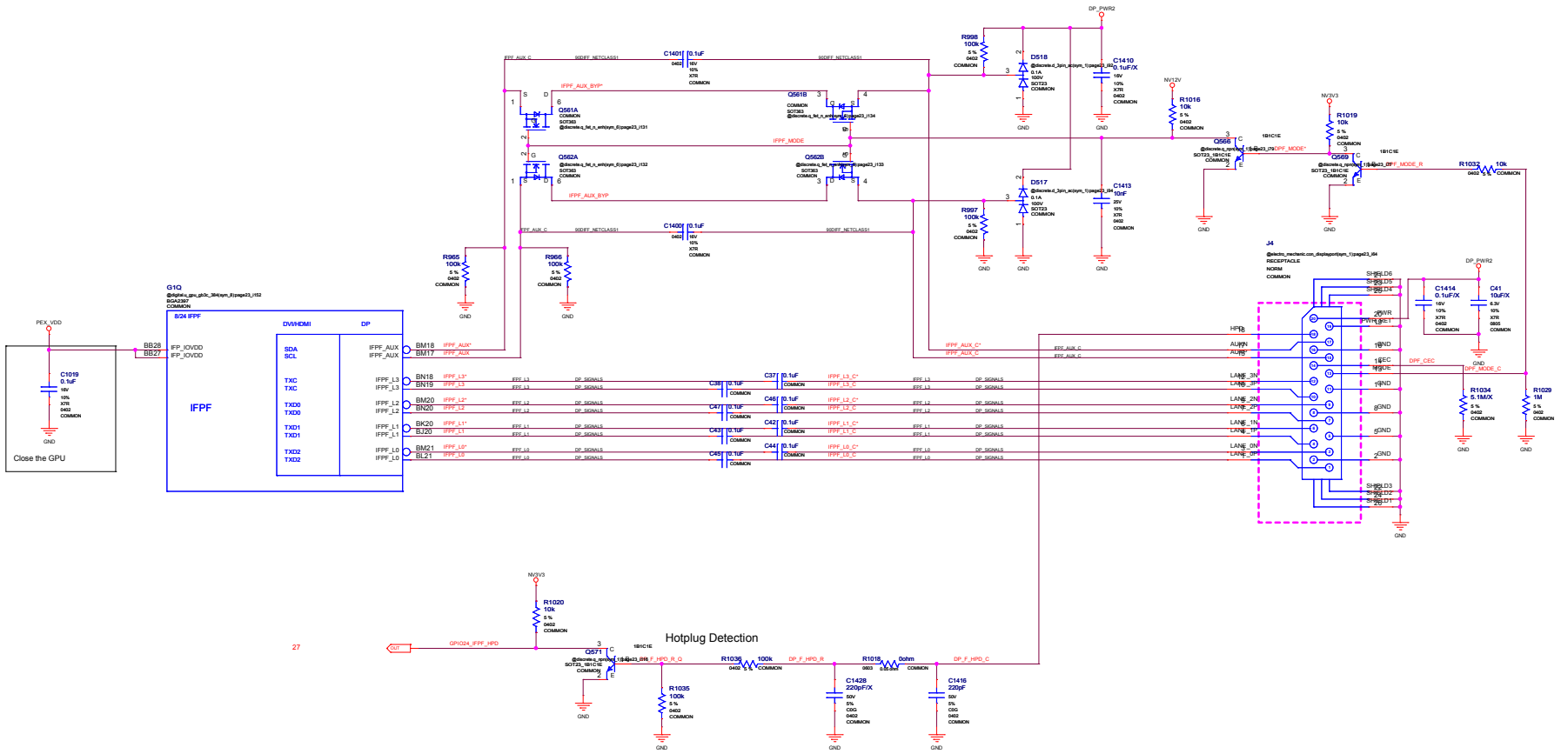
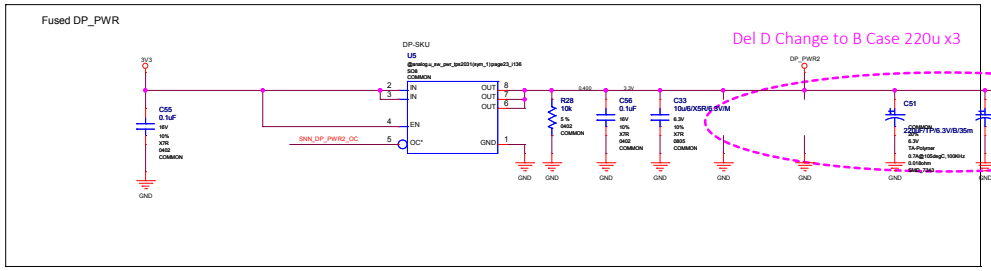
Page23: IFPF DP





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PAGE DETAIL	IFPF DP

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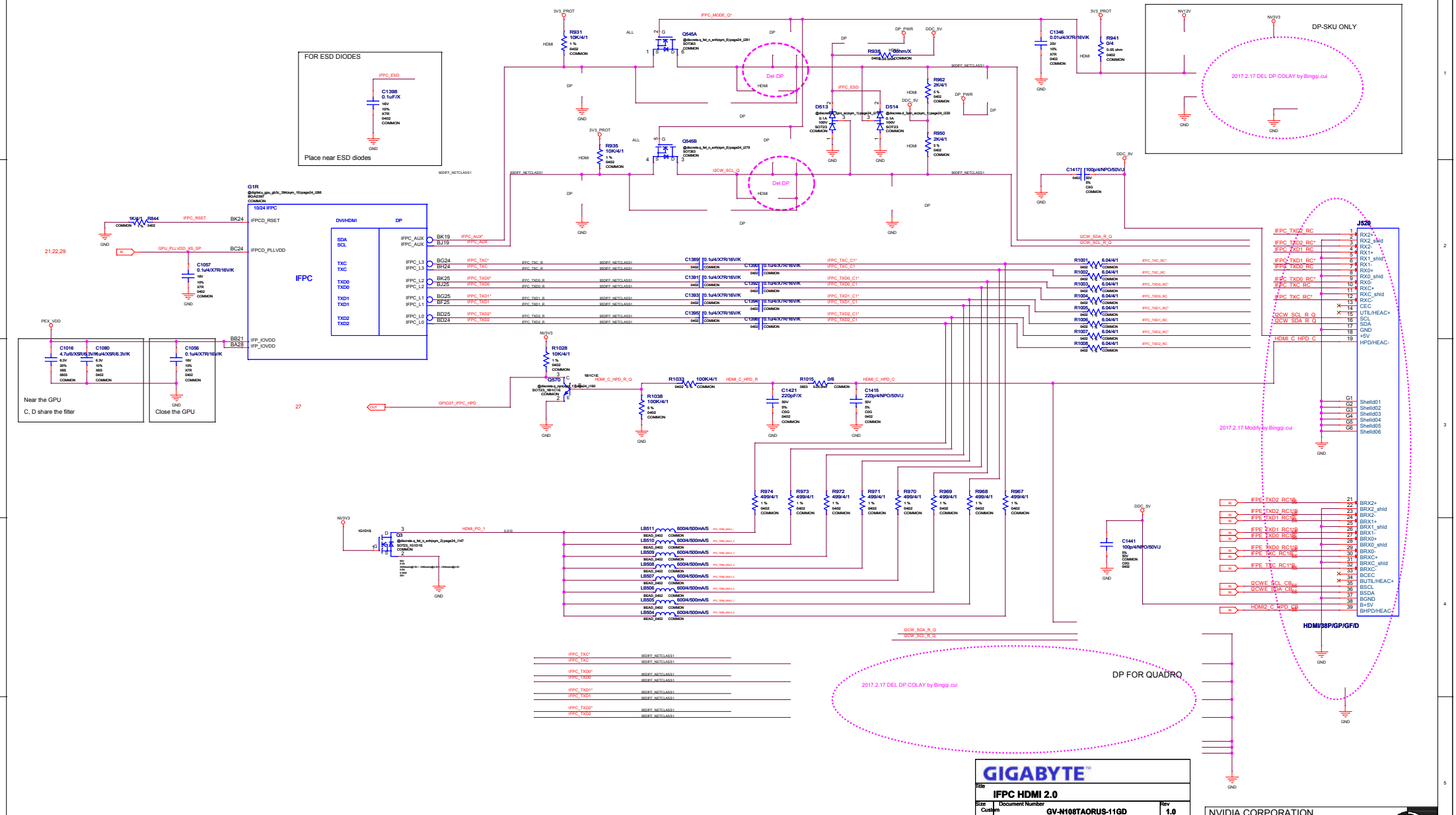
Page24: IFPC HDMI 2.0/DP



GIGABYTE

Title	IFPC HDMI 2.0		
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPC HDMI/DP

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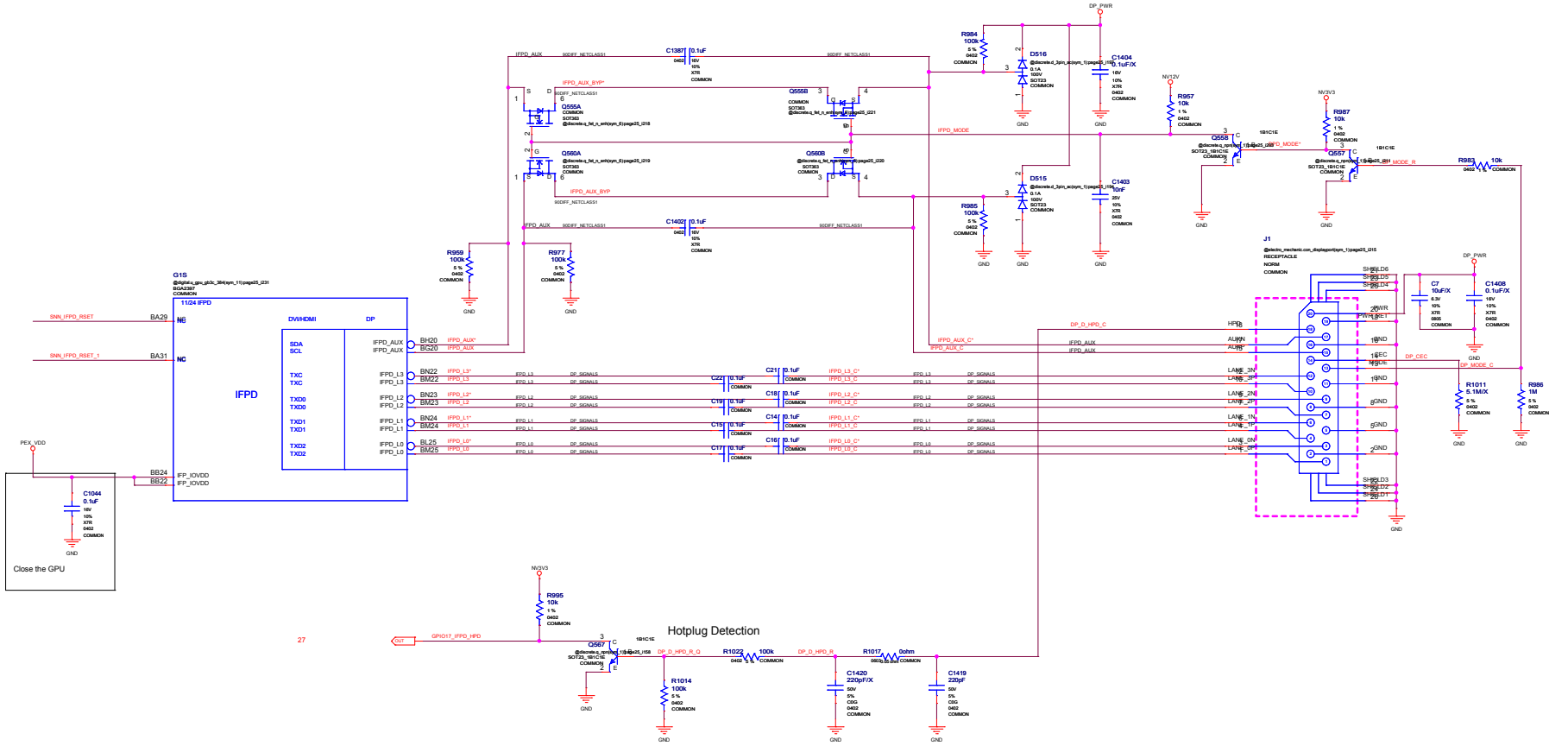
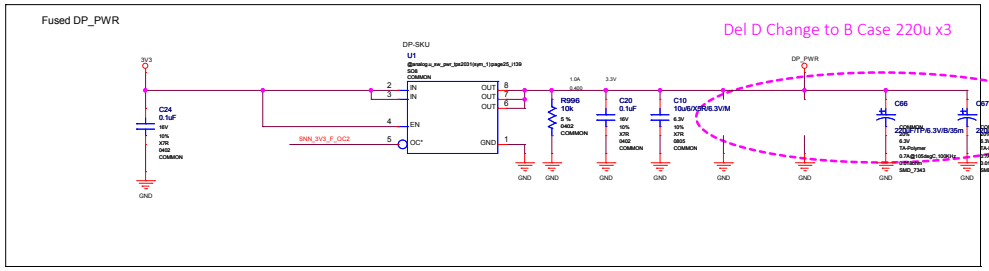
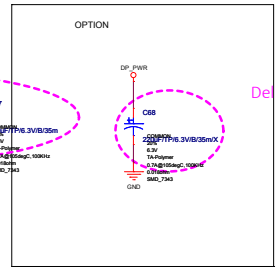
Page25: IFPD DP







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PAGE DETAIL	IFPD DP

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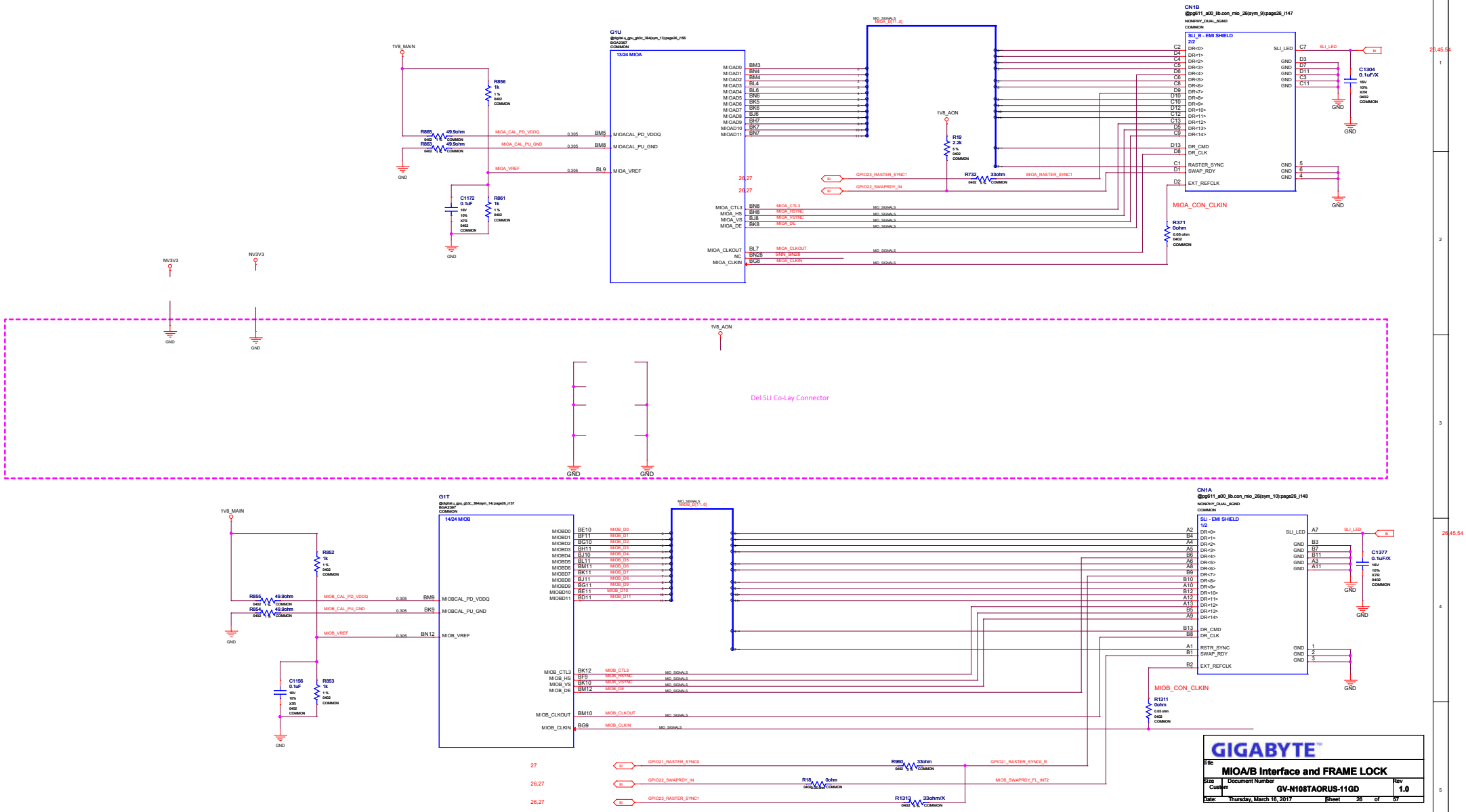
Page26: MIOA/B Interface and FRAME LOCK



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MIOA/B INTERFACE & FRAME LOCK

GIGABYTE

Title: MIOA/B Interface and FRAME LOCK

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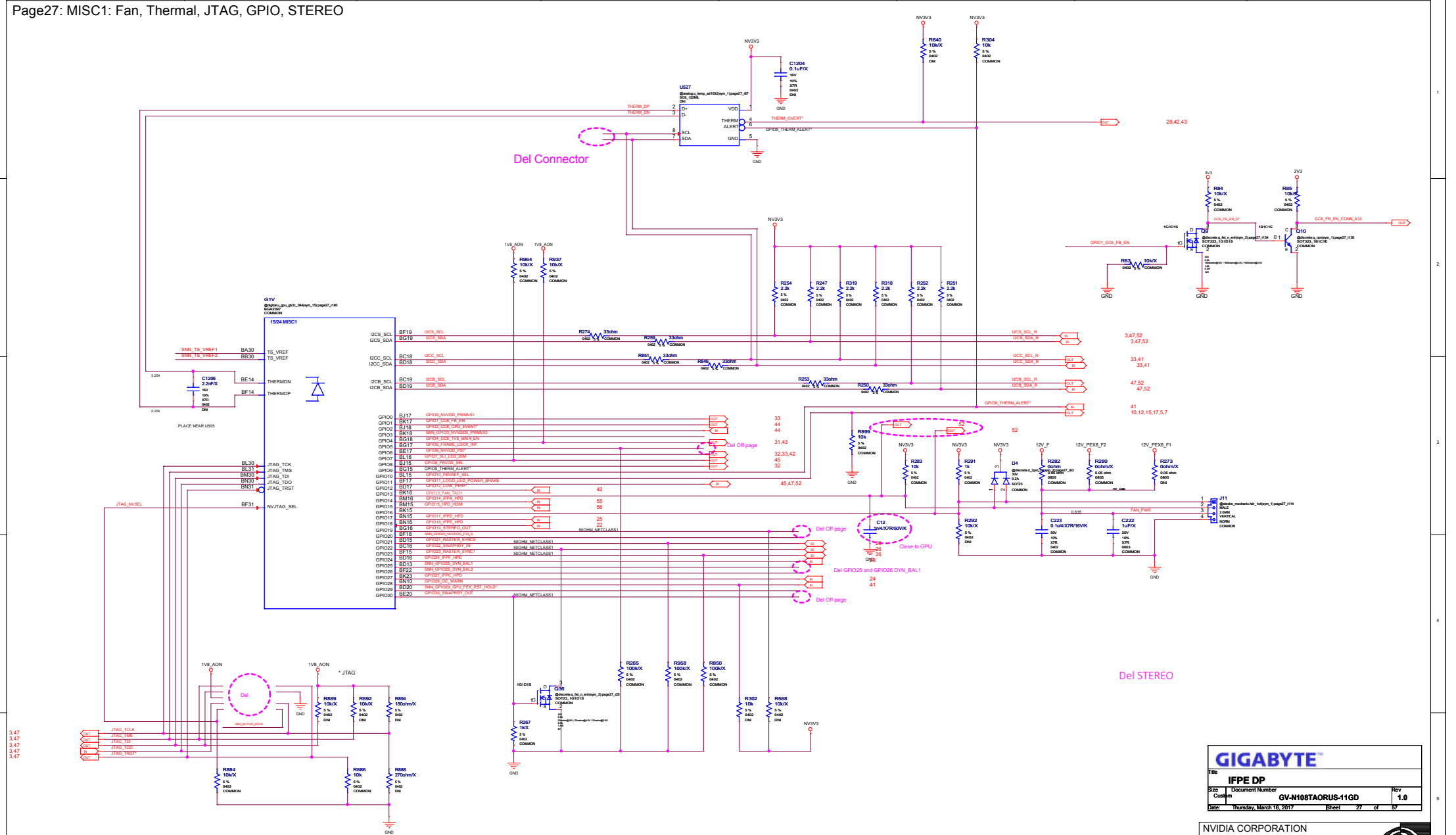
Page27: MISC1: Fan, Thermal, JTAG, GPIO, STEREO



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Page28: MISC2: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

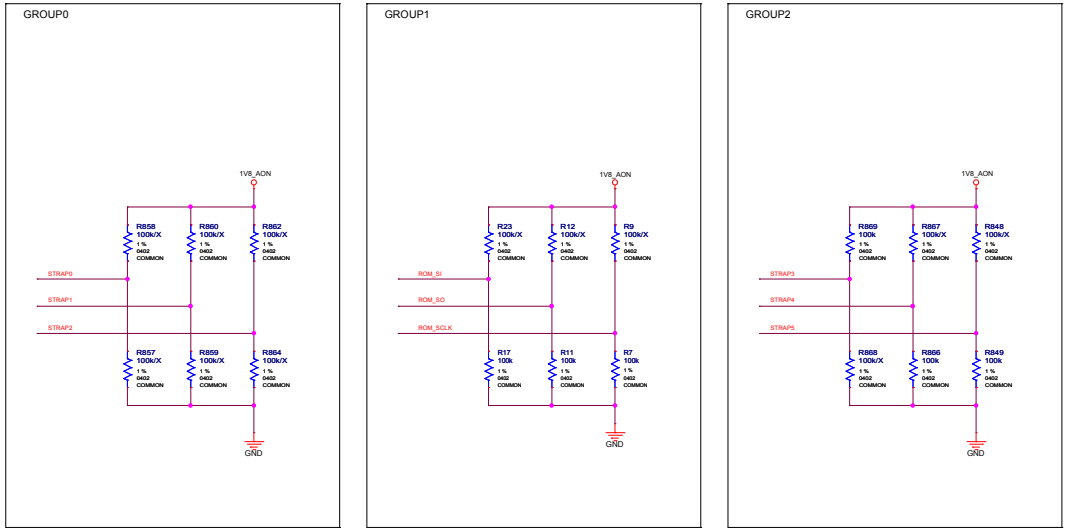
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

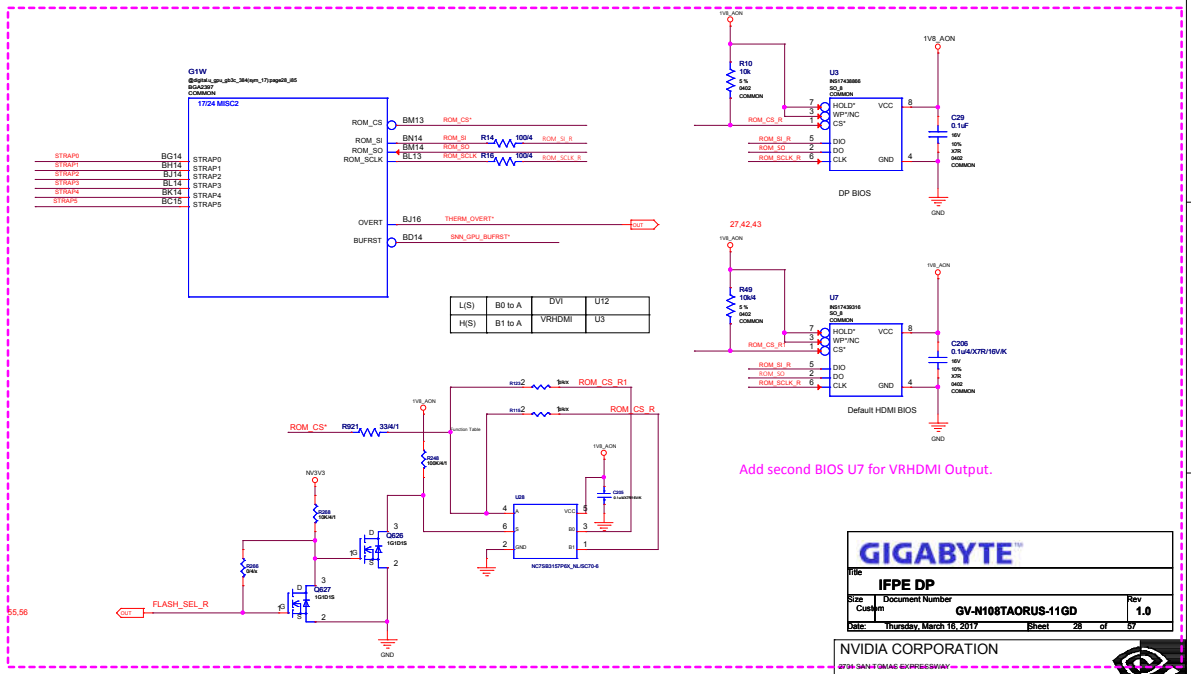
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE





L(S)	B0 to A	DVI	U12
H(S)	B1 to A	VRHDMI	U3

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC: ROM, STRAPS

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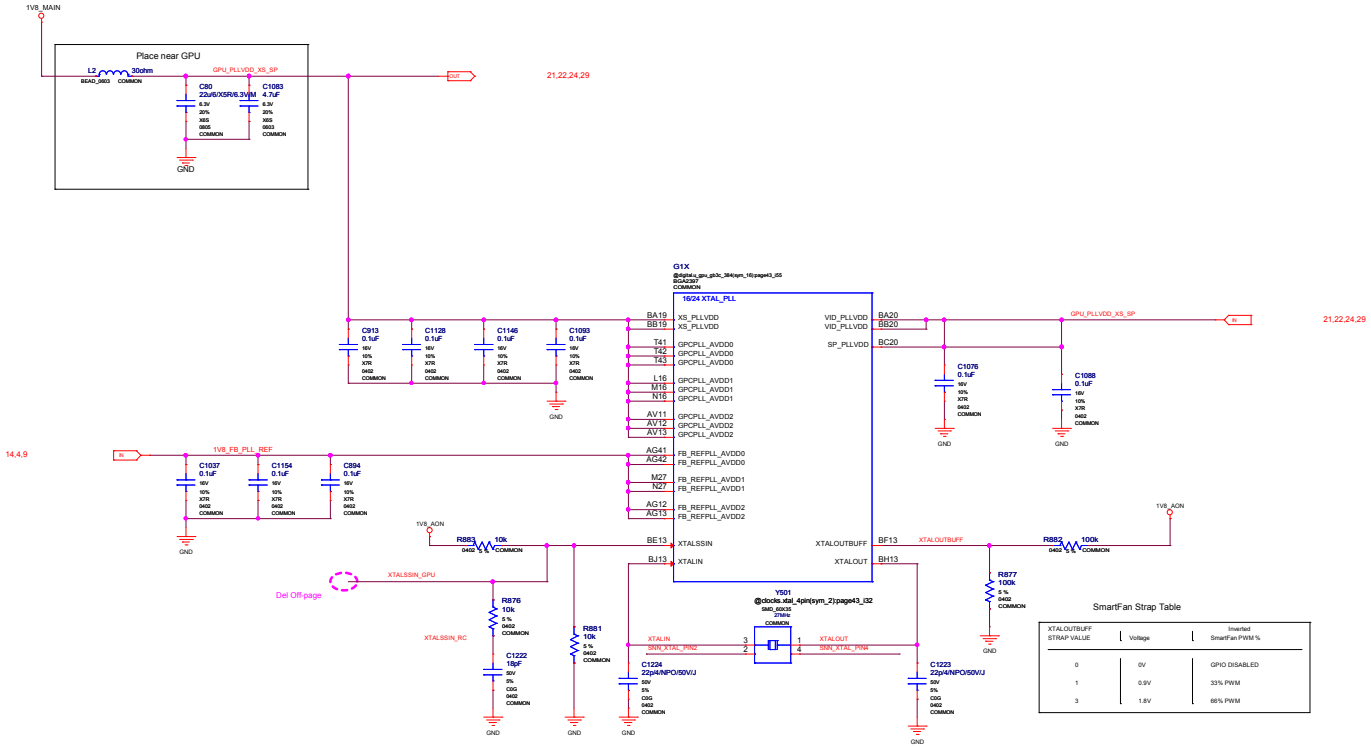
Page29: MISC2: XTAL. PLL



SmartFan Strap Table

XTALOUTBUFF STRAP VALUE	Voltage	Inverted SmartFan PWM %
0	0V	GPIO DISABLED
1	0.9V	33% PWM
3	1.8V	66% PWM

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC: XTAL, PLL

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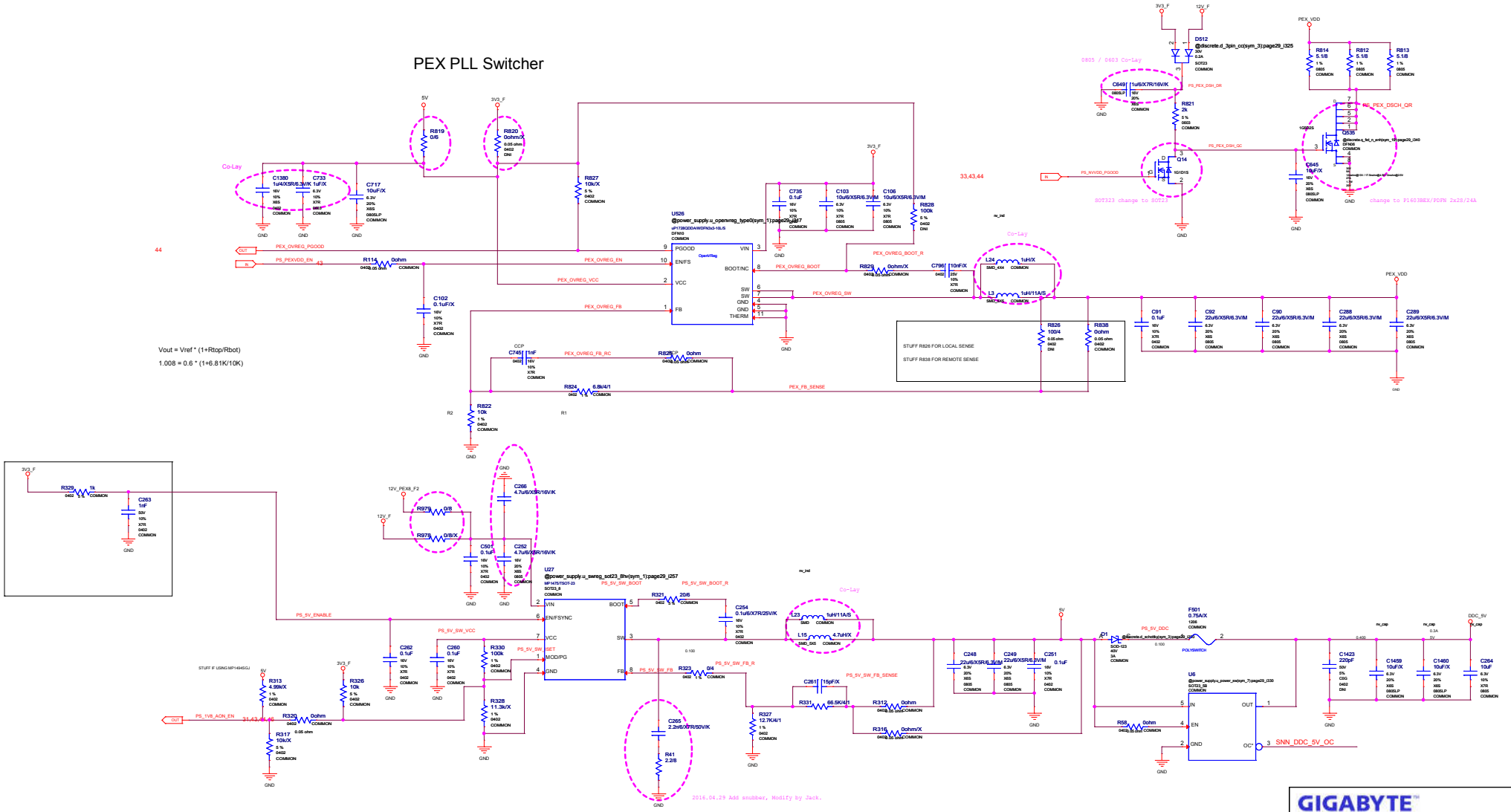
Page30: PS: 5V, PEX_VDD

PEX PLL Switcher



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PAGE DETAIL	PS: 5V, PEXVDD

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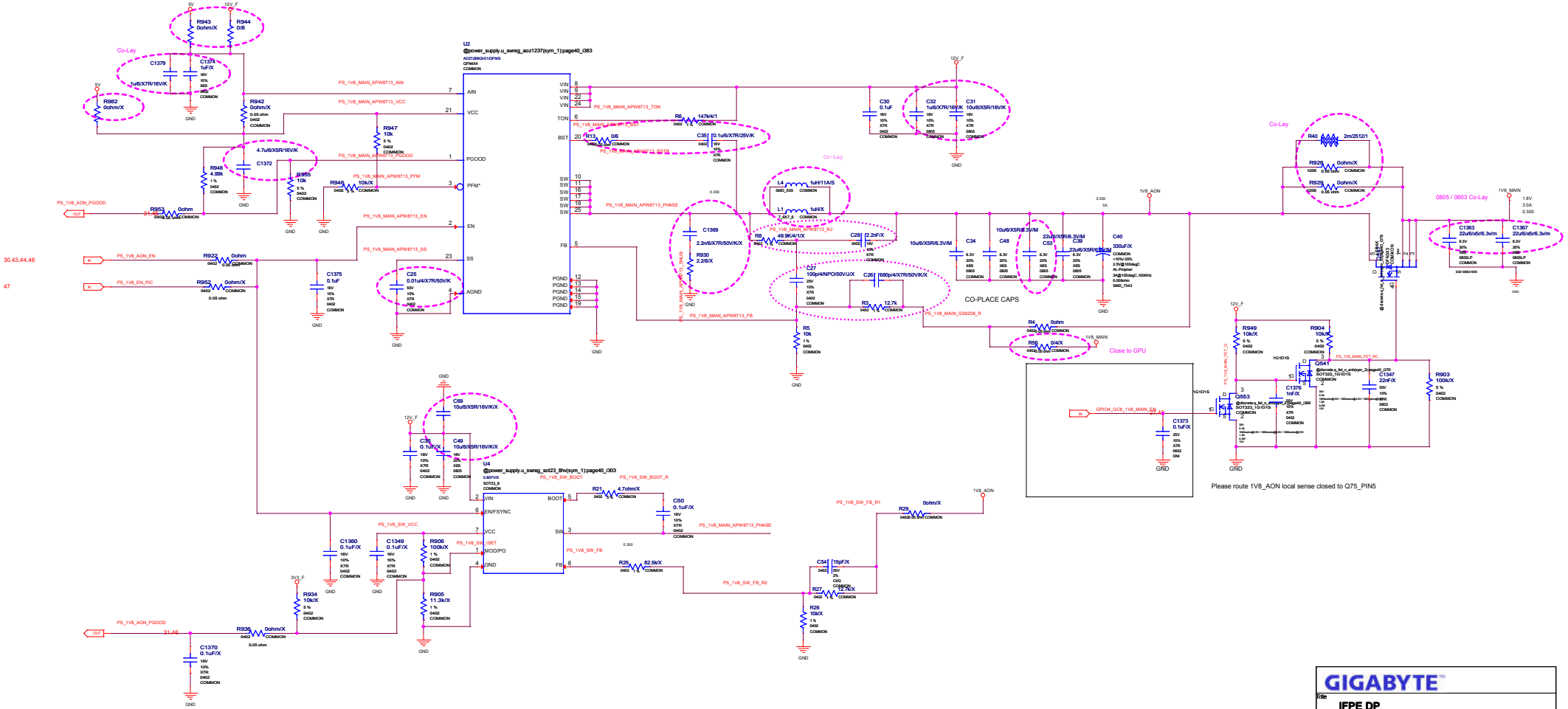
Page31: PS: 1V8 Rails



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PAGE DETAIL	PS: 1V8 Rails

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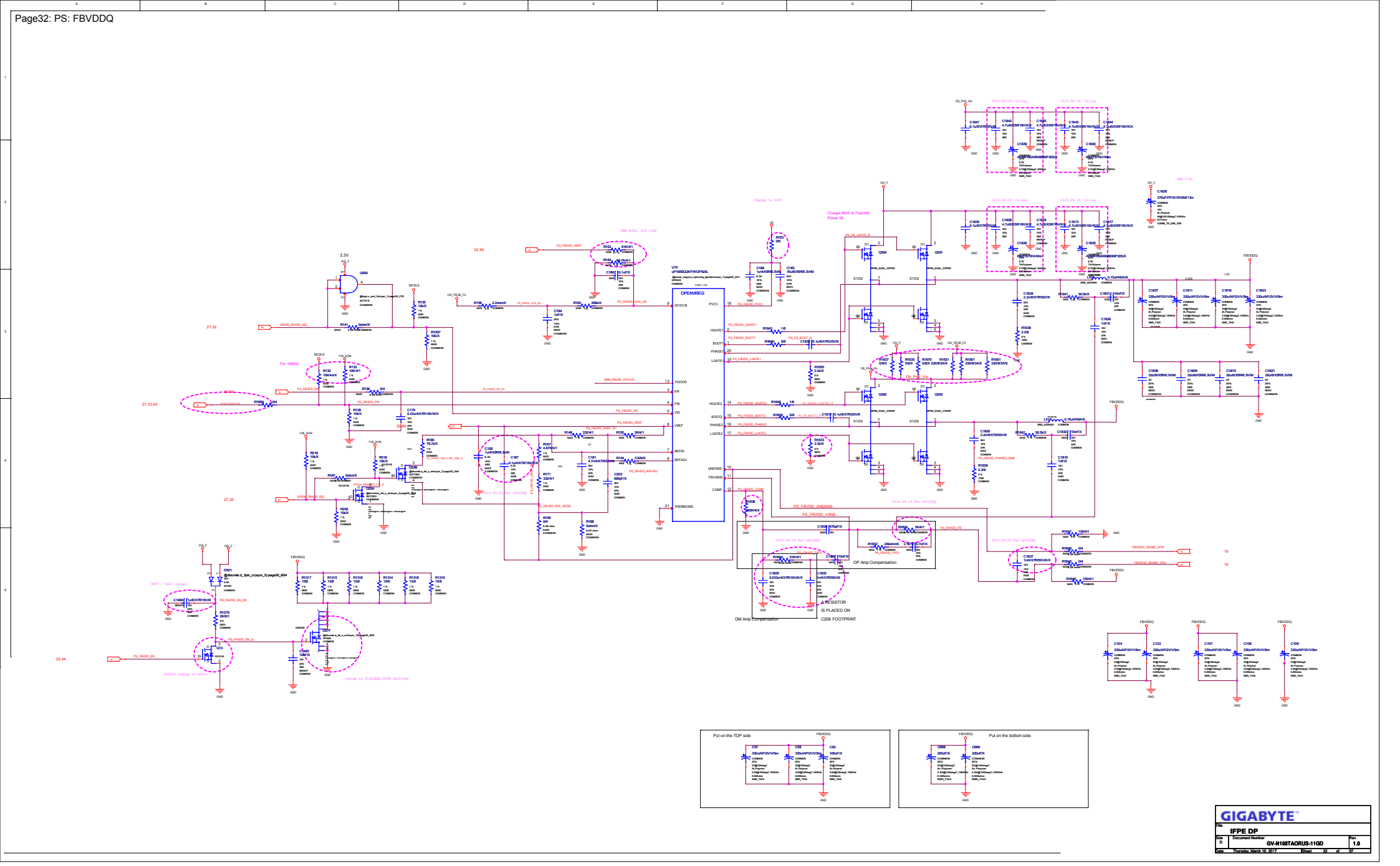
OPENREG
U15
Change MOS to Fairchild Power 56
OP Amp Compensation
GM Amp Compensation
A RESISTOR IS PLACED ON C206 FOOTPRINT
Put on the TOP side
Put on the bottom side
FBVDDQ
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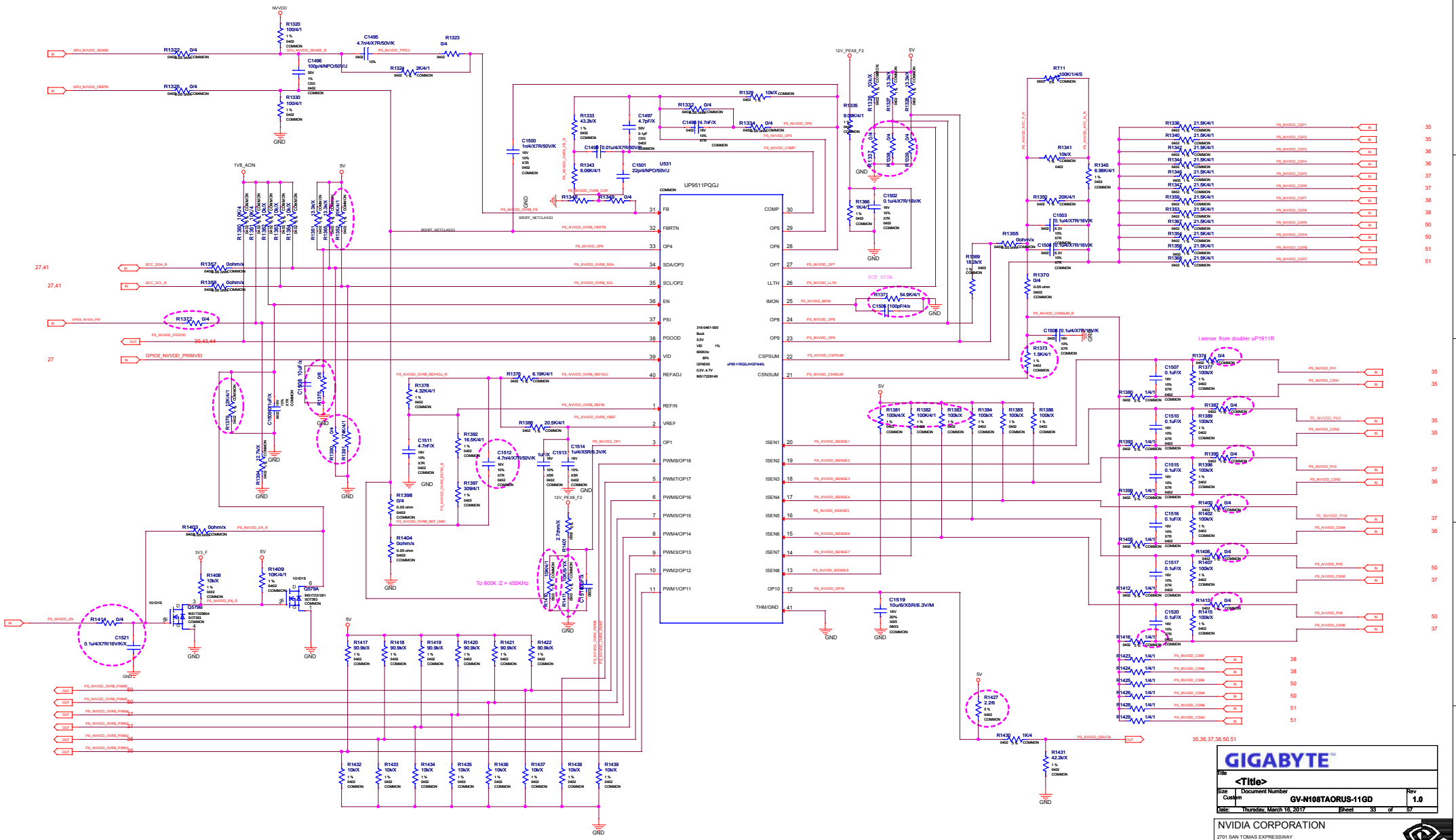
Page27: PS: NVVDD_OVR8



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD_OVR8

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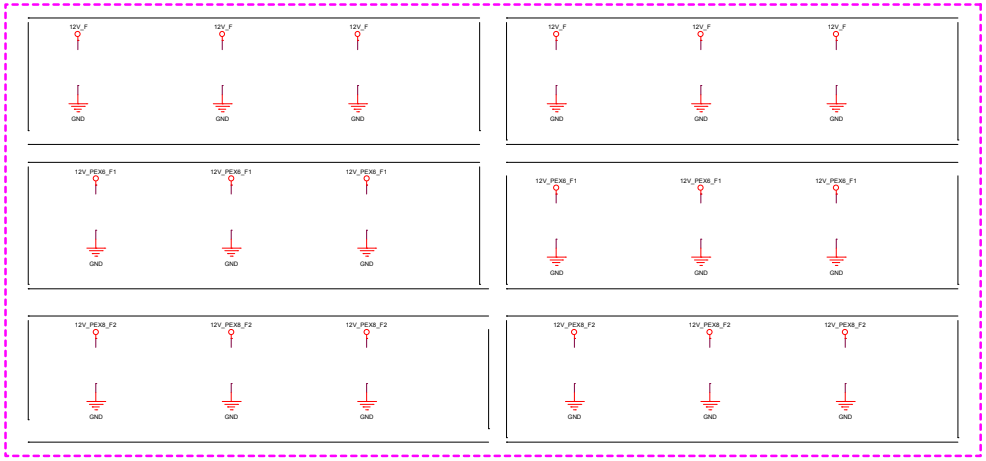
Del PWM MODULE

CO-LAYOUT: CHOOSE ONE ONLY



Del P-Board CAP

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>		
PAGE DETAIL	PS: NVVDD Controller_PWR-MODULE		
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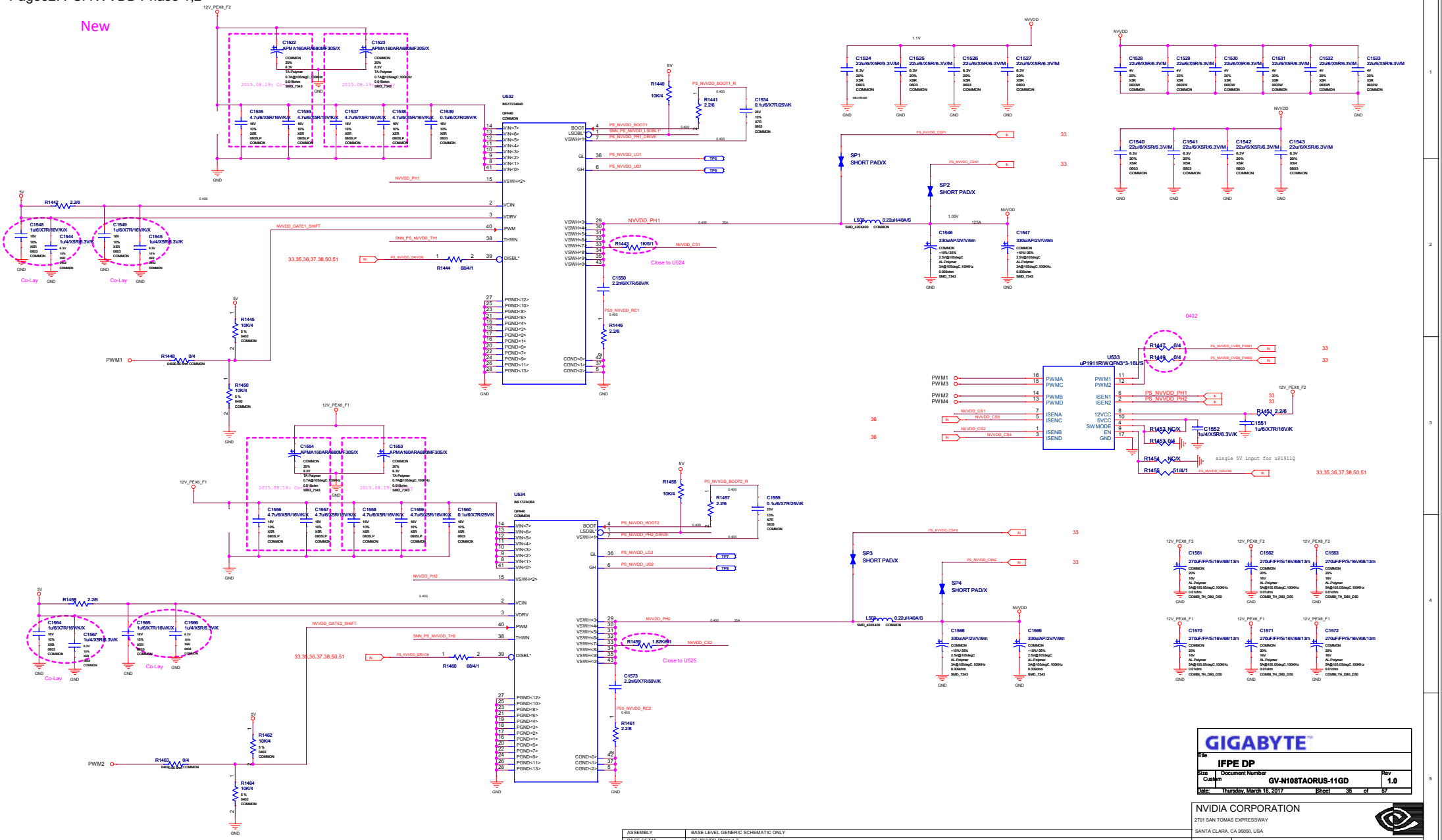
Page32: PS: NVVDD Phase 1,2

New



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD Phase 1,2

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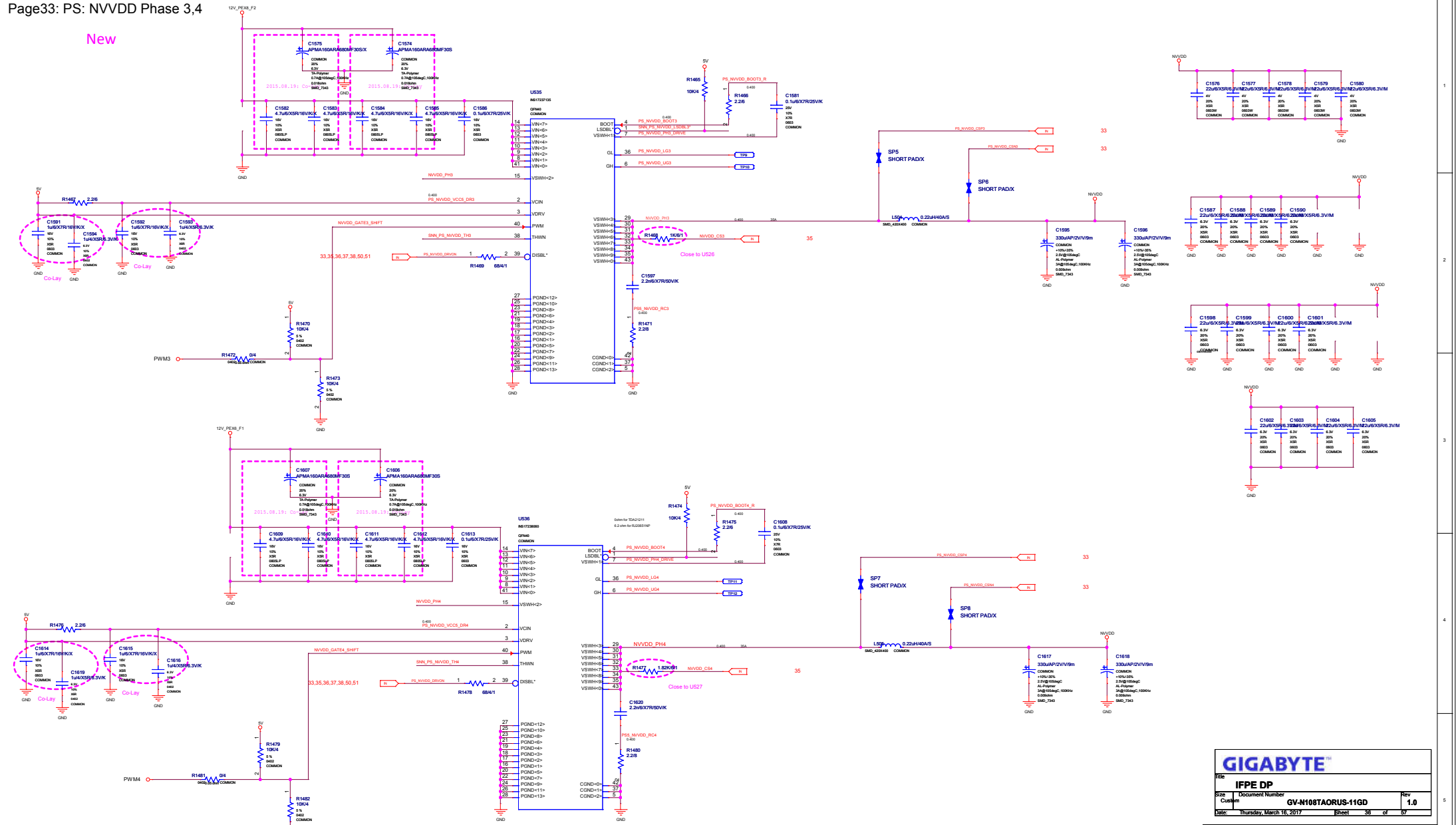
Page33: PS: NVVDD Phase 3,4

New



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD Phase 3,4

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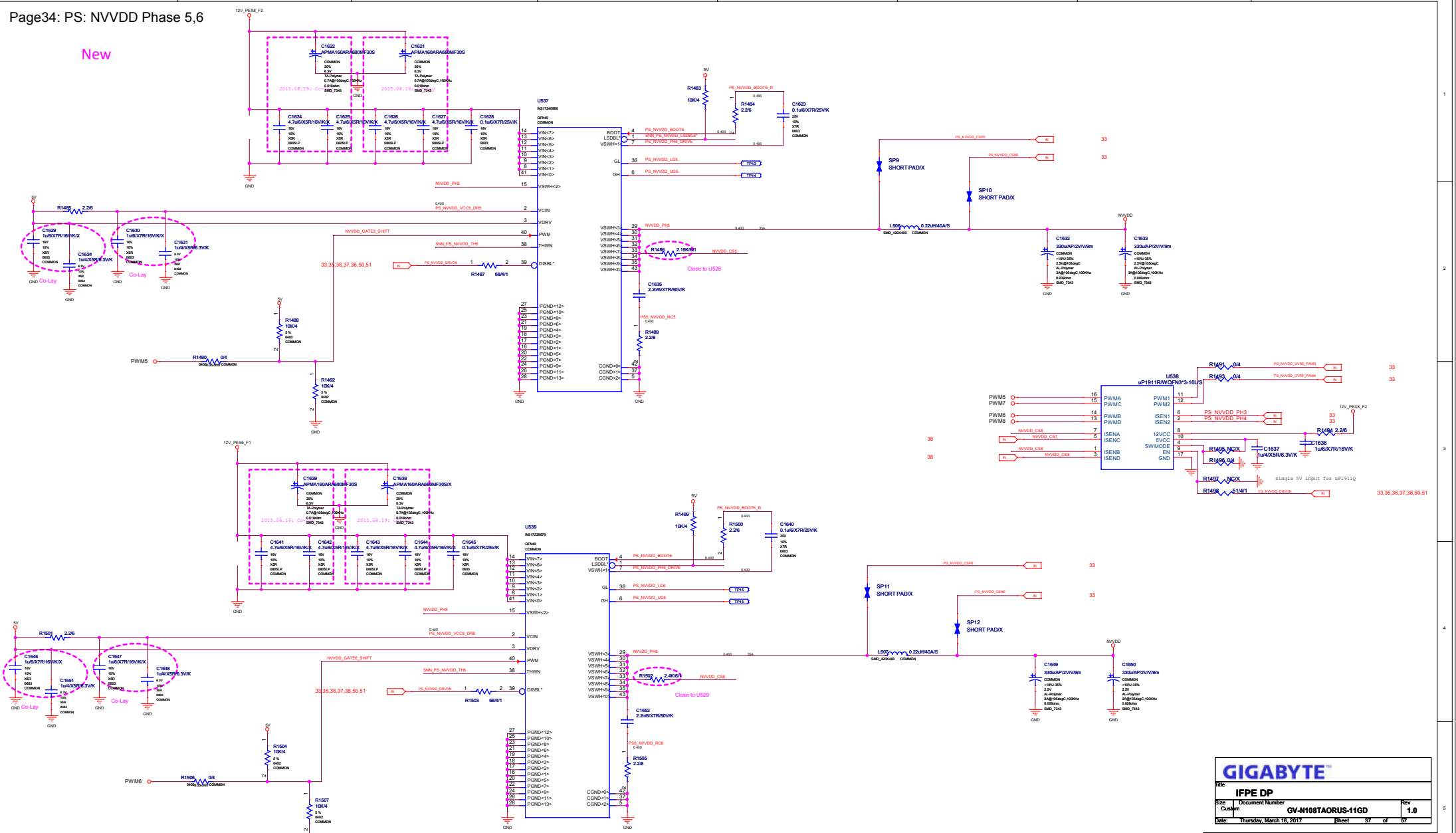
Page34: PS: NVVDD Phase 5,6

New



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD Phase 5,6

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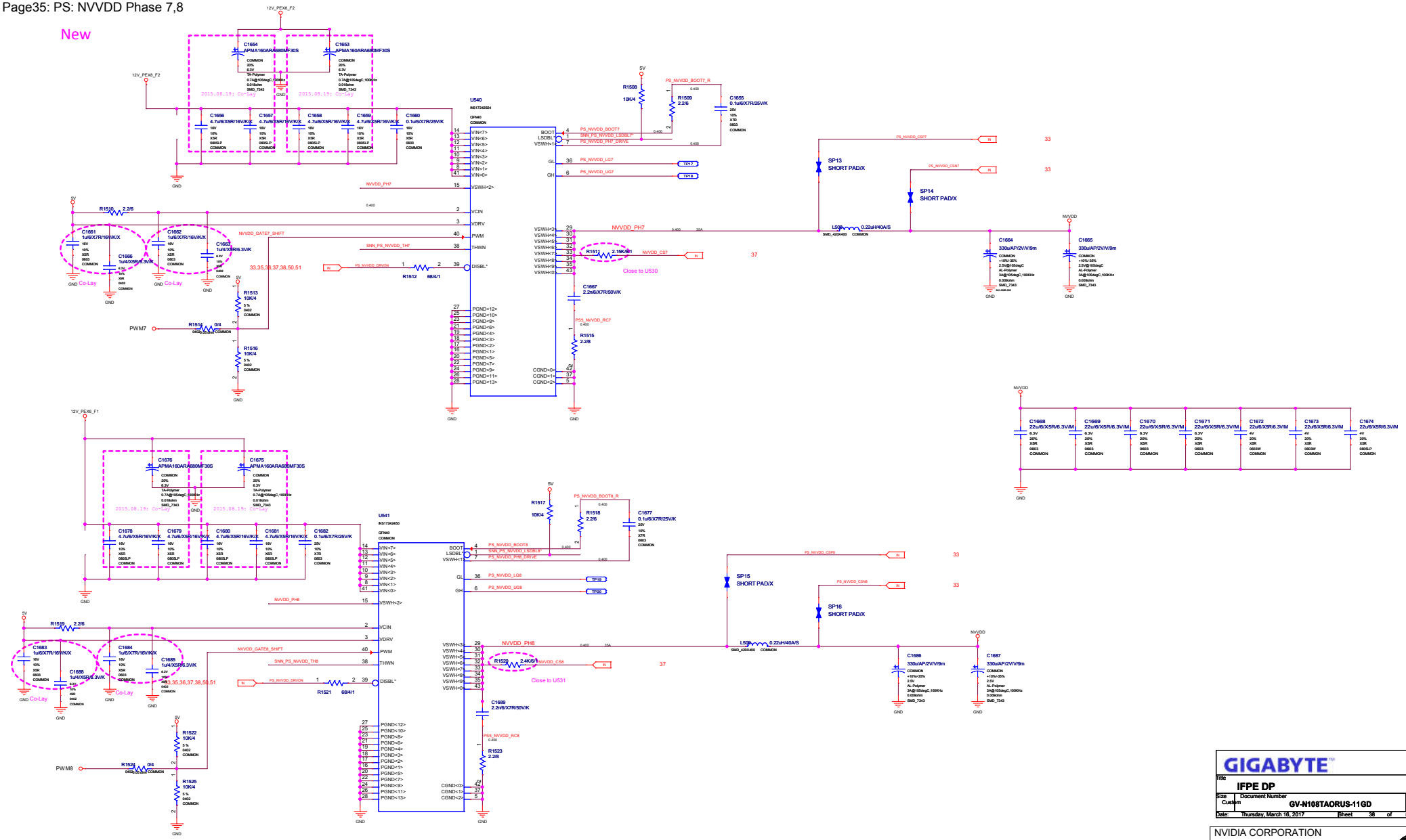
Page35: PS: NVVDD Phase 7,8

New



CO-LAYOUT: CHOOSE UA OR UB

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD Dynamic Switch Phases

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Page39: PS: Dynamic Power Balance Phases

Delete

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Dynamic power balance phase

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Page40: PS: Dynamic Power Balance Logic

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Dynamic power balance logic

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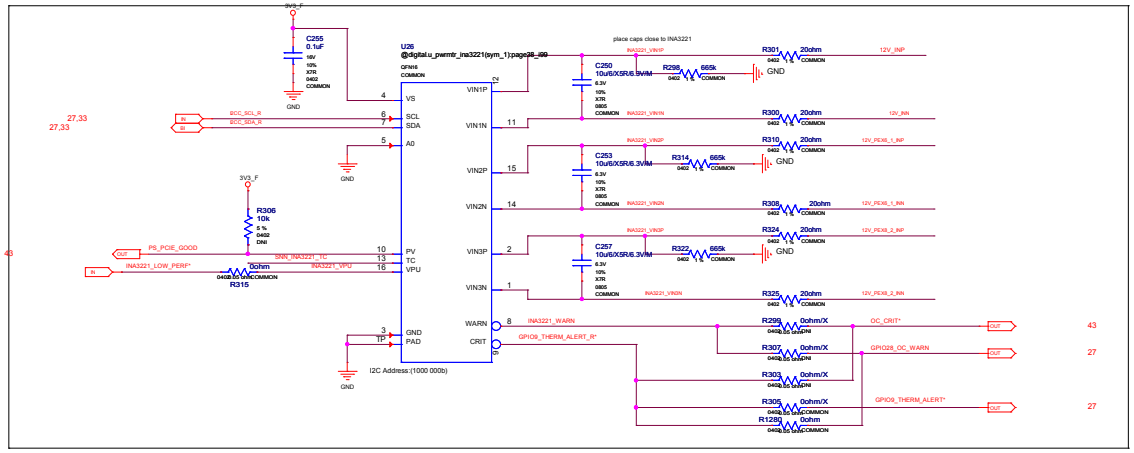
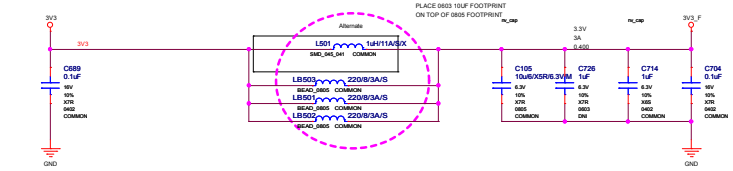
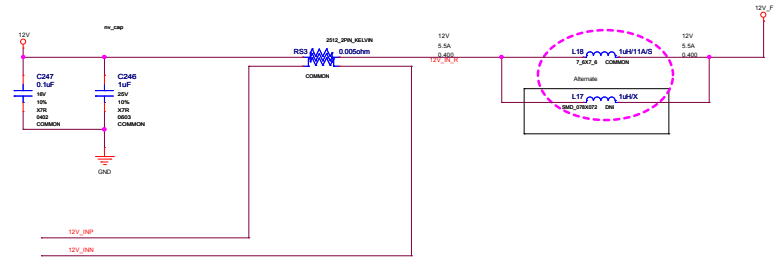
Page41: PS: Inputs, Filtering, and Monitoring



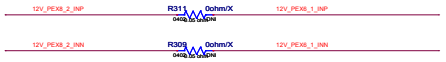
PEX 3V3 INPUT - 10W

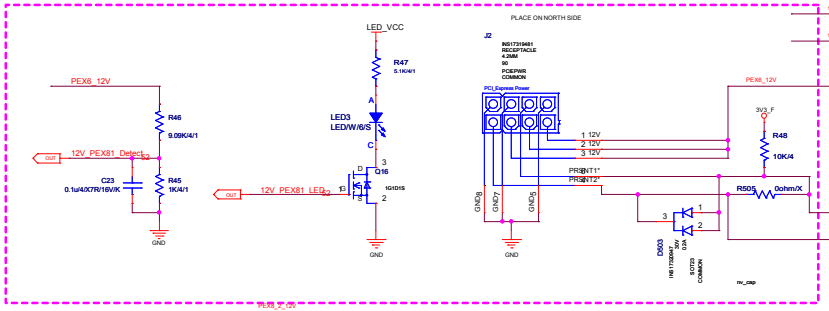


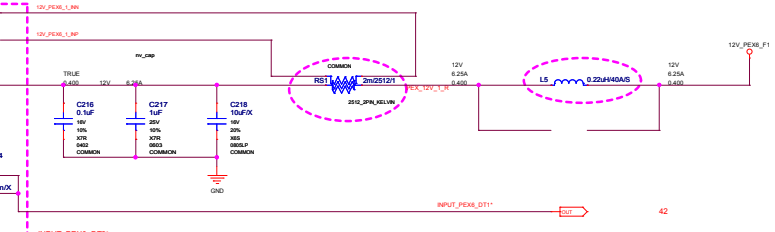
PEX_12V INPUT - 66W



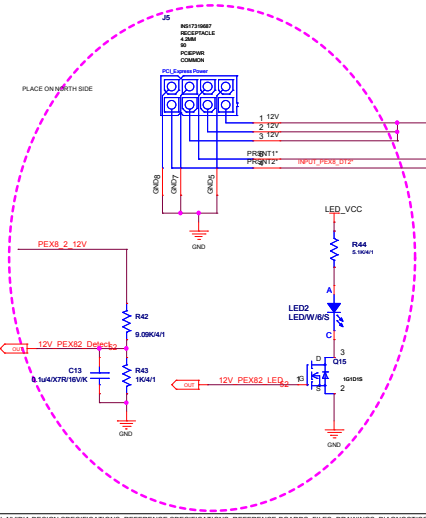
PEX6 INPUT 1 - 2x3 PCIE CON 75W

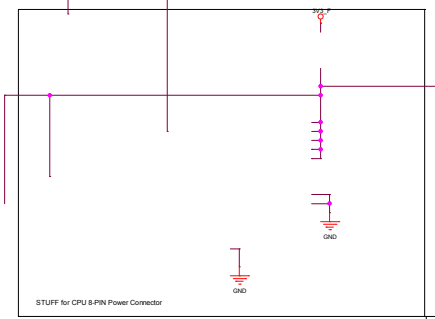


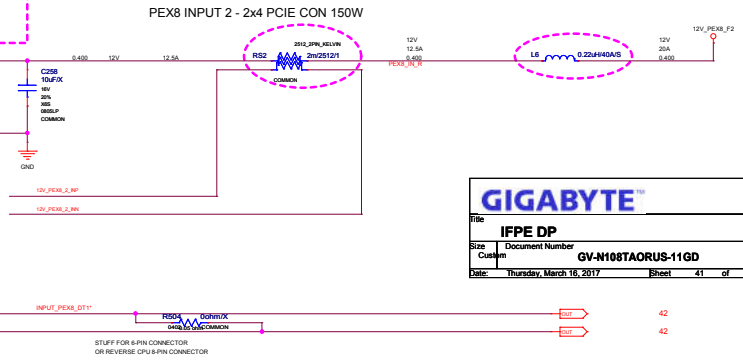




PEX8 INPUT 2 - 2x4 PCIE CON 150W







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PAGE DETAIL	PS: Input, filtering, and Monitoring		
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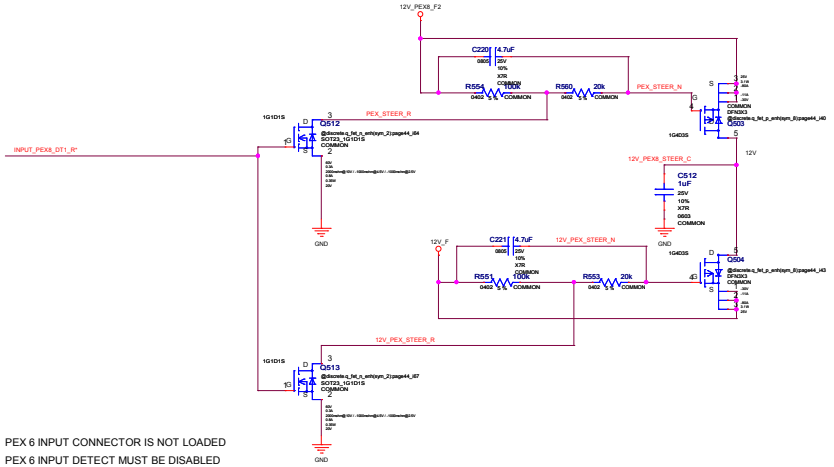
Page42: PS: 12V Current Steering & Hot Unplug Detect

QUADRO/TESLA:

12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

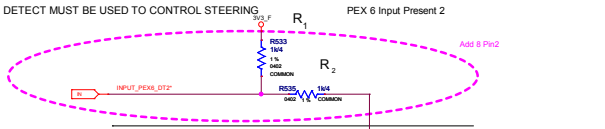
For OpenVreg Type4 + Phase Doubler, 2 phase PSI mode



PEX 6 INPUT CONNECTOR IS NOT LOADED

PEX 6 INPUT DETECT MUST BE DISABLED

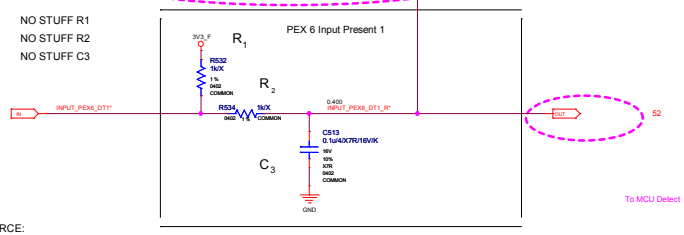
PEX 8 INPUT DETECT MUST BE USED TO CONTROL STEERING



NO STUFF R1

NO STUFF R2

NO STUFF C3



GeFORCE:

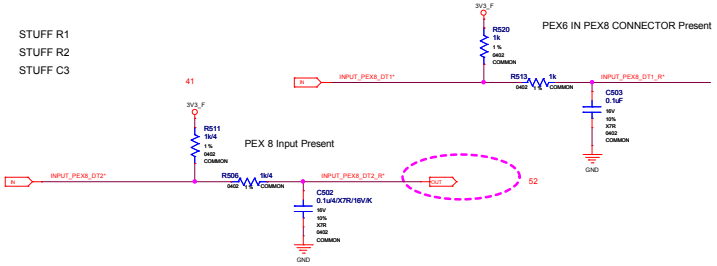
PEX 6 INPUT CONNECTOR IS LOADED

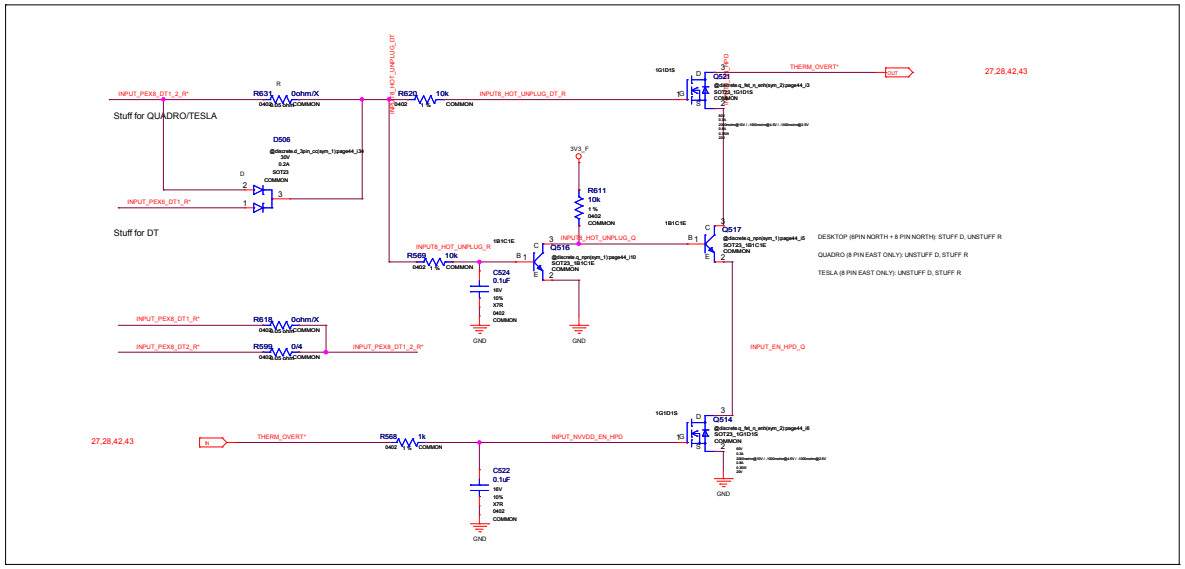
PEX 6 INPUT DETECT MUST BE USED TO CONTROL STEERING

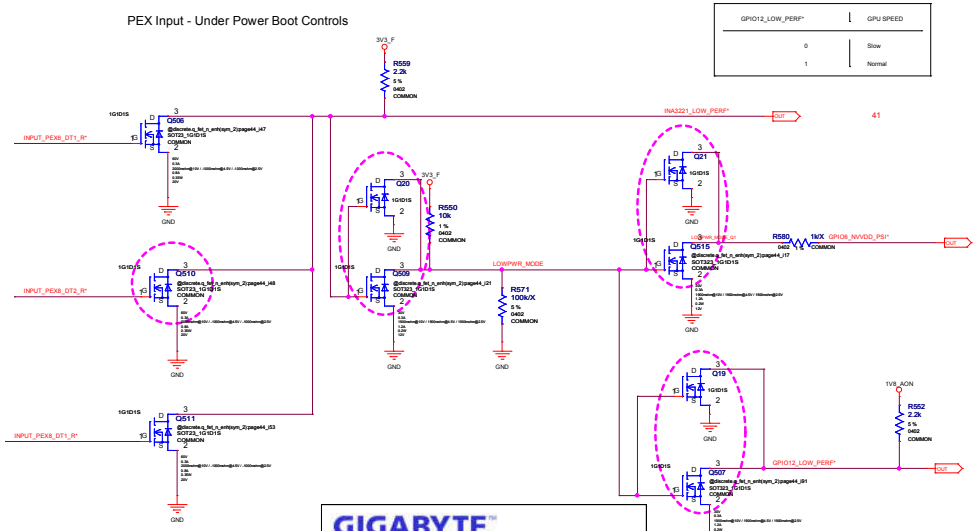
STUFF R1

STUFF R2

STUFF C3







A 2 x 4 auxiliary power connector plug from the power supply unit must not use the 75 W sense coding (Sense1=Open and Sense0=Ground) to avoid end-user confusion.

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Current Steering, Hot Unplug

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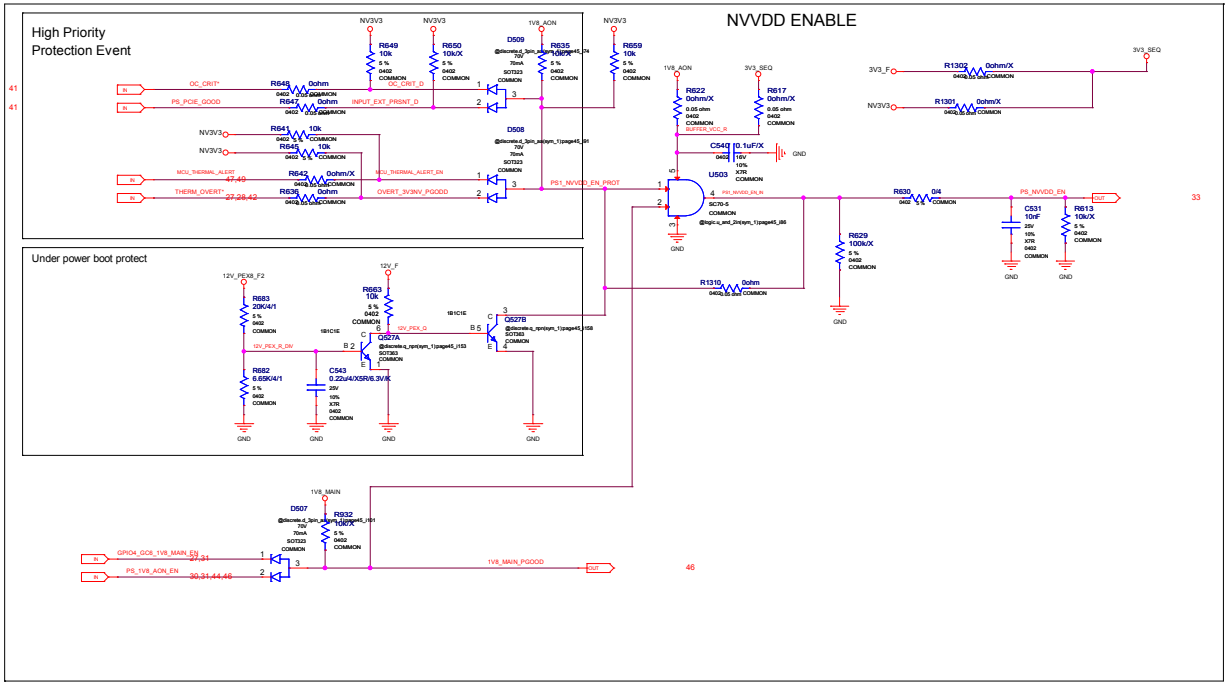
Page43: PS: NVVDD ENABLE

NVVDD ENABLE

High Priority Protection Event



Under power boot protect

PEXVDD ENABLE

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD ENABLE

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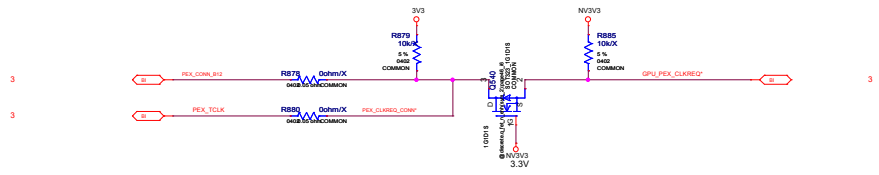
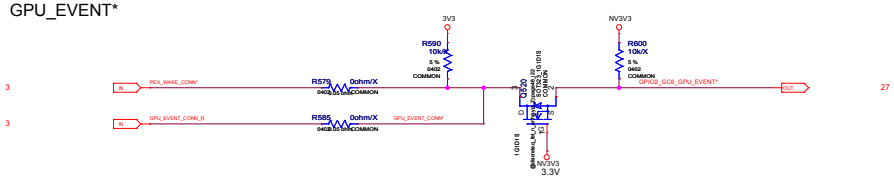
Page44: GC6 MISC

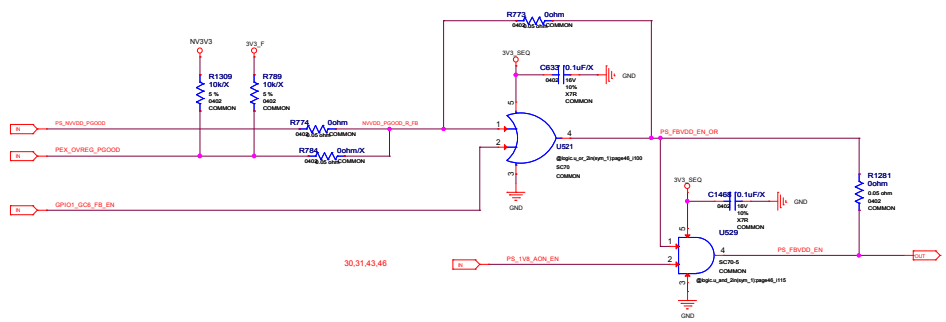
PEX_CLKREQ*



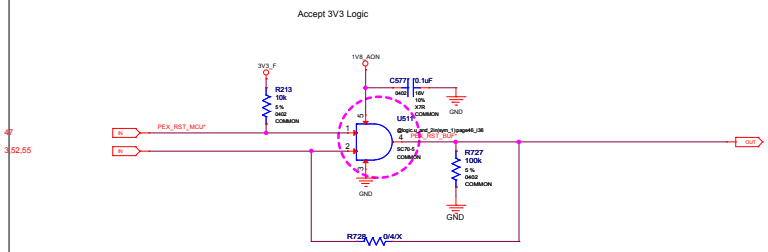
GPU_EVENT*



FBVDD/Q ENABLE



PEX_RST# LOGIC



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PAGE DETAIL	PS: GC6 MISC

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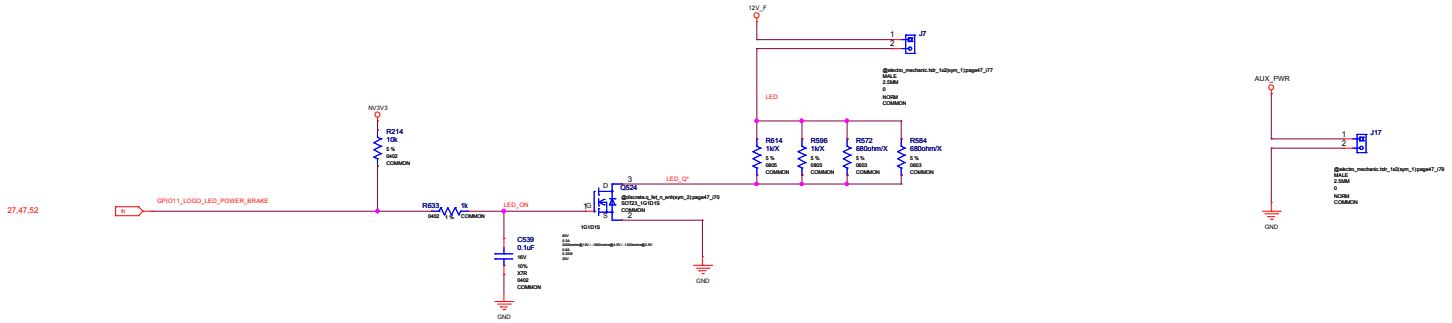
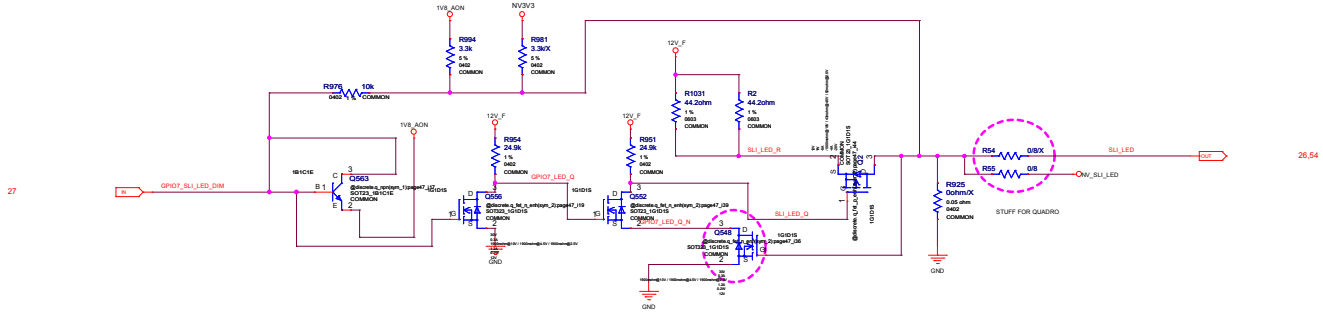
Page45:GEFORCE LED & SLI LED

LED HEADER(GEFORCE ONLY)



SLI LED (GEFORCE ONLY)



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GEFORCE LED AND SLI LED

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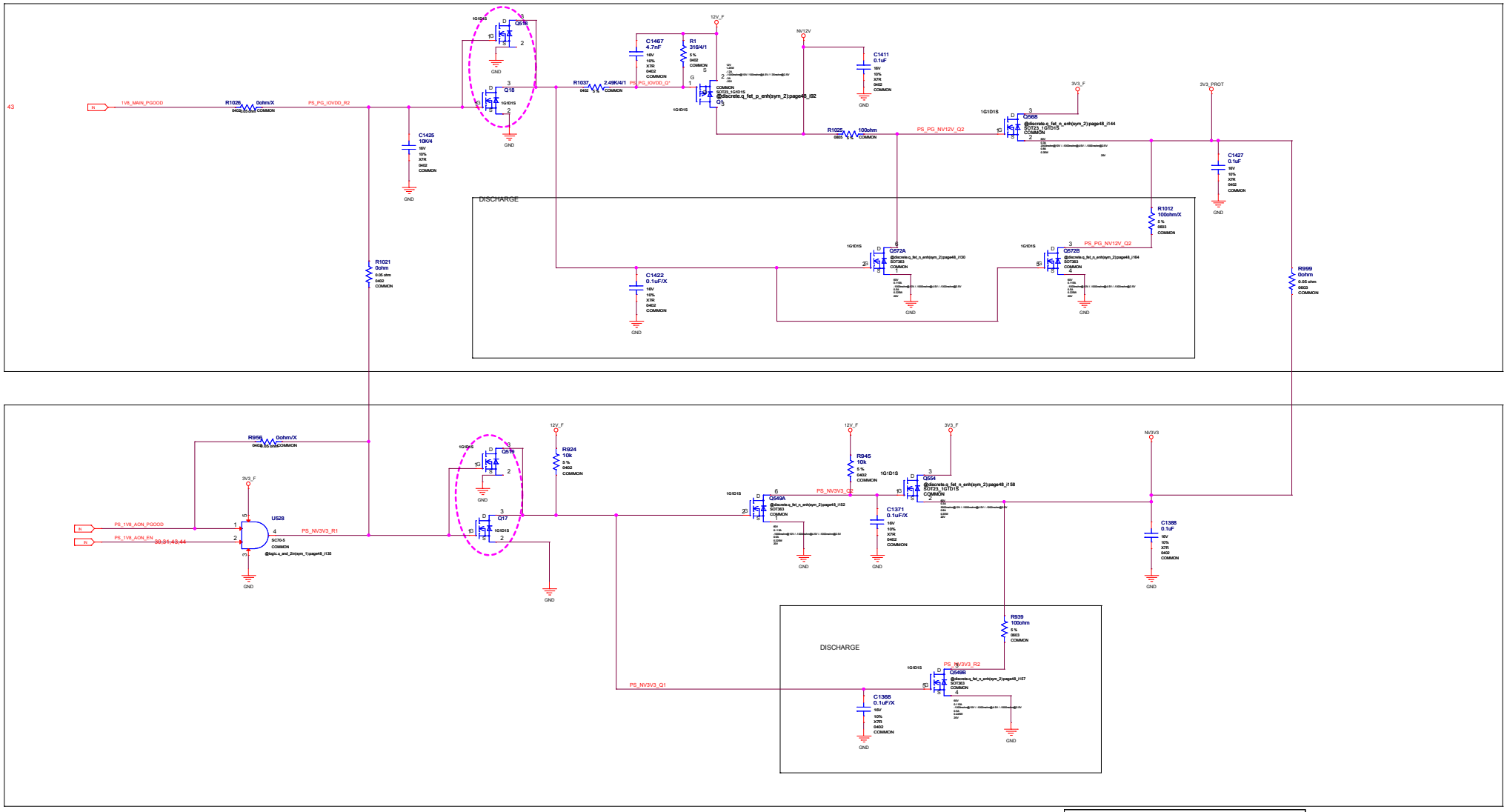
Page46:NV3V3, NV12V



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NV3V3, NV12V

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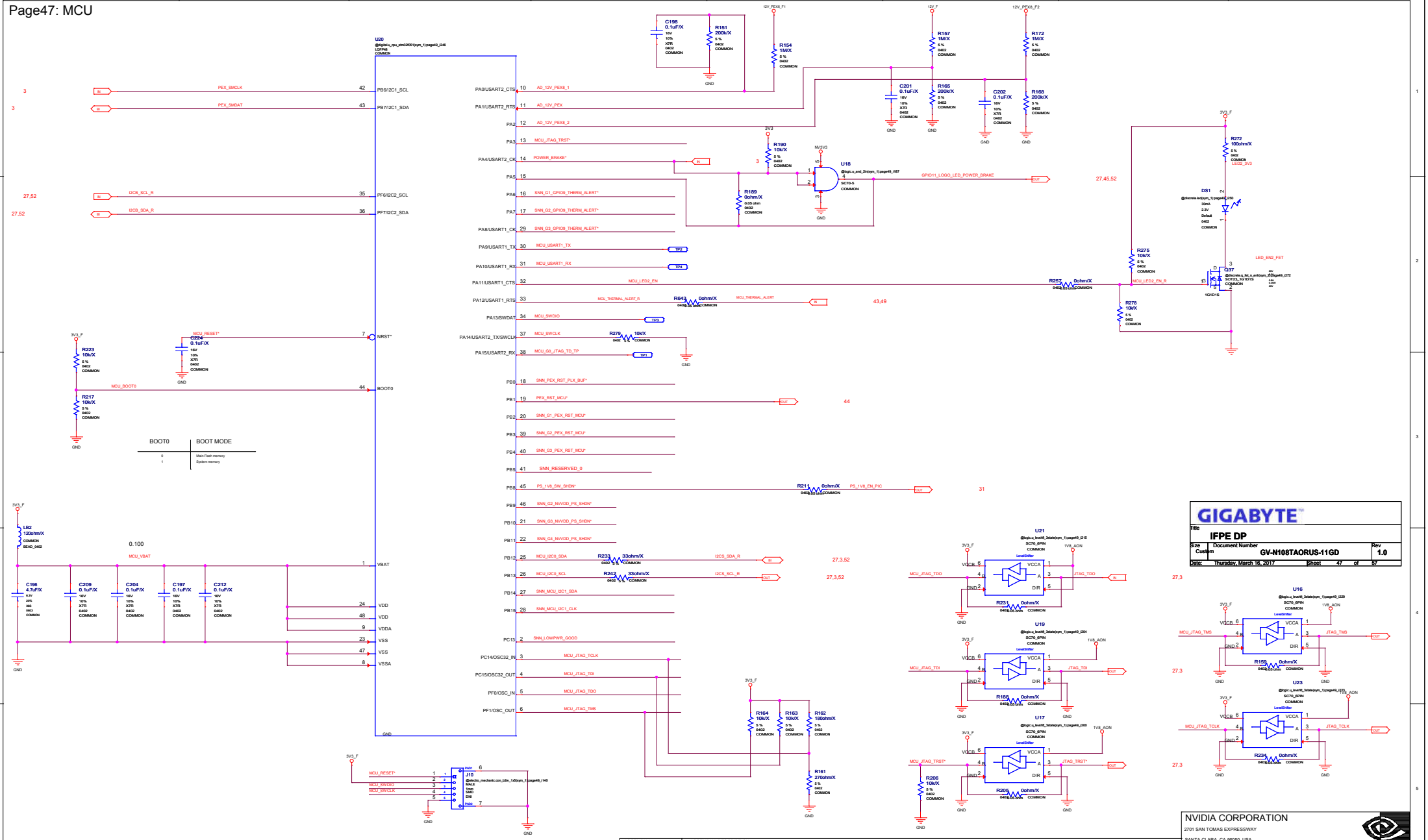
Page47: MCU



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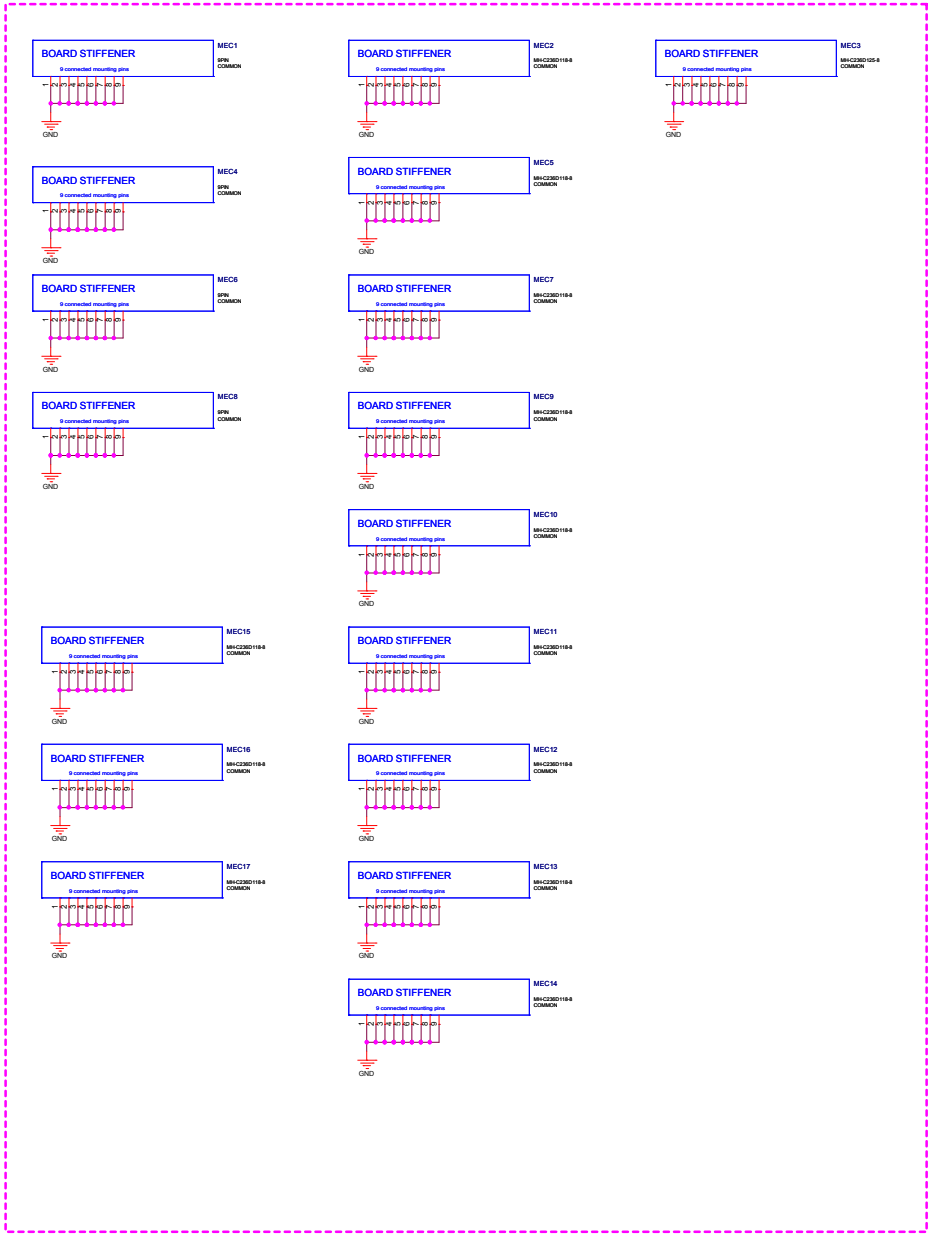
Page48: Mechanical: Bracket/Thermal Solution



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MECH

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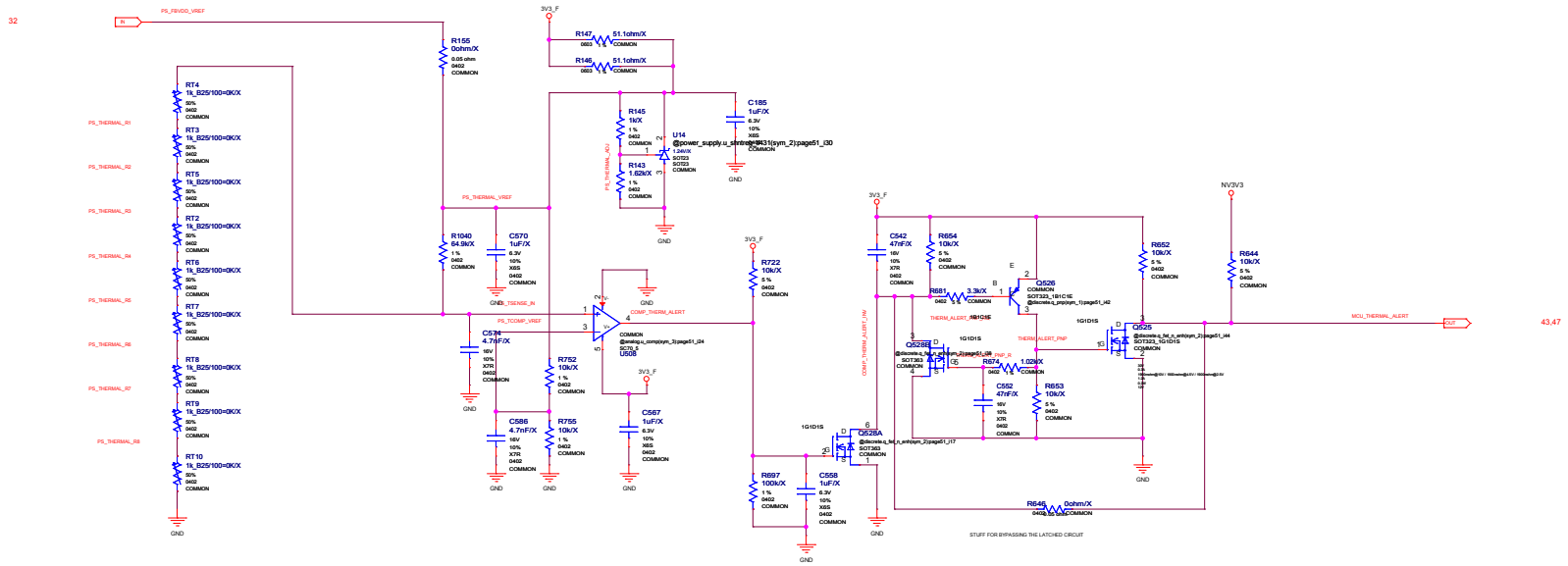
Page49: VR THERMAL PROTECTION



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	VR Thermal Protection

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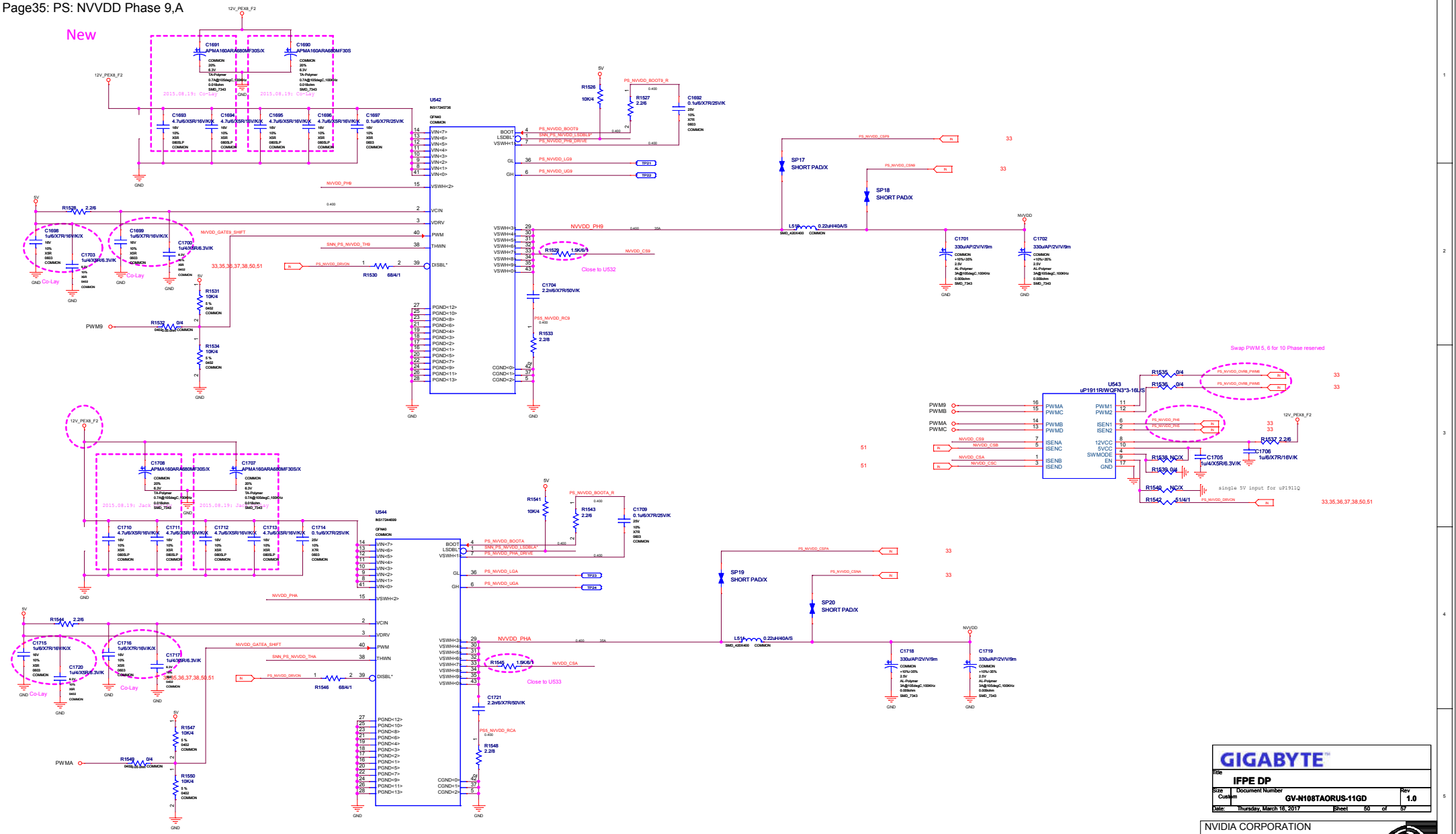
Page35: PS: NVVDD Phase 9,A

New



CO-LAYOUT: CHOOSE UA OR UB

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD Dynamic Switch Phases

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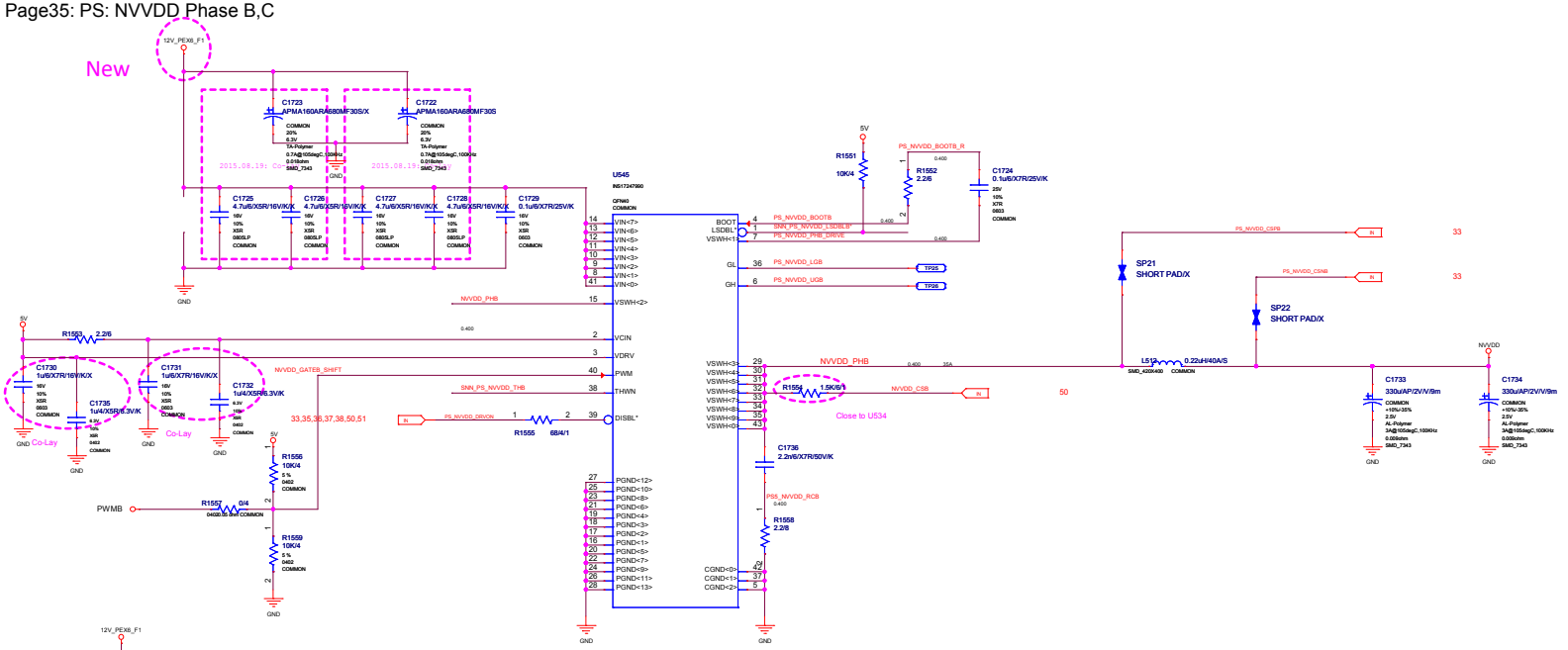
Page35: PS: NVVDD Phase B,C



CO-LAYOUT: CHOOSE UA OR UB

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD Dynamic Switch Phases

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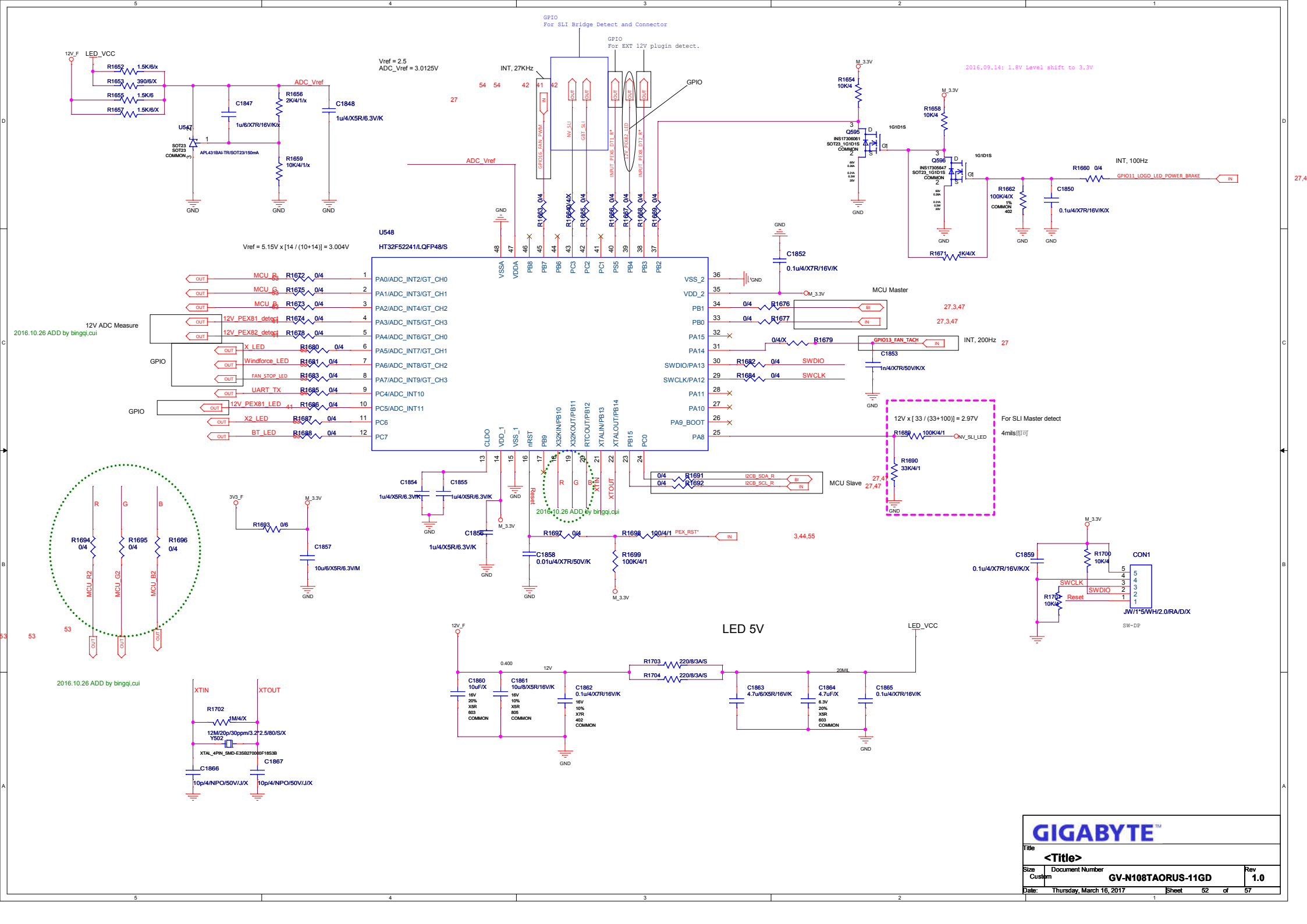

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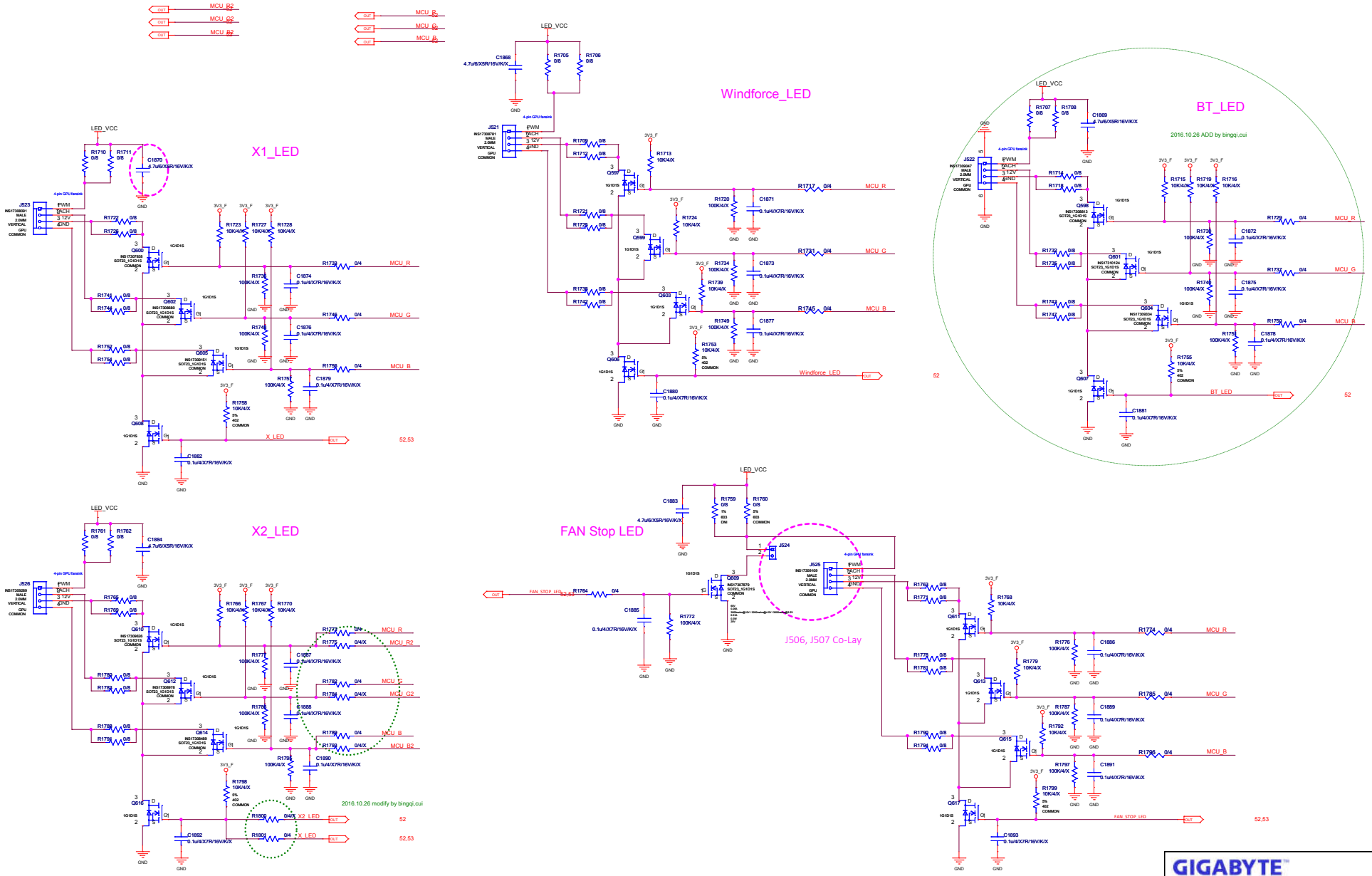

ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
MECH

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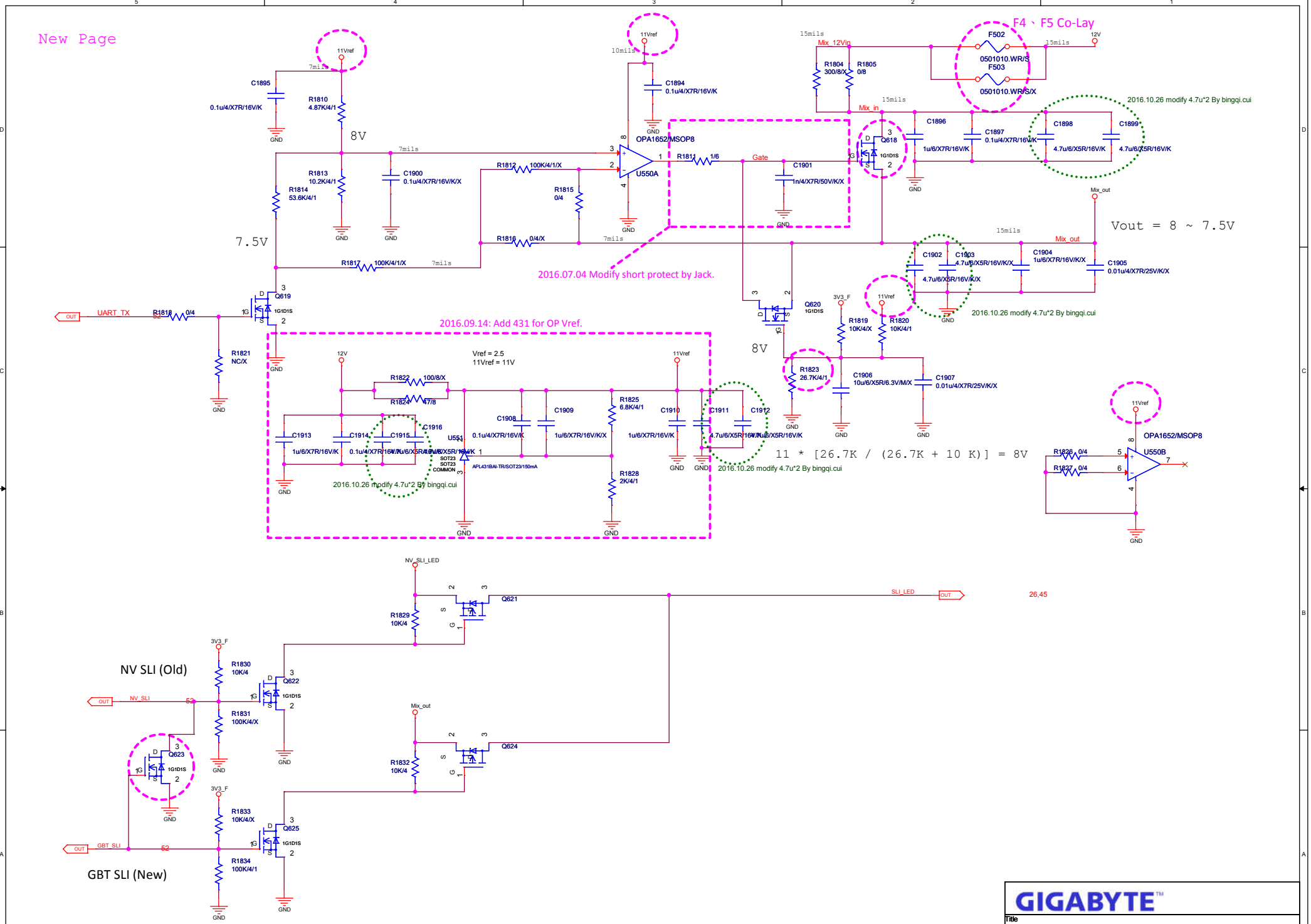

GIGABYTE™

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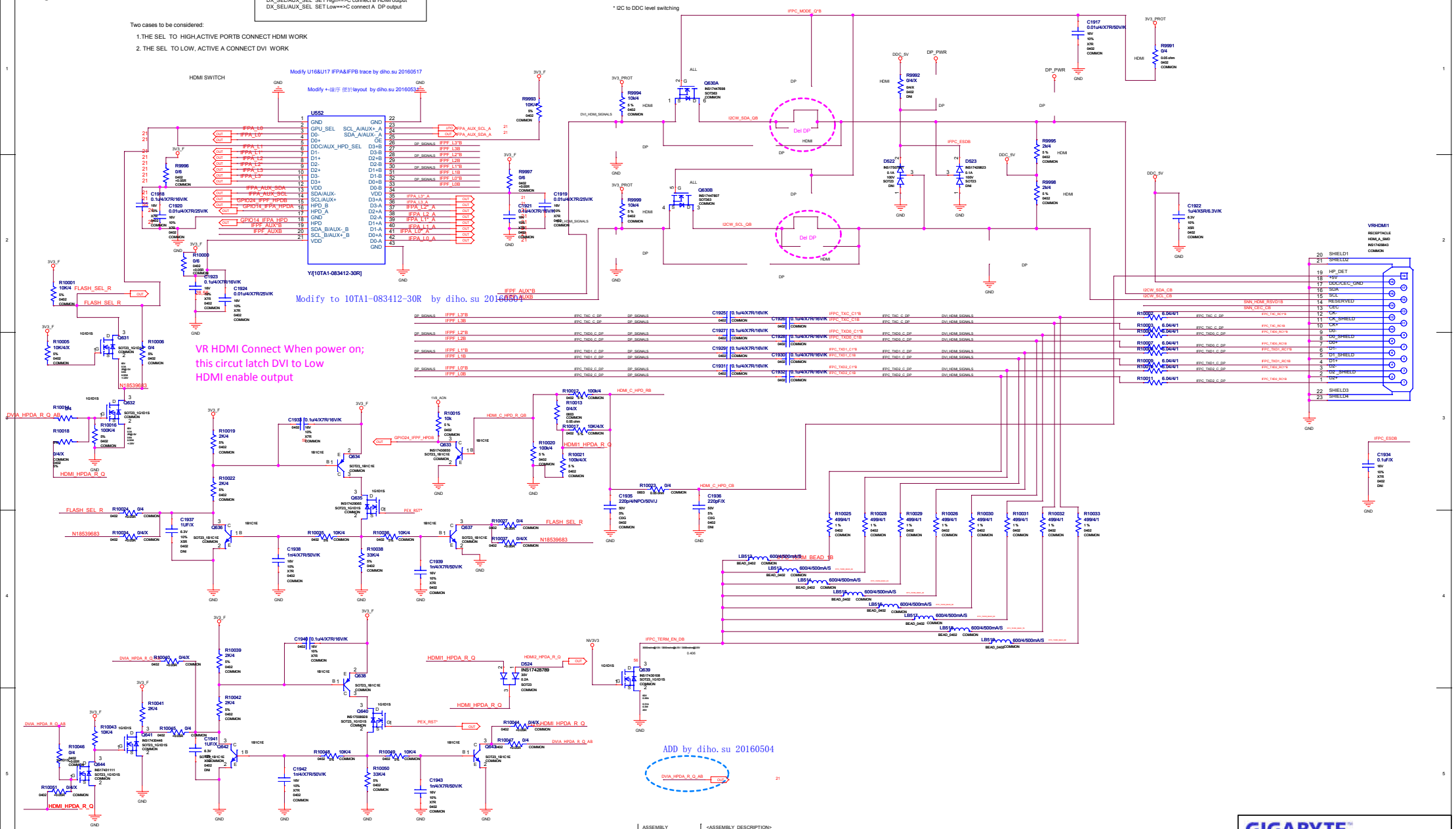
Page28: New VRHDMI1/DPF

DX_SEL/AUX_SEL SET High==>C connect B HDMI output
DX_SEL/AUX_SEL SET Low==>C connect A DP output

Two cases to be considered:

1. THE SEL TO HIGH,ACTIVE PORTB CONNECT HDMI WORK
2. THE SEL TO LOW, ACTIVE A CONNECT DVI WORK



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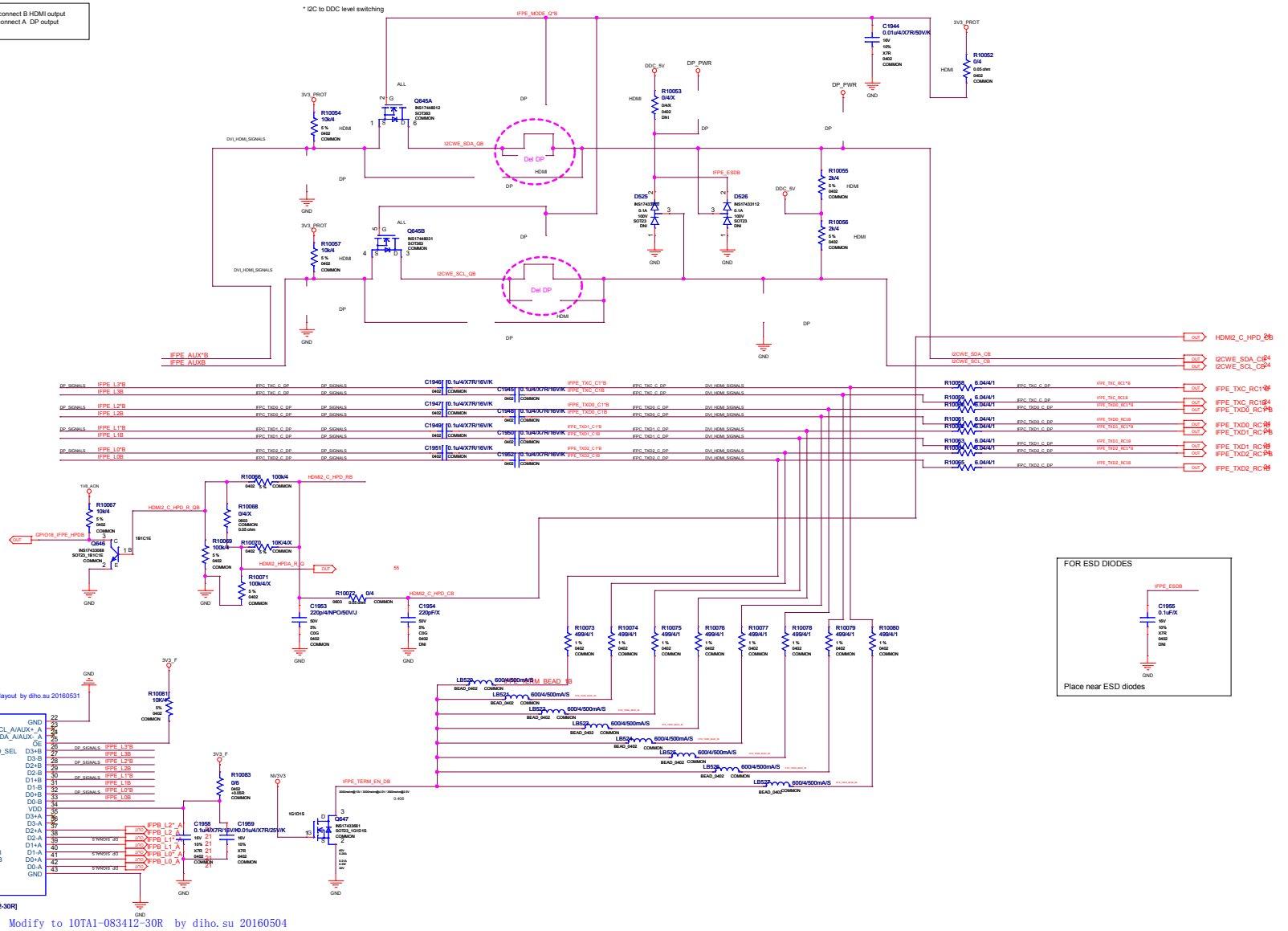
Page31: New VRHDMI2/DPE

DX_SEL/AUX_SEL SET High==>C connect B HDMI output
DX_SEL/AUX_SEL SET Low==>C connect A DP output



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History

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2017.03.01	First version