

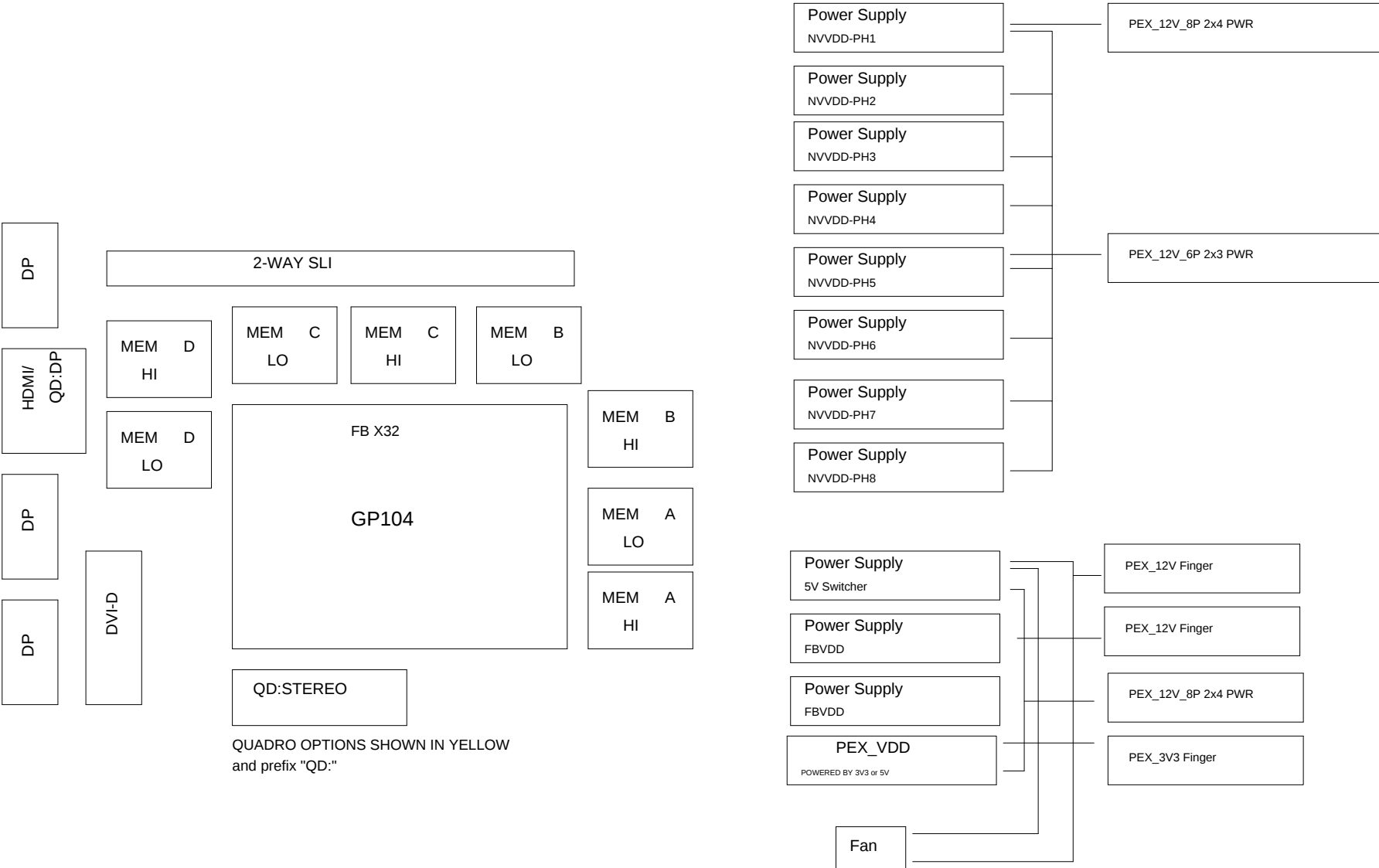
PG413 A00

GP104 - 8GB GDDR5X, 256b, 256Mx32
Tall DVI-D + DP + DP + DP/HDMI + DP

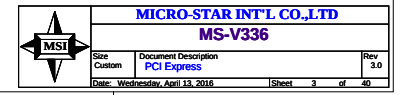
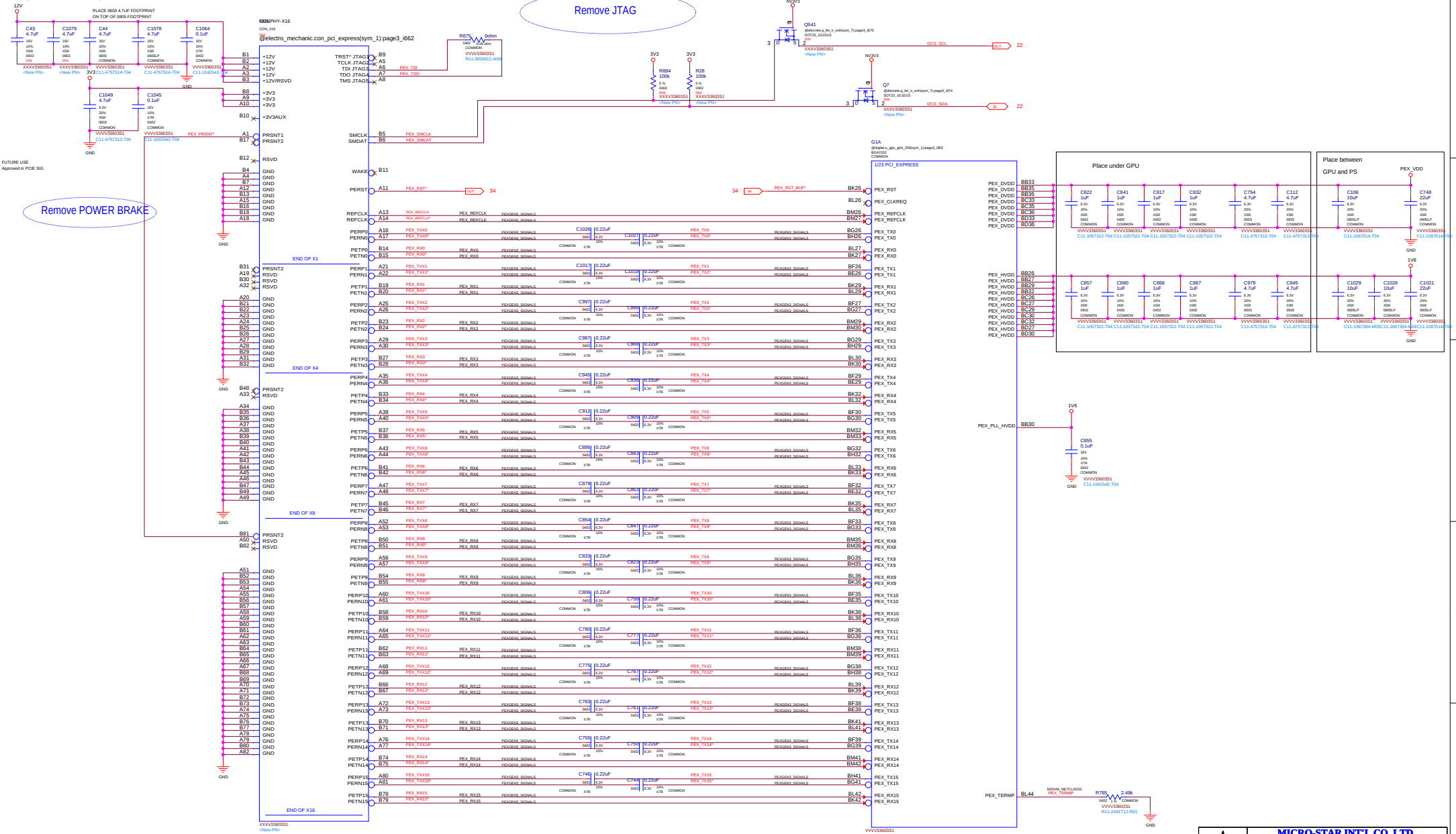
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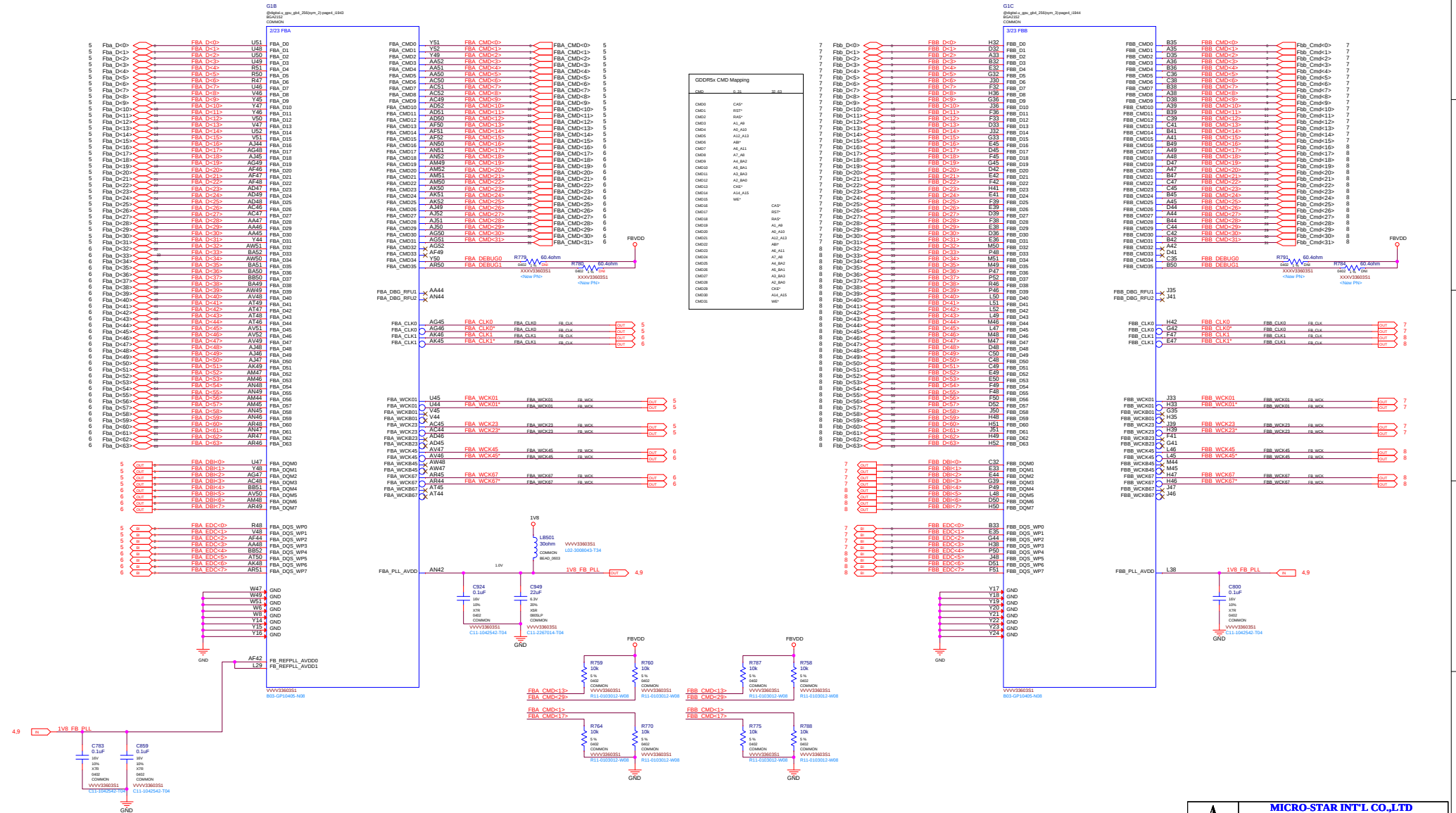
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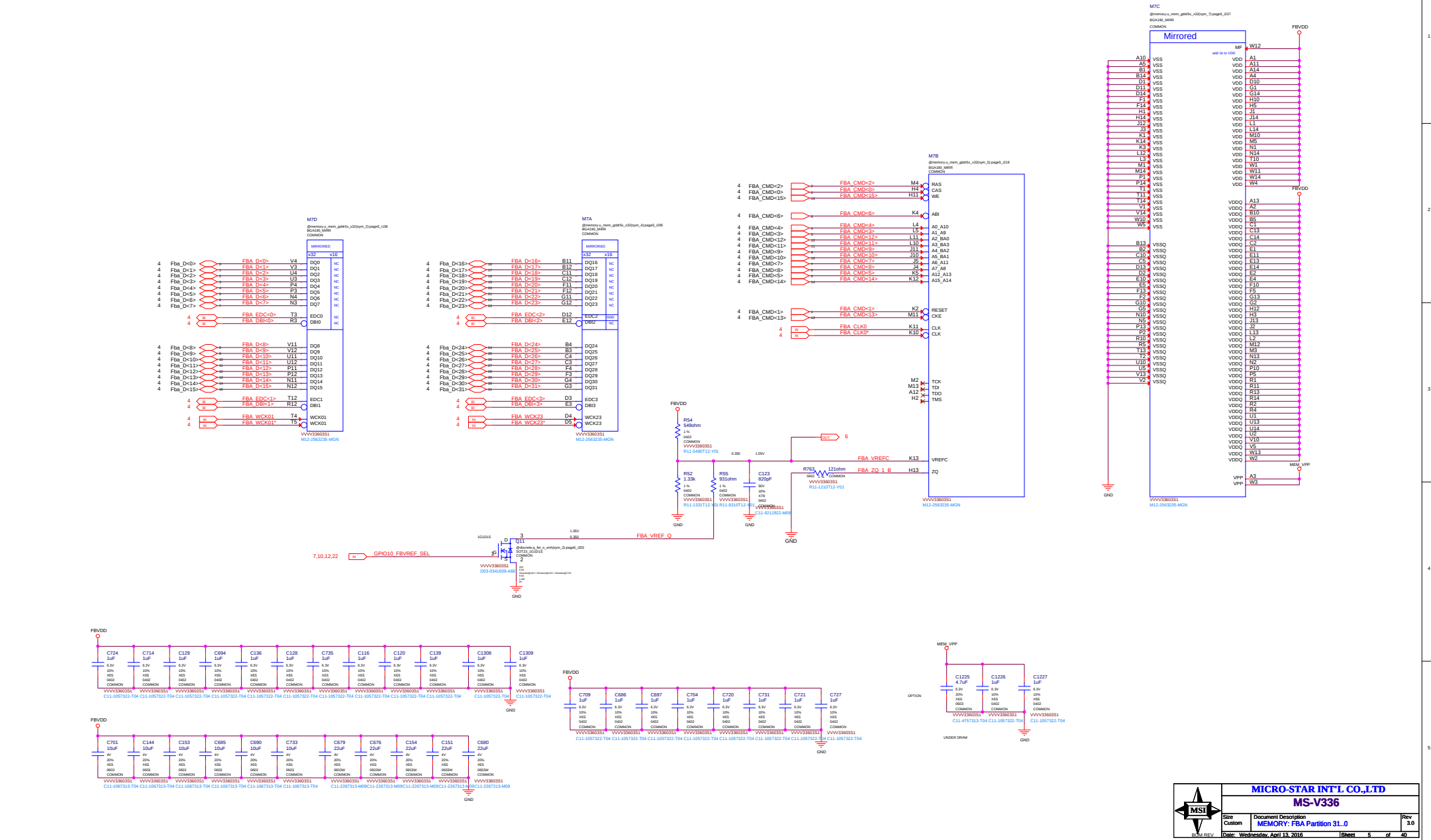
Page	Description
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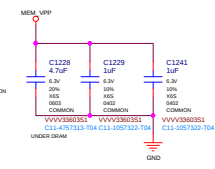
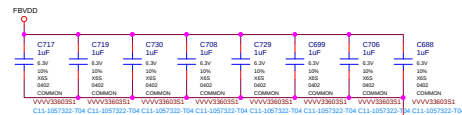
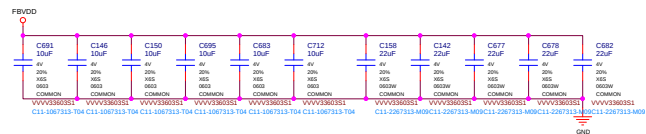
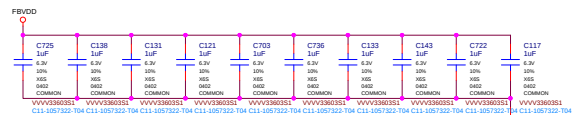
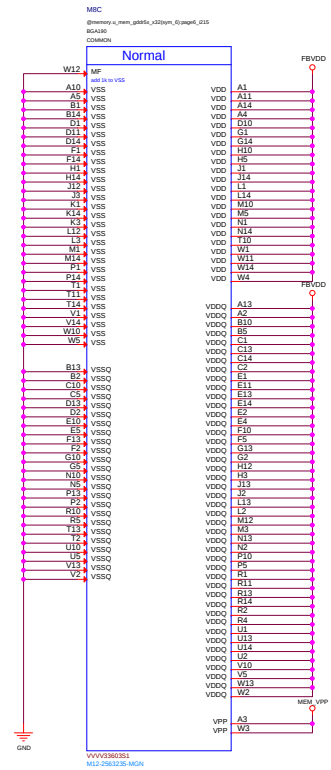
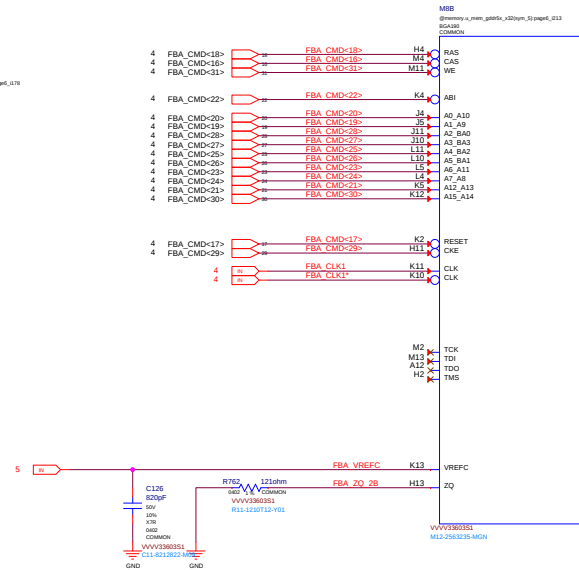
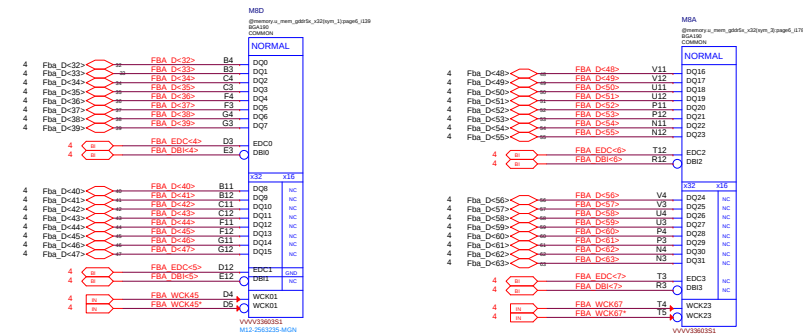


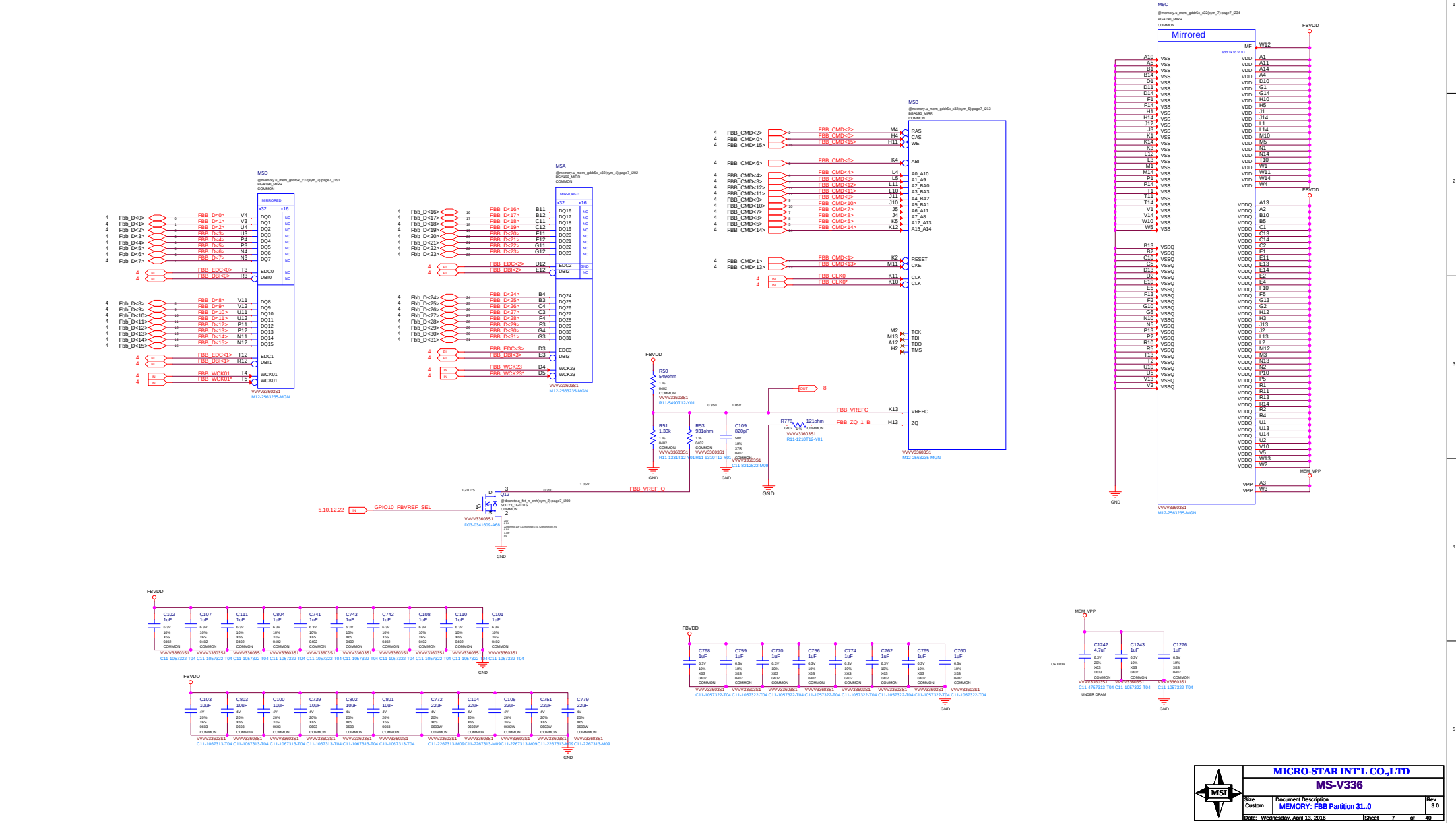
Page3: PCI Express

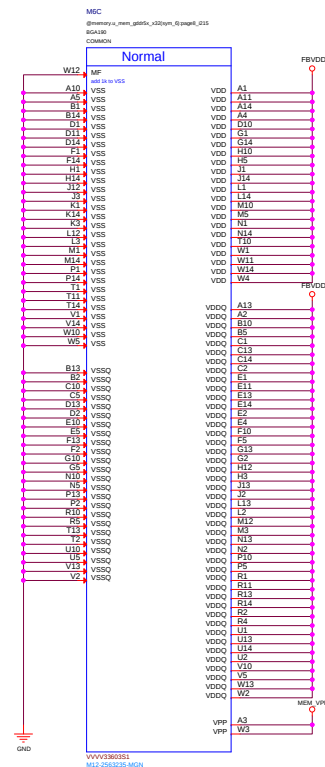
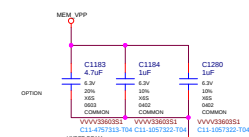
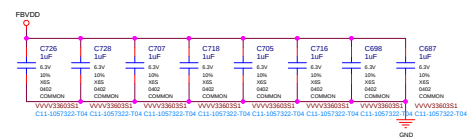
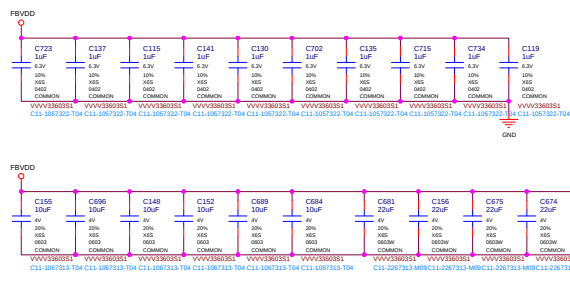
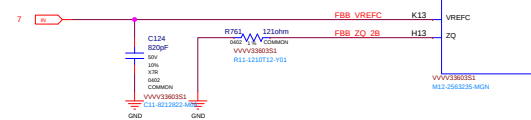
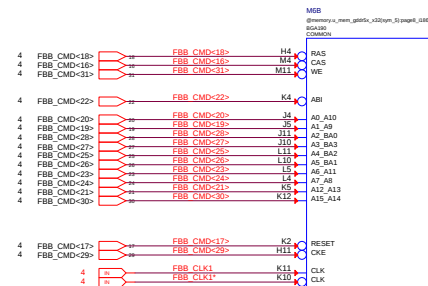
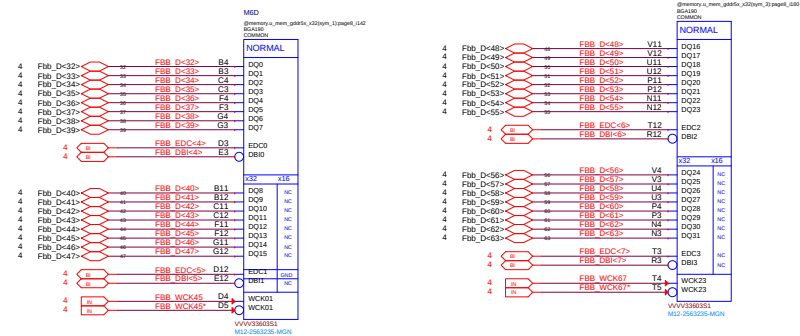


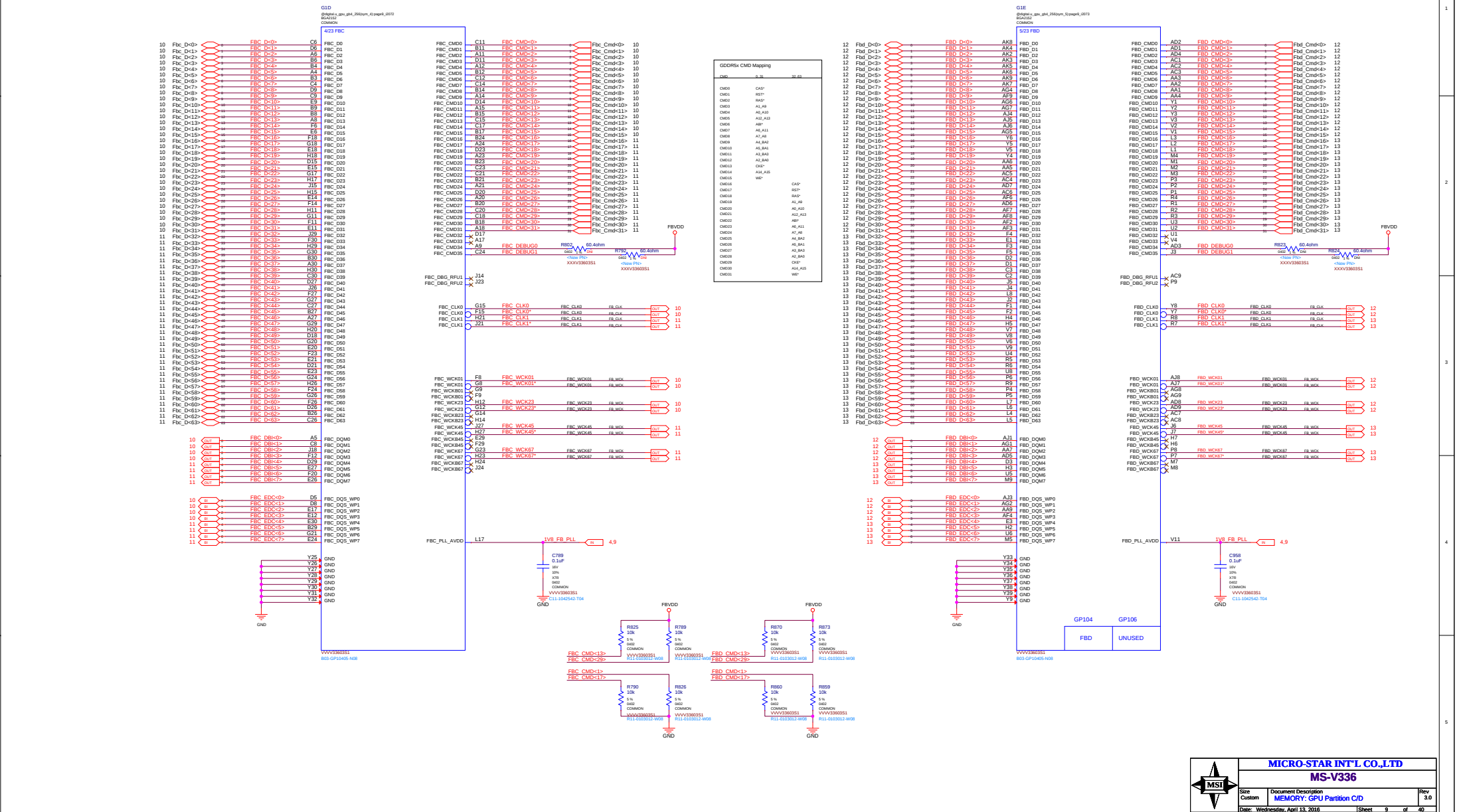


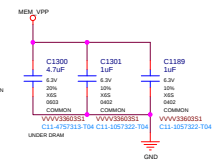
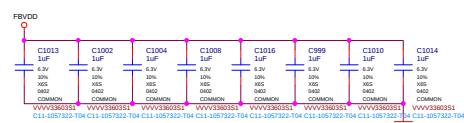
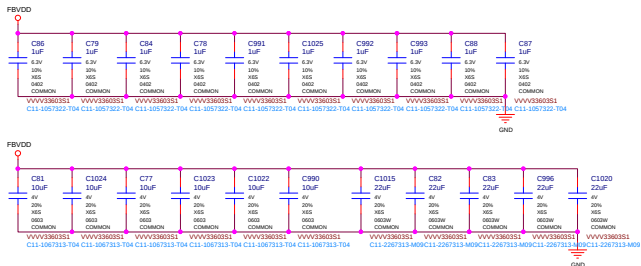
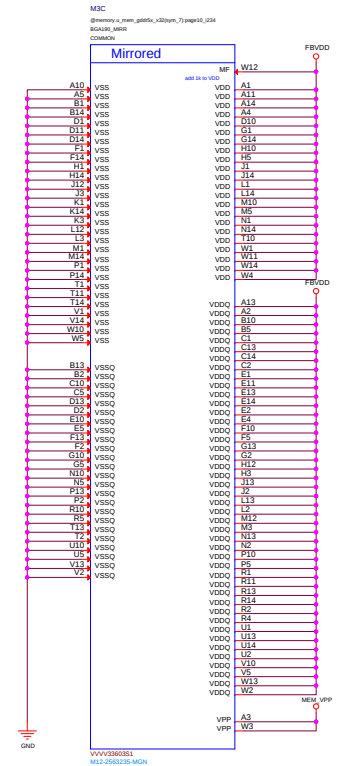
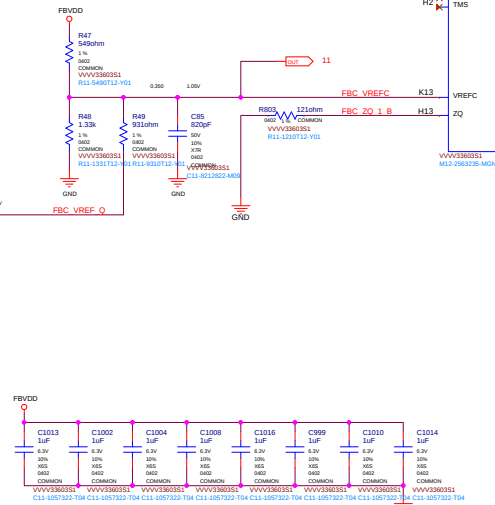
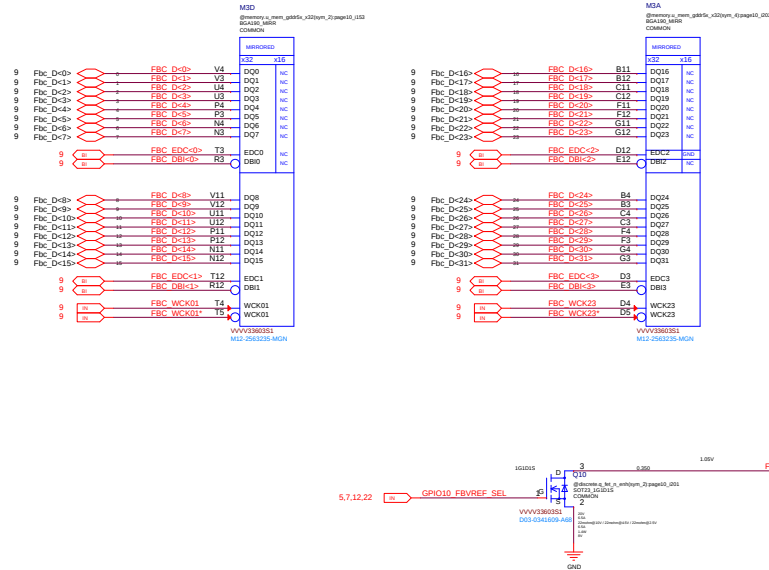


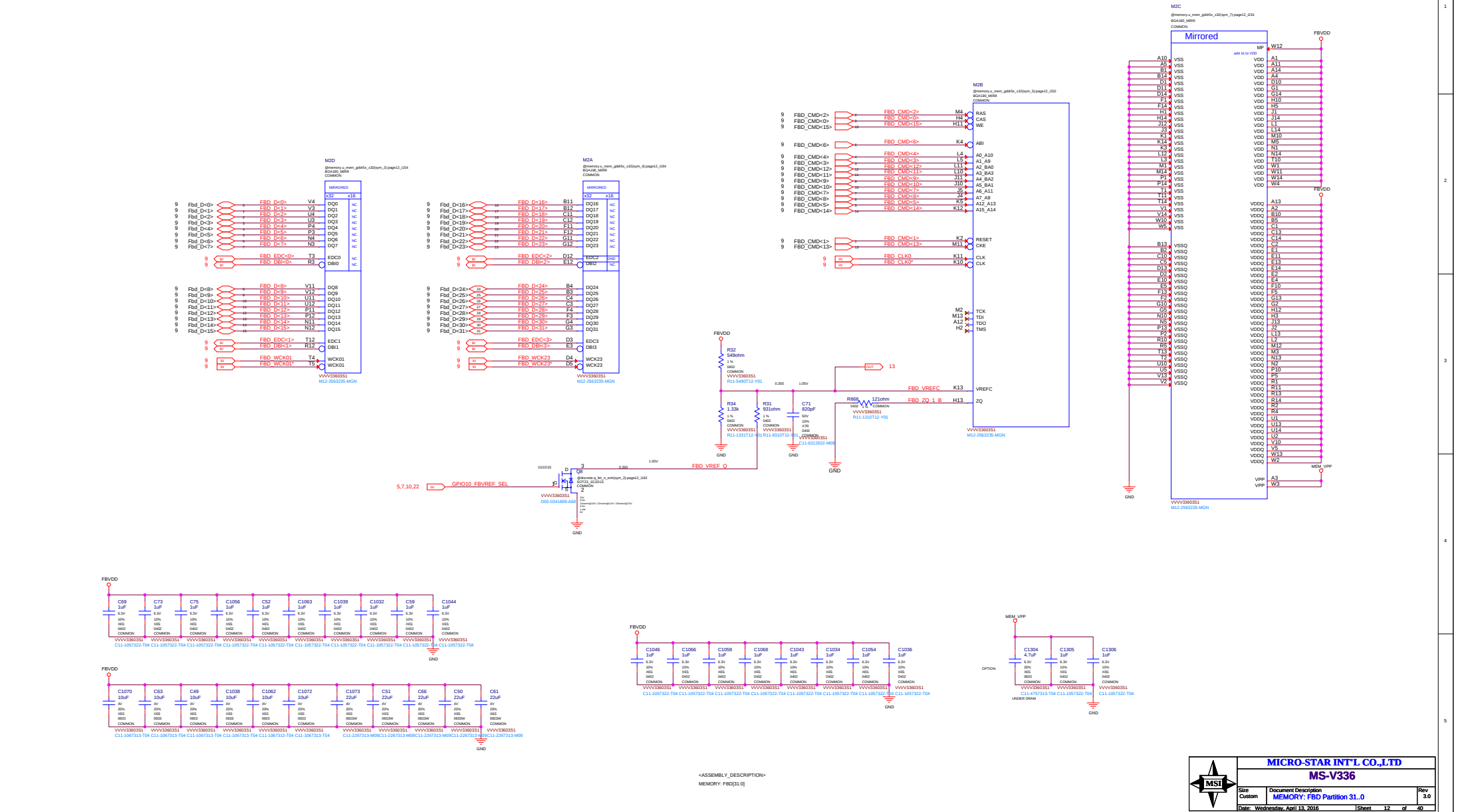


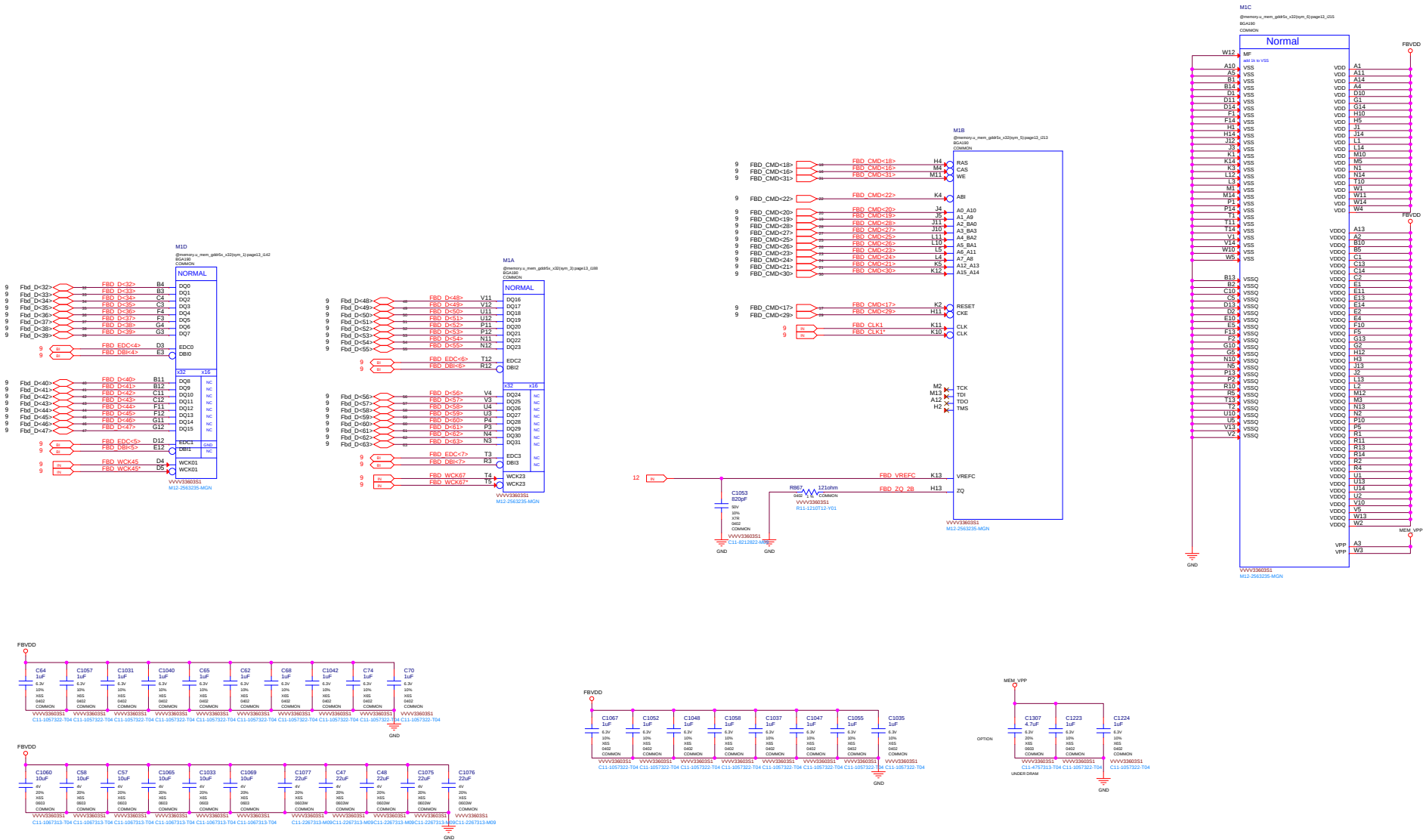


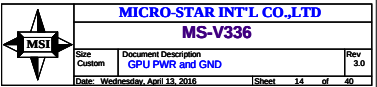




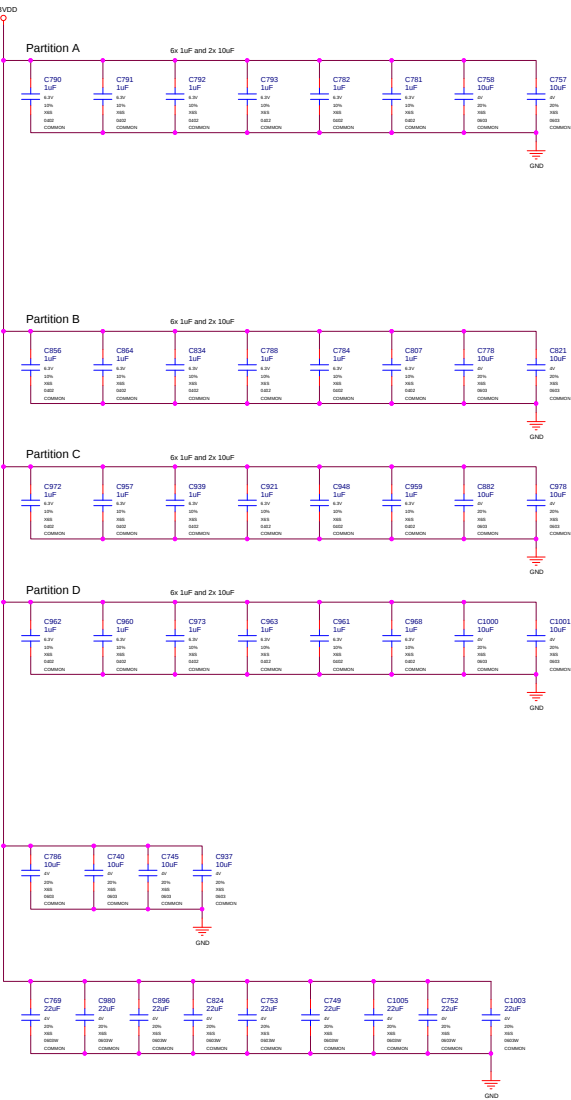




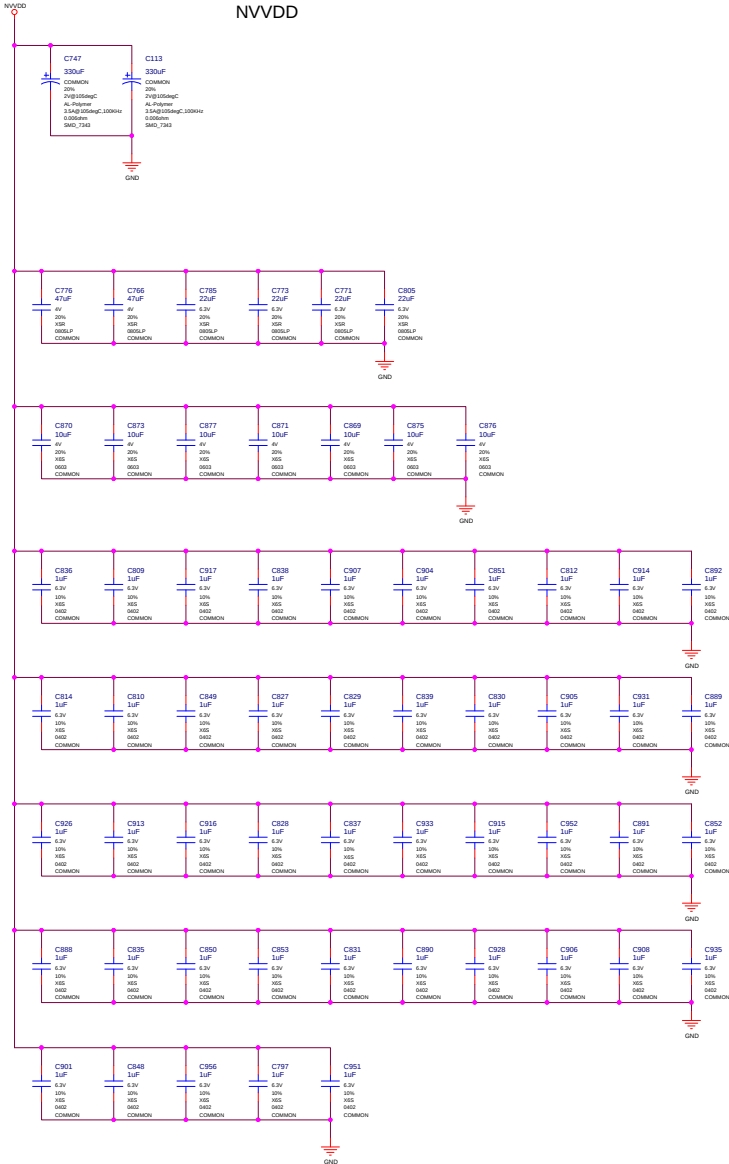




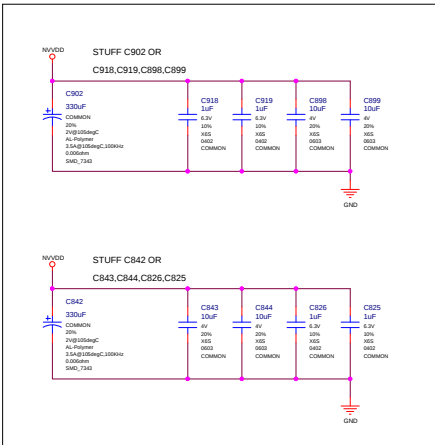
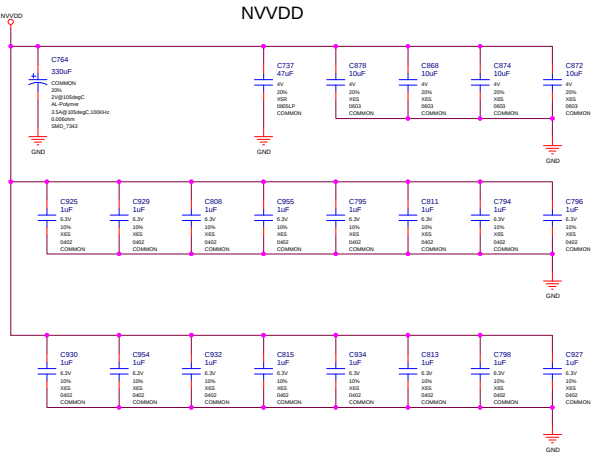
FBVDD



NVVD

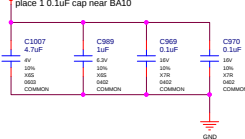


NVVD

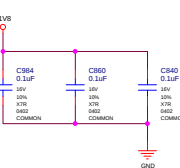


1V8_AON

place 10.1uF cap near BA10

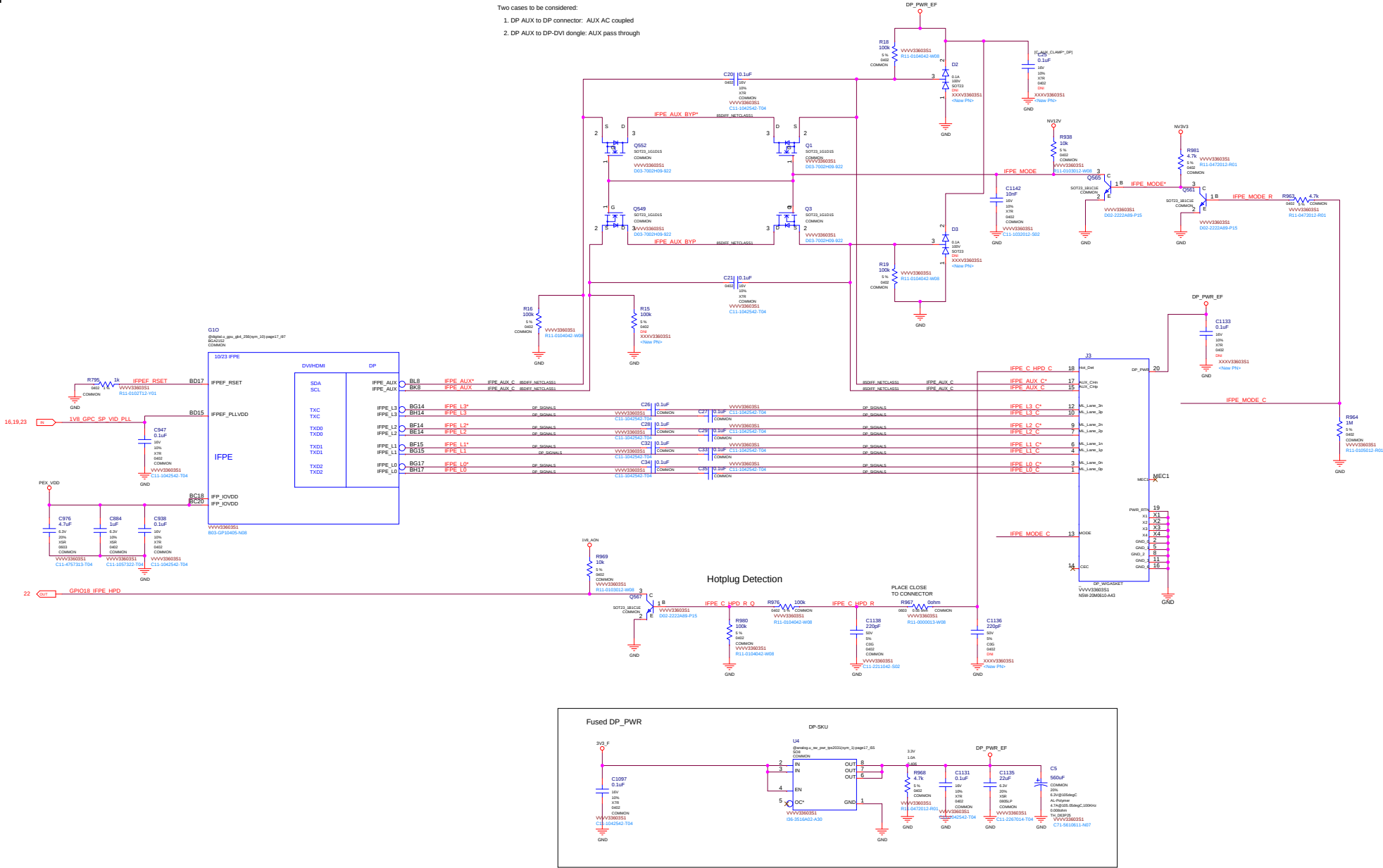


VDD18

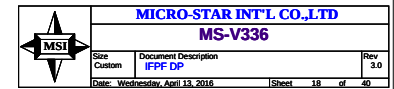


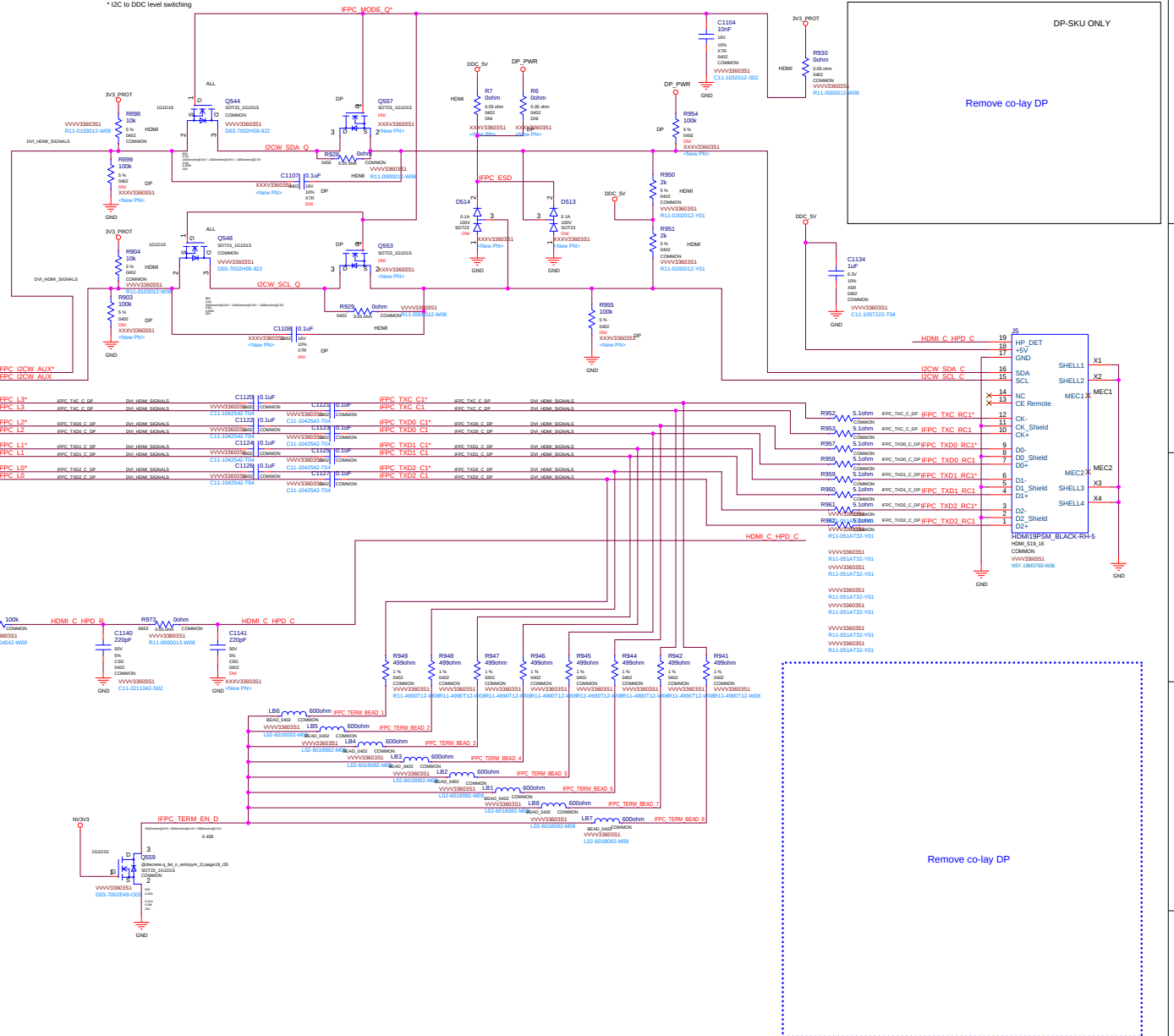
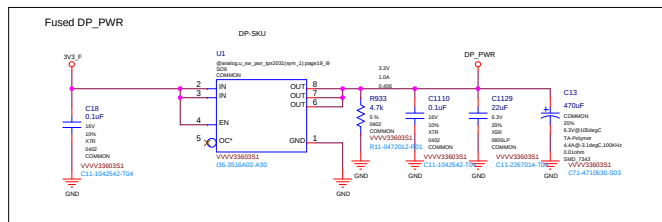
place 10.1uF cap for BB14 and BC14 to share

- Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through

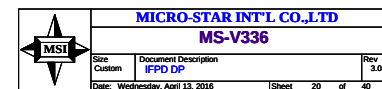
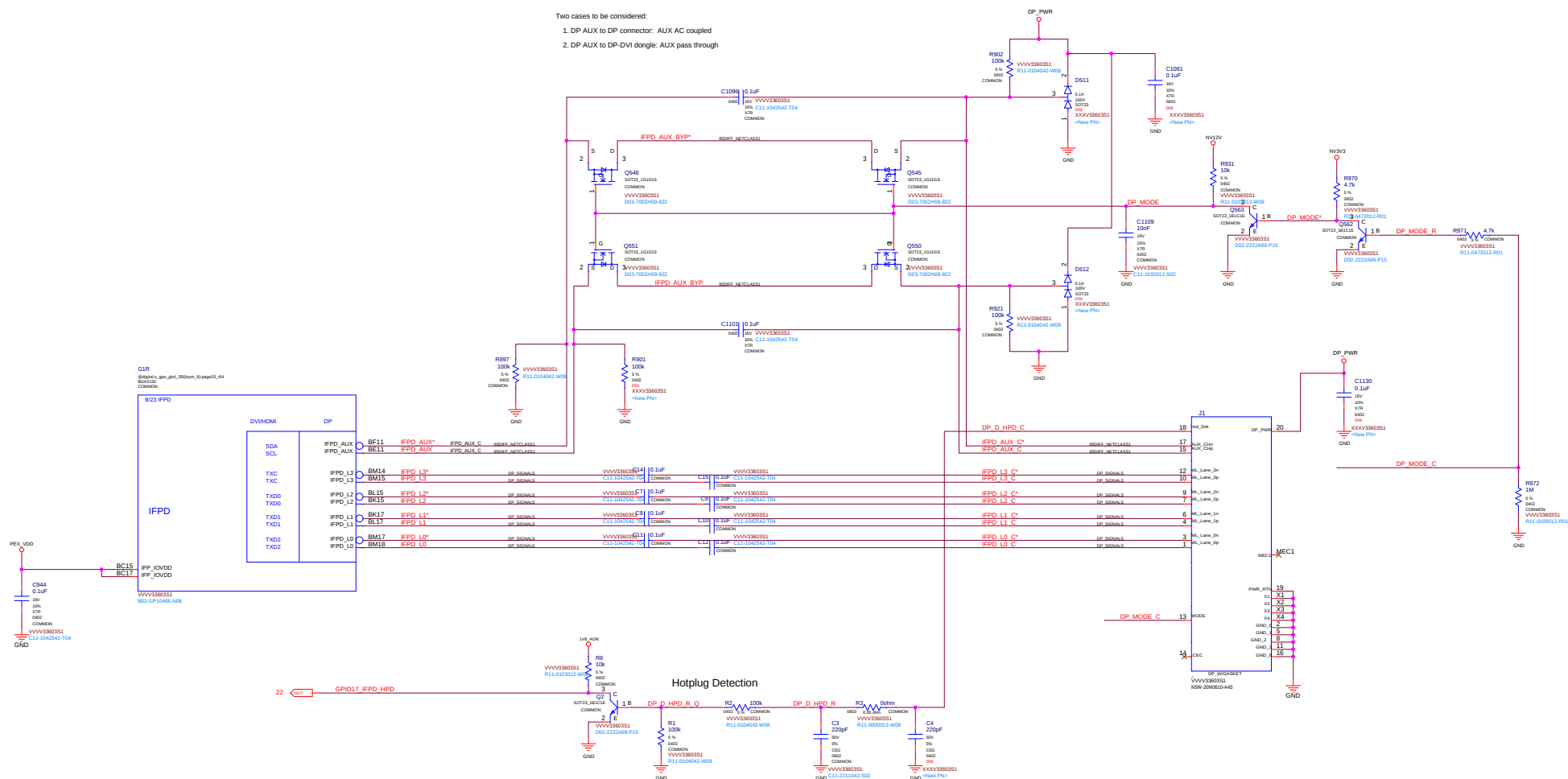


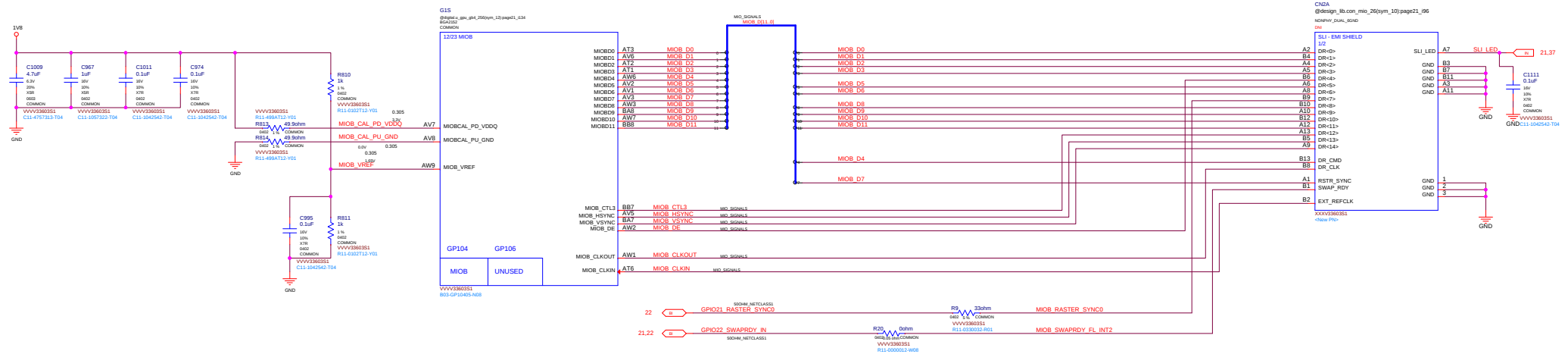
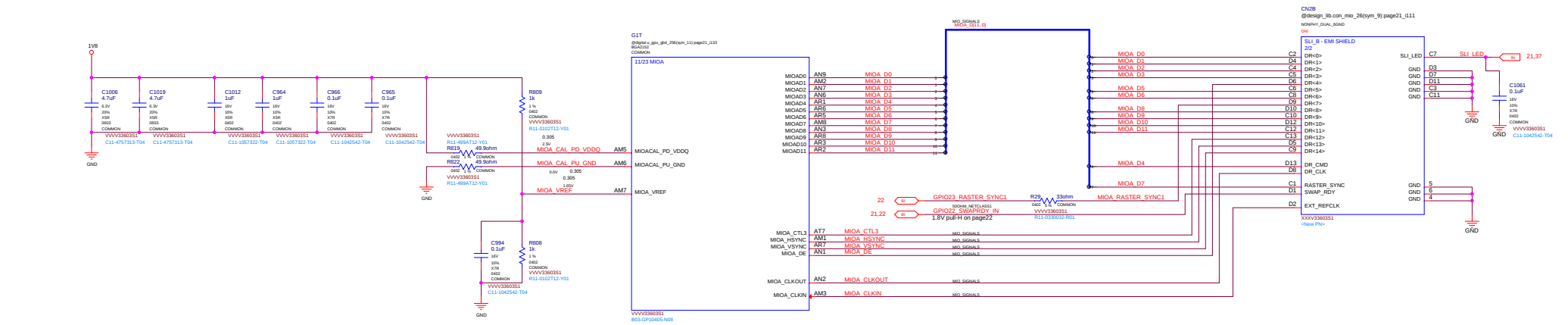
1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through

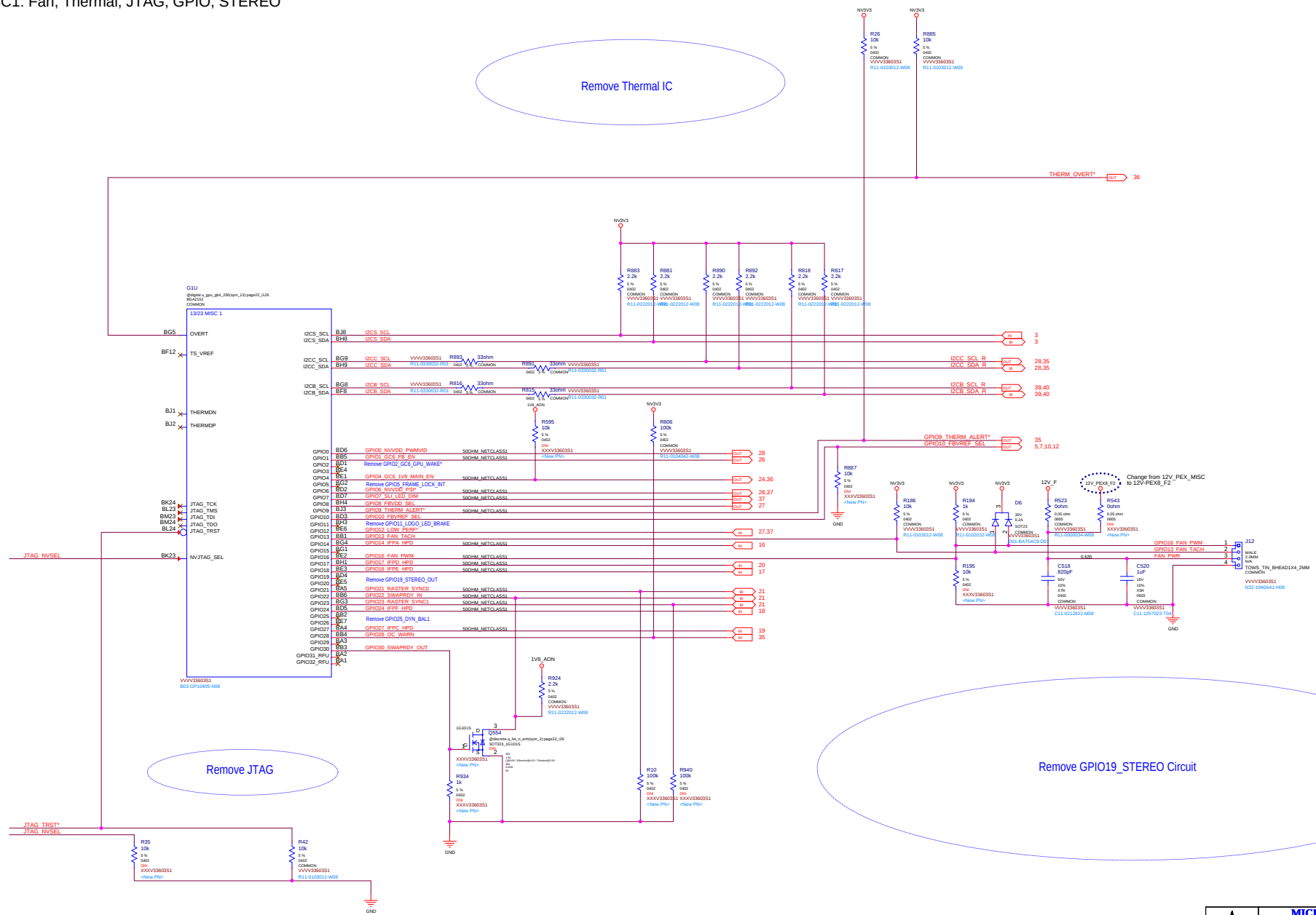




1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through







STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

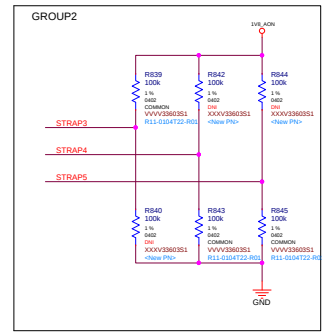
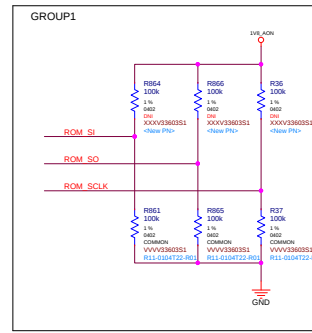
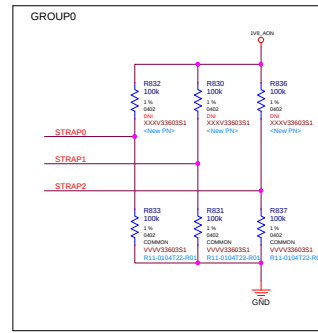
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

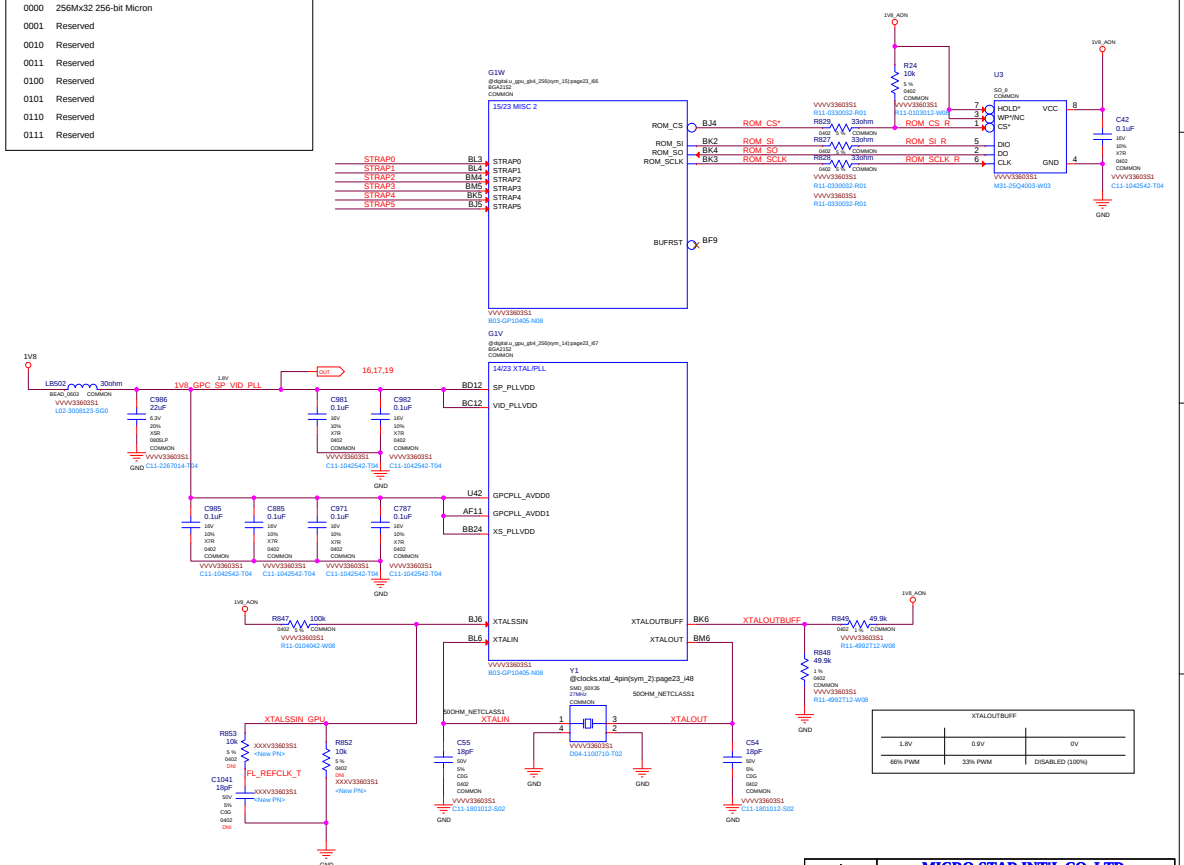
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

```
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE
```

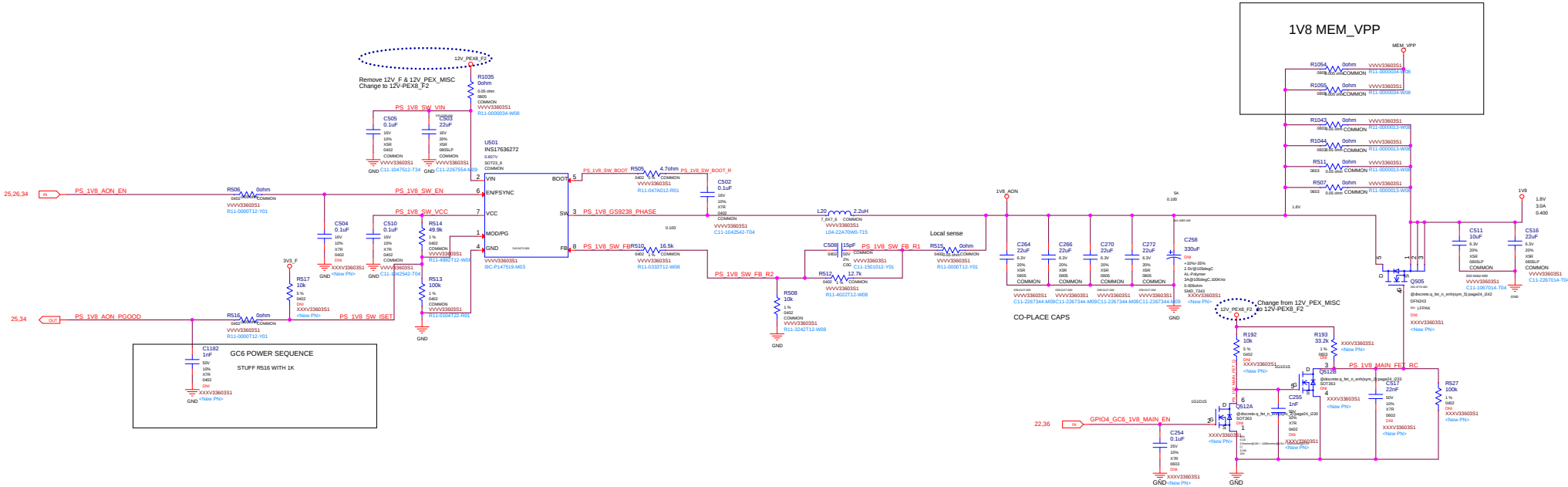


CFG[3:0] Config	Width	Vendor
0000	256Mx32	256-bit Micron
0001	Reserved	
0010	Reserved	
0011	Reserved	
0100	Reserved	
0101	Reserved	
0110	Reserved	
0111	Reserved	

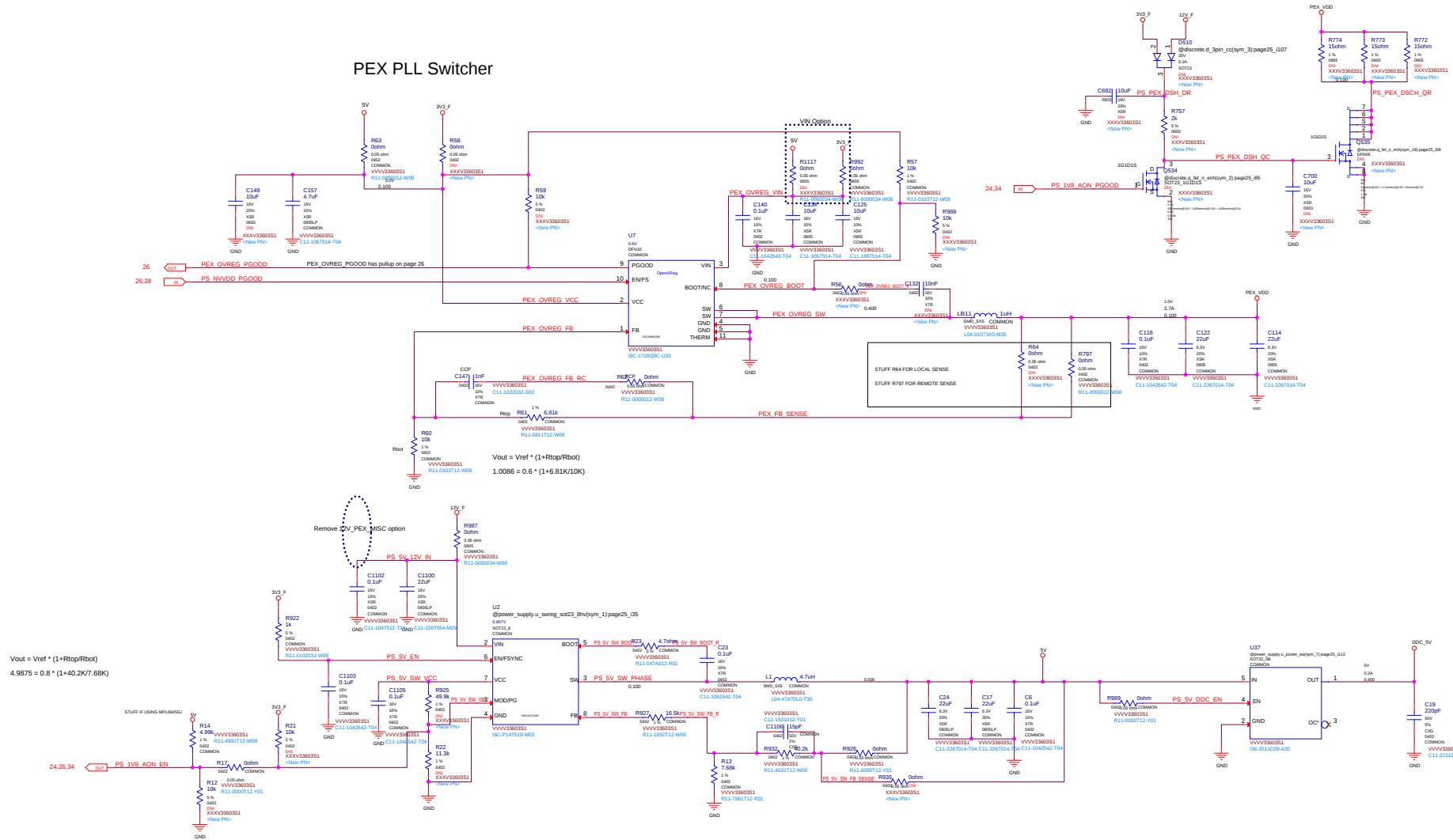


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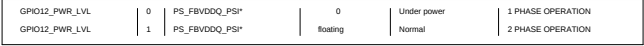
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PEX PLL Switcher





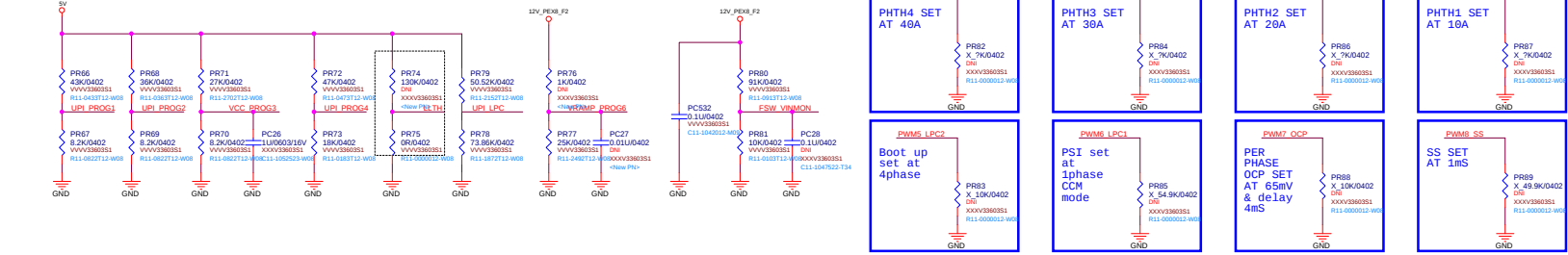
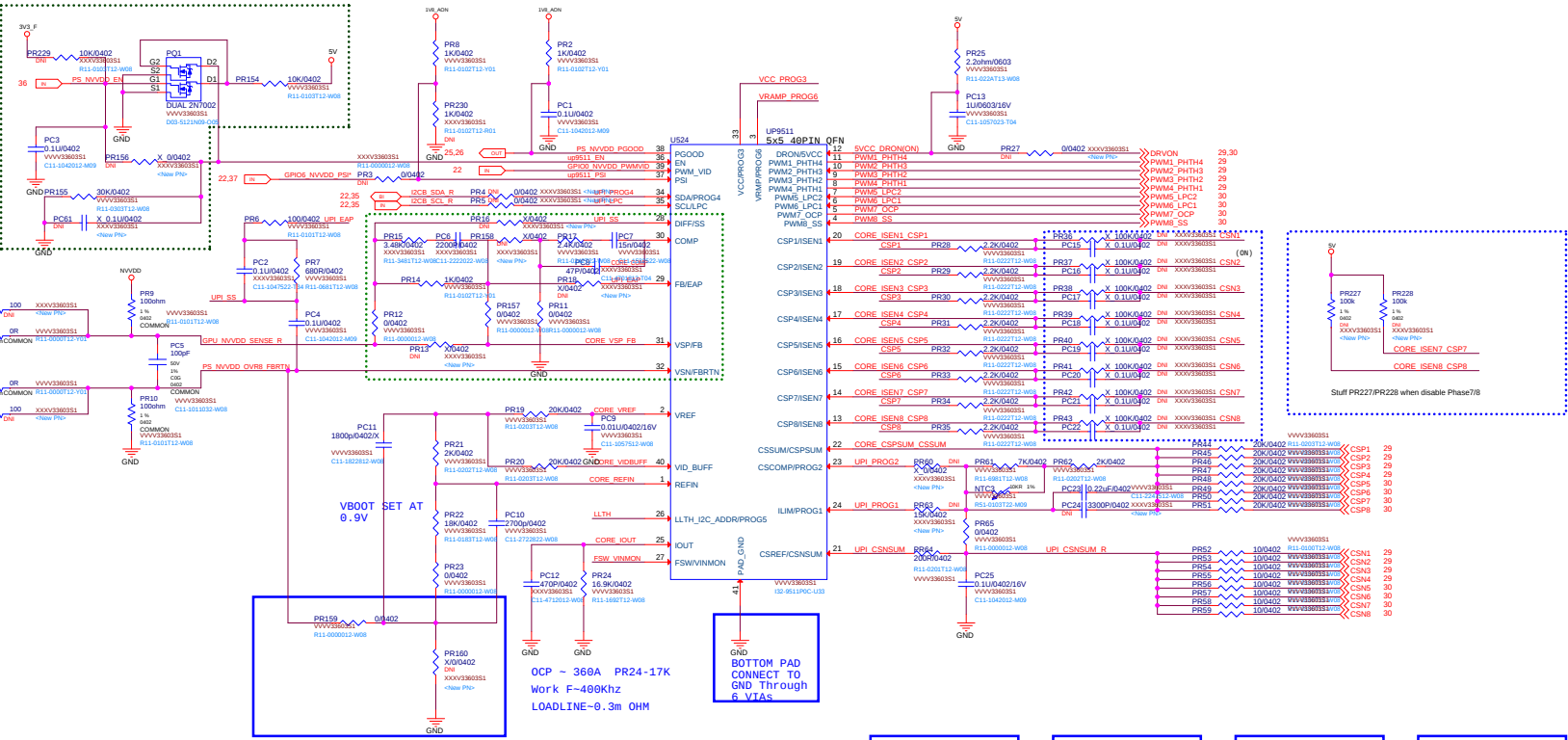


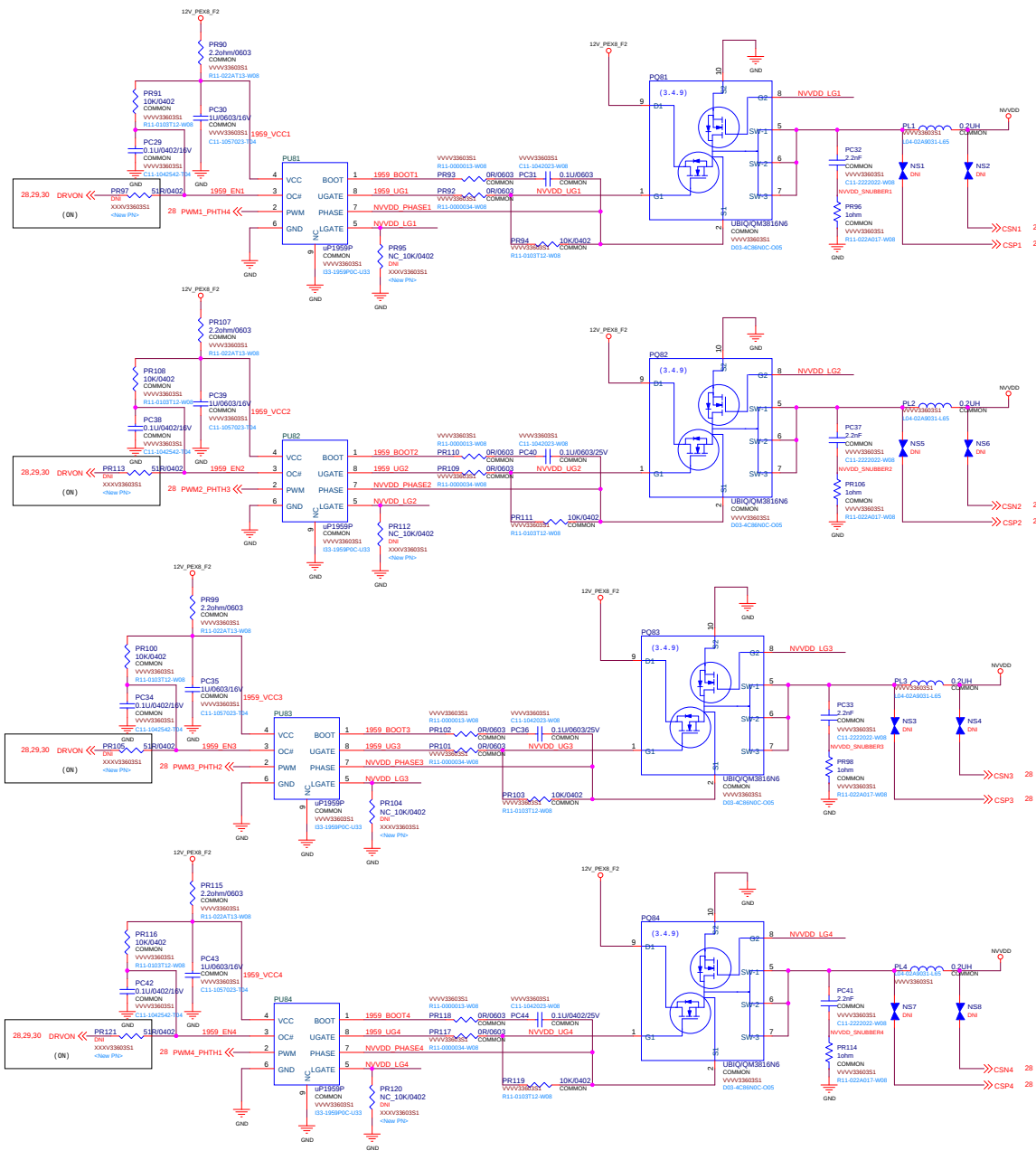
```
GPIOB = 1 FBVDDQV = 1.383V
GPIOB = 0 FBVDDQV = 1.503V

VID = 1 SHORTS RSET AND FBRTN
VREFN = VREF X ((R2/R1R2)) / (R1+R2/R1R2))
VREFN = 2.0 X (4.99/14.33) / (1.65+4.99/14.33)
VREFN = 1.363V

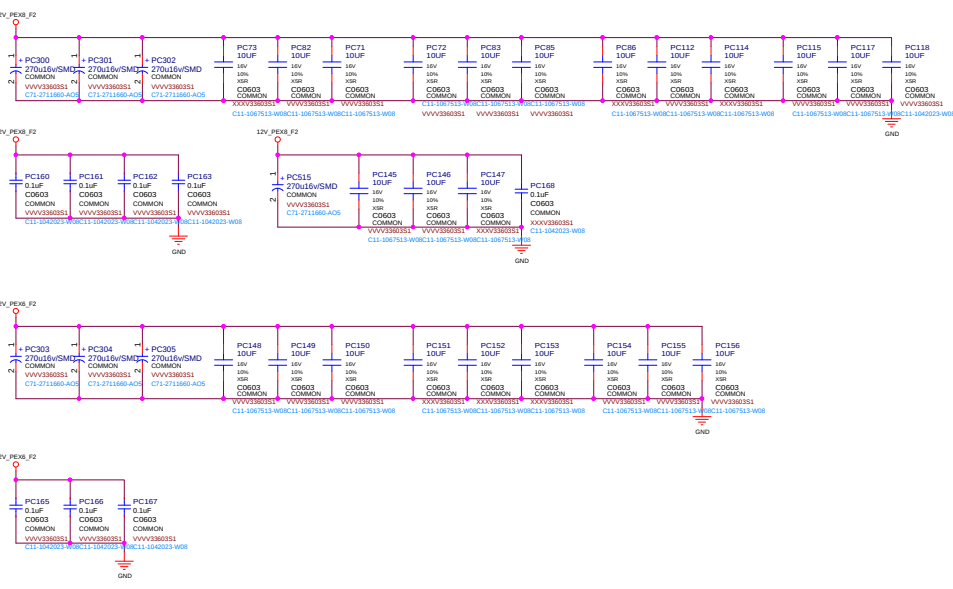
VID = 0 DISCONNECTS RSET AND FBRTN
VREFN = VREF X (R2 / (R1+R2))
VREFN = 2.0 X .59 / (1.65+.59)
VREFN = 1.502V
```

default not stuff

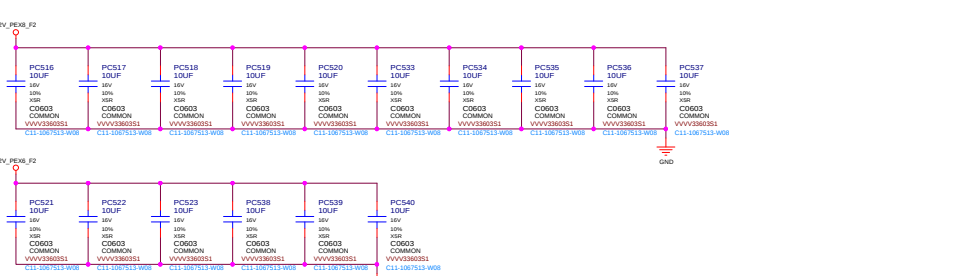


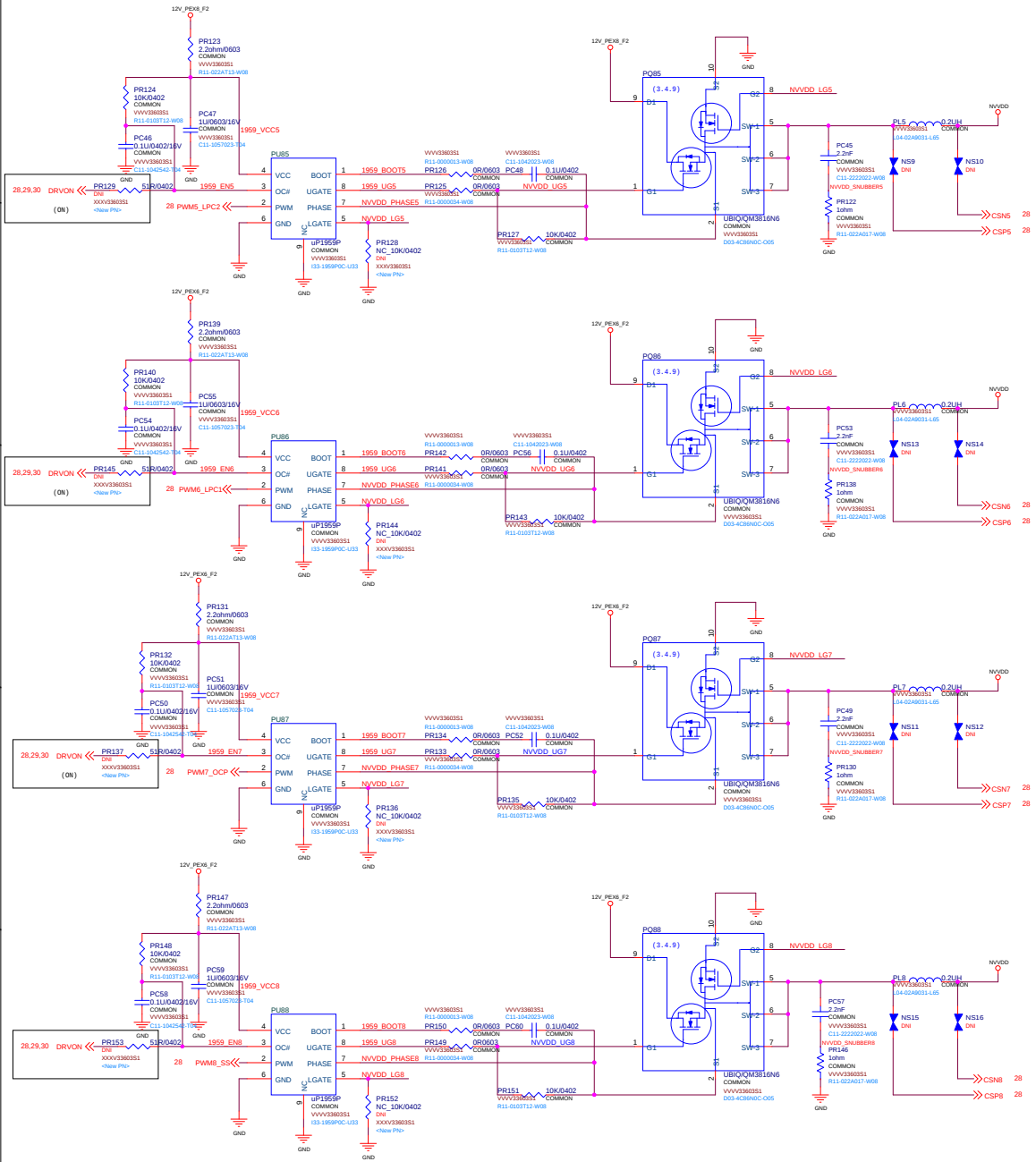


EXT_12V Input CAP

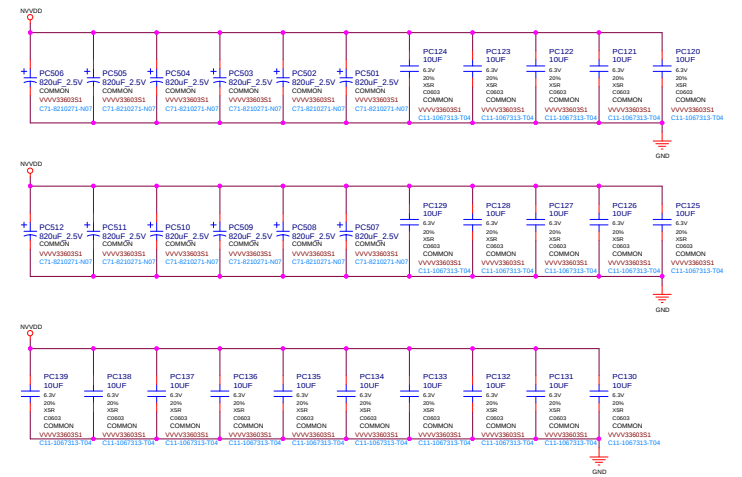


EXT_12V Input CAP(Backup)





NVDD Output CAP



1

2

3

4

5

1

2

3

4

5



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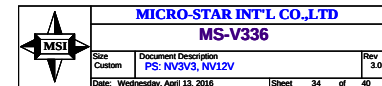
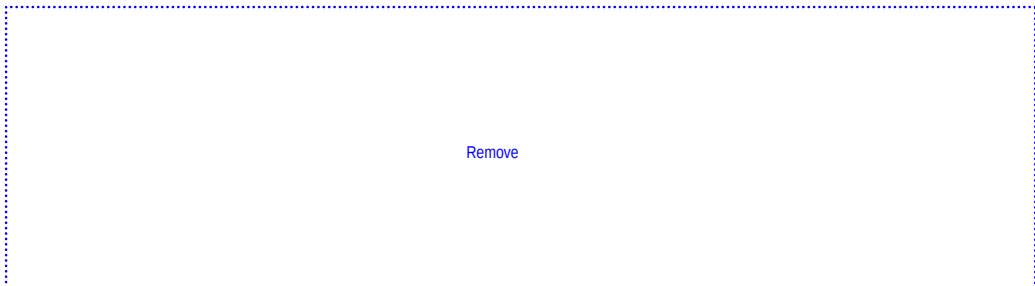
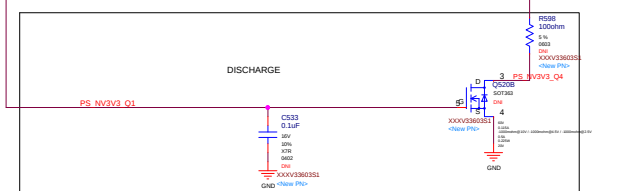
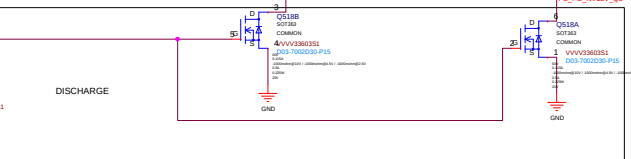
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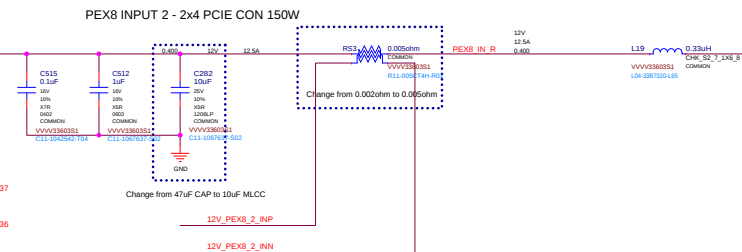
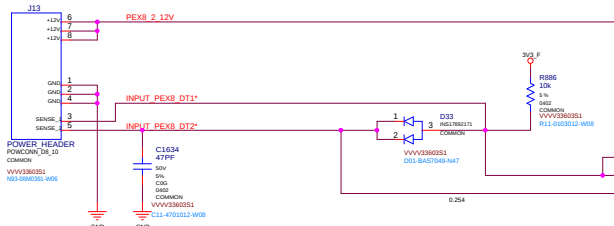
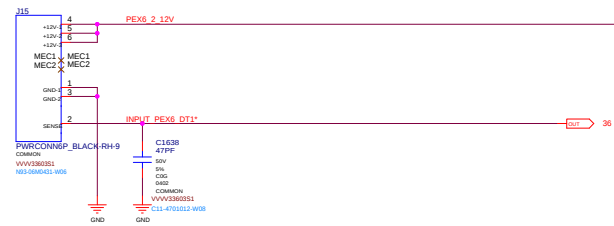
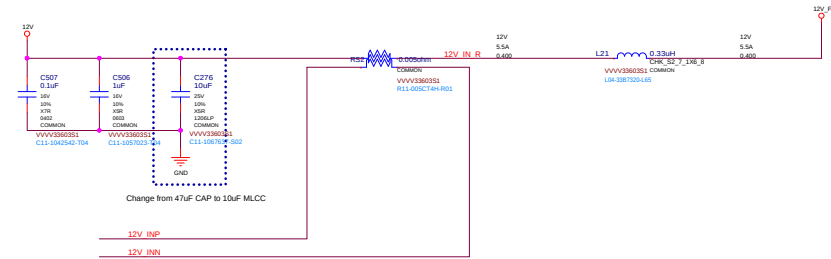
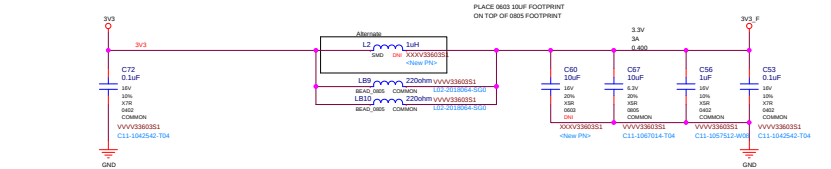
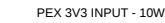
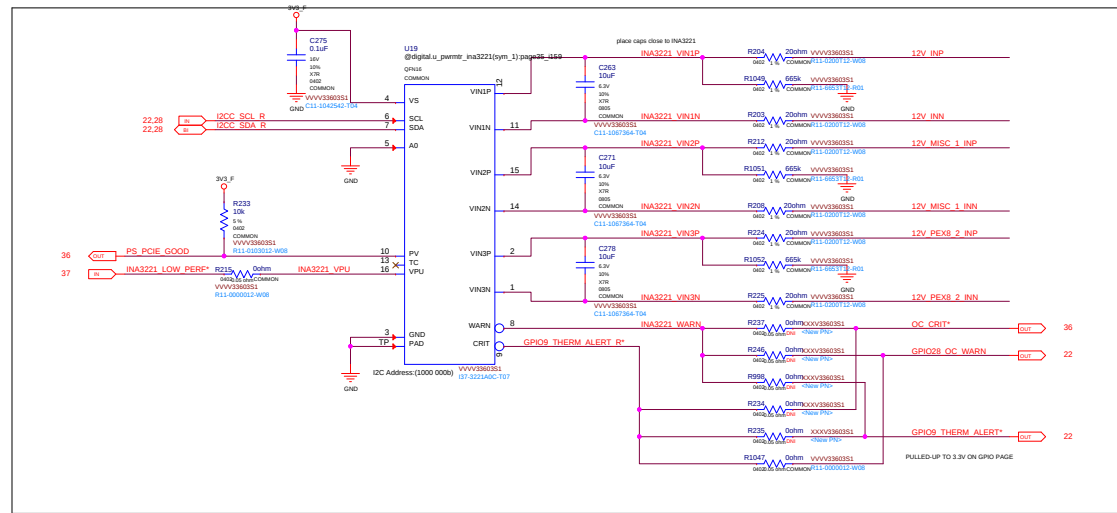


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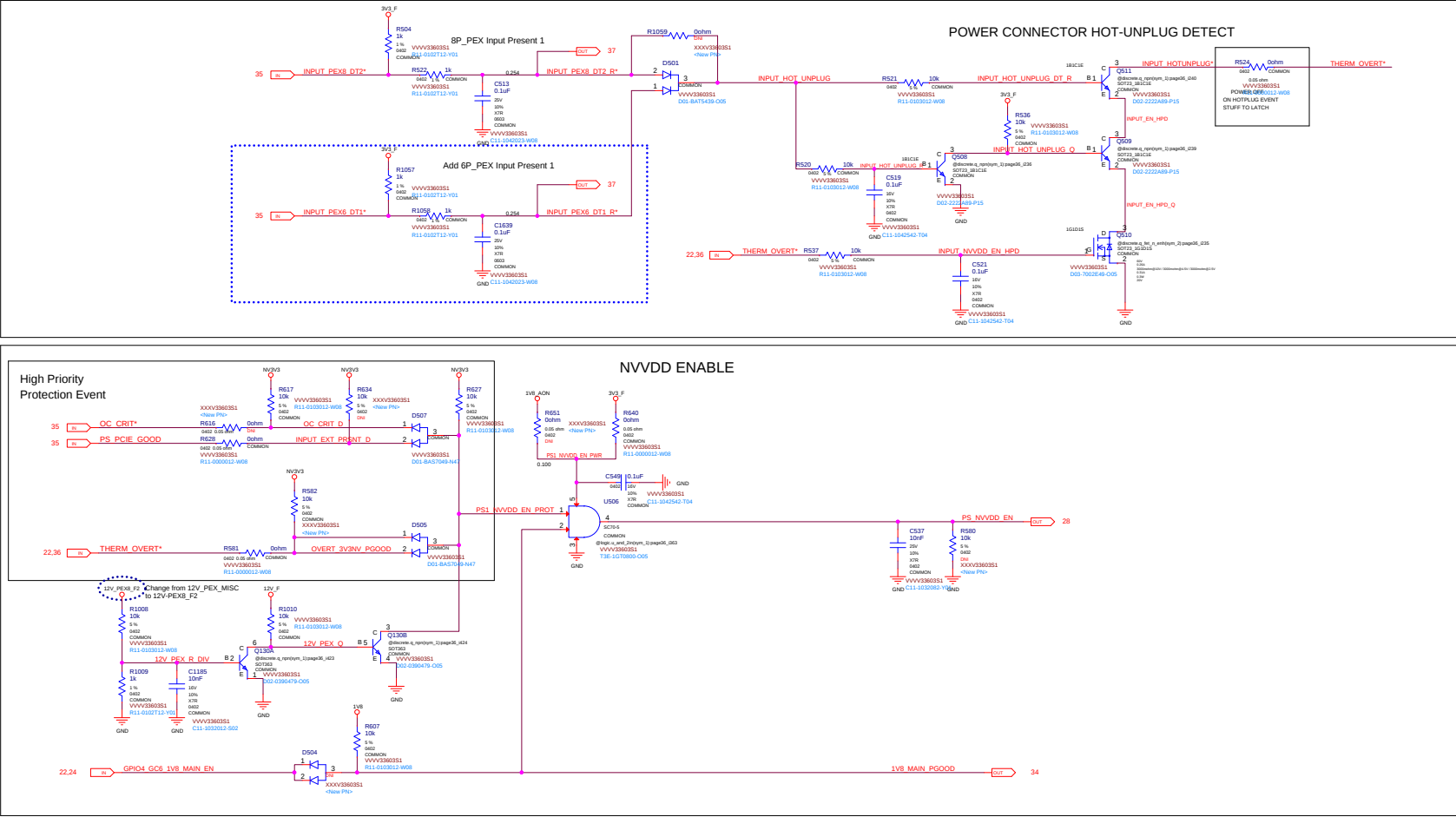


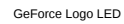
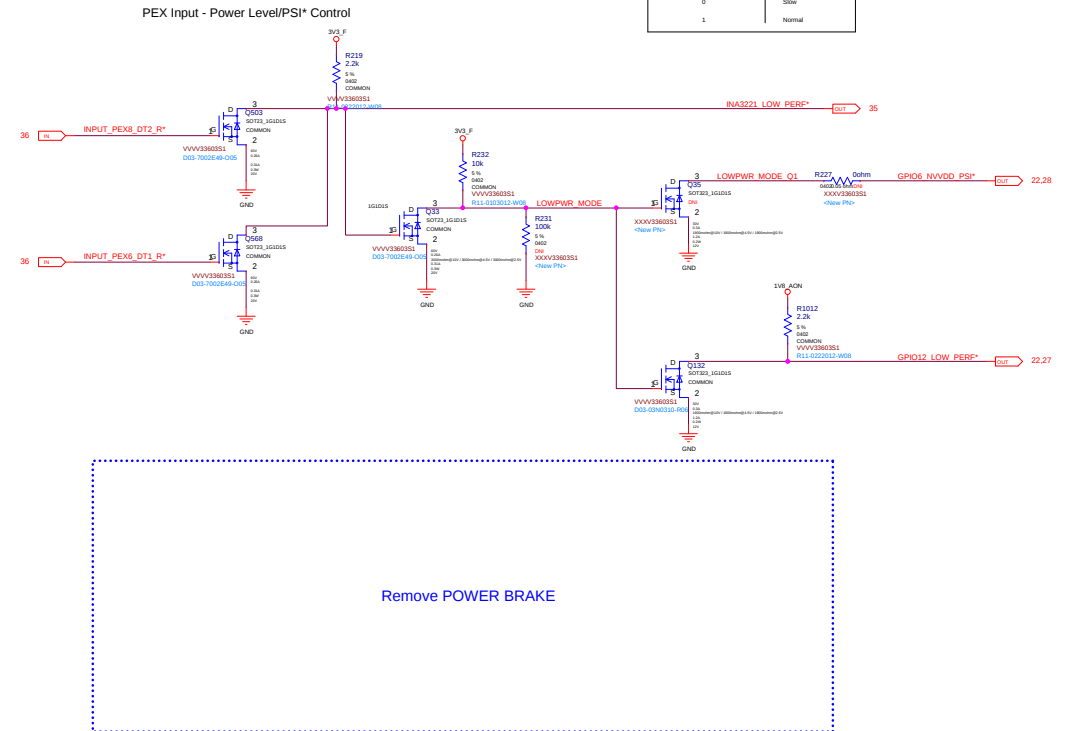
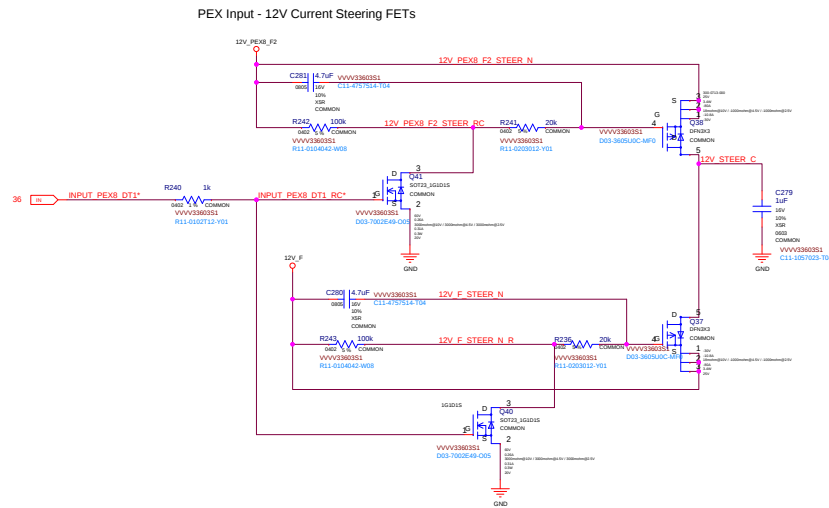


STUFF FOR 6-PIN CONNECTOR
OR REVERSE CPU 8-PIN CONNECTOR



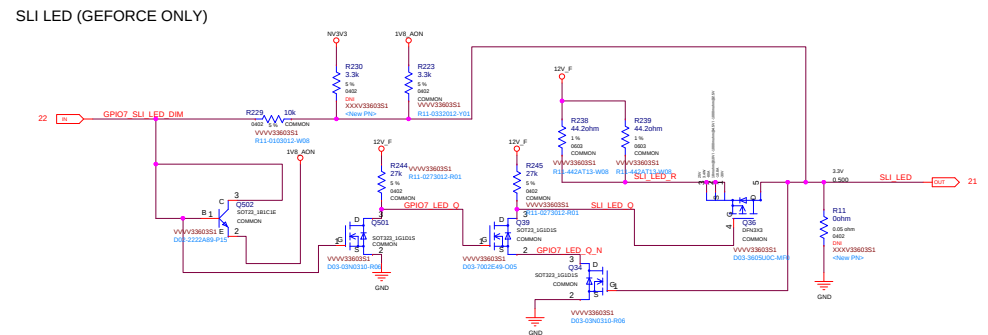
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Size Custom	Document Description PS: Inputs, Filtering, and Monitoring	Rev 3.0
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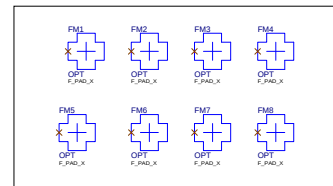
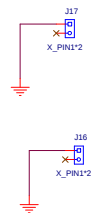
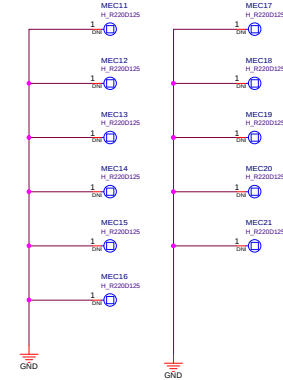
LED HEADER
(COMMON)

Remove Logo LED



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Size Custom	Document Description Mechanical: Bracket/Thermal Solution	Rev 3.0
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Size	Document Description	Rev
Custom	VOLTAGE SUPERVISOR	3.0
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