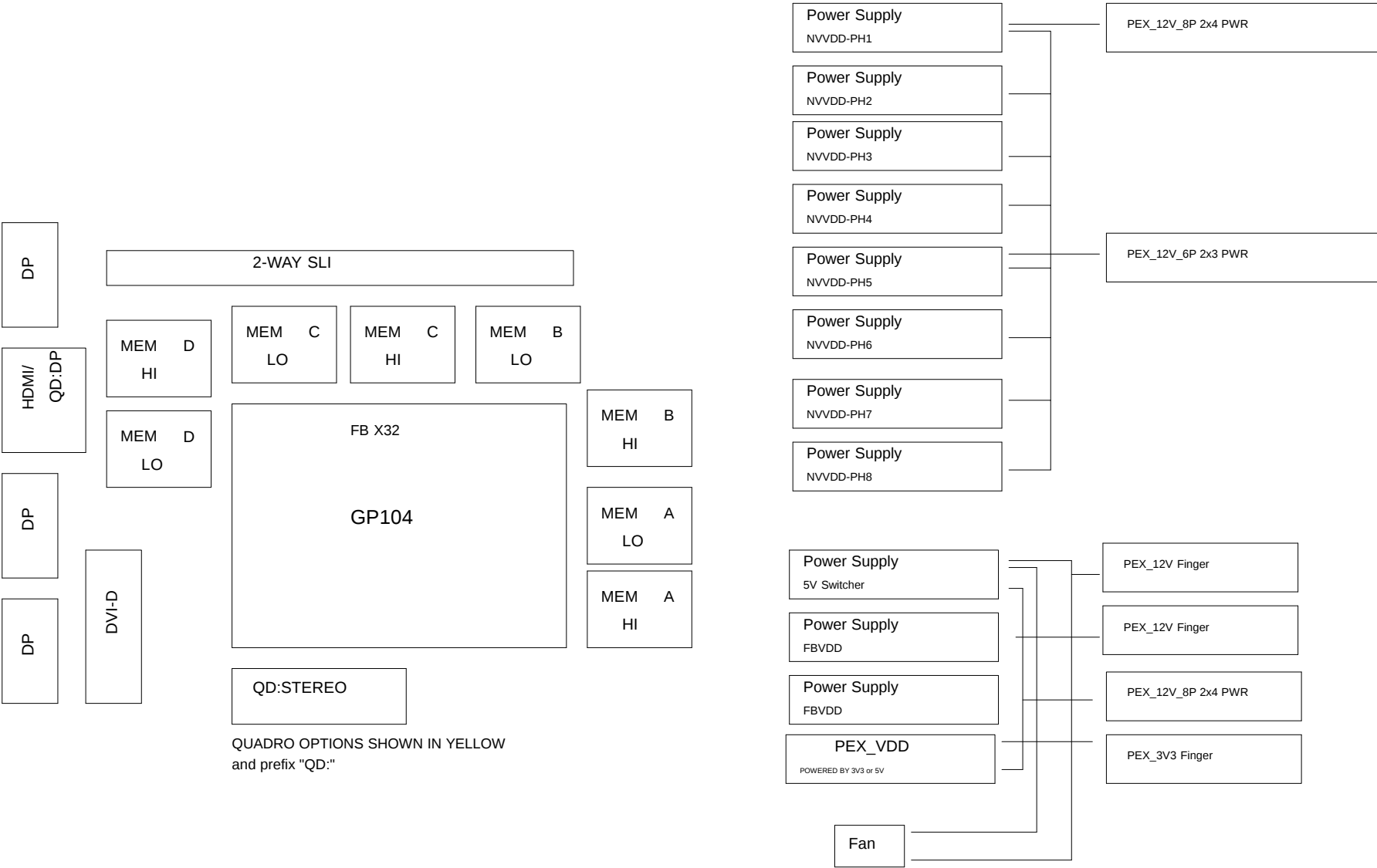


PG413 A00

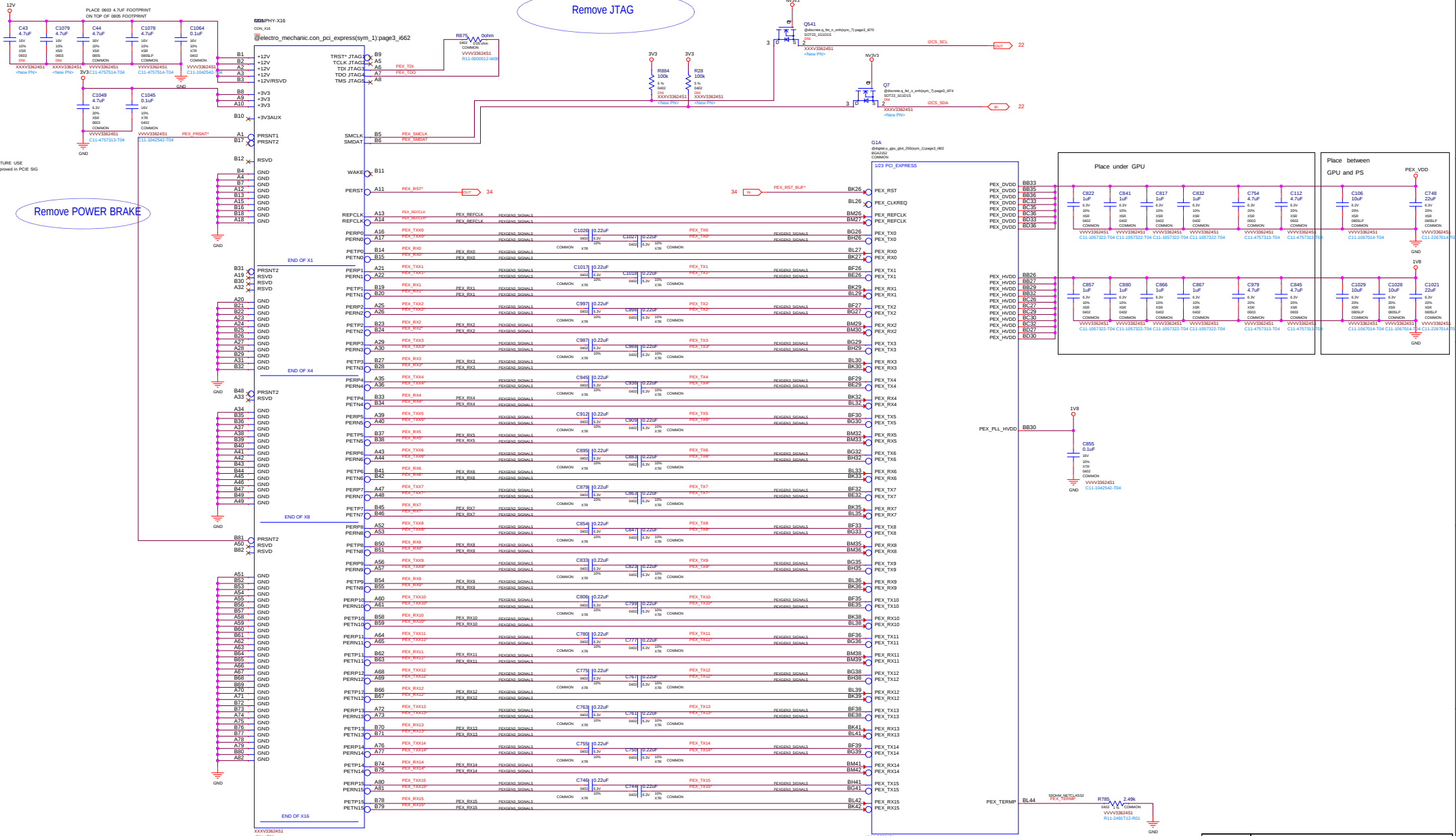
GP104 - 8GB GDDR5X, 256b, 256Mx32
Tall DVI-D + DP + DP + DP/HDMI + DP

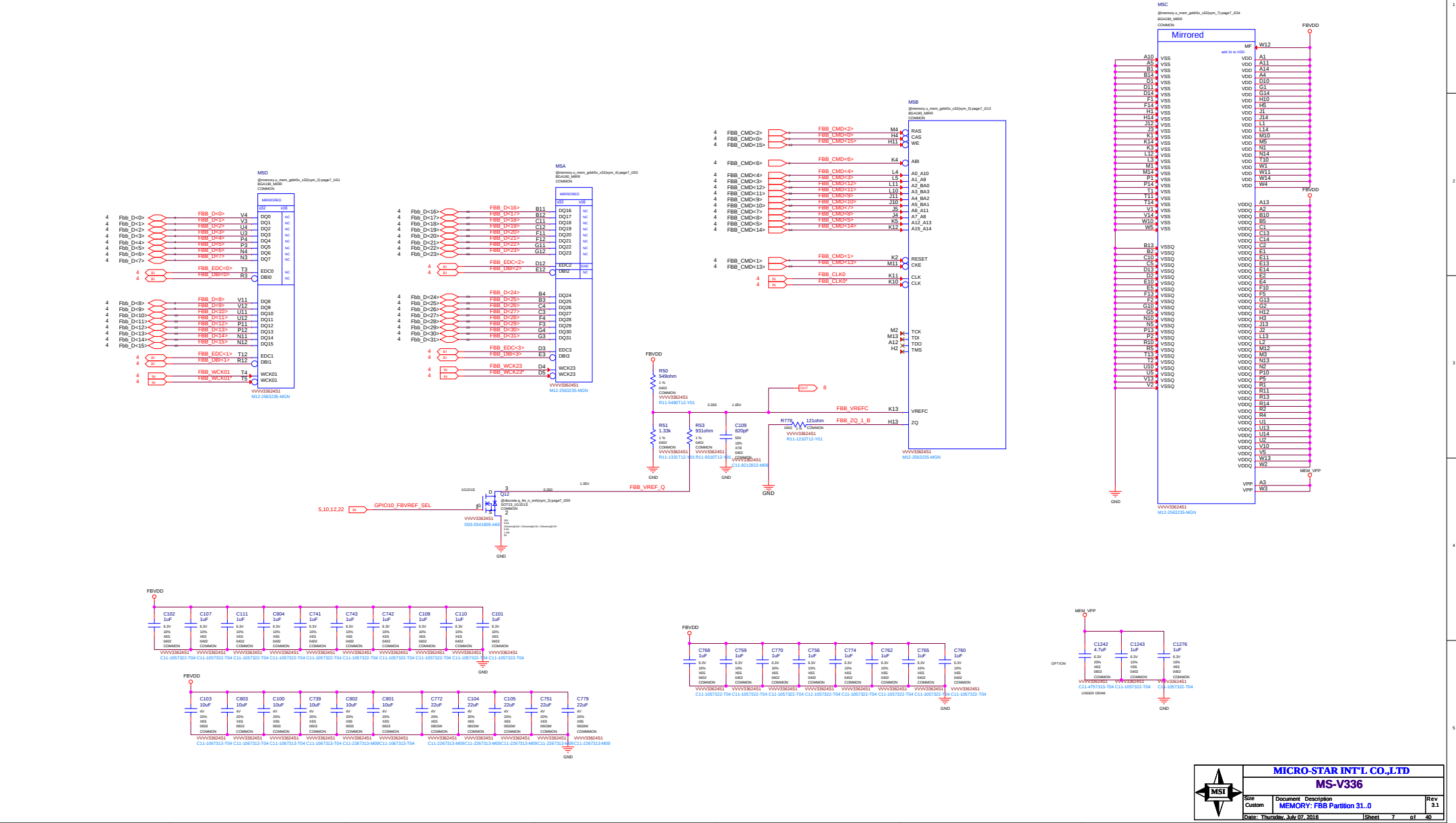
TABLE OF CONTENTS

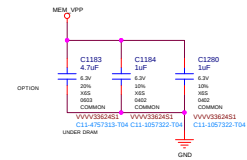
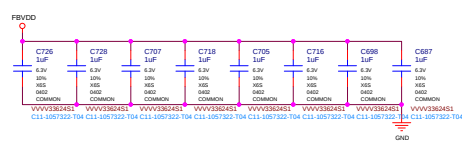
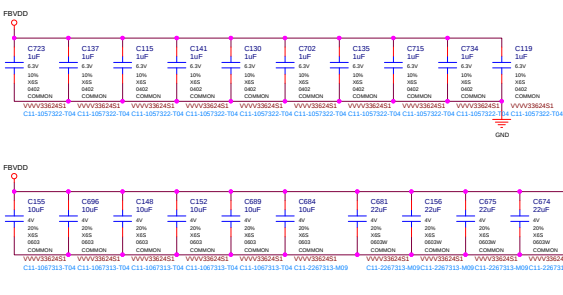
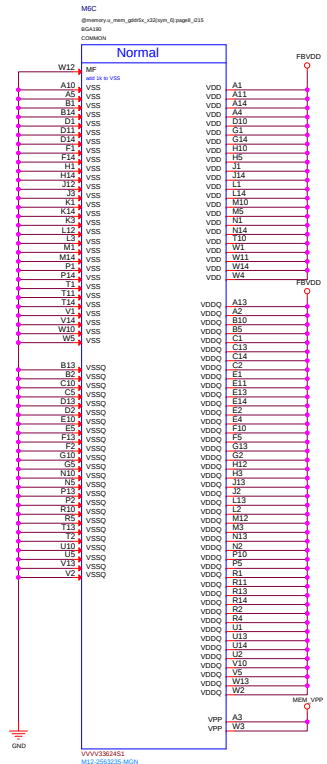
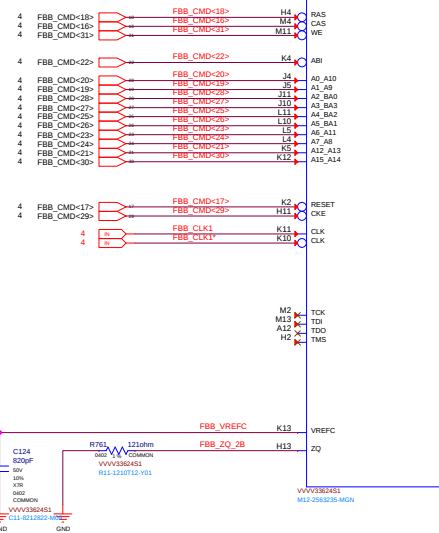
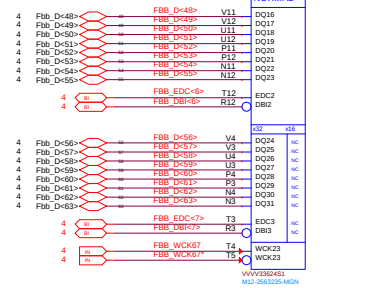
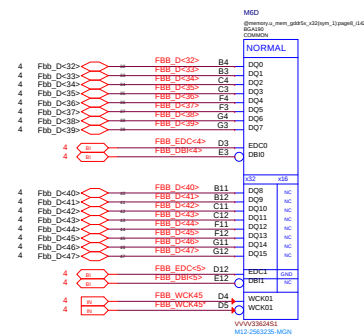
Page	Description	Page	Description	V336-3.0	Change List	V336-3.1	Change List
1	Table of Contents	26	PS: FBVDD	01	Remove JTAG/POWER BRAKE circuit	39	ENE3574 VCC power change to 3V3_F
2	Block Diagram	27	PS: NVVDD_OVR8	14	Remove FBVDD_SENSE_RTN resistor		
3	PCI Express	28	PS: Blank Page	17	Change DP Library/Footprint		
4	MEMORY: GPU Partition A/B	29	PS: NVVDD Phase 1-4	18	Change DP Library/Footprint		
5	MEMORY: FBA[31:0]	30	PS: NVVDD Phase 5 & 6	19	Change HDMI Library/Footprint		
6	MEMORY: FBA[63:32]	31	PS: Blank Page		Remove co-lay DP		
7	MEMORY: FBB[31:0]	32	PS: Dynamic Power Balance Phases	20	Change DP Library/Footprint		
8	MEMORY: FBB[63:32]	33	PS: Dynamic Power Balance Logic	21	Remove MIOA/B FRAME LOCK circuit		
9	MEMORY: GPU Partition C/D	34	PS: NV3V3, NV12V	22	Remove Thermal IC		
10	MEMORY: FBC[31:0]	35	PS: Inputs, Filtering, and Monitoring		Remove GPIO19_STEREO Circuit		
11	MEMORY: FBC[63:32]	36	PS: Shutdown and Sequencing		Remove Unused GPIO		
12	MEMORY: FBD[31:0]	37	PS: 12V Current Steering PSI Control and LED	24	Remove co-lay APW8713AQBI-TRG, BUCK		
13	MEMORY: FBD[63:32]	38	MECH: Bracket/Thermal	25	Remove 12V_PEX_MISC option		
14	GPU PWR and GND			26	FBVDD controller circuit change to Page 27		
15	GPU Decoupling			28	Copy NVVDD controller circuit from V323-0b		
16	IFPAB DVI-D-DL			29	Copy driver/MOS circuit from V323-0b		
17	IFPE DP			30	Copy driver/MOS circuit from V323-0b		
18	IFPEF DP			32	Remove Dynamic Power Balance Phases		
19	IFPC HDMI 2.0/DP			33	Remove Dynamic Power Balance Phases		
20	IFPD DP			34	Remove Unused GPIO circuit		
21	MIOA/B Interface and Frame Lock			35	Change Input power connector to 6+8		
22	MISC1; Fan, Thermal, JTAG, GPIO, Stereo			36	Add 6pin POWER CONNECTOR HOT-UNPLUG DETECT		
23	MISC2: ROM, XTAL, Straps			37	Add 6pin PEX Input - Power Level/PSI* Control		
24	PS: 1V8, 1V8_AON			39	Add LED_CONTROLLER_ENE3574		
25	PS: 5V, PEX_VDD						

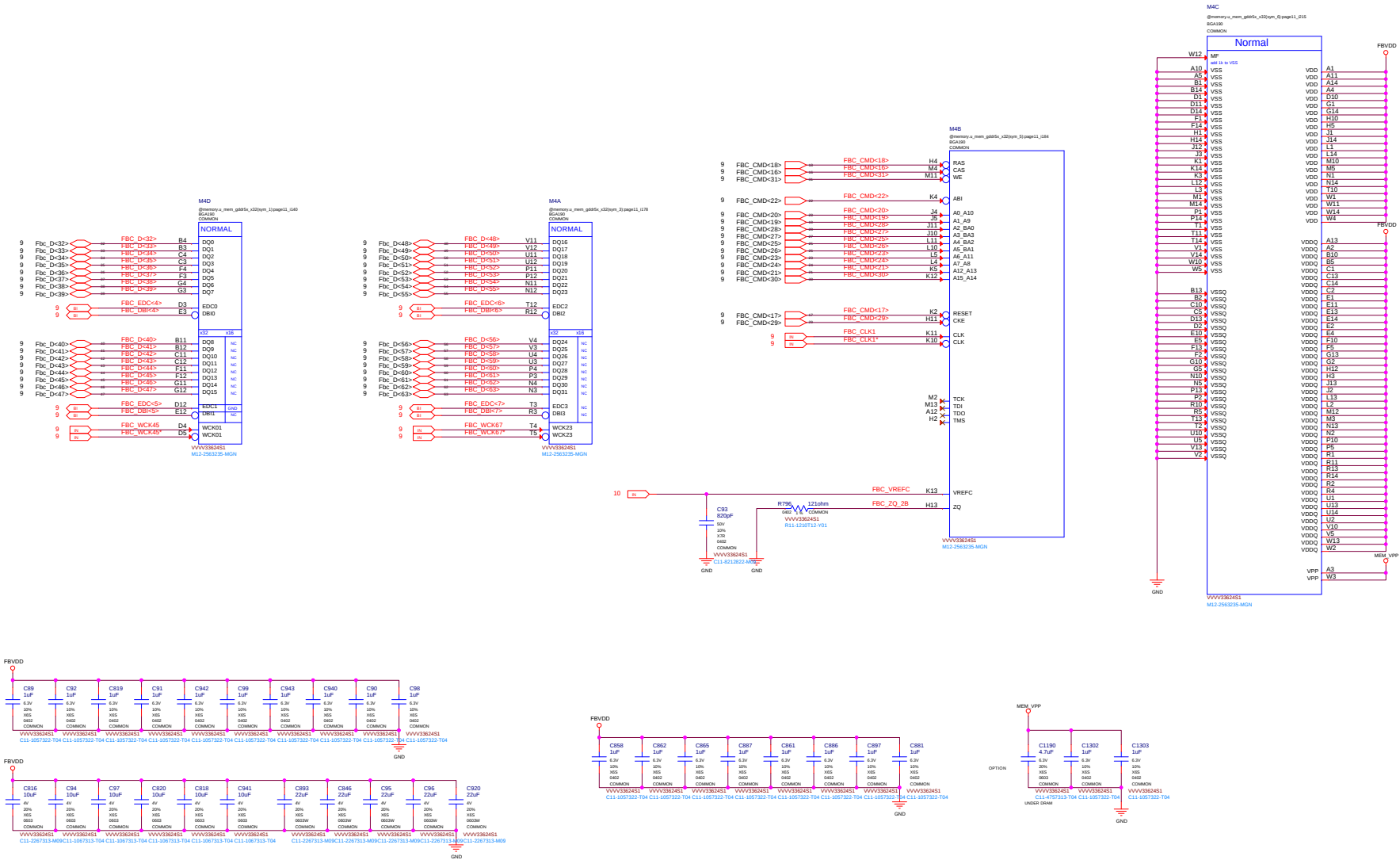


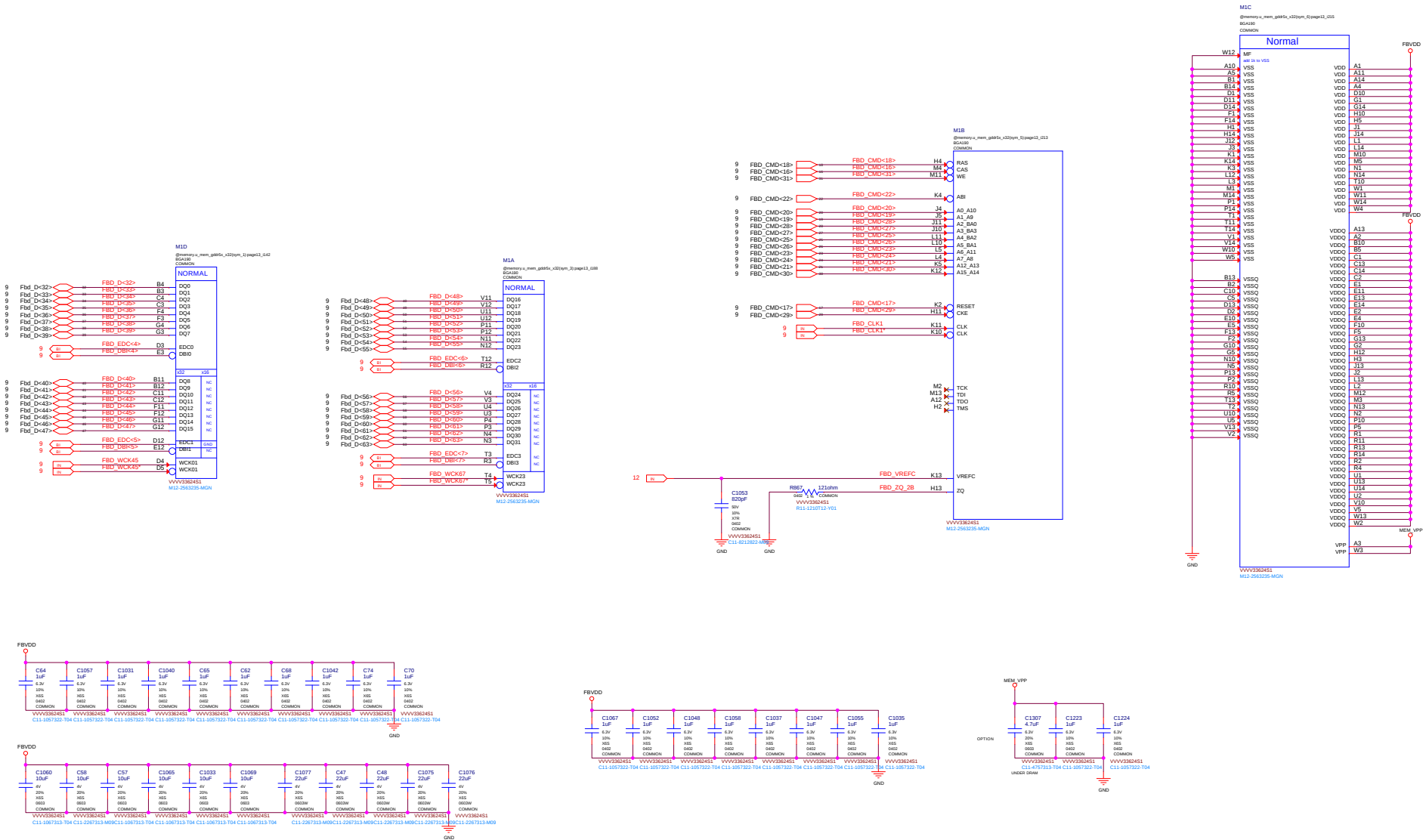
QUADRO OPTIONS SHOWN IN YELLOW
and prefix "QD:"

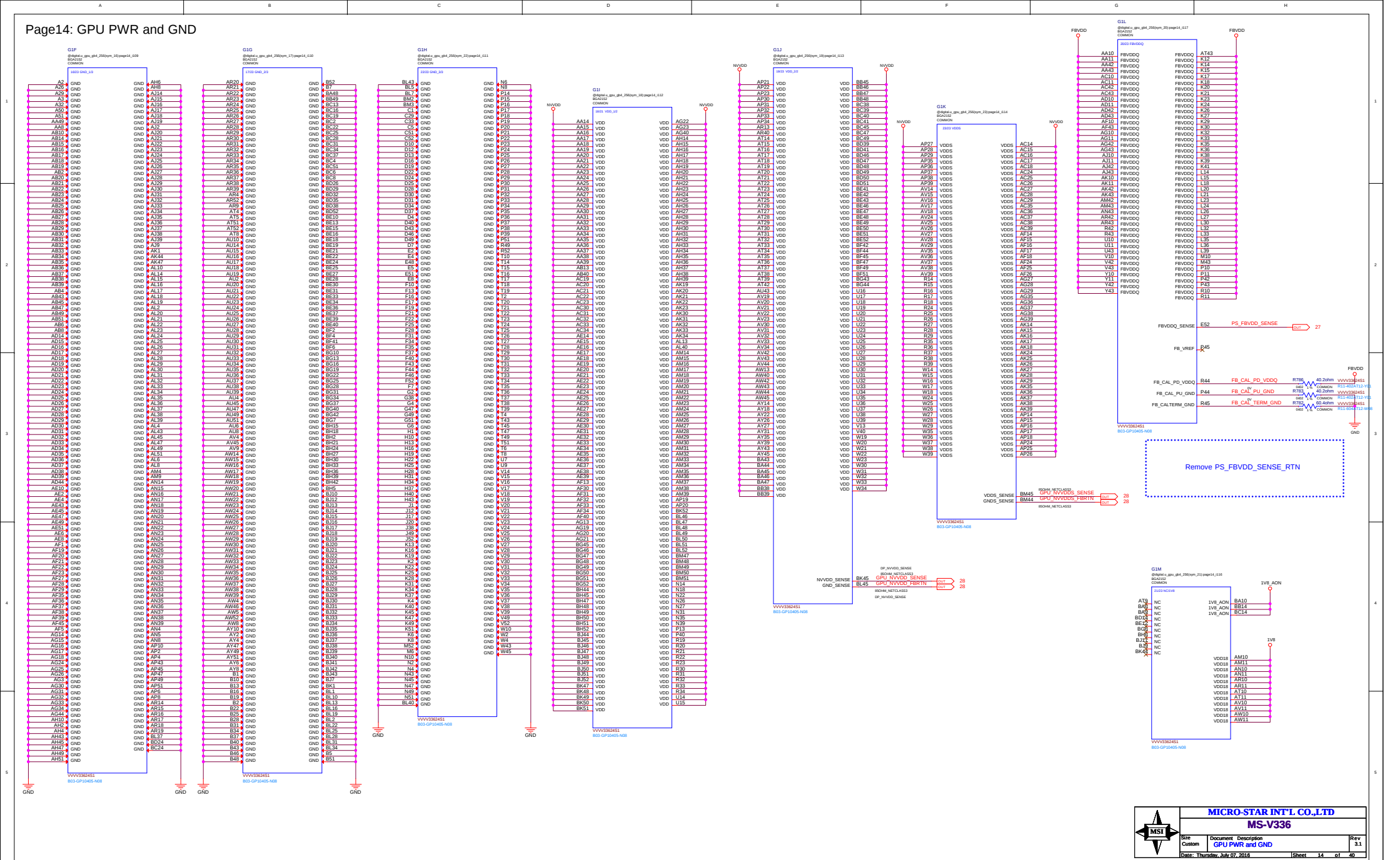




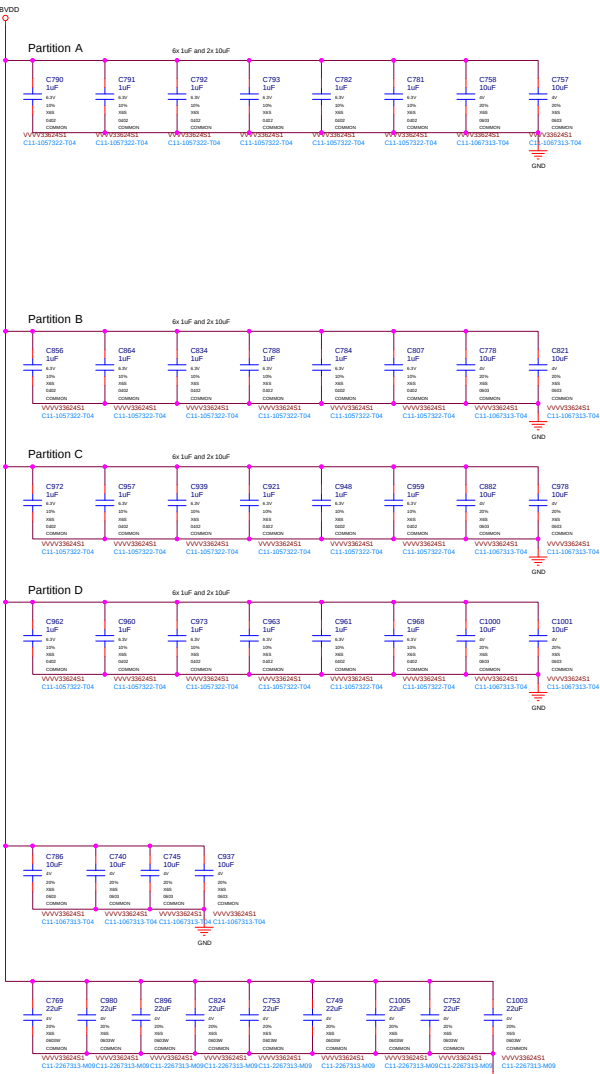




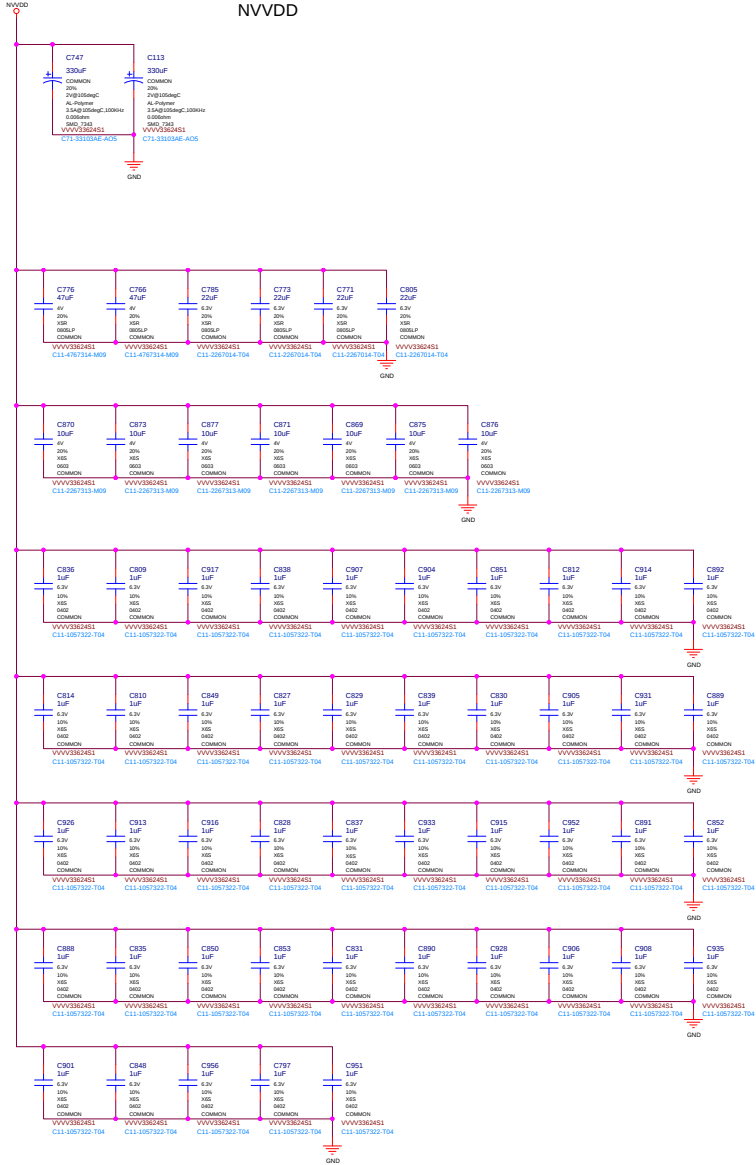




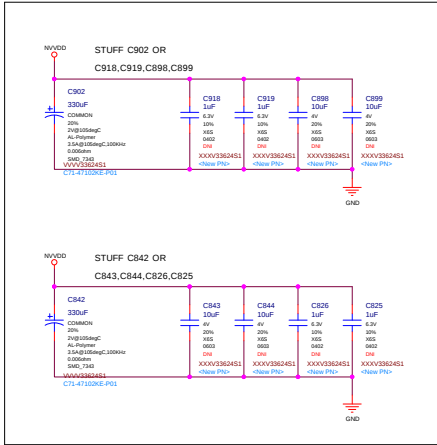
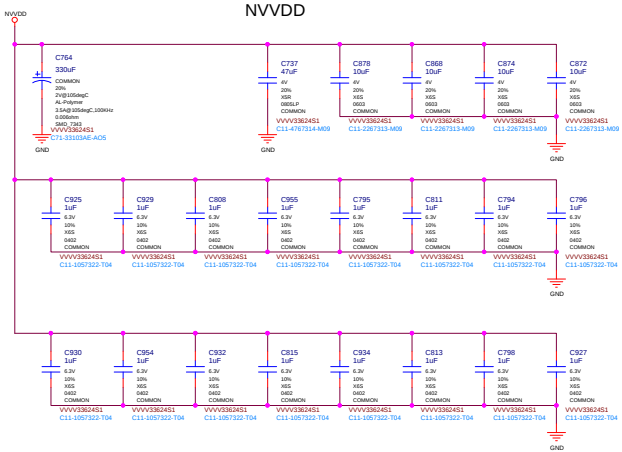
FBVDD



NVVDD



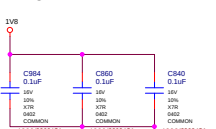
NVVD



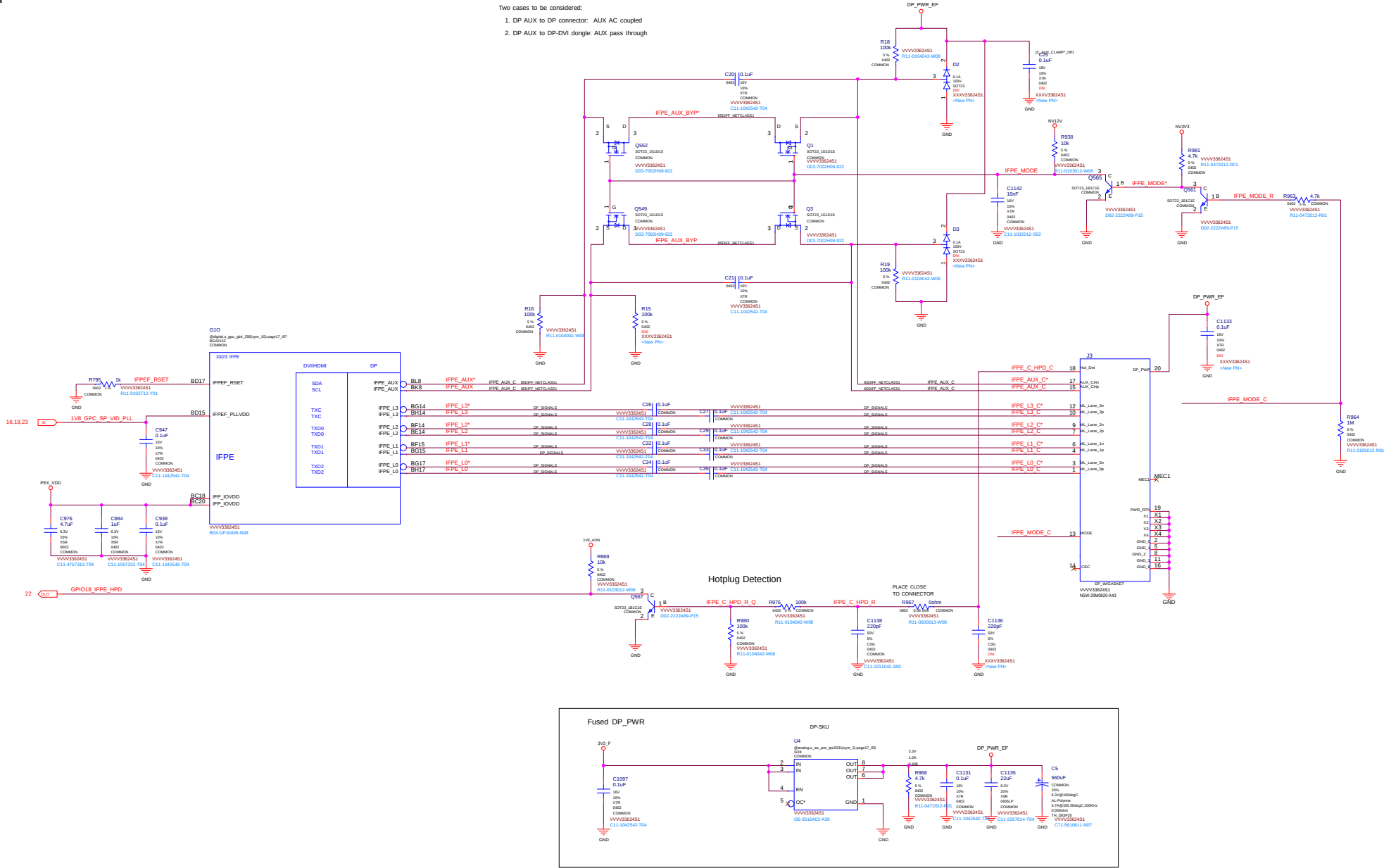
1V8_AON



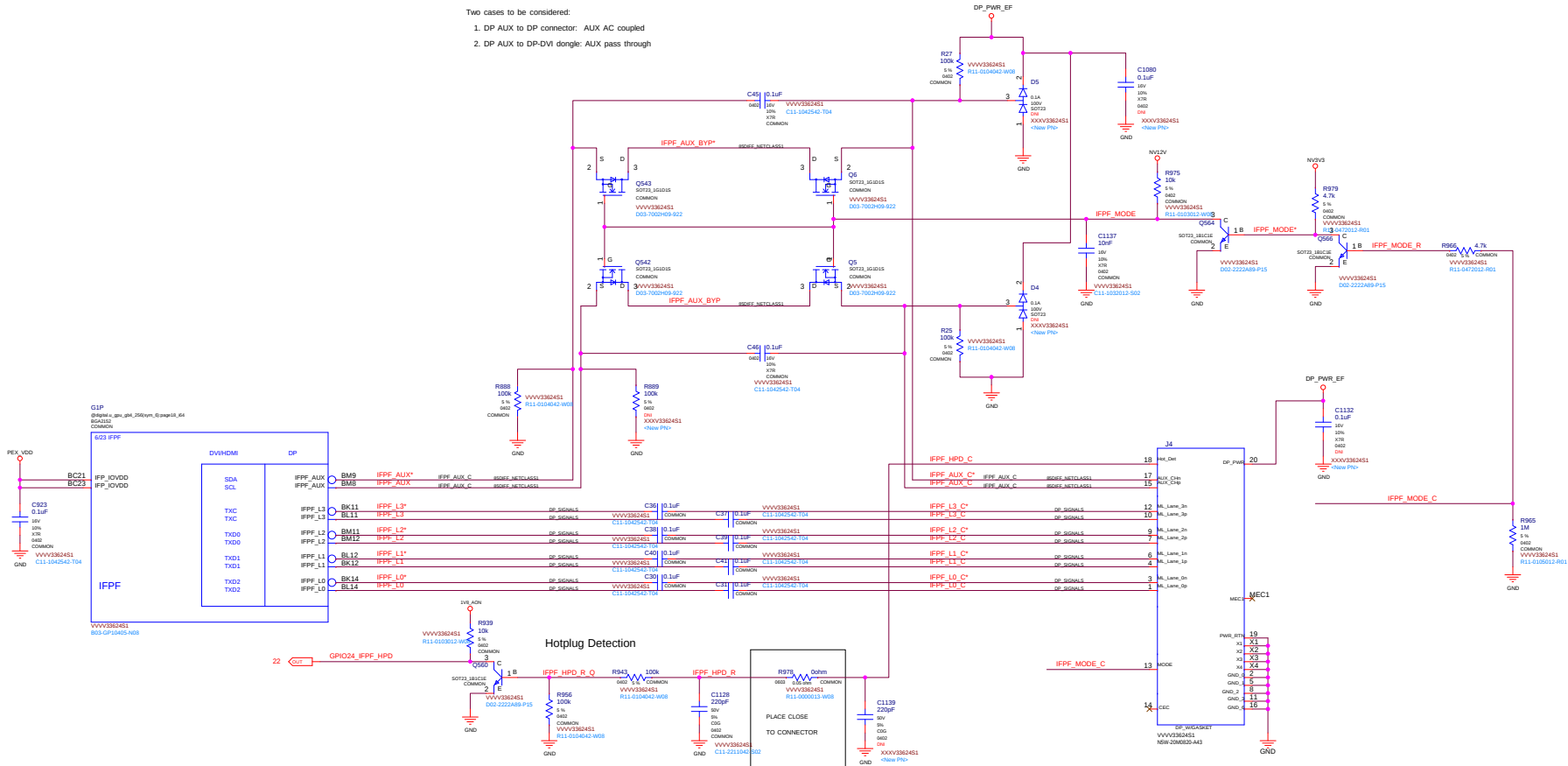
VDD18

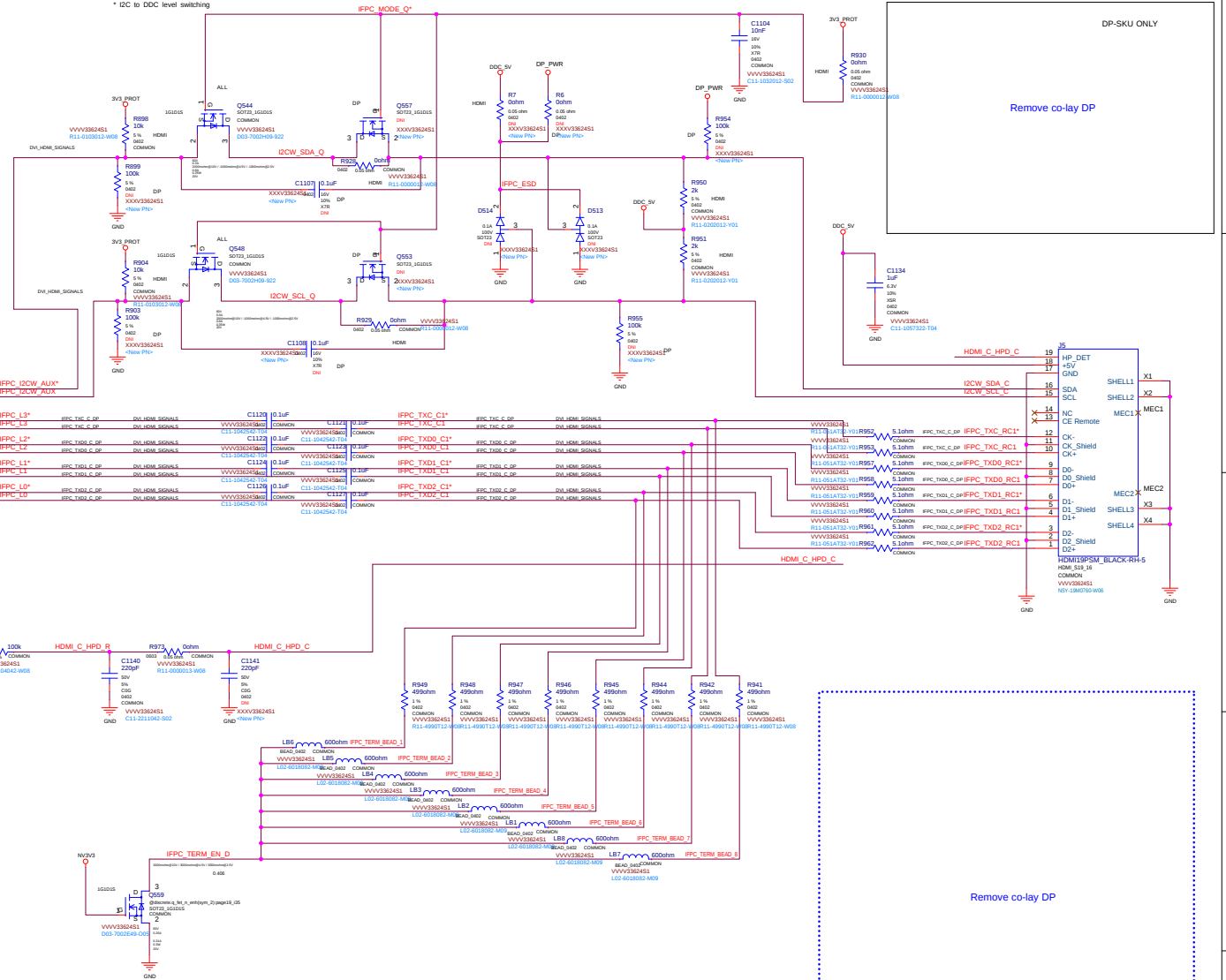
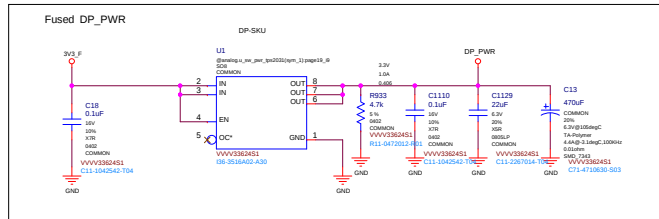


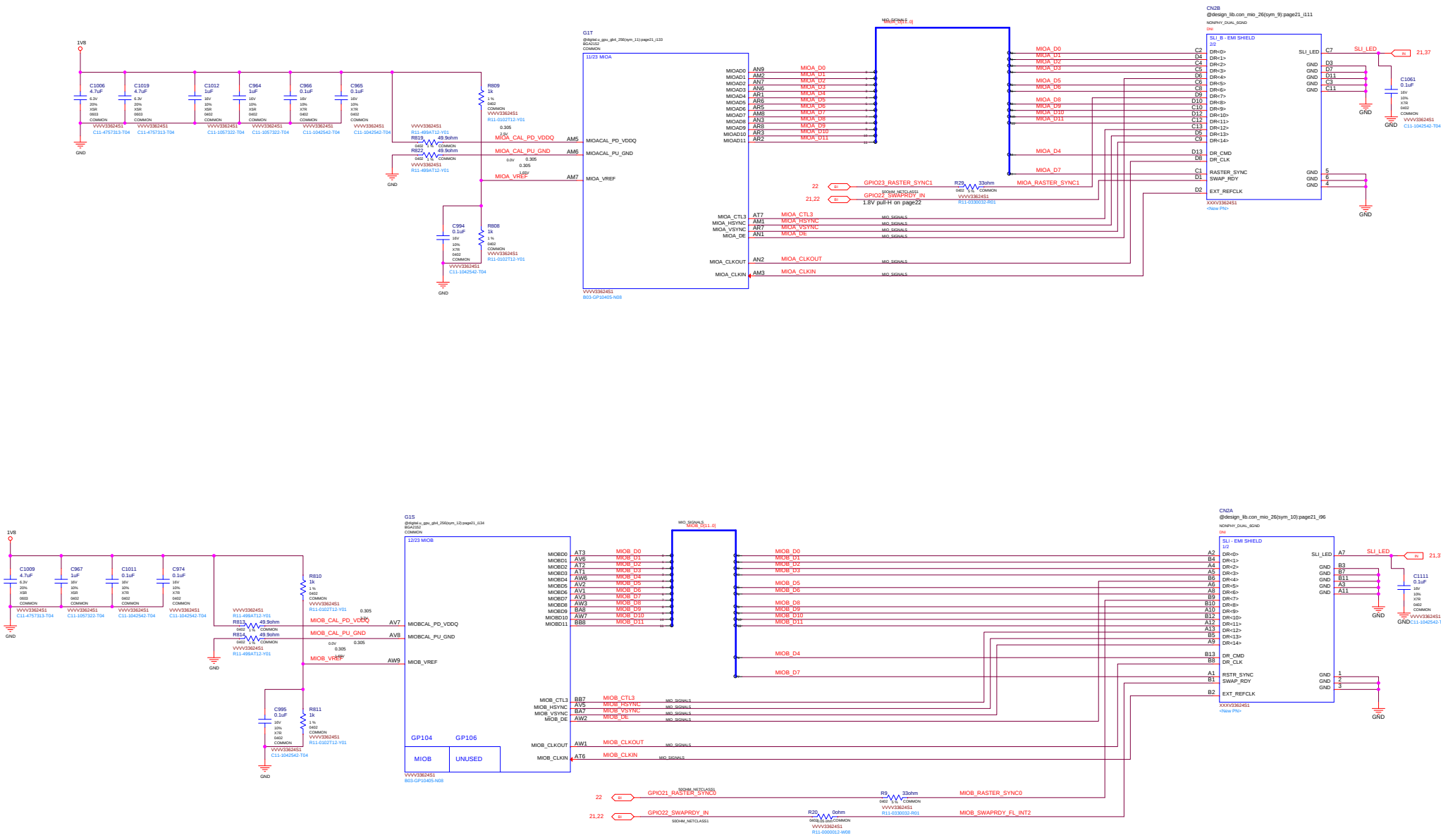
Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DV1 dongle: AUX pass through

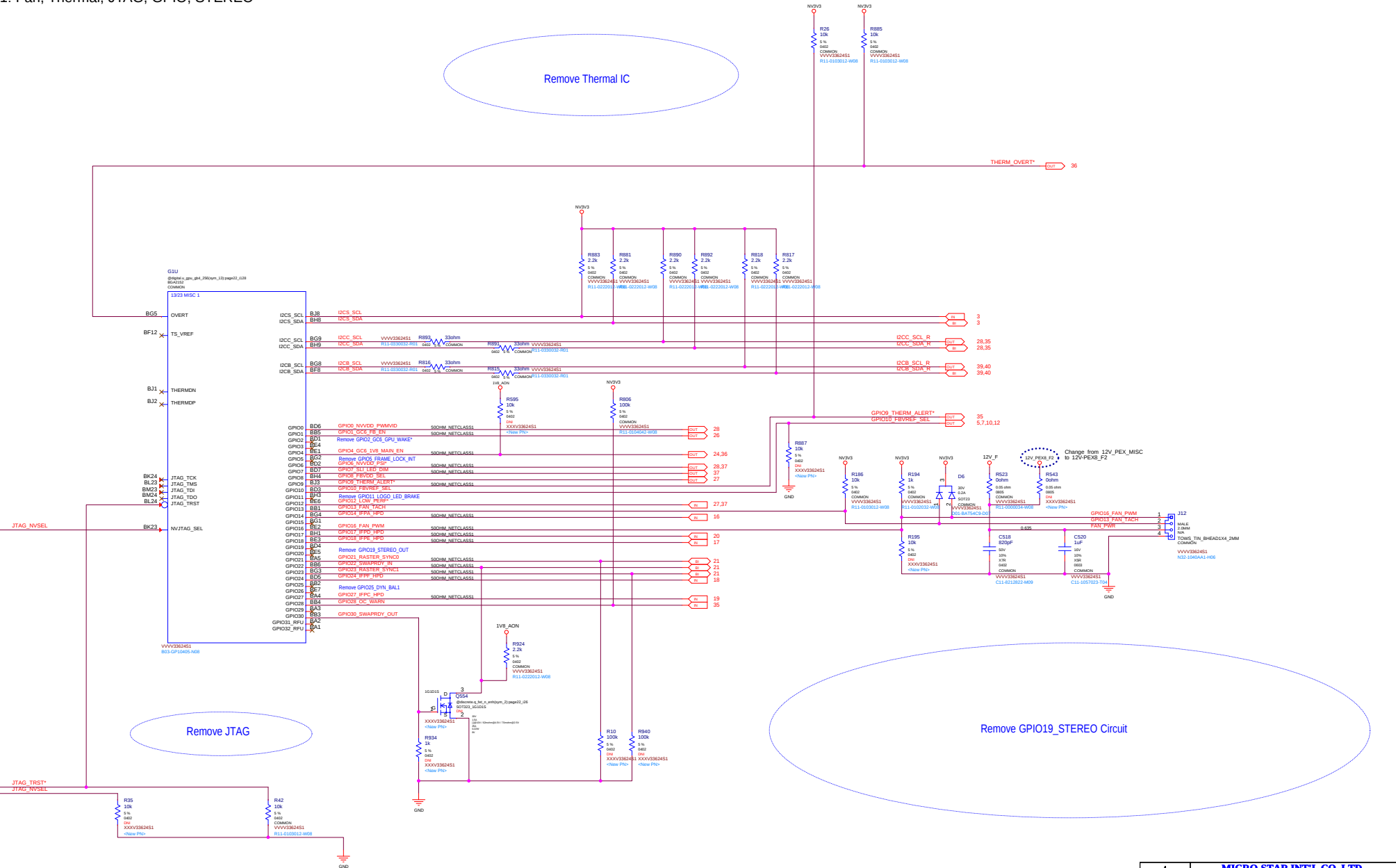


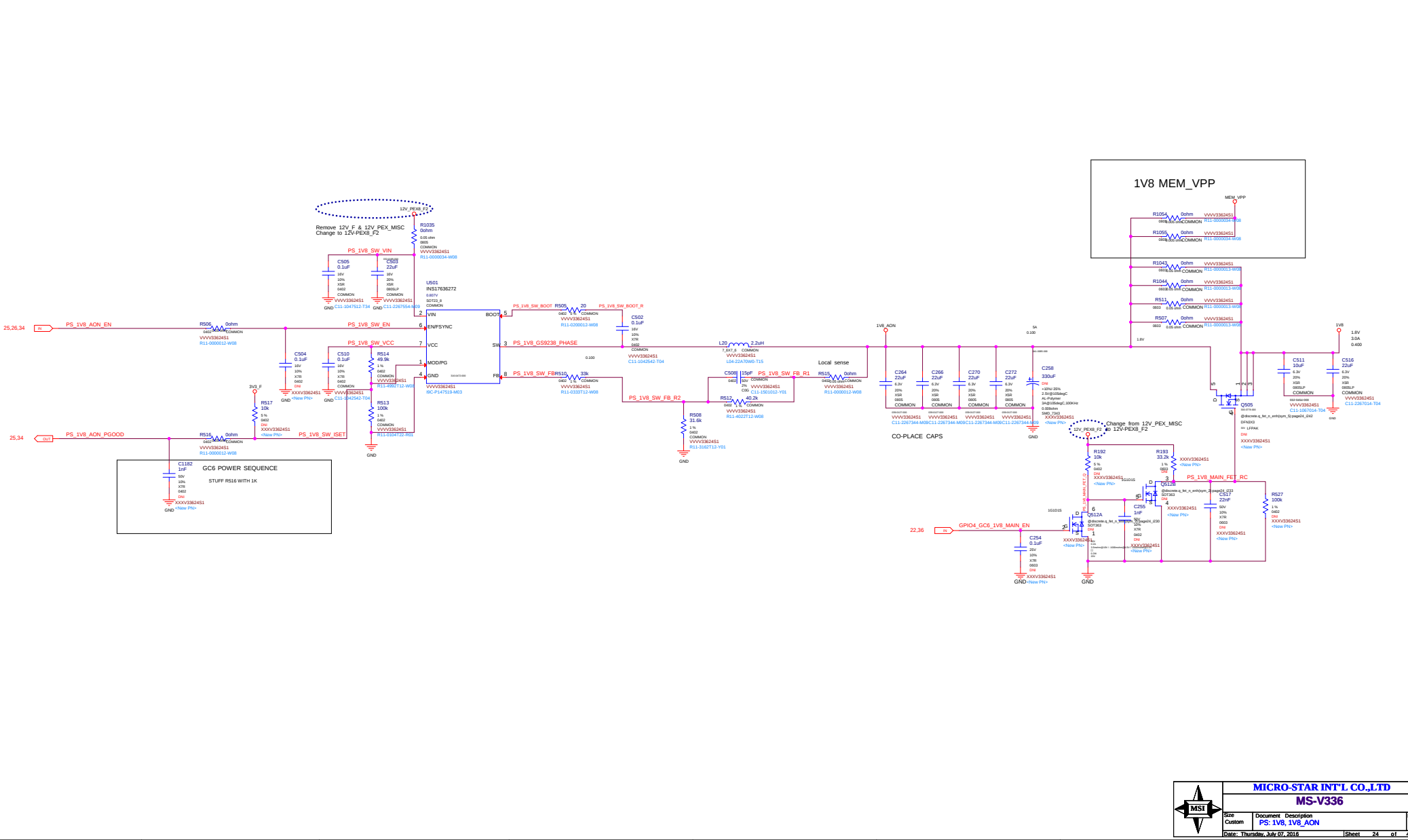
- Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through



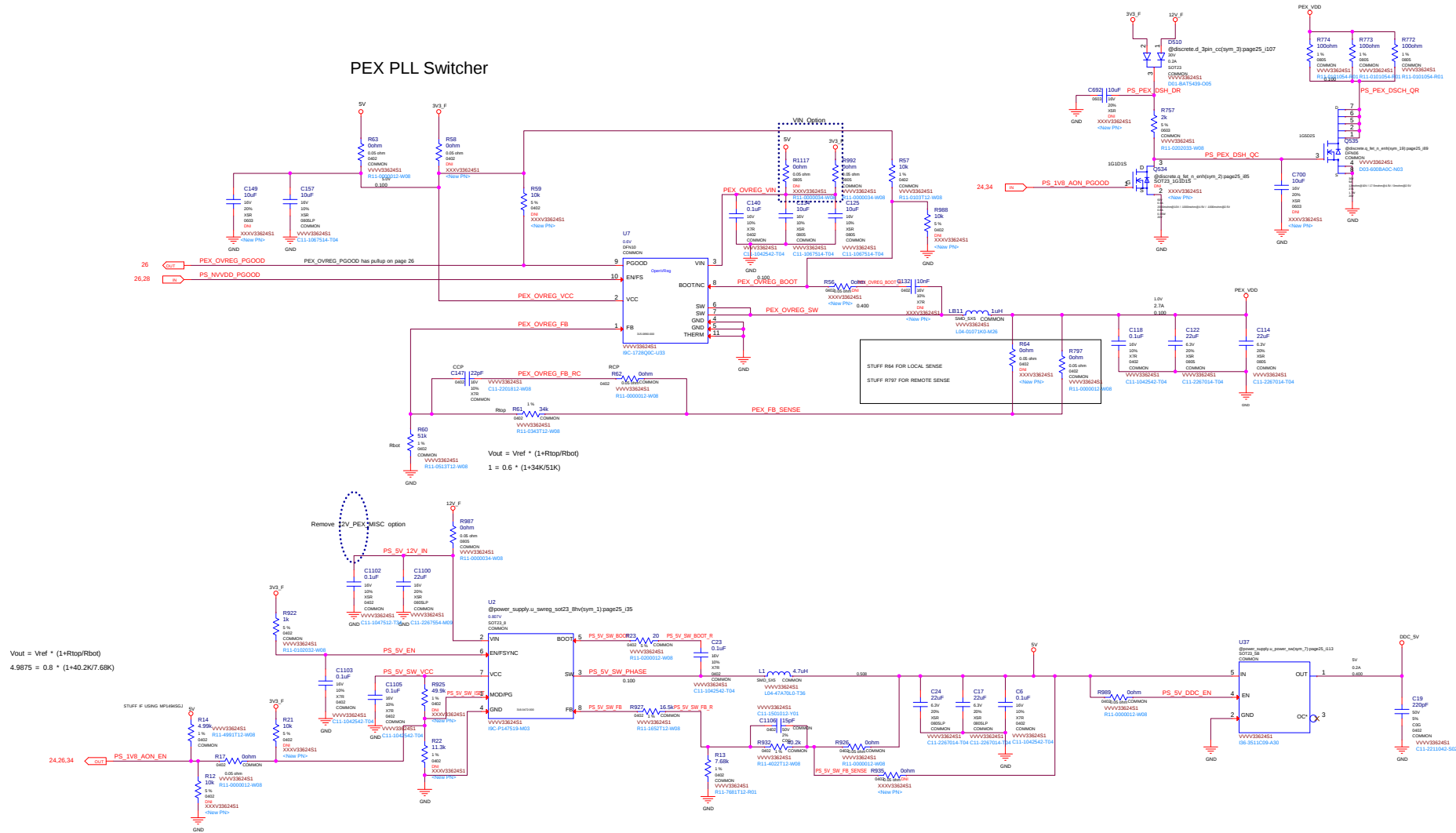








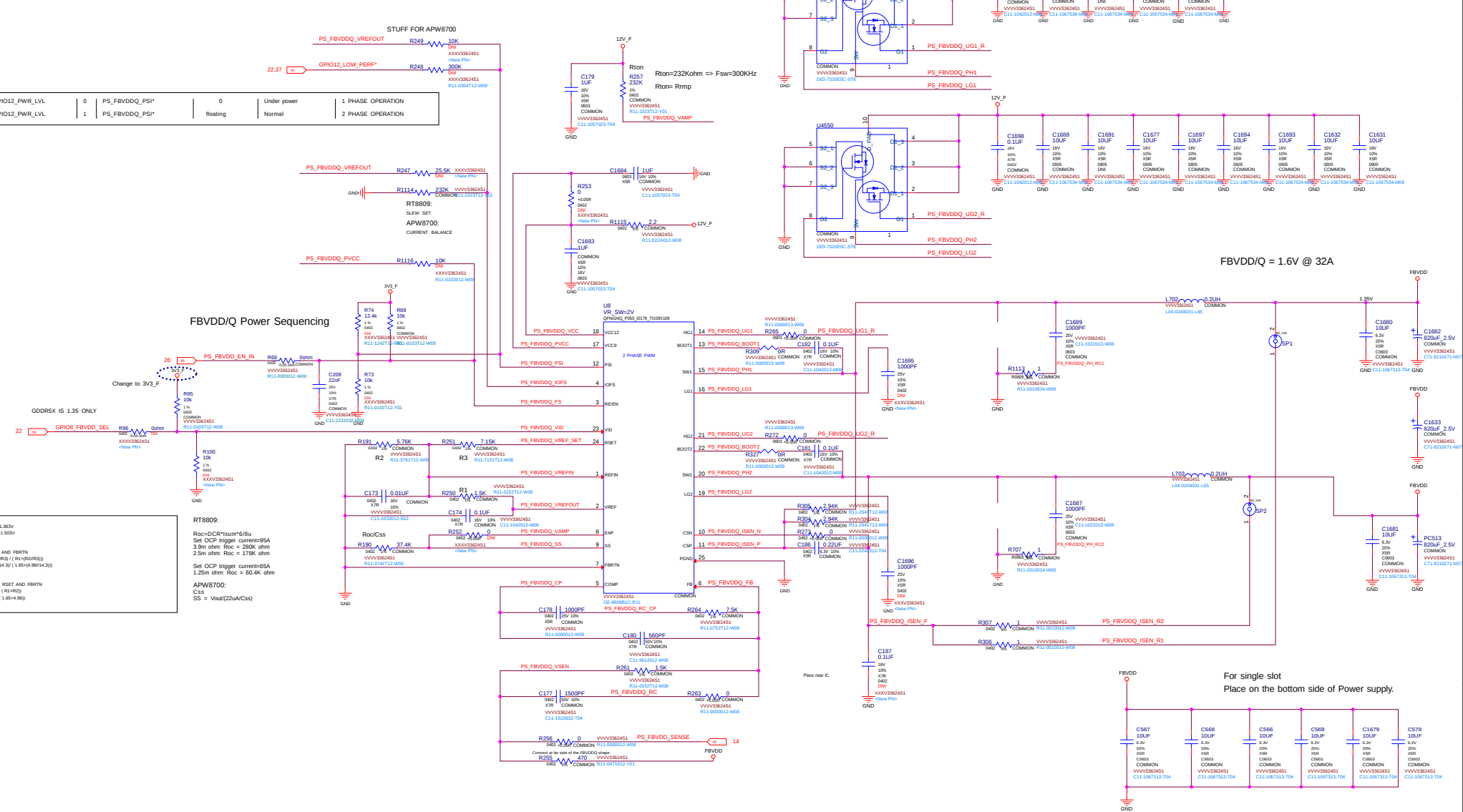
PEX PLL Switcher



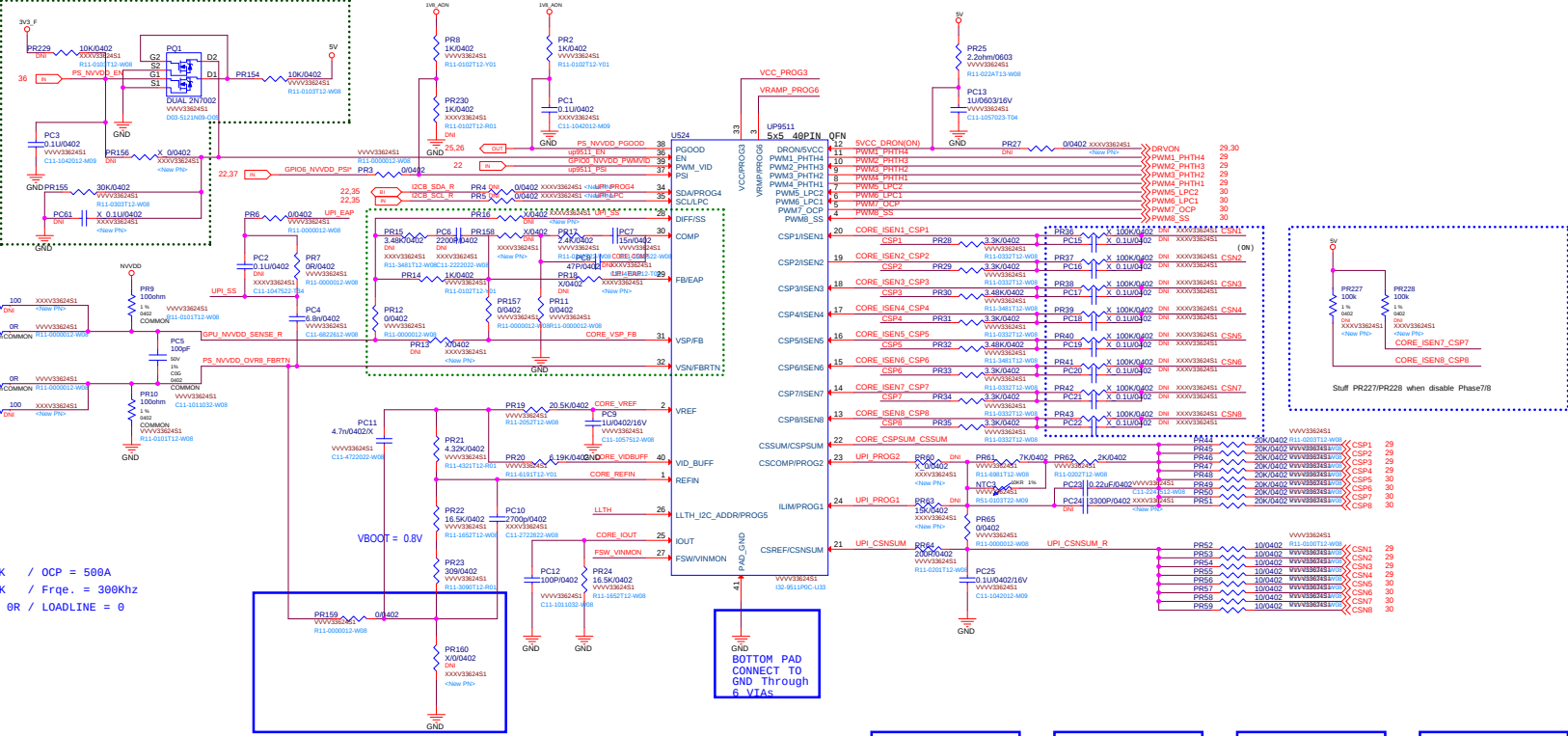
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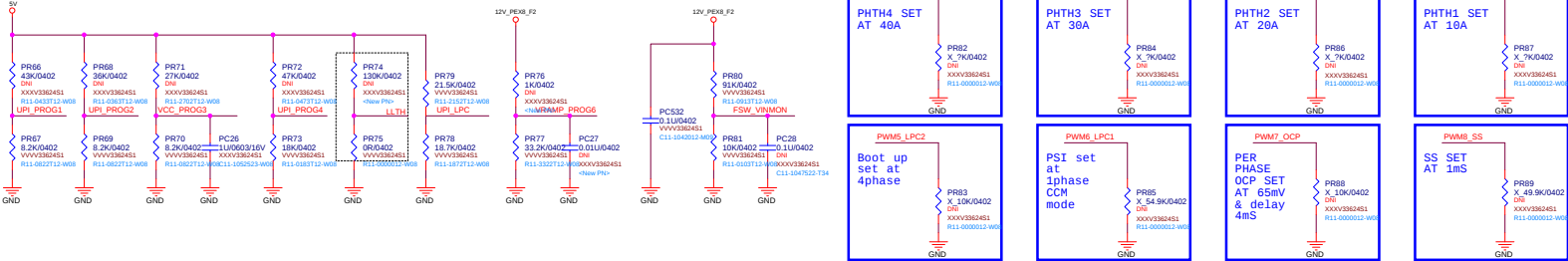


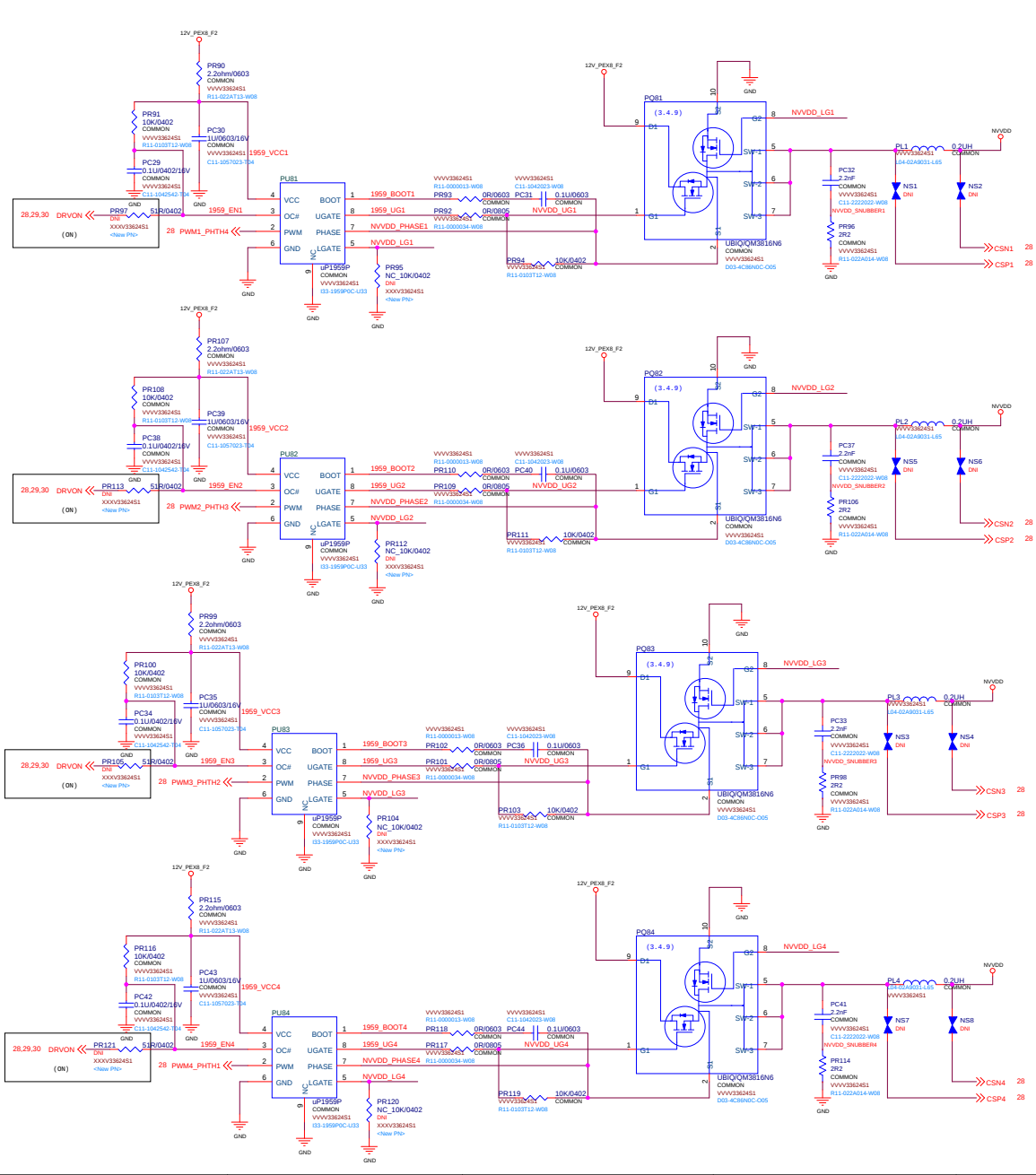


default not stuff

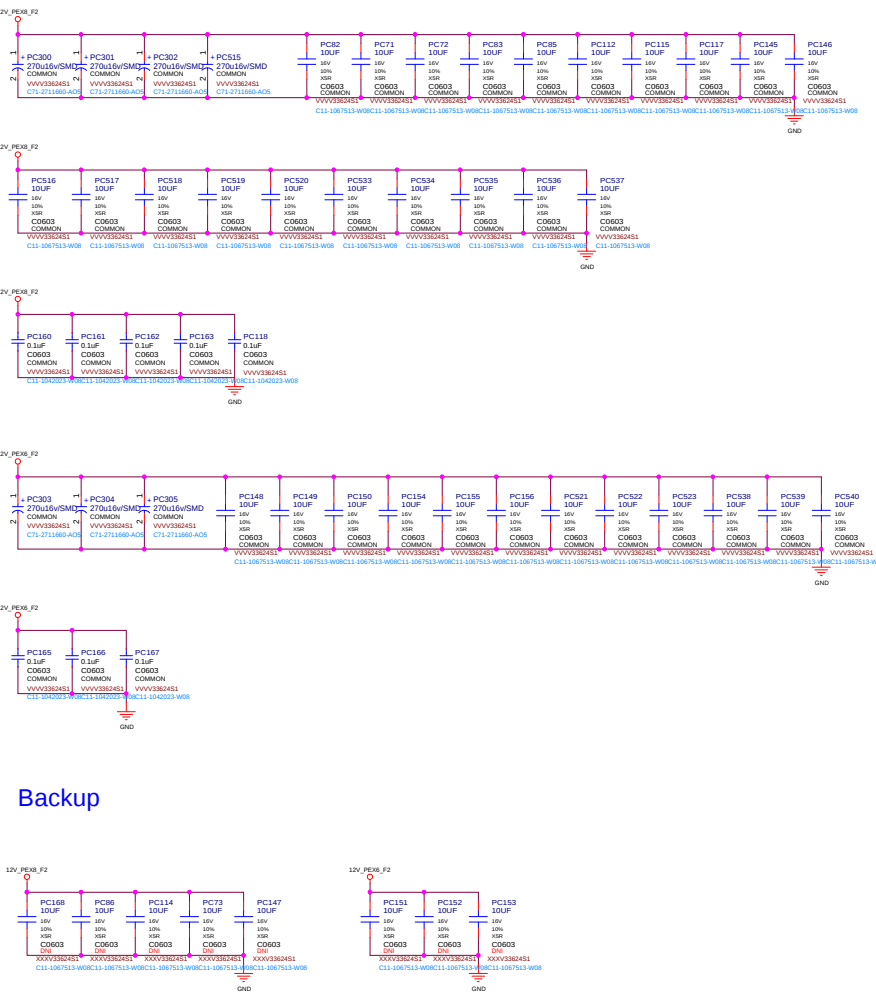


PR24 = 16.5K / OCP = 500A
PR77 = 33.2K / Frqe. = 300kHz
PR6 = PR7 = 0R / LOADLINE = 0

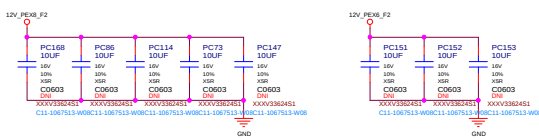


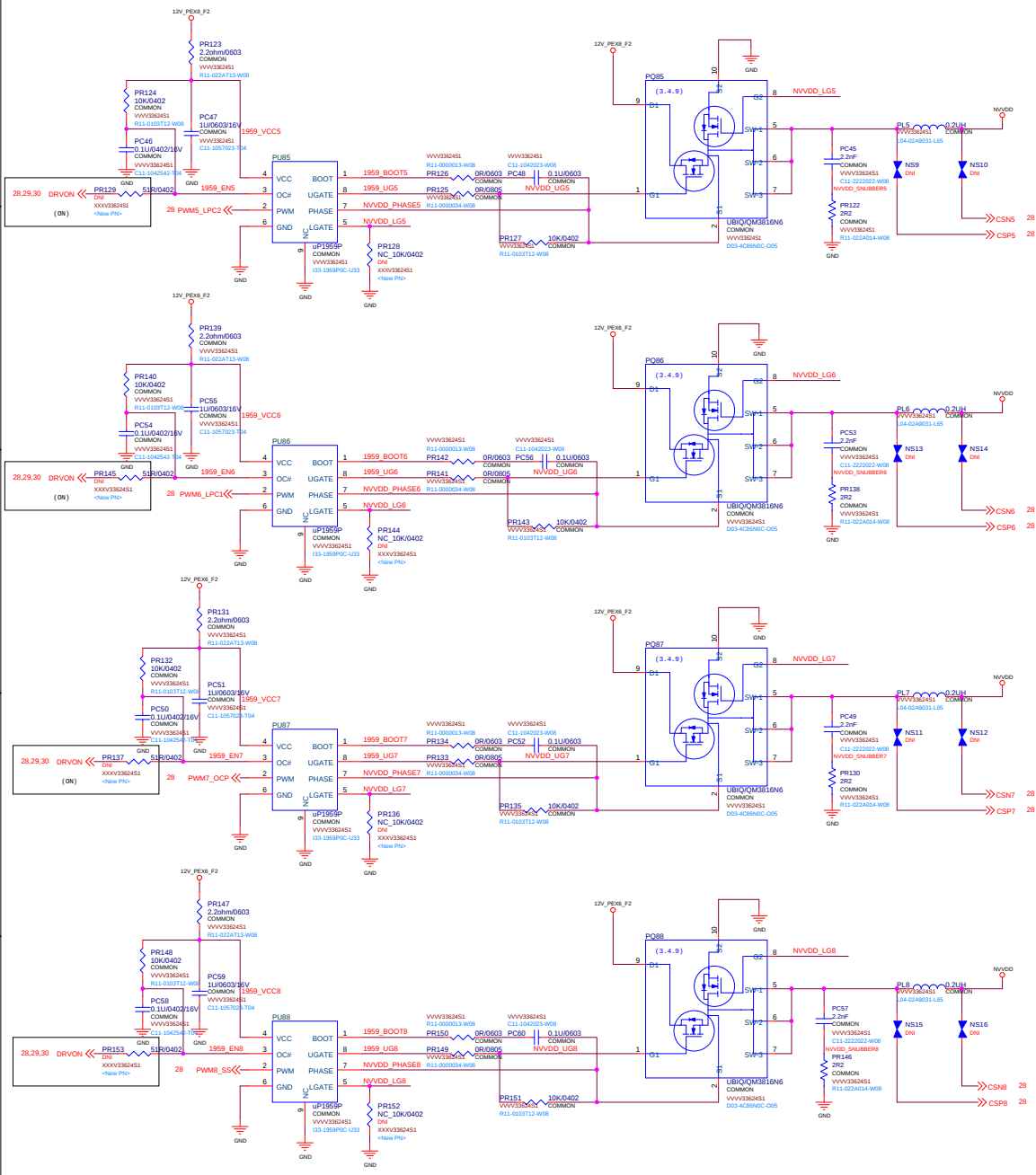


EXT_12V Input CAP

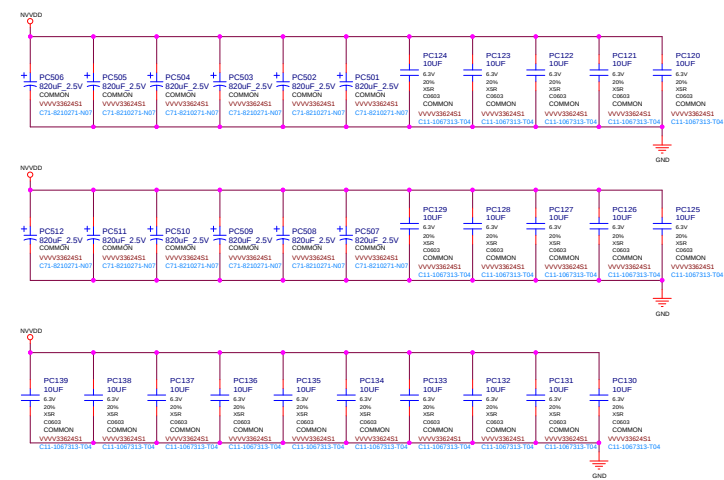


Backup





NVDD Output CAP





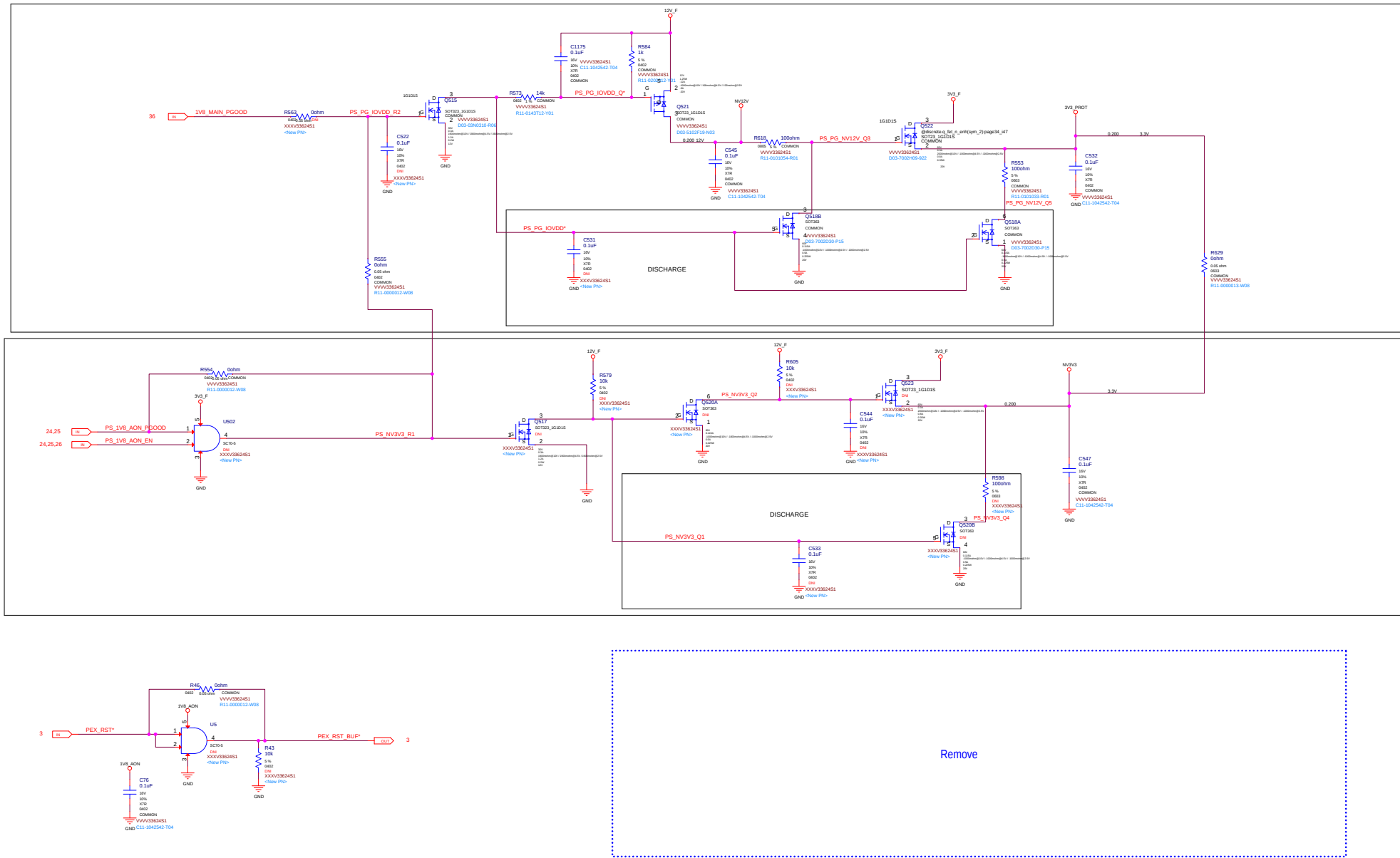
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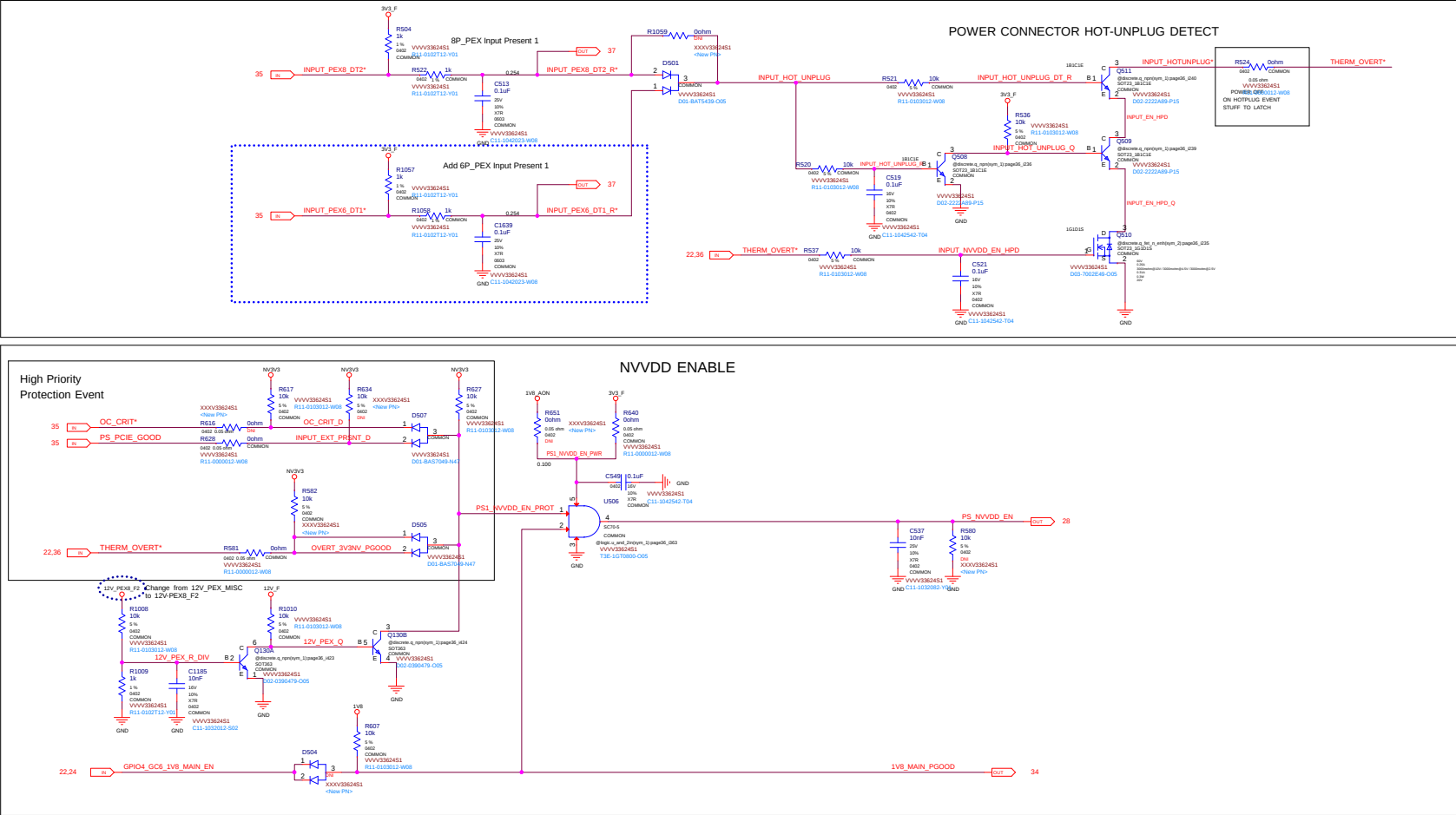


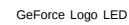
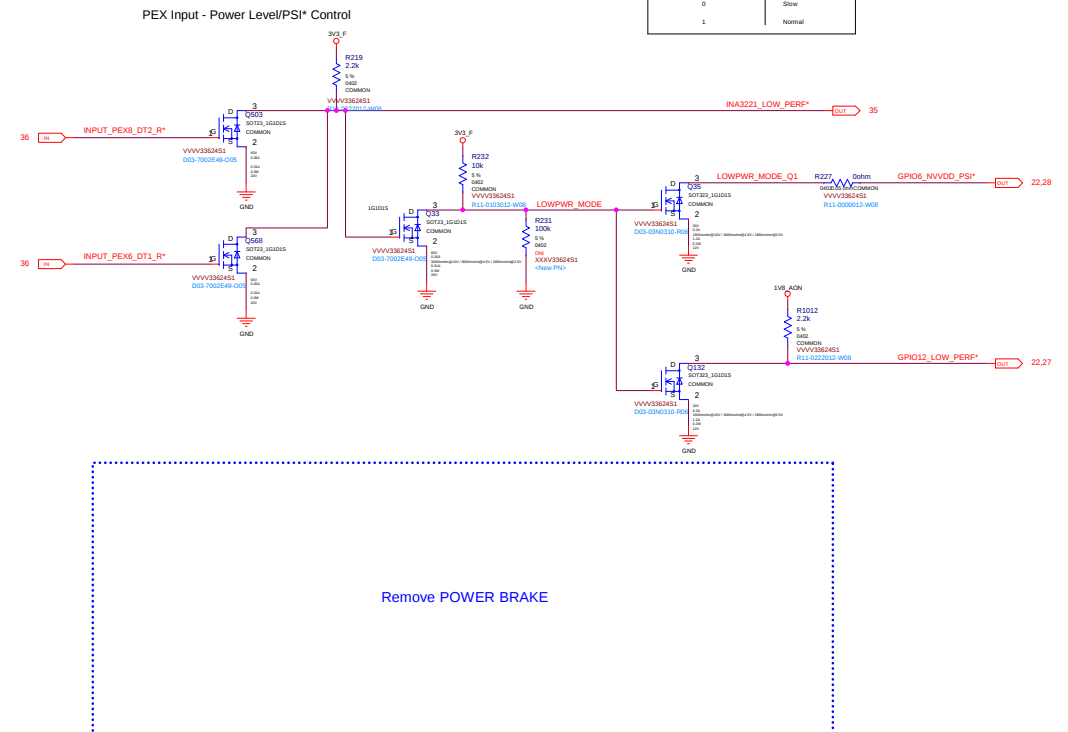
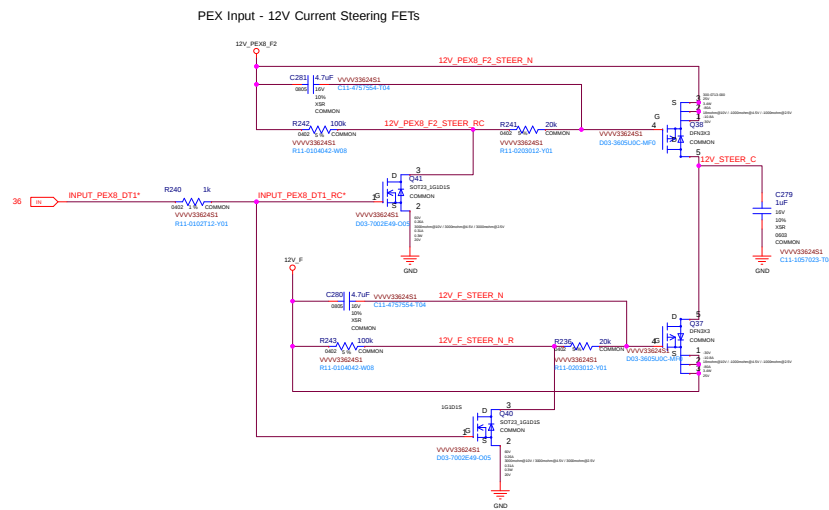
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Custom	PS: Dynamic Power Balance Logic		3.1
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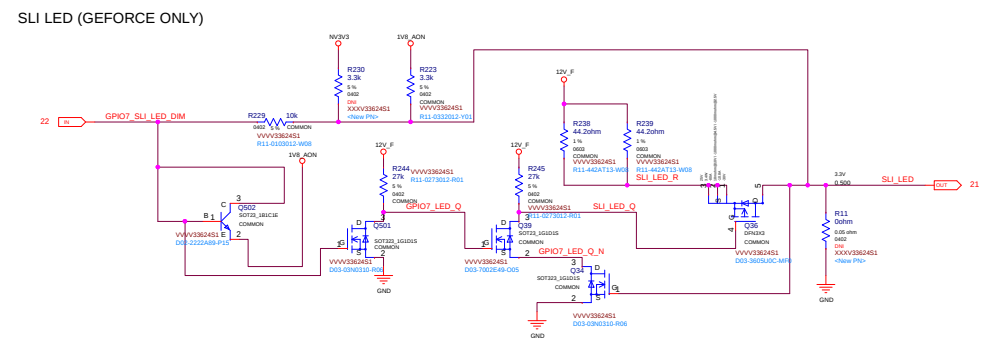






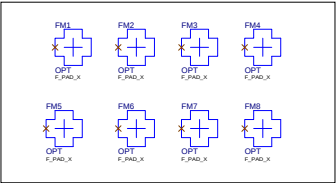
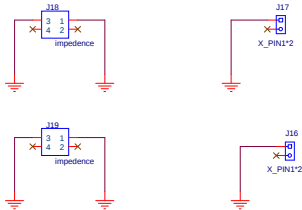
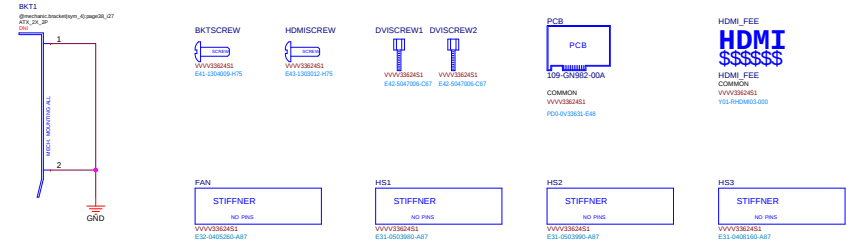
LED HEADER
(COMMON)

Remove Logo LED

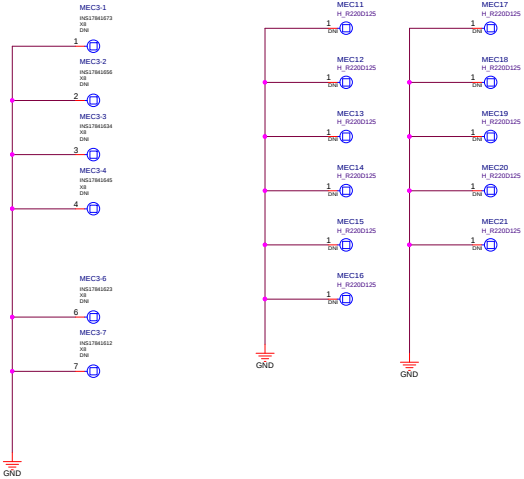


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MS-V336			
Size Custom	Document Description PS: 12V Current Steering, PSI Control, and LED		Rev 3.1
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Brackets:



GPU Stiffner





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