PG611 A00

12GB GDDR5X, 384b, 256Mx32
TALL DVI-D + DP + DP + HDMI/DP + DP

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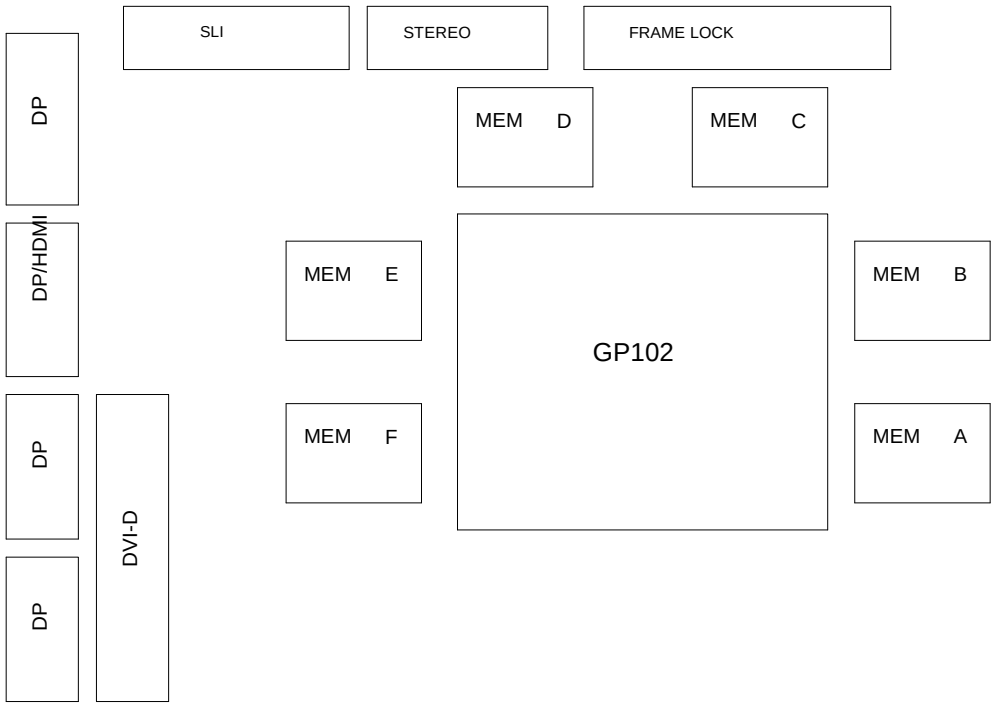

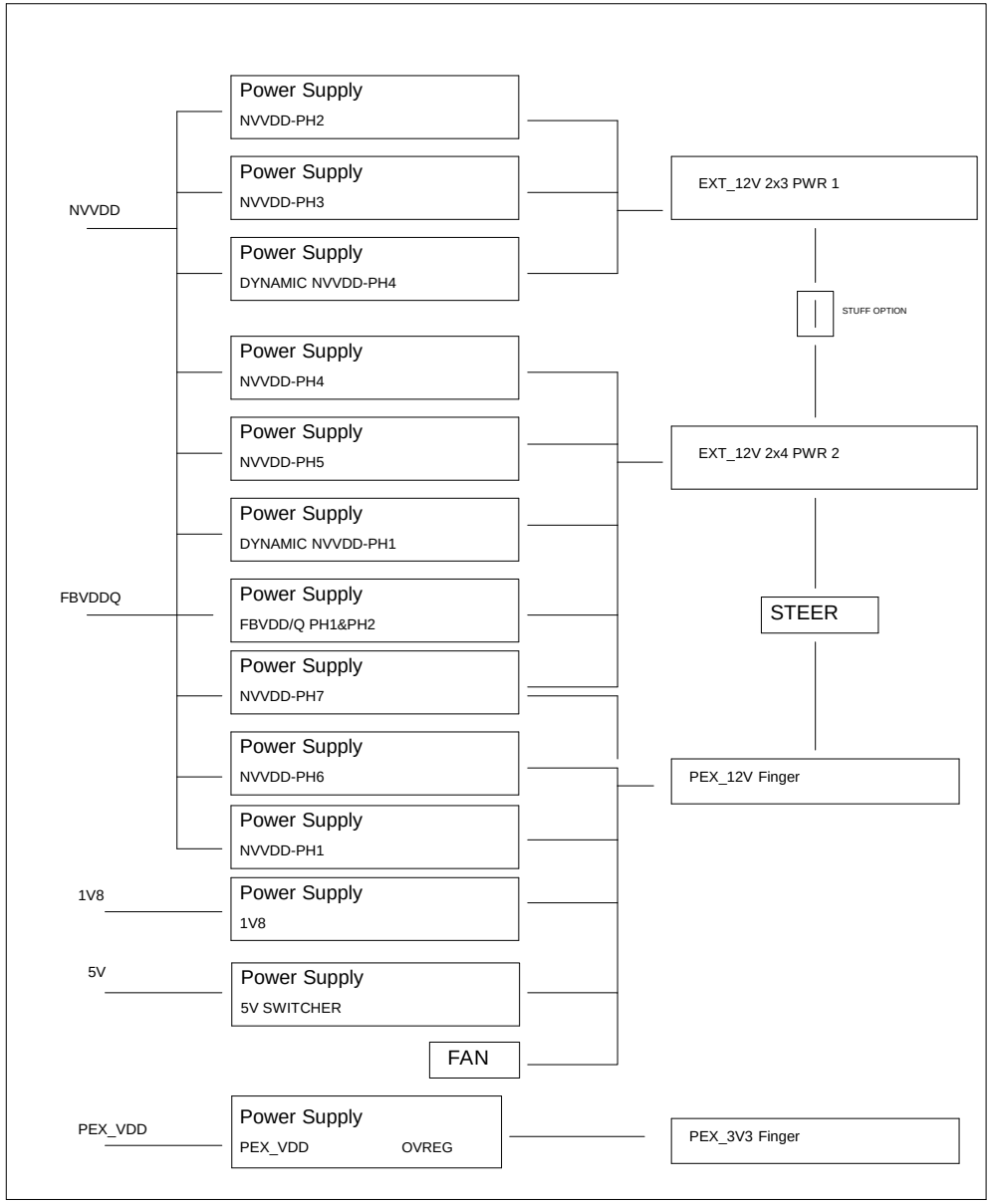

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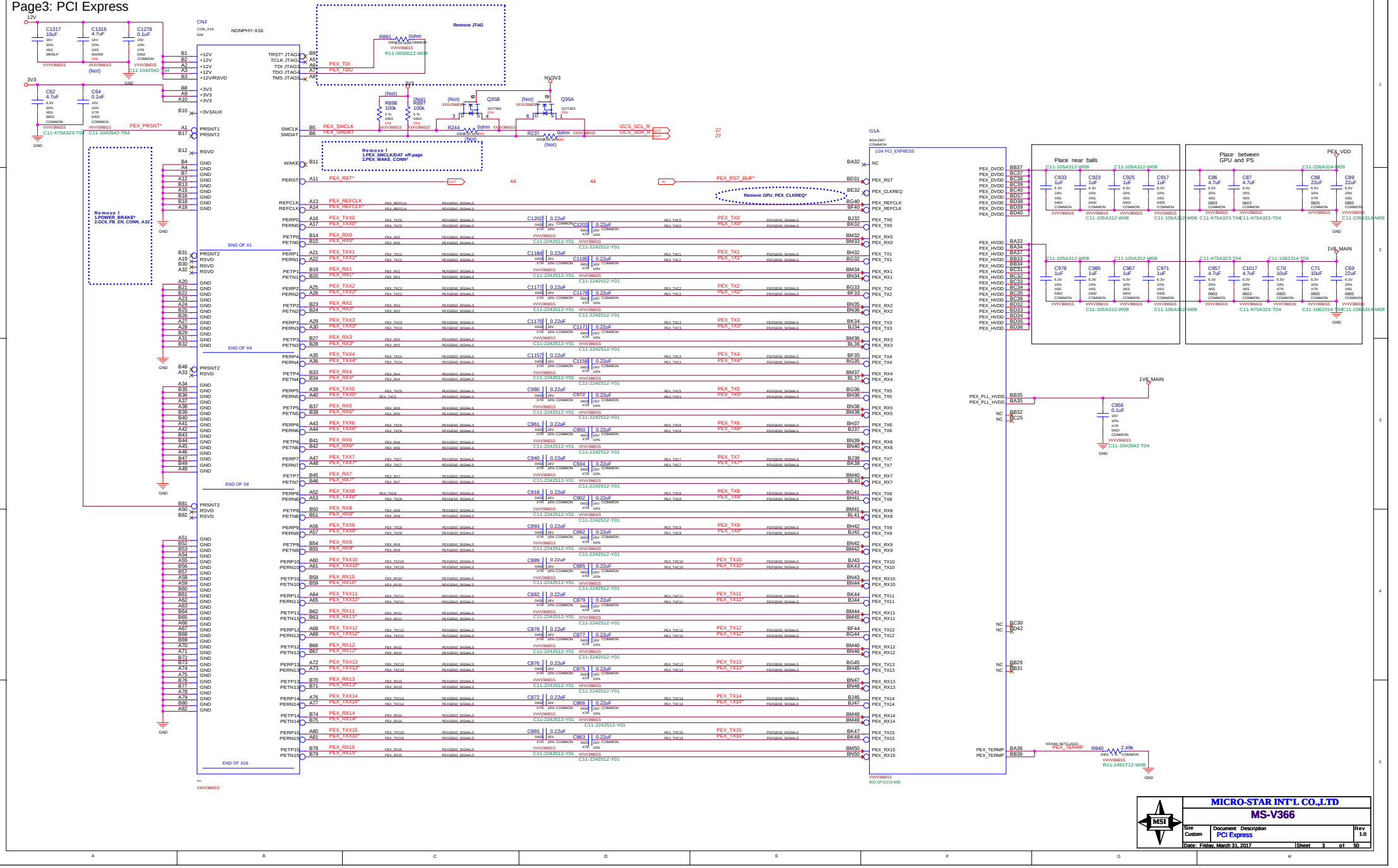

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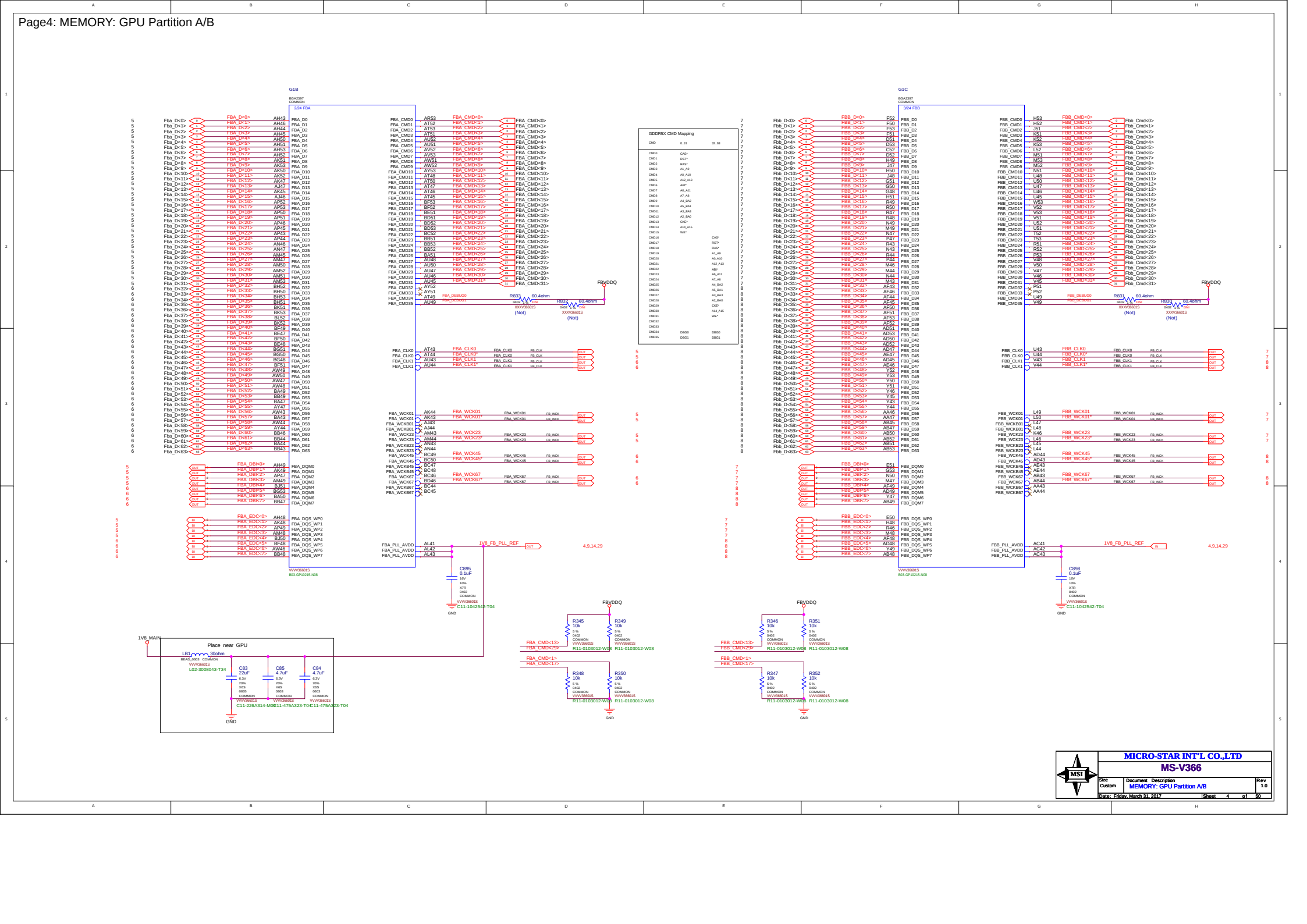

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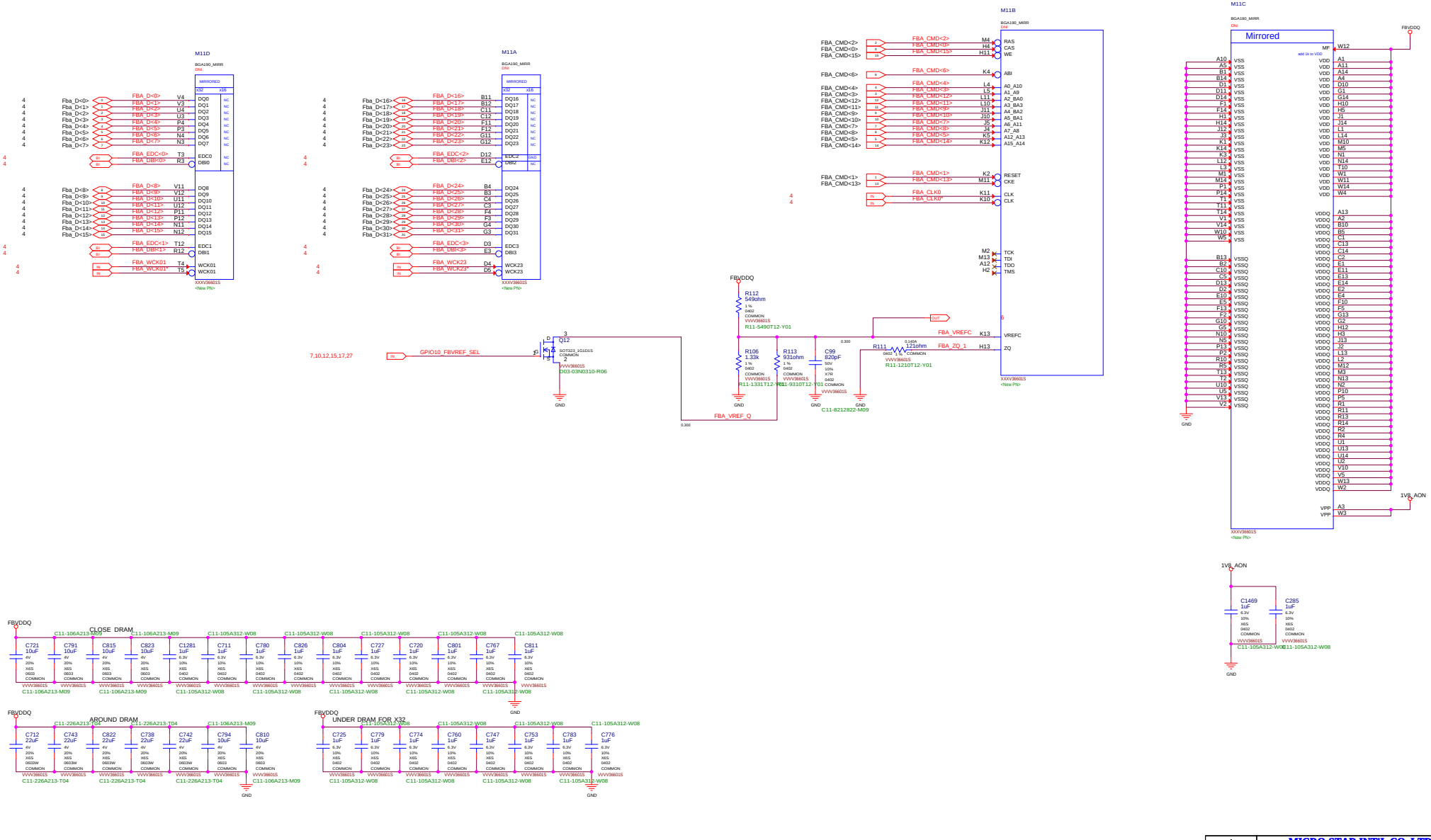

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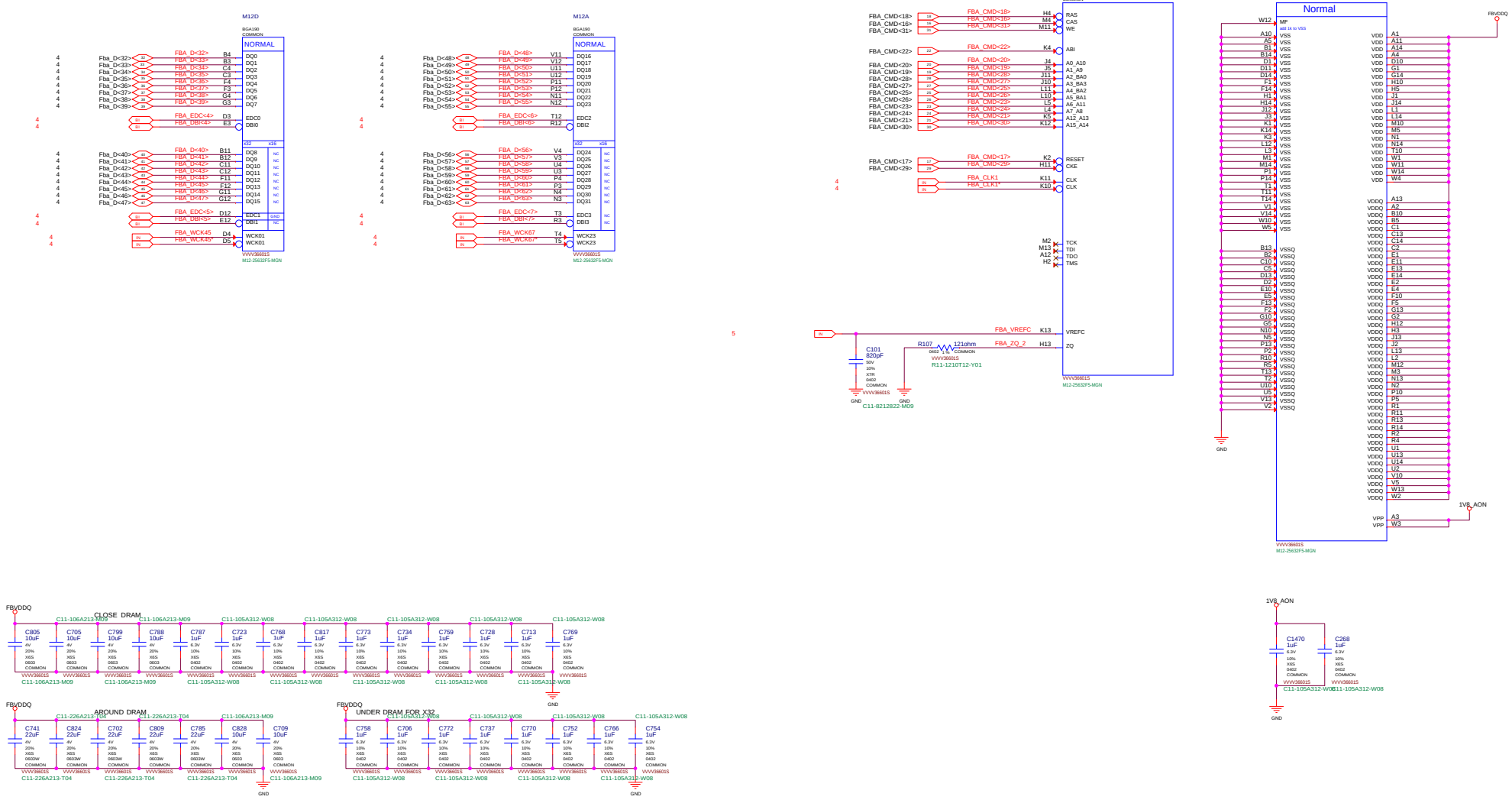

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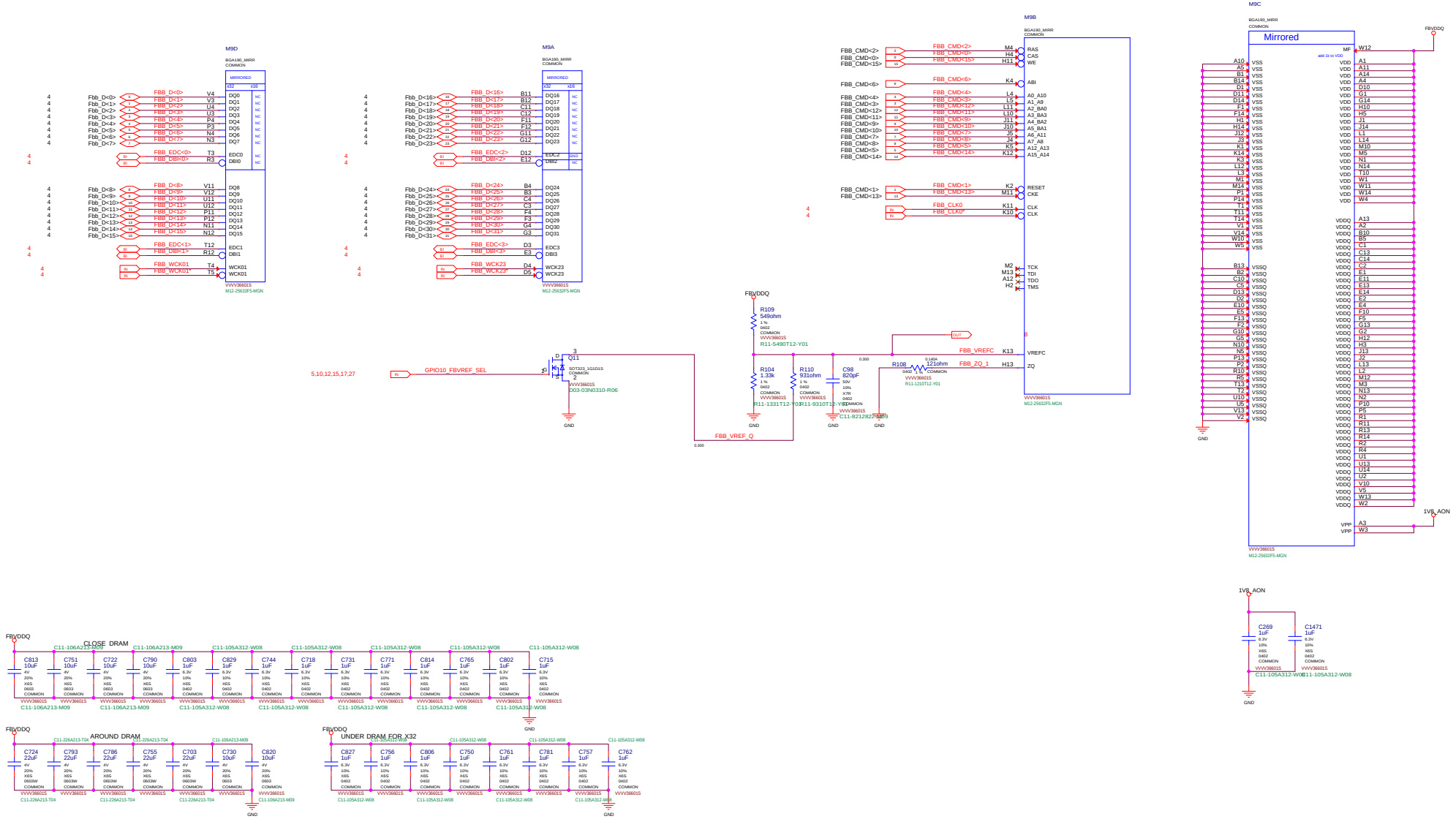

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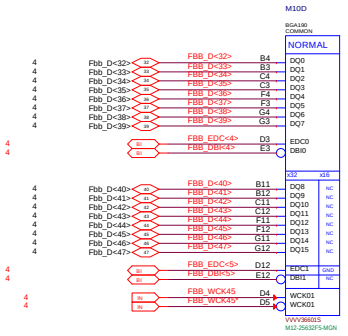

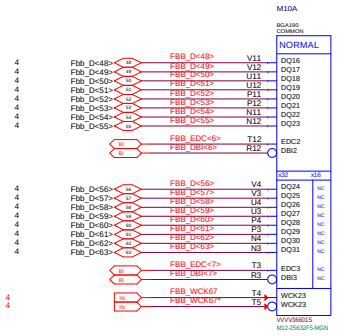

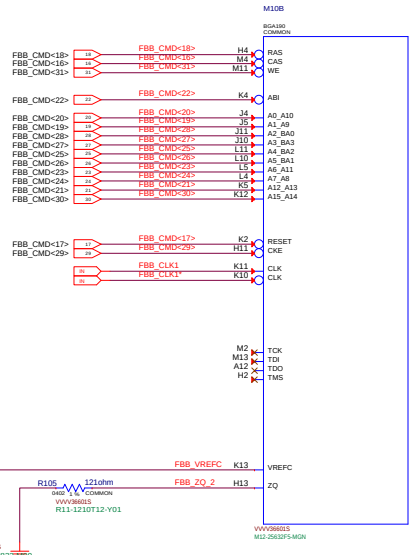

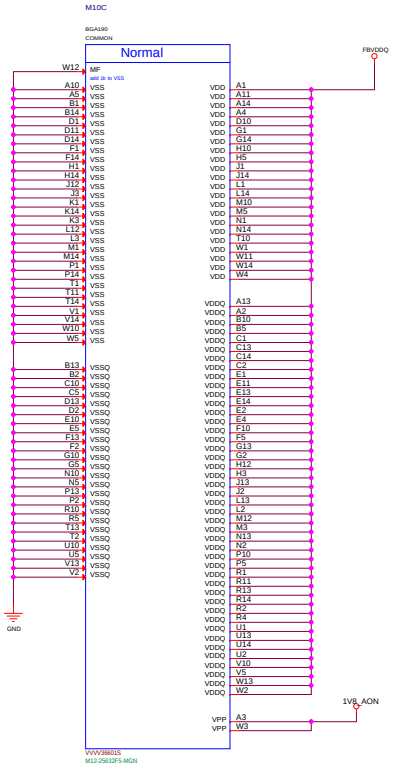

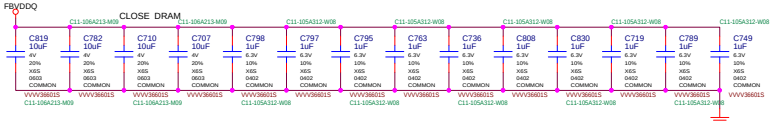

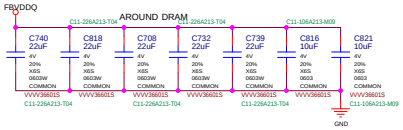

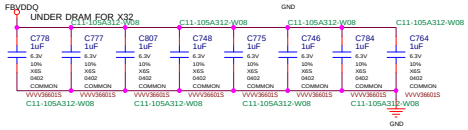

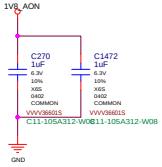

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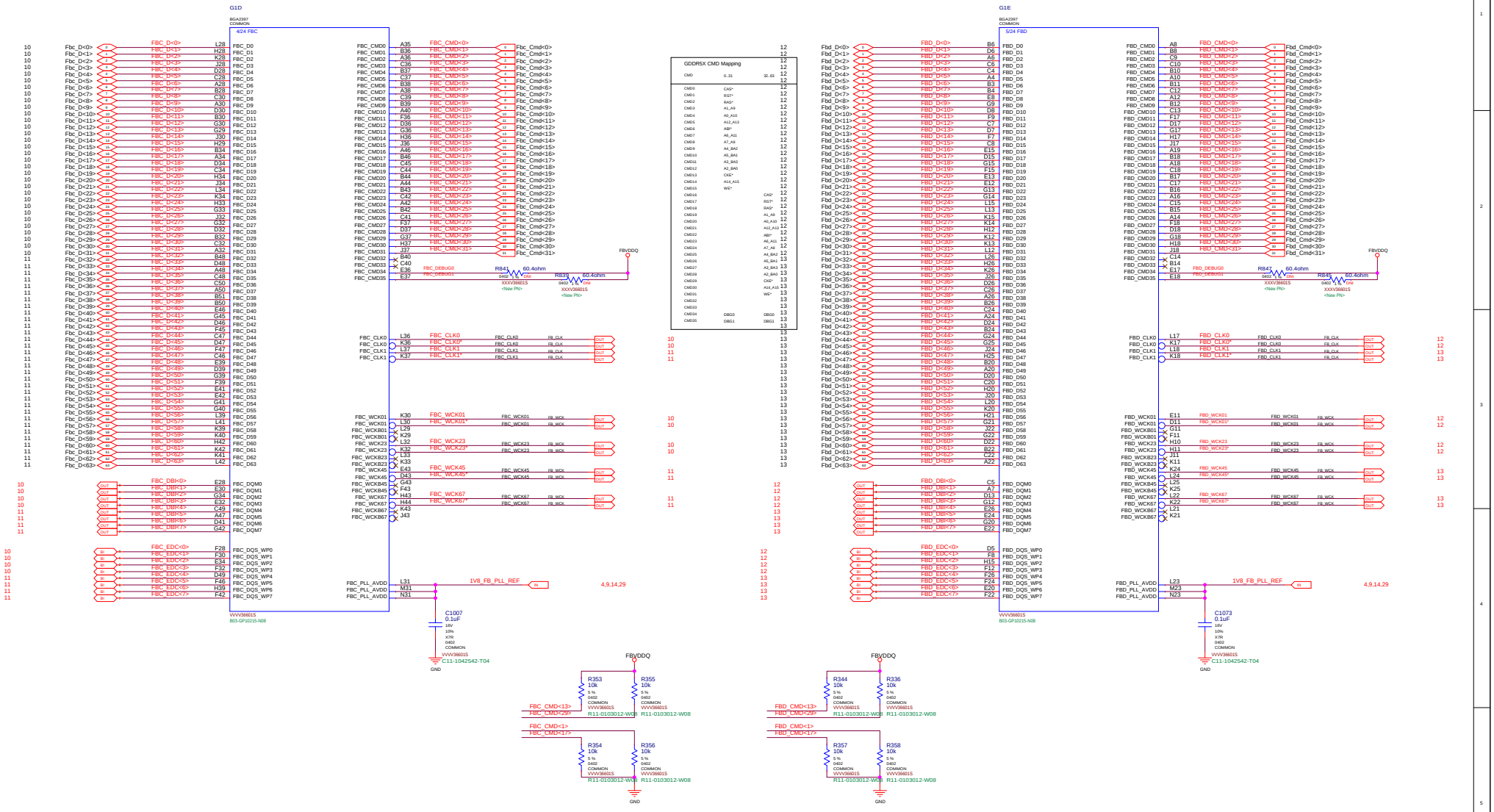

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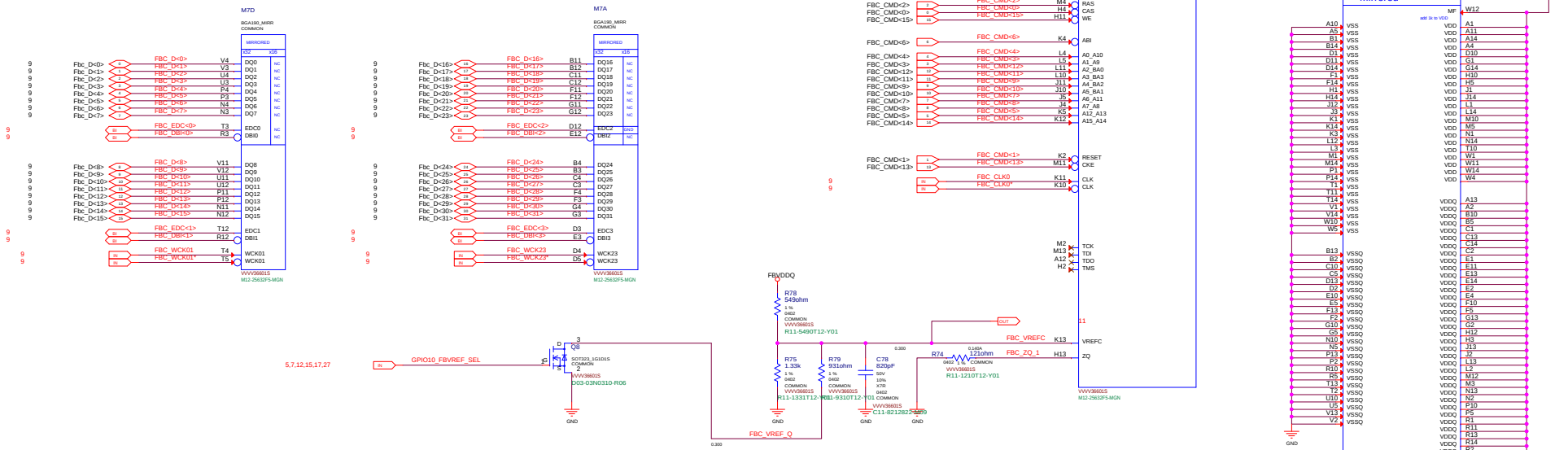

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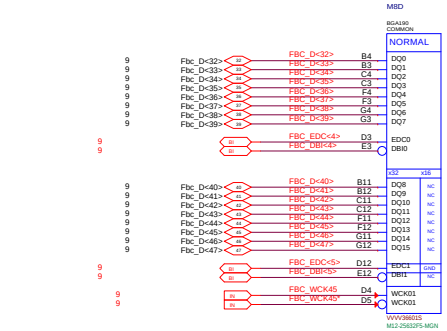

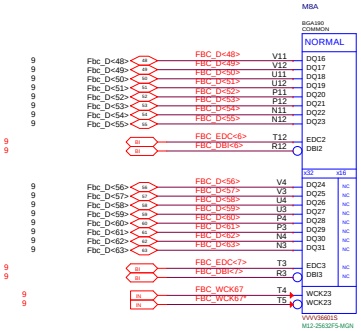

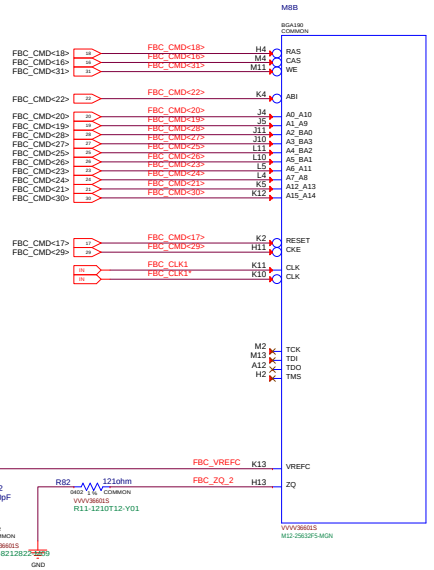

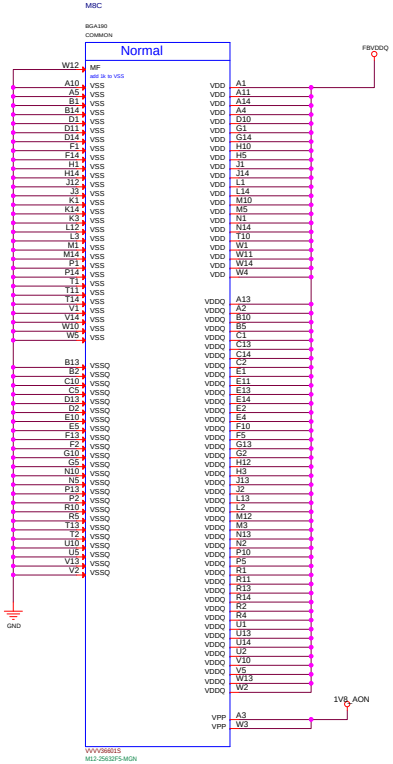

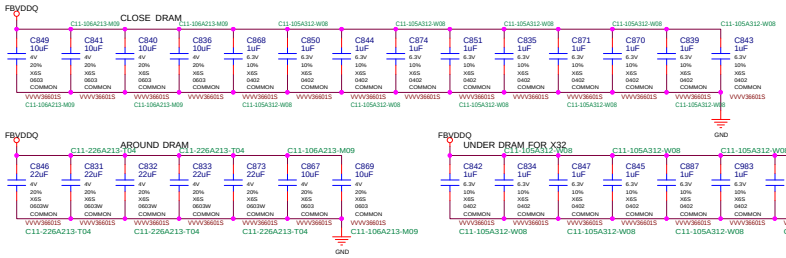

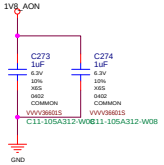

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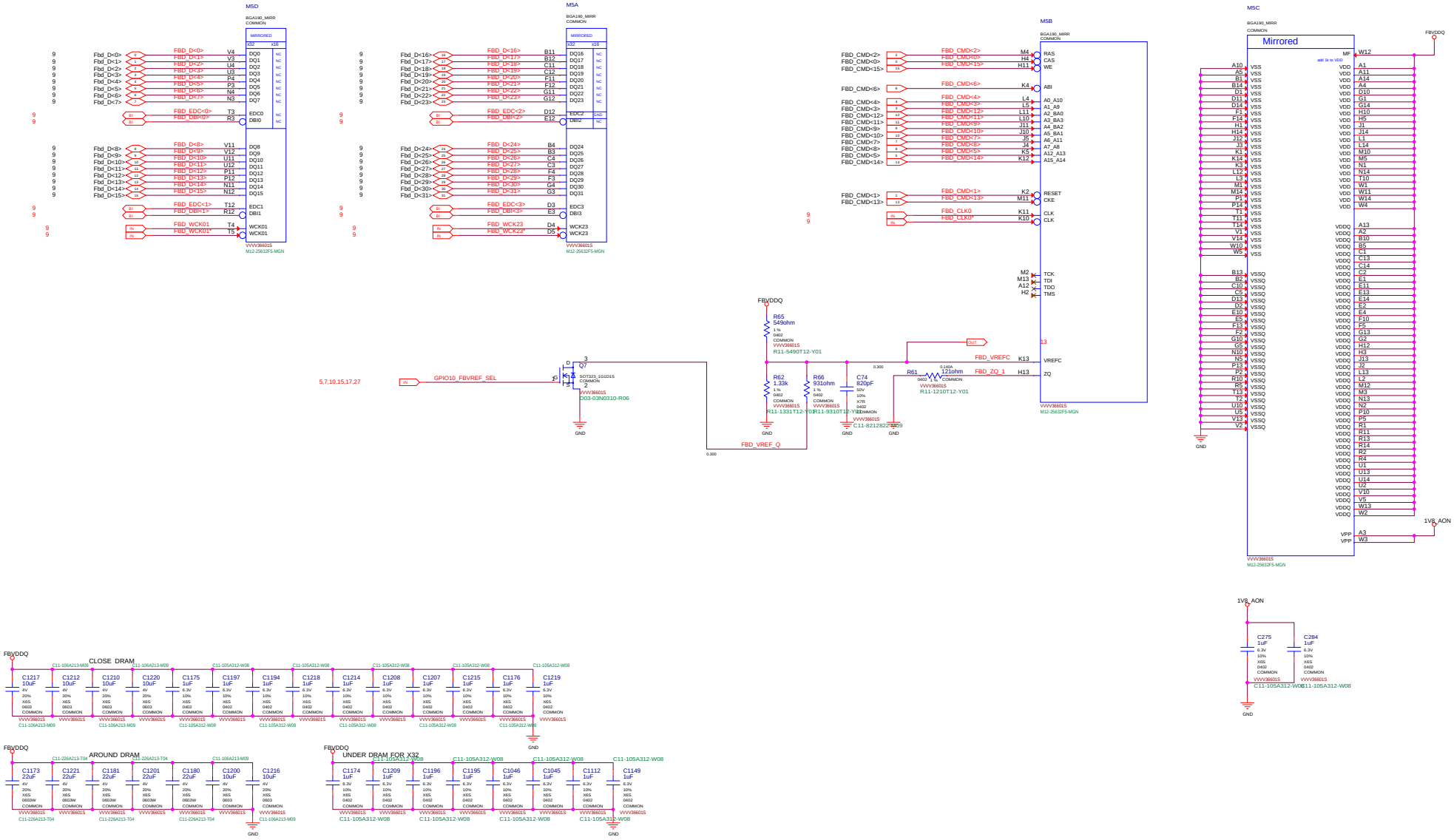

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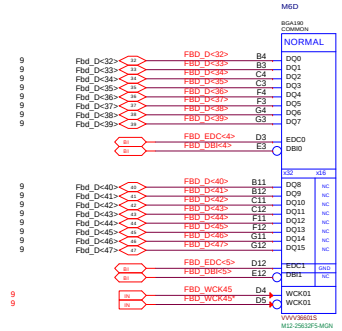

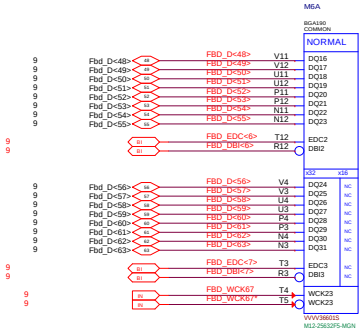

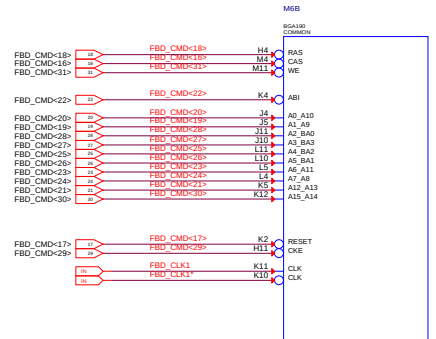

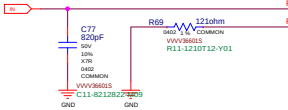

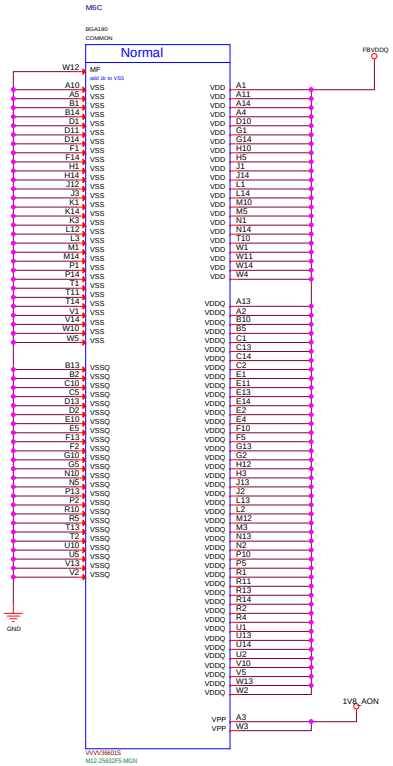

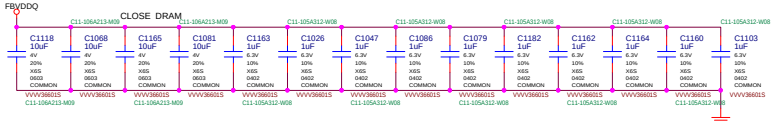

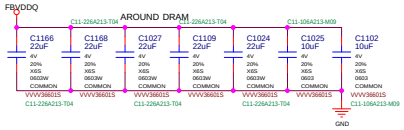

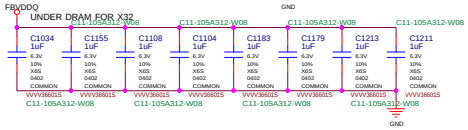

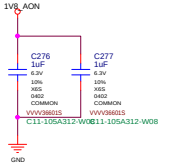

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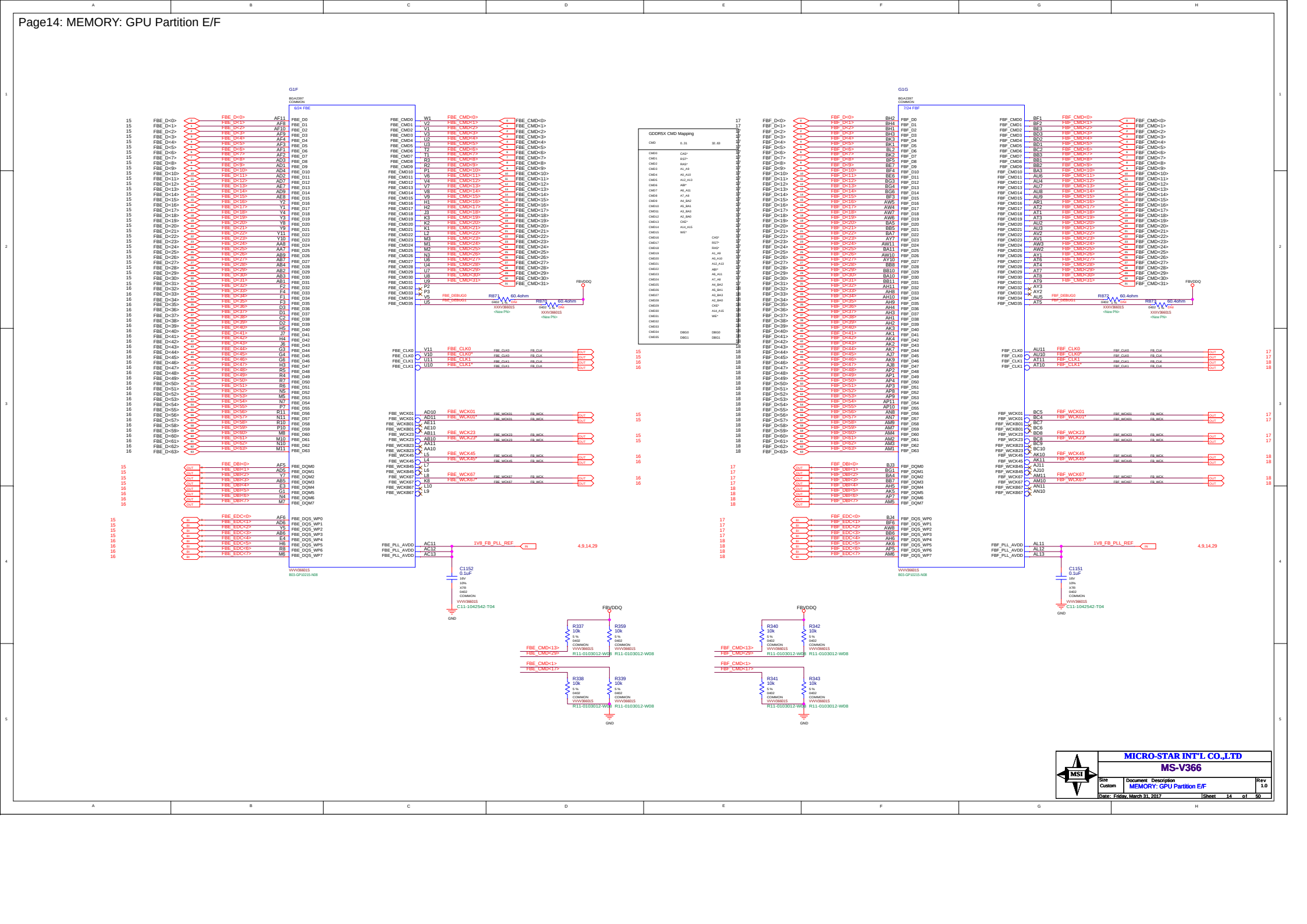

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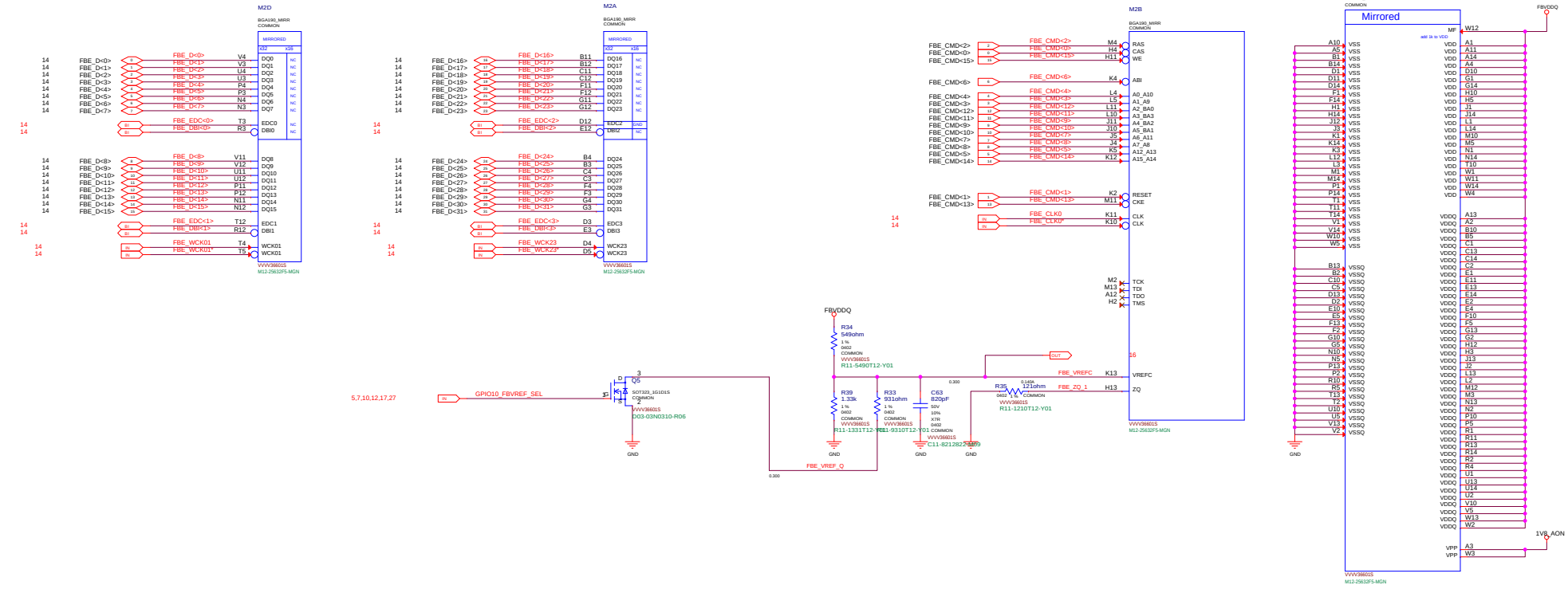

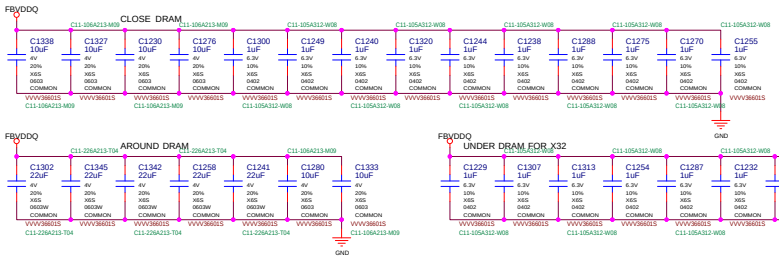

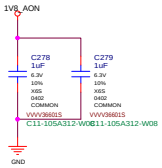

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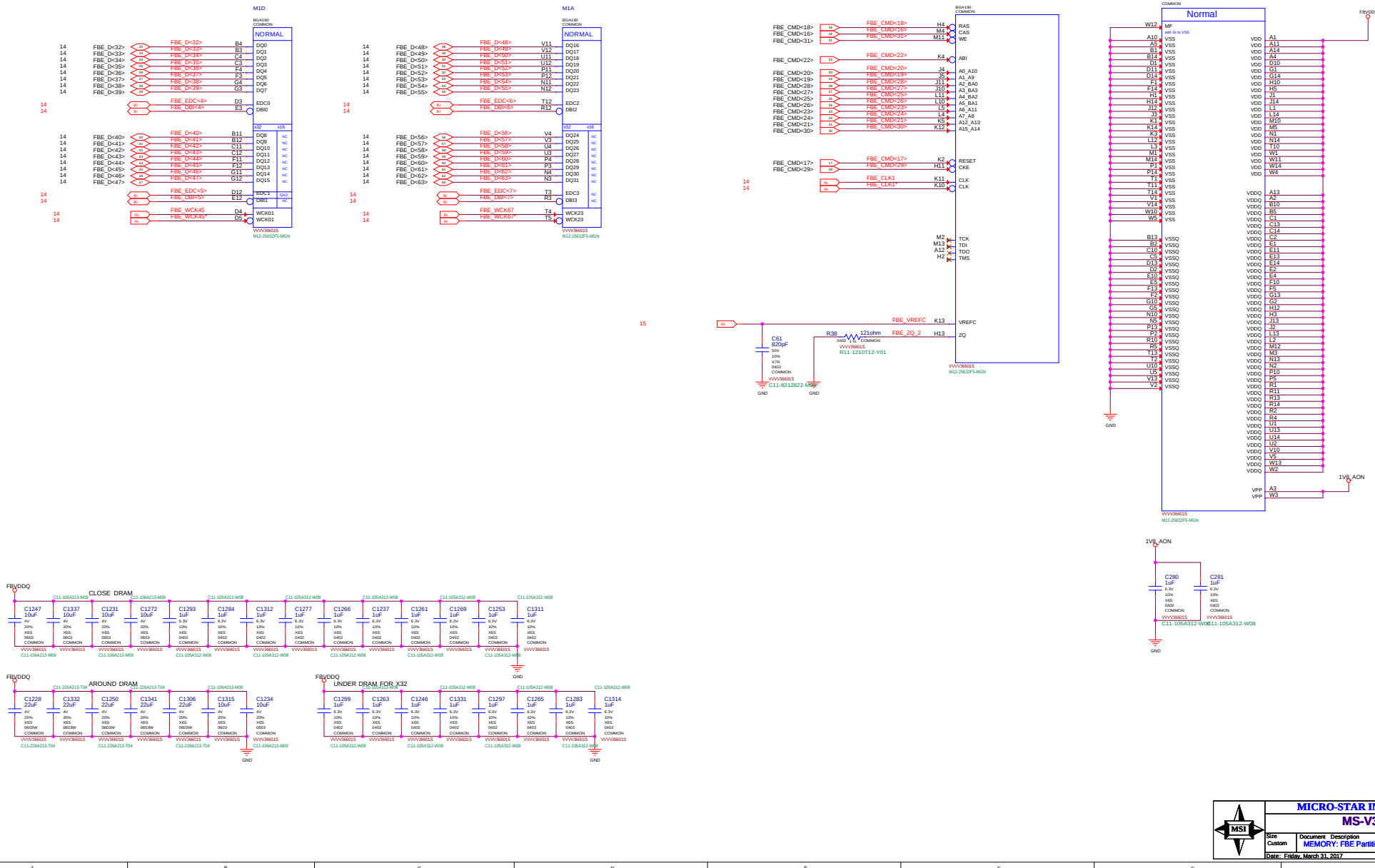

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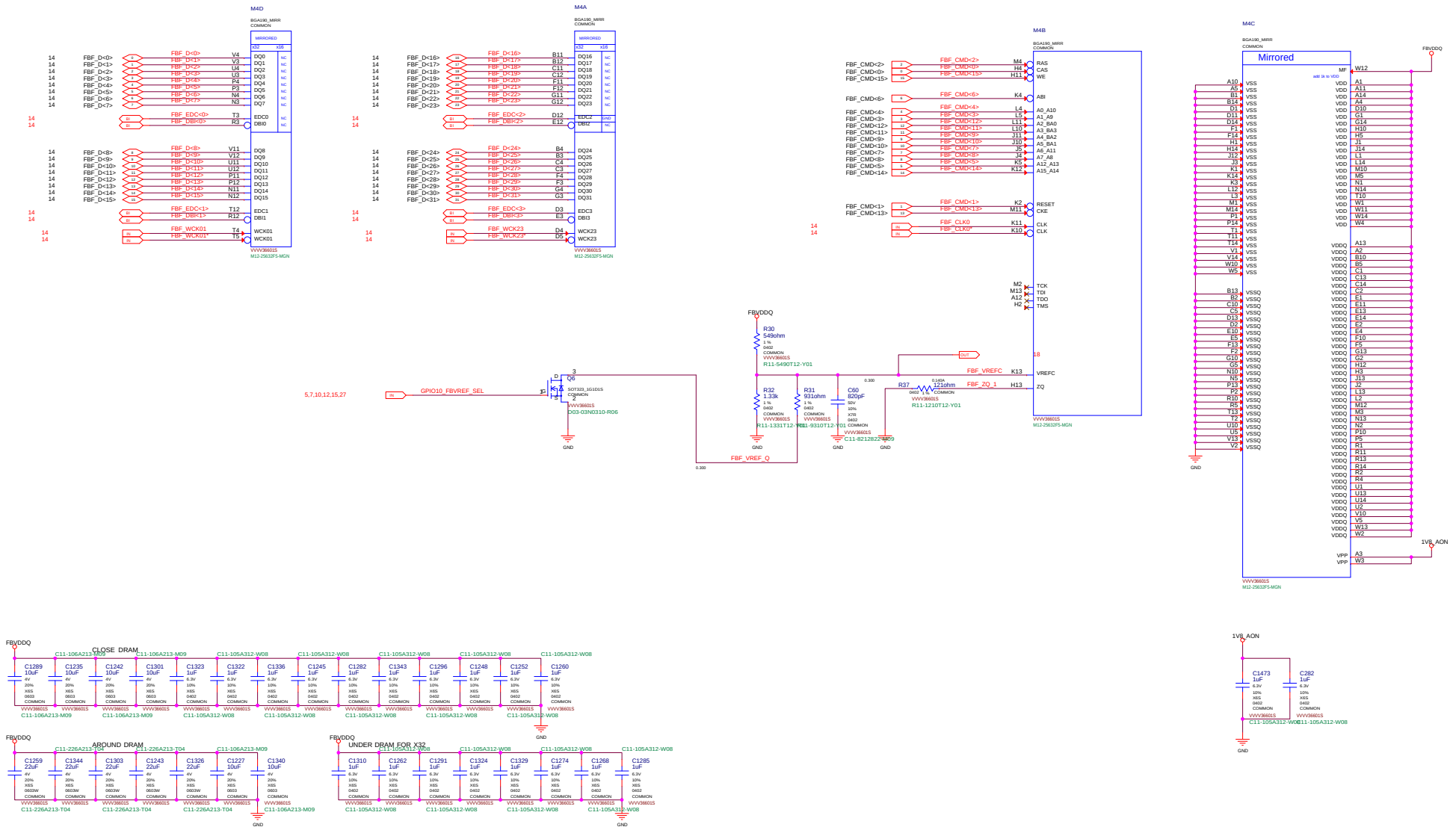

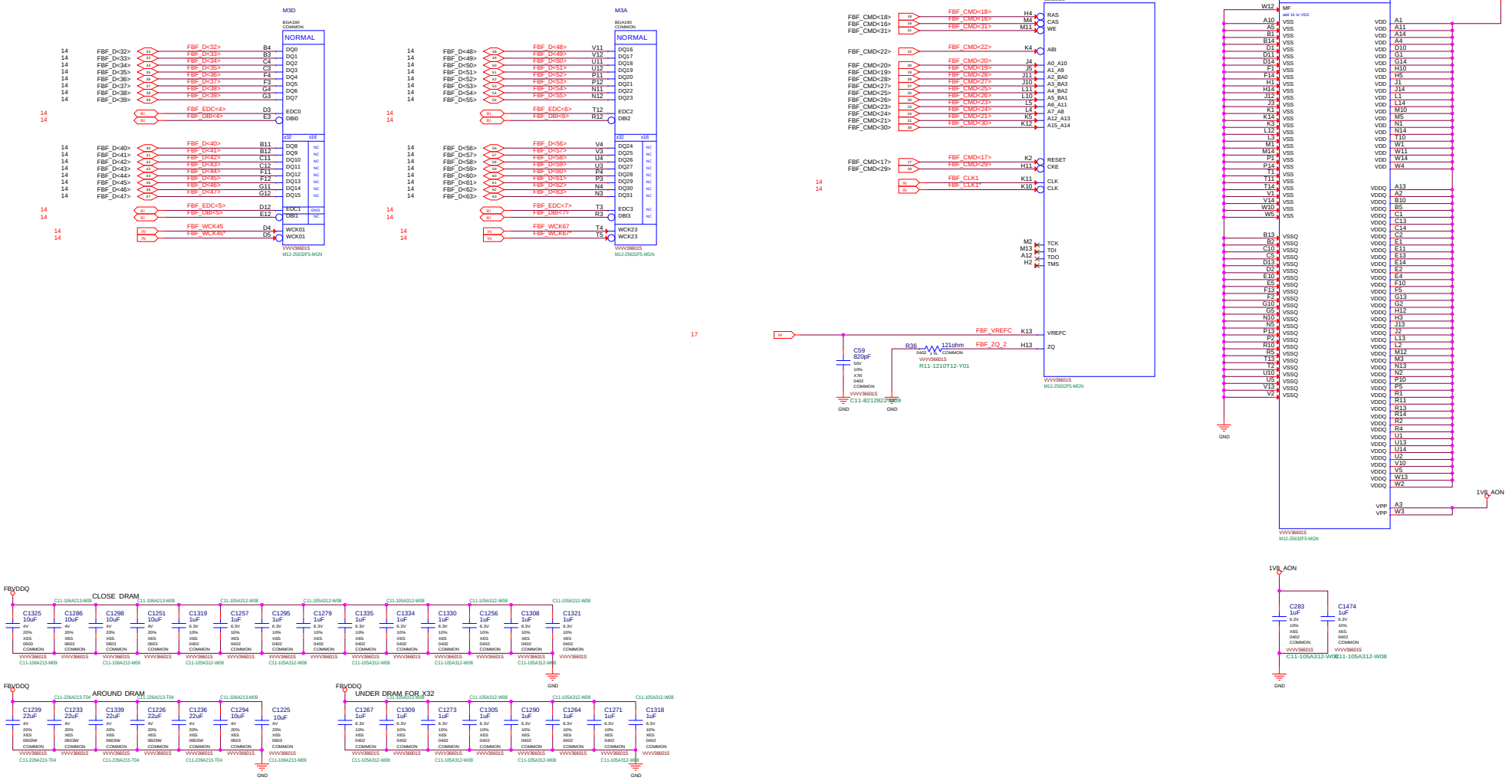

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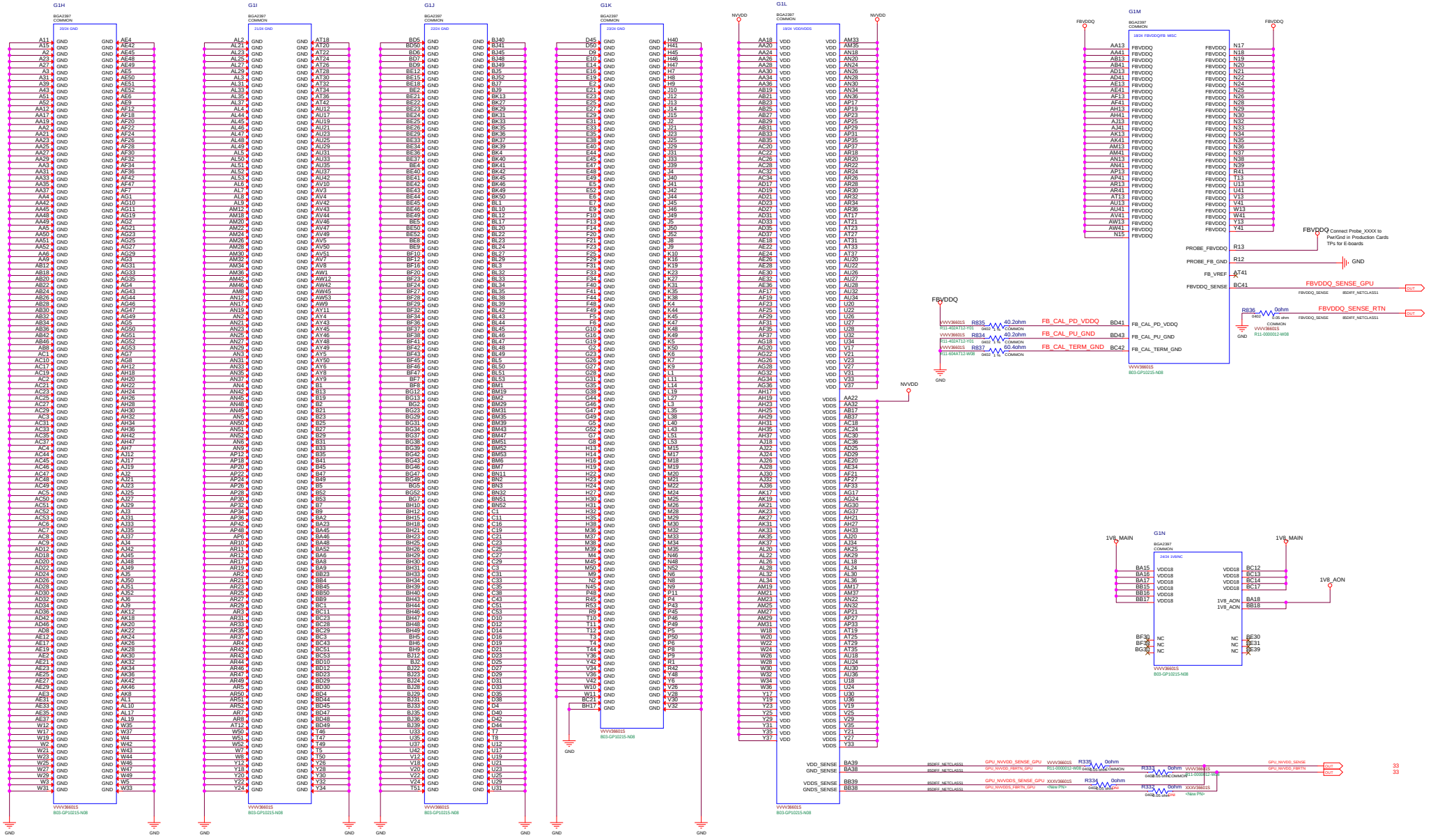

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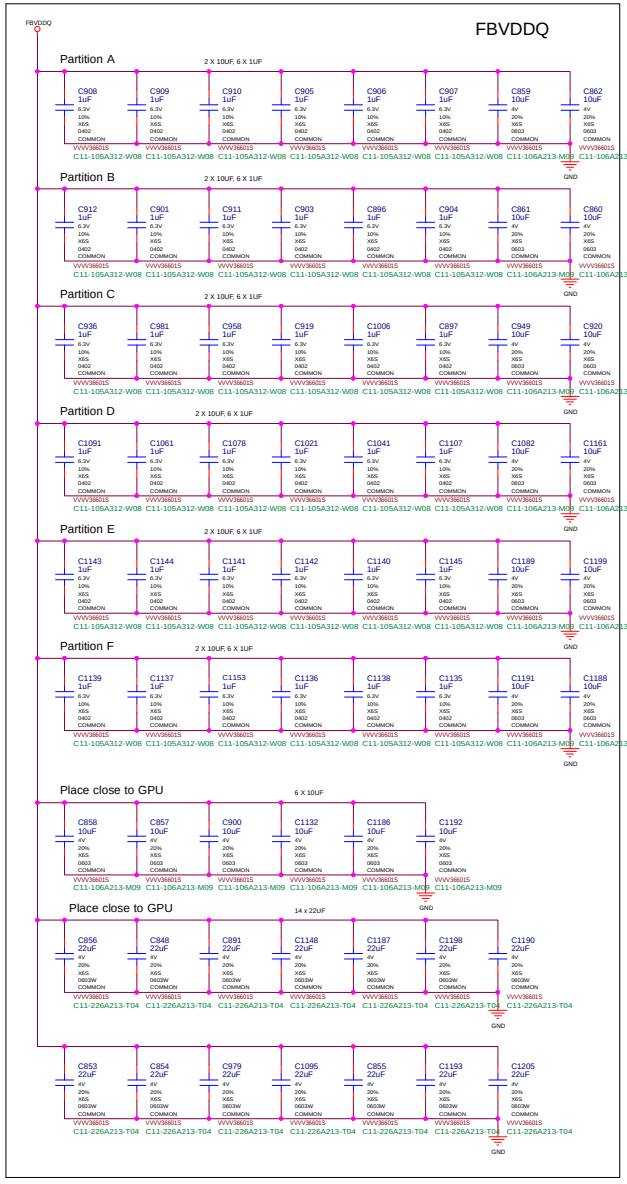

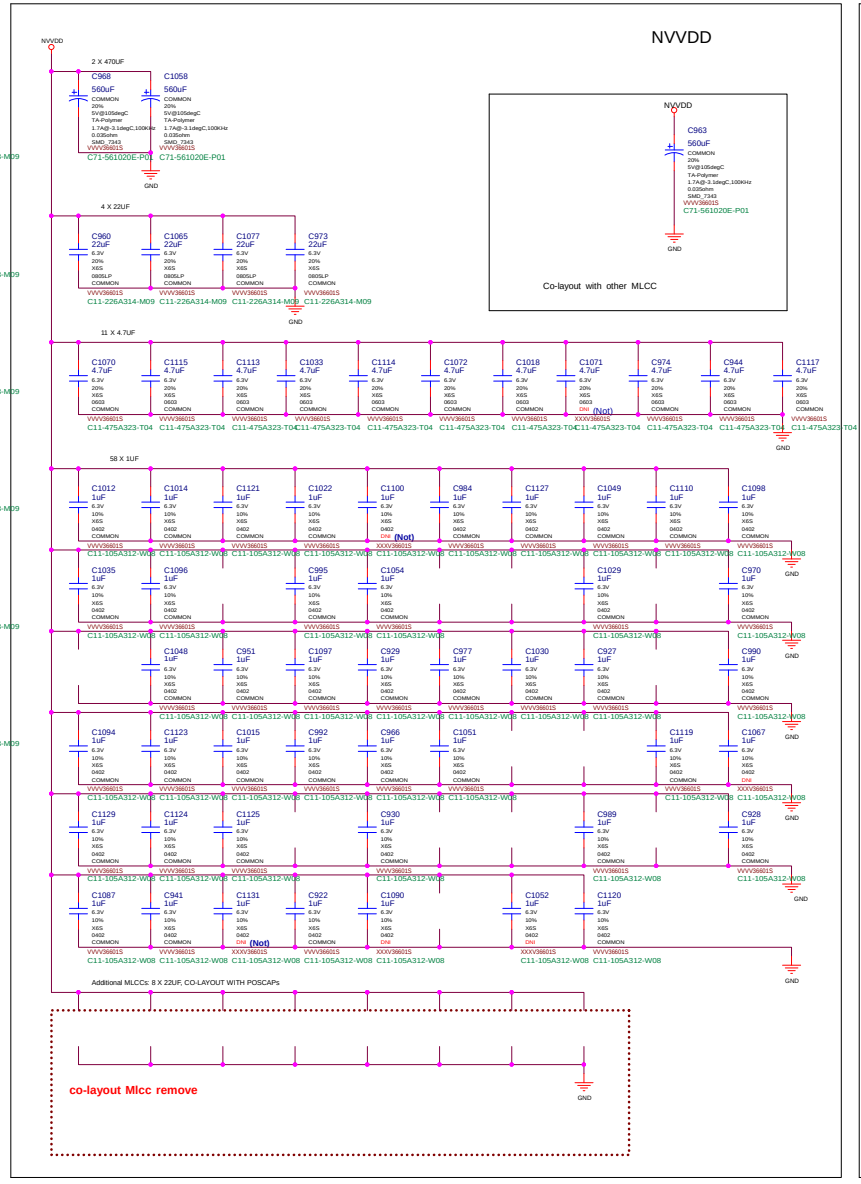

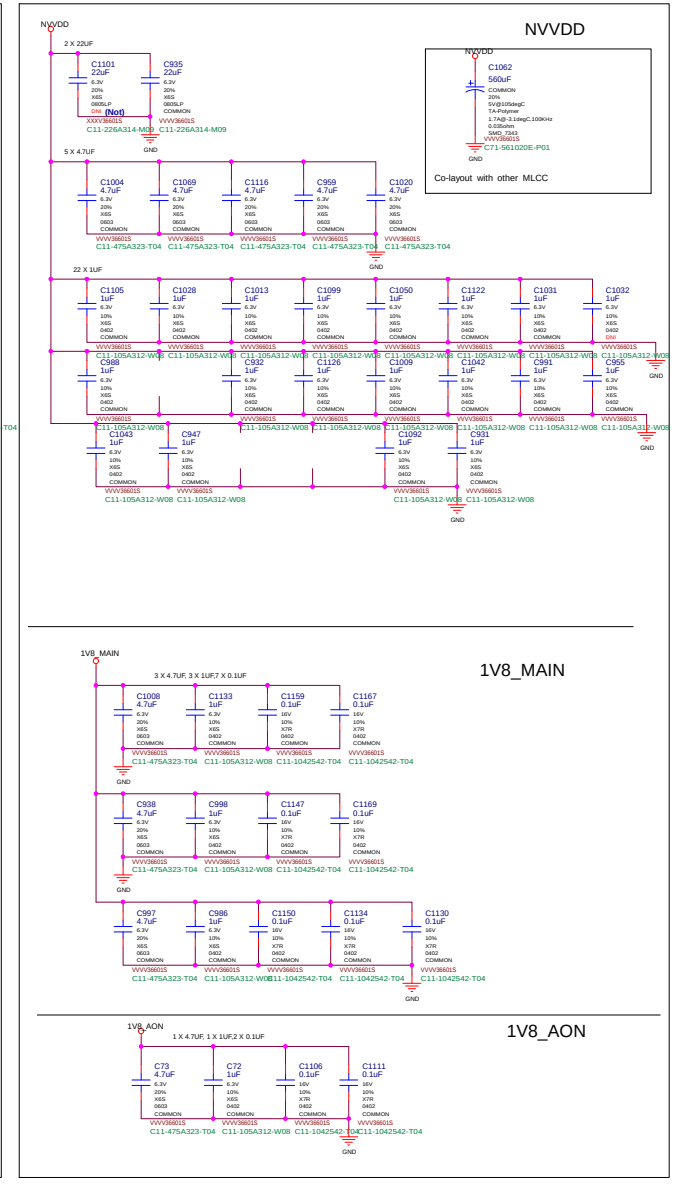

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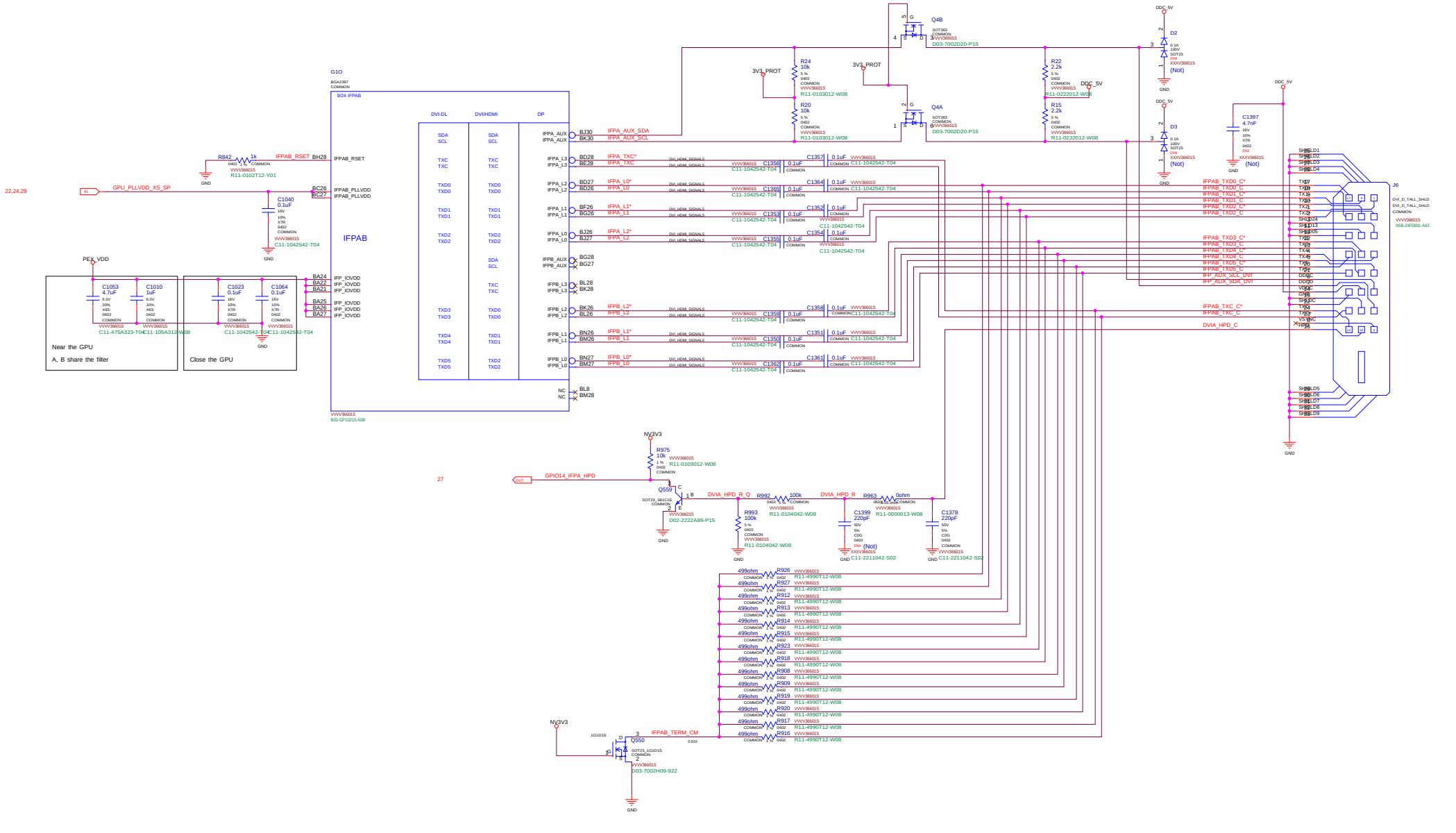

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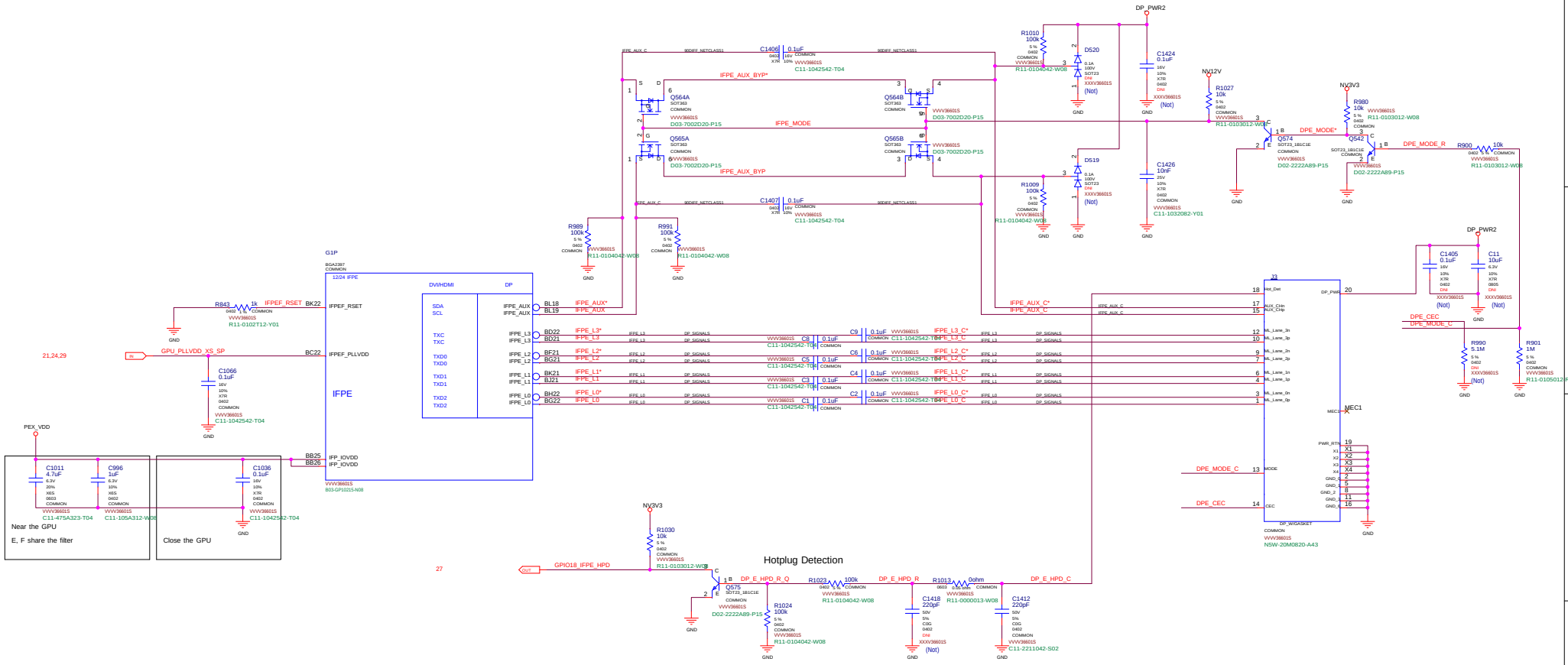
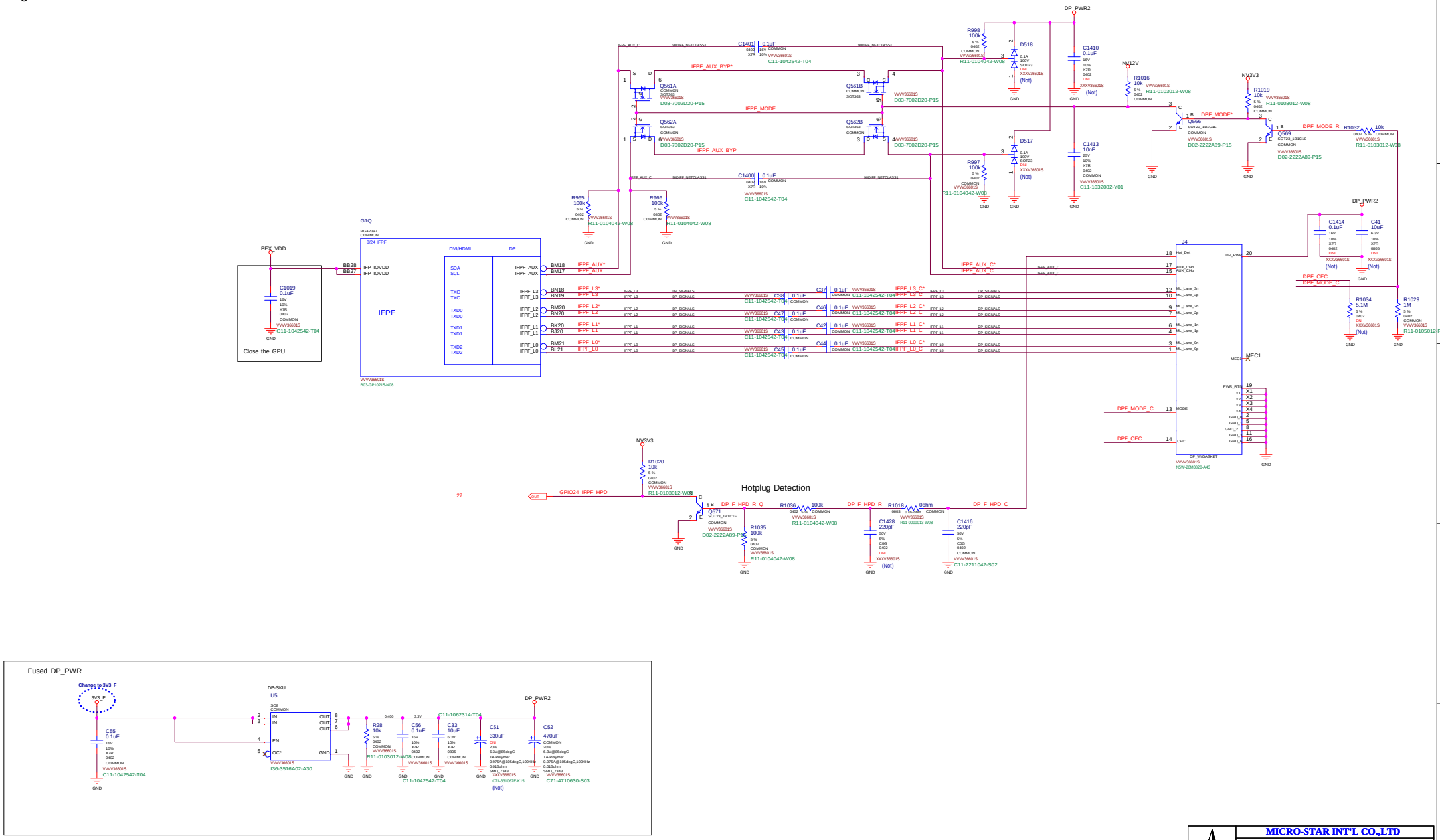


Page23: IFPF DP



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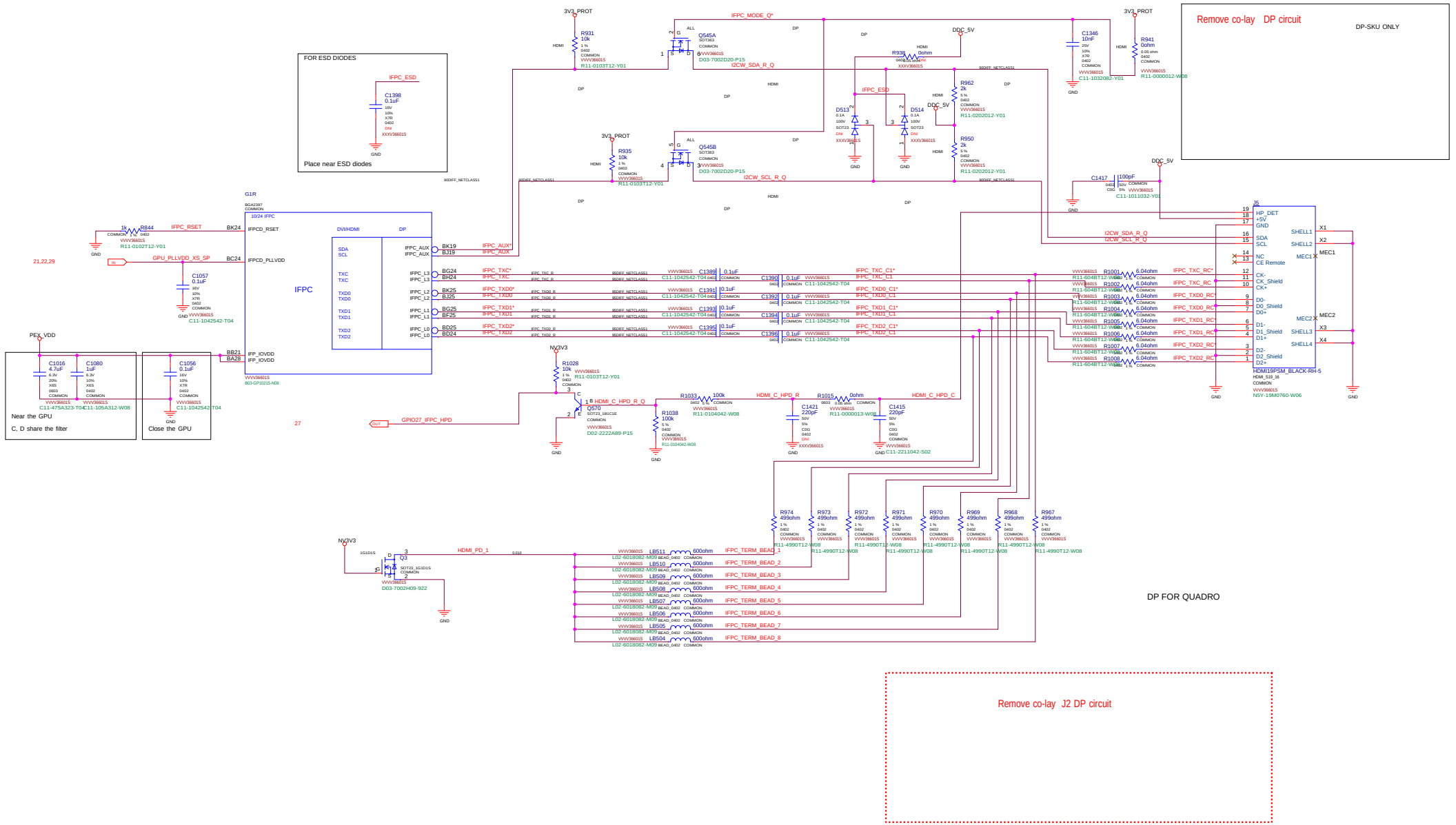

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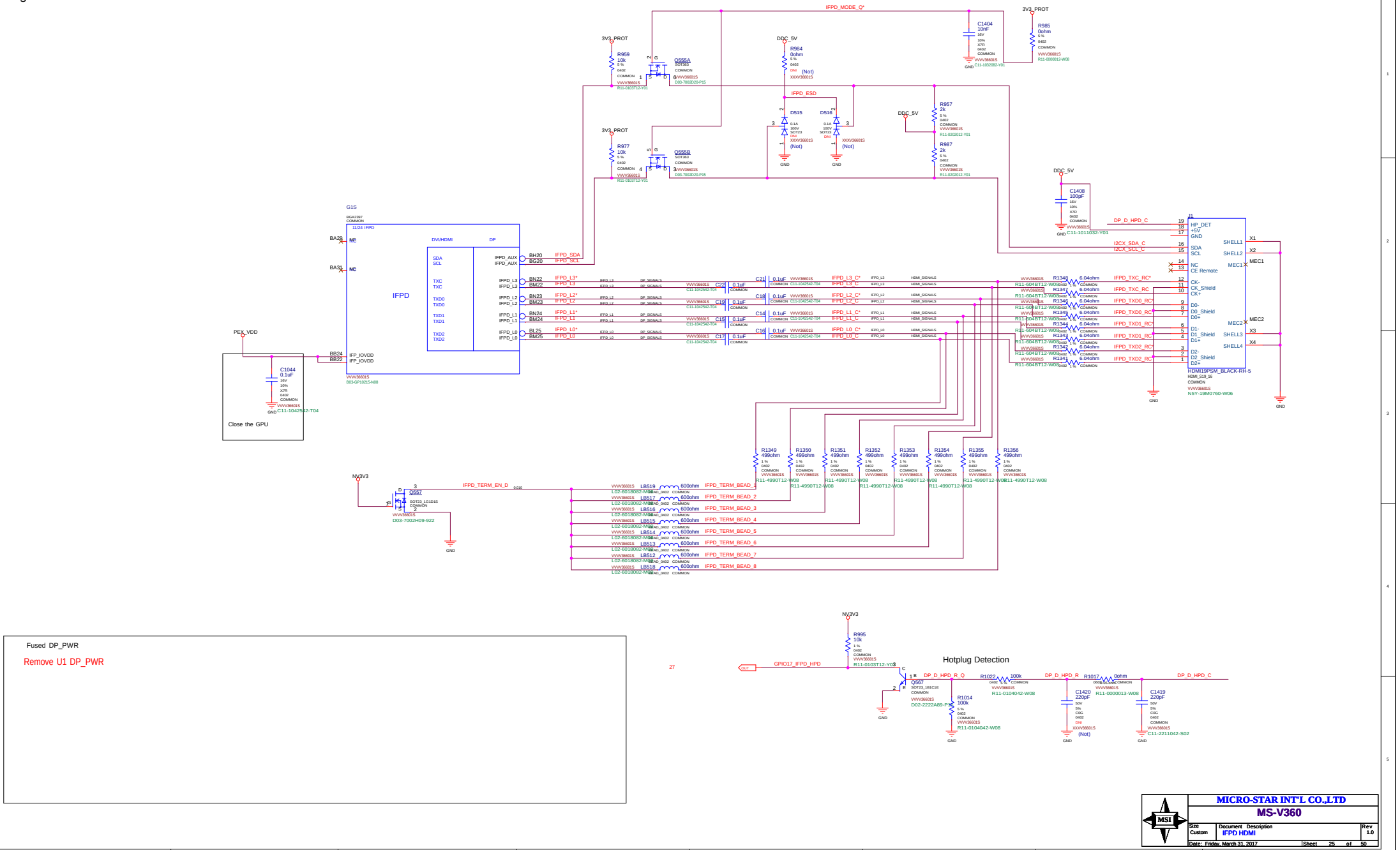

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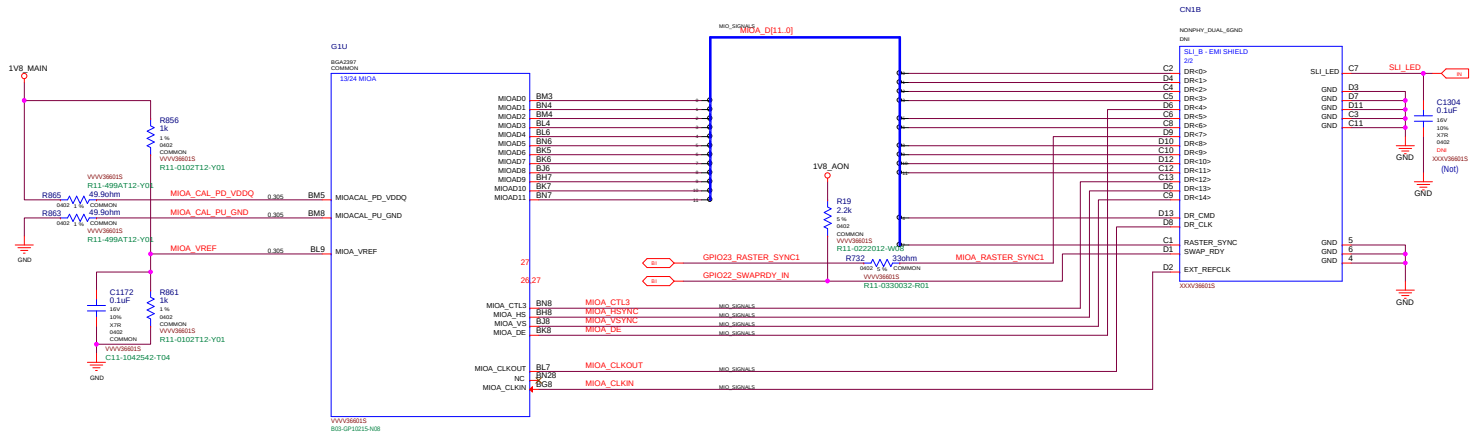

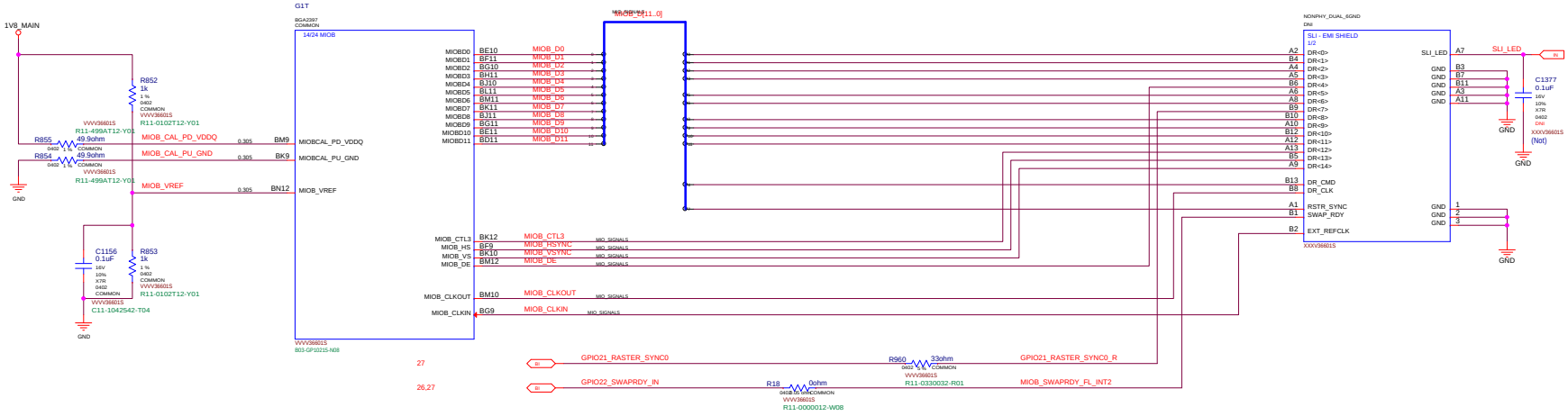

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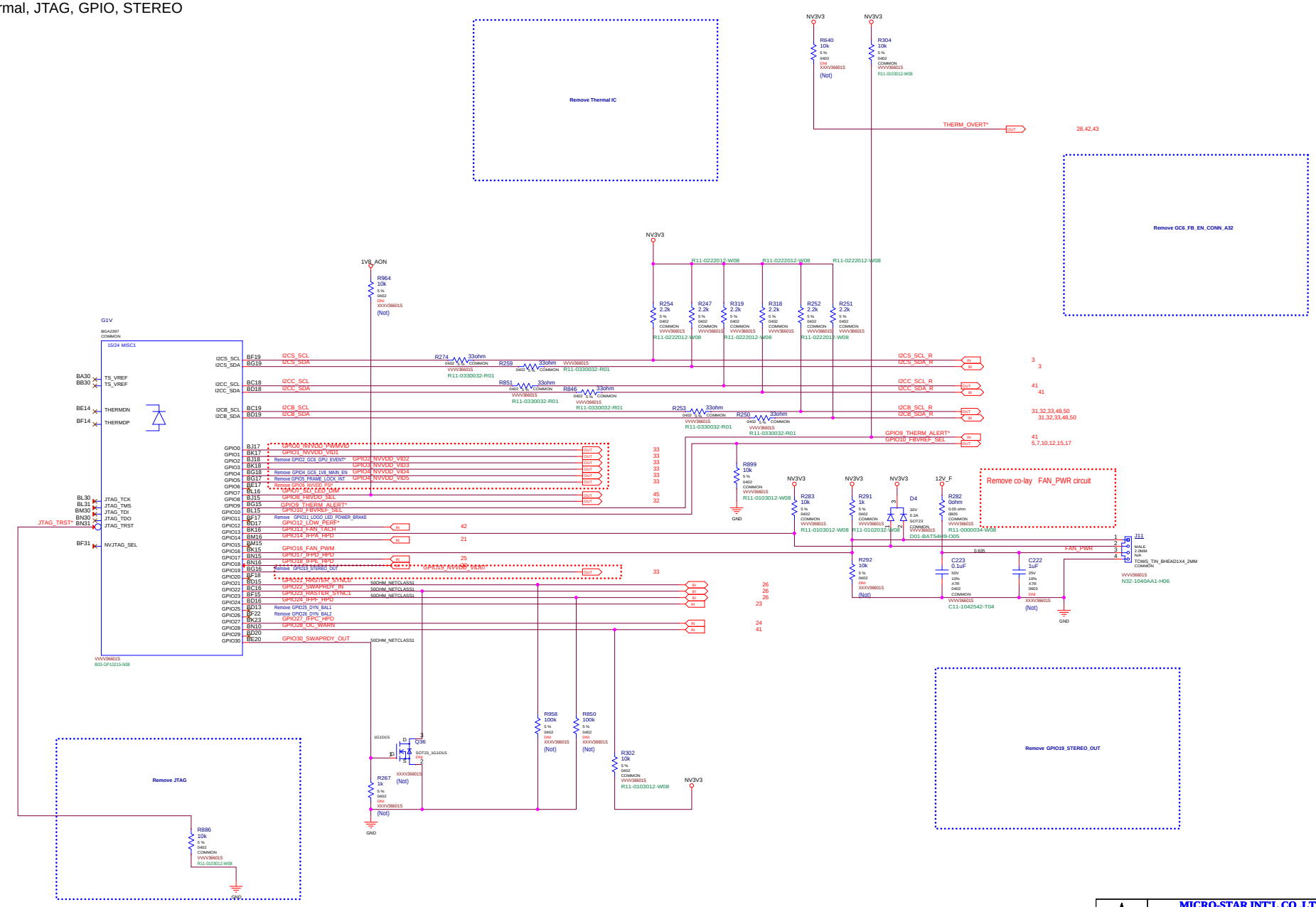
Page27: MISC1: Fan, Thermal, JTAG, GPIO, STEREO



Page28: MISC2: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

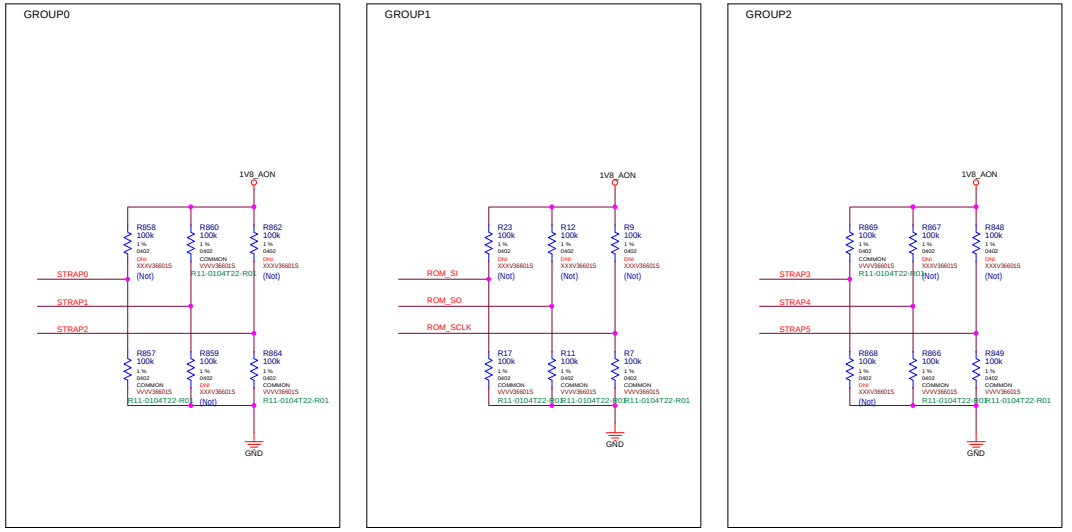
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

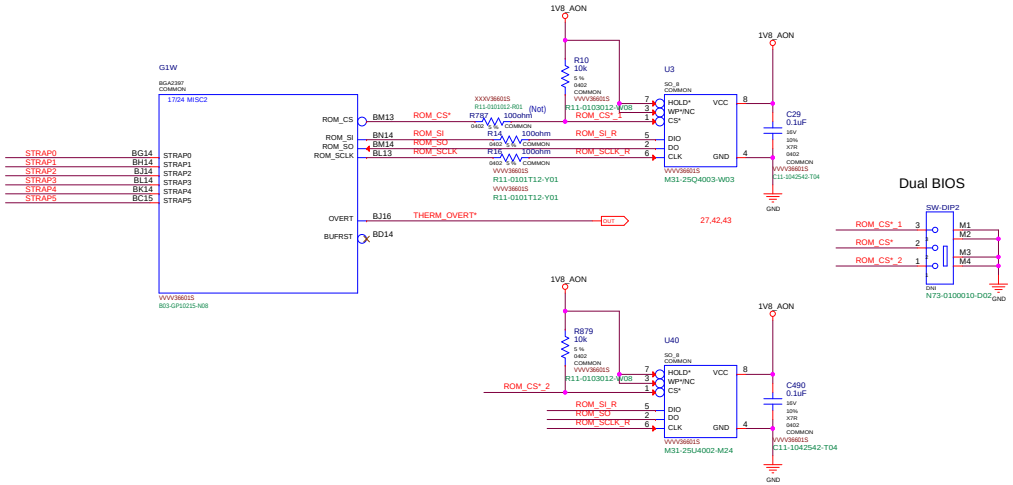
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

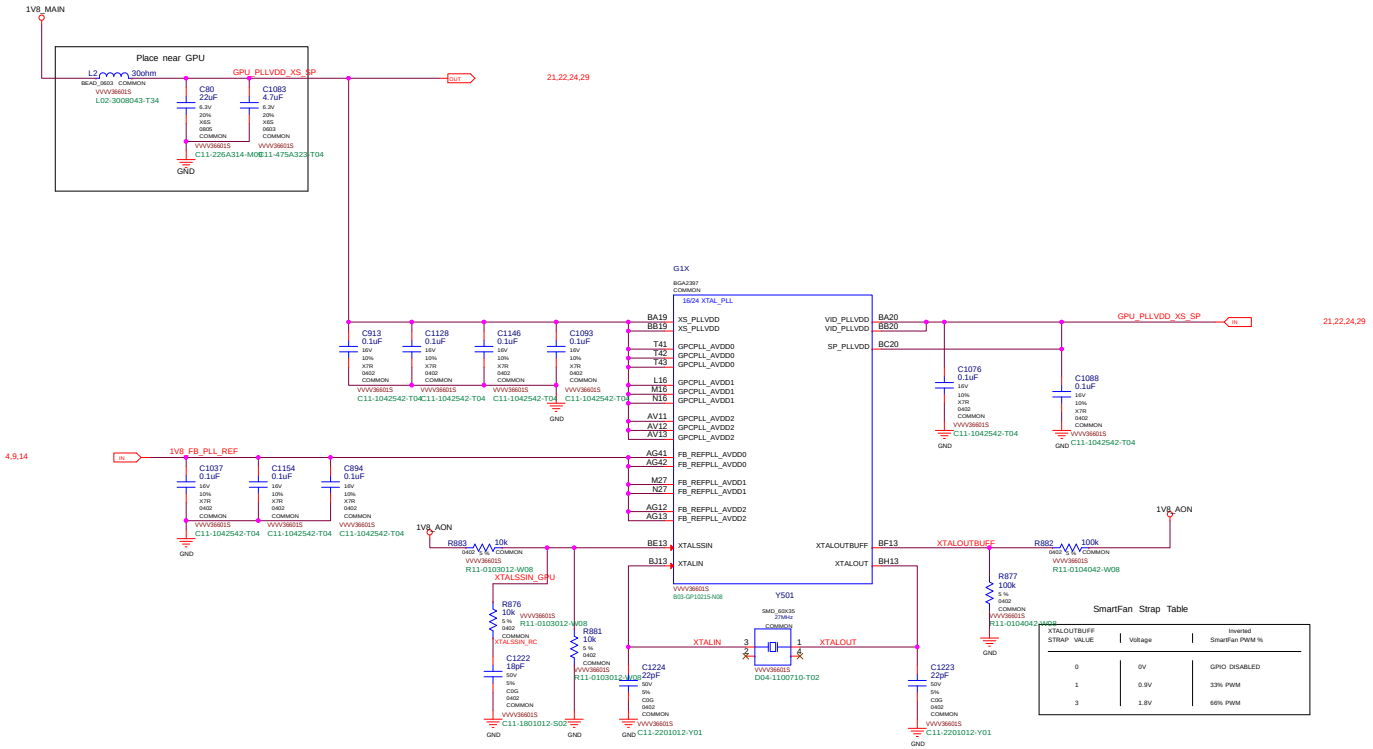
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE





MICRO-STAR INT'L CO.,LTD	
MS-V360	
Size: Custom	Document Description: MISC2: ROM, Straps
Rev: 1.0	
Date: Friday, March 31, 2017	Sheet 28 of 50



MICRO-STAR INT'L CO.,LTD		
MS-V360		
Size: Custom	Document Description: MISC2: XTAL. PLL	Rev: 1.0
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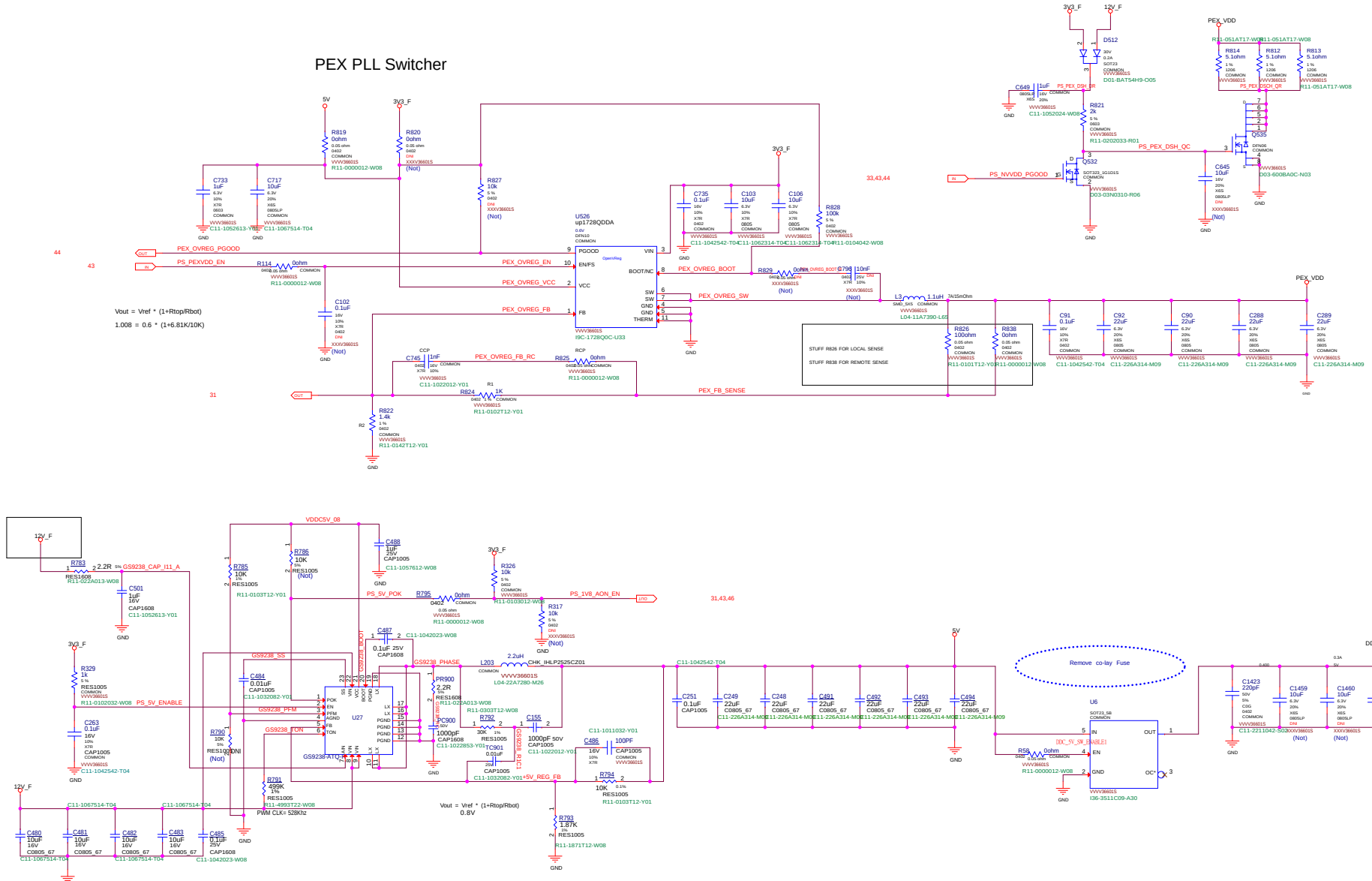
PEX PLL Switcher



MICRO-STAR INT'L CO.,LTD			
MS-V360			
Size: Custom	Document Description: PS: 5V, PEX_VDD		Rev: 1.0
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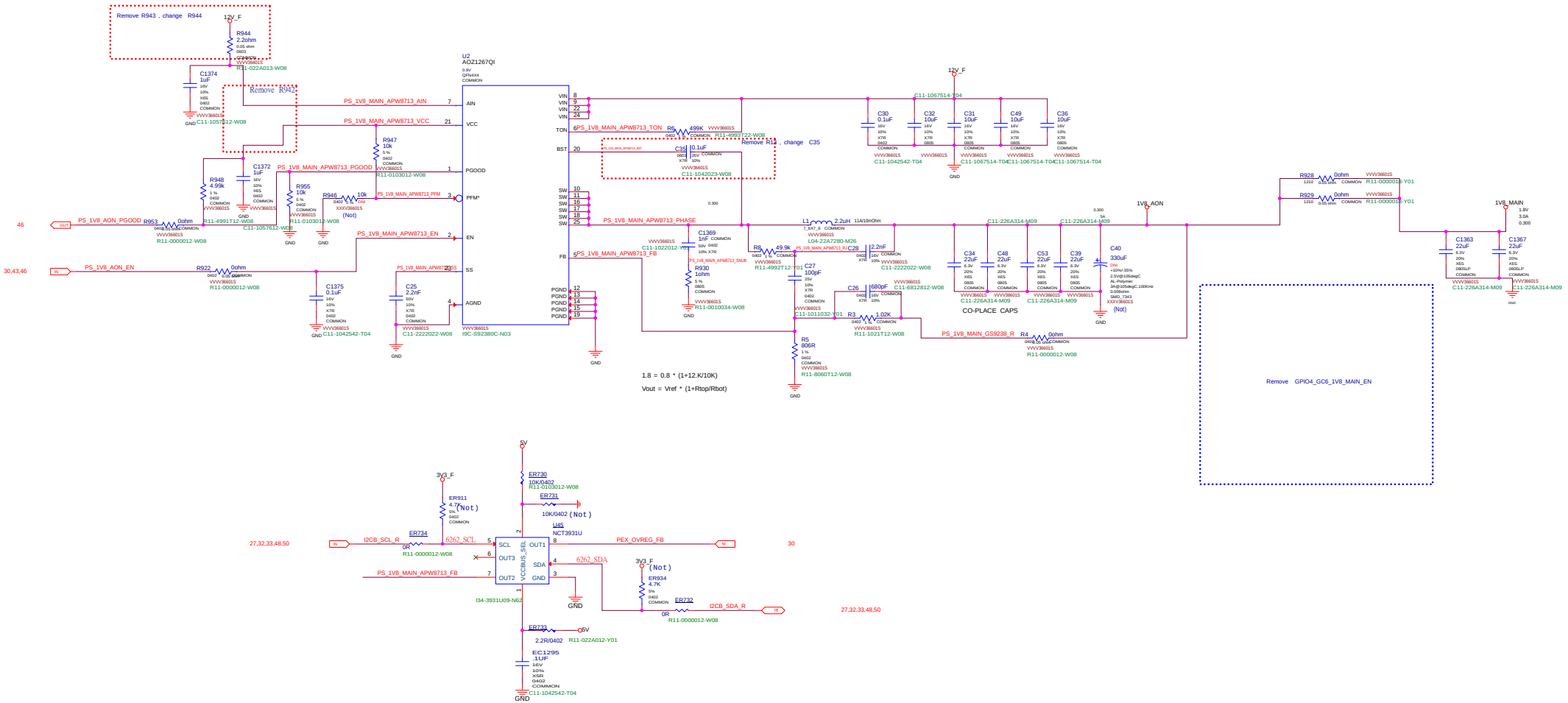
Page31: PS: 1V8 Rails



MICRO-STAR INT'L CO.,LTD	
MS-V360	
Size: Custom	Document Description: PS: 1V8 Rails
Rev: 1.0	
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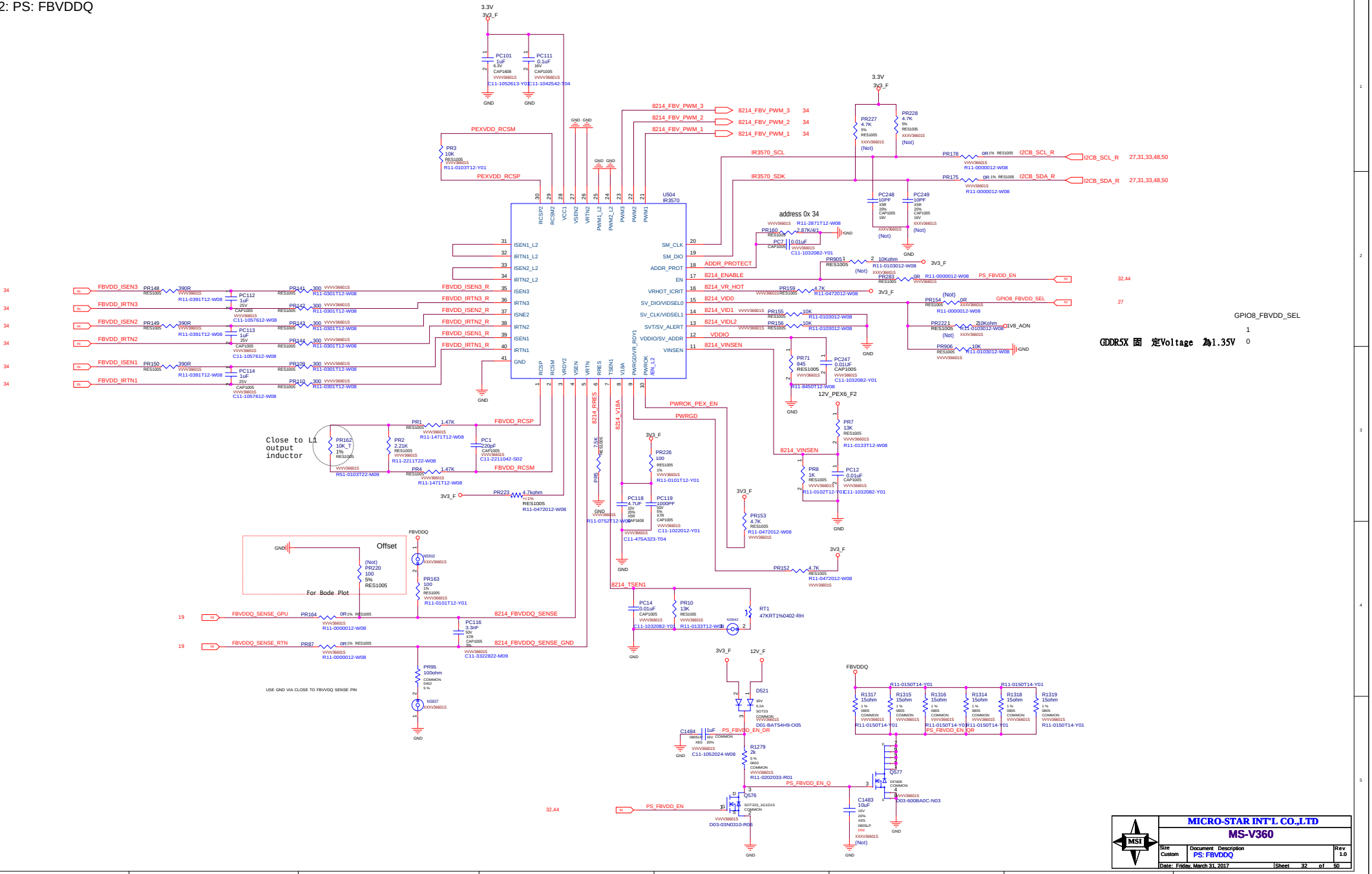
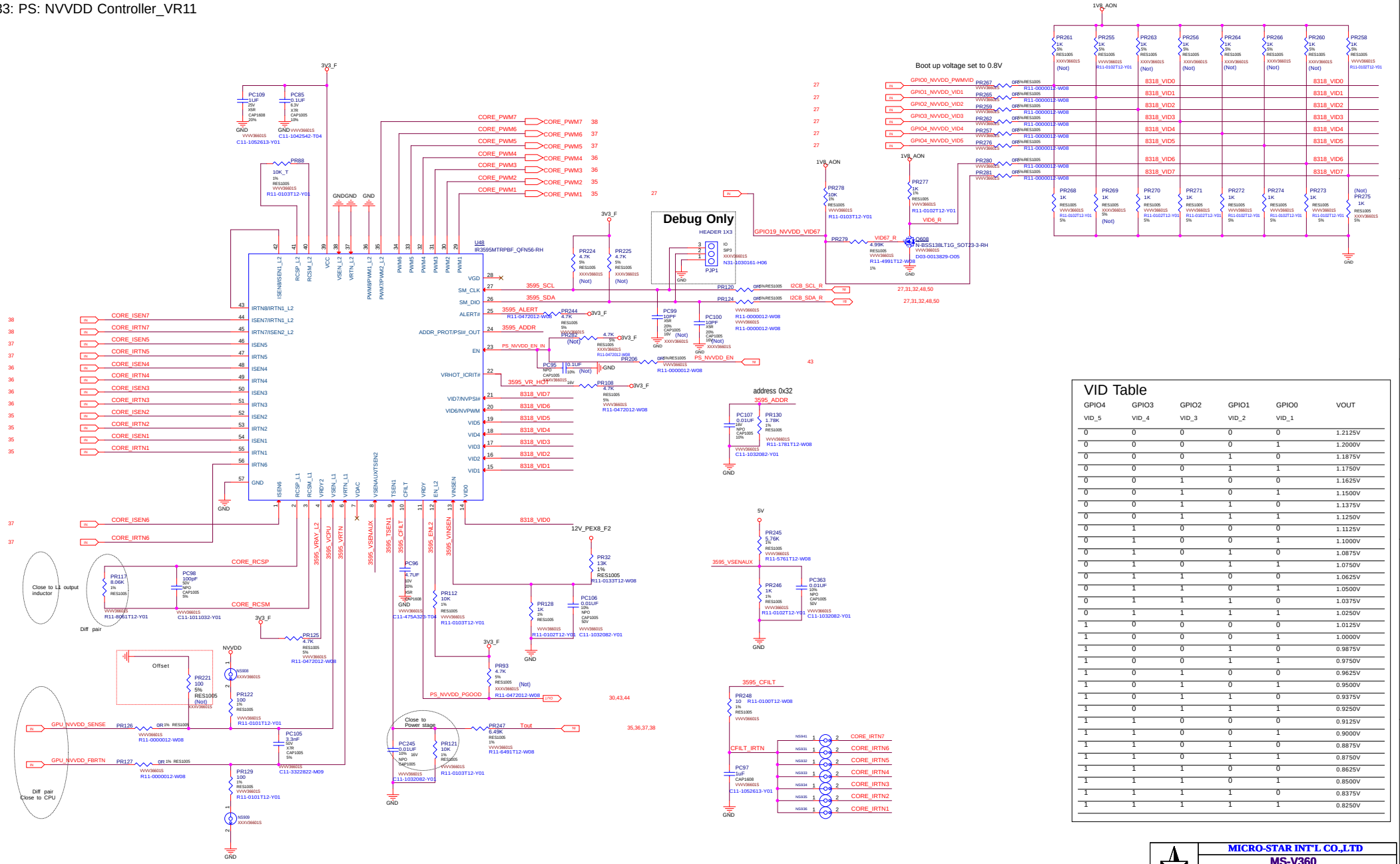
Page32: PS: FBVDDQ



Page33: PS: NVVDD Controller_VR11



VID Table

GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	VOUT
VID_5	VID_4	VID_3	VID_2	VID_1	
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	0	1	0	0.8875V
1	1	0	1	1	0.8750V
1	1	1	0	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V

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Size: Custom	Document Description: PS: NVVDD Controller_OVR8	Rev: 1.0
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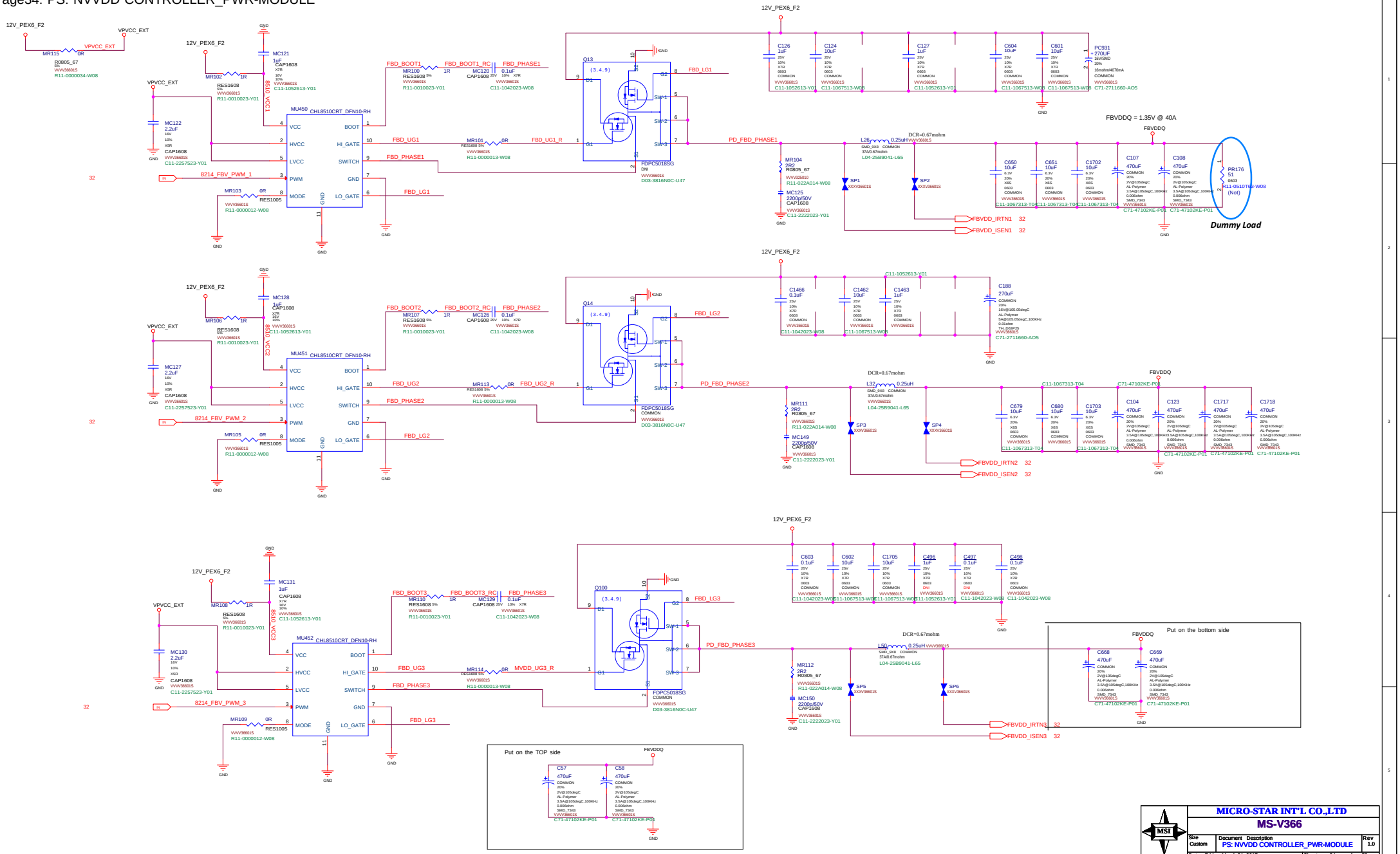
Page34: PS: NVVDD CONTROLLER_PWR-MODULE



MICRO-STAR INT'L CO.,LTD	
MS-V366	
Size: Custom	Document Description: PS: NVVDD CONTROLLER_PWR-MODULE
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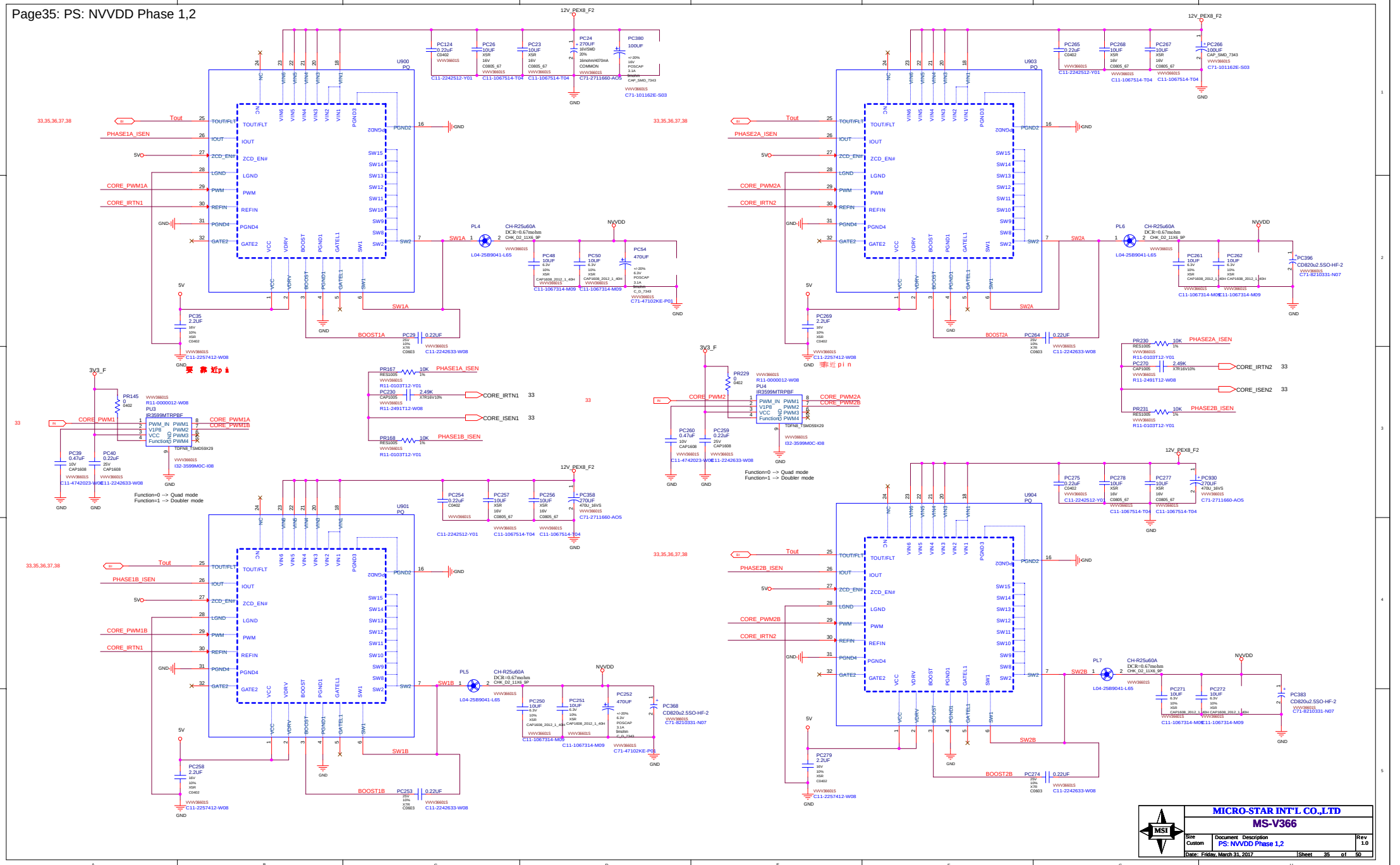
Page35: PS: NVVDD Phase 1,2
U900
U901
U903
U904
12V_PEX8_F2
NVVDD
3V3_F
33,35,36,37,38
Tout
PHASE1A_ISEN
PHASE1B_ISEN
PHASE2A_ISEN
PHASE2B_ISEN
CORE_PWM1A
CORE_PWM1B
CORE_PWM2A
CORE_PWM2B
CORE_IRTN1
CORE_IRTN2
SW1A
SW1B
SW2A
SW2B
BOOST1A
BOOST1B
BOOST2A
BOOST2B
CORE_ISEN1
CORE_ISEN2
Function=0 --> Quad mode
Function=1 --> Doubler mode
MICRO-STAR INT'L CO.,LTD
MS-V366
PS: NVVDD Phase 1,2
Rev 1.0
Date: Friday, March 31, 2017
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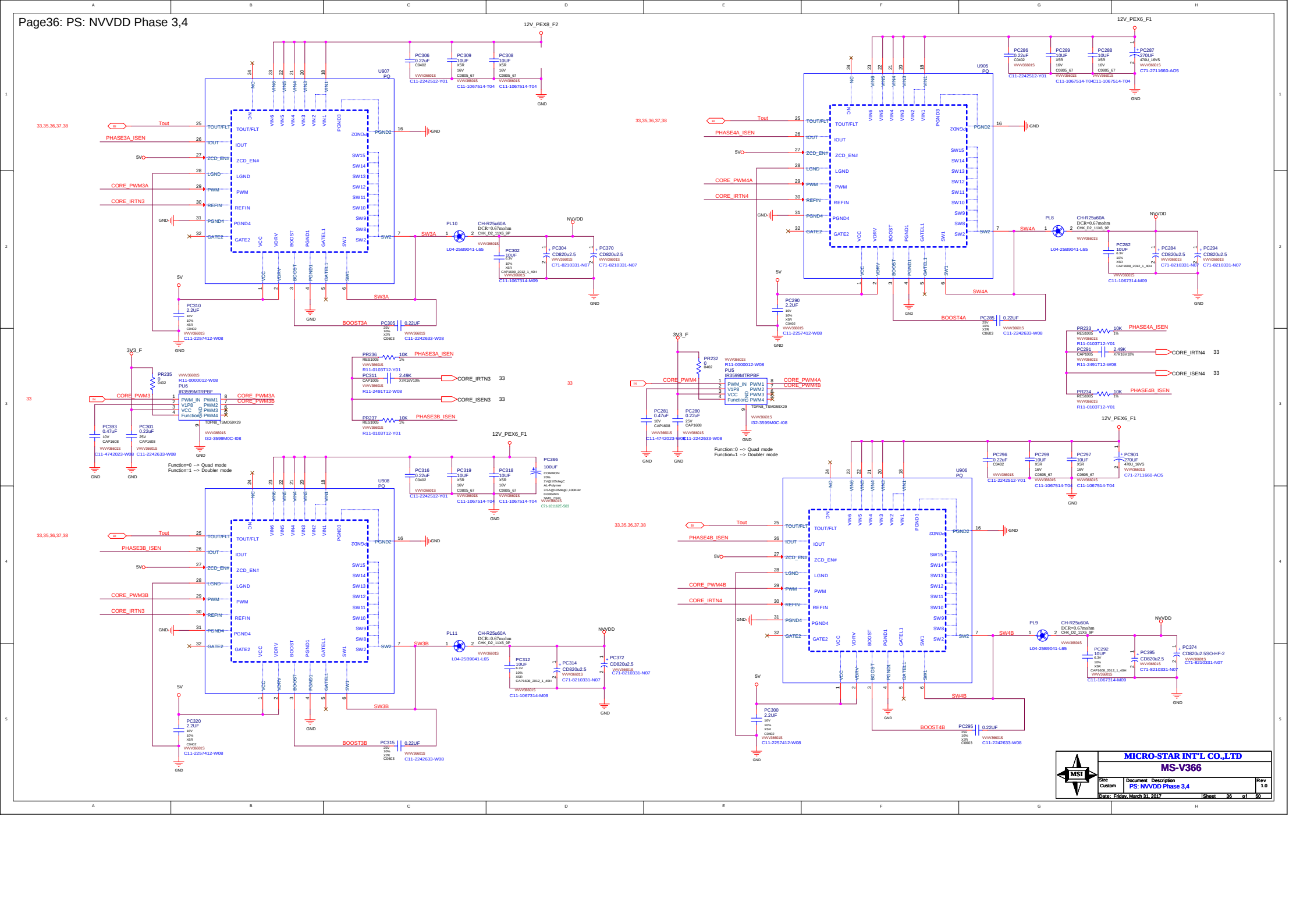
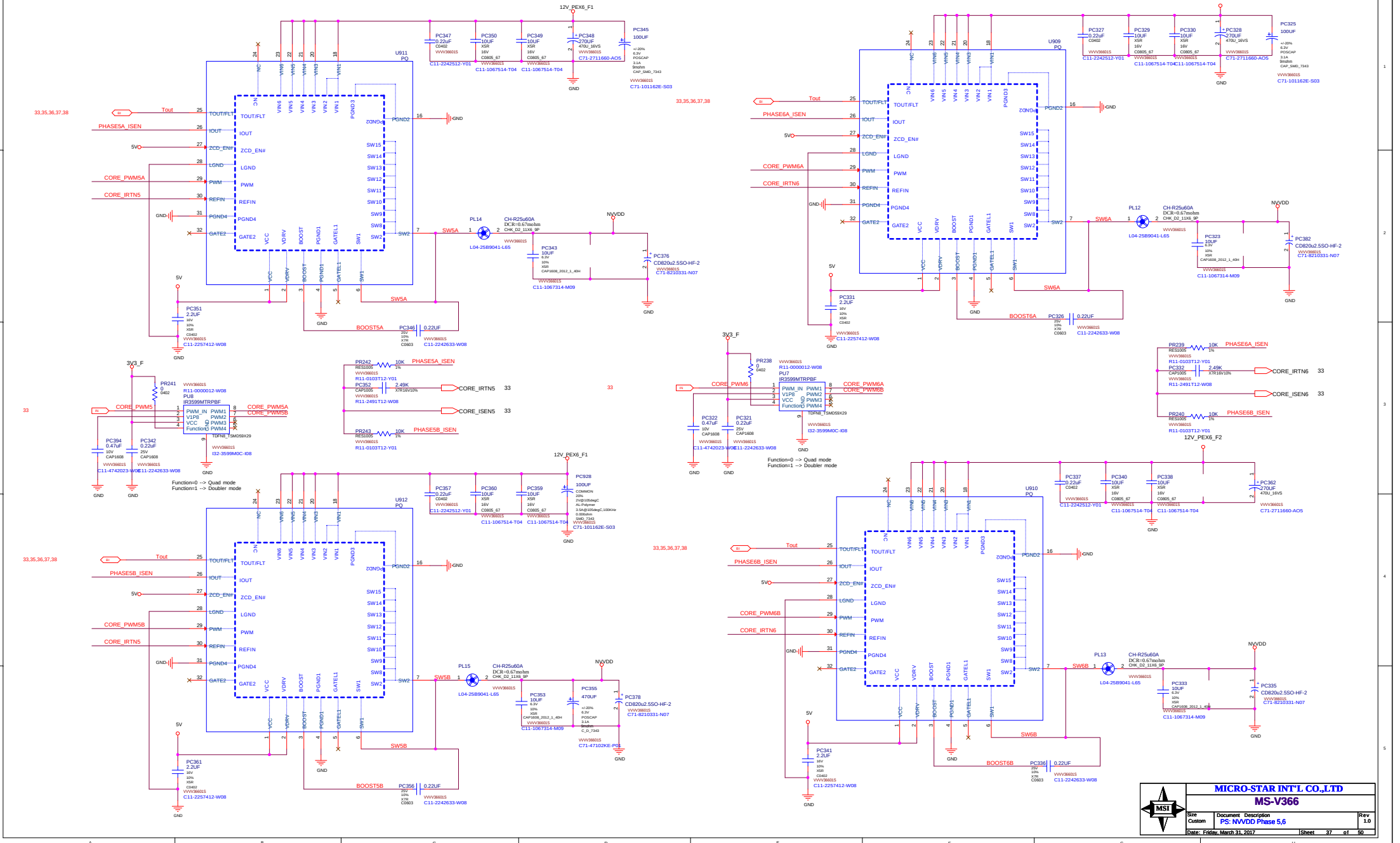
Page36: PS: NVVDD Phase 3,4



Page37: PS: NVVDD Phase 5,6

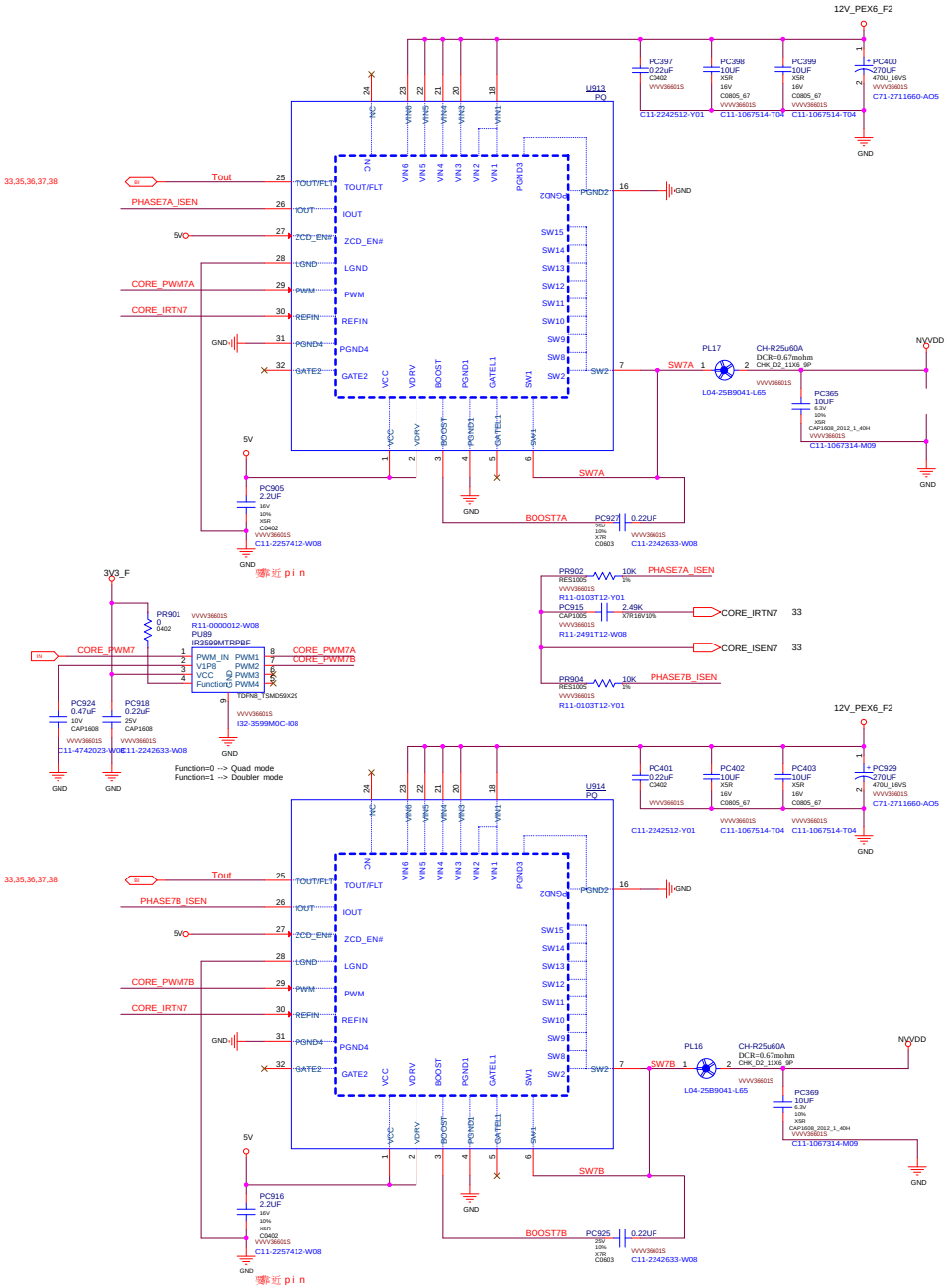


MICRO-STAR INT'L CO.,LTD

MS-V366

Size	Document Description	Rev
Custom	PS: NVVDD Phase 5,6	1.0

Date: Friday, March 31, 2017 Sheet 37 of 50



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V366	
Size: Custom	Document Description: PS:NVVDD Phase 6,7	Rev: 1.0
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Page39: PS: Dynamic Power Balance Phases

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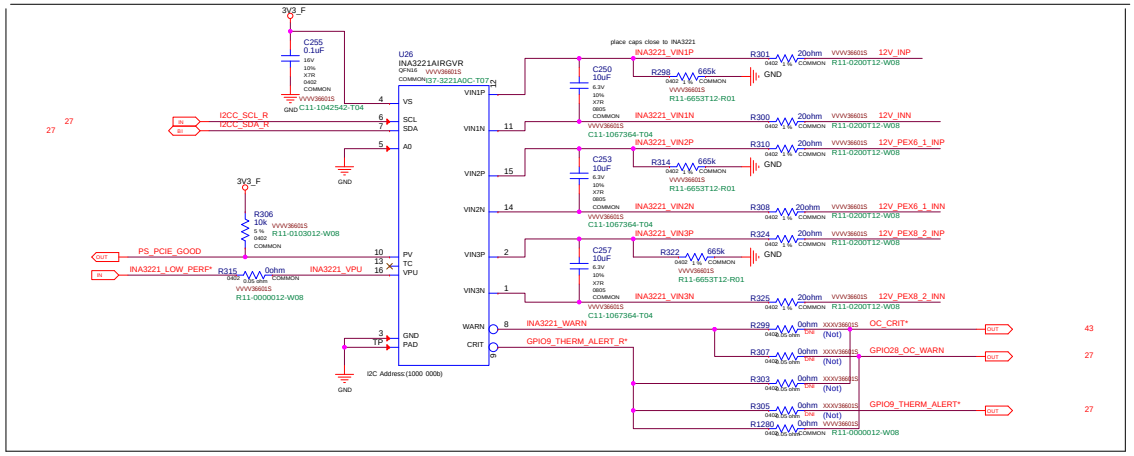
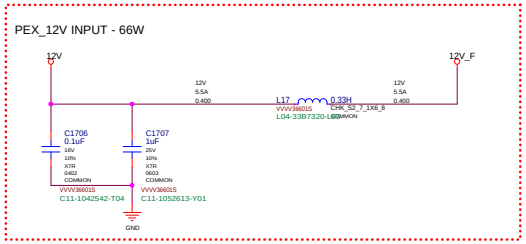
MS-V366	
Size: Custom	Document Description: Dynamic Power Balance Phases — Rev: 1.0
Date: Wednesday, March 29, 2017	Sheet 39 of 50

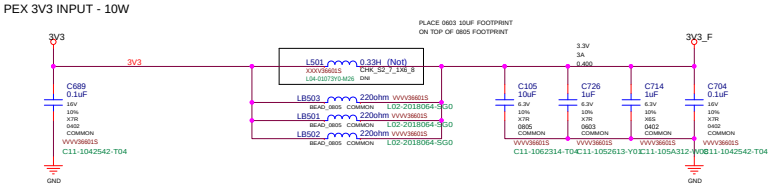
Page40: PS: Dynamic Power Balance Logic

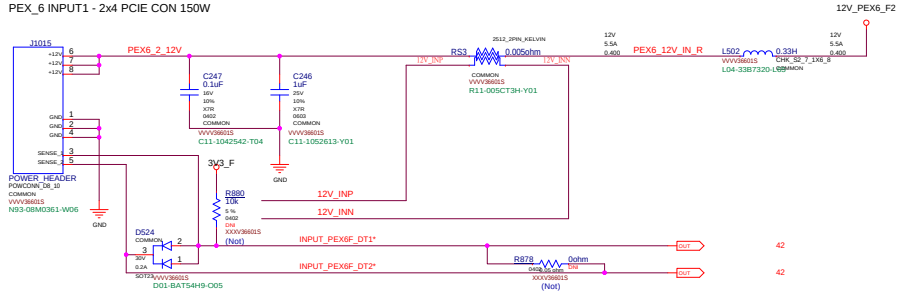
MICRO-STAR INT'L CO.,LTD	
MS-V366	
Size: Custom	Document Description: PS: Dynamic Power Balance Logic
Rev: 1.0	
Date: Wednesday, March 29, 2017	Sheet 40 of 50

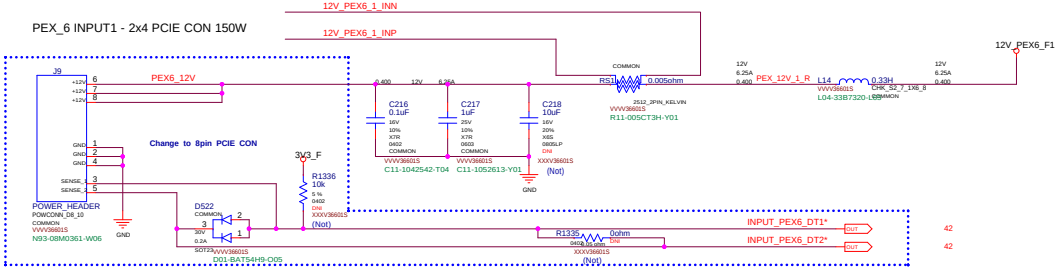
Page41: PS: Inputs, Filtering, and Monitoring

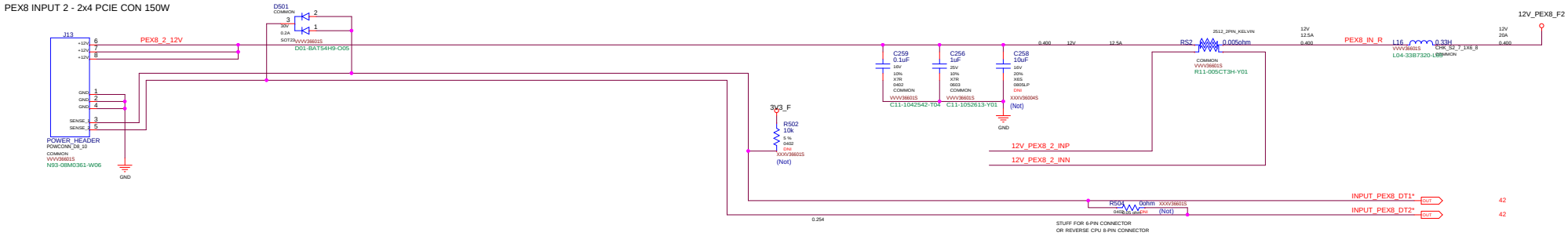












MICRO-STAR INT'L CO.,LTD	
MS-V366	
Size: Custom	Document Description: PS: Inputs, Filtering, and Monitoring
Rev: 1.0	
Date: Friday, March 31, 2017	Sheet 41 of 50

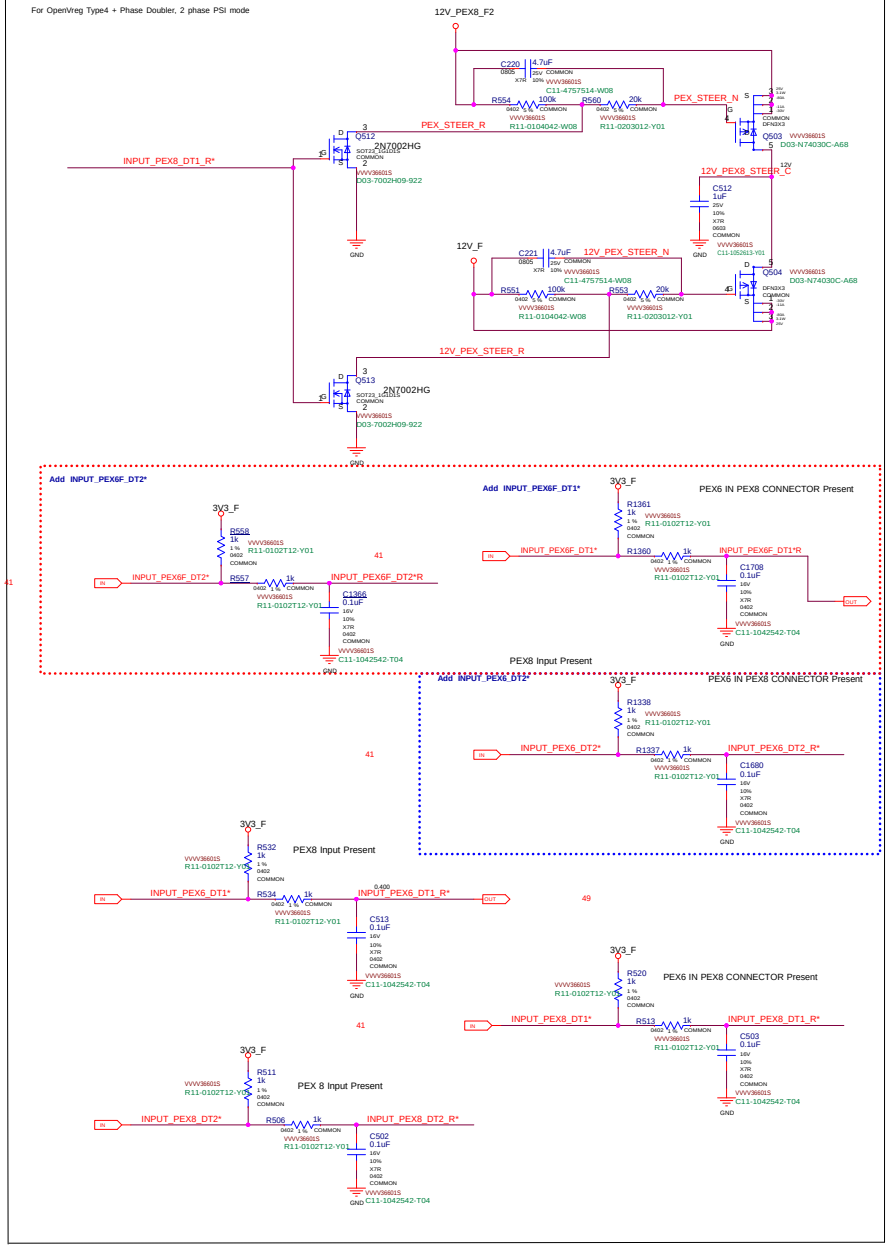
Page42: PS: 12V Current Steering & Hot Unplug Detect

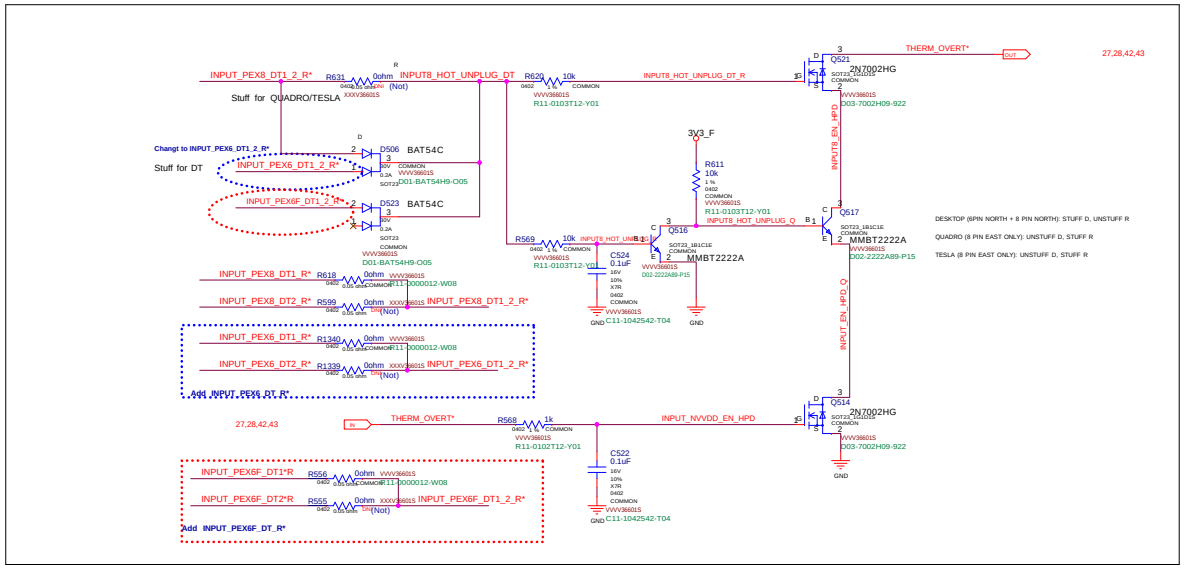
QUADRO/TESLA:

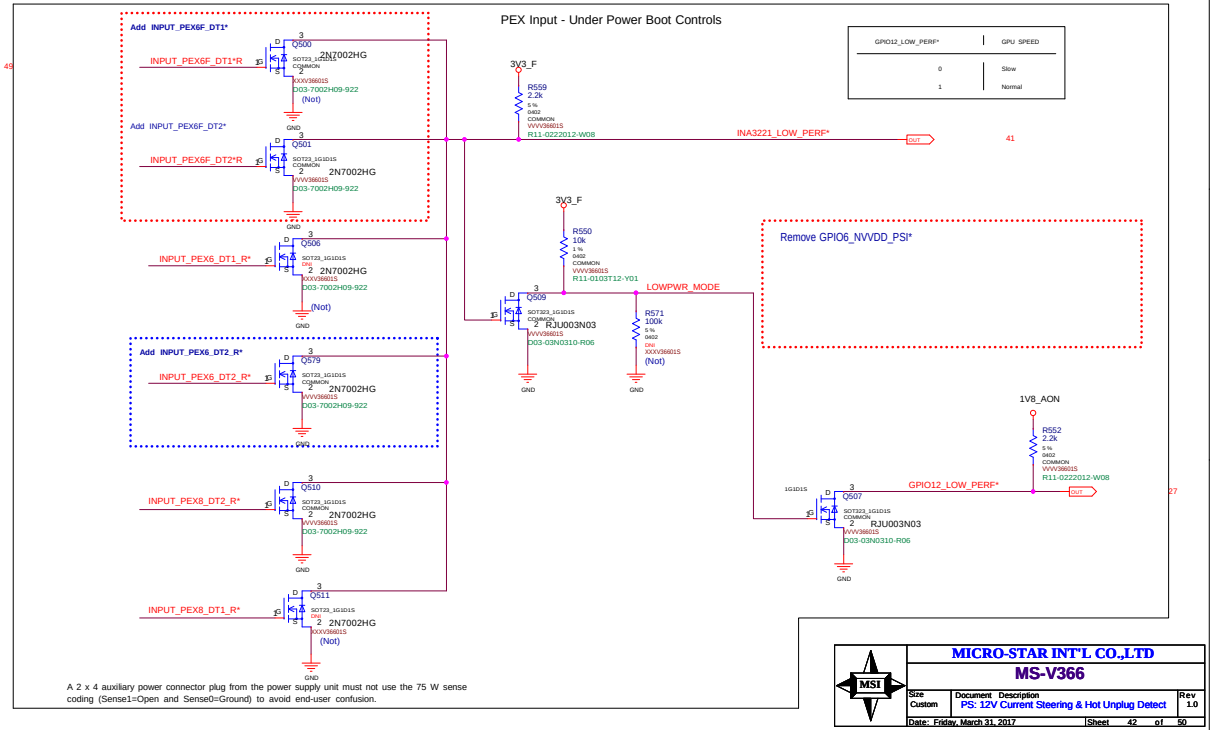
12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

For OpenVreg Type4 + Phase Doubler, 2 phase PSI mode

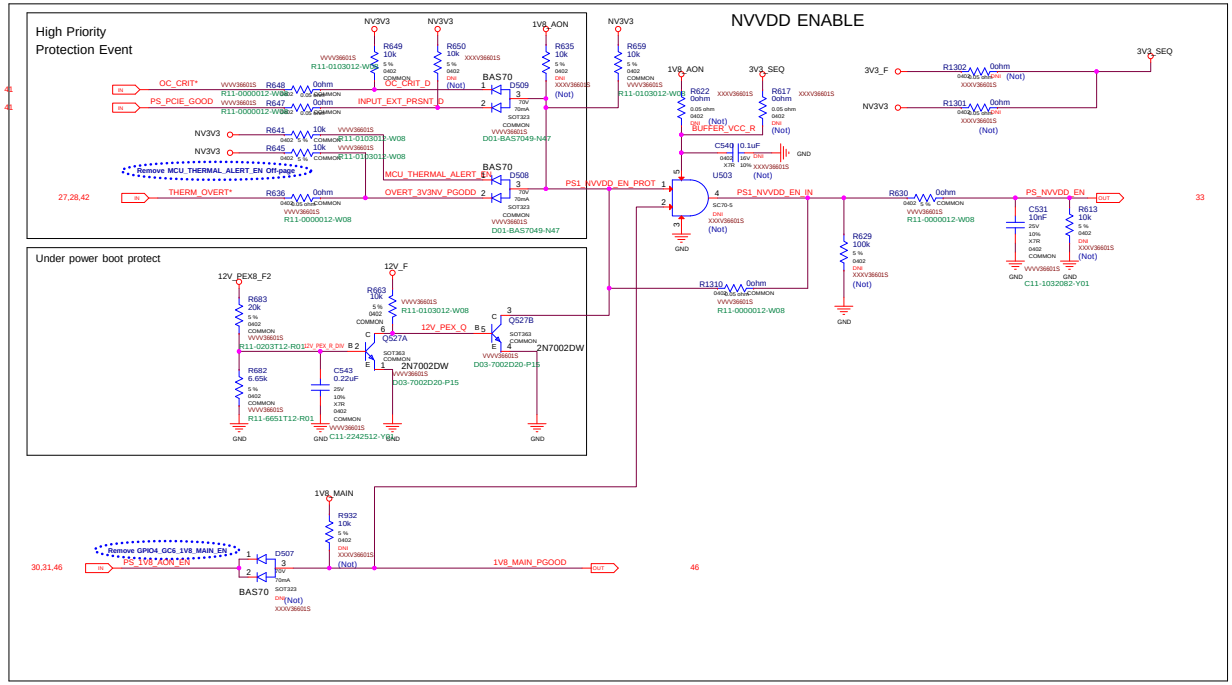


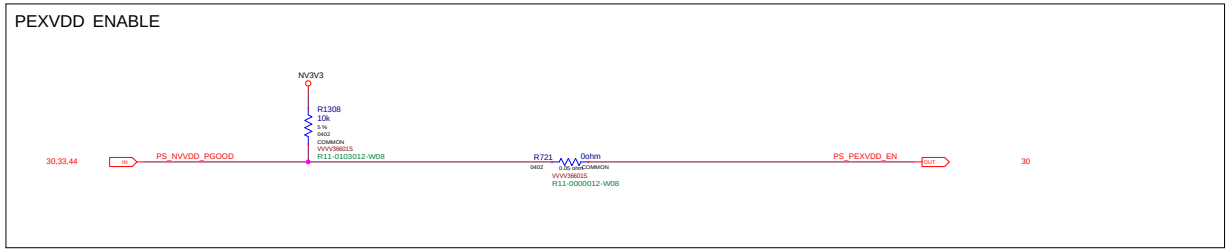




MICRO-STAR INT'L CO.,LTD	
MS-V366	
Size: Custom	Document Description: PS: 12V Current Steering & Hot Unplug Detect
Rev: 1.0	
Date: Friday, March 31, 2017	Sheet 42 of 50

Page43: PS: NVVDD ENABLE





MICRO-STAR INT'L CO.,LTD	
MS-V366	
Size: Custom	Document Description: PS: NVVDD ENABLE
Rev: 1.0	
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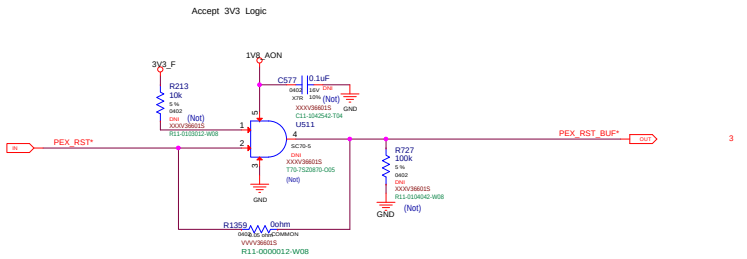
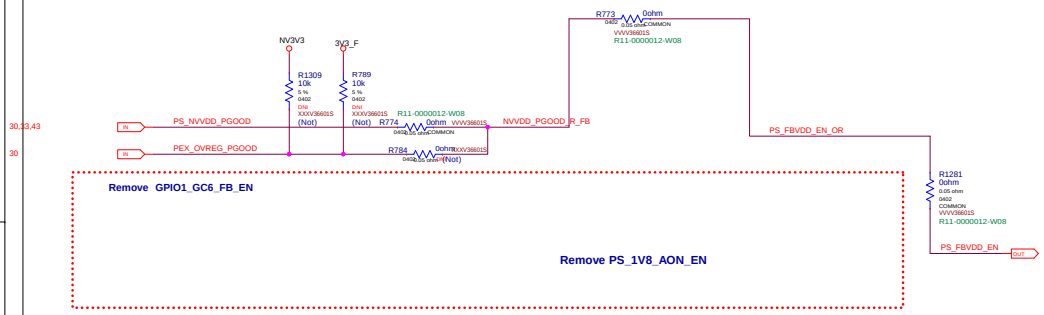
Remove PEX_CLKREQ*

Remove GPU_EVENT*

PEX_RST# LOGIC



FBVDD/Q ENABLE



MICRO-STAR INT'L CO.,LTD	
MS-V366	
Size: Custom	Document Description: GC6 MISC
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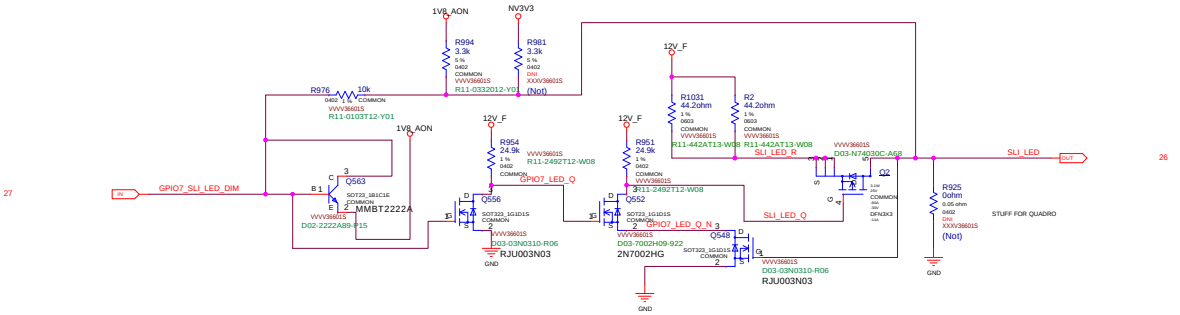
Page45:GEFORCE LED & SLI LED

Remove LED HEADER(GEFORCE ONLY)

SLI LED (GEFORCE ONLY)



MICRO-STAR INT'L CO.,LTD	
MS-V366	
Size: Custom	Document Description: GEFORCE LED & SLI LED
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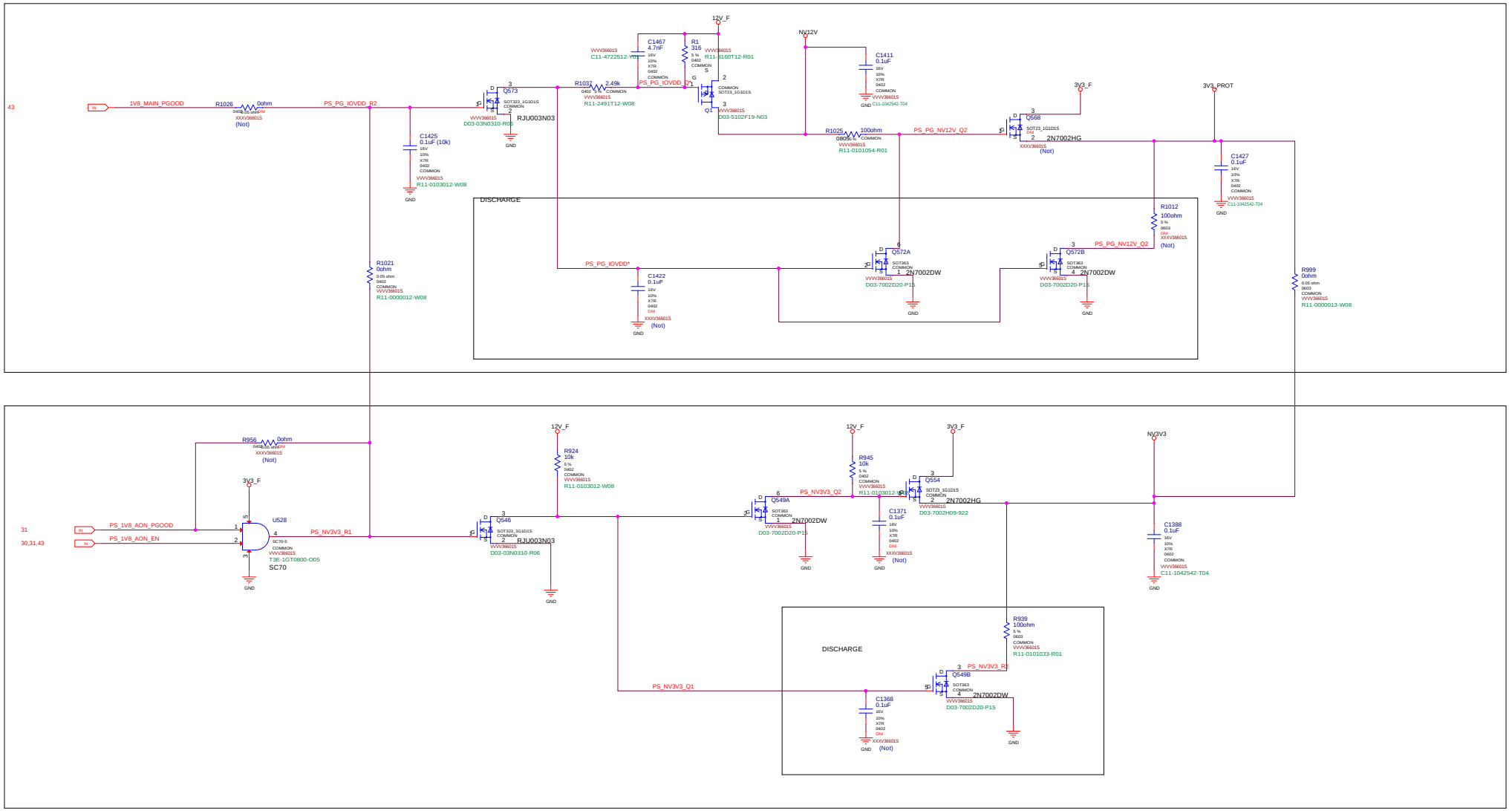

MICRO-STAR INT'L CO.,LTD	
MS-V366	
Size: Custom	Document Description: NV3V3, NV12V
Rev: 1.0	
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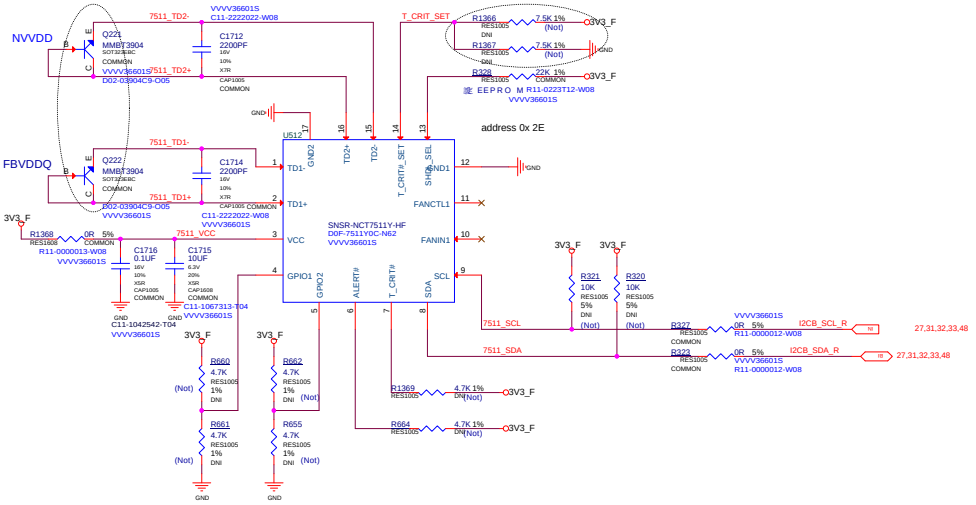
Thermal IC : NCT7511Y

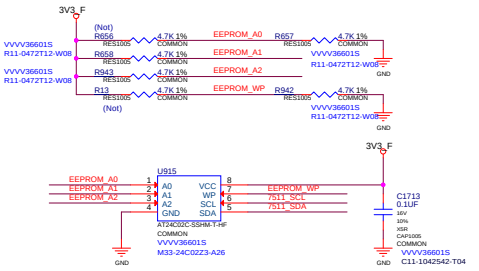
Layout notice :
*Add ground shielding for D+ and Dtraces.
*D+/D- route has to be away from the high noise area.
*The recommended traces width and ground shielding spacing are 10mils.

Please refer datasheet
TCRIT_SET Table
If floating,shutdown temp. set to 65℃

Thermal Diode



EEPROM



MICRO-STAR INT'L CO.,LTD		
MS-V366		
Size: Custom	Document Description: MCU	Rev: 1.0
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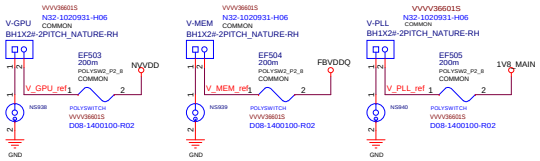
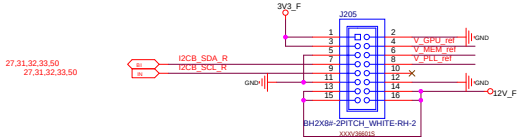
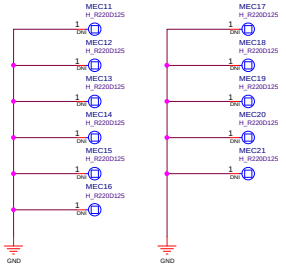
Page48: Mechanical: Bracket/Thermal Solution

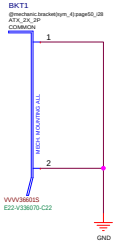




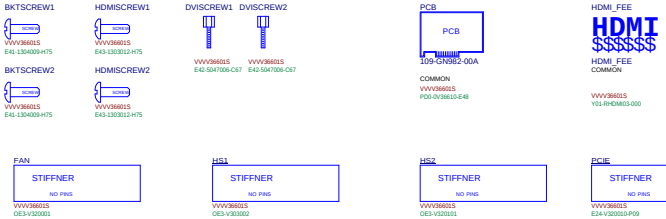
Mechanical Holes Symbol



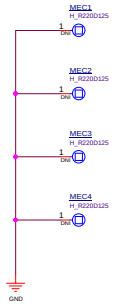
Brackets:

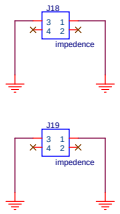


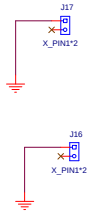
Screw

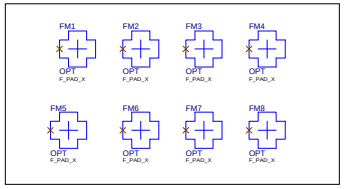


GPU HOLES SYMBOL









MICRO-STAR INT'L CO.,LTD			
MS-V366			
Size: Custom	Document Description: Mechanical: Bracket/Thermal Solution		Rev: 1.0
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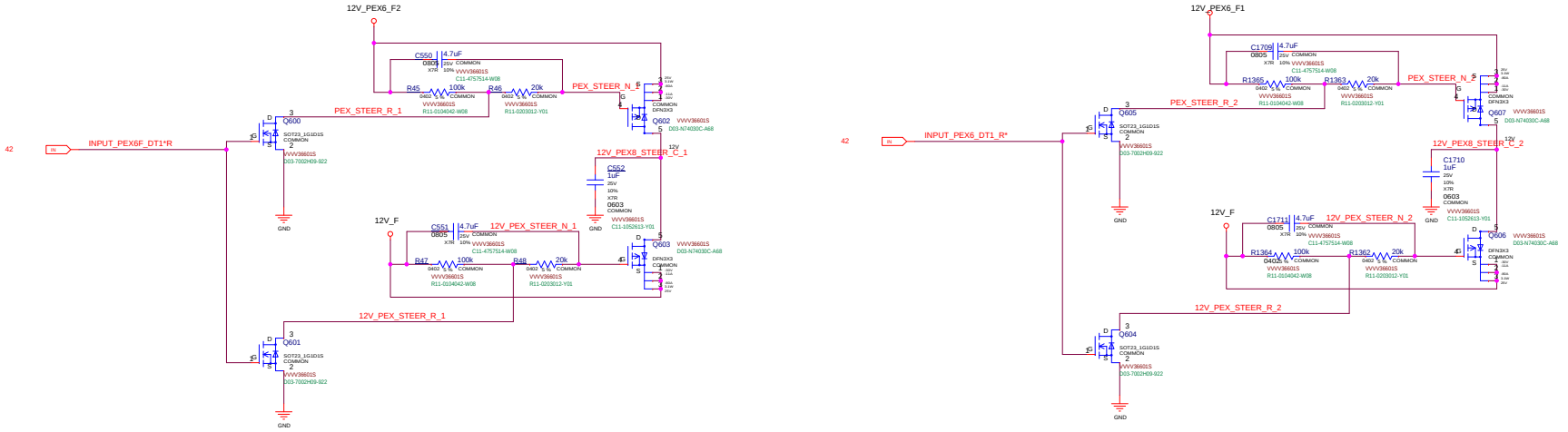
Page49: Current Steering 2



MSI	MICRO-STAR INT'L CO.,LTD	
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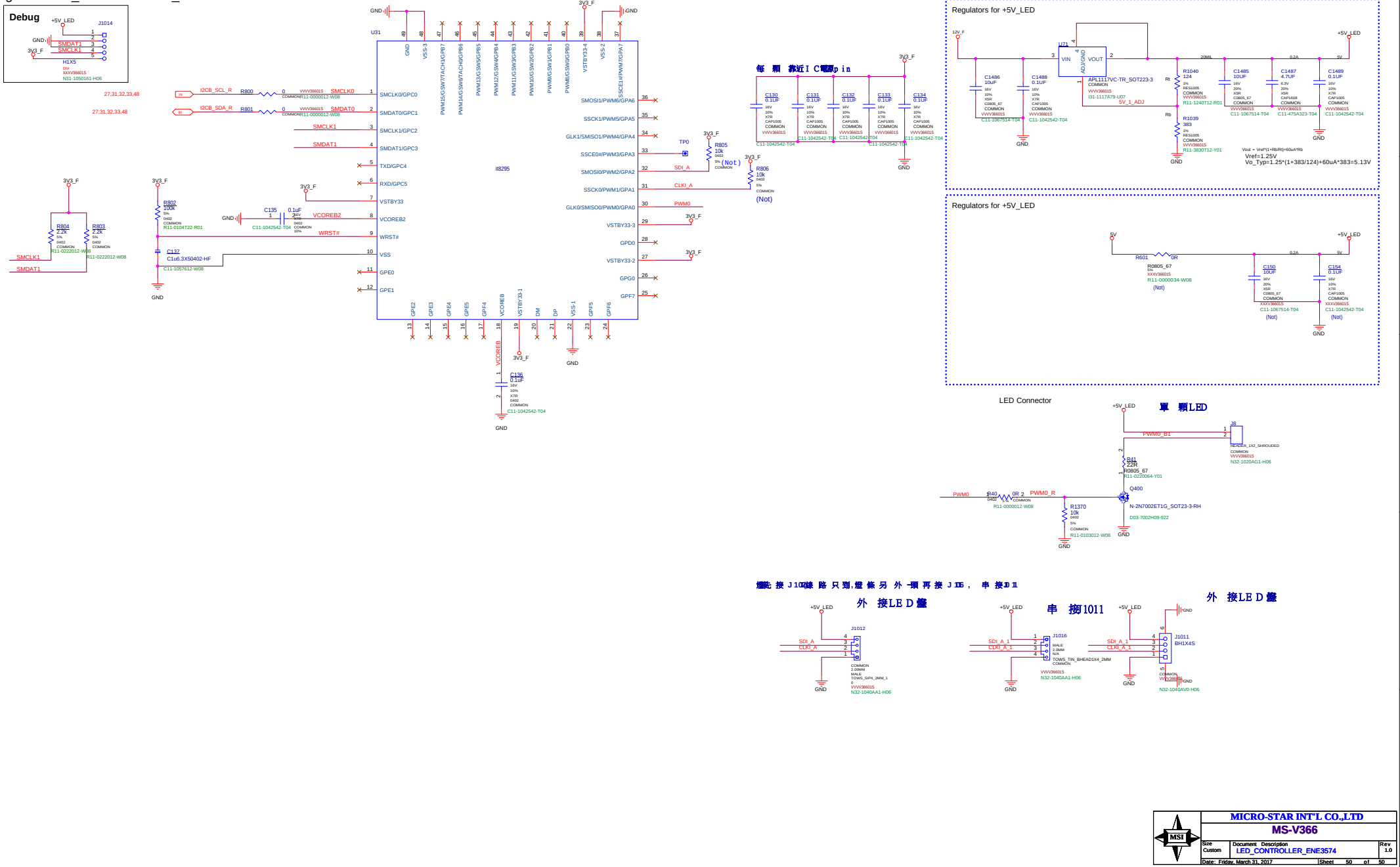

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