

PG413 A00

GP104 - 8GB GDDR5X, 256b, 256Mx32
Tall DVI-D + DP + DP + DP/HDMI + DP

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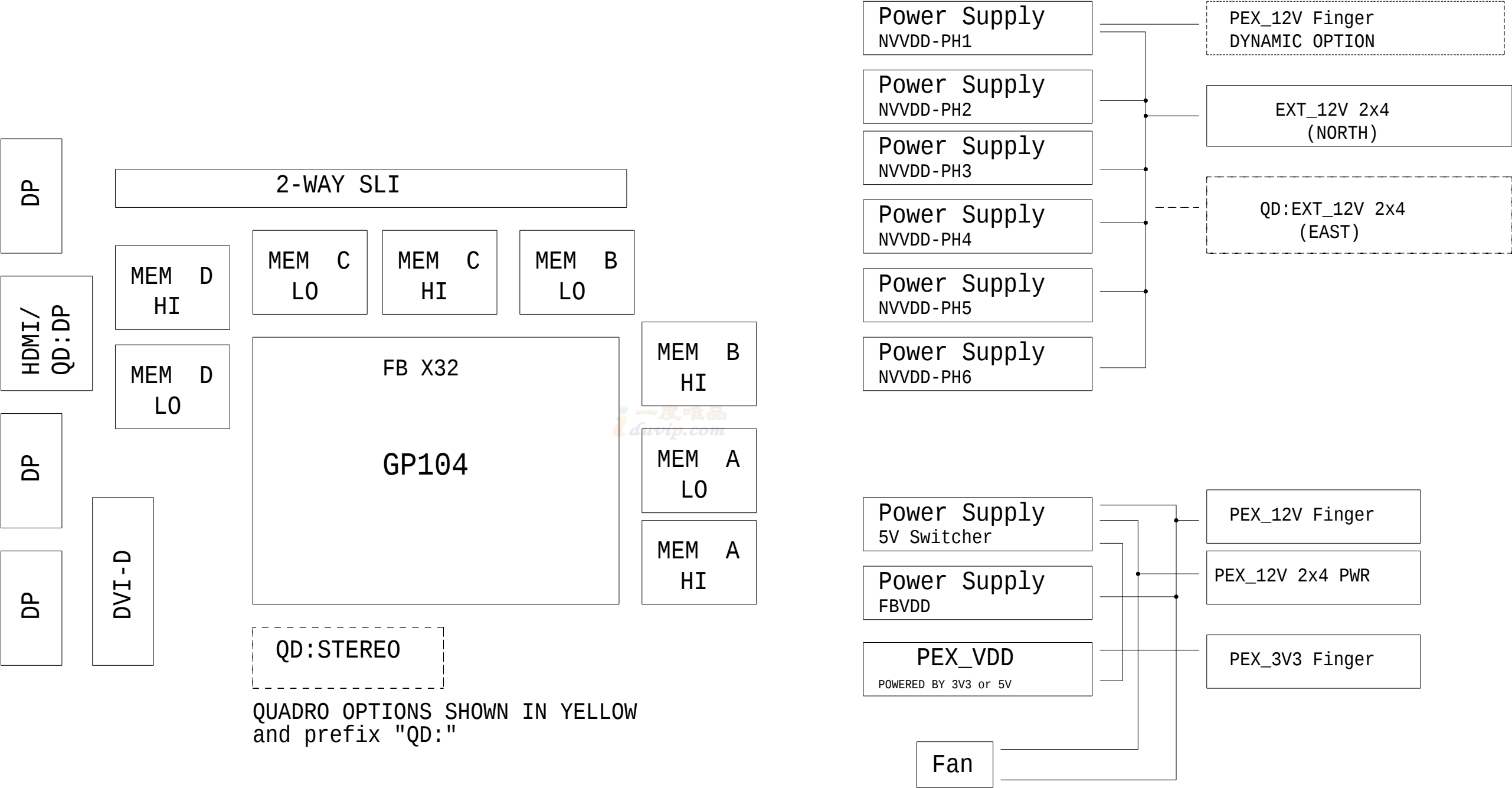
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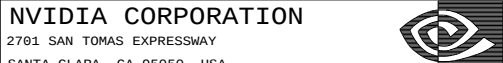
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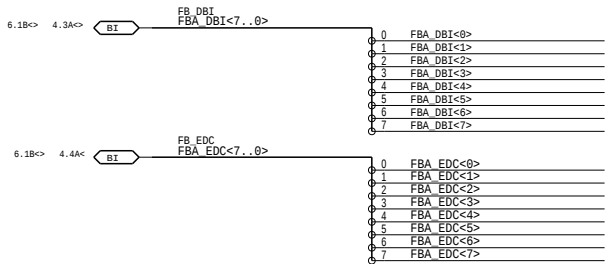
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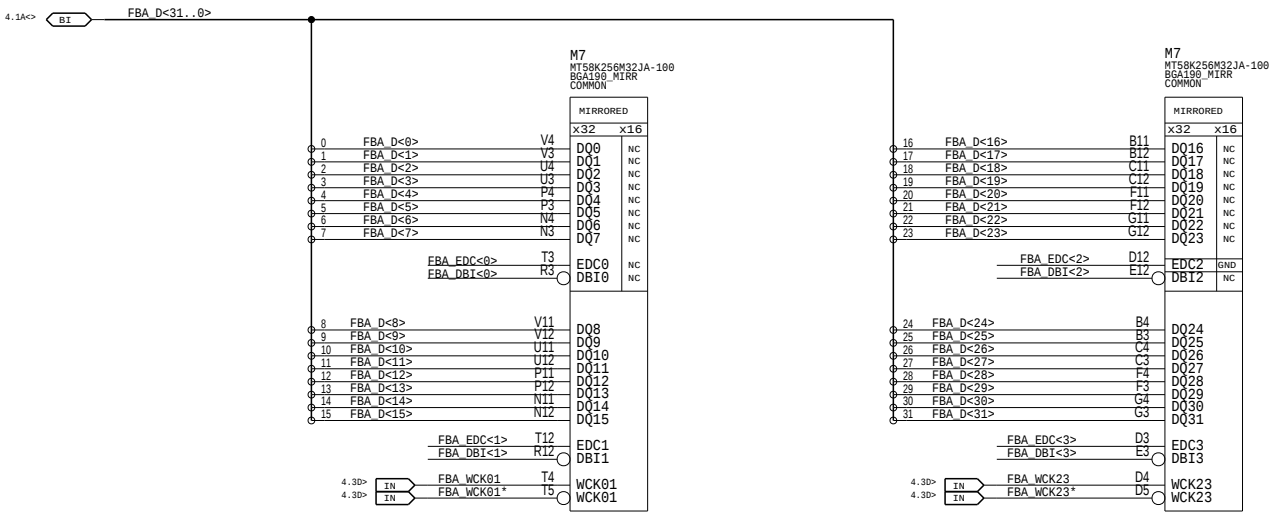


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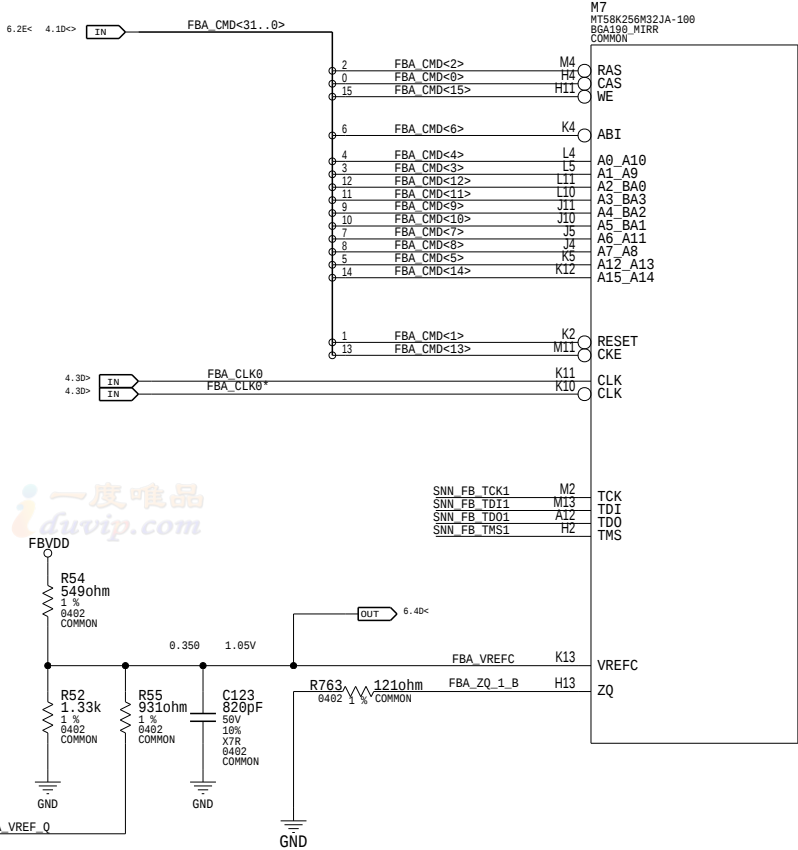
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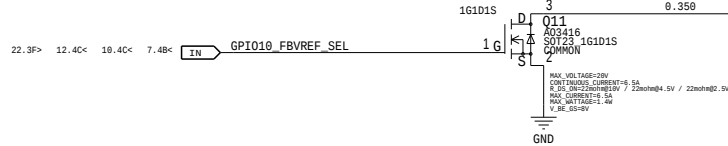
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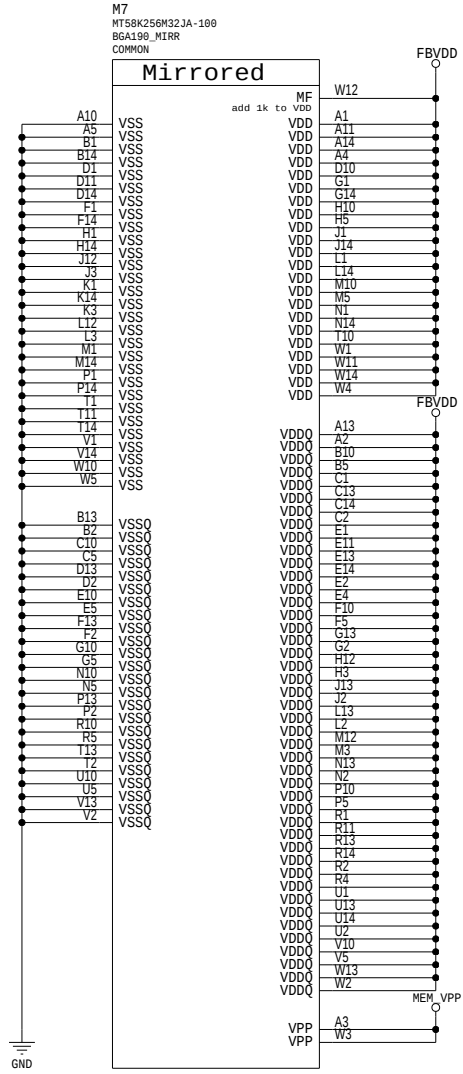
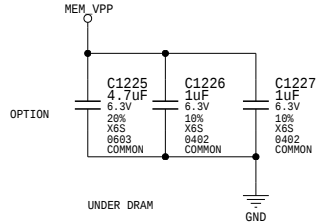
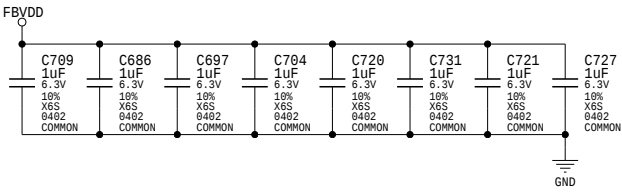
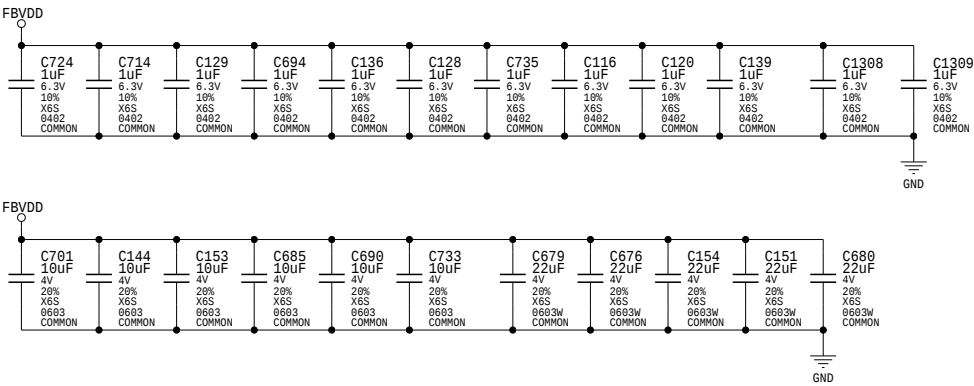
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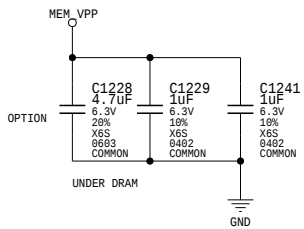
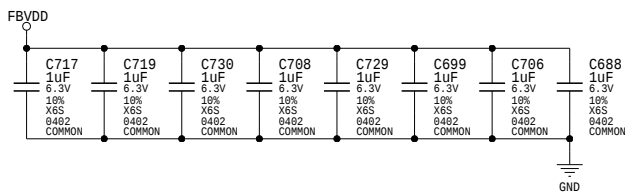
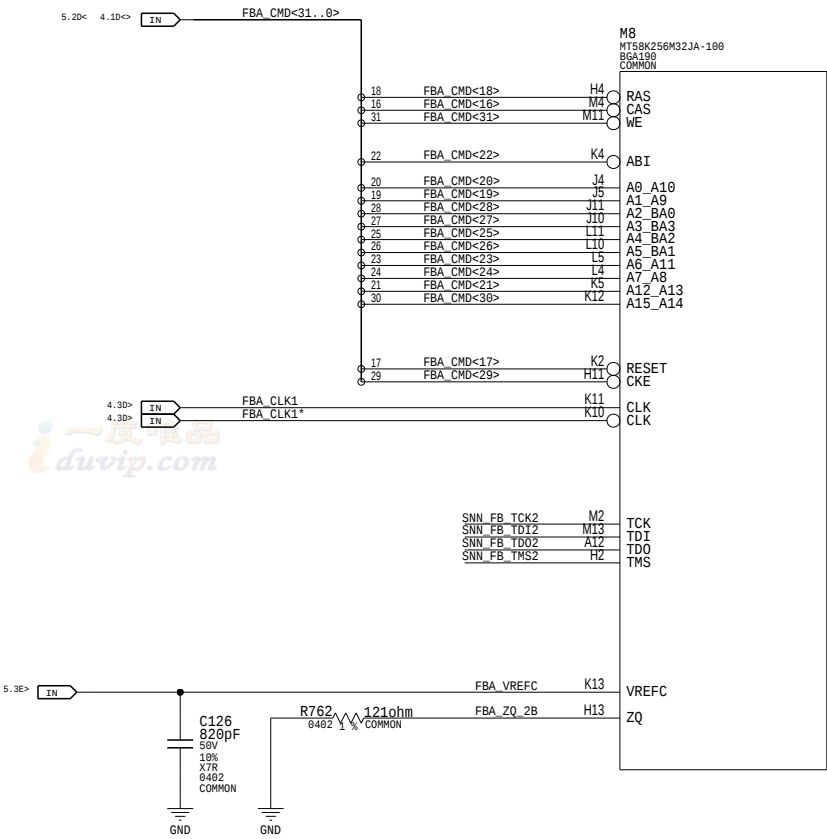
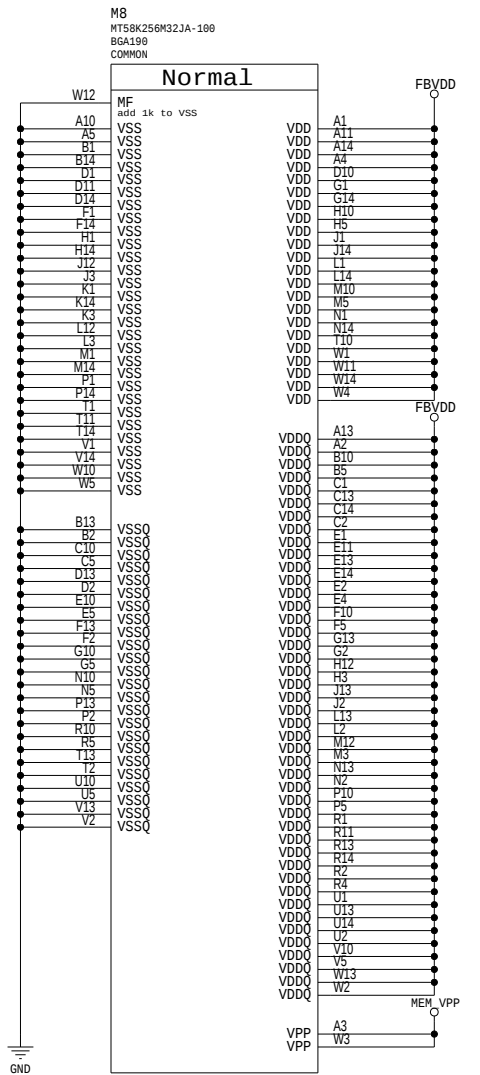
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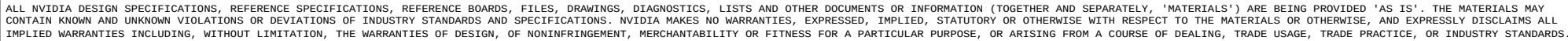
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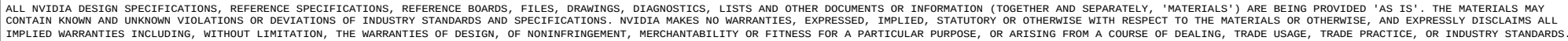
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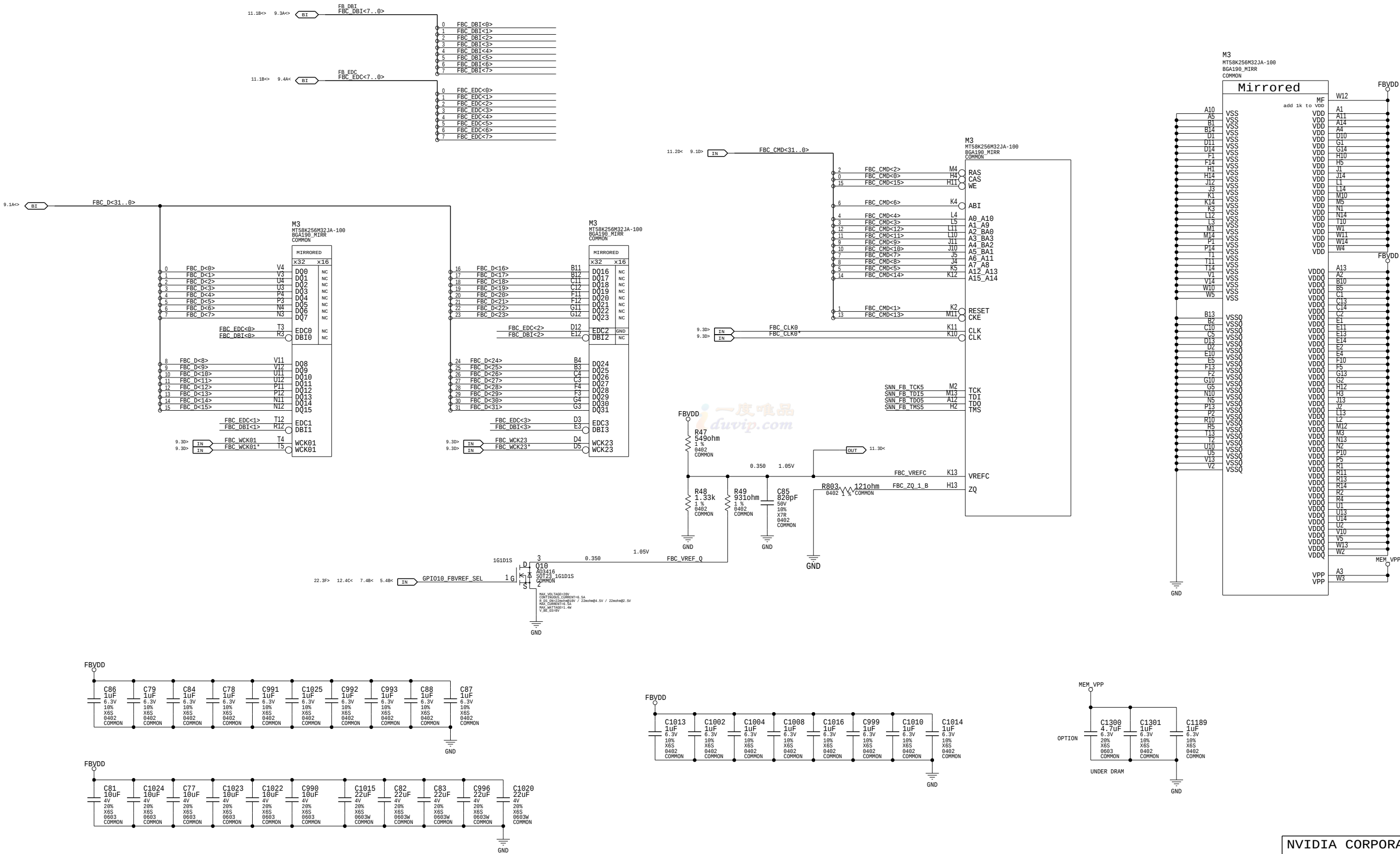
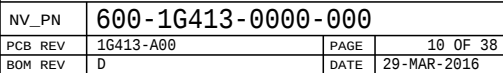


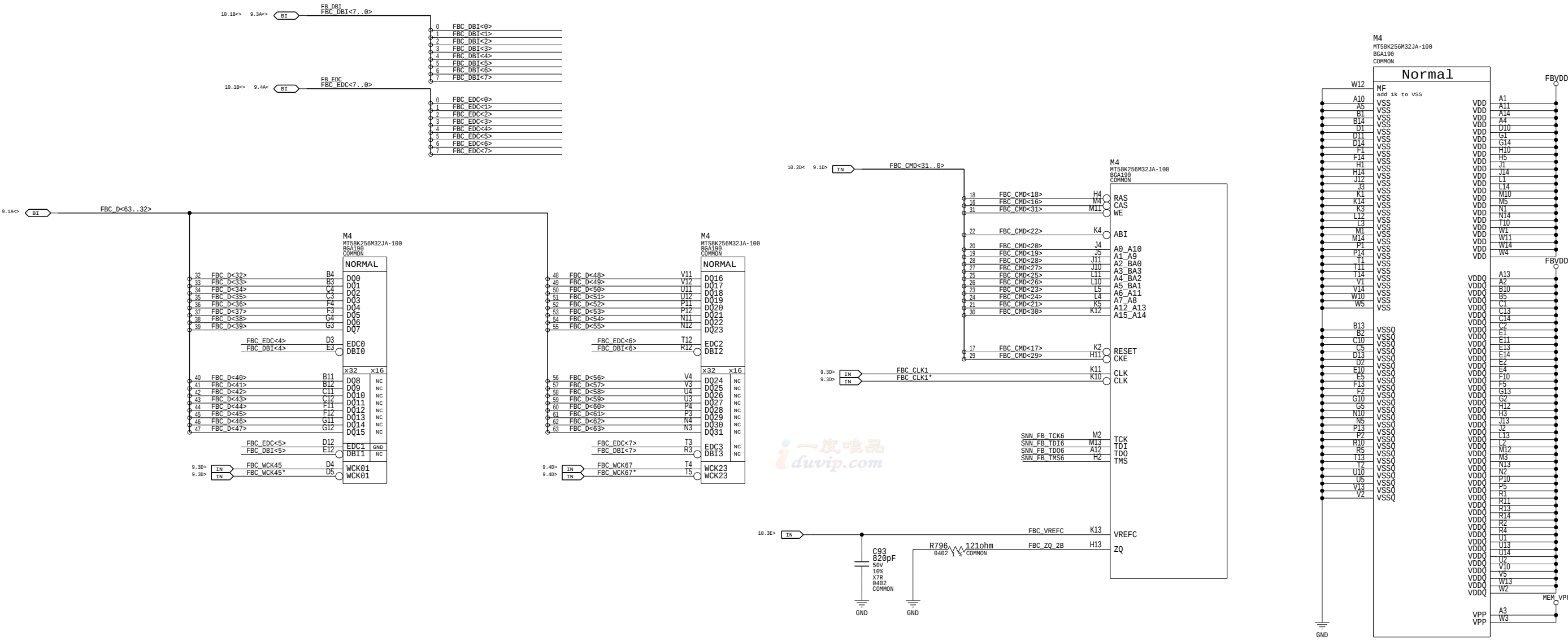


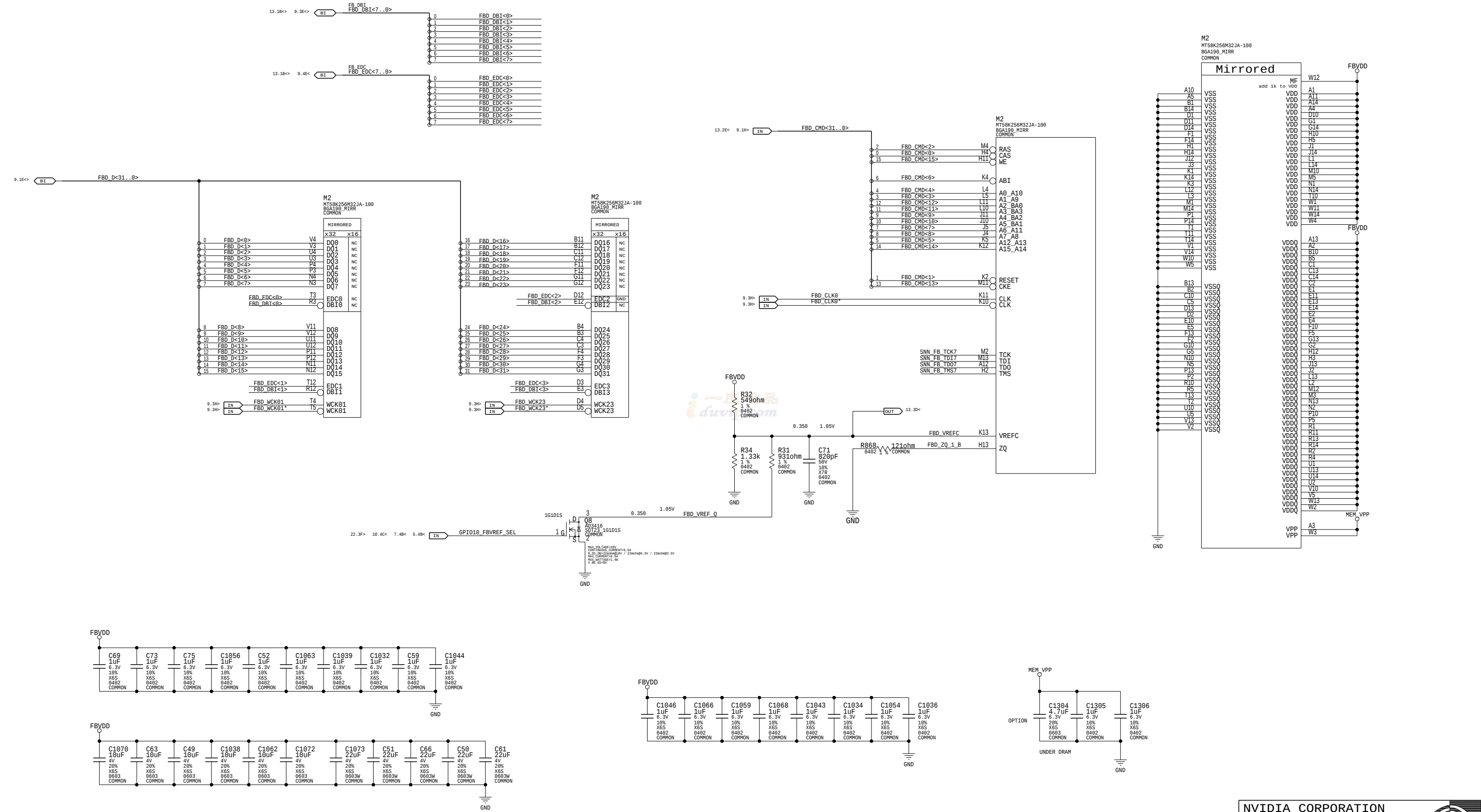
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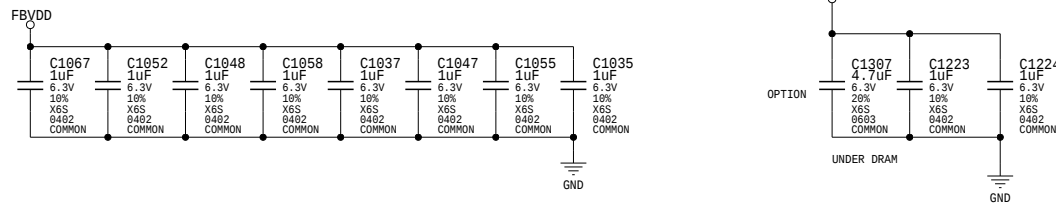
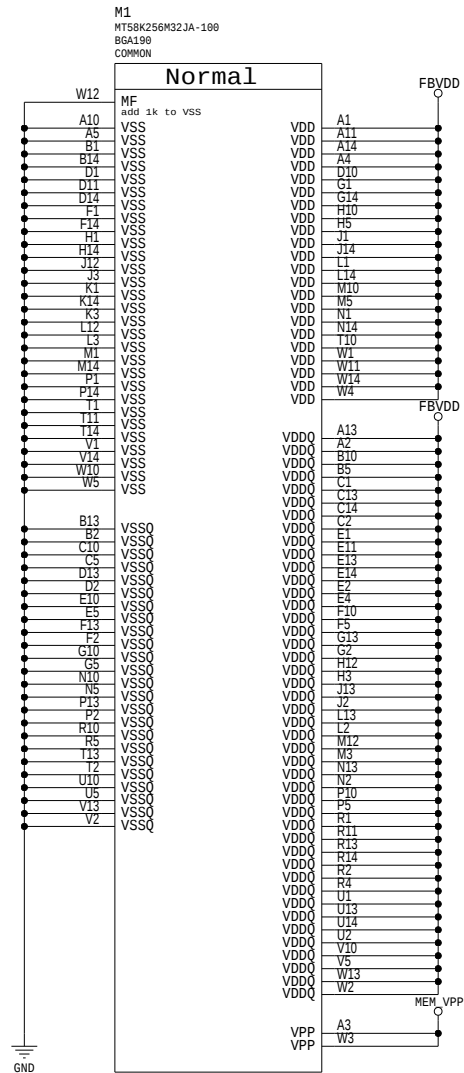












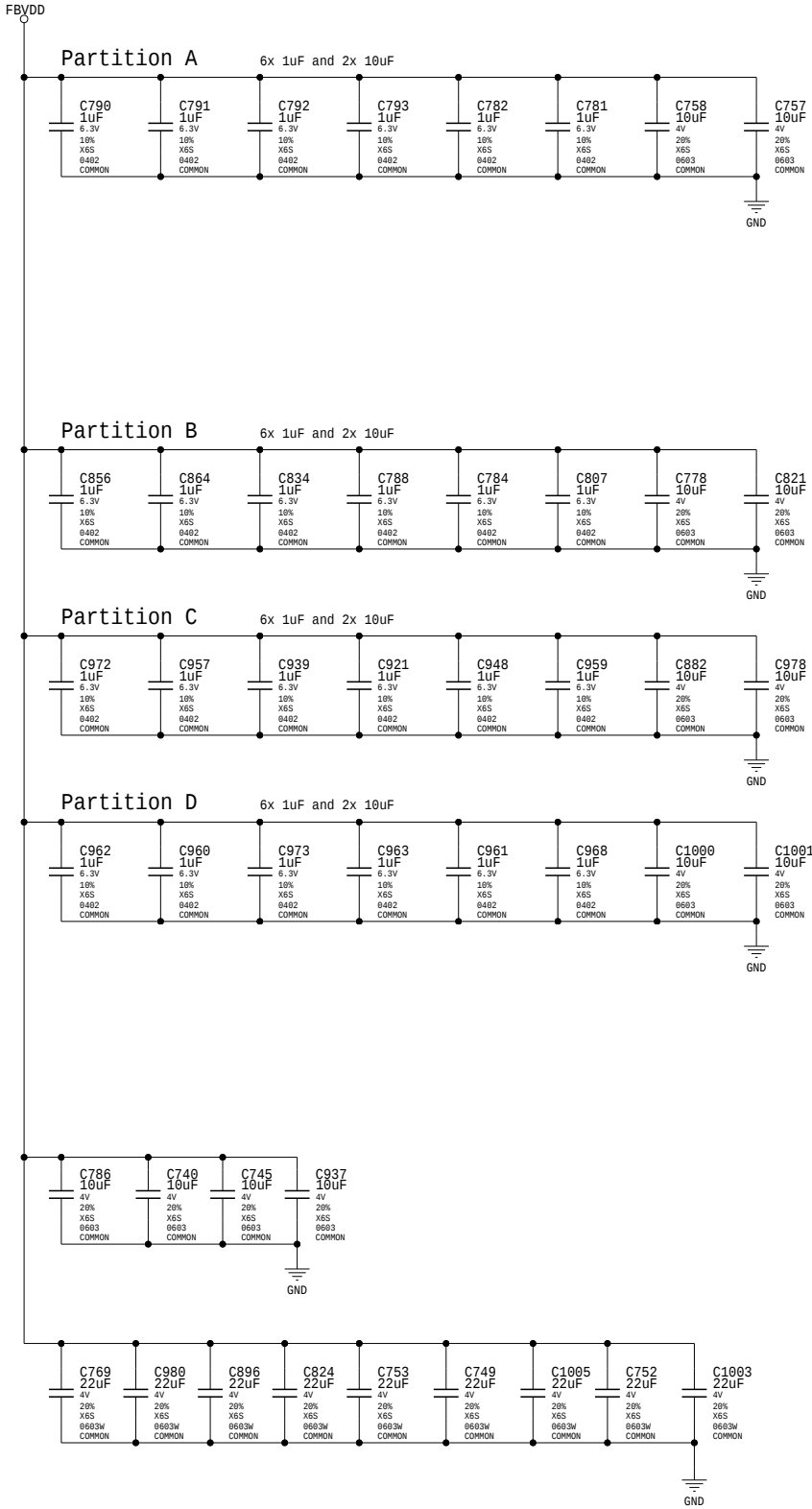
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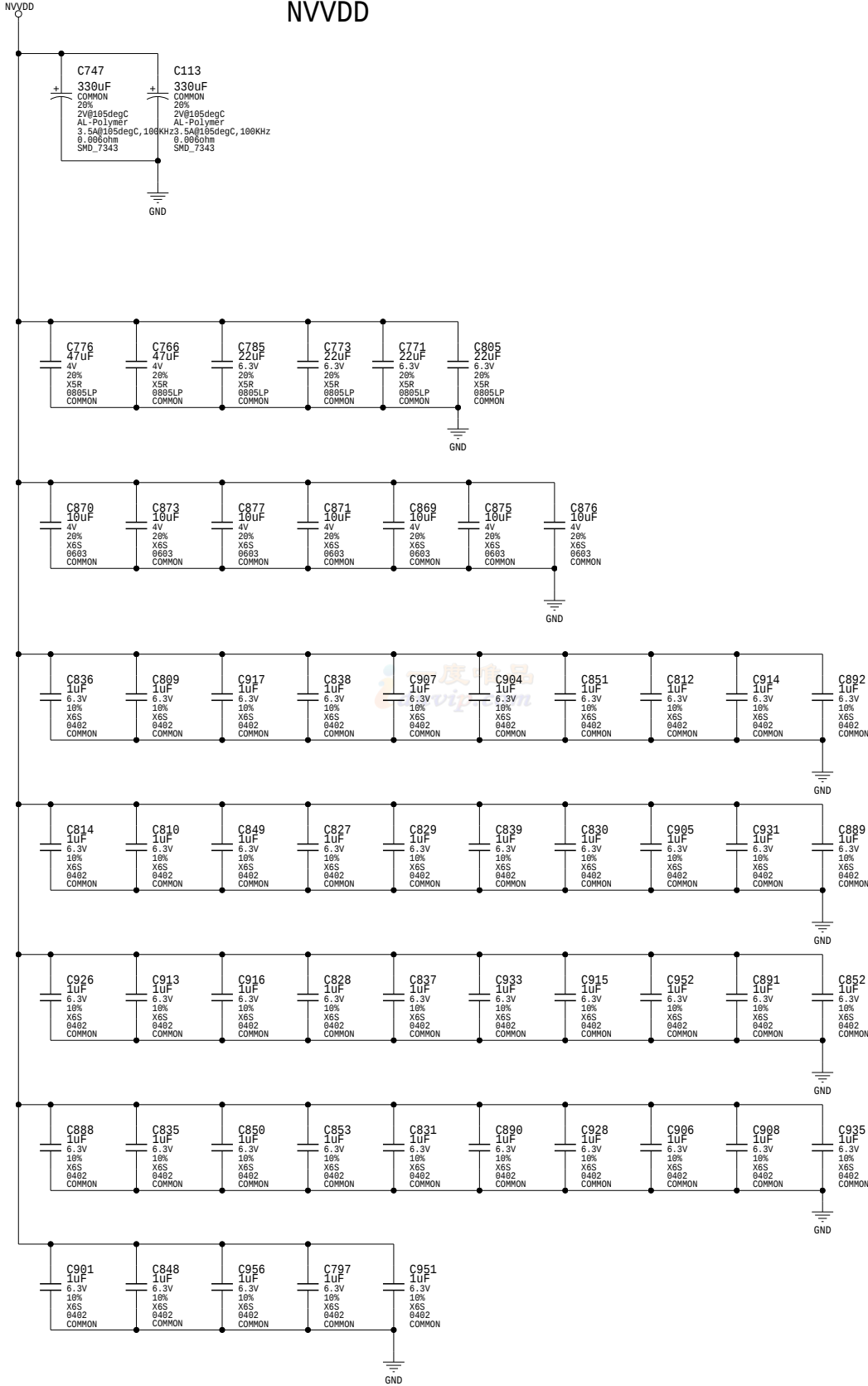
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Page15: GPU Decoupling

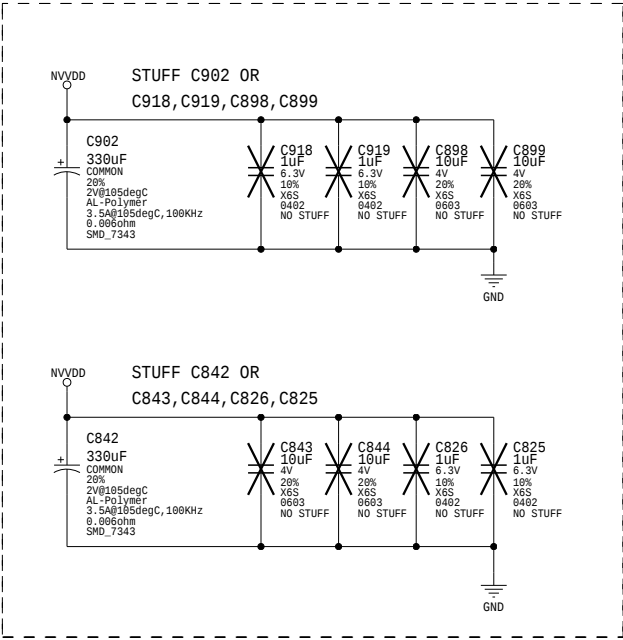
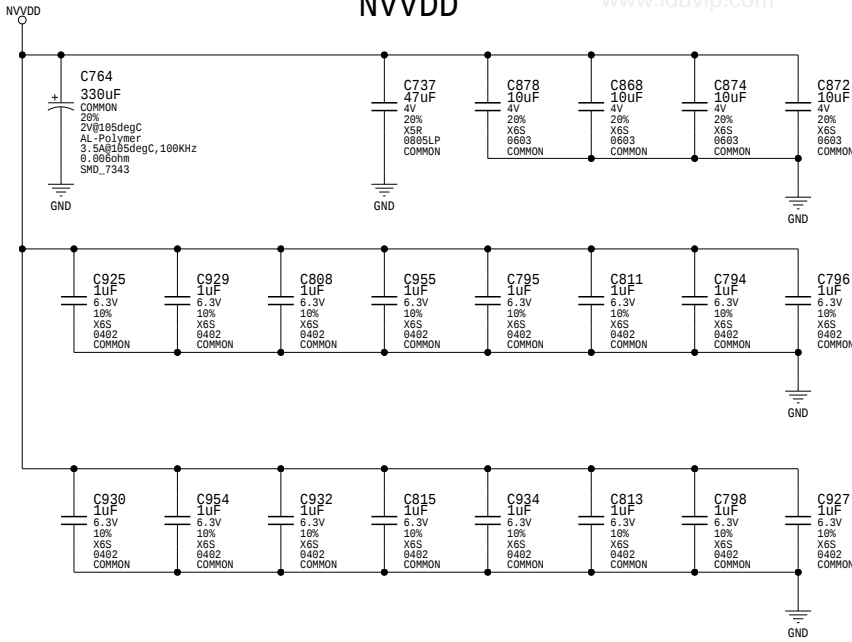
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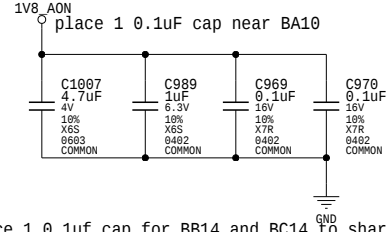
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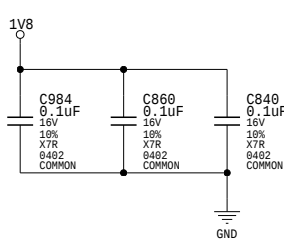
NVVDD



1V8_AON



VDD18



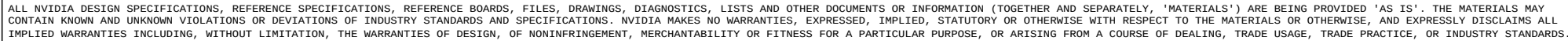
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PAGE DETAIL	GPU Decoupling

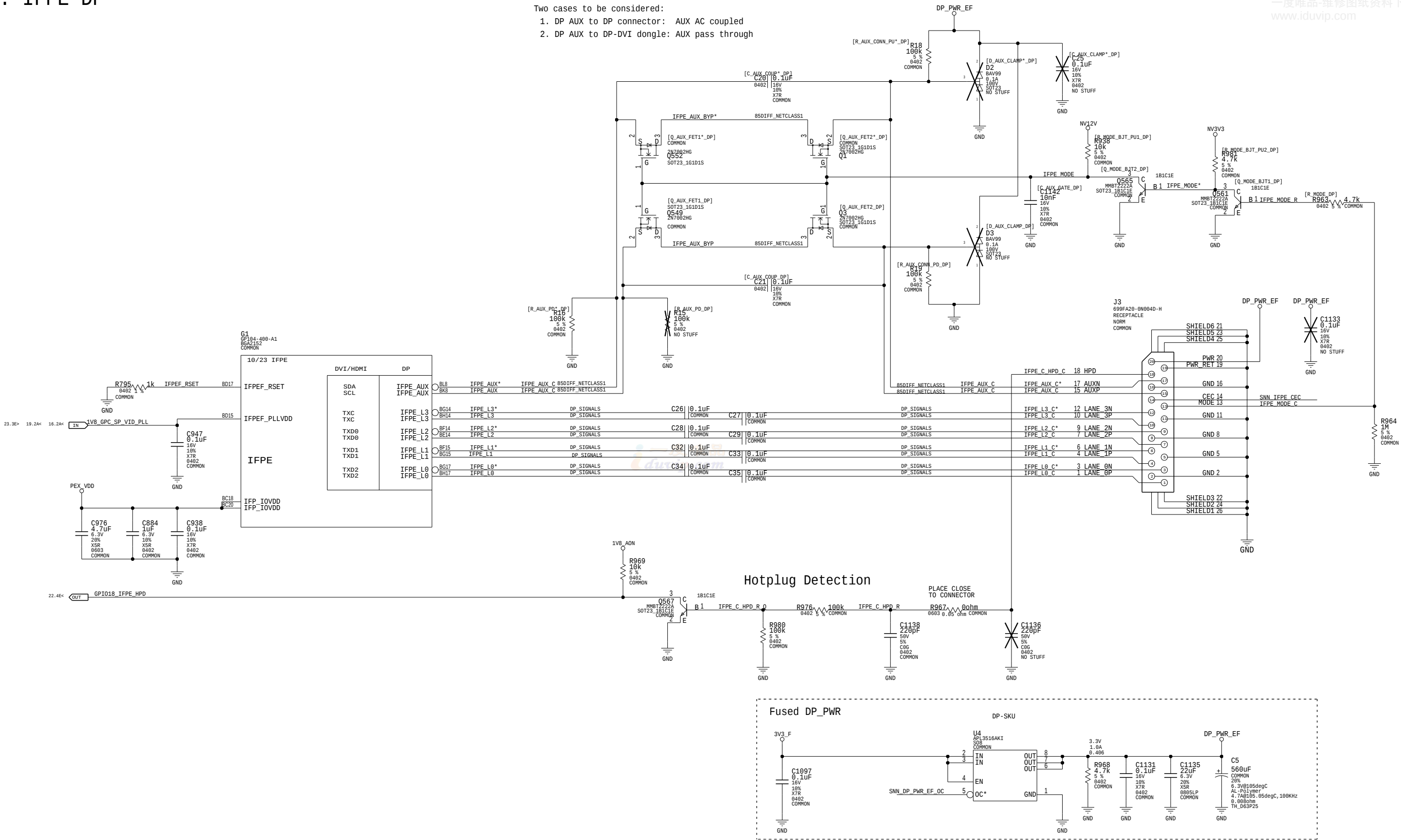
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- Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through

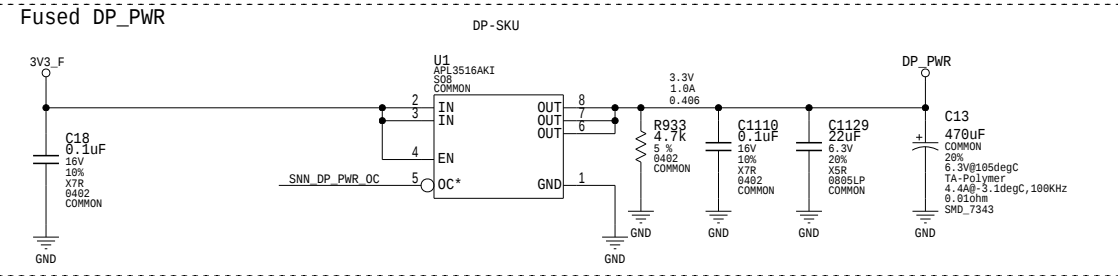
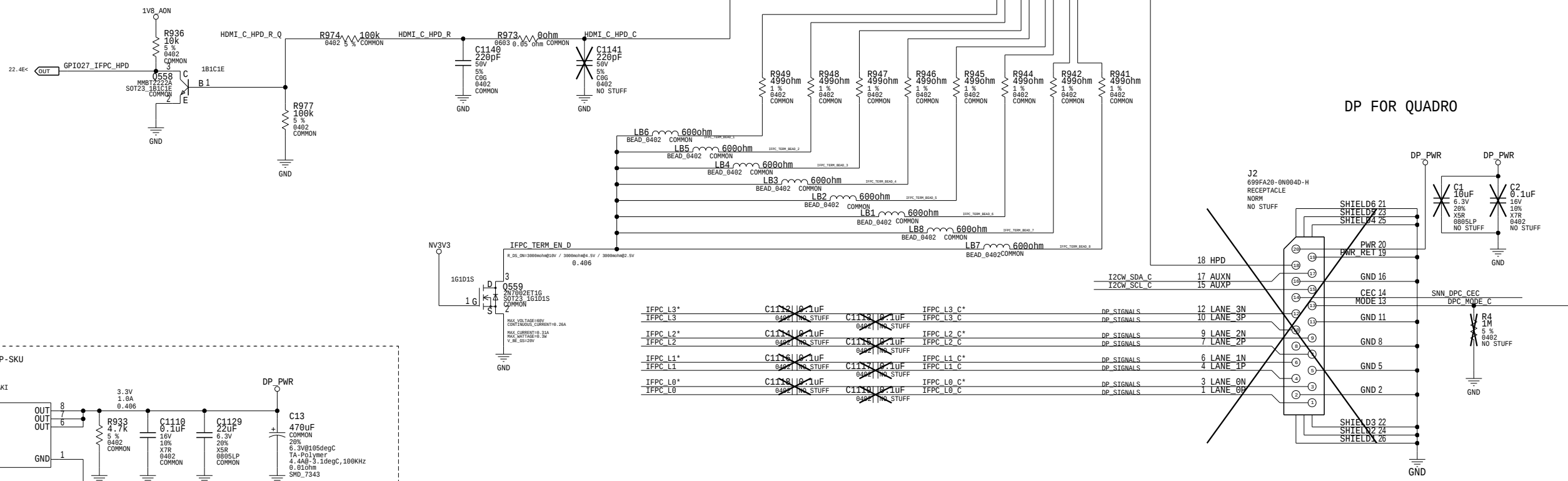
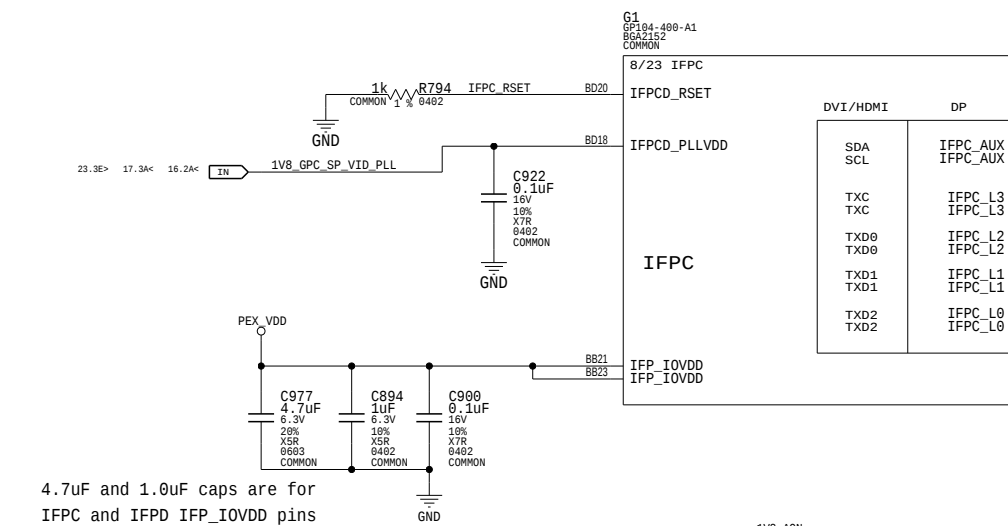
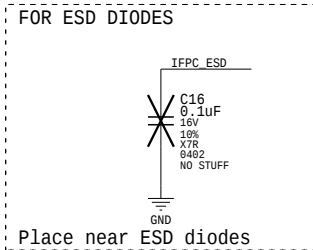


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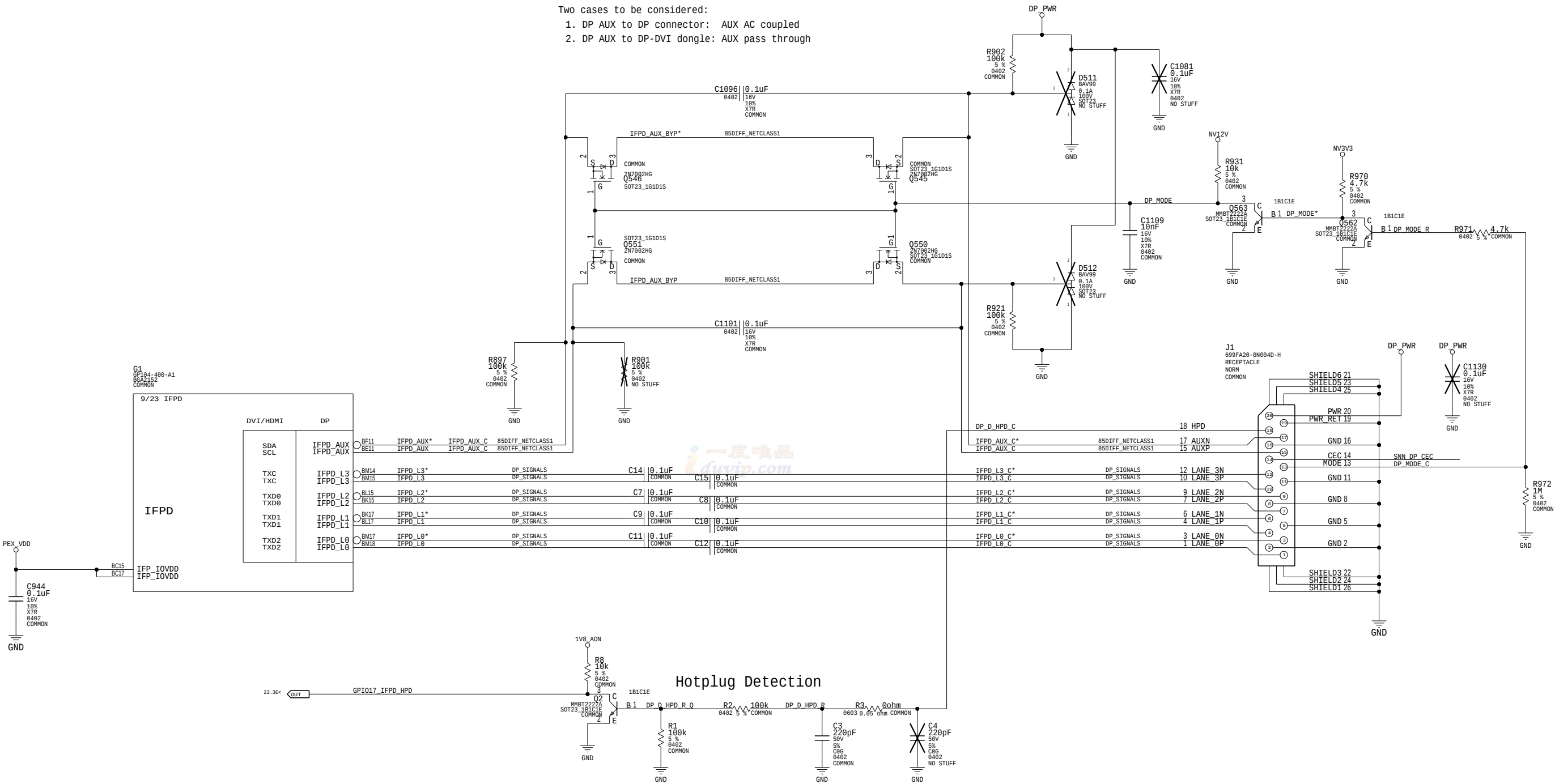


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PAGE DETAIL	IFPC HDMI 2.0/DP

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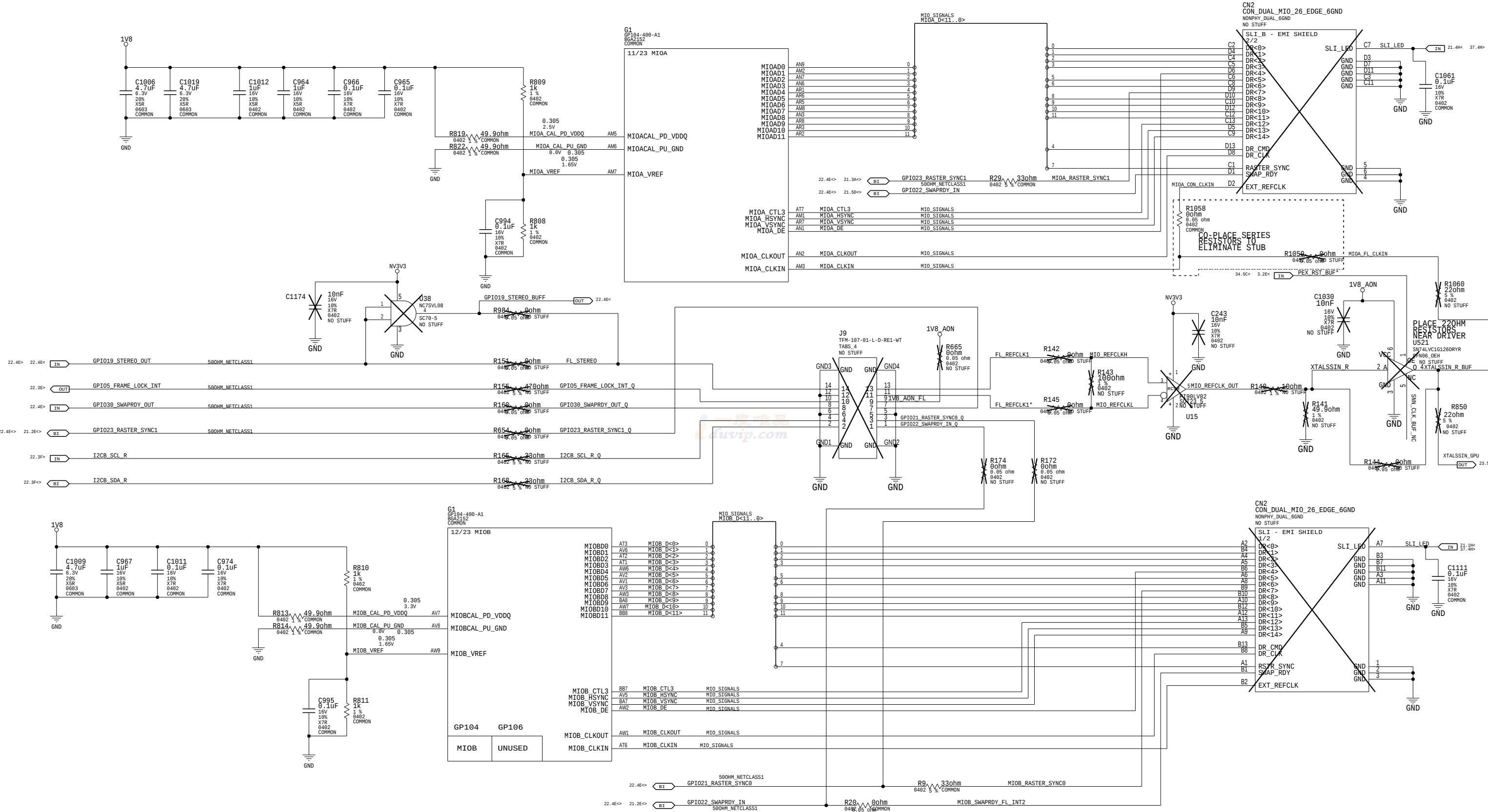
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- Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through



Page21: MIOA/B Interface and FRAME LOCK

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Page23: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
L	L	L	1111 DEFAULT
L	L	H	1110
L	H	L	1101
L	H	H	1100
H	L	L	1011
H	L	H	1010
H	H	L	1001
H	H	H	1000
L	L	M	0111
L	M	L	0110
L	M	H	0101
L	H	M	0100
H	L	M	0011
H	M	L	0010
H	M	H	0001
H	H	M	0000

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

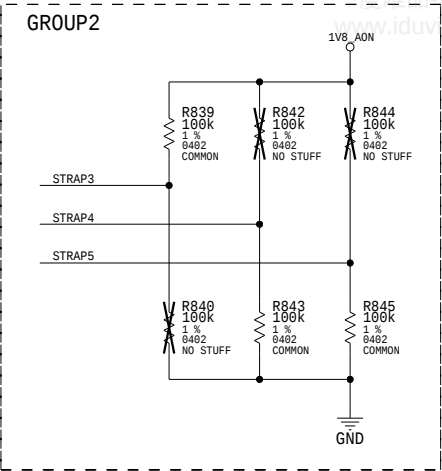
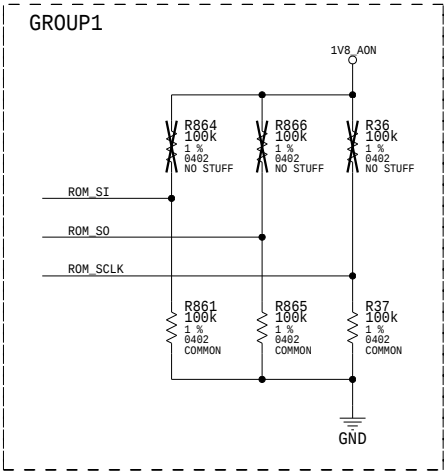
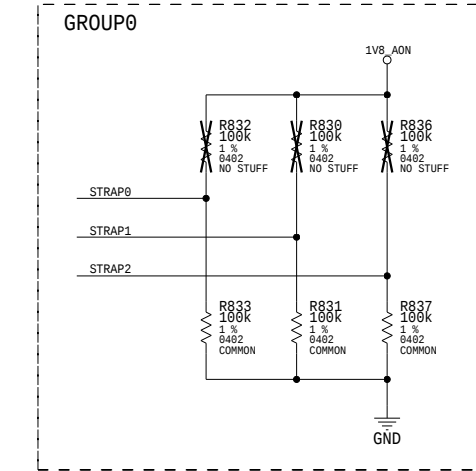
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

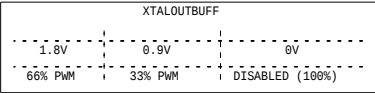
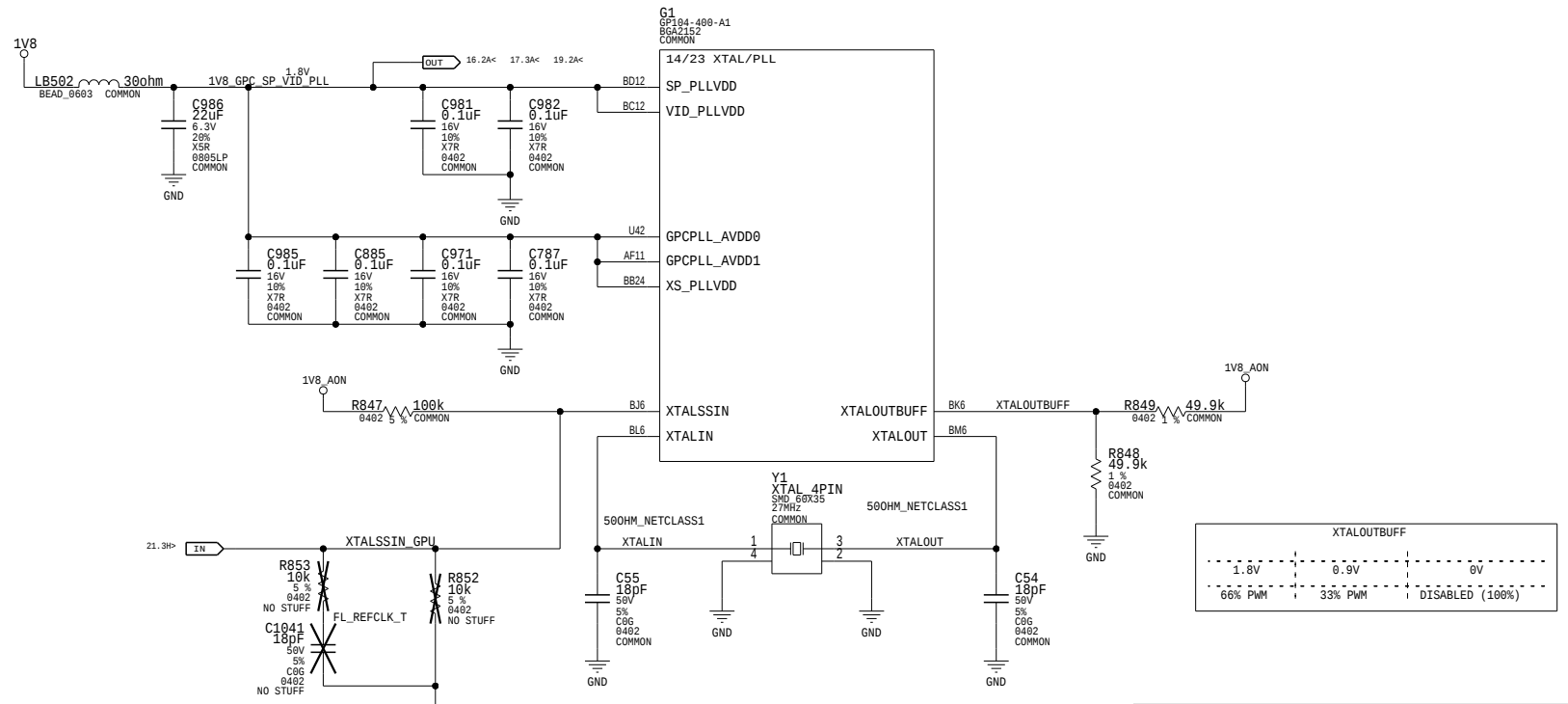
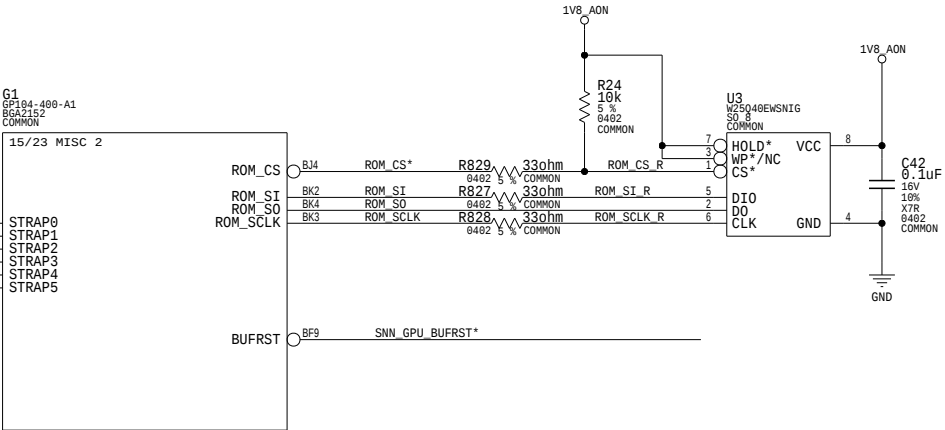
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



CFG[3:0]	Config	Width	Vendor
0000	256Mx32	256-bit	Micron
0001	Reserved		
0010	Reserved		
0011	Reserved		
0100	Reserved		
0101	Reserved		
0110	Reserved		
0111	Reserved		

STRAP0	BL3
STRAP1	BL4
STRAP2	BM4
STRAP3	BM5
STRAP4	BK5
STRAP5	B35



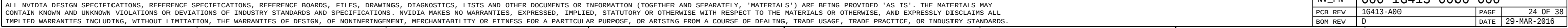
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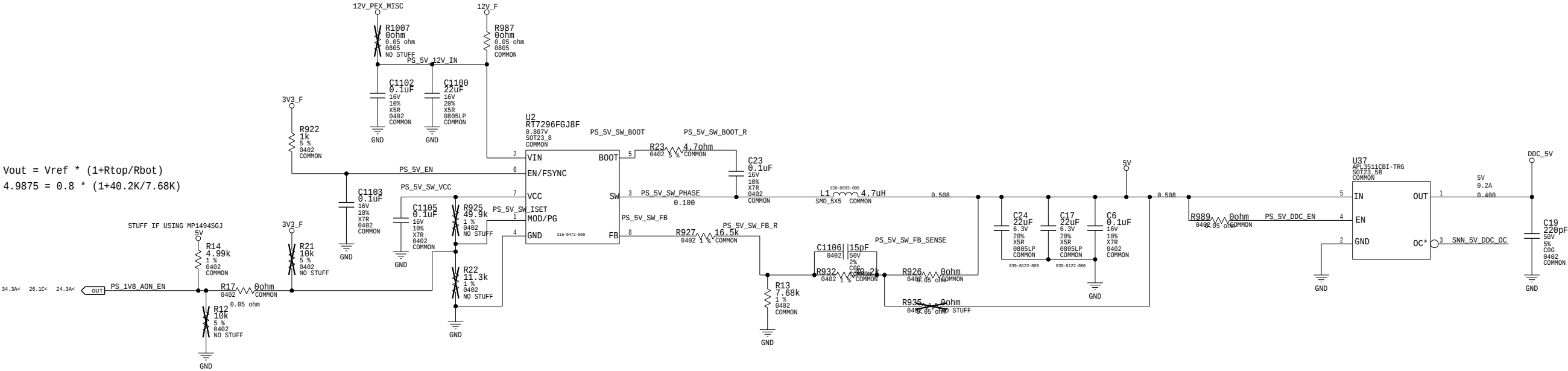
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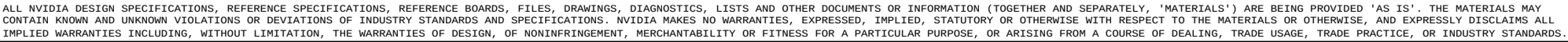


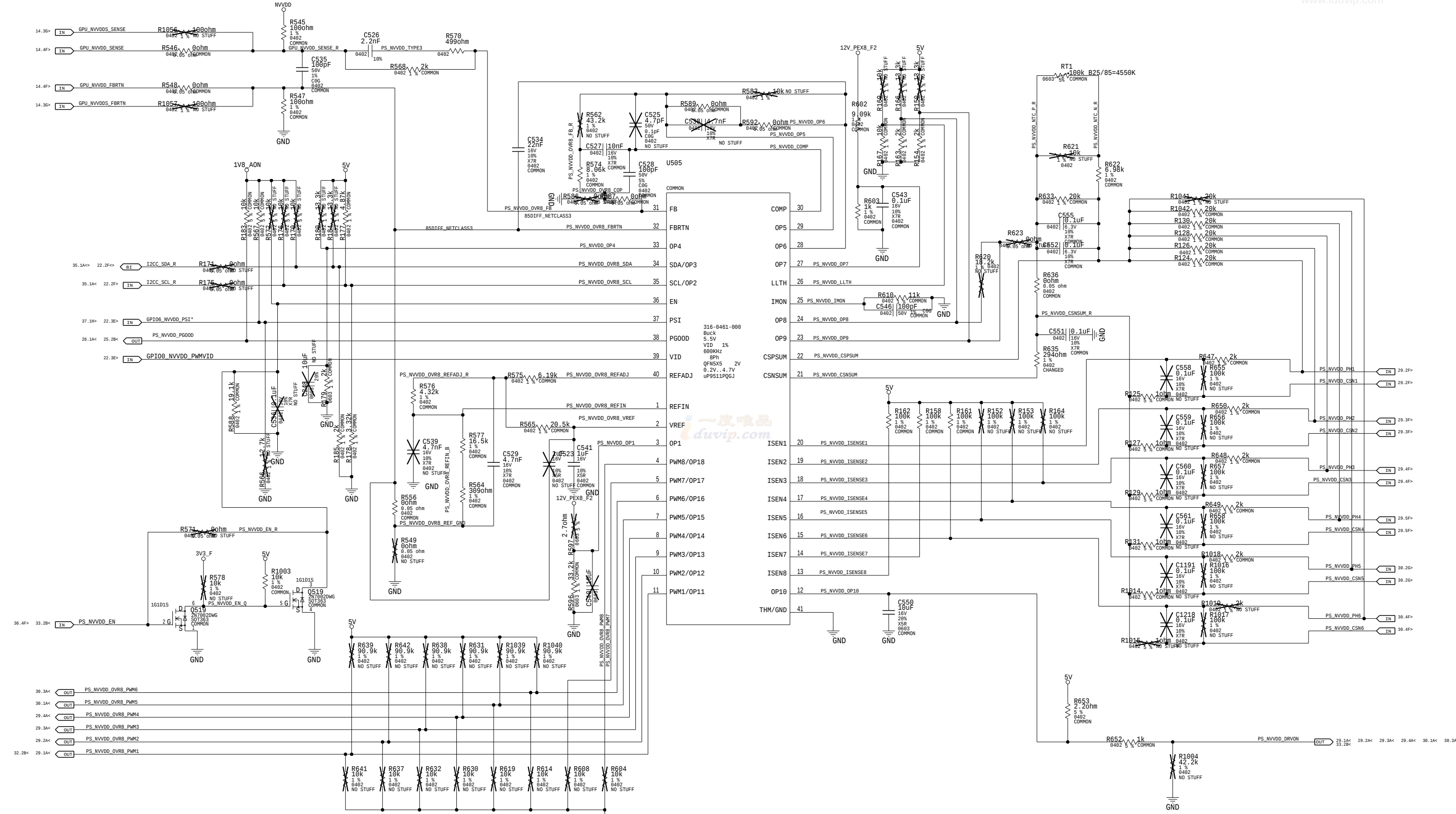
ASSEMBLY	SKU0000 SCHEMATIC COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: 1V8, 1V8_A0N

PEX PLL Switcher

$$V_{out} = V_{ref} * (1 + R_{top}/R_{bot})$$
$$1.0086 = 0.6 * (1 + 6.81K/10K)$$

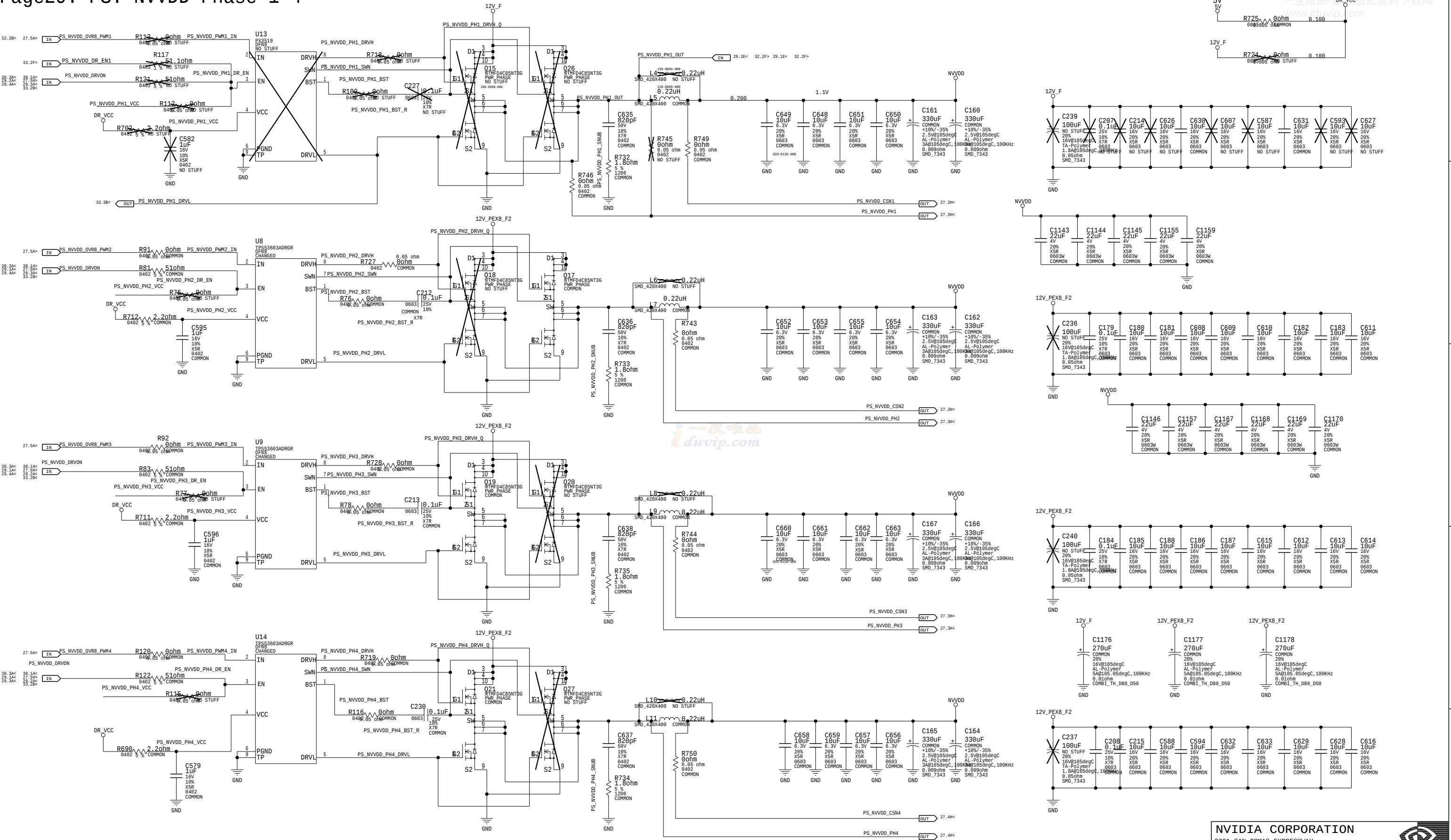


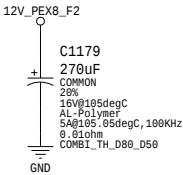
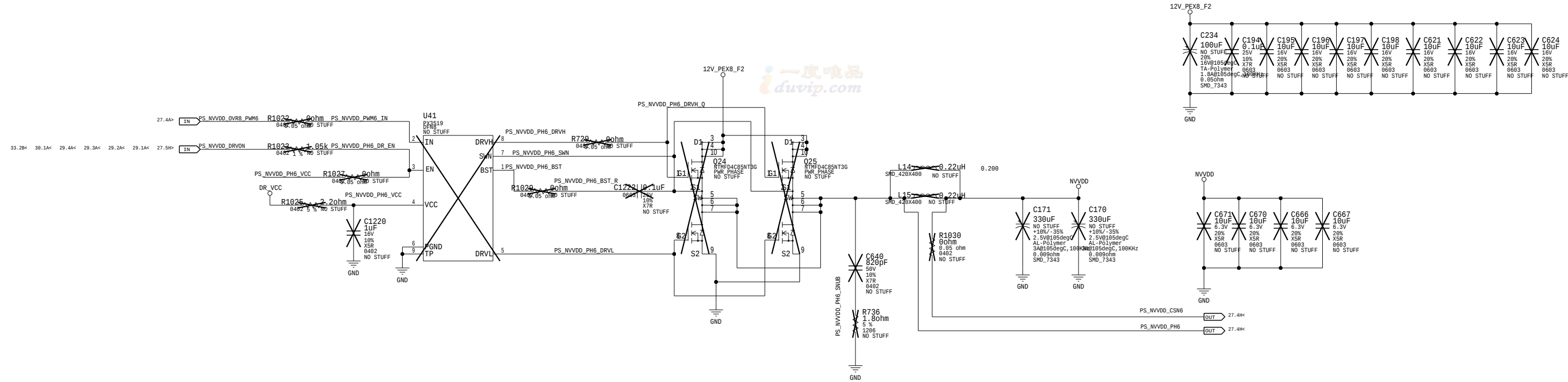
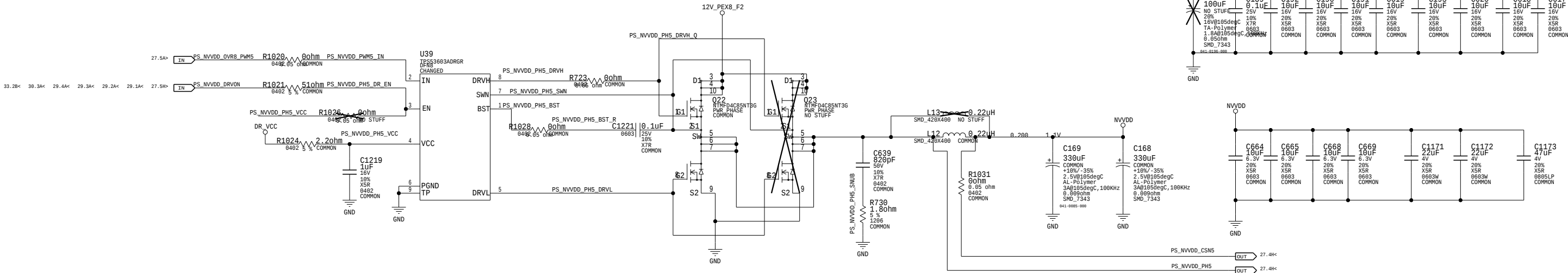




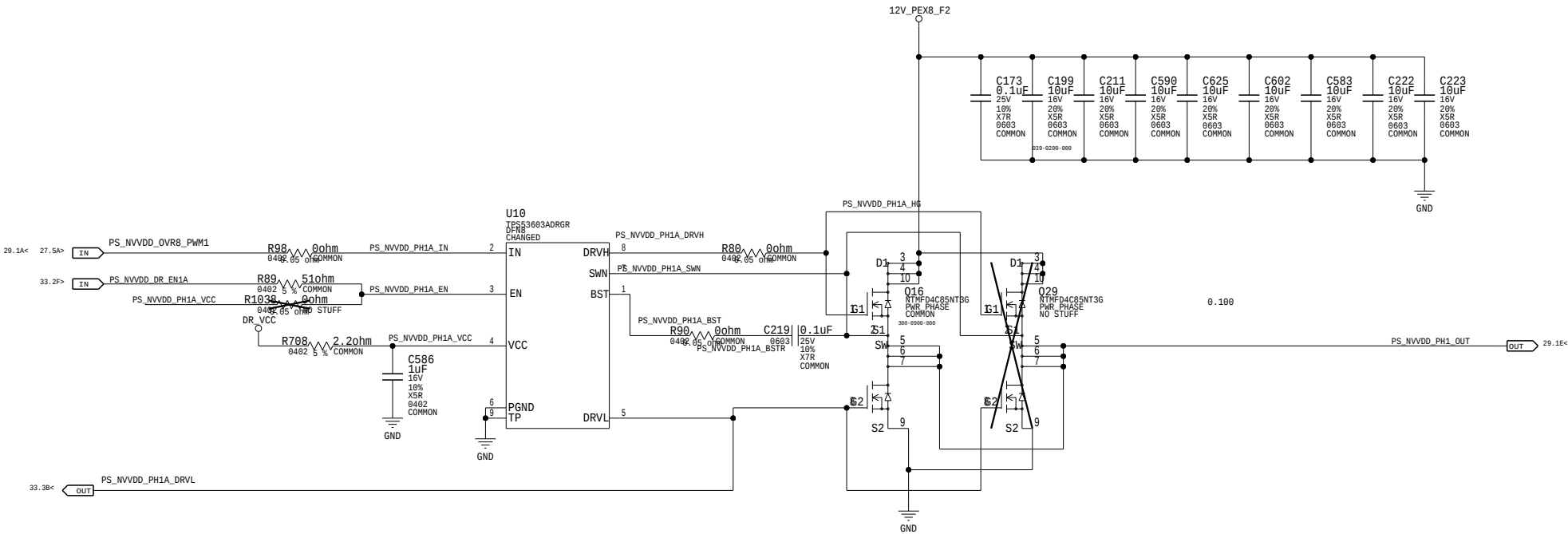


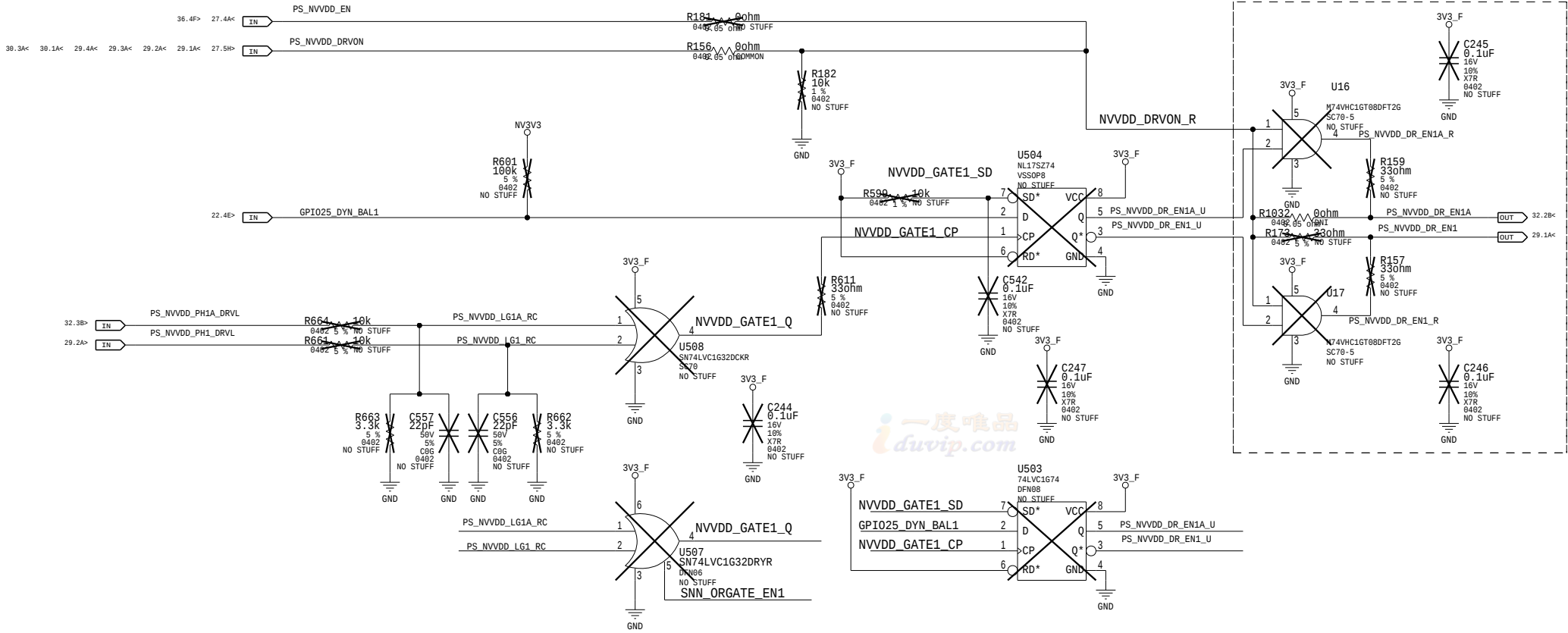
Page29: PS: NVVDD Phase 1-4











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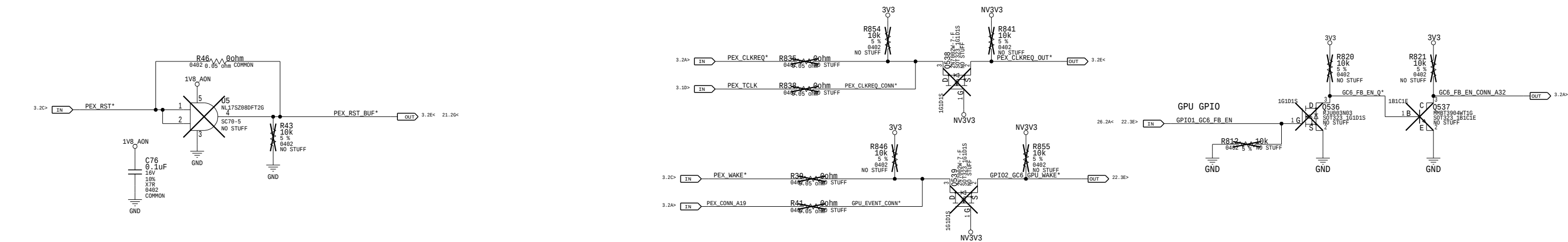
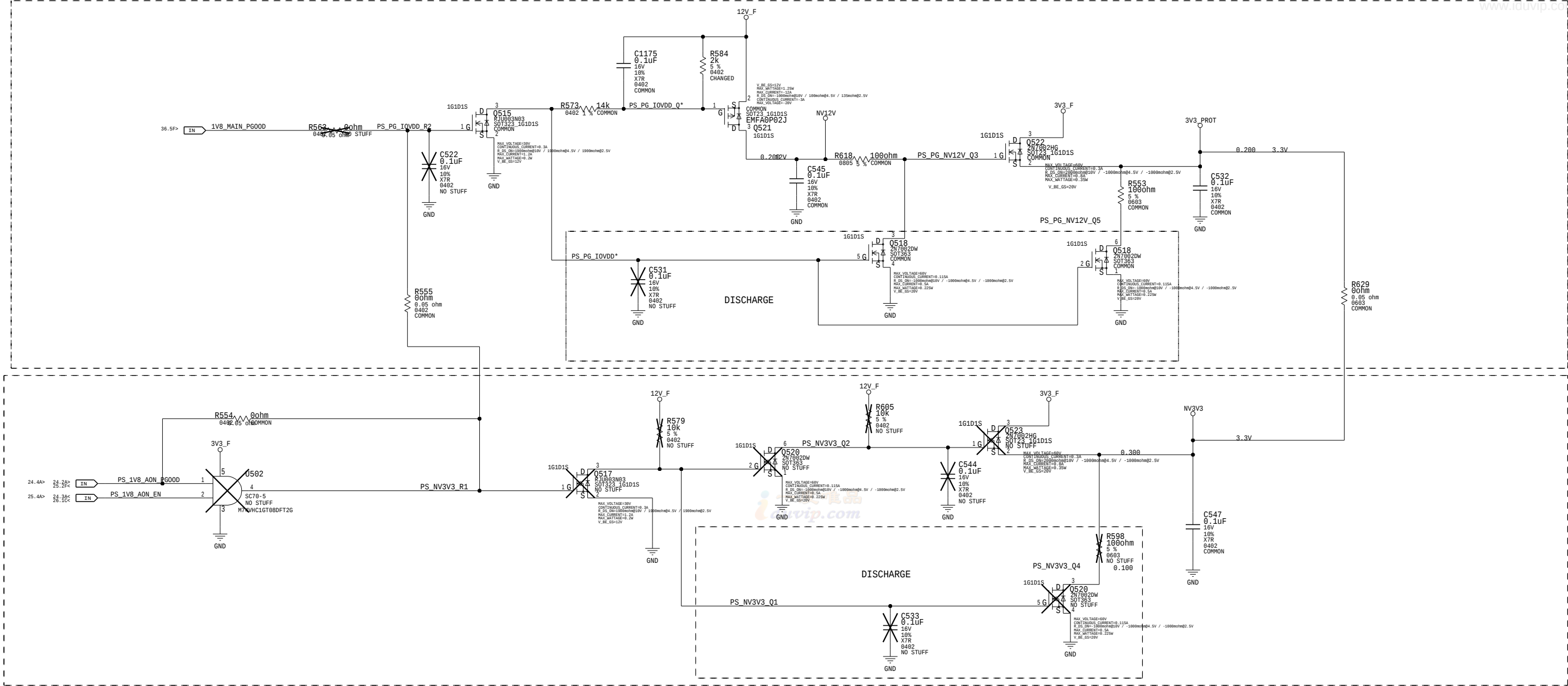
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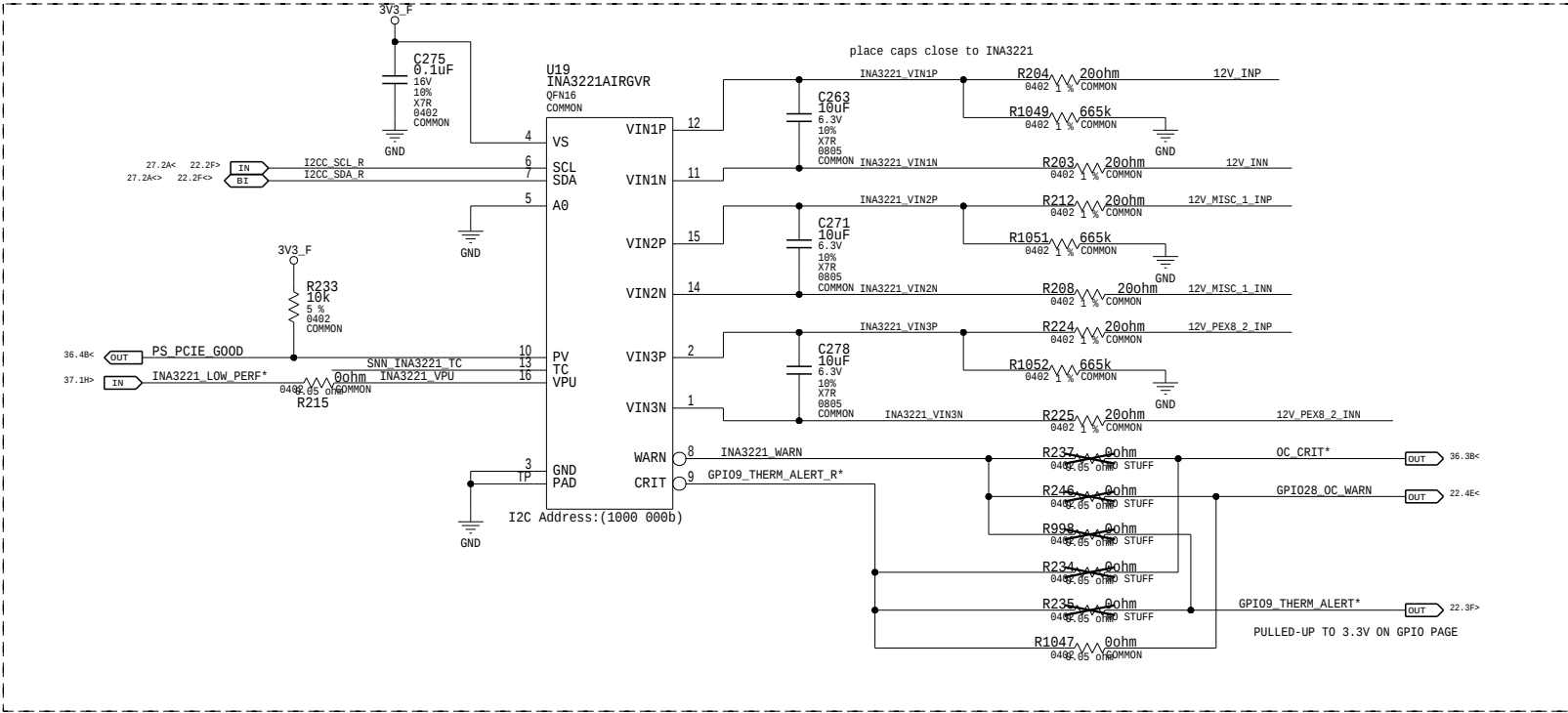
NV_PN	600-1G413-0000-000		
PCB REV	1G413-A00	PAGE	33 OF 38
BOM REV	D	DATE	29-MAR-2016

ASSEMBLY	SKU0000 SCHEMATIC COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: Dynamic Power Balance Logic

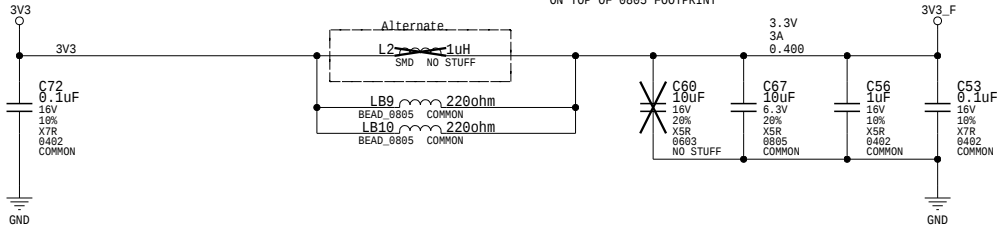


Page35: PS: Inputs, Filtering, and Monitoring

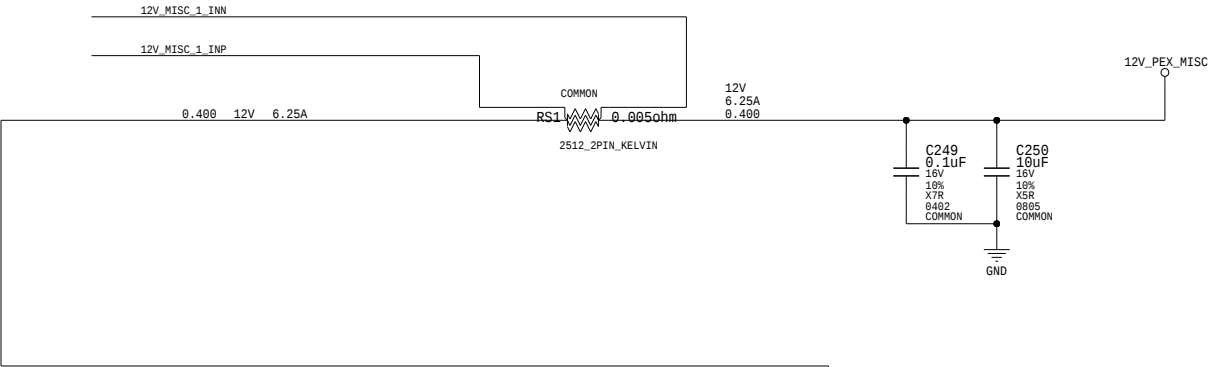
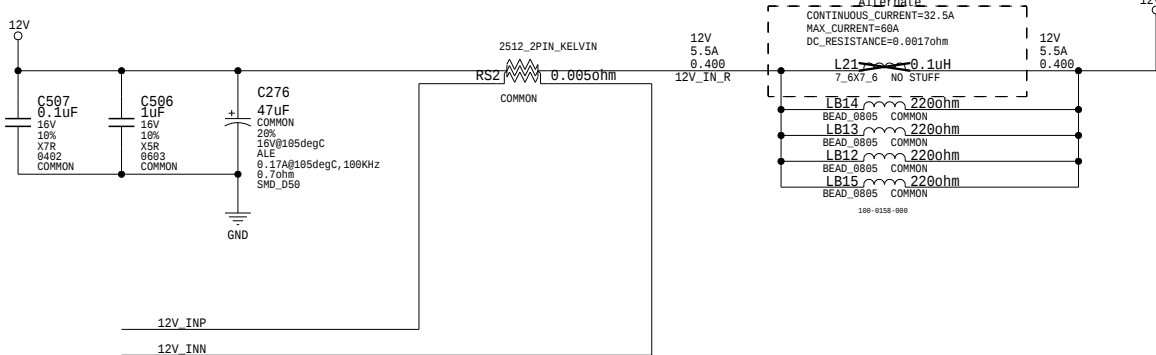
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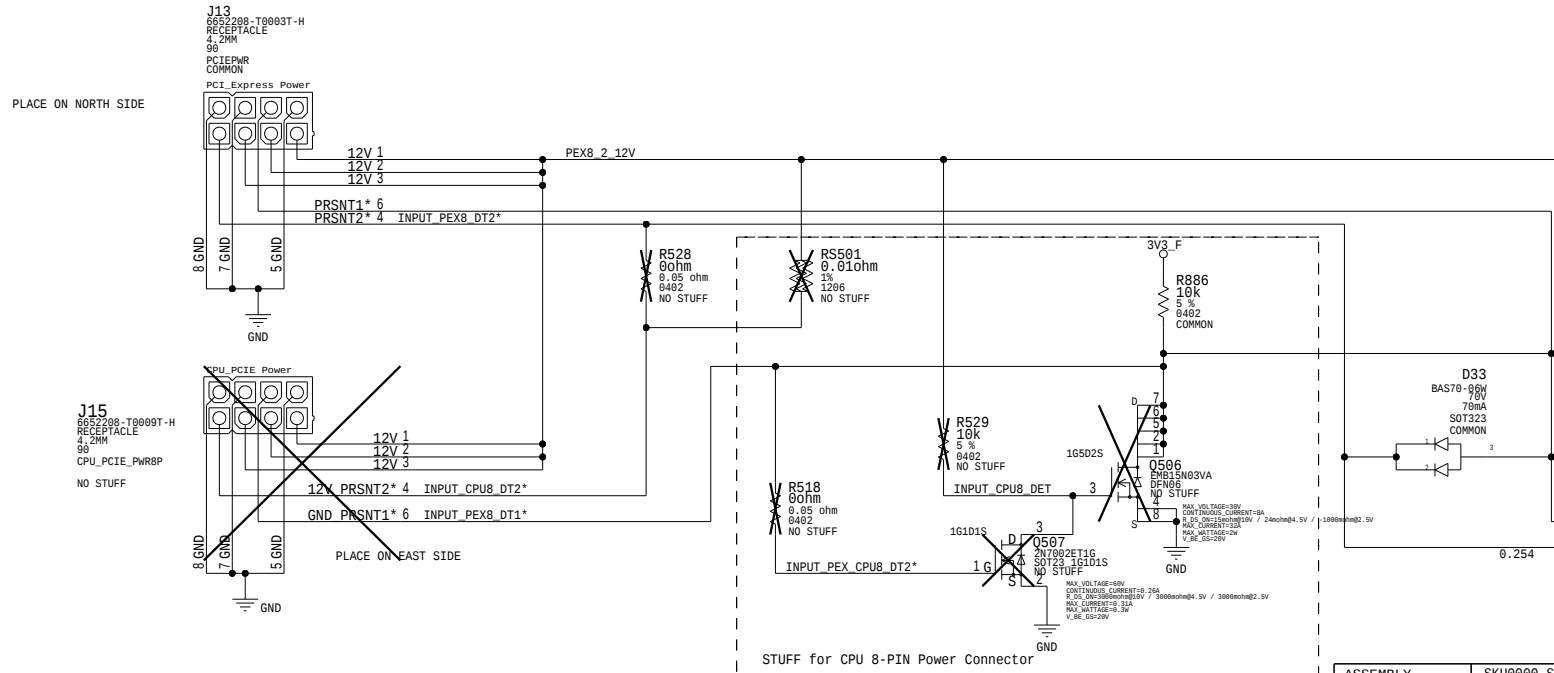
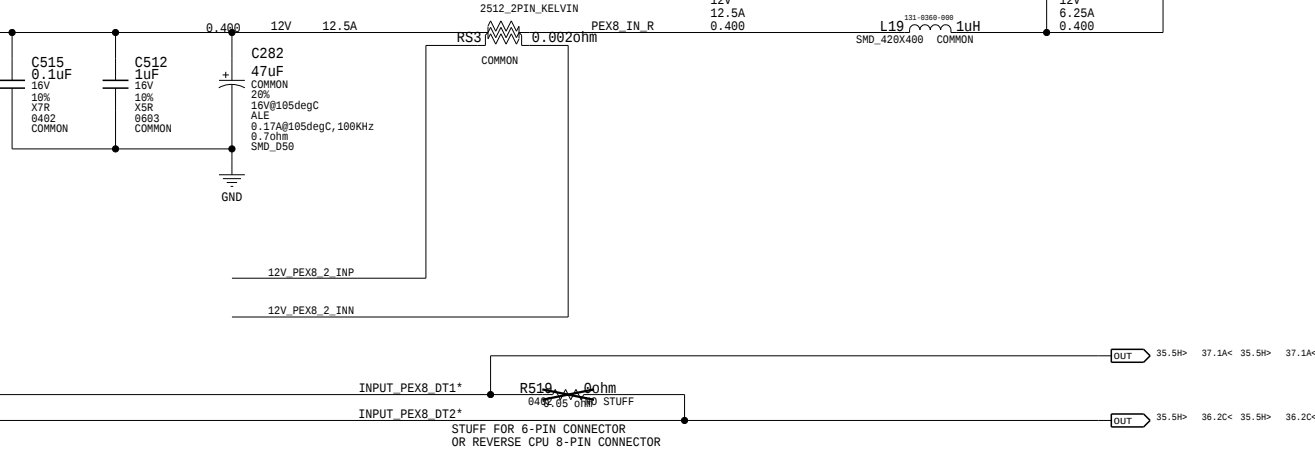
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



PEX8 INPUT 2 - 2x4 PCIE CON 150W



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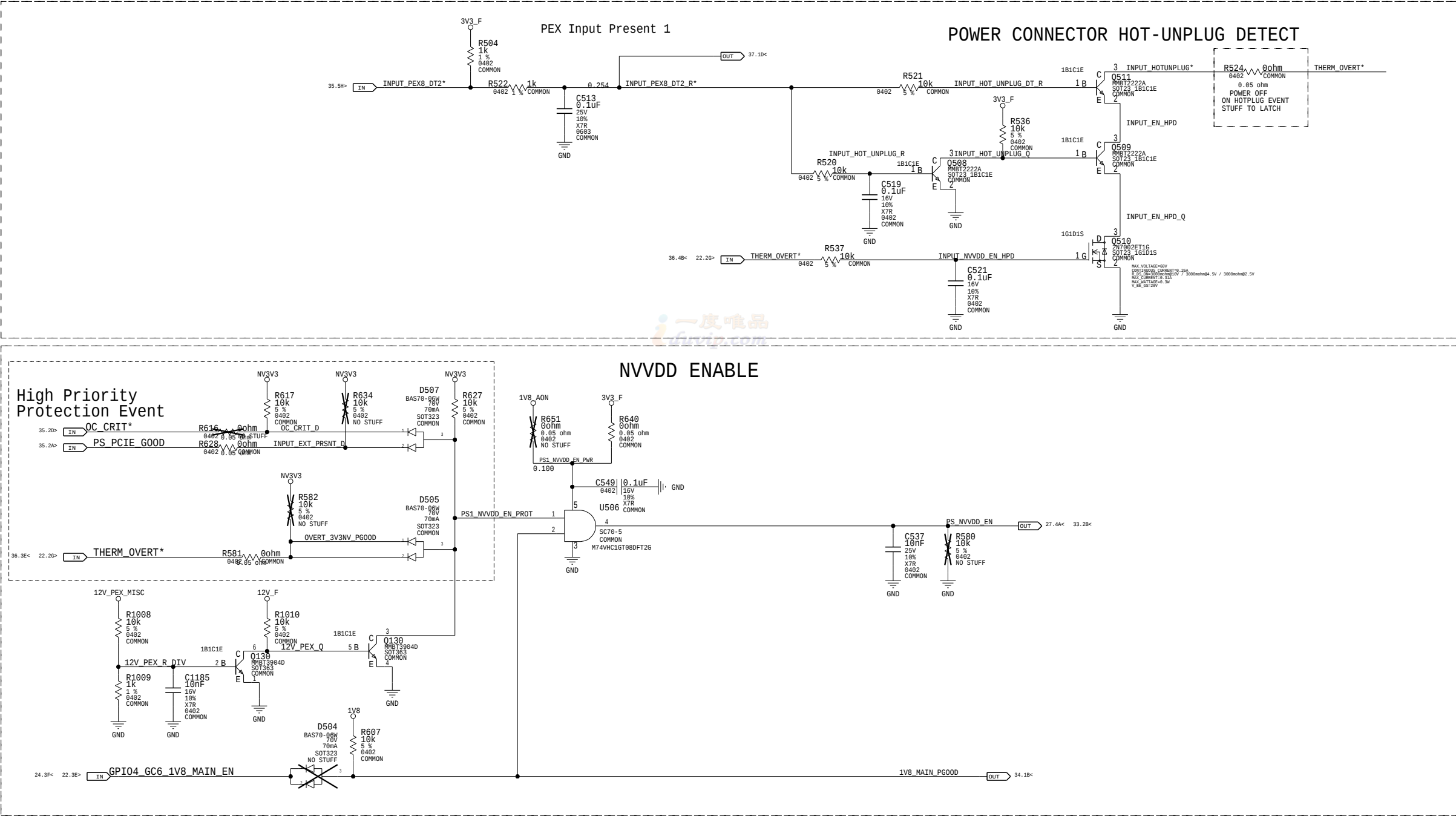
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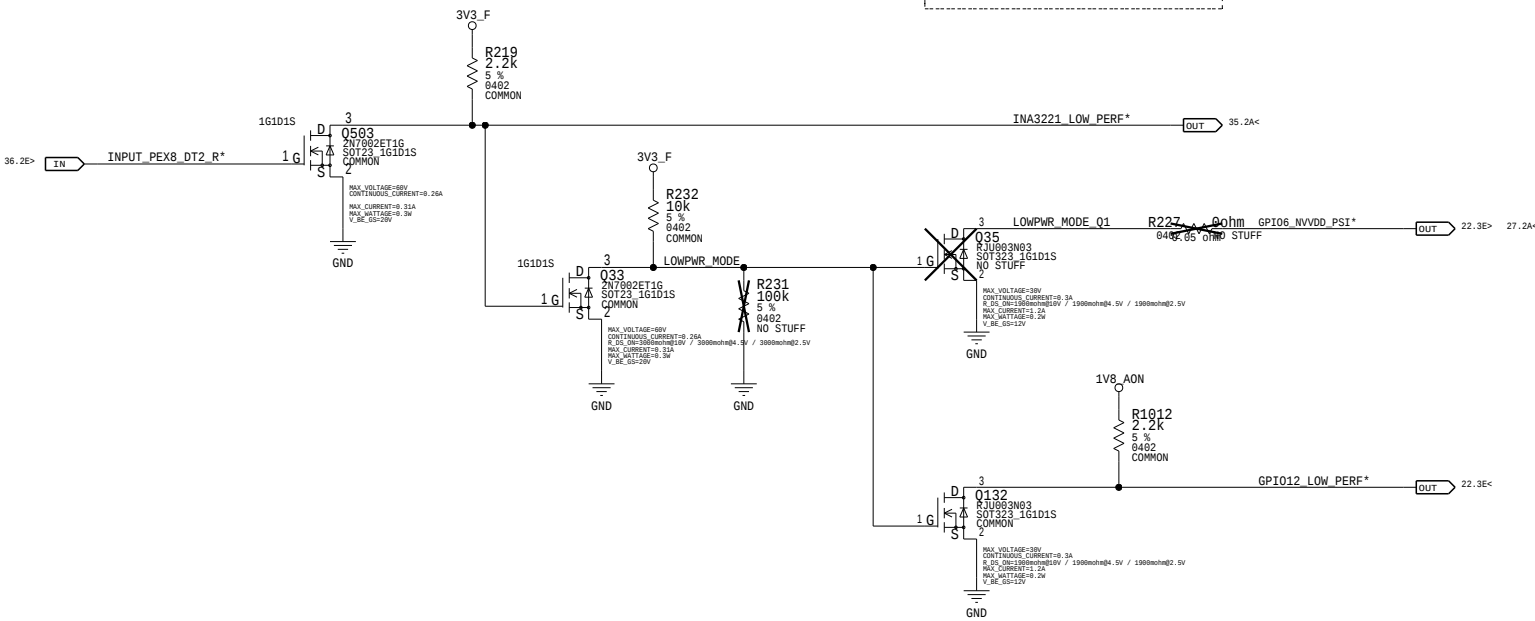
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PCB REV 1G413-A00 PAGE 35 OF 38
BOM REV D DATE 29-MAR-2016

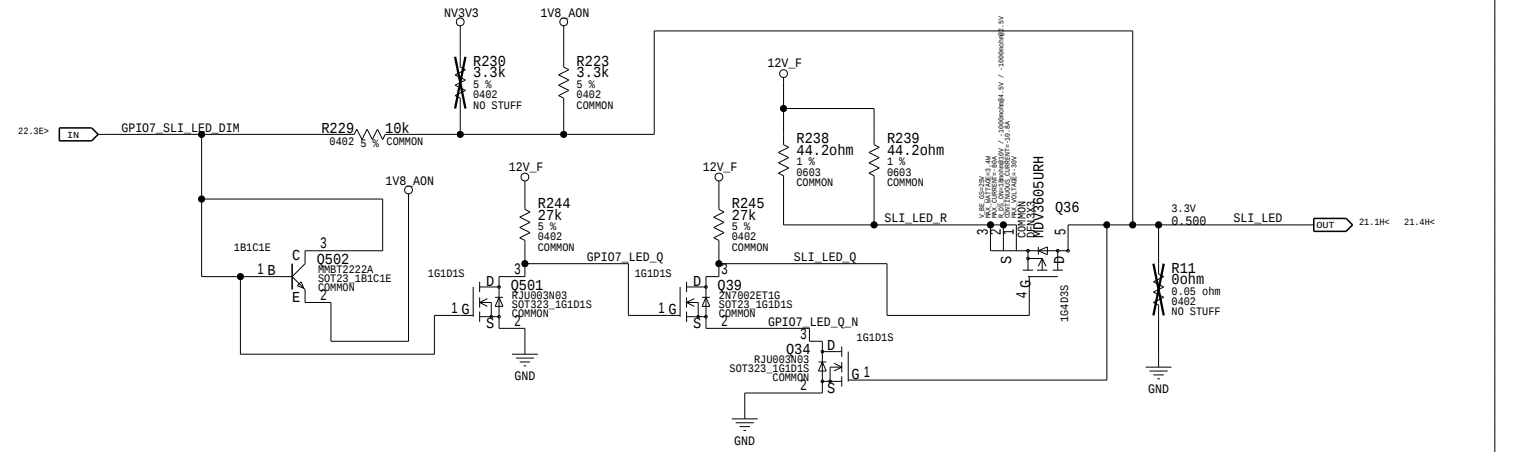
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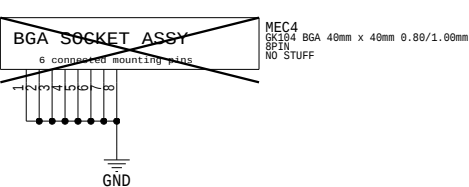
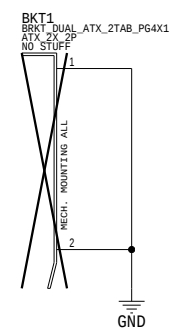
PEX Input - Power Level/PSI* Control



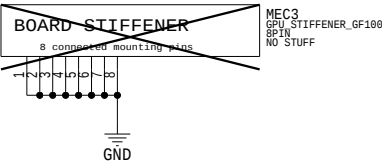
SLI LED (GEFORCE ONLY)



Brackets:



GPU Stiffner



Mechanical Holes Symbol

