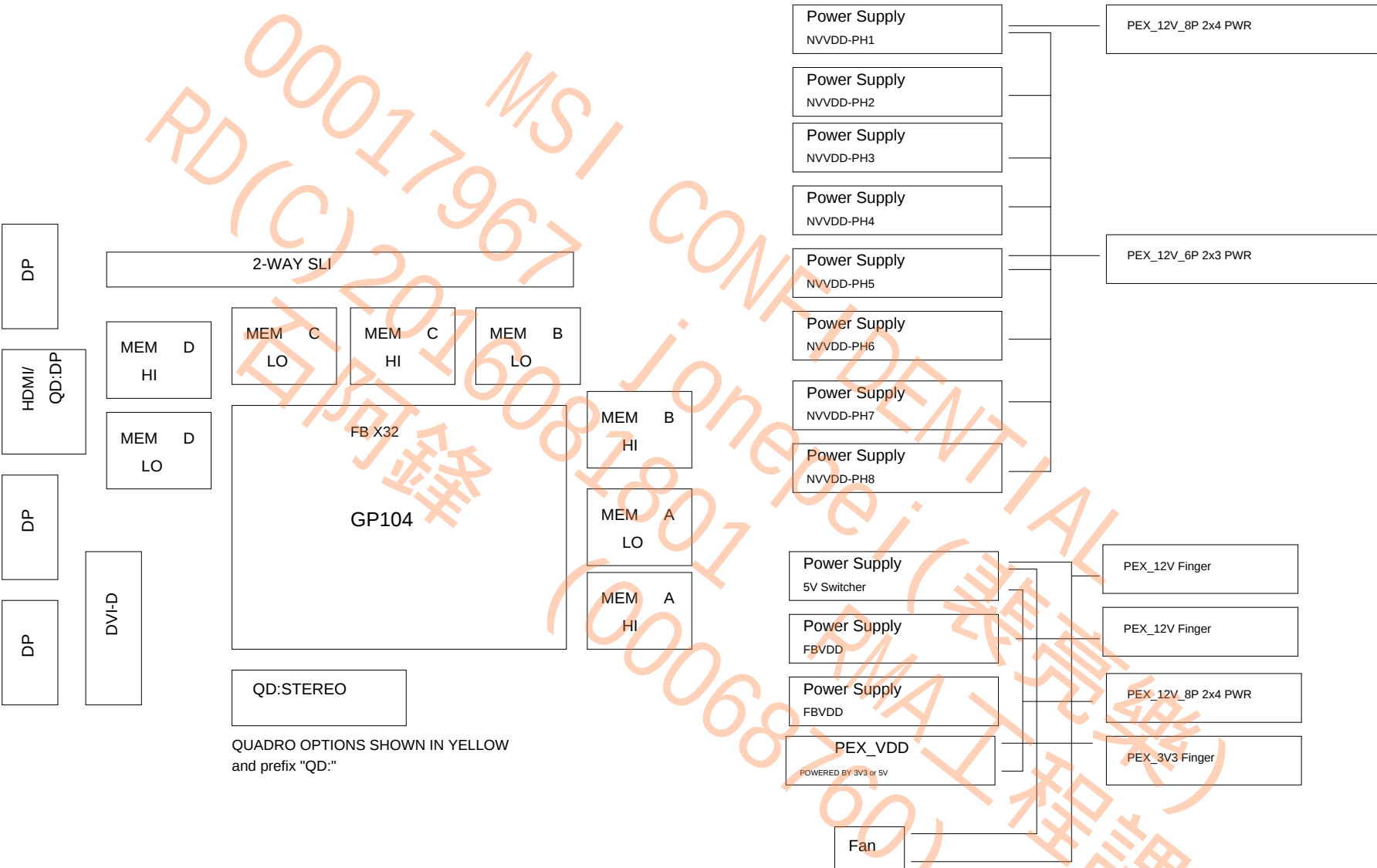


PG413 A00

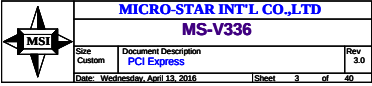
GP104 - 8GB GDDR5X, 256b, 256Mx32
Tall DVI-D + DP + DP + DP/HDMI + DP

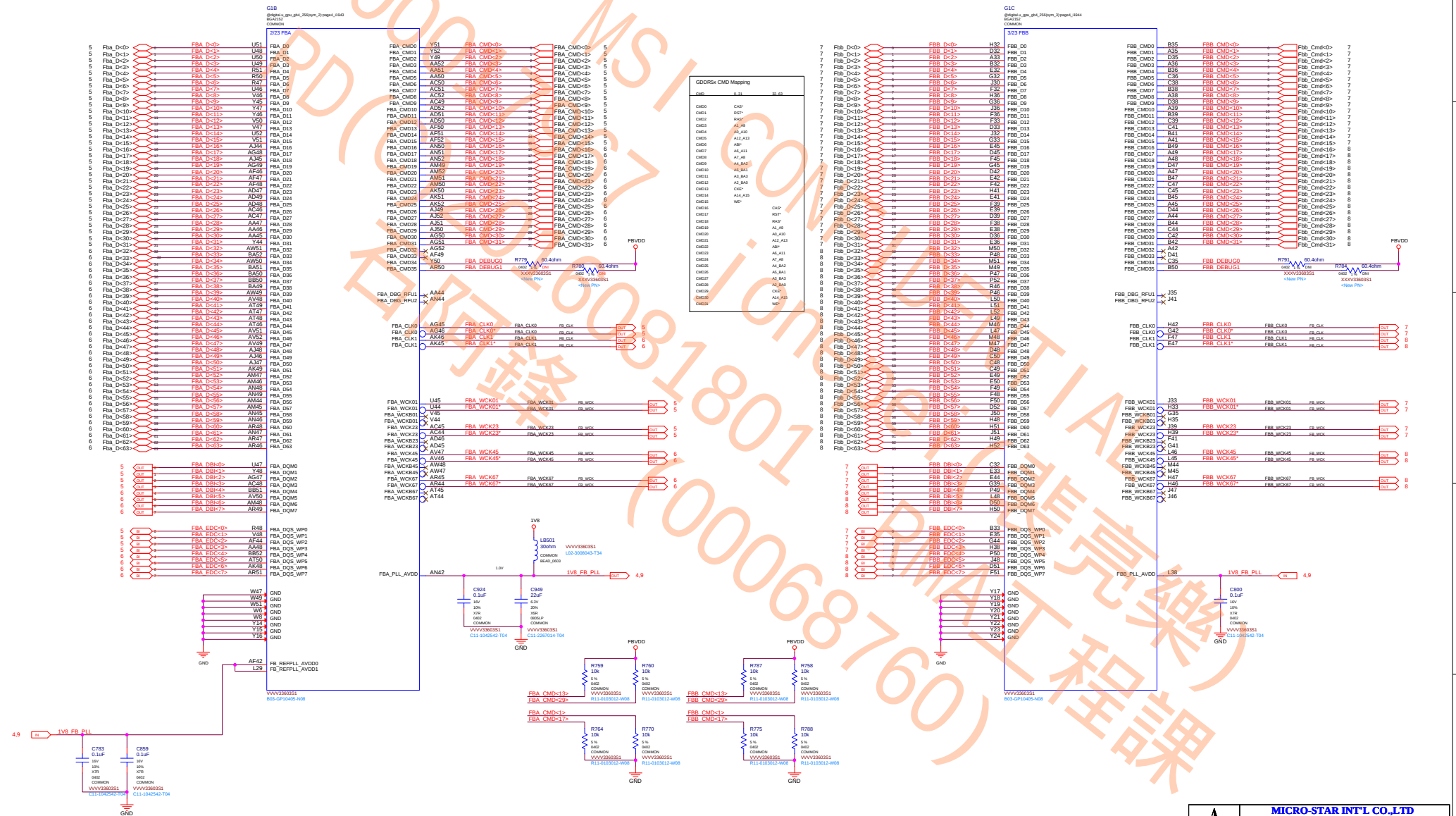
TABLE OF CONTENTS

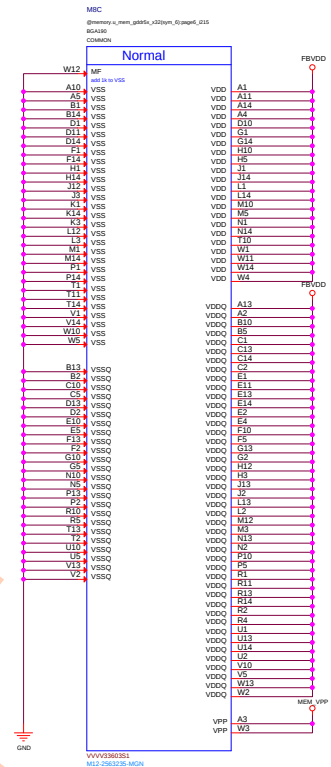
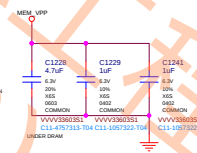
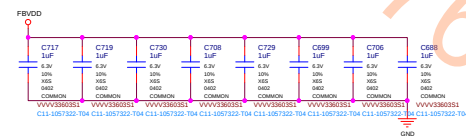
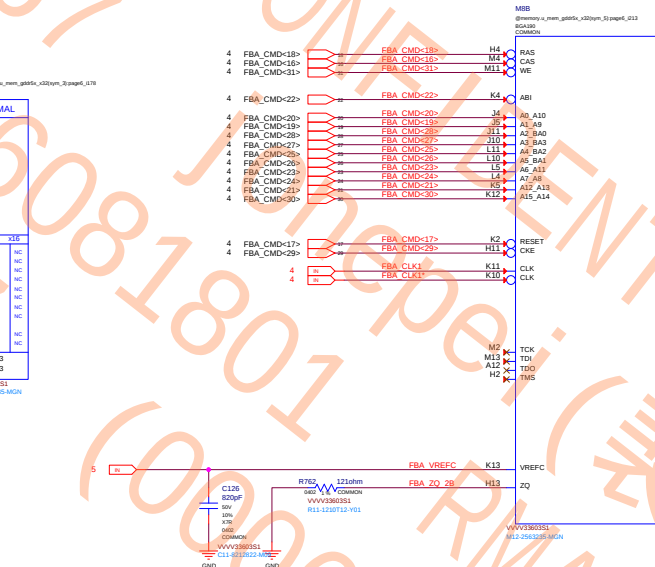
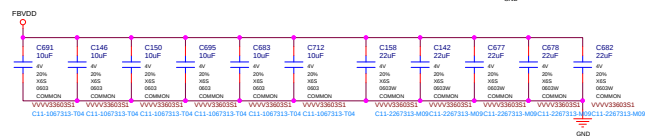
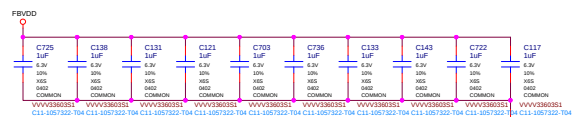
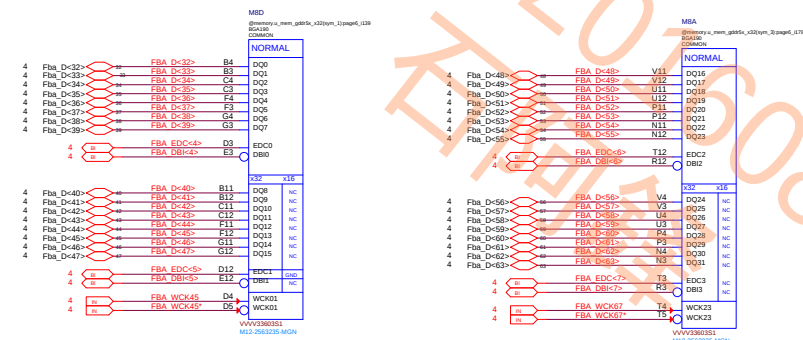
Page	Description	Page	Description
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3	PCI Express	28	PS: Blank Page
4	MEMORY: GPU Partition A/B	29	PS: NVVDD Phase 1-4
5	MEMORY: FBA[31:0]	30	PS: NVVDD Phase 5 & 6
6	MEMORY: FBA[63:32]	31	PS: Blank Page
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8	MEMORY: FBB[63:32]	33	PS: Dynamic Power Balance Logic
9	MEMORY: GPU Partition C/D	34	PS: NV3V3, NV12V
10	MEMORY: FBC[31:0]	35	PS: Inputs, Filtering, and Monitoring
11	MEMORY: FBC[63:32]	36	PS: Shutdown and Sequencing
12	MEMORY: FBD[31:0]	37	PS: 12V Current Steering PSI Control and LED
13	MEMORY: FBD[63:32]	38	MECH: Bracket/Thermal
14	GPU PWR and GND		
15	GPU Decoupling		
16	IFPAB DVI-D-DL		
17	IFPE DP		
18	IFPEF DP		
19	IFPC HDMI 2.0/DP		
20	IFPD DP		
21	MIOA/B Interface and Frame Lock		
22	MISC1: Fan, Thermal, JTAG, GPIO, Stereo		
23	MISC2: ROM, XTAL, Straps		
24	PS: 1V8, 1V8_AON		
25	PS: 5V, PEX_VDD		

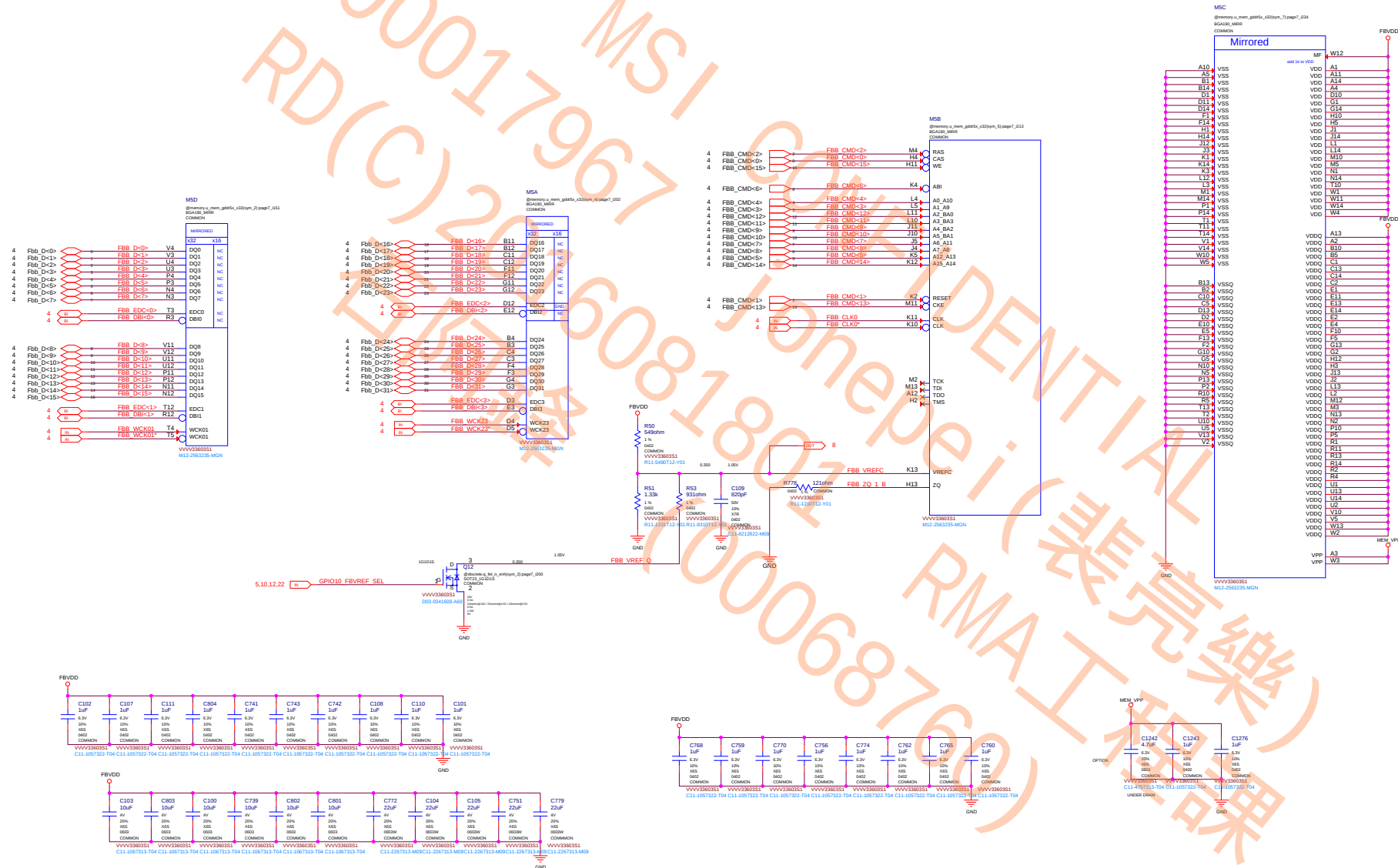


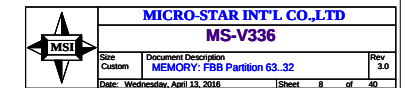
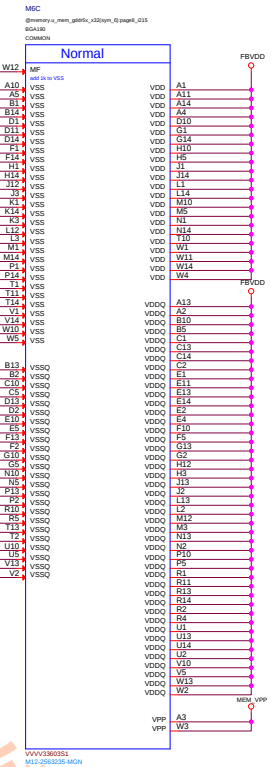
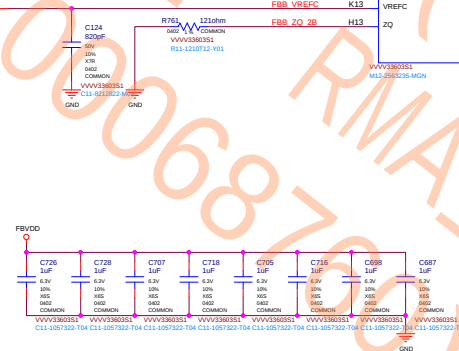
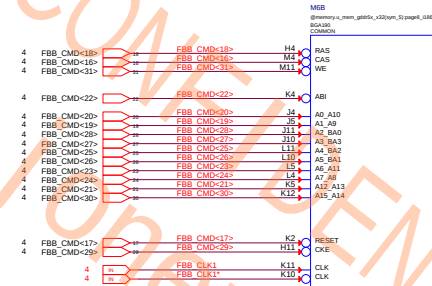
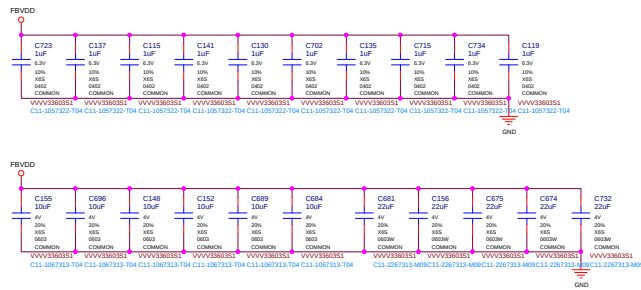
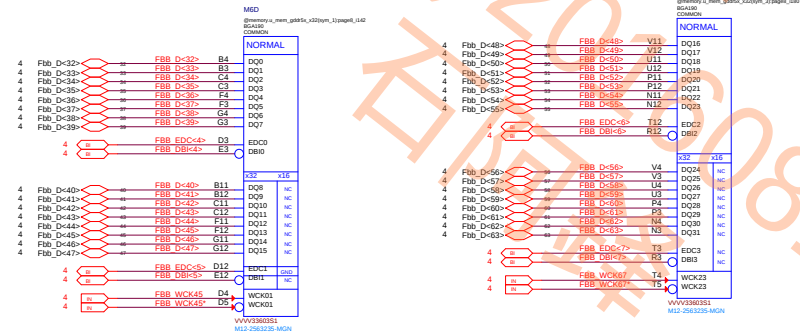
QUADRO OPTIONS SHOWN IN YELLOW
and prefix "QD:"

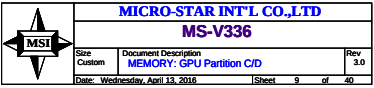


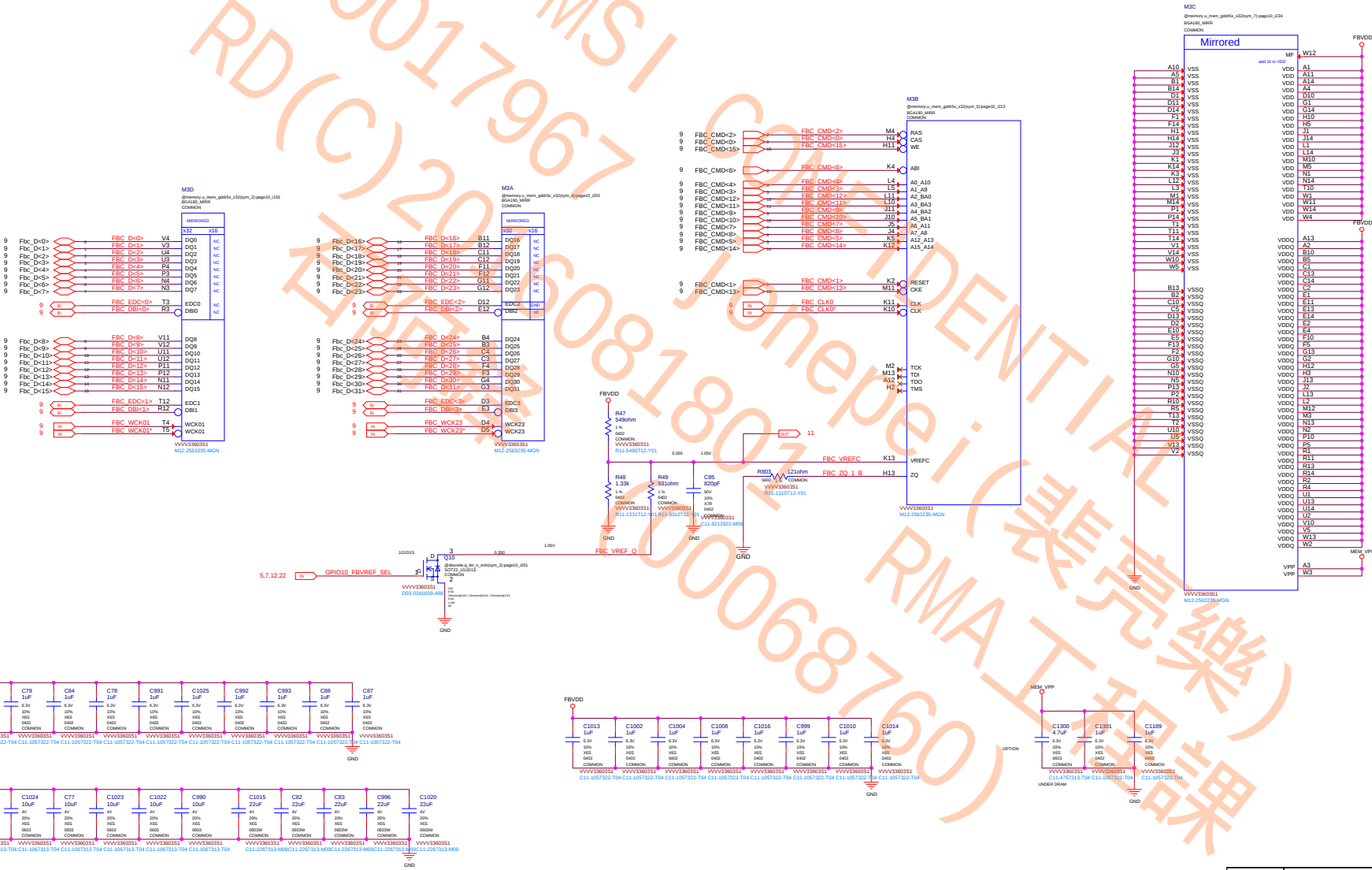


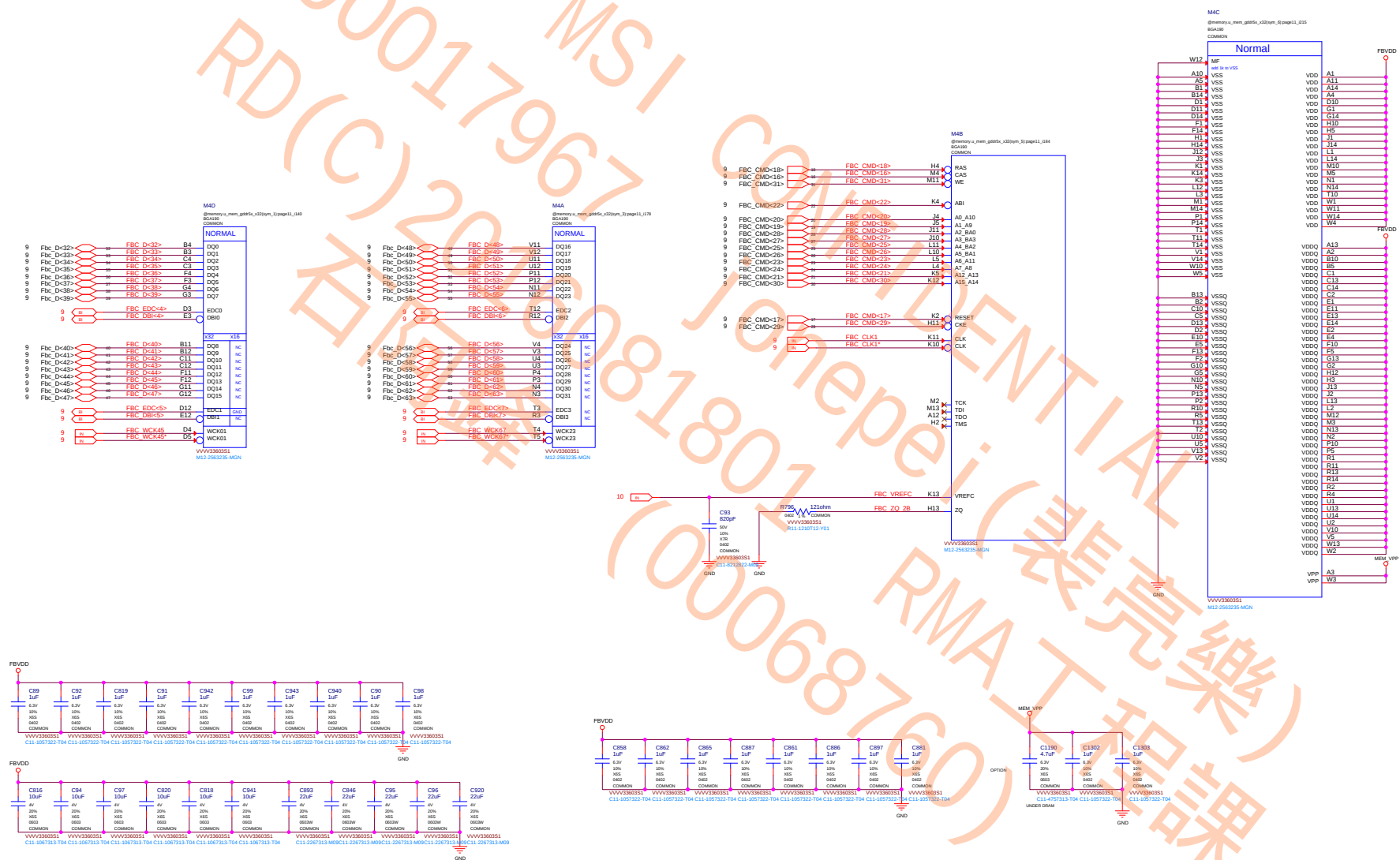


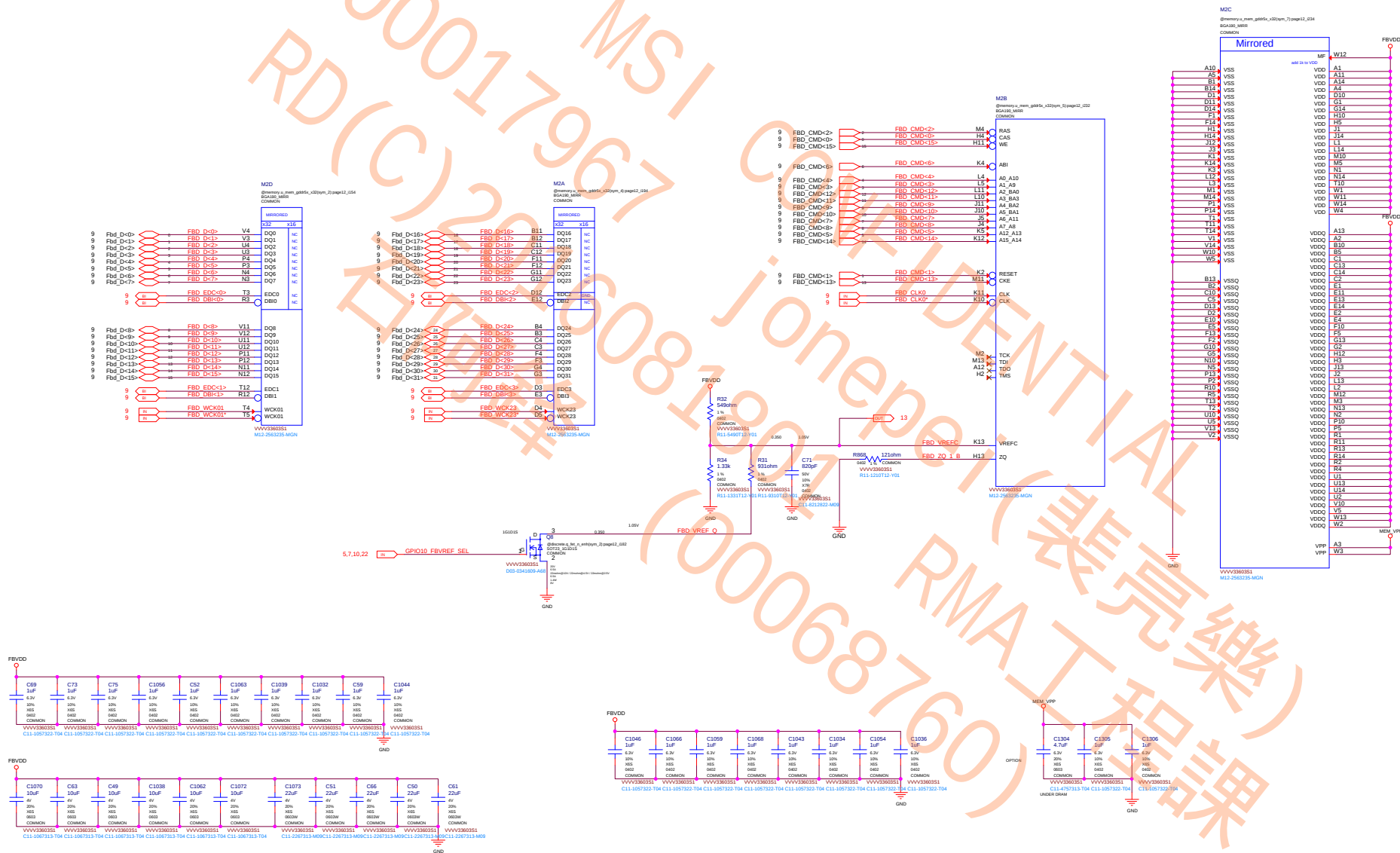


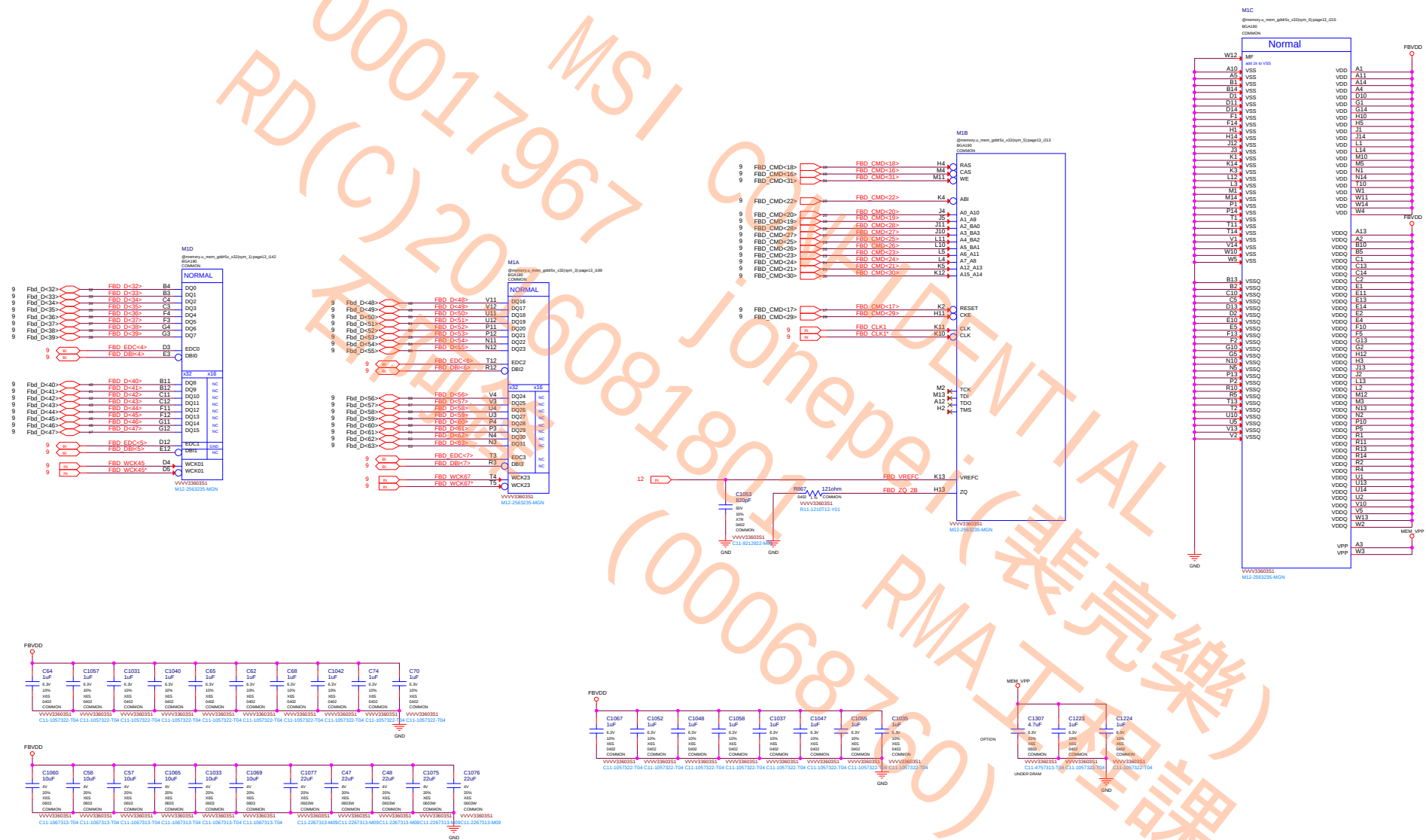




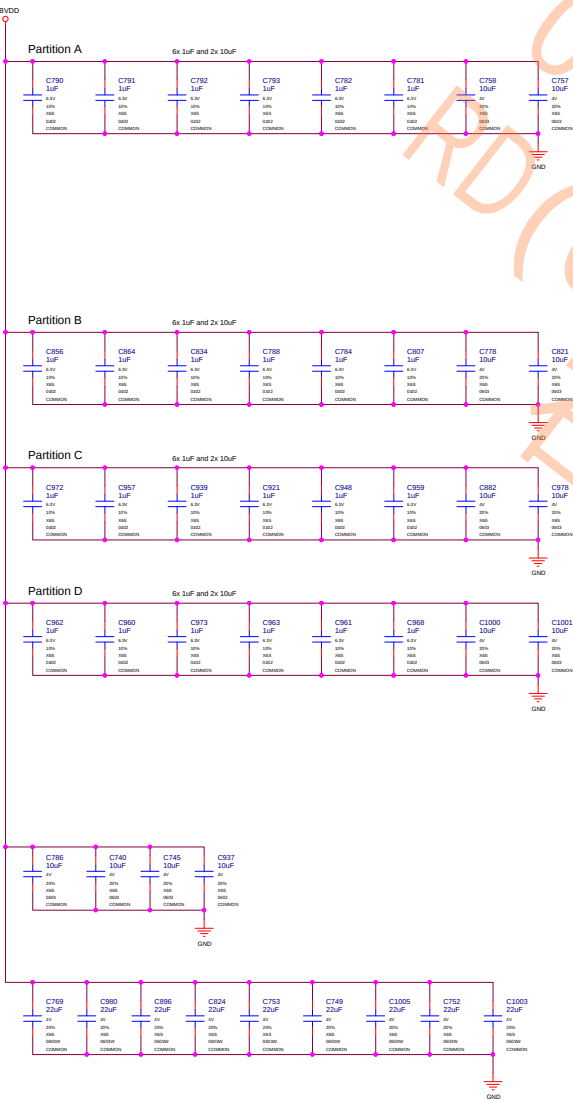




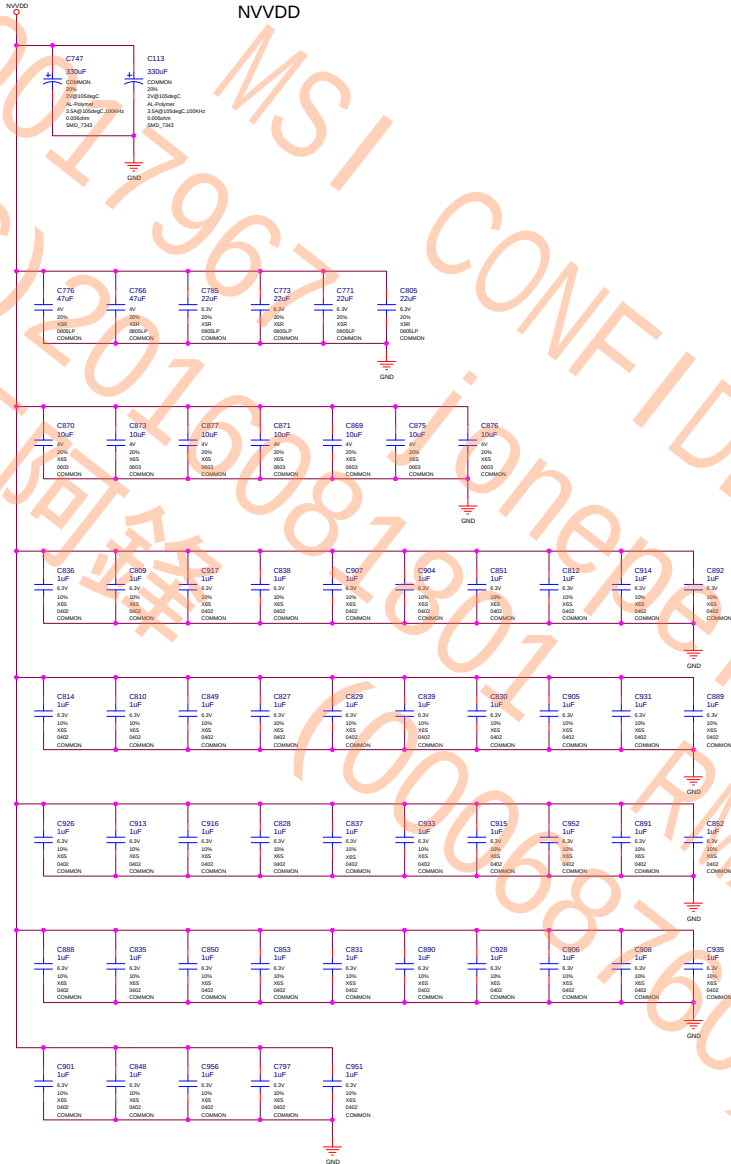




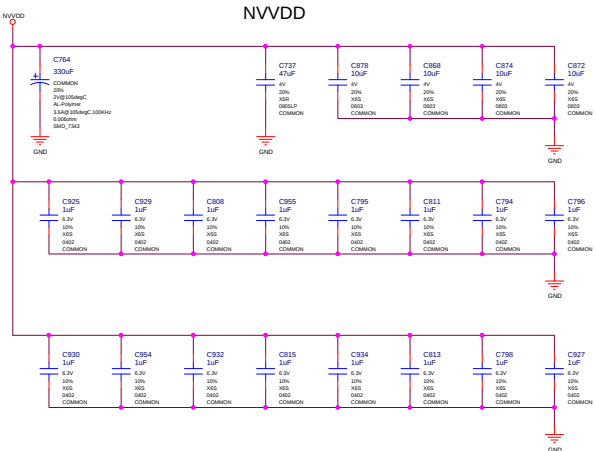
FBVDD



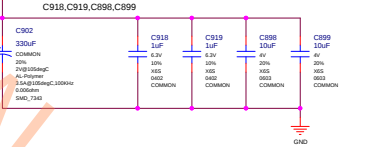
NVVD



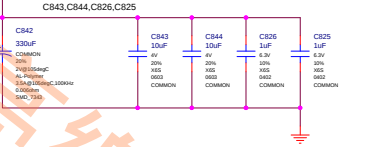
NVVD



STUFF C902 OR

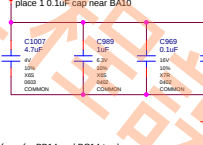


STUFF C842 OR

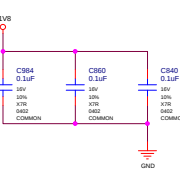


1V8_AON

place 10.1uF cap near BA10

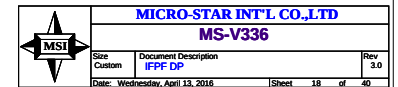
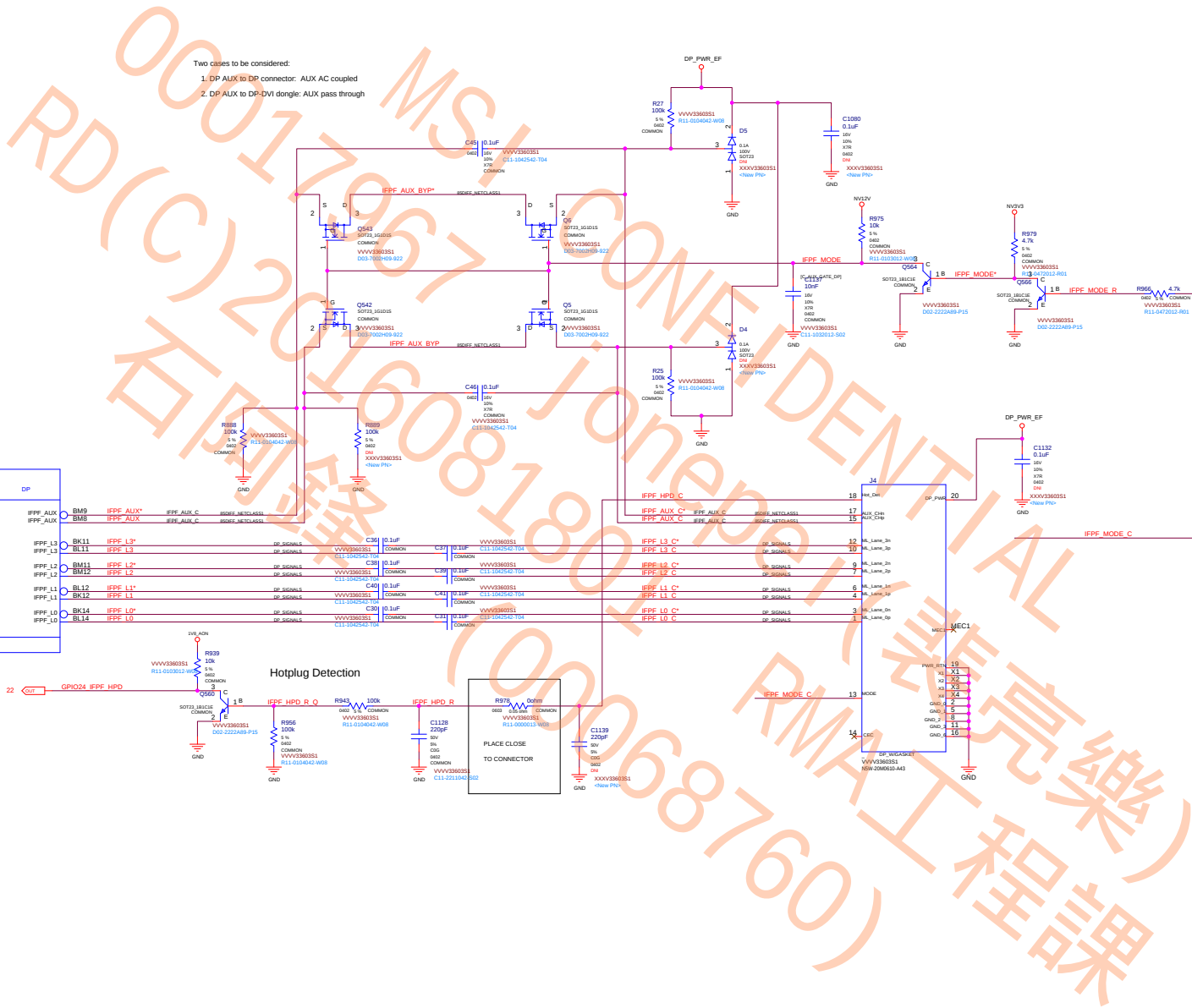


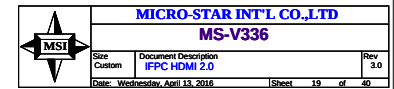
VDD18

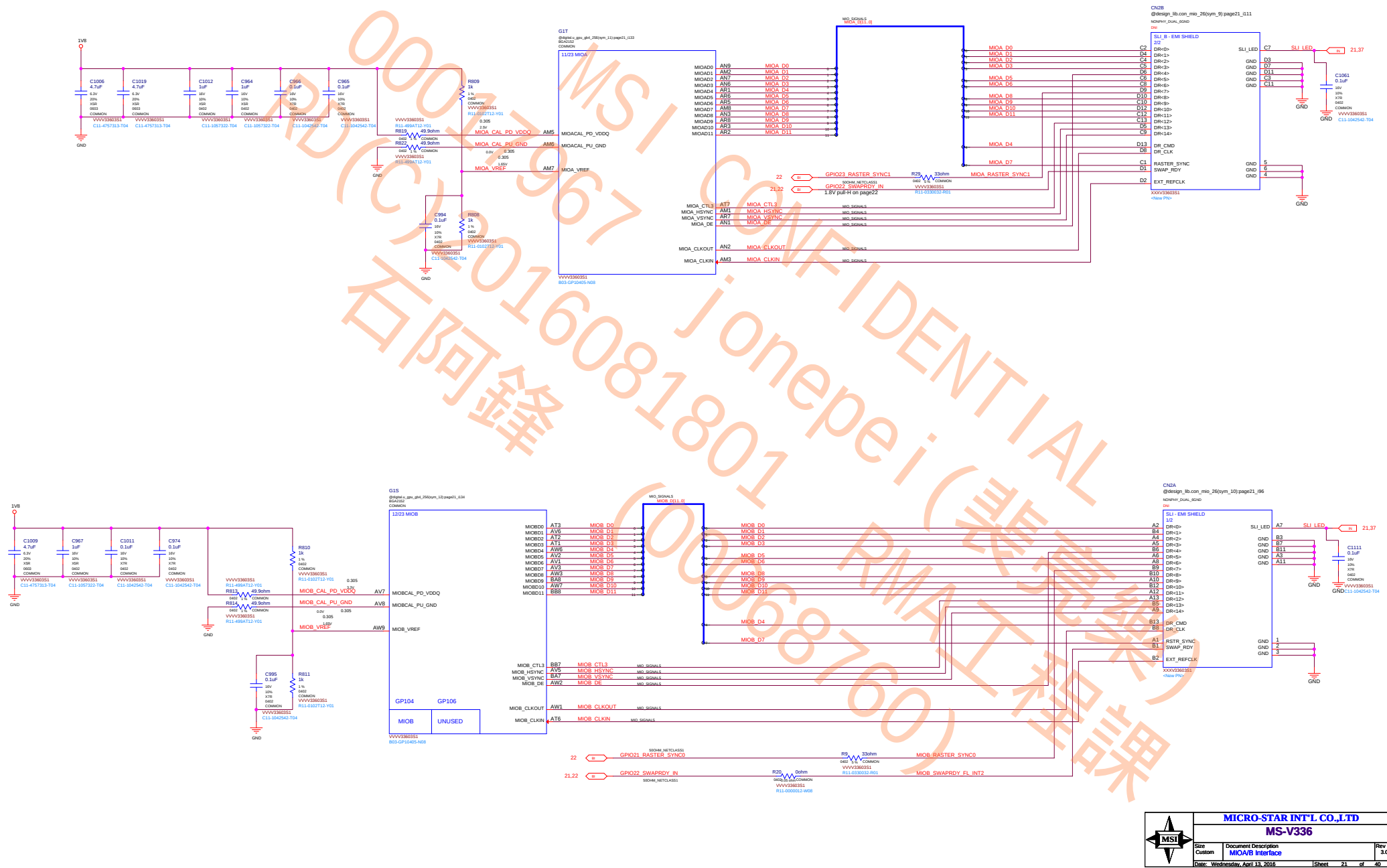


place 10.1uF cap for BB14 and BC14 to share

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through







STRAP2	STRAP1	STRAP0	RAMCFG[4:0]			
L	L	L	00000			
L	H	L	00010			
L	H	H	00011			
H	H	L	00110			
H	H	H	00111			
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0] 1:ENABLE 0:DISABLE			
L	L	L	1111 DEFAULT SOR0/1/2/3 ENABLE			
L	L	H	1110			
L	H	L	1101			
L	H	H	1100			
H	L	L	1011			
H	L	H	1010			
H	H	L	1001			
H	H	H	1000			
L	L	M	0111			
L	M	L	0110			
L	M	H	0101			
L	H	M	0100			
H	L	M	0011			
H	M	L	0010			
H	M	H	0001			
H	H	M	0000			

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0
L	L	L	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

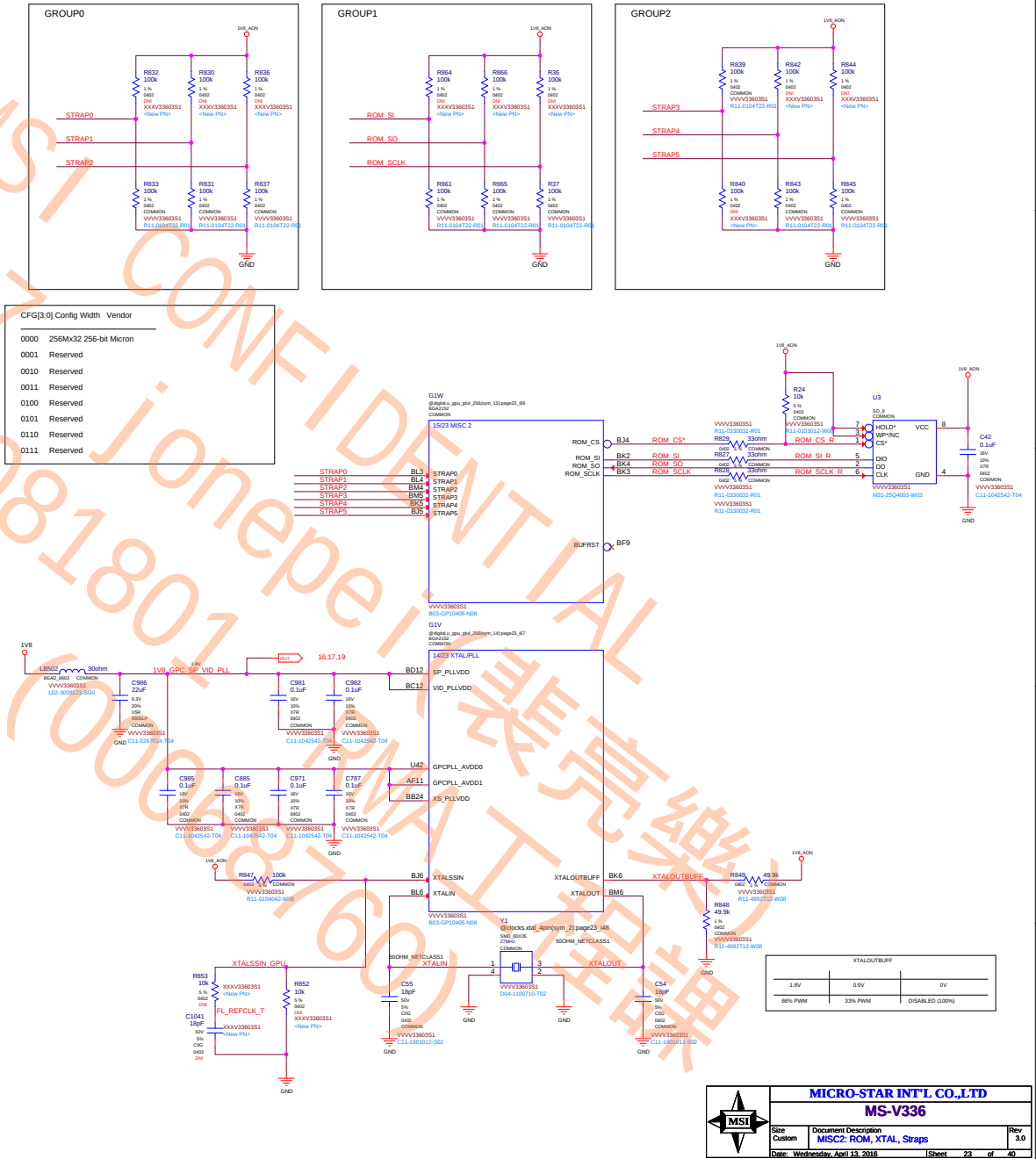
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

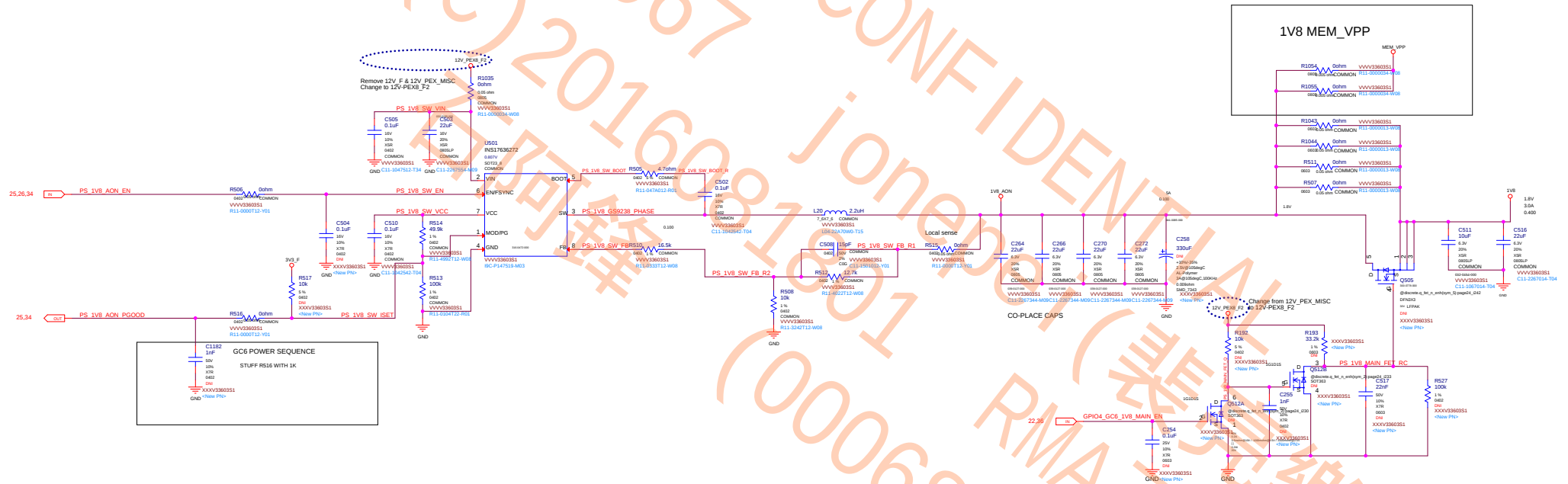
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

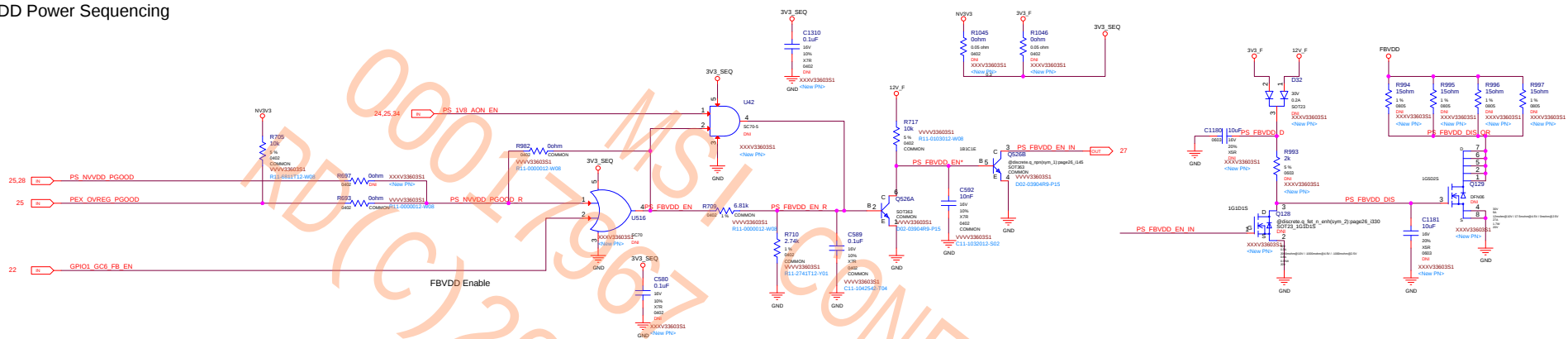
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

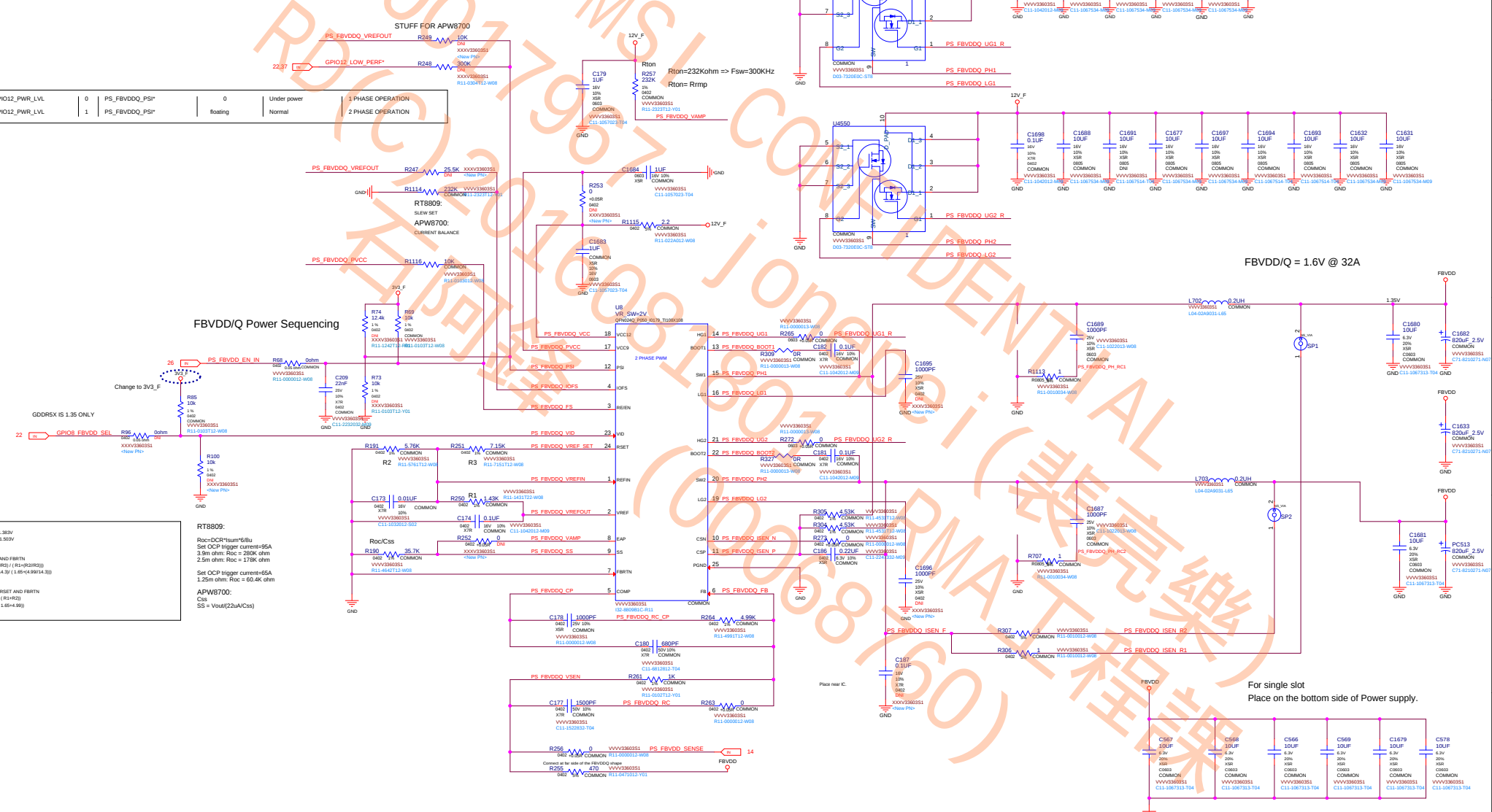
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

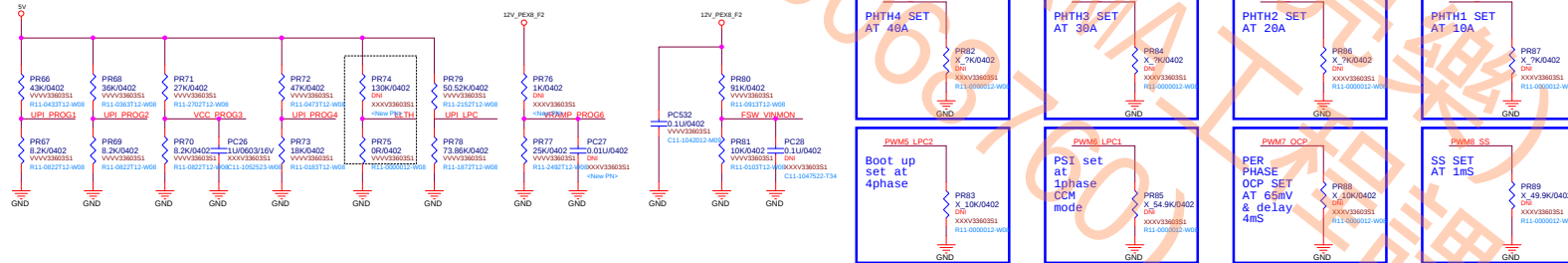
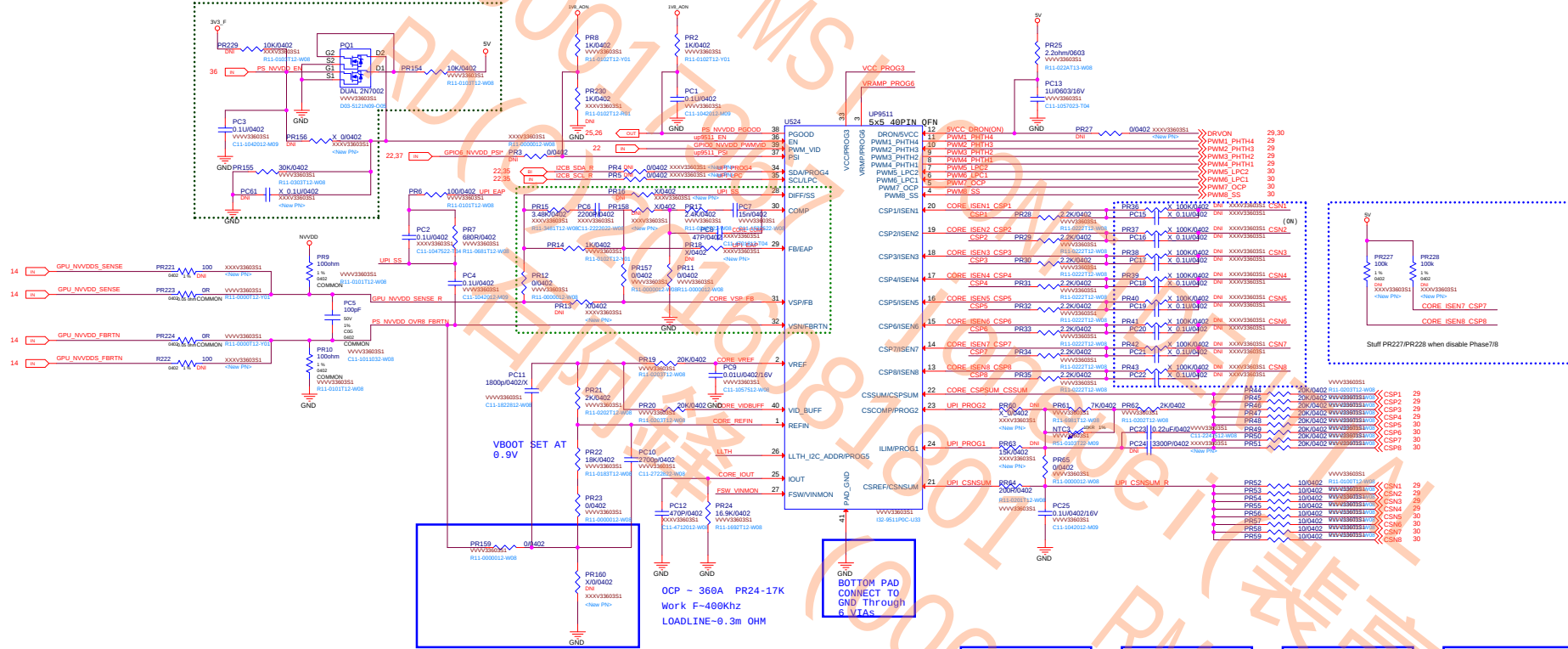
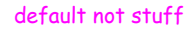
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

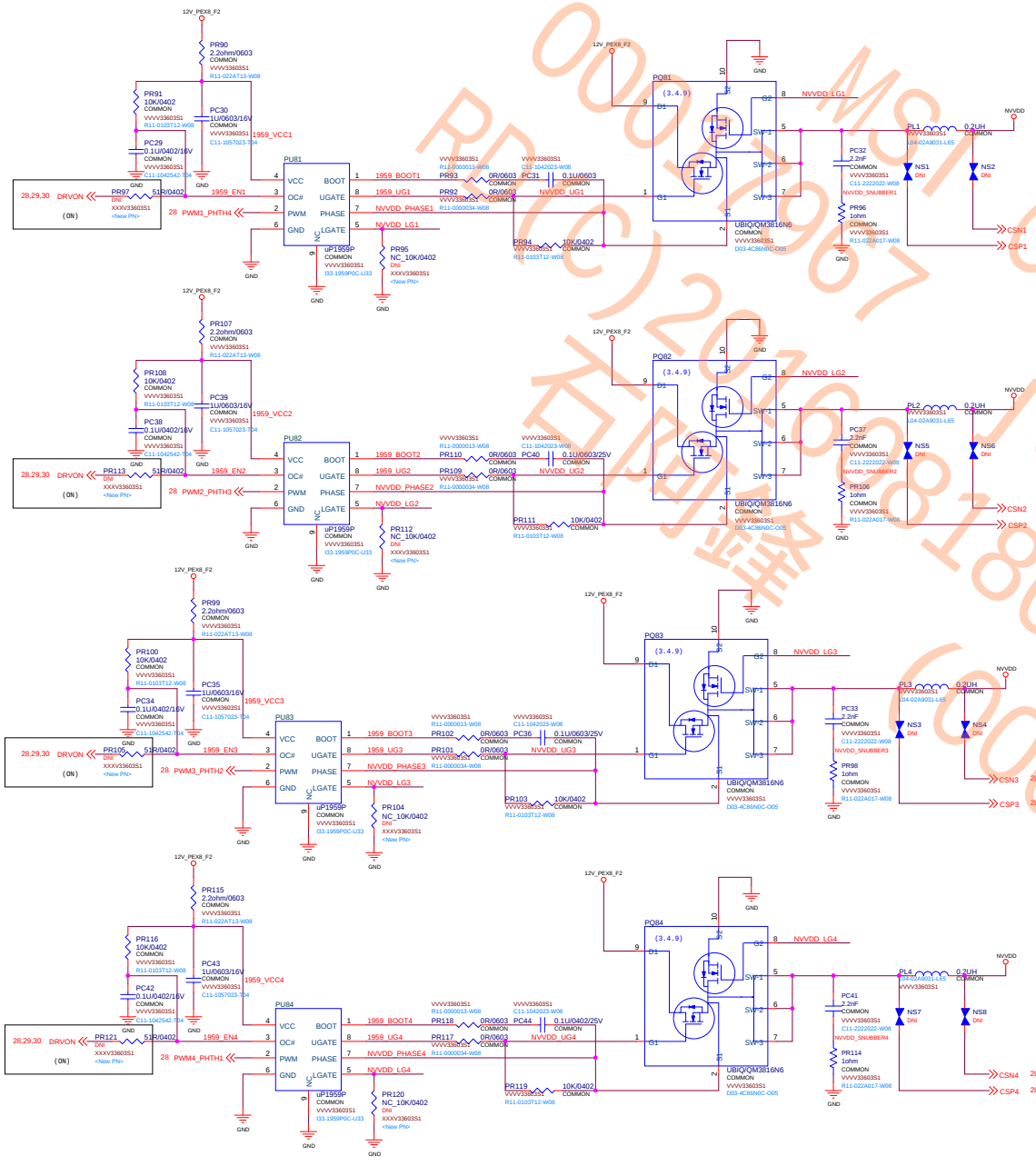




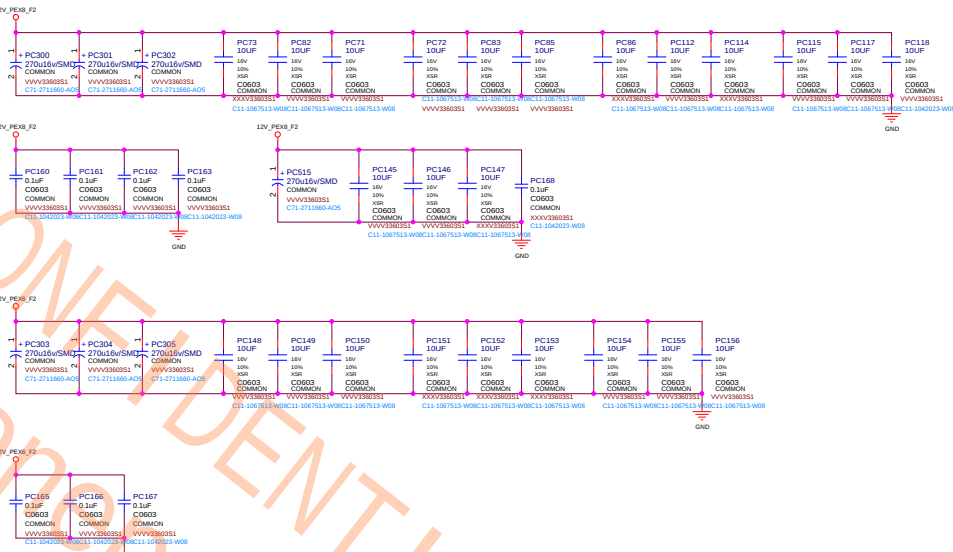




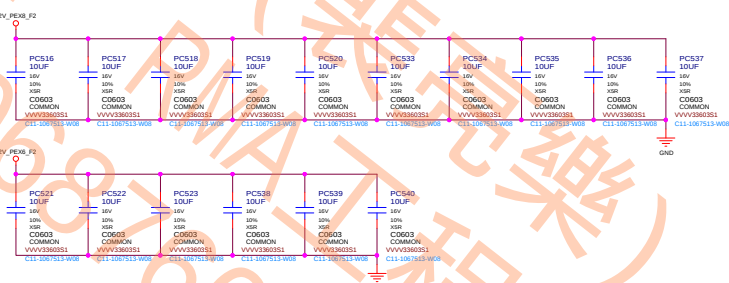


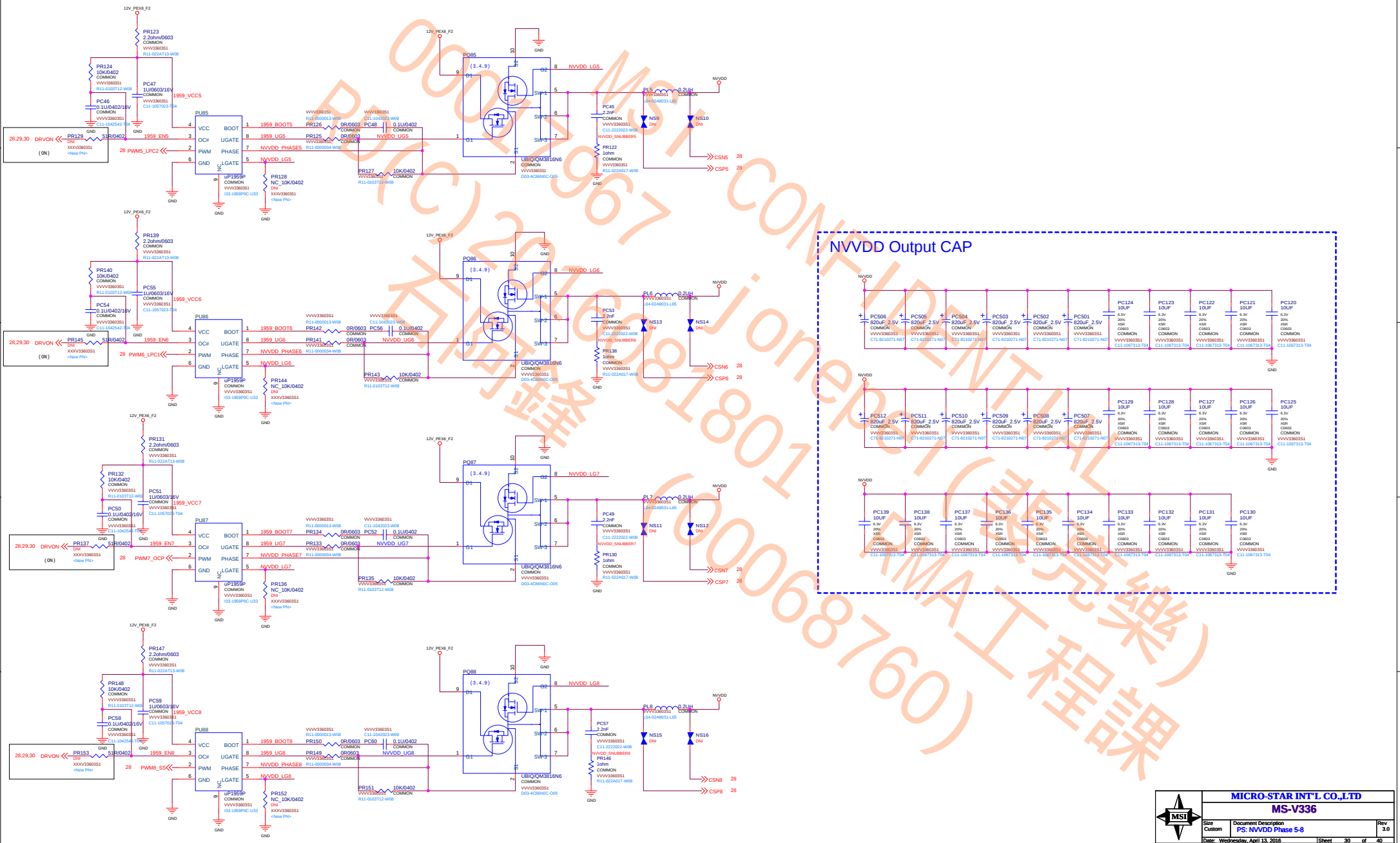


EXT_12V Input CAP



EXT_12V Input CAP(Backup)

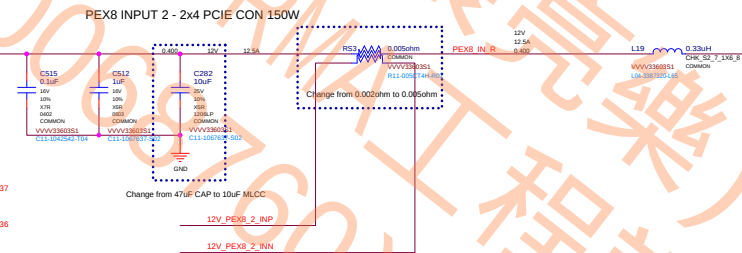
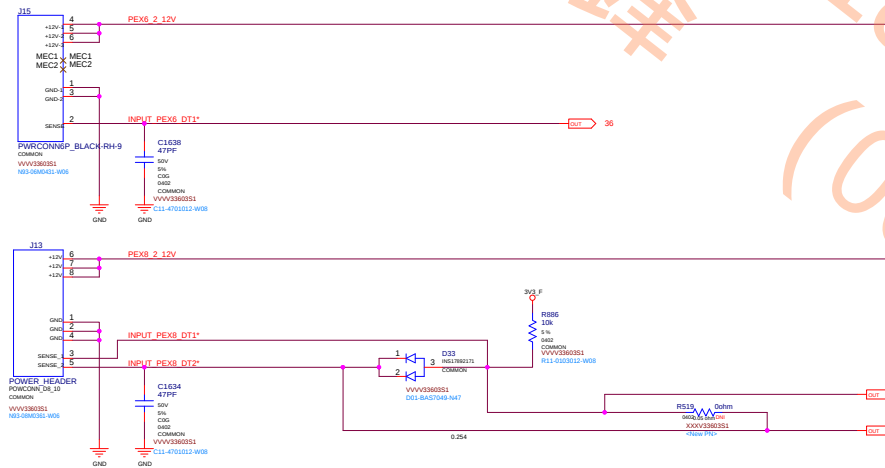
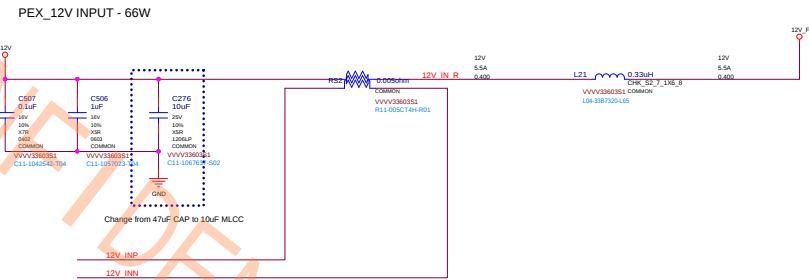
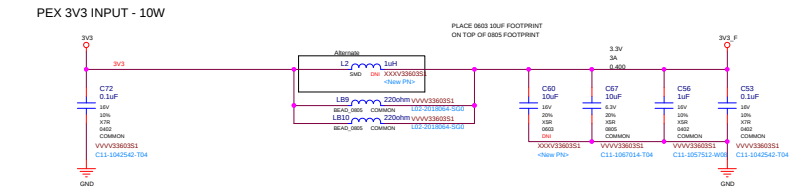
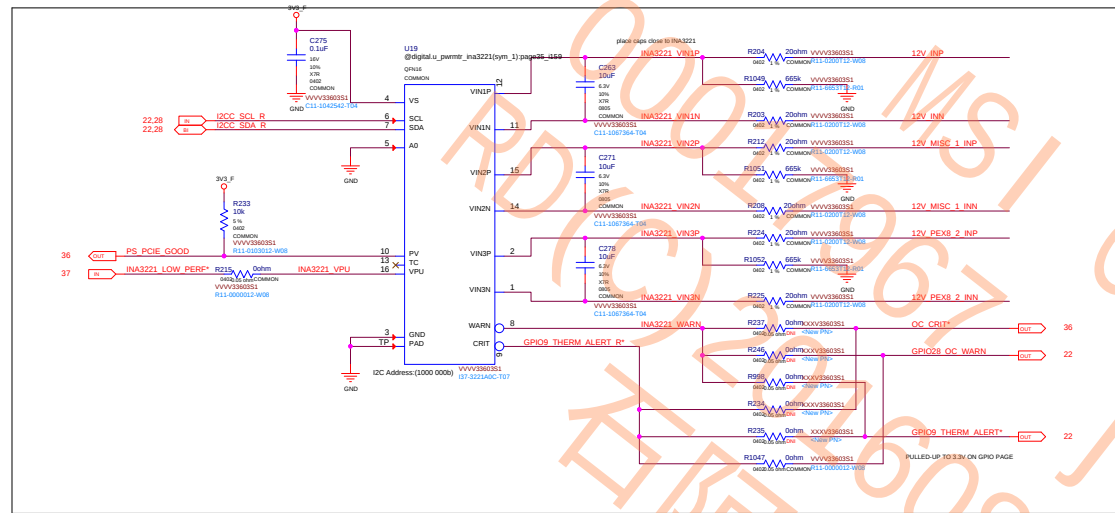




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RD(C)2016081801 RMA工程課
石阿鋒 (00068760)

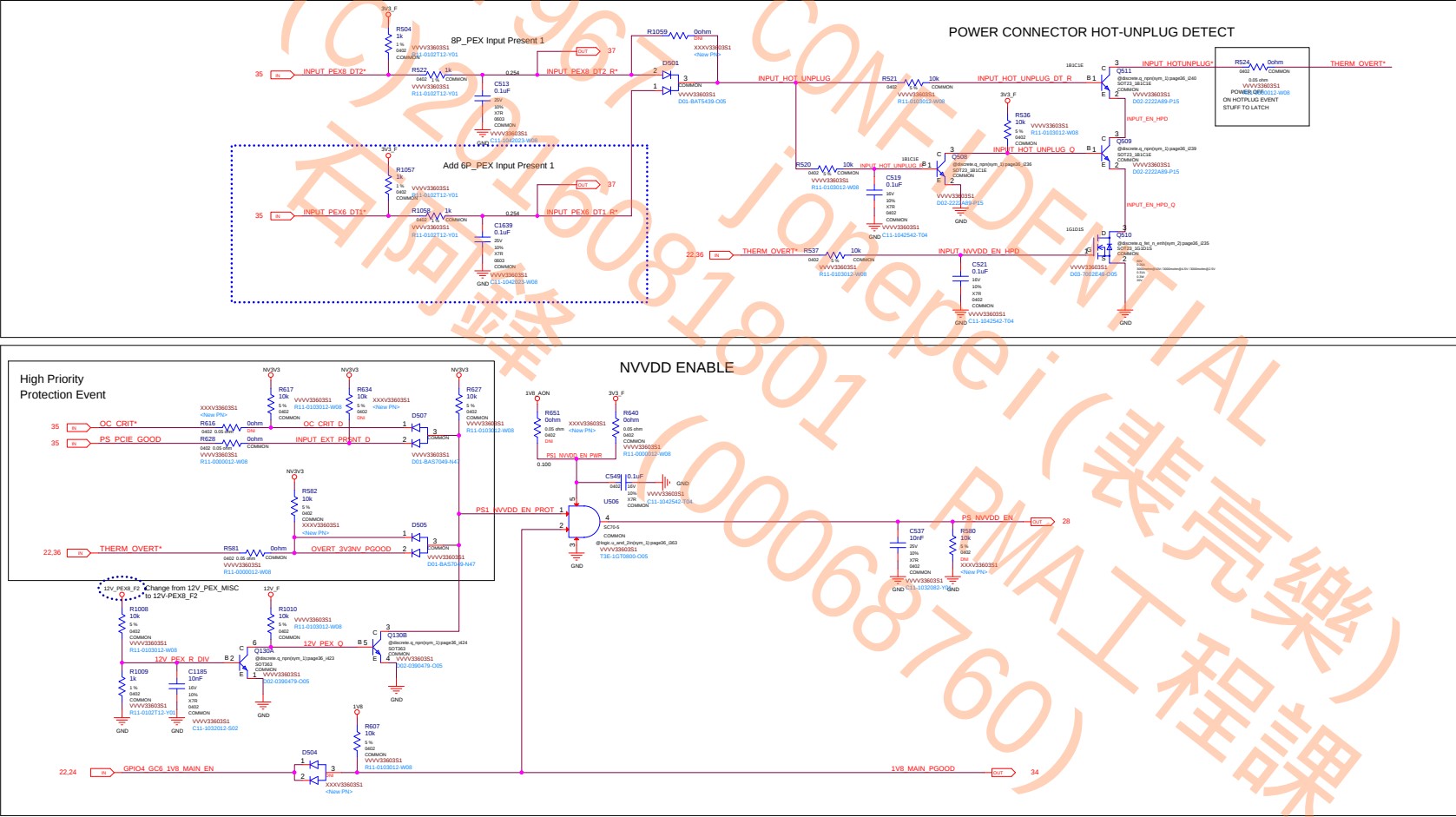
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00017967 jonepei (裴亮樂)
RD(C)2016081801 RMA工程課
石阿鋒 (00068760)

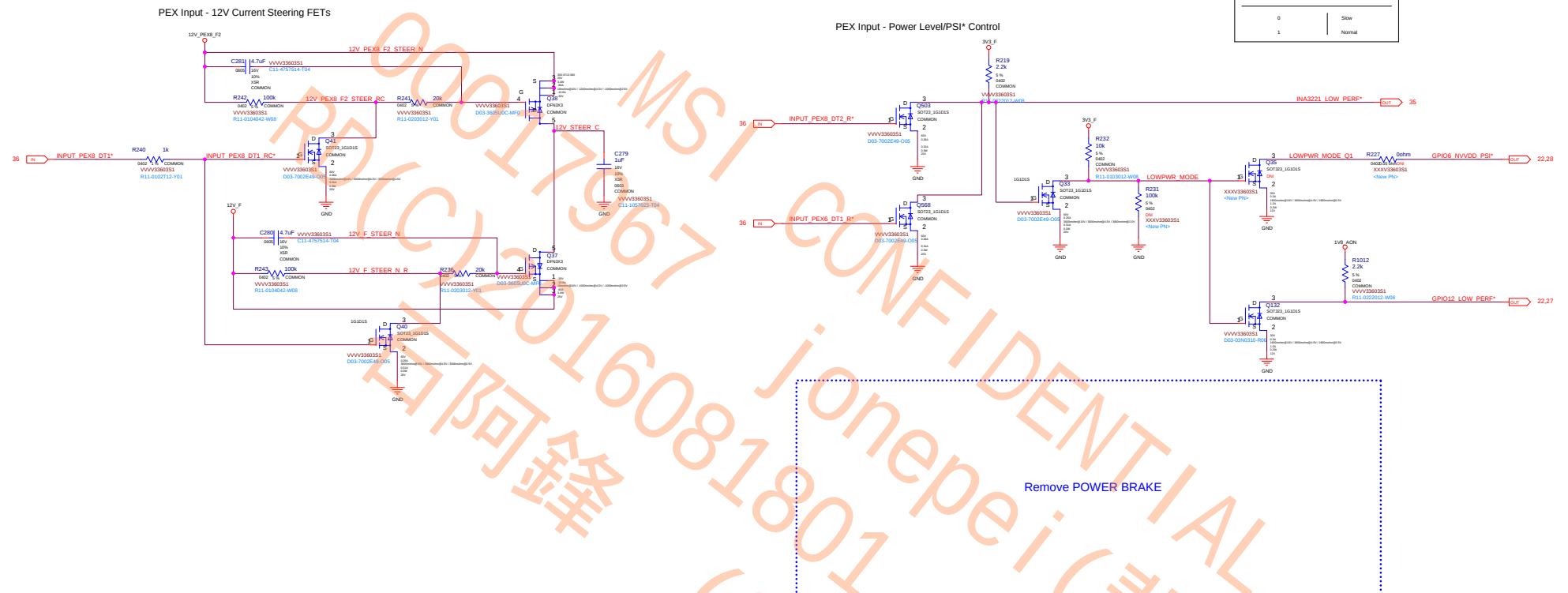
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石阿鋒 (00068760)



STUFF FOR 8-PIN CONNECTOR
OR REVERSE CPU 8-PIN CONNECTOR



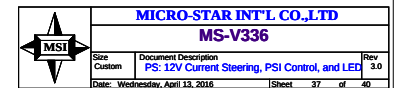
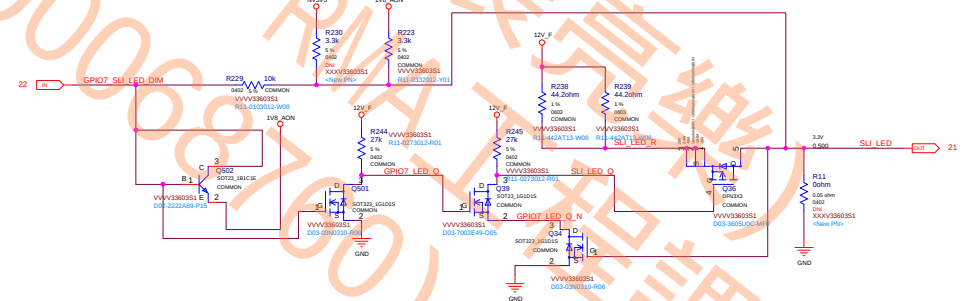




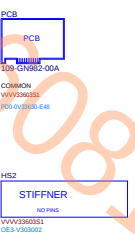
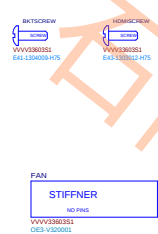
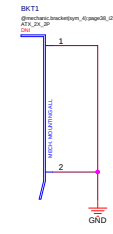
LED HEADER
(COMMON)

Remove Logo LED

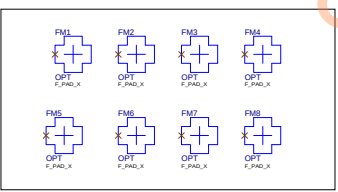
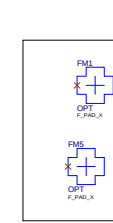
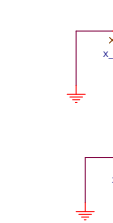
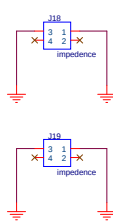
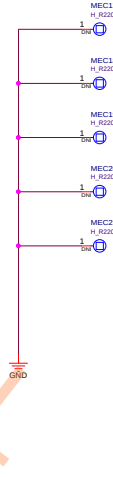
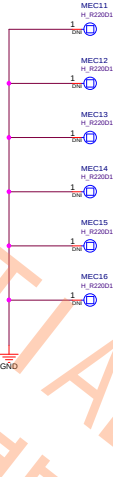
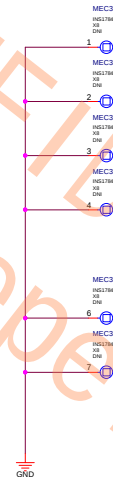
SLI LED (GEFORCE ONLY)



Brackets:



GPU Stiffner



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Date: Saturday, April 08, 2016		Sheet 40 of 40