PG413 A00

GP104 - 8GB GDDR5X, 256b, 256Mx32
Tall DVI-D + DP + DP + DP/HDMI + DP

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14	Remove FBVDD_SENSE_RTN resistor
17	Change DP Library/Footprint
18	Change DP Library/Footprint
19	Change HDMI Library/Footprint
	Remove co-lay DP
20	Change DP Library/Footprint
21	Remove MIOA/B FRAME LOCK circuit
22	Remove Thermal IC
	Remove GPIO19_STEREO Circuit
	Remove Unused GPIO
24	Remove co-lay APW8713AQBI-TRG,BUCK
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30	Copy driver/MOS circuit from V323-0b
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36	Add 6pin POWER CONNECTOR HOT-UNPLUG DETECT
37	Add 6pin PEX Input - Power Level/PSI* Control
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V336-3.1	Change List
39	ENE3574 VCC power change to 3V3_F

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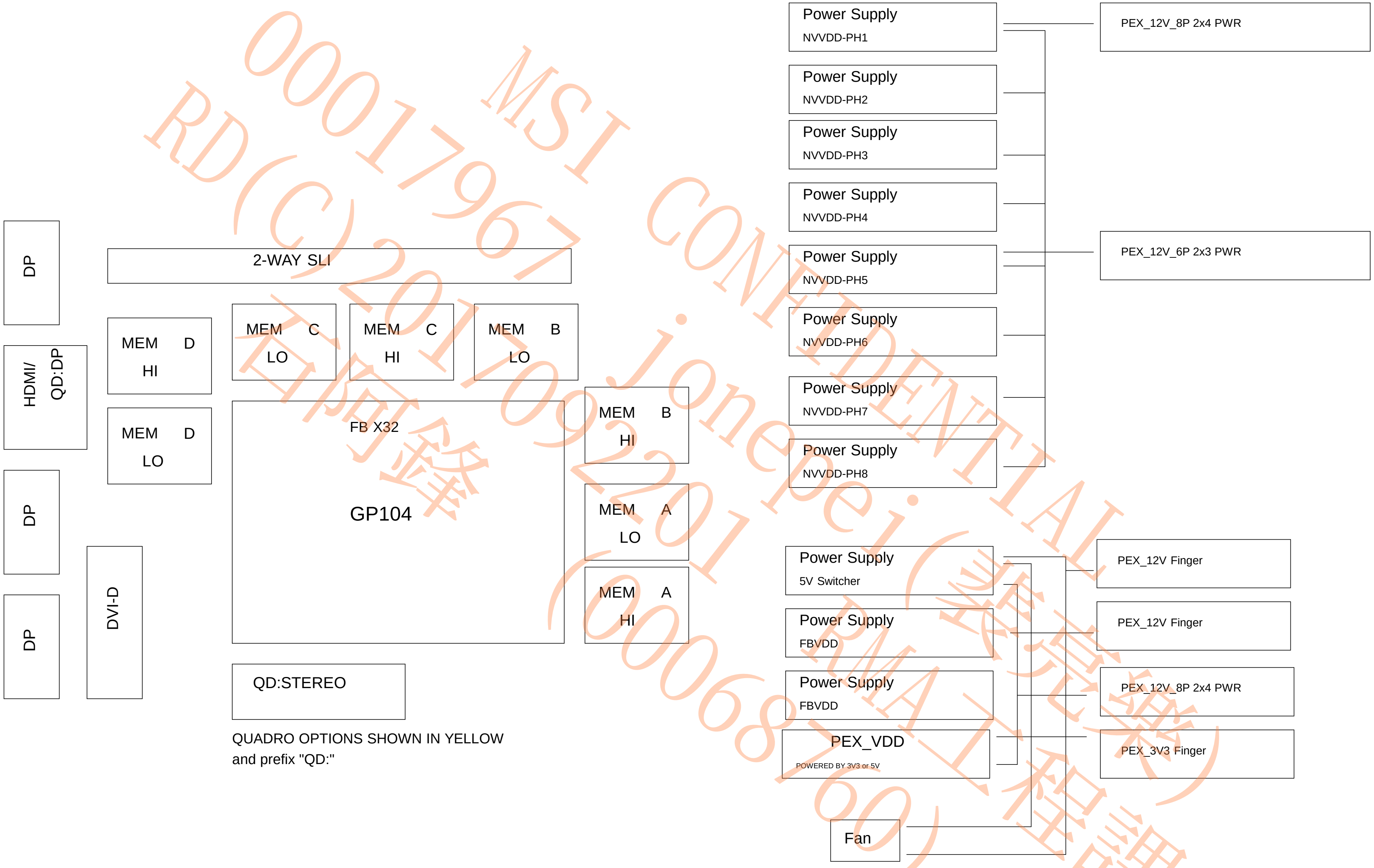
Page2: Block Diagram



Power Supply
NVVDD-PH1
Power Supply
NVVDD-PH2
Power Supply
NVVDD-PH3
Power Supply
NVVDD-PH4
Power Supply
NVVDD-PH5
Power Supply
NVVDD-PH6
Power Supply
NVVDD-PH7
Power Supply
NVVDD-PH8
PEX_12V_8P 2x4 PWR
PEX_12V_6P 2x3 PWR
DP
2-WAY SLI
HDMI/
QD:DP
MEM D
HI
MEM D
LO
MEM C
LO
MEM C
HI
MEM B
LO
MEM B
HI
MEM A
LO
MEM A
HI
FB X32
GP104
DP
DP
DVI-D
QD:STEREO
Power Supply
5V Switcher
Power Supply
FBVDD
Power Supply
FBVDD
PEX_VDD
POWERED BY 3V3 or 5V
Fan
PEX_12V Finger
PEX_12V Finger
PEX_12V_8P 2x4 PWR
PEX_3V3 Finger

QUADRO OPTIONS SHOWN IN YELLOW
and prefix "QD:"

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Page3: PCI Express

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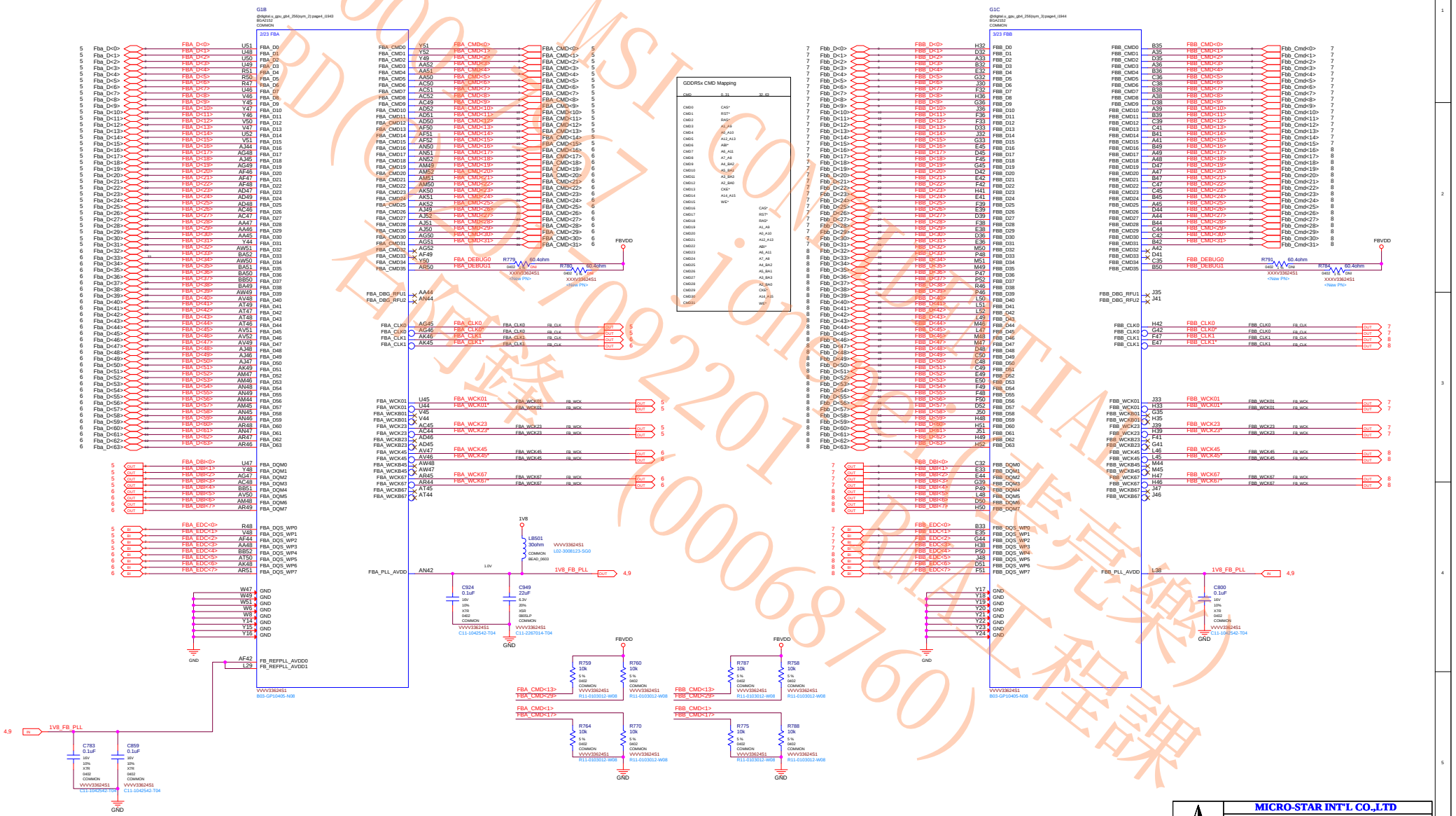
Page4: MEMORY: GPU Partition A/B



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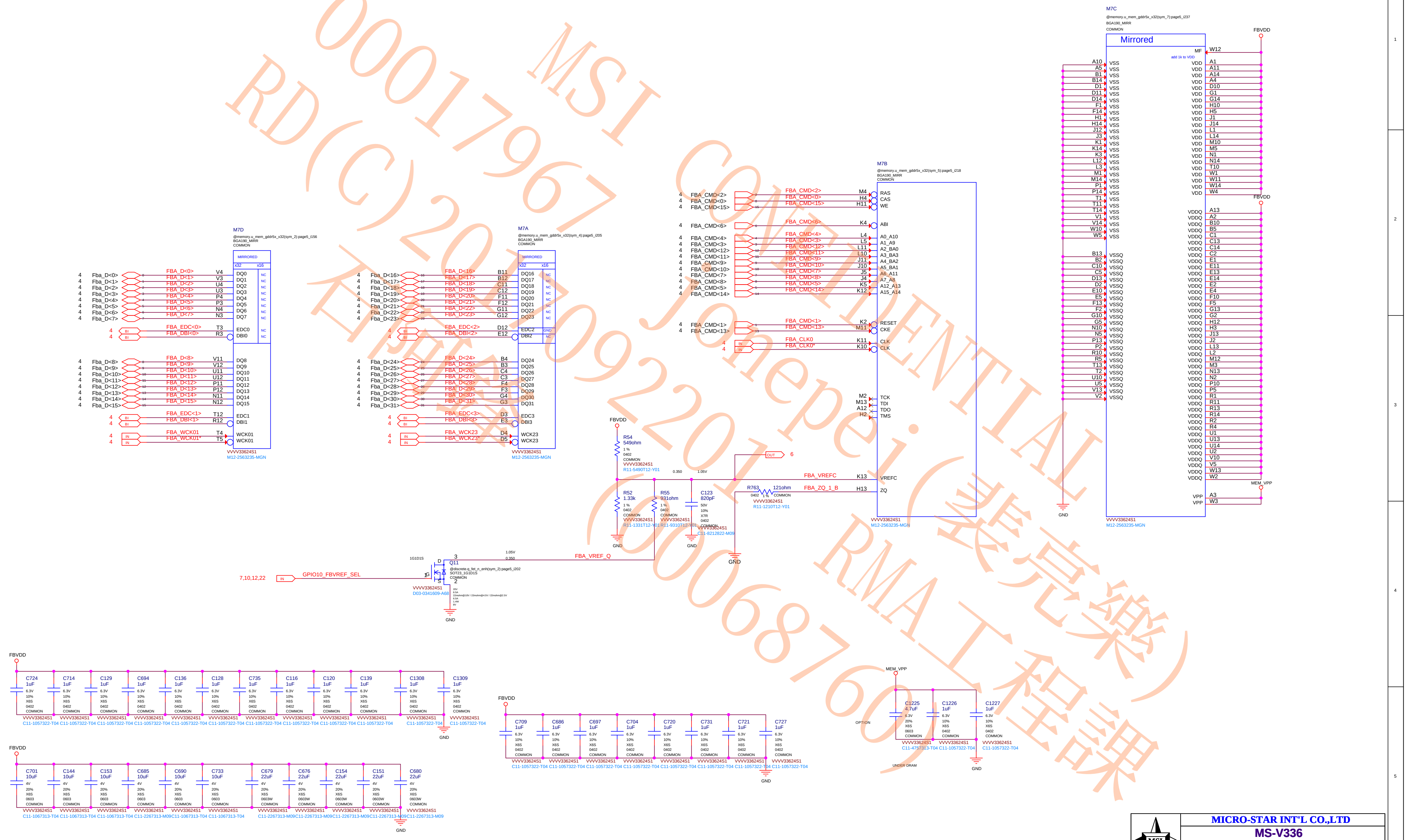
Page5: MEMORY: FBA Partition 31..0



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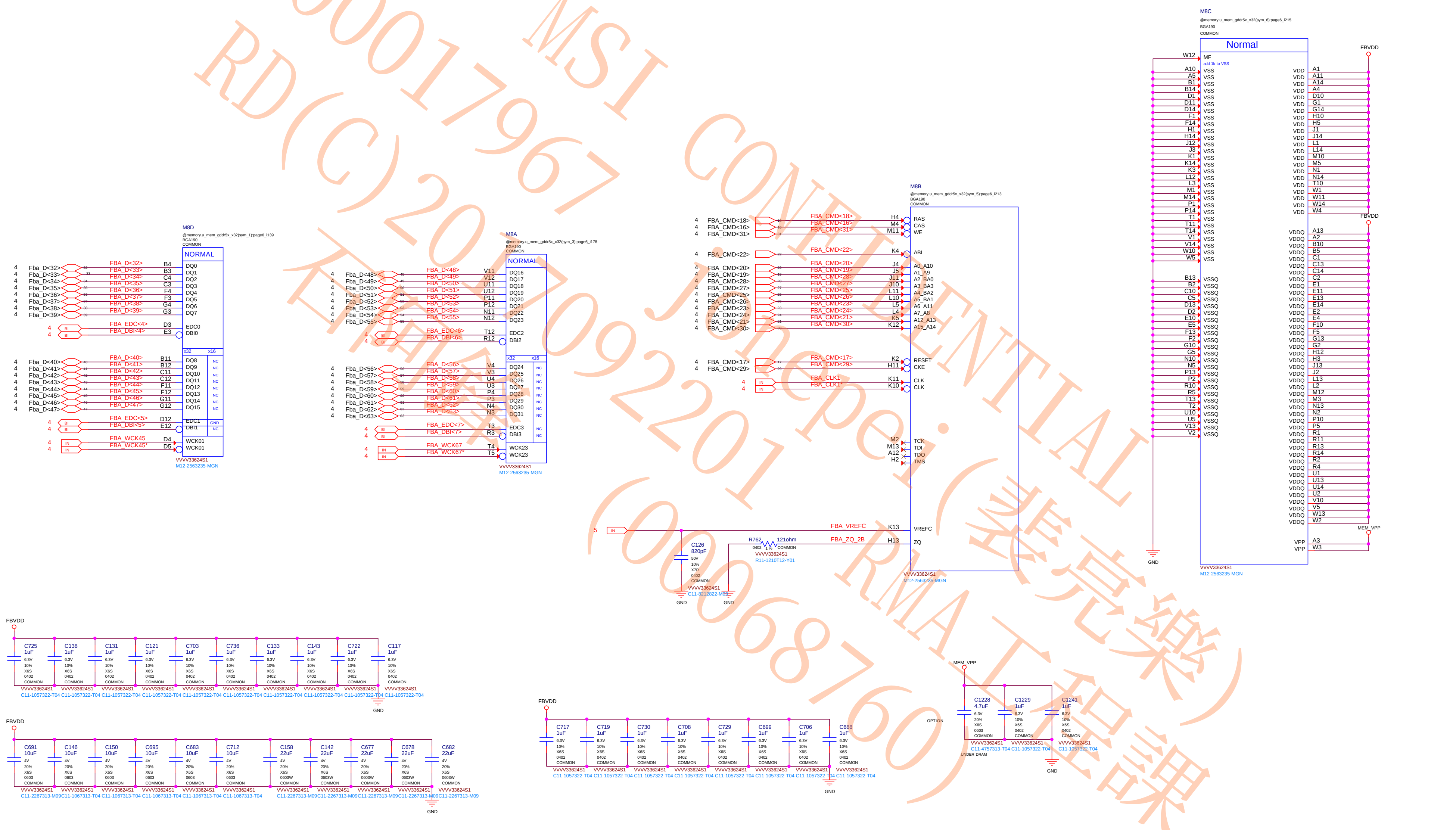
Page6: MEMORY: FBA Partition 63..32



M8D
NORMAL
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7
EDC0 DBI0
DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15
EDC1 DBI1
WCK01 WCK01
Fba_D<32> Fba_D<33> Fba_D<34> Fba_D<35> Fba_D<36> Fba_D<37> Fba_D<38> Fba_D<39>
Fba_D<40> Fba_D<41> Fba_D<42> Fba_D<43> Fba_D<44> Fba_D<45> Fba_D<46> Fba_D<47>
FBA_EDC<4> FBA_DBI<4> FBA_EDC<5> FBA_DBI<5> FBA_WCK45 FBA_WCK45*
M12-2563235-MGN
M8A
NORMAL
DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23
EDC2 DBI2
DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31
EDC3 DBI3
WCK23 WCK23
Fba_D<48> Fba_D<49> Fba_D<50> Fba_D<51> Fba_D<52> Fba_D<53> Fba_D<54> Fba_D<55>
Fba_D<56> Fba_D<57> Fba_D<58> Fba_D<59> Fba_D<60> Fba_D<61> Fba_D<62> Fba_D<63>
FBA_EDC<6> FBA_DBI<6> FBA_EDC<7> FBA_DBI<7> FBA_WCK67 FBA_WCK67*
M12-2563235-MGN
M8B
RAS CAS WE ABI
A0_A10 A1_A9 A2_BA0 A3_BA3 A4_BA2 A5_BA1 A6_A11 A7_A8 A12_A13 A15_A14
RESET CKE CLK CLK
TCK TDI TDO TMS
VREFC ZQ
FBA_CMD<18> FBA_CMD<16> FBA_CMD<31> FBA_CMD<22>
FBA_CMD<20> FBA_CMD<19> FBA_CMD<28> FBA_CMD<27> FBA_CMD<25> FBA_CMD<26> FBA_CMD<23> FBA_CMD<24> FBA_CMD<21> FBA_CMD<30>
FBA_CMD<17> FBA_CMD<29>
FBA_CLK1 FBA_CLK1*
FBA_VREFC FBA_ZQ_2B
R762 121ohm
C126 820pF
M12-2563235-MGN
M8C
Normal
MF
VSS VDD VSSQ VDDQ VPP
FBVDD MEM_VPP GND
M12-2563235-MGN
C725 C138 C131 C121 C703 C736 C133 C143 C722 C117 1uF
C691 C146 C150 C695 C683 C712 10uF
C158 C142 C677 C678 C682 22uF
C717 C719 C730 C708 C729 C699 C706 C688 1uF
C1228 4.7uF C1229 1uF C1241 1uF

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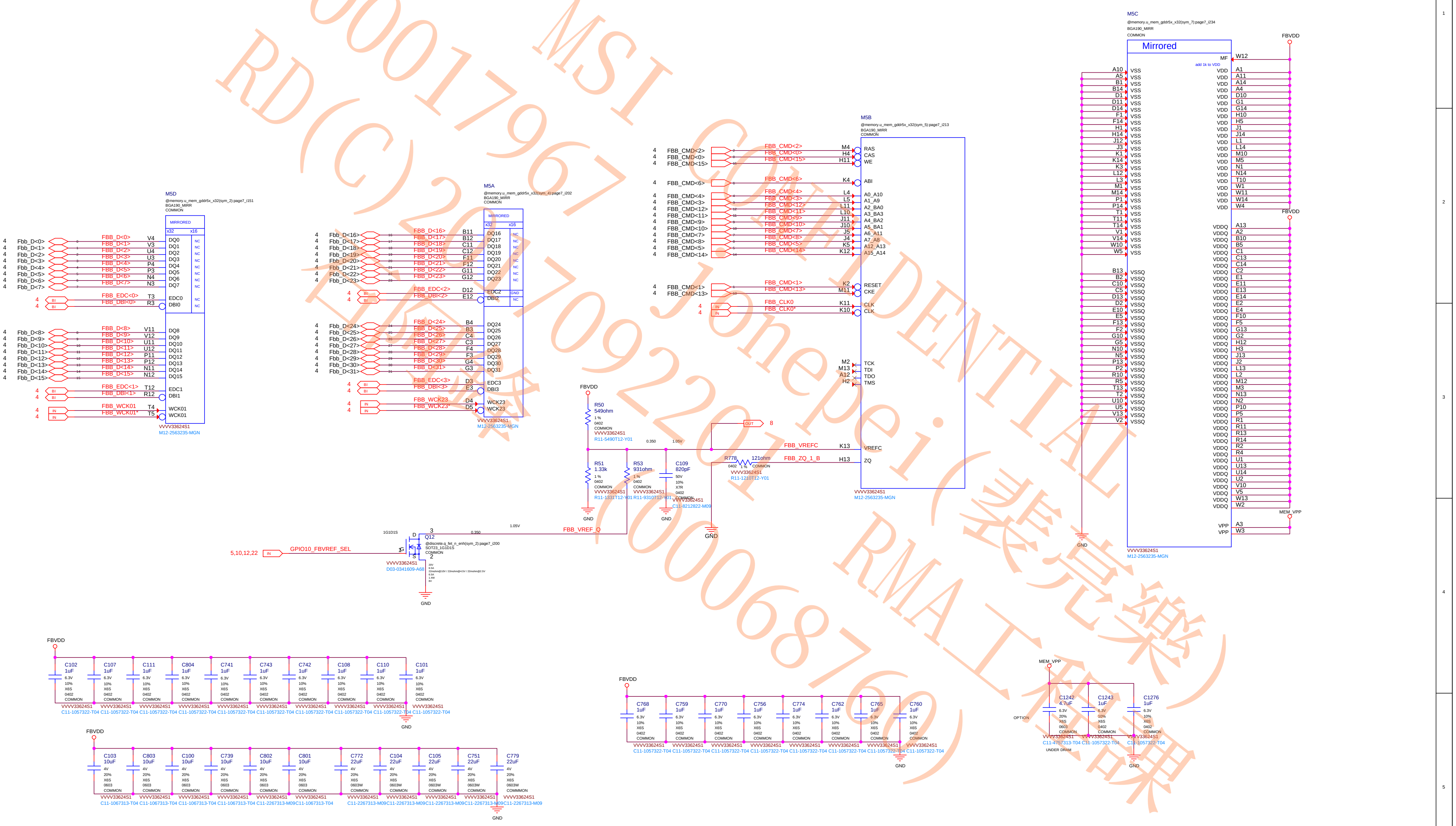
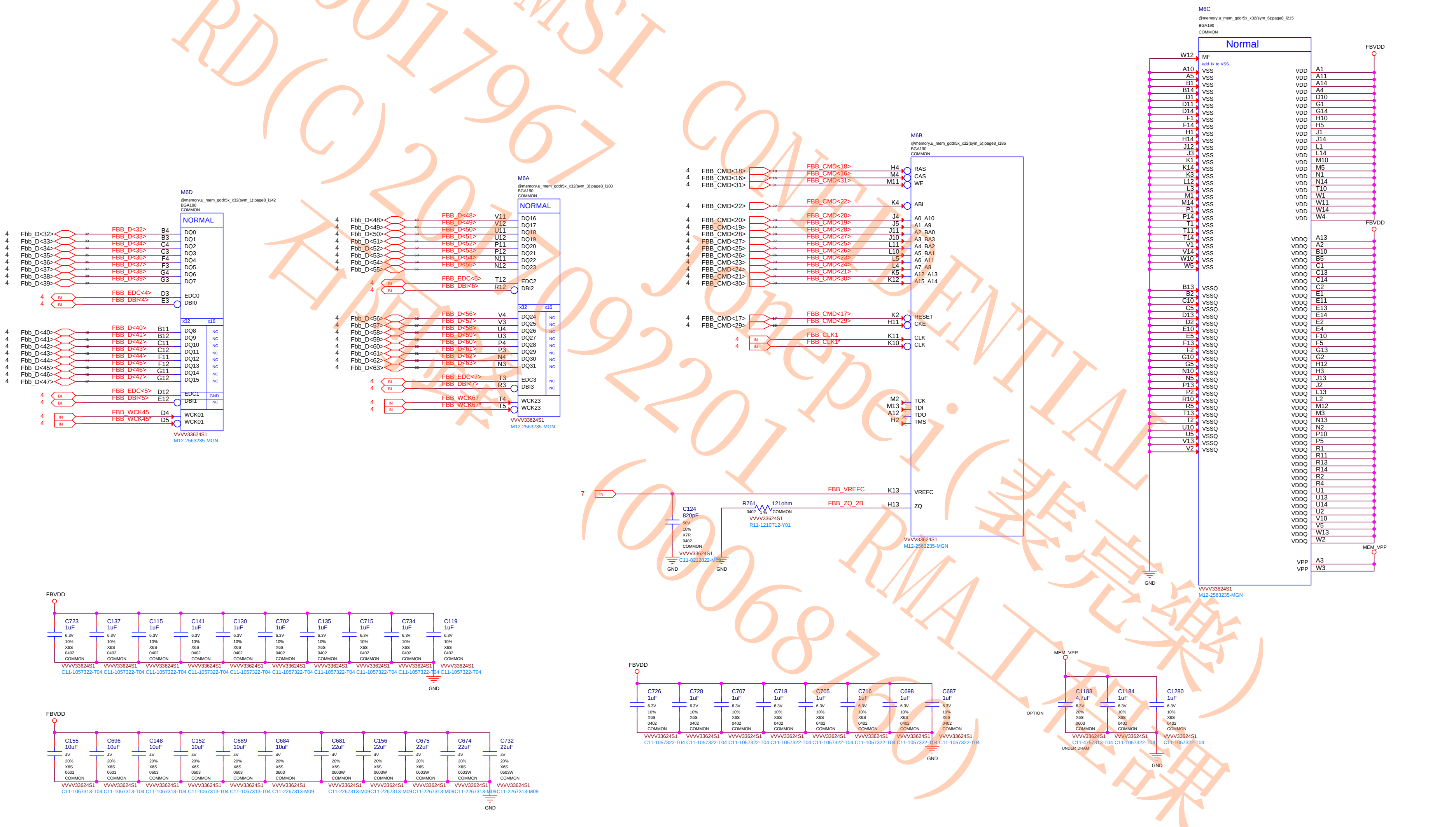
Page7: MEMORY: FBB Partition 31..0



Page8: MEMORY: FBB Partition 63..32



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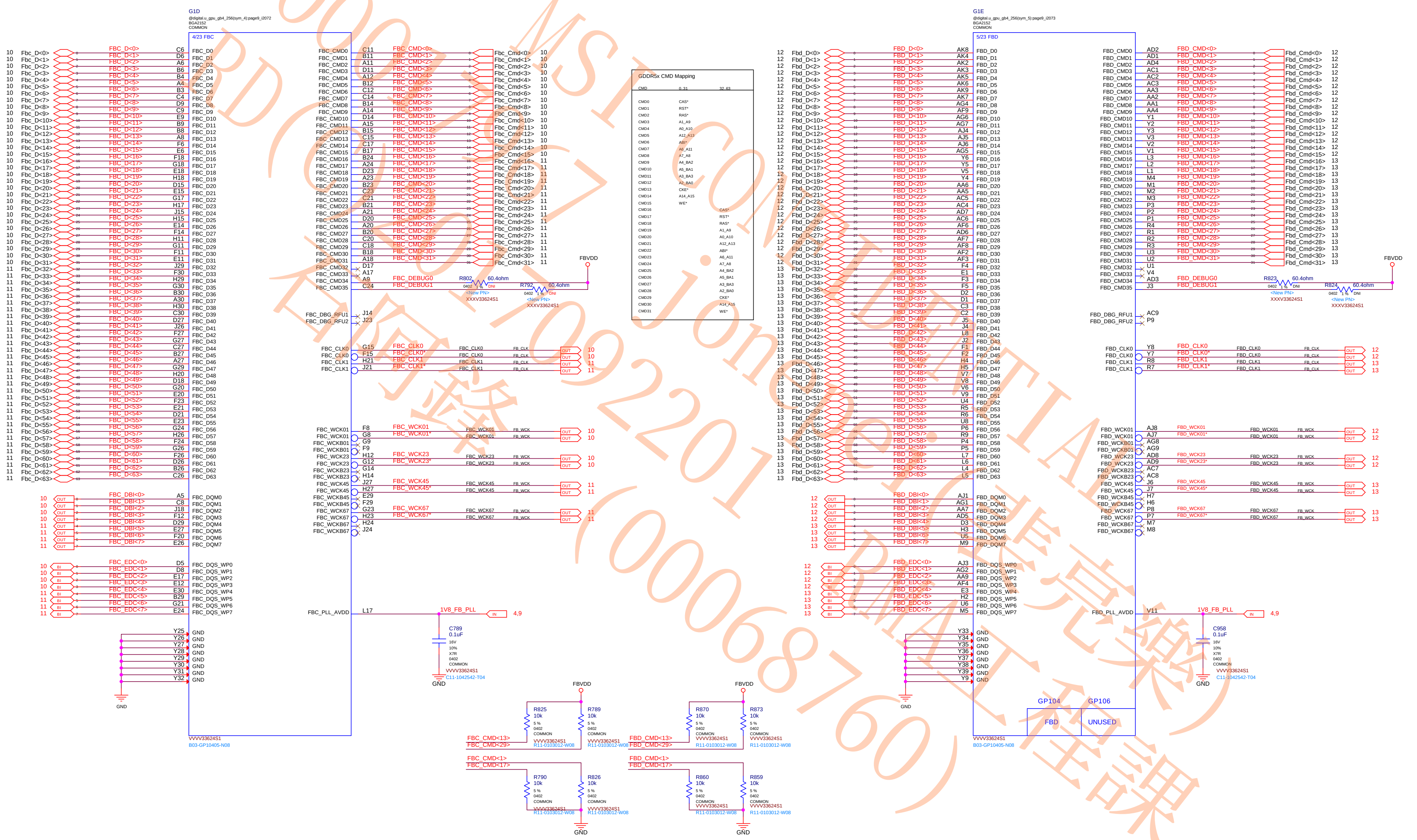
Page9: MEMORY: GPU Partition C/D



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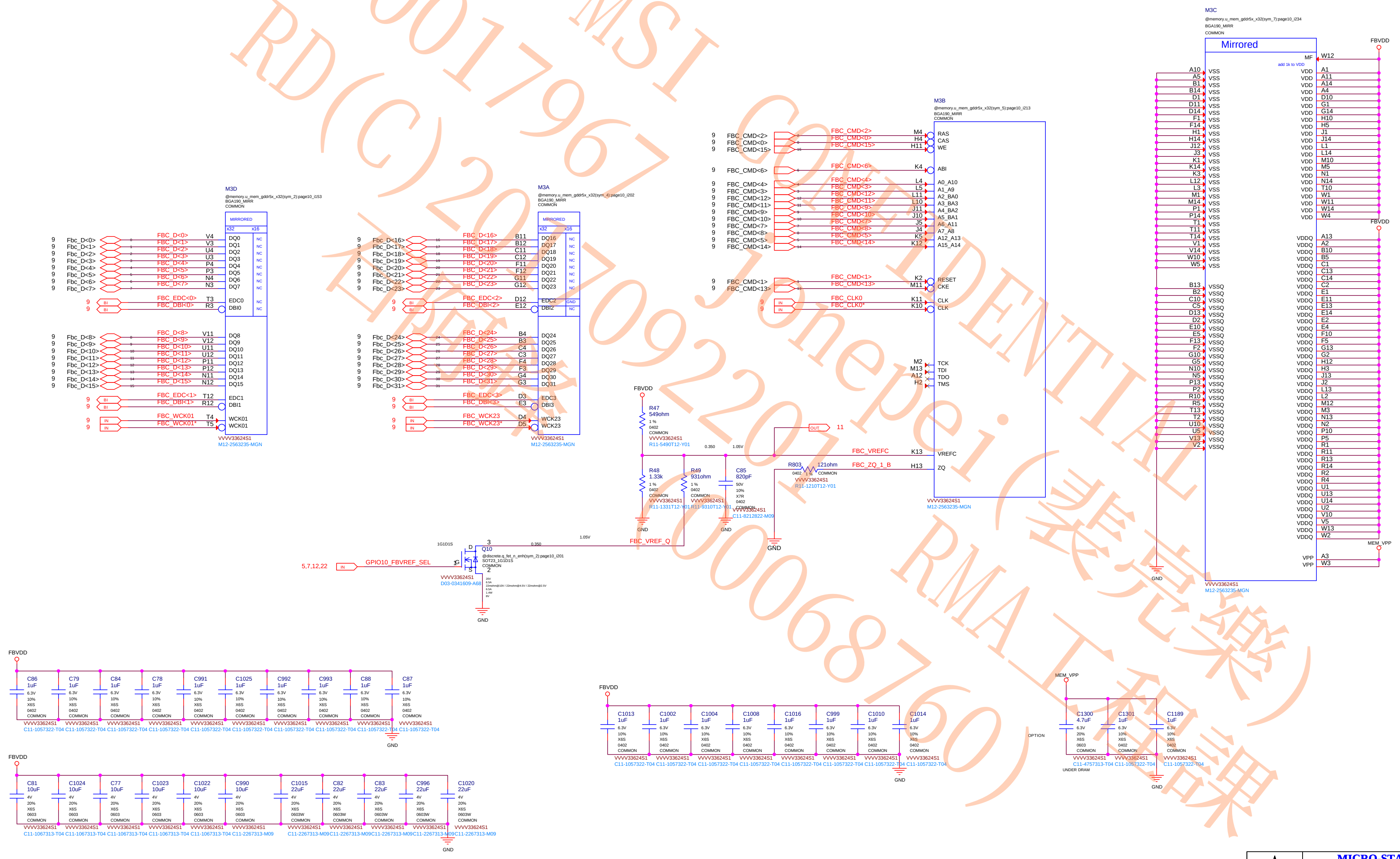
Page10: MEMORY: FBC Partition 31..0



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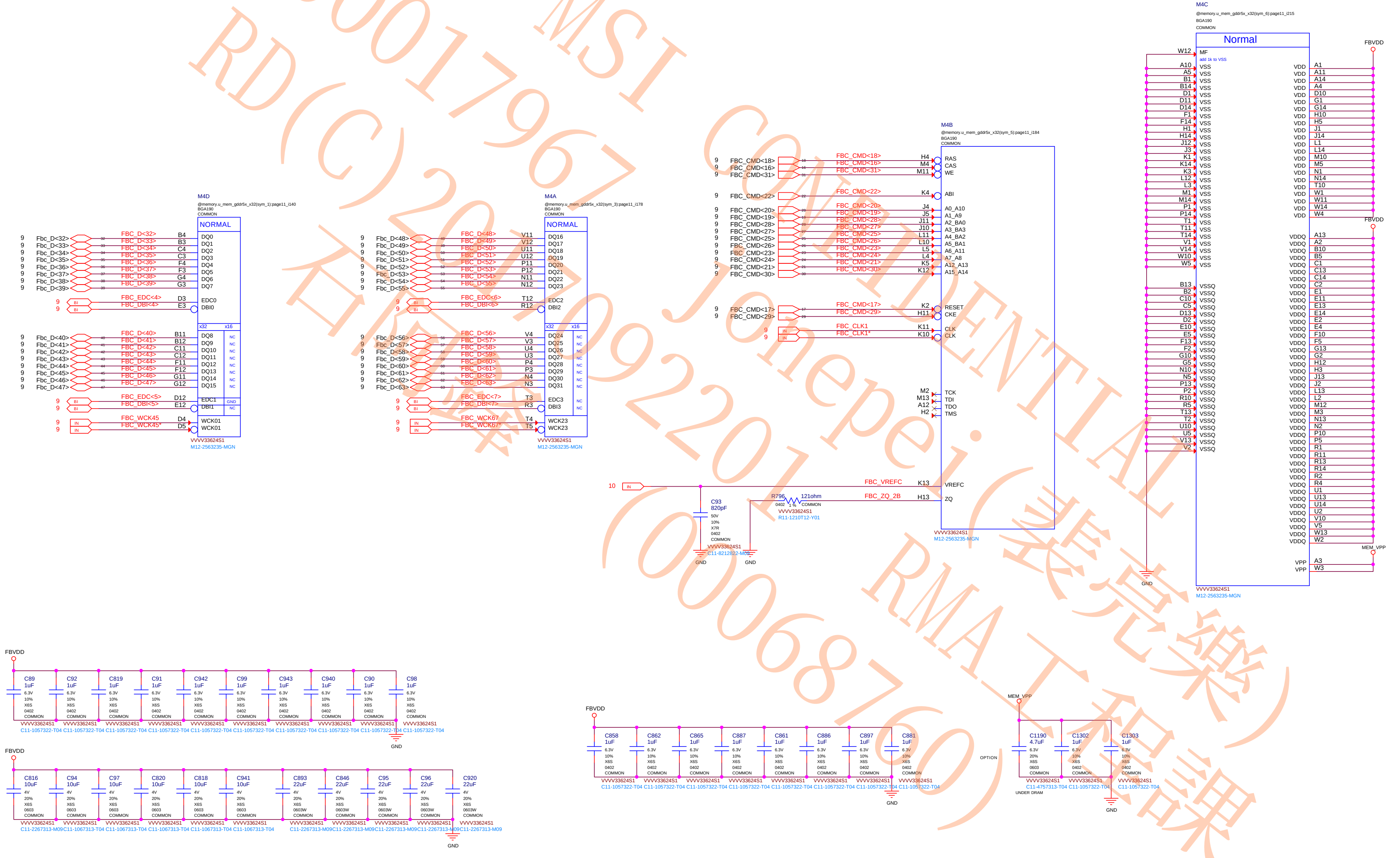
Page11: MEMORY: FBC Partition 63..32



M4D
NORMAL
M4A
NORMAL
M4B
M4C
Normal
FBC_D<32>
FBC_D<39>
FBC_EDC<4>
FBC_DBI<4>
FBC_D<40>
FBC_D<47>
FBC_EDC<5>
FBC_DBI<5>
FBC_WCK45
FBC_WCK45*
FBC_D<48>
FBC_D<55>
FBC_EDC<6>
FBC_DBI<6>
FBC_D<56>
FBC_D<63>
FBC_EDC<7>
FBC_DBI<7>
FBC_WCK67
FBC_WCK67*
FBC_CMD<18>
FBC_CMD<16>
FBC_CMD<31>
FBC_CMD<22>
FBC_CMD<20>
FBC_CMD<30>
FBC_CMD<17>
FBC_CMD<29>
FBC_CLK1
FBC_CLK1*
FBC_VREFC
FBC_ZQ_2B
RAS
CAS
WE
ABI
RESET
CKE
CLK
VREFC
ZQ
R796
121ohm
C93
820pF
FBVDD
MEM_VPP
GND
VDD
VDDQ
VSS
VSSQ
VPP
M12-2563235-MGN
C11-1057322-T04
C11-2267313-M09
C11-1067313-T04
C11-4757313-T04
OPTION
UNDER DRAM

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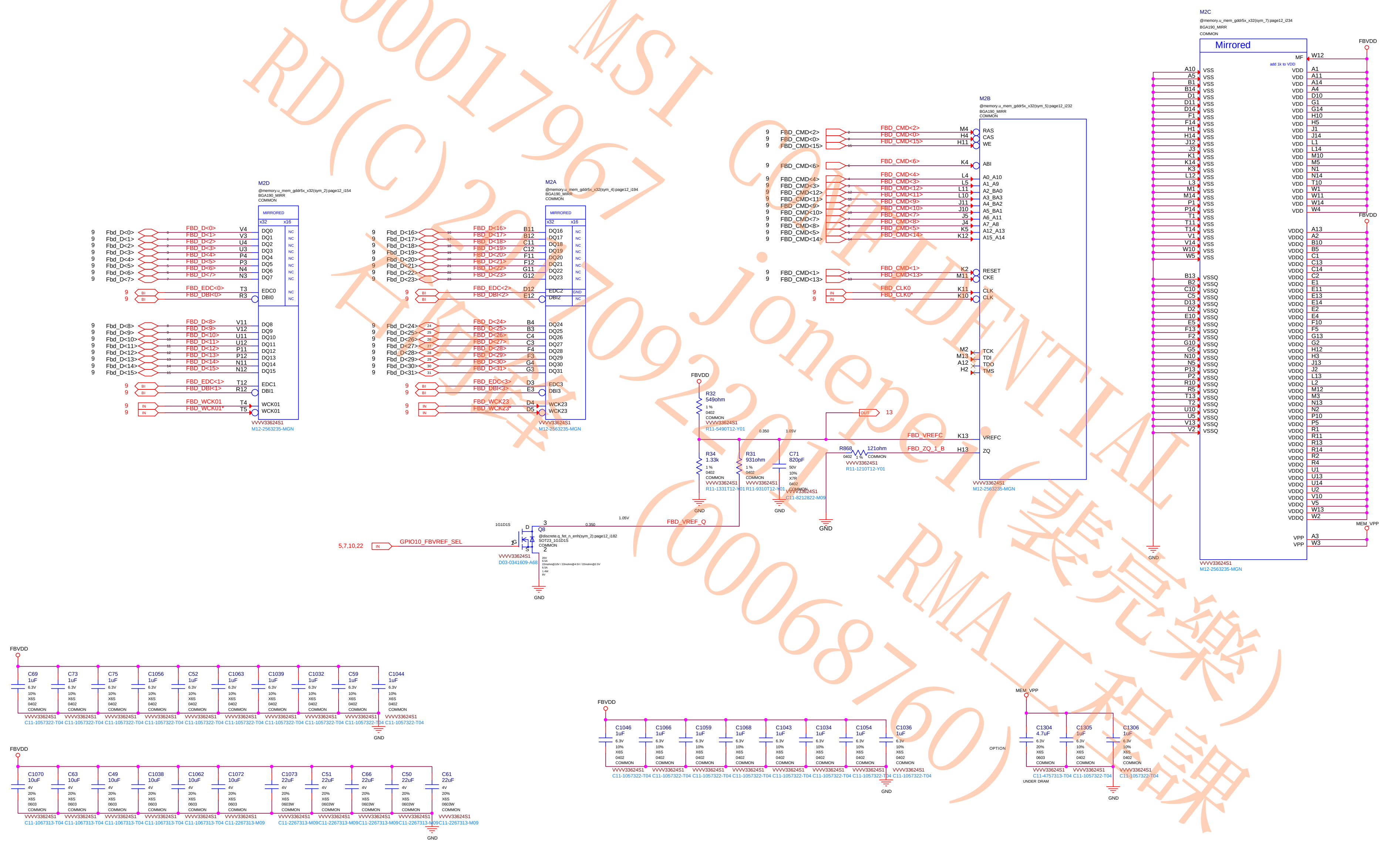
Page12: MEMORY: FBD Partition 31..0



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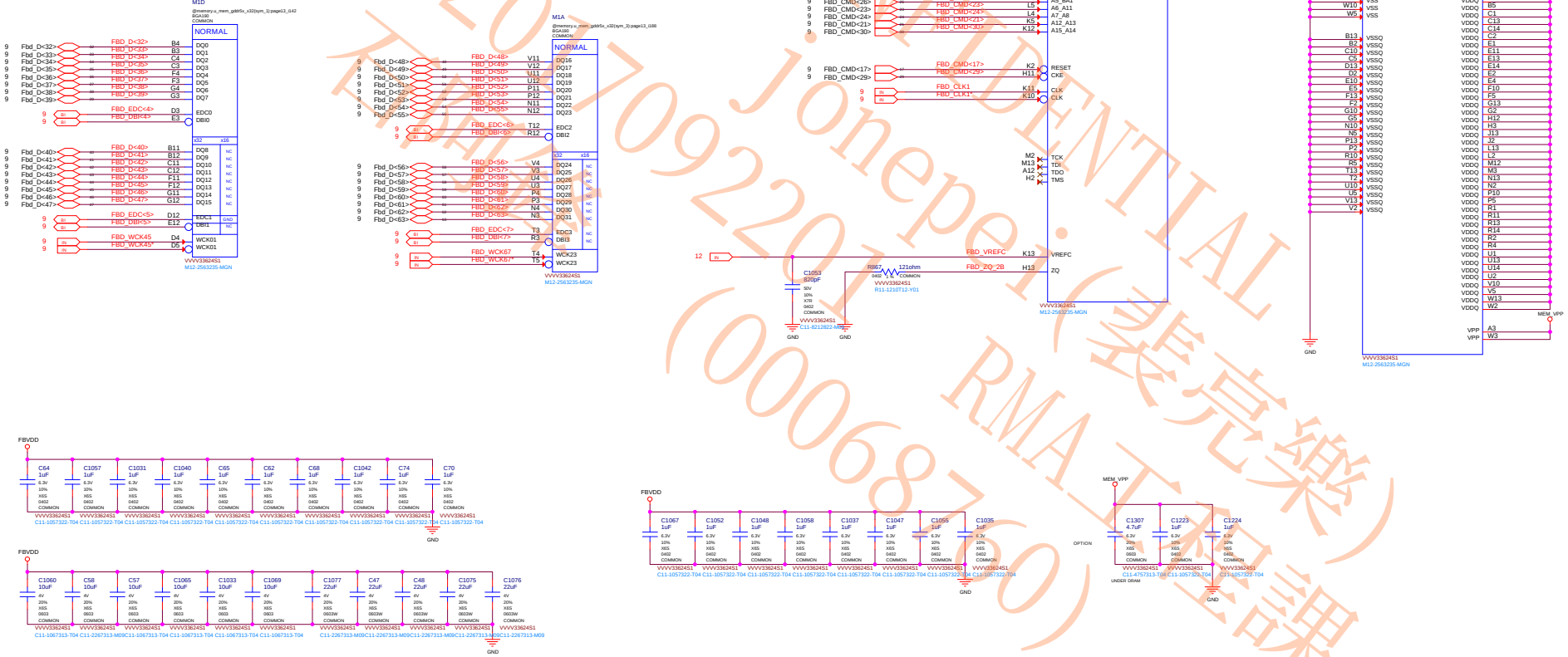

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Page14: GPU PWR and GND

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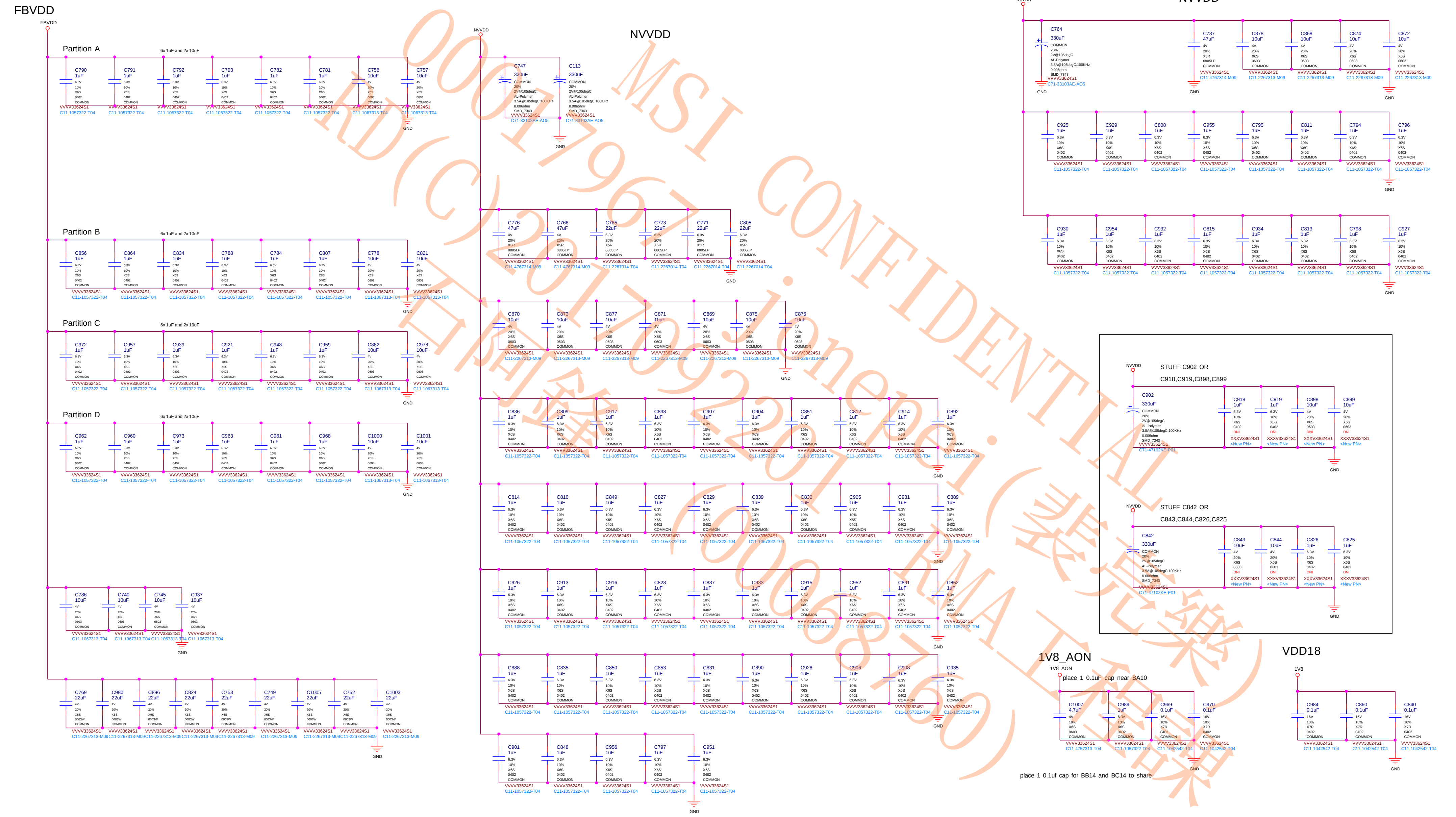
Page15: GPU Decoupling



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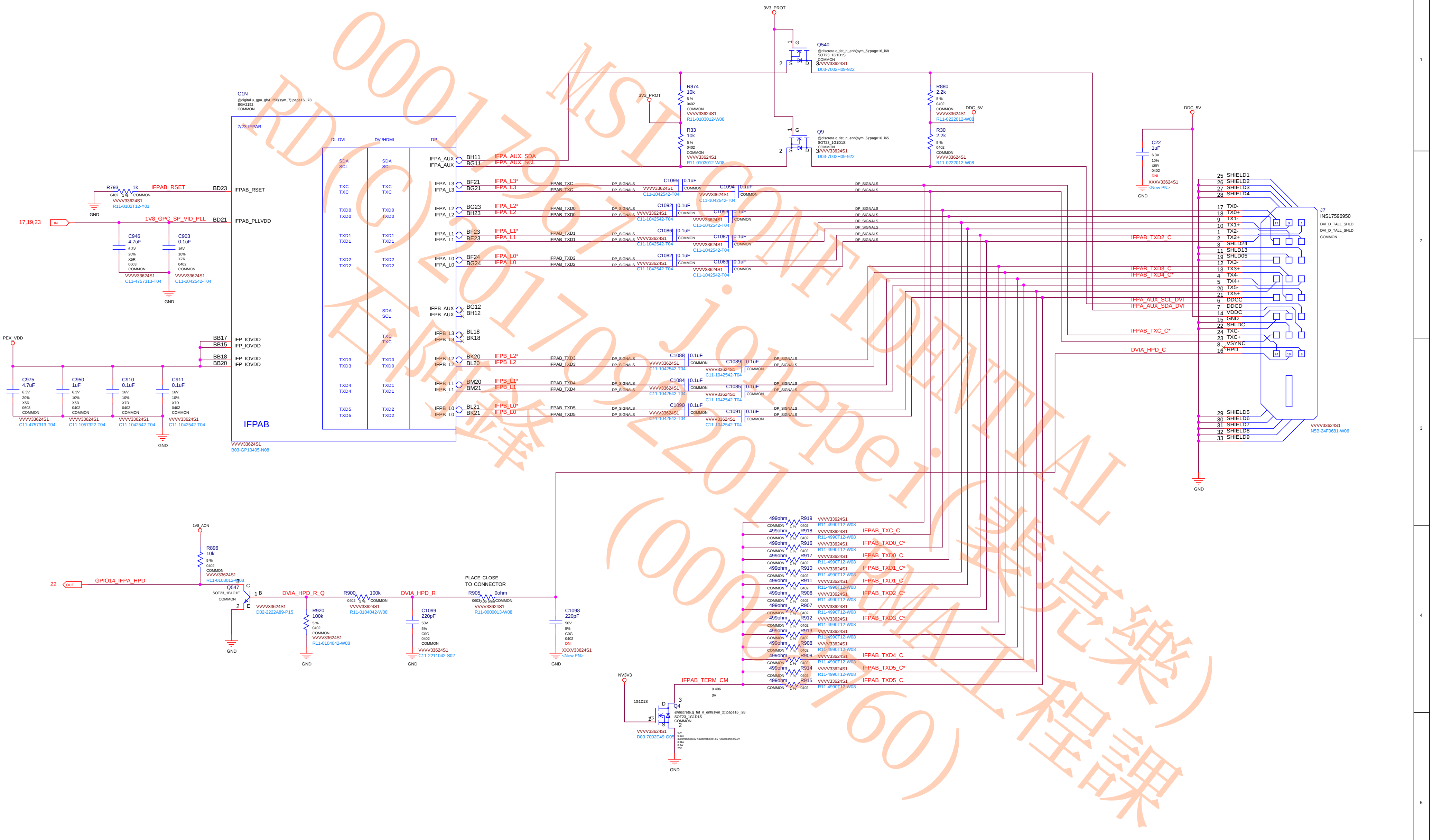
Page16: IFPAB DVI-D-DL



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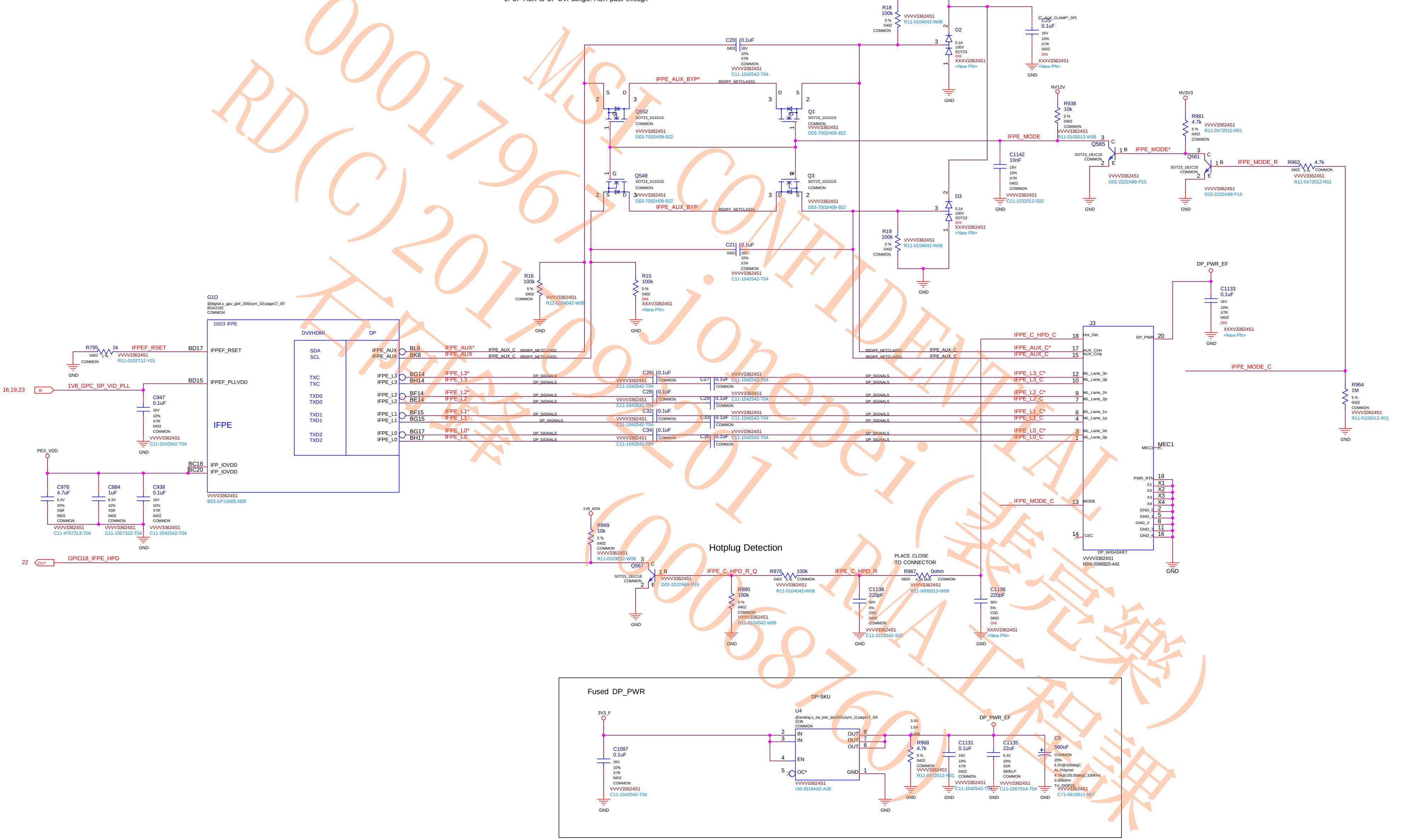
Page17: IFPE DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



DP_PWR_EF
R18 100k
D2
C20 0.1uF
C22 0.1uF
IFPE_AUX_BYP*
IFPE_AUX_BYP
Q552
Q1
Q549
Q3
D3
R19 100k
C21 0.1uF
R16 100k
R15 100k
NV12V
R938 10k
NV3V3
R981 4.7k
IFPE_MODE
C1142 10nF
Q565
IFPE_MODE*
Q561
IFPE_MODE_R
R963 4.7k
R964 1M
IFPE_MODE_C
C1133 0.1uF
G1O
10/23 IFPE
DVI/HDMI
DP
IFPEF_RSET
IFPEF_PLLVDD
IFPE
IFP_IOVDD
R795 1k
IFPEF_RSET
1V8_GPC_SP_VID_PLL
16,19,23
C947 0.1uF
PEX_VDD
C976 4.7uF
C884 1uF
C938 0.1uF
IFPE_AUX*
IFPE_AUX
IFPE_L3*
IFPE_L3
IFPE_L2*
IFPE_L2
IFPE_L1*
IFPE_L1
IFPE_L0*
IFPE_L0
C26 0.1uF
C27 0.1uF
C28 0.1uF
C29 0.1uF
C32 0.1uF
C33 0.1uF
C34 0.1uF
C35 0.1uF
J3
IFPE_C_HPD_C
IFPE_AUX_C*
IFPE_AUX_C
IFPE_L3_C*
IFPE_L3_C
IFPE_L2_C*
IFPE_L2_C
IFPE_L1_C*
IFPE_L1_C
IFPE_L0_C*
IFPE_L0_C
IFPE_MODE_C
MEC1
DP_W/GASKET
Hotplug Detection
1V8_AON
R969 10k
22
GPIO18_IFPE_HPD
Q567
IFPE_C_HPD_R_Q
R976 100k
IFPE_C_HPD_R
PLACE CLOSE TO CONNECTOR
R967 0ohm
R980 100k
C1138 220pF
C1136 220pF
Fused DP_PWR
DP-SKU
3V3_F
U4
C1097 0.1uF
DP_PWR_EF
R968 4.7k
C1131 0.1uF
C1135 22uF
C5 560uF
GND

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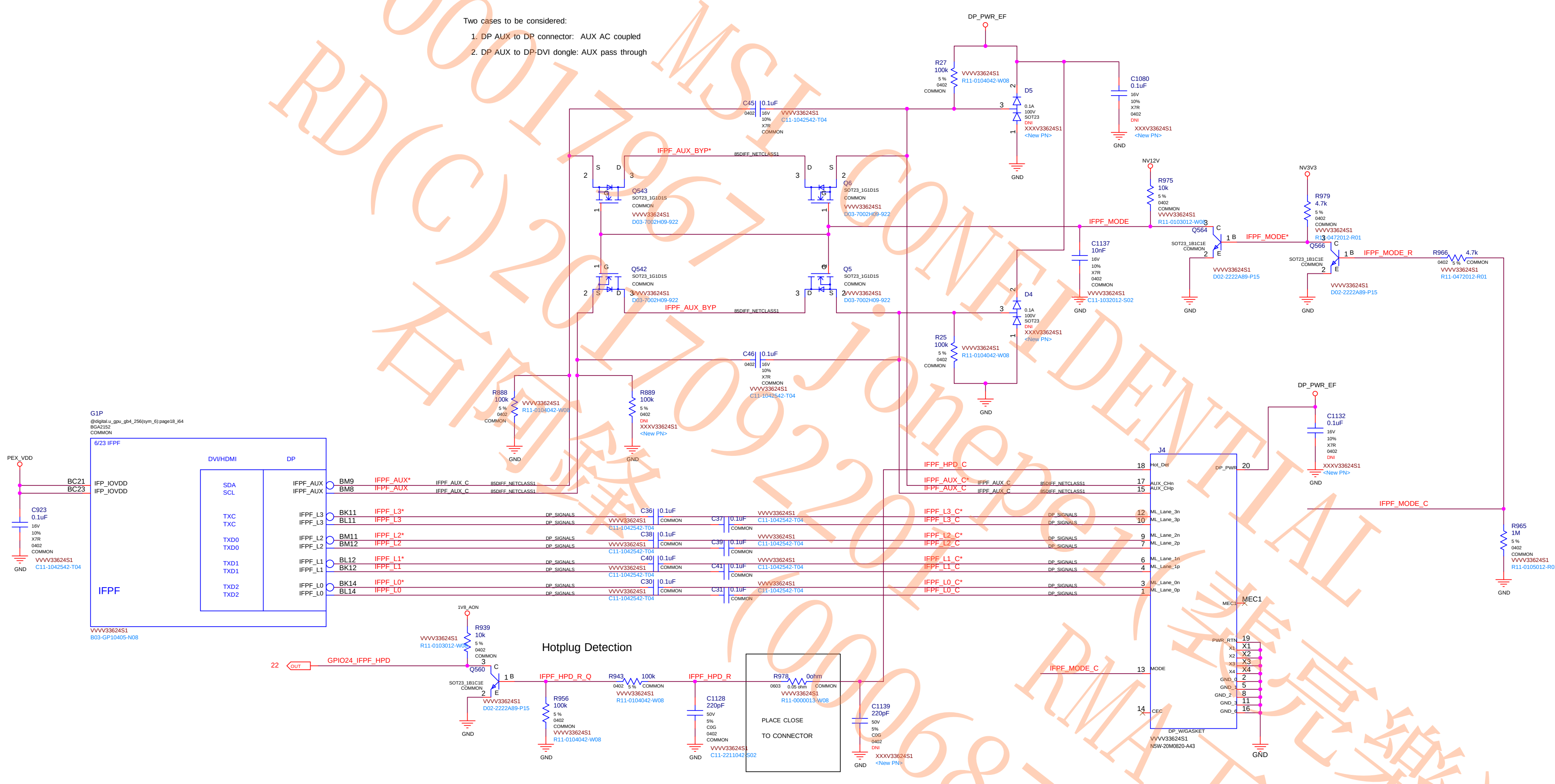
Page18: IFPF DP



Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through
DP_PWR_EF
R27 100k
D5
C1080 0.1uF
C45 0.1uF
IFPF_AUX_BYP*
Q543
Q6
Q542
Q5
IFPF_AUX_BYP
C46 0.1uF
D4
R25 100k
R888 100k
R889 100k
NV12V
R975 10k
NV3V3
R979 4.7k
IFPF_MODE
Q564
IFPF_MODE*
Q566
IFPF_MODE_R
R966 4.7k
C1137 10nF
C1132 0.1uF
G1P
6/23 IFPF
DVI/HDMI
DP
SDA
SCL
TXC
TXC
TXD0
TXD0
TXD1
TXD1
TXD2
TXD2
IFPF
PEX_VDD
IFP_IOVDD
C923 0.1uF
IFPF_AUX*
IFPF_AUX
IFPF_L3*
IFPF_L3
IFPF_L2*
IFPF_L2
IFPF_L1*
IFPF_L1
IFPF_L0*
IFPF_L0
C36 0.1uF
C37 0.1uF
C38 0.1uF
C39 0.1uF
C40 0.1uF
C41 0.1uF
C30 0.1uF
C31 0.1uF
IFPF_HPD_C
IFPF_AUX_C*
IFPF_AUX_C
IFPF_L3_C*
IFPF_L3_C
IFPF_L2_C*
IFPF_L2_C
IFPF_L1_C*
IFPF_L1_C
IFPF_L0_C*
IFPF_L0_C
J4
IFPF_MODE_C
R965 1M
Hotplug Detection
GPIO24_IFPF_HPD
R939 10k
Q560
IFPF_HPD_R_Q
R943 100k
R956 100k
IFPF_HPD_R
C1128 220pF
R978 0ohm
PLACE CLOSE
TO CONNECTOR
C1139 220pF
IFPF_MODE_C
DP_W/GASKET
GND

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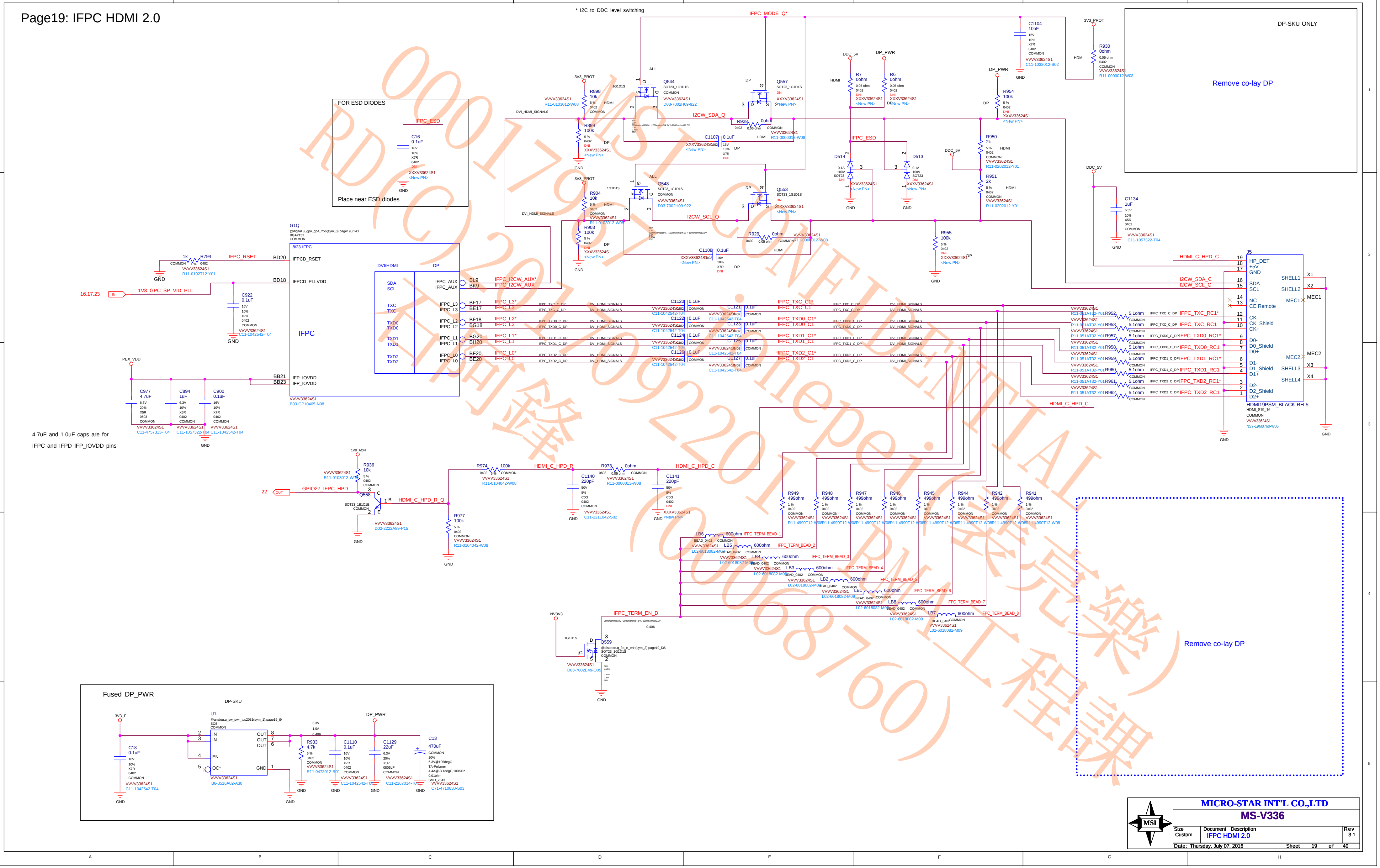
Page19: IFPC HDMI 2.0


* I2C to DDC level switching
IFPC_MODE_Q*
DP-SKU ONLY
Remove co-lay DP
FOR ESD DIODES
IFPC_ESD
Place near ESD diodes
I2CW_SDA_Q
I2CW_SCL_Q
IFPC
IFPCD_RSET
IFPCD_PLLVDD
1V8_GPC_SP_VID_PLL
IFPC_RSET
IFPC_AUX
IFPC_L3
IFPC_L2
IFPC_L1
IFPC_L0
IFP_IOVDD
IFPC_I2CW_AUX*
IFPC_I2CW_AUX
IFPC_TXC_C1*
IFPC_TXC_C1
IFPC_TXD0_C1*
IFPC_TXD0_C1
IFPC_TXD1_C1*
IFPC_TXD1_C1
IFPC_TXD2_C1*
IFPC_TXD2_C1
HDMI_C_HPD_C
I2CW_SDA_C
I2CW_SCL_C
HDMI19PSM_BLACK-RH-5
4.7uF and 1.0uF caps are for
IFPC and IFPD IFP_IOVDD pins
GPIO27_IFPC_HPD
HDMI_C_HPD_R_Q
HDMI_C_HPD_R
IFPC_TERM_EN_D
IFPC_TERM_BEAD_1
IFPC_TERM_BEAD_2
IFPC_TERM_BEAD_3
IFPC_TERM_BEAD_4
IFPC_TERM_BEAD_5
IFPC_TERM_BEAD_6
IFPC_TERM_BEAD_7
IFPC_TERM_BEAD_8
Remove co-lay DP
Fused DP_PWR
DP-SKU
3V3_F
DP_PWR

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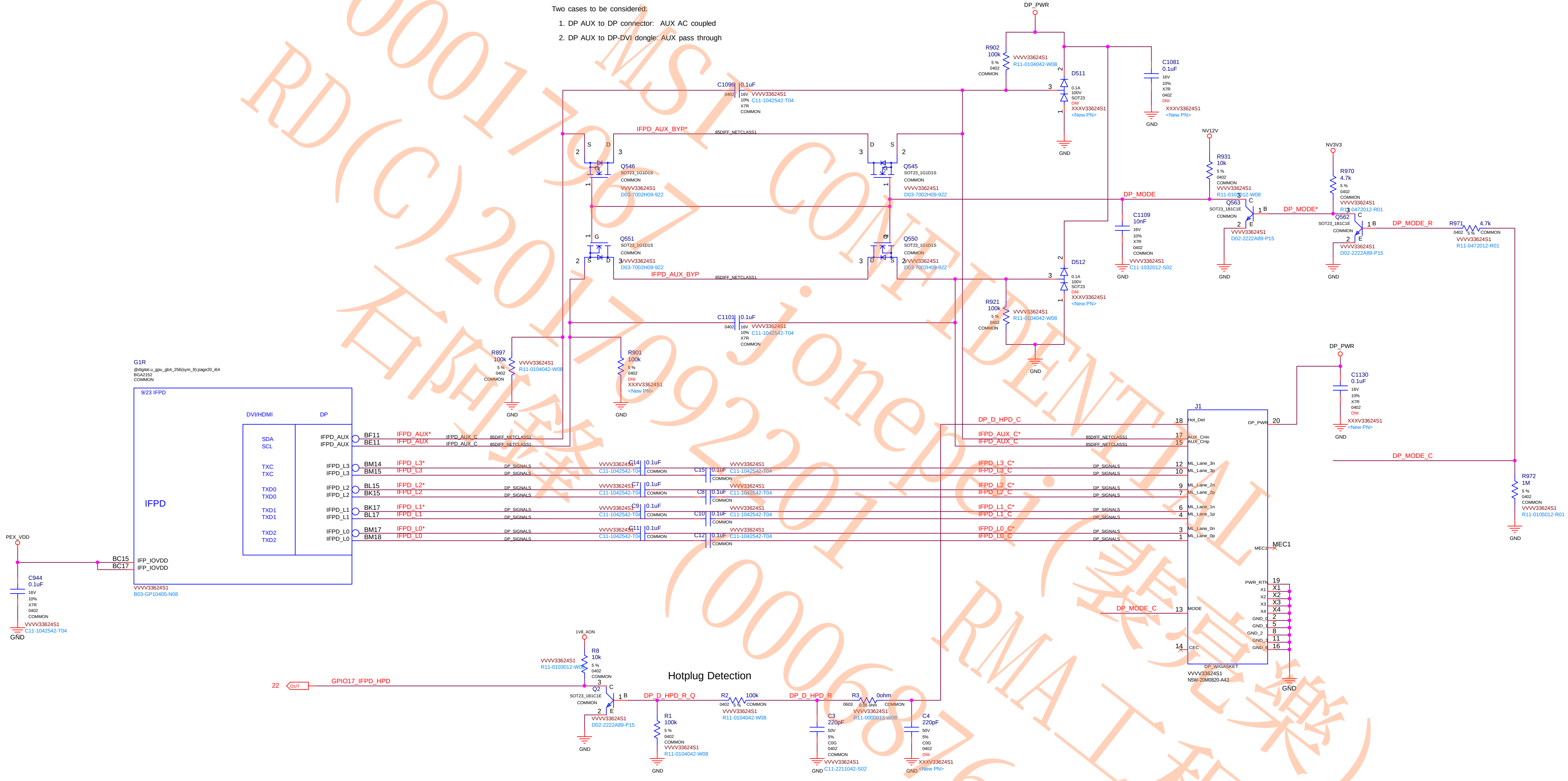
Page20: IFPD DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



DP_PWR
R902 100k
D511
C1081 0.1uF
C1090 0.1uF
IFPD_AUX_BYP*
Q546
Q545
Q551
Q550
IFPD_AUX_BYP
C1101 0.1uF
D512
R921 100k
DP_MODE
C1109 10nF
NV12V
R931 10k
Q563
DP_MODE*
NV3V3
R970 4.7k
Q562
DP_MODE_R
R971 4.7k
R897 100k
R901 100k
G1R
IFPD
DVI/HDMI
DP
IFPD_AUX*
IFPD_AUX
IFPD_L3*
IFPD_L3
IFPD_L2*
IFPD_L2
IFPD_L1*
IFPD_L1
IFPD_L0*
IFPD_L0
DP_D_HPD_C
IFPD_AUX_C*
IFPD_AUX_C
J1
DP_PWR
C1130 0.1uF
DP_MODE_C
R972 1M
MEC1
PEX_VDD
C944 0.1uF
GND
1V8_AON
R8 10k
GPIO17_IFPD_HPD
Hotplug Detection
Q2
DP_D_HPD_R_Q
R2 100k
DP_D_HPD_R
R3 0ohm
R1 100k
C3 220pF
C4 220pF

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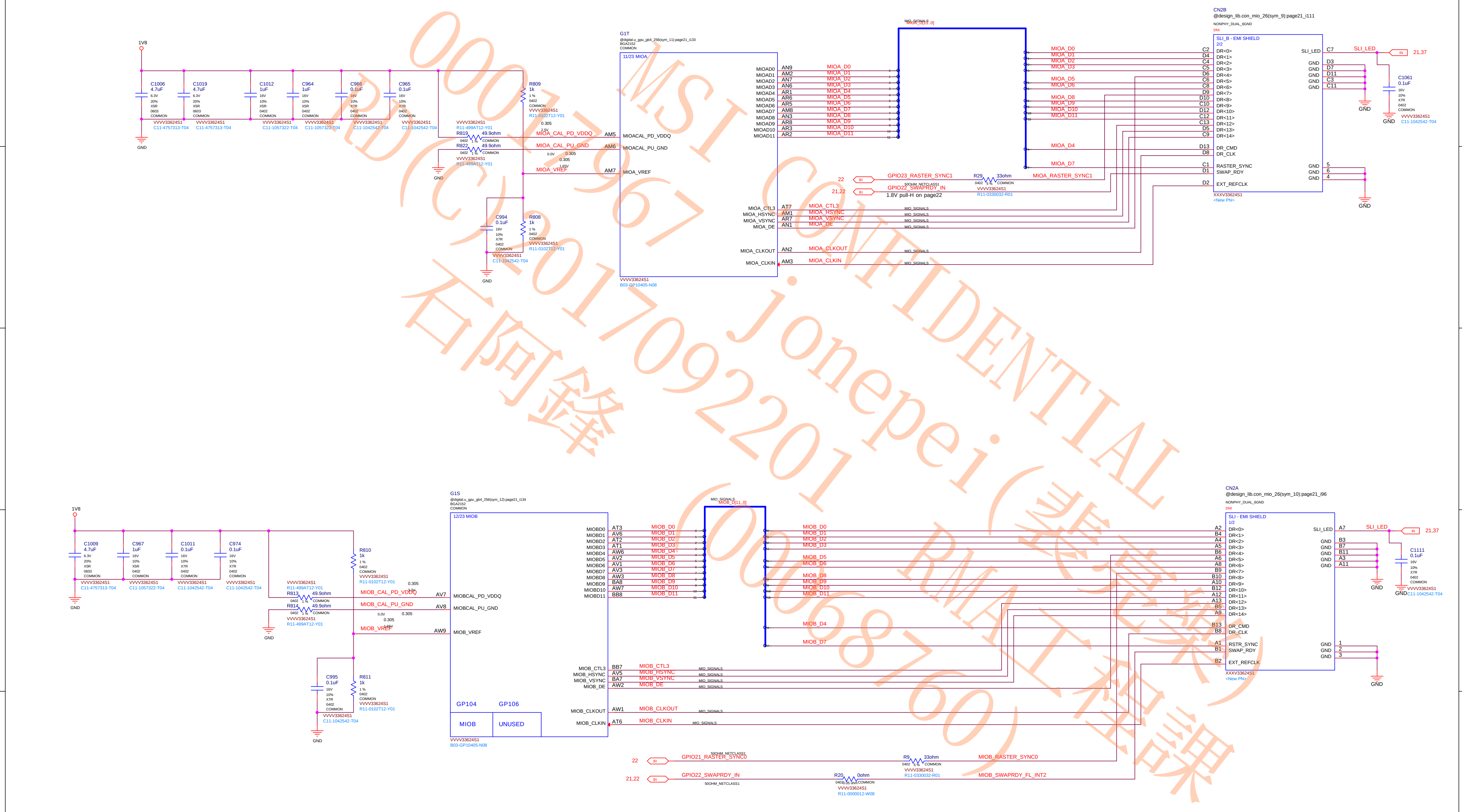
Page21: MIOA/B Interface



G1T
11/23 MIOA
MIOAD0
MIOAD1
MIOAD2
MIOAD3
MIOAD4
MIOAD5
MIOAD6
MIOAD7
MIOAD8
MIOAD9
MIOAD10
MIOAD11
MIOACAL_PD_VDDQ
MIOACAL_PU_GND
MIOA_VREF
MIOA_CTL3
MIOA_HSYNC
MIOA_VSYNC
MIOA_DE
MIOA_CLKOUT
MIOA_CLKIN
CN2B
SLI_B - EMI SHIELD
SLI_LED
RASTER_SYNC
SWAP_RDY
EXT_REFCLK
DR_CMD
DR_CLK
GPIO23_RASTER_SYNC1
GPIO22_SWAPRDY_IN
MIOA_RASTER_SYNC1
1.8V pull-H on page22
1V8
GND
G1S
12/23 MIOB
MIOBD0
MIOBD1
MIOBD2
MIOBD3
MIOBD4
MIOBD5
MIOBD6
MIOBD7
MIOBD8
MIOBD9
MIOBD10
MIOBD11
MIOBCAL_PD_VDDQ
MIOBCAL_PU_GND
MIOB_VREF
MIOB_CTL3
MIOB_HSYNC
MIOB_VSYNC
MIOB_DE
MIOB_CLKOUT
MIOB_CLKIN
GP104
GP106
MIOB
UNUSED
CN2A
SLI - EMI SHIELD
RSTR_SYNC
GPIO21_RASTER_SYNC0
MIOB_RASTER_SYNC0
MIOB_SWAPRDY_FL_INT2

MICRO-STAR INT'L CO.,LTD		
MS-V336		
Size: Custom	Document Description: MIOA/B Interface	Rev: 3.1
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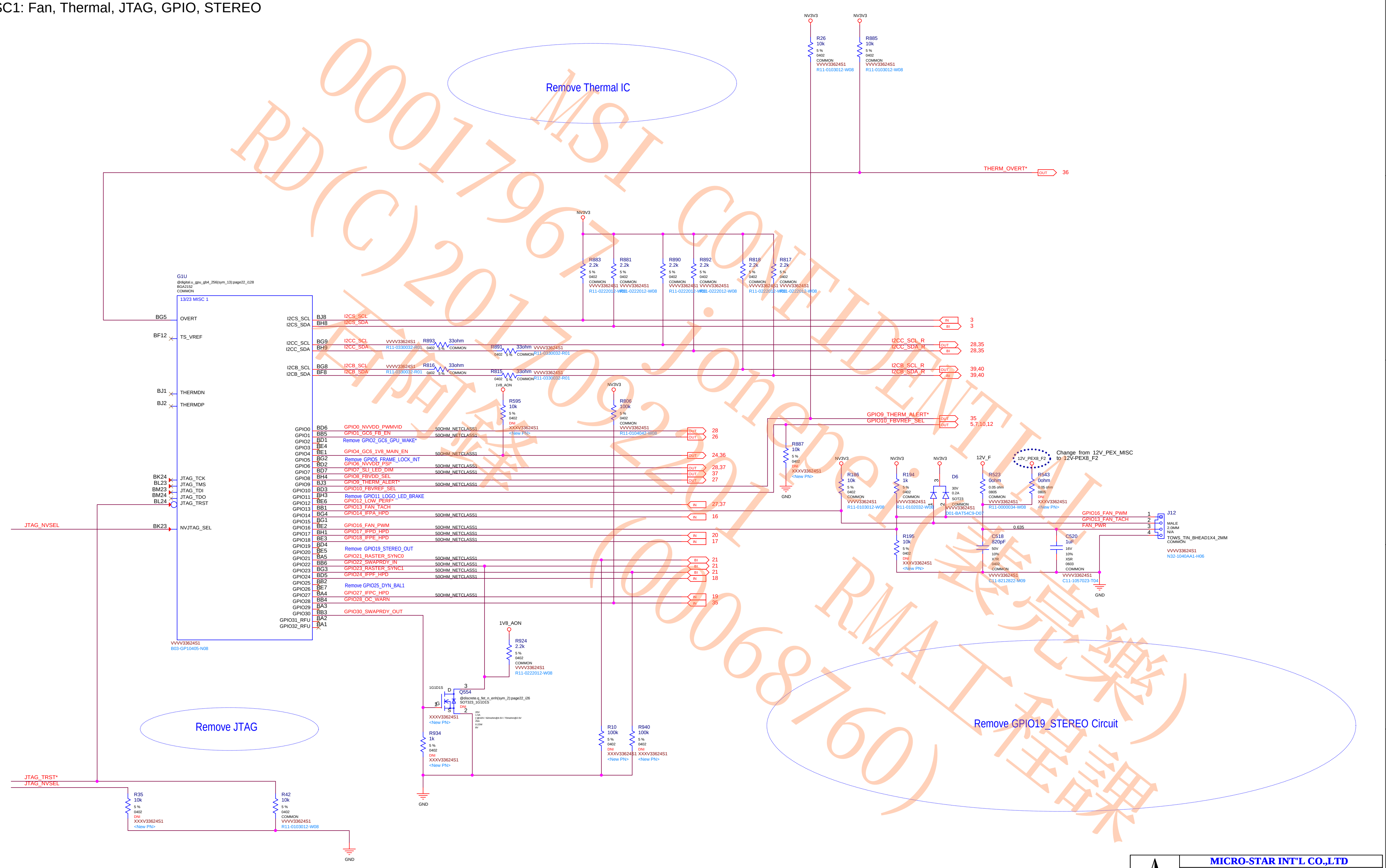
Page22: MISC1: Fan, Thermal, JTAG, GPIO, STEREO



Remove Thermal IC
Remove JTAG
Remove GPIO19_STEREO Circuit
Change from 12V_PEX_MISC to 12V-PEX8_F2
G1U
13/23 MISC 1
OVERT
TS_VREF
THERMDN
THERMDP
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST
NVJTAG_SEL
JTAG_NVSEL
JTAG_TRST*
THERM_OVERT*
I2CS_SCL
I2CS_SDA
I2CC_SCL
I2CC_SDA
I2CB_SCL
I2CB_SDA
I2CC_SCL_R
I2CC_SDA_R
I2CB_SCL_R
I2CB_SDA_R
GPIO9_THERM_ALERT*
GPIO10_FBVREF_SEL
GPIO0_NVVDD_PWMVID
GPIO1_GC6_FB_EN
Remove GPIO2_GC6_GPU_WAKE*
GPIO4_GC6_1V8_MAIN_EN
Remove GPIO5_FRAME_LOCK_INT
GPIO6_NVVDD_PSI*
GPIO7_SLI_LED_DIM
GPIO8_FBVDD_SEL
GPIO9_THERM_ALERT*
GPIO10_FBVREF_SEL
Remove GPIO11_LOGO_LED_BRAKE
GPIO12_LOW_PERF*
GPIO13_FAN_TACH
GPIO14_IFPA_HPD
GPIO16_FAN_PWM
GPIO17_IFPD_HPD
GPIO18_IFPE_HPD
Remove GPIO19_STEREO_OUT
GPIO21_RASTER_SYNC0
GPIO22_SWAPRDY_IN
GPIO23_RASTER_SYNC1
GPIO24_IFPF_HPD
Remove GPIO25_DYN_BAL1
GPIO27_IFPC_HPD
GPIO28_OC_WARN
GPIO30_SWAPRDY_OUT
FAN_PWR
J12
TOWS_TIN_BHEAD1X4_2MM
NV3V3
1V8_AON
12V_F
GND
Q554
D6
C518 820pF
C520 1uF

MSI

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MS-V336

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Custom	MISC1: Fan, Thermal, JTAG, GPIO, STEREO	3.1

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Page23: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

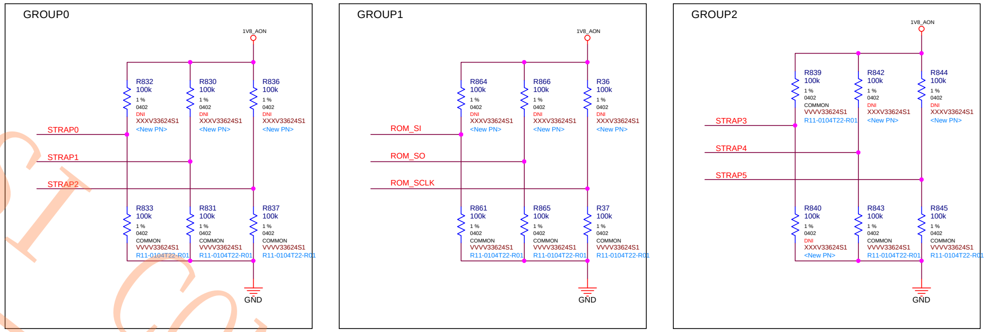
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

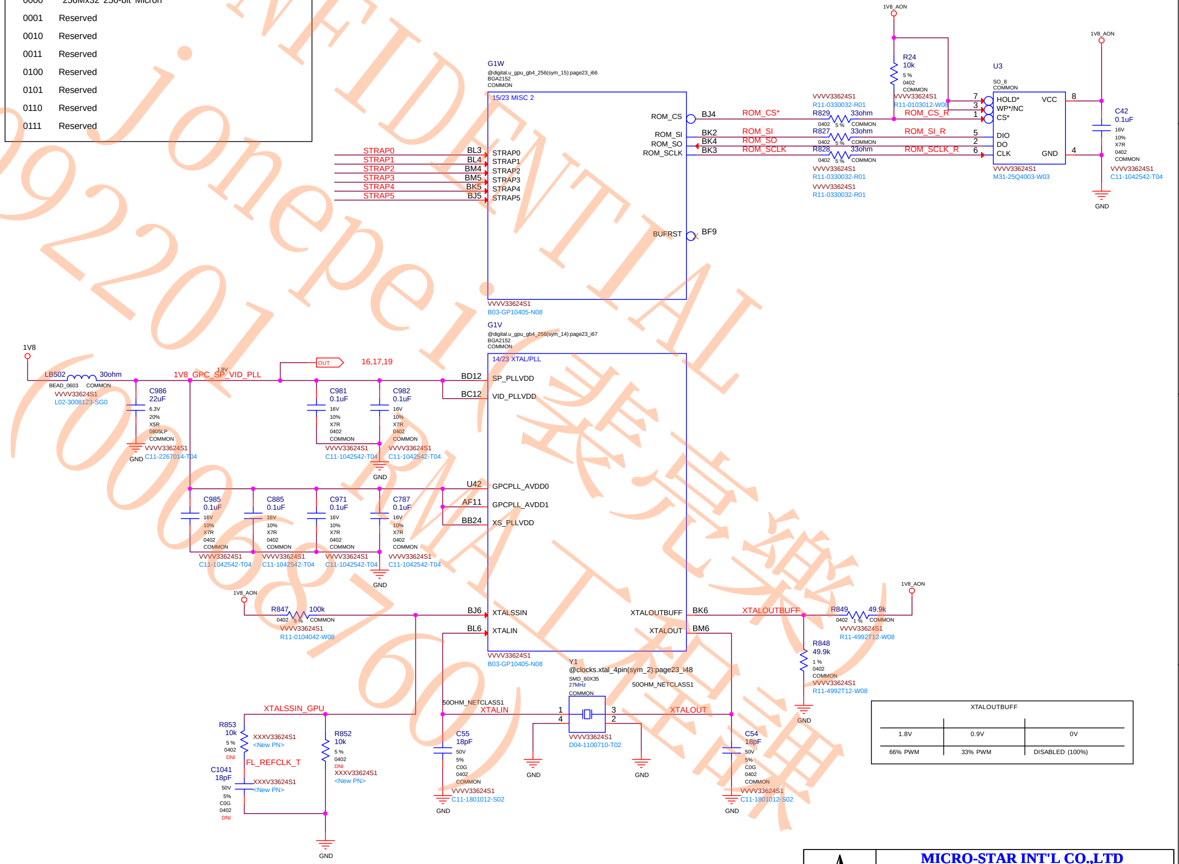
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



CFG[3:0]	Config	Width	Vendor
0000	256Mx32	256-bit	Micron
0001	Reserved		
0010	Reserved		
0011	Reserved		
0100	Reserved		
0101	Reserved		
0110	Reserved		
0111	Reserved		



MICRO-STAR INT'L CO.,LTD			
MS-V336			
Size: Custom	Document Description: MISC2: ROM, XTAL, Straps		Rev 3.1
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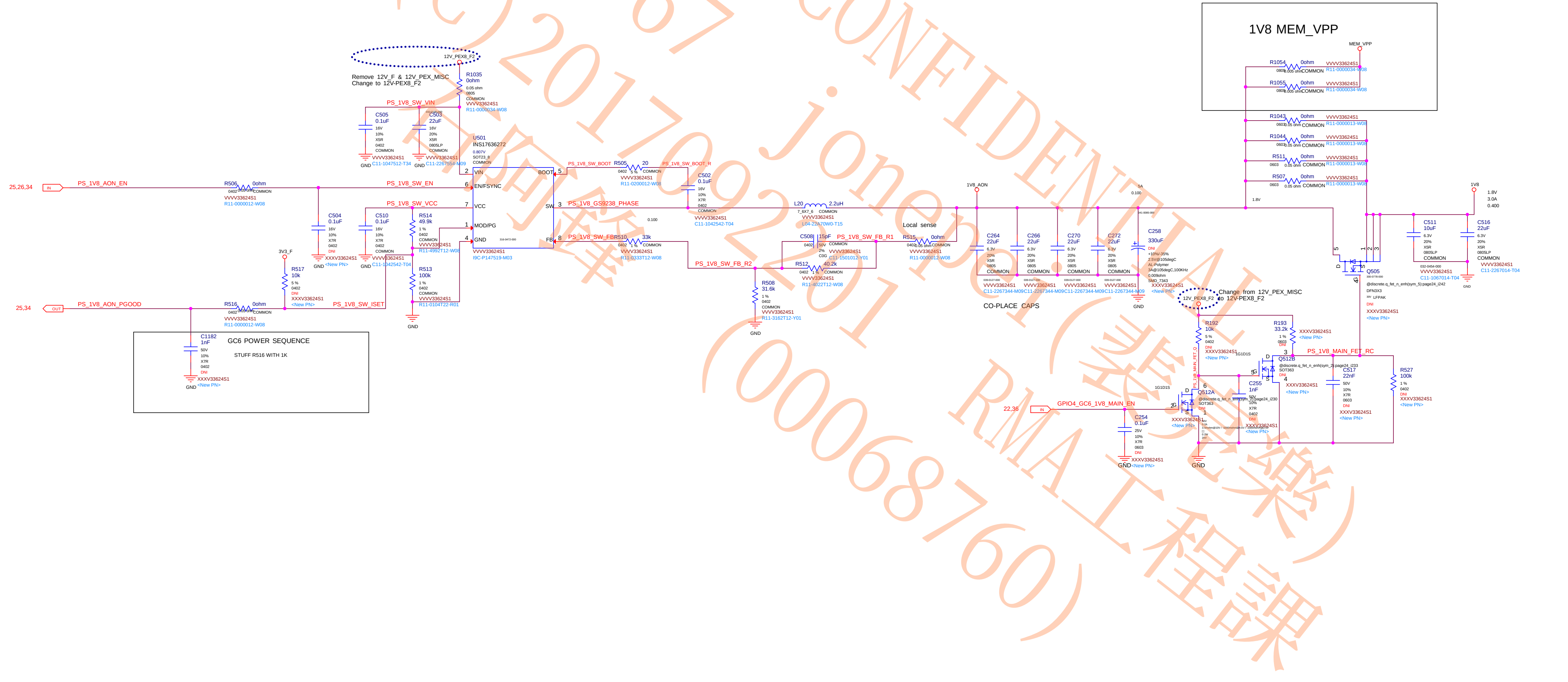
Page24: PS: 1V8, 1V8_AON



1V8 MEM_VPP
MEM_VPP
Remove 12V_F & 12V_PEX_MISC
Change to 12V-PEX8_F2
12V_PEX8_F2
R1035
0ohm
PS_1V8_SW_VIN
C505
0.1uF
C503
22uF
U501
INS17636272
25,26,34
PS_1V8_AON_EN
R506
0ohm
PS_1V8_SW_EN
VIN
EN/FSYNC
VCC
MOD/PG
GND
BOOT
SW
FB
PS_1V8_SW_BOOT
R505
20
PS_1V8_SW_BOOT_R
C502
0.1uF
PS_1V8_GS9238_PHASE
PS_1V8_SW_VCC
C504
0.1uF
C510
0.1uF
R514
49.9k
R513
100k
3V3_F
R517
10k
PS_1V8_SW_FBR
R510
33k
PS_1V8_SW_FB_R2
PS_1V8_SW_FB_R1
C508
15pF
R512
40.2k
R508
31.6k
R515
0ohm
L20
2.2uH
Local sense
1V8_AON
C264
22uF
C266
22uF
C270
22uF
C272
22uF
C258
330uF
CO-PLACE CAPS
25,34
PS_1V8_AON_PGOOD
R516
0ohm
PS_1V8_SW_ISET
C1182
1nF
GC6 POWER SEQUENCE
STUFF R516 WITH 1K
R1054
R1055
R1043
R1044
R511
R507
0ohm
1V8
1.8V
3.0A
0.400
C511
10uF
C516
22uF
Q505
Change from 12V_PEX_MISC
to 12V-PEX8_F2
R192
10k
R193
33.2k
PS_1V8_MAIN_FET_RC
Q512B
Q512A
C255
1nF
C517
22nF
R527
100k
22,36
GPIO4_GC6_1V8_MAIN_EN
C254
0.1uF
GND

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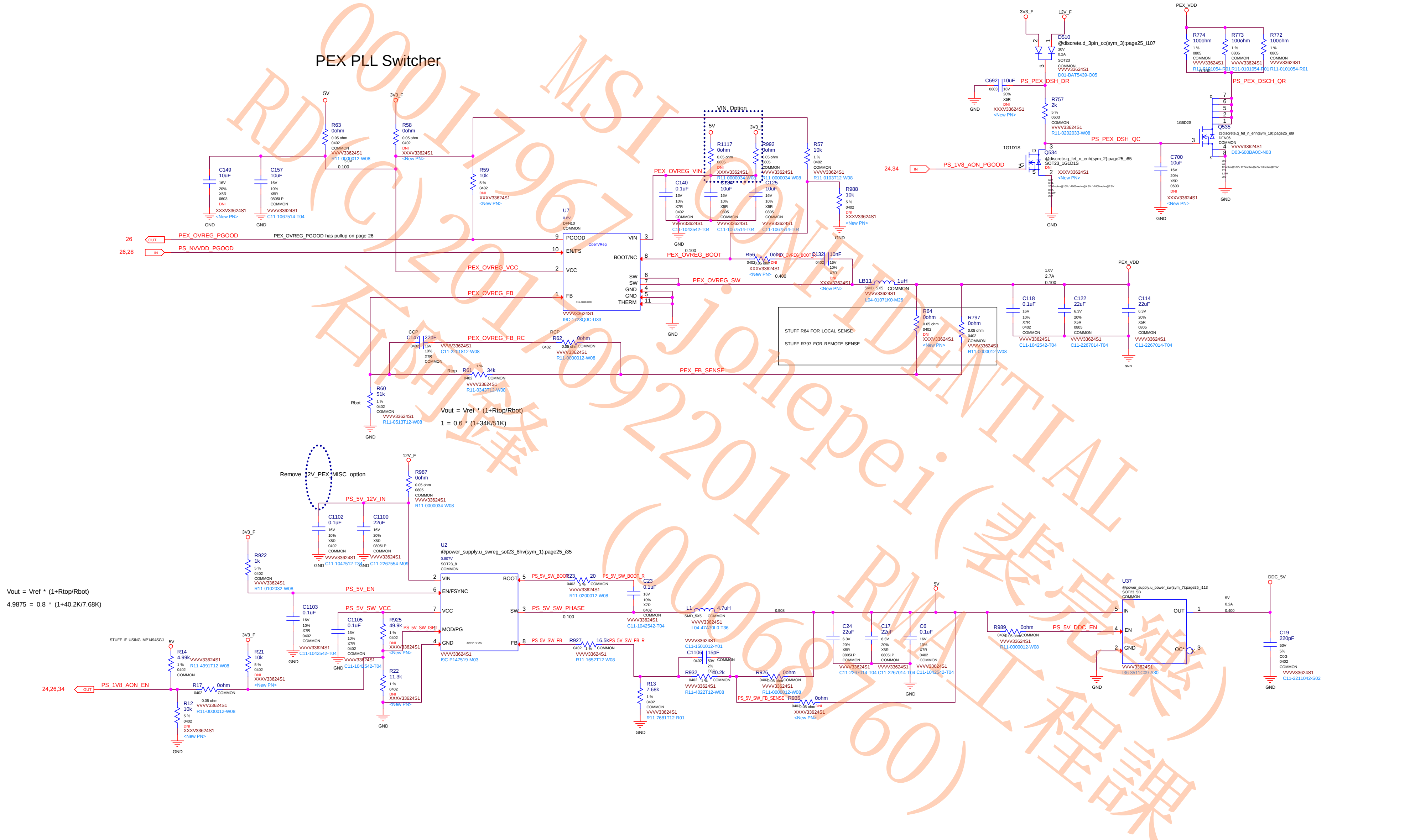
Page25: PS: 5V, PEX_VDD



PEX PLL Switcher
VIN_Option
PEX_OVREG_PGOOD
PEX_OVREG_PGOOD has pullup on page 26
PS_NVVDD_PGOOD
PEX_OVREG_VCC
PEX_OVREG_FB
PEX_OVREG_VIN
PEX_OVREG_BOOT
PEX_OVREG_SW
PEX_OVREG_FB_RC
PEX_FB_SENSE
STUFF R64 FOR LOCAL SENSE
STUFF R797 FOR REMOTE SENSE
Vout = Vref * (1+Rtop/Rbot)
1 = 0.6 * (1+34K/51K)
PS_1V8_AON_PGOOD
PS_PEX_DSH_DR
PS_PEX_DSH_QC
PS_PEX_DSCH_QR
PEX_VDD
Remove 12V_PEX_MISC option
PS_5V_12V_IN
PS_5V_EN
PS_5V_SW_VCC
PS_5V_SW_PHASE
PS_5V_DDC_EN
PS_1V8_AON_EN
Vout = Vref * (1+Rtop/Rbot)
4.9875 = 0.8 * (1+40.2K/7.68K)
STUFF IF USING MP1494SGJ
DDC_5V

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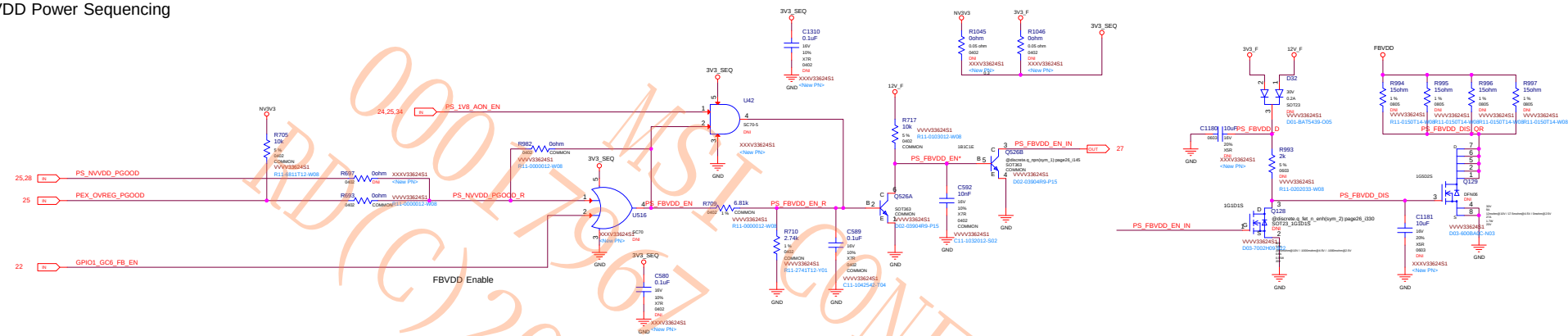
Page26: PS: FBVDD Power Sequencing



MICRO-STAR INT'L CO.,LTD		
MS-V336		
Size: Custom	Document Description: PS:FBVDD Power Sequencing	Rev: 3.1
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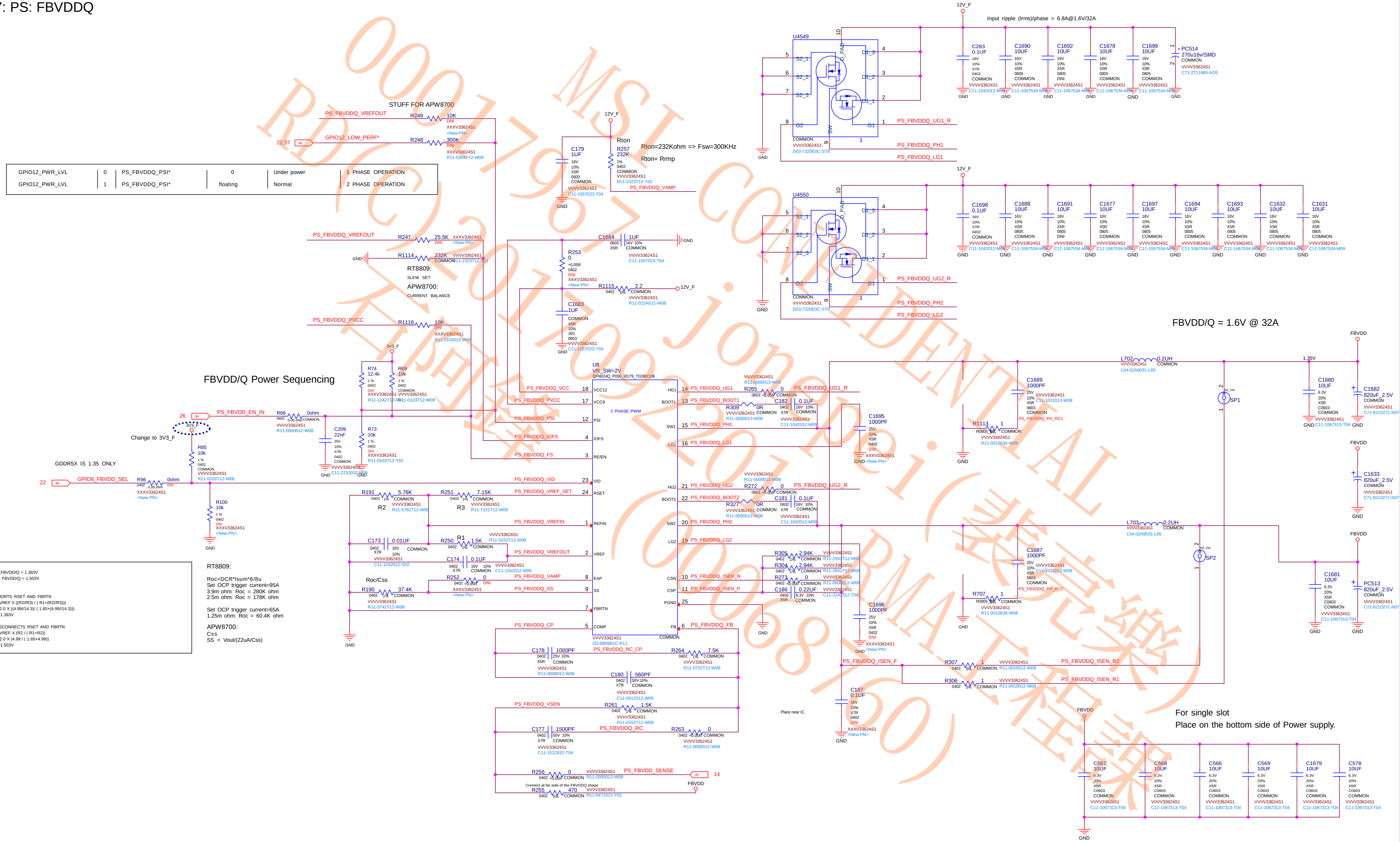
Page27: PS: FBVDDQ



GPIO12_PWR_LVL	0	PS_FBVDDQ_PSI*	0	Under power	1 PHASE OPERATION
GPIO12_PWR_LVL	1	PS_FBVDDQ_PSI*	floating	Normal	2 PHASE OPERATION

GPIO8 =1 FBVDD/Q = 1.383V
GPIO8 = 0 FBVDD/Q = 1.503V

VID =1 SHORTS RSET AND FBRTN
VREFIN = VREF X ((R2//R3) / (R1+(R2//R3)))
VREFIN = 2.0 X ((4.99//14.3)/ (1.65+(4.99//14.3)))
VREFIN = 1.383V

VID =0 DISCONNECTS RSET AND FBRTN
VREFIN = VREF X (R2 / (R1+R2))
VREFIN = 2.0 X (4.99 / (1.65+4.99))
VREFIN = 1.503V

RT8809:

Roc=DCR*Isum*6/8u
Set OCP trigger current=95A
3.9m ohm: Roc = 280K ohm
2.5m ohm: Roc = 178K ohm

Set OCP trigger current=65A
1.25m ohm: Roc = 60.4K ohm

APW8700:
Css
SS = Vout/(22uA/Css)

MICRO-STAR INT'L CO.,LTD
MS-V336

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Custom	PS: FBVDDQ	3.1

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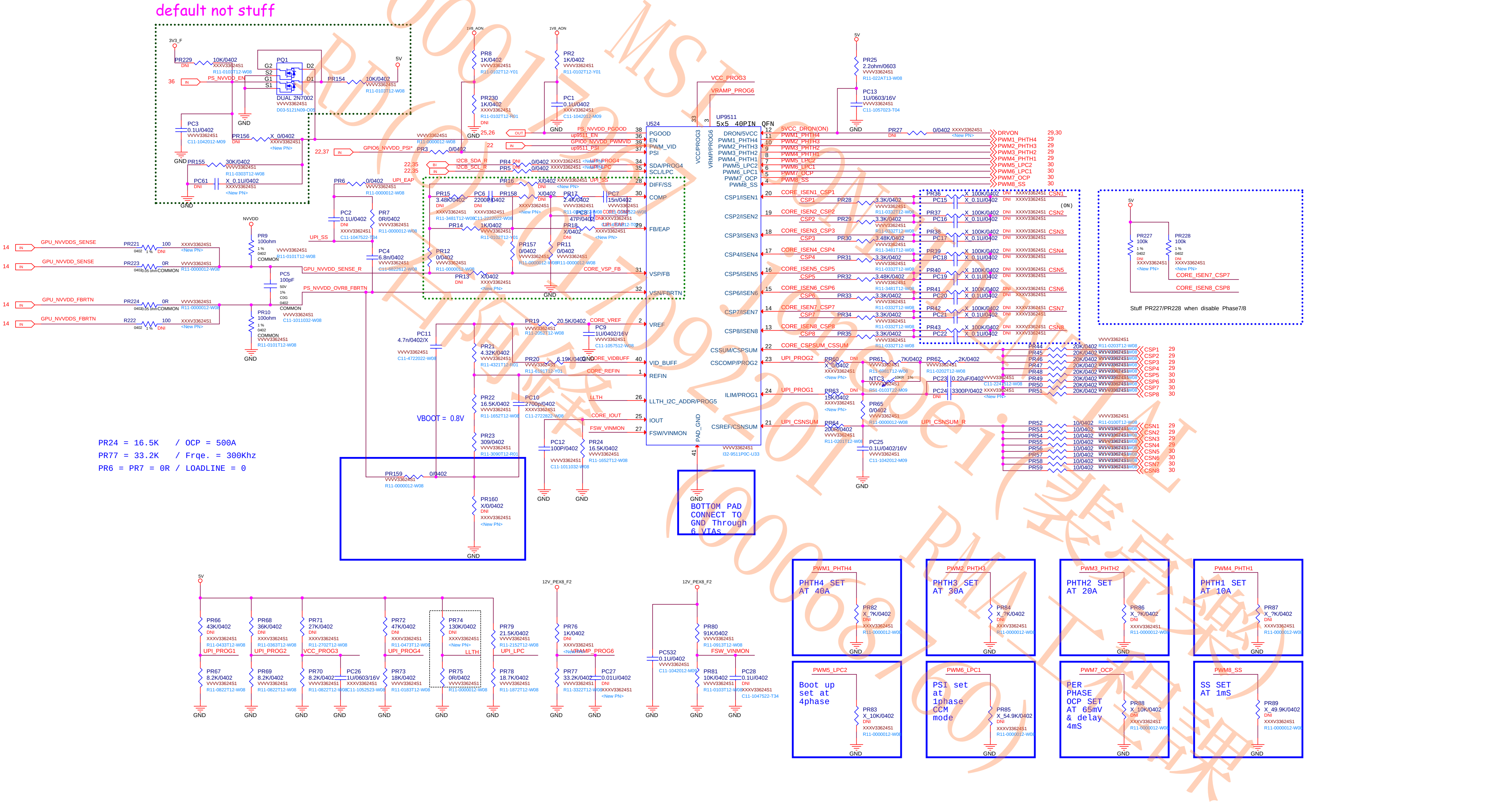
Page28: PS: NVVDD_OVR8



default not stuff
U524
UP9511
5x5 40PIN QFN
PGOOD
EN
PWM_VID
PSI
SDA/PROG4
SCL/LPC
DIFF/SS
COMP
FB/EAP
VSP/FB
VSN/FBRTN
VREF
VID_BUFF
REFIN
LLTH_I2C_ADDR/PROG5
IOUT
FSW/VINMON
DRON/5VCC
PWM1_PHTH4
PWM2_PHTH3
PWM3_PHTH2
PWM4_PHTH1
PWM5_LPC2
PWM6_LPC1
PWM7_OCP
PWM8_SS
CSP1/ISEN1
CSP2/ISEN2
CSP3/ISEN3
CSP4/ISEN4
CSP5/ISEN5
CSP6/ISEN6
CSP7/ISEN7
CSP8/ISEN8
CSSUM/CSPSUM
CSCOMP/PROG2
ILIM/PROG1
CSREF/CSNSUM
PAD_GND
VCC/PROG3
VRAMP/PROG6
GPU_NVVDDS_SENSE
GPU_NVVDD_SENSE
GPU_NVVDD_FBRTN
GPU_NVVDDS_FBRTN
VBOOT = 0.8V
PR24 = 16.5K / OCP = 500A
PR77 = 33.2K / Frqe. = 300Khz
PR6 = PR7 = 0R / LOADLINE = 0
BOTTOM PAD CONNECT TO GND Through 6 VIAS
Stuff PR227/PR228 when disable Phase7/8
PWM1_PHTH4 PHTH4 SET AT 40A
PWM2_PHTH3 PHTH3 SET AT 30A
PWM3_PHTH2 PHTH2 SET AT 20A
PWM4_PHTH1 PHTH1 SET AT 10A
PWM5_LPC2 Boot up set at 4phase
PWM6_LPC1 PSI set at 1phase CCM mode
PWM7_OCP PER PHASE OCP SET AT 65mV & delay 4mS
PWM8_SS SS SET AT 1mS

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MS-V323			
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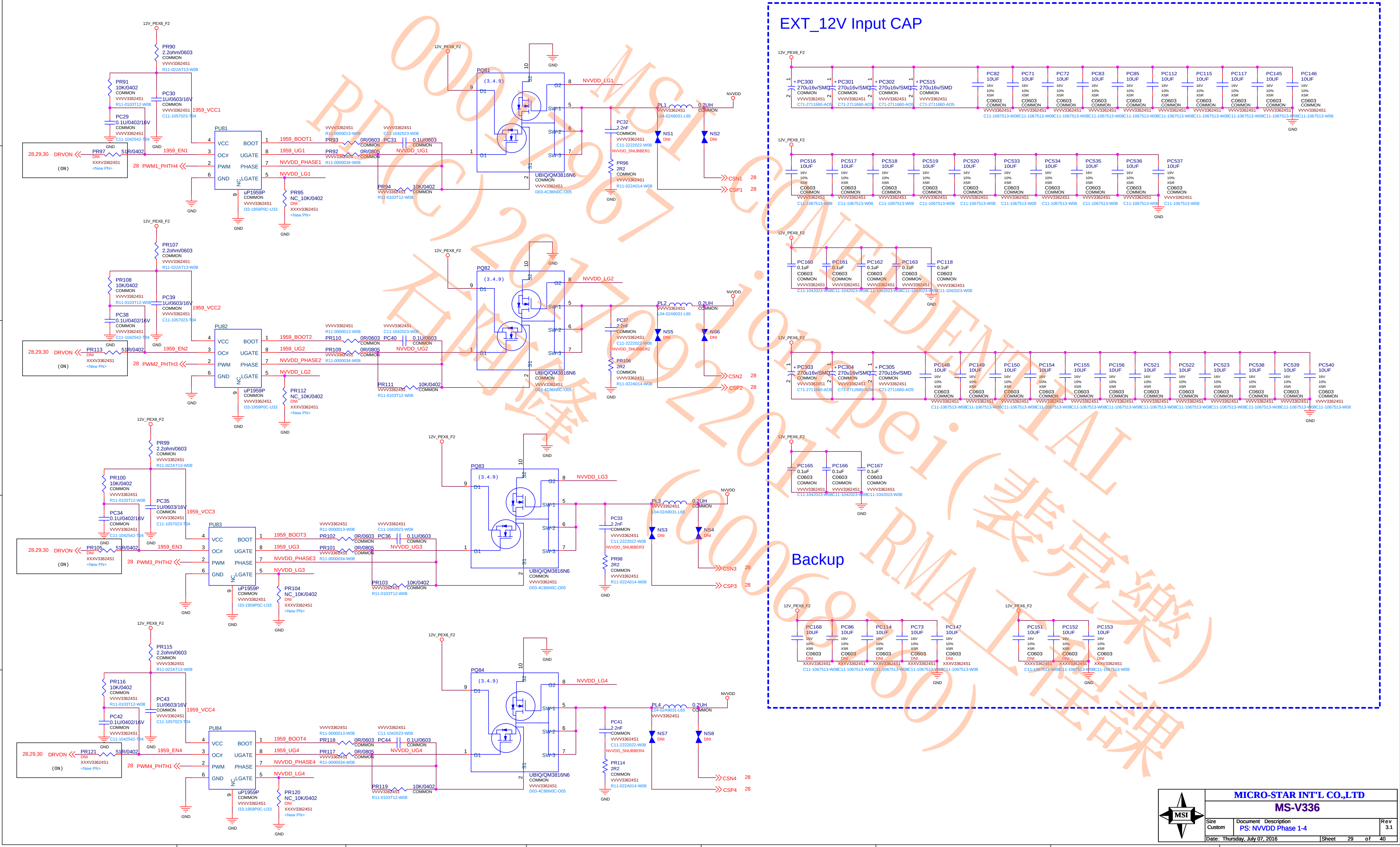
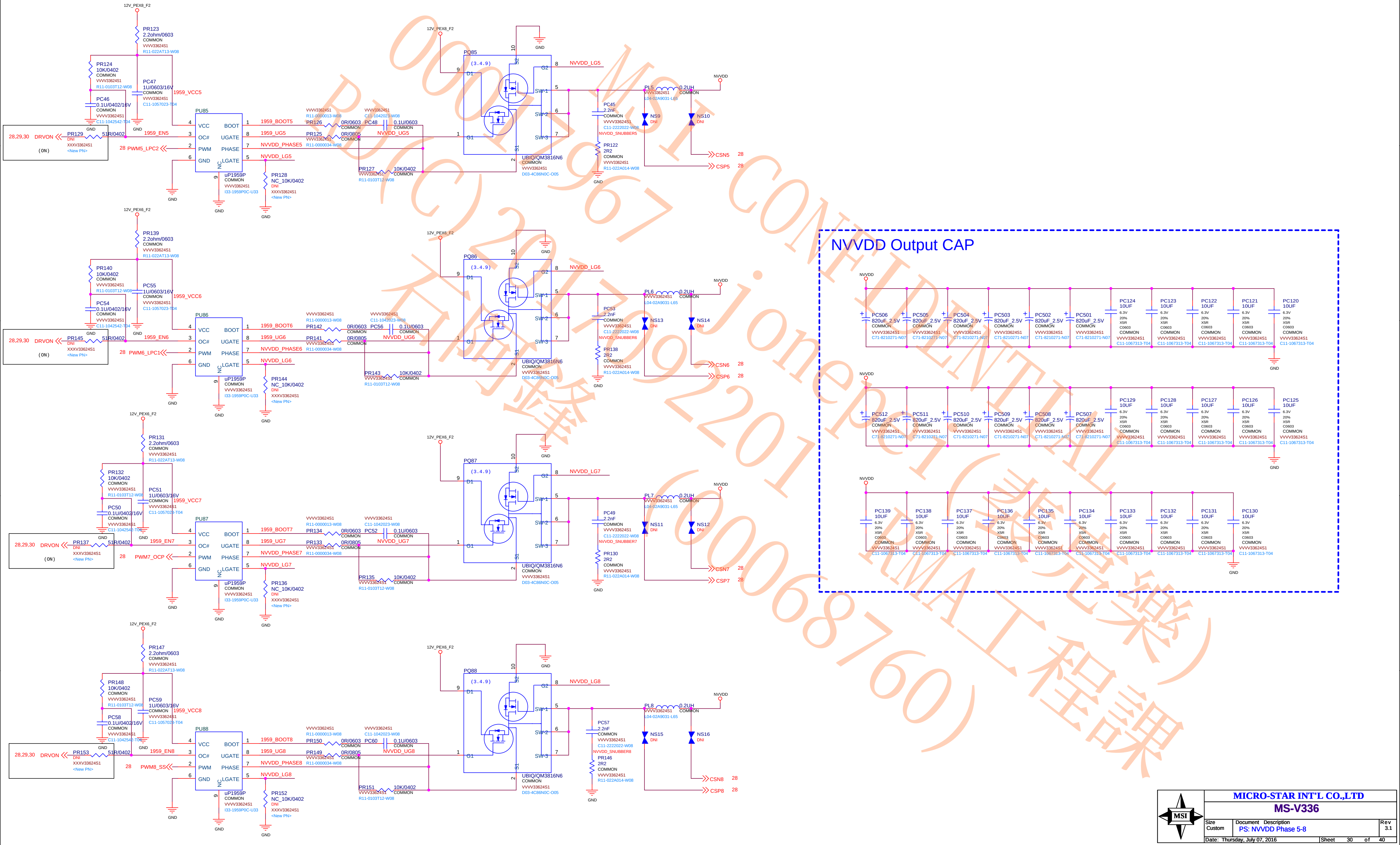
Page29: PS: NVVDD Phase 1-4



Page30: PS: NVVDD Phase 5-8



NVVDD Output CAP
PU85
PU86
PU87
PU88
uP1959P
PQ85
PQ86
PQ87
PQ88
UBIQ/QM3816N6
NVVDD_LG5
NVVDD_LG6
NVVDD_LG7
NVVDD_LG8
NVVDD_PHASE5
NVVDD_PHASE6
NVVDD_PHASE7
NVVDD_PHASE8
1959_BOOT5
1959_BOOT6
1959_BOOT7
1959_BOOT8
1959_UG5
1959_UG6
1959_UG7
1959_UG8
1959_EN5
1959_EN6
1959_EN7
1959_EN8
1959_VCC5
1959_VCC6
1959_VCC7
1959_VCC8
PWM5_LPC2
PWM6_LPC1
PWM7_OCP
PWM8_SS
DRVON
CSN5
CSP5
CSN6
CSP6
CSN7
CSP7
CSN8
CSP8
12V_PEX8_F2
12V_PEX6_F2
NVVDD
GND
MICRO-STAR INT'L CO.,LTD
MS-V336
PS: NVVDD Phase 5-8
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Page31: PS: Blank Page

MSI	MICRO-STAR INT'L CO.,LTD	
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Page32: PS: Dynamic Power Balance Phases

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V336	
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Page33: PS: Dynamic Power Balance Logic

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	MS-V336	
Size: Custom	Document Description: PS: Dynamic Power Balance Logic	Rev: 3.1
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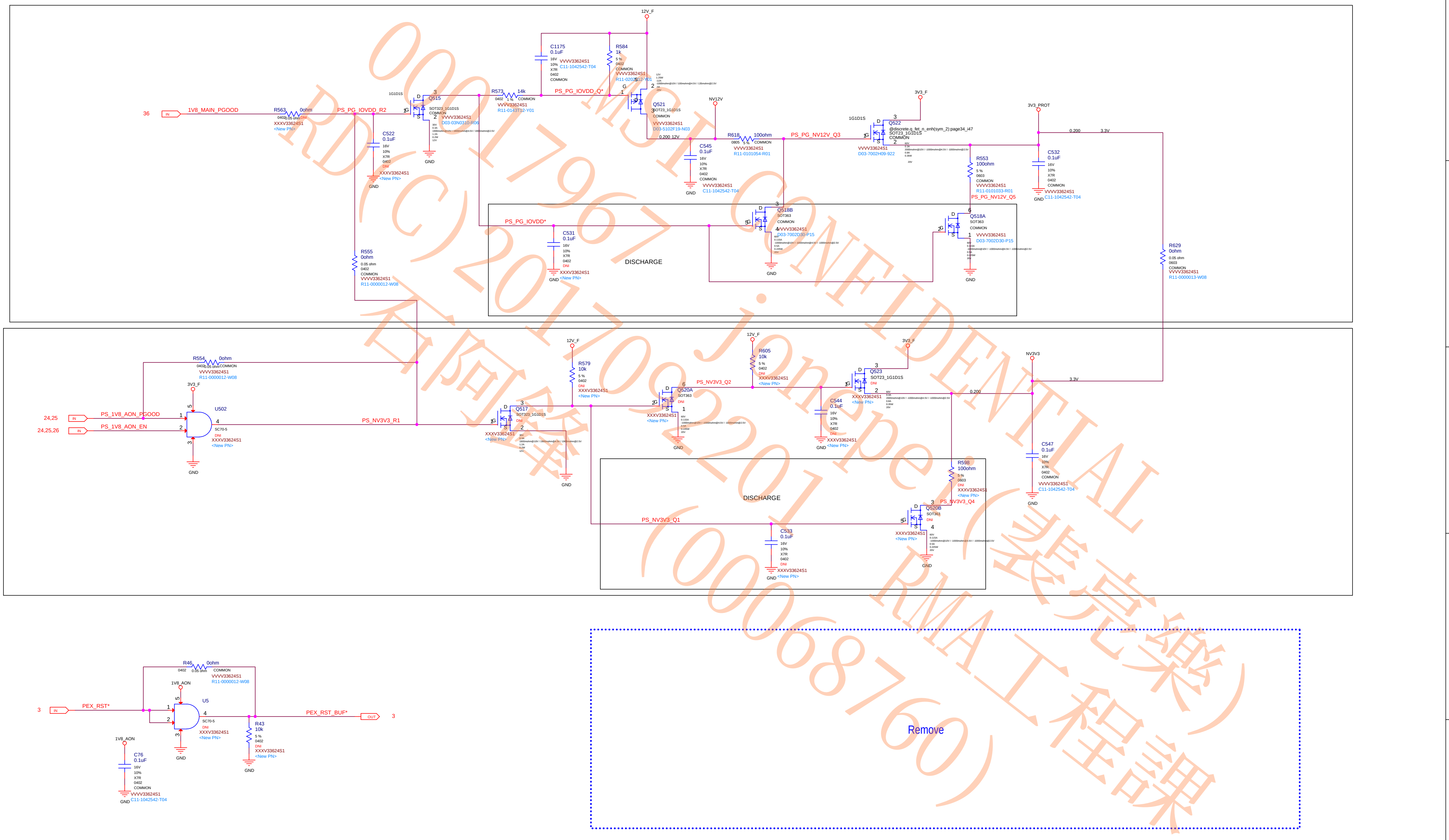
Page34:PS: NV3V3, NV12V



12V_F
C1175 0.1uF
R584 1k
Q515
Q521
R573 14k
R563 0ohm
1V8_MAIN_PGOOD
PS_PG_IOVDD_R2
PS_PG_IOVDD_Q*
C522 0.1uF
NV12V
C545 0.1uF
R618 100ohm
PS_PG_NV12V_Q3
3V3_F
Q522
3V3_PROT
C532 0.1uF
R553 100ohm
PS_PG_NV12V_Q5
Q518B
Q518A
PS_PG_IOVDD*
C531 0.1uF
DISCHARGE
R555 0ohm
R629 0ohm
R554 0ohm
3V3_F
U502
PS_1V8_AON_PGOOD
PS_1V8_AON_EN
PS_NV3V3_R1
R579 10k
Q517
R605 10k
Q520A
PS_NV3V3_Q2
Q523
C544 0.1uF
NV3V3
C547 0.1uF
R598 100ohm
PS_NV3V3_Q4
Q520B
PS_NV3V3_Q1
C533 0.1uF
DISCHARGE
R46 0ohm
1V8_AON
U5
PEX_RST*
PEX_RST_BUF*
R43 10k
C76 0.1uF
GND
Remove

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	PS: NV3V3, NV12V	3.1

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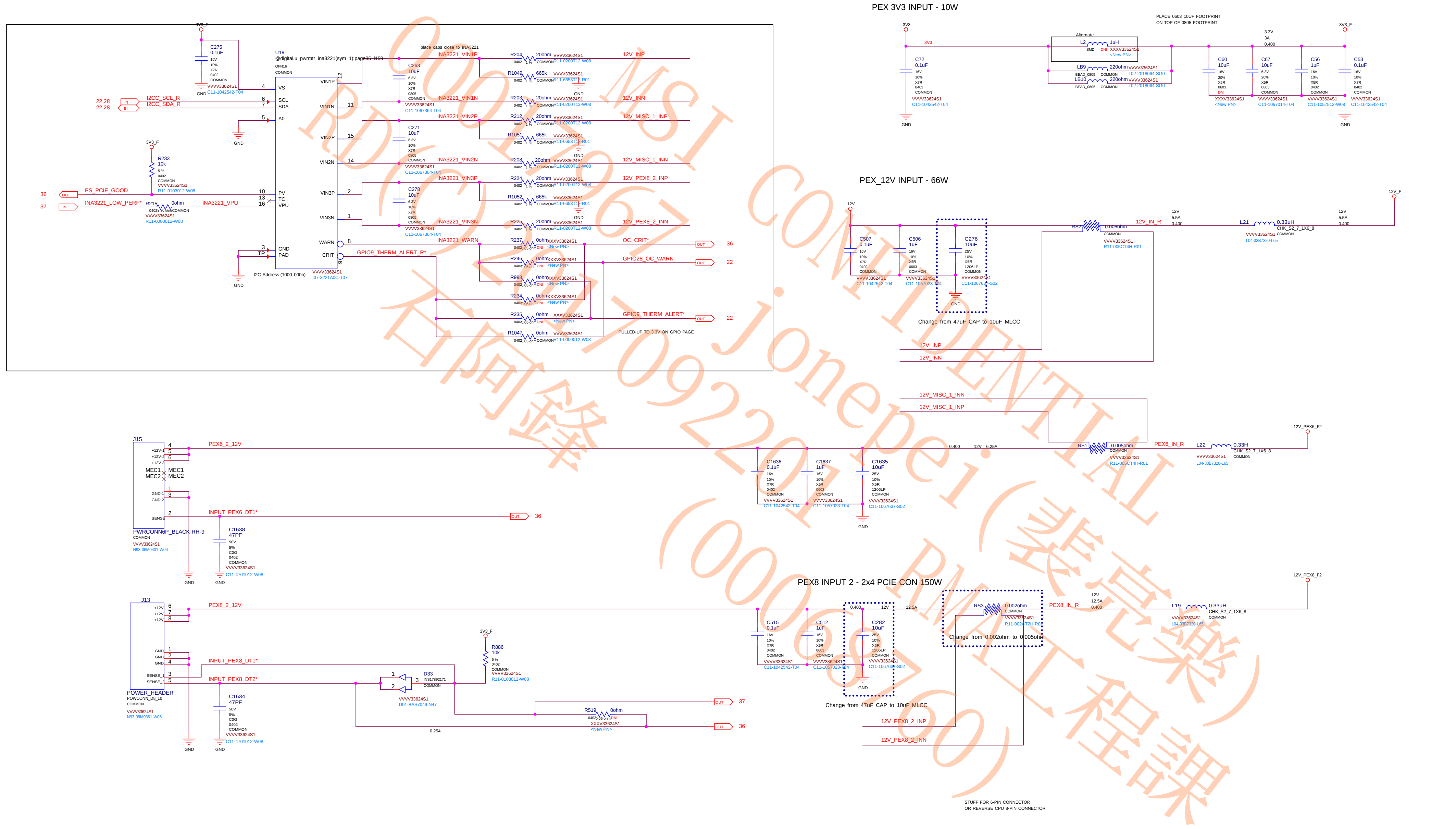
Page35: PS: Inputs, Filtering, and Monitoring



MICRO-STAR INT'L CO.,LTD		
MS-V336		
Size: Custom	Document Description: PS: Inputs, Filtering, and Monitoring	Rev: 3.1
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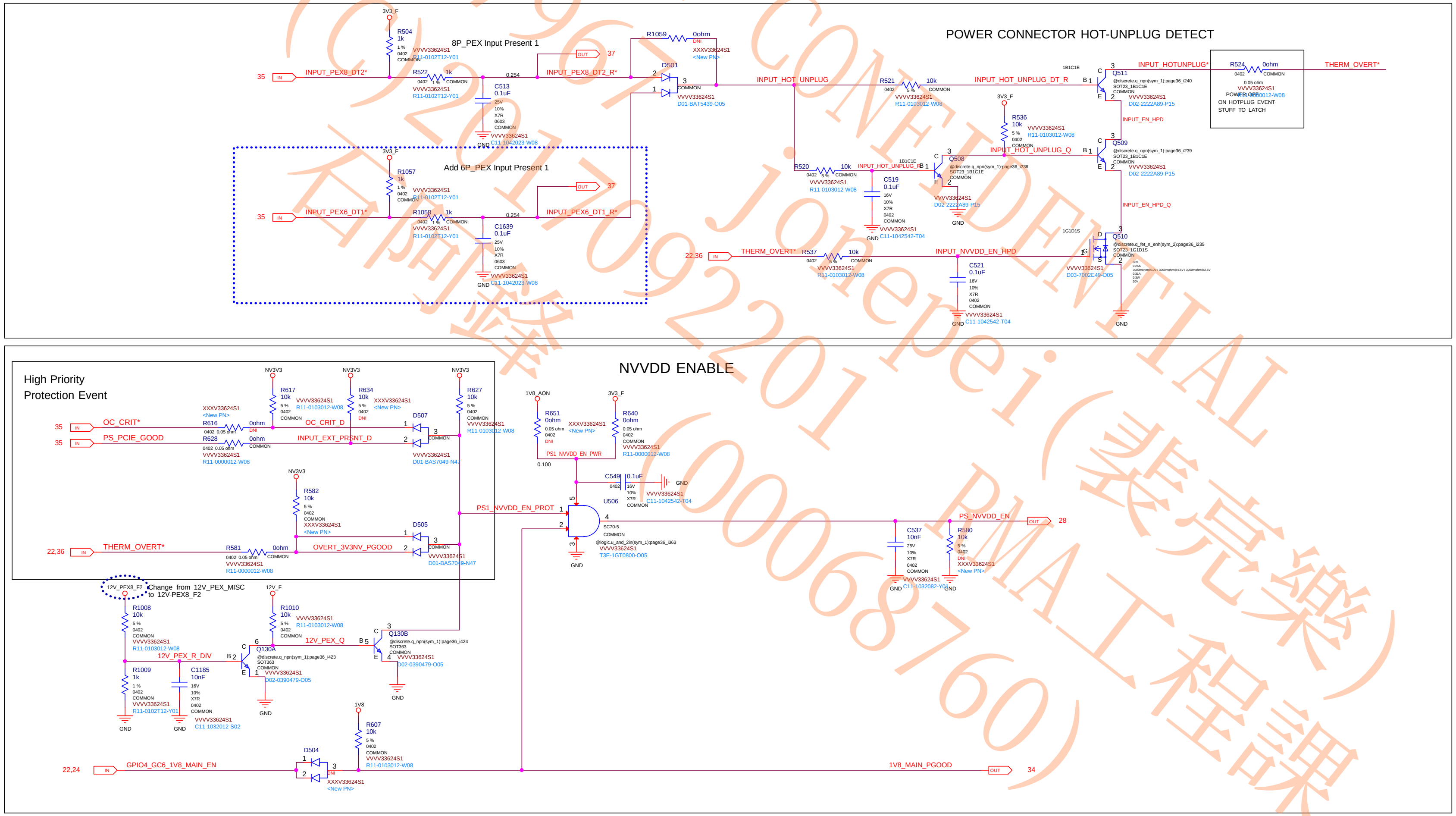
Page36: PS: Shutdown and Sequencing



POWER CONNECTOR HOT-UNPLUG DETECT
8P_PEX Input Present 1
Add 6P_PEX Input Present 1
INPUT_PEX8_DT2*
INPUT_PEX8_DT2_R*
INPUT_PEX6_DT1*
INPUT_PEX6_DT1_R*
INPUT_HOT_UNPLUG
INPUT_HOT_UNPLUG_DT_R
INPUT_HOTUNPLUG*
THERM_OVERT*
INPUT_EN_HPD
INPUT_HOT_UNPLUG_Q
INPUT_EN_HPD_Q
INPUT_NVVDD_EN_HPD
POWER OFF ON HOTPLUG EVENT STUFF TO LATCH
NVVDD ENABLE
High Priority Protection Event
OC_CRIT*
PS_PCIE_GOOD
OC_CRIT_D
INPUT_EXT_PRSNT_D
OVERT_3V3NV_PGOOD
PS1_NVVDD_EN_PROT
PS1_NVVDD_EN_PWR
PS_NVVDD_EN
Change from 12V_PEX_MISC to 12V-PEX8_F2
12V_PEX_R_DIV
12V_PEX_Q
GPIO4_GC6_1V8_MAIN_EN
1V8_MAIN_PGOOD

MICRO-STAR INT'L CO.,LTD

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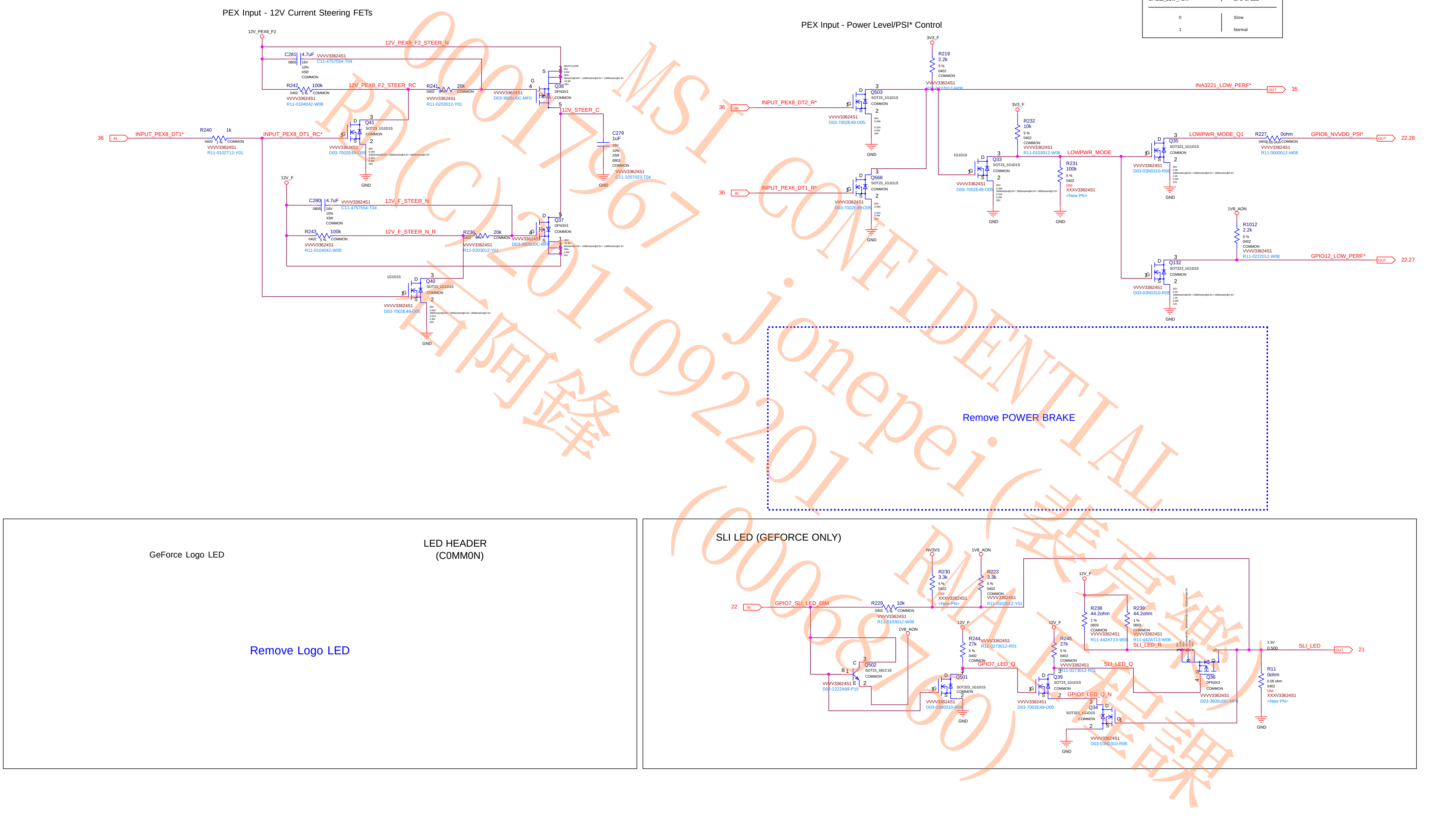
Size	Document Description	Rev
Custom	PS: Shutdown and Sequencing	3.1

Date: Thursday, July 07, 2016 Sheet 36 of 40

Page37: PS: 12V Current Steering, PSI Control, and LED



PEX Input - 12V Current Steering FETs
12V_PEX8_F2
12V_PEX8_F2_STEER_N
12V_PEX8_F2_STEER_RC
INPUT_PEX8_DT1*
INPUT_PEX8_DT1_RC*
12V_STEER_C
12V_F
12V_F_STEER_N
12V_F_STEER_N_R
C281 4.7uF
C280 4.7uF
C279 1uF
R240 1k
R241 20k
R242 100k
R243 100k
R235 20k
Q38
Q37
Q40
Q41
GND
PEX Input - Power Level/PSI* Control
GPIO12_LOW_PERF*
GPU SPEED
0
Slow
1
Normal
3V3_F
R219 2.2k
INA3221_LOW_PERF*
INPUT_PEX8_DT2_R*
INPUT_PEX6_DT1_R*
Q503
Q568
Q33
Q35
Q132
R232 10k
R231 100k
LOWPWR_MODE
LOWPWR_MODE_Q1
R227 0ohm
GPIO6_NVVDD_PSI*
1V8_AON
R1012 2.2k
GPIO12_LOW_PERF*
Remove POWER BRAKE
GeForce Logo LED
LED HEADER
(C0MM0N)
Remove Logo LED
SLI LED (GEFORCE ONLY)
NV3V3
R230 3.3k
R223 3.3k
R229 10k
GPIO7_SLI_LED_DIM
R238 44.2ohm
R239 44.2ohm
R244 27k
R245 27k
Q502
Q501
Q39
Q34
Q36
GPIO7_LED_Q
GPIO7_LED_Q_N
SLI_LED_Q
SLI_LED_R
SLI_LED
R11 0ohm

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MS-V336		
Size: Custom	Document Description: PS: 12V Current Steering, PSI Control, and LED	Rev: 3.1
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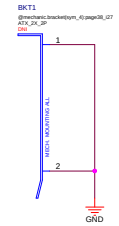
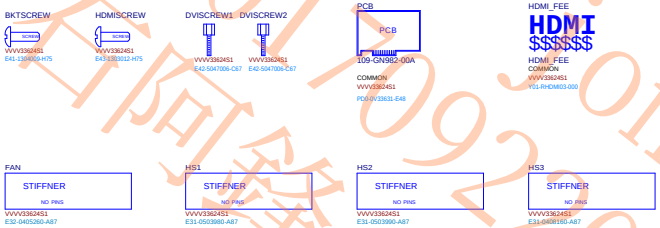
Brackets:





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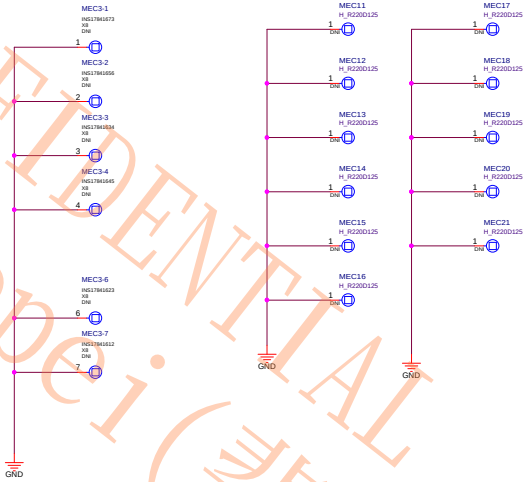

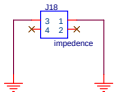

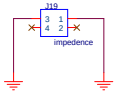

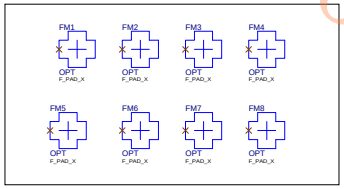

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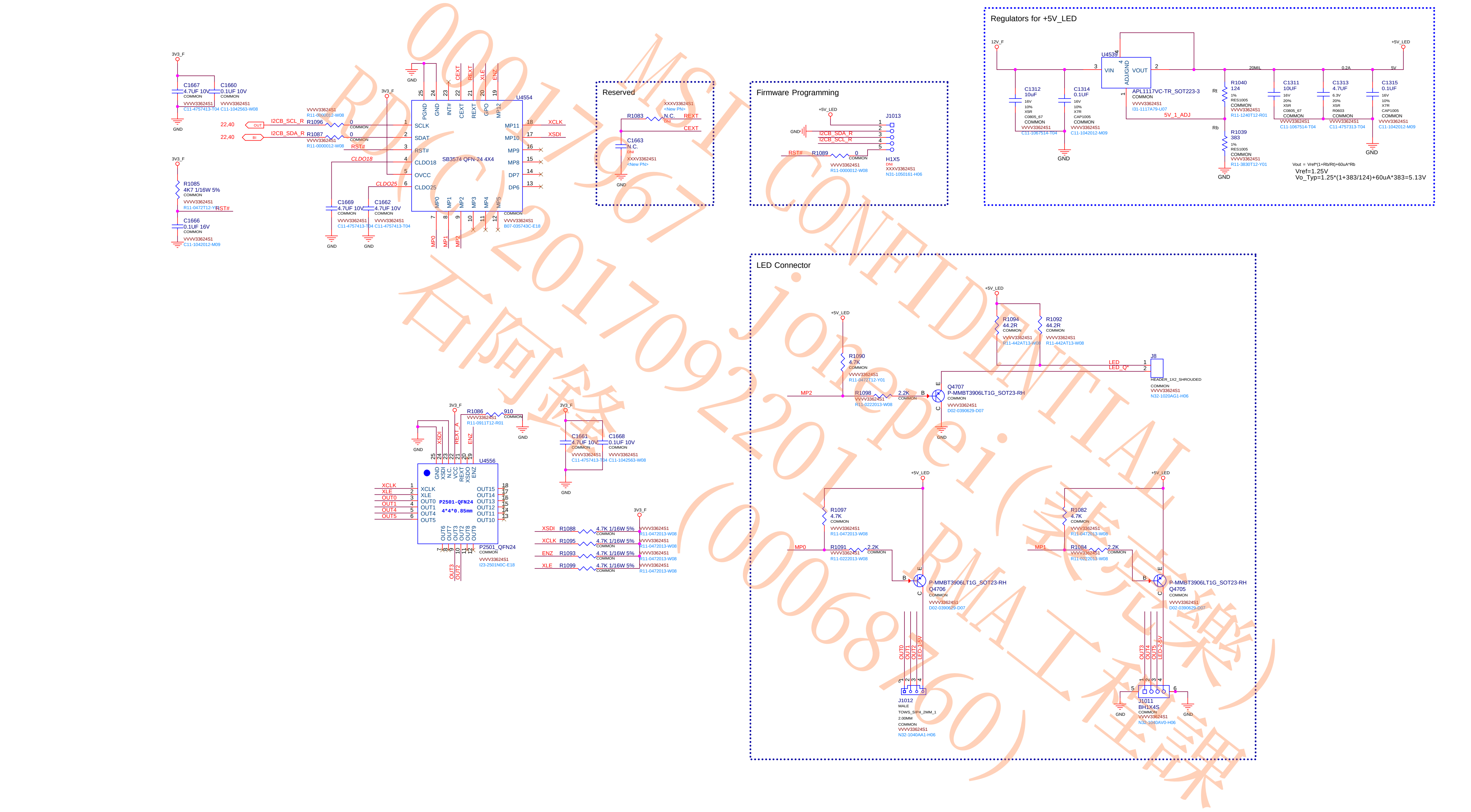

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