PG413 A00

GP104 - 8GB GDDR5X, 256b, 256Mx32
Tall DVI-D + DP + DP + DP/HDMI + DP

TABLE OF CONTENTS

Page	Description
1	Table of Contents
2	Block Diagram
3	PCI Express
4	MEMORY: GPU Partition A/B
5	MEMORY: FBA[31:0]
6	MEMORY: FBA[63:32]
7	MEMORY: FBB[31:0]
8	MEMORY: FBB[63:32]
9	MEMORY: GPU Partition C/D
10	MEMORY: FBC[31:0]
11	MEMORY: FBC[63:32]
12	MEMORY: FBD[31:0]
13	MEMORY: FBD[63:32]
14	GPU PWR and GND
15	GPU Decoupling
16	IFPAB DVI-D-DL
17	IFPE DP
18	IFPEF DP
19	IFPC HDMI 2.0/DP
20	IFPD DP
21	MIOA/B Interface and Frame Lock
22	MISC1; Fan, Thermal, JTAG, GPIO, Stereo
23	MISC2: ROM, XTAL, Straps
24	PS: 1V8, 1V8_AON
25	PS: 5V, PEX_VDD

Page	Description
26	PS: FBVDD
27	PS: NVVDD_OVR8
28	PS: Blank Page
29	PS: NVVDD Phase 1-4
30	PS: NVVDD Phase 5 & 6
31	PS: Blank Page
32	PS: Dynamic Power Balance Phases
33	PS: Dynamic Power Balance Logic
34	PS: NV3V3, NV12V
35	PS: Inputs, Filtering, and Monitoring
36	PS: Shutdown and Sequencing
37	PS: 12V Current Steering PSI Control and LED
38	MECH: Bracket/Thermal

V336-3.0	Change List
01	Remove JTAG/POWER BRAKE circuit
14	Remove FBVDD_SENSE_RTN resistor
17	Change DP Library/Footprint
18	Change DP Library/Footprint
19	Change HDMI Library/Footprint Remove co-lay DP
20	Change DP Library/Footprint
21	Remove MIOA/B FRAME LOCK circuit
22	Remove Thermal IC Remove GPIO19_STEREO Circuit Remove Unused GPIO
24	Remove co-lay APW8713AQBI-TRG,BUCK
25	Remove 12V_PEX_MISC option
26	FBVDD controller circuit change to Page 27
28	Copy NVVDD controller circuit from V323-0b
29	Copy driver/MOS circuit from V323-0b
30	Copy driver/MOS circuit from V323-0b
32	Remove Dynamic Power Balance Phases
33	Remove Dynamic Power Balance Phases
34	Remove Unused GPIO circuit
35	Change Input power connector to 6+8
36	Add 6pin POWER CONNECTOR HOT-UNPLUG DETECT
37	Add 6pin PEX Input - Power Level/PSI* Control
39	Add LED_CONTROLLER_ENE3574

V336-3.1	Change List
39	ENE3574 VCC power change to 3V3_F

V336-3.2	Change List
19	Remove co-layout DP RC componets Remove DP_PWR circuit
20	IFPD change to HDMI circuit
22	Remove GPIO4_GC6_1V8_MAIN_EN
24	Remove GPIO4_GC6_1V8_MAIN_EN
25	Co-layout LDO (Option)
29	EXT_12V Input 0603 CAP fooprint change to 0805
35	Remove 3V3 co-Layout Choke
21	Remove MIOA/B FRAME LOCK circuit
22	Remove Thermal IC Remove GPIO19_STEREO Circuit Remove Unused GPIO
24	Remove co-lay APW8713AQBI-TRG,BUCK
25	Remove 12V_PEX_MISC option
36	Remove GPIO4_GC6_1V8_MAIN_EN
38	Change GPU MOUNTING_HOLE

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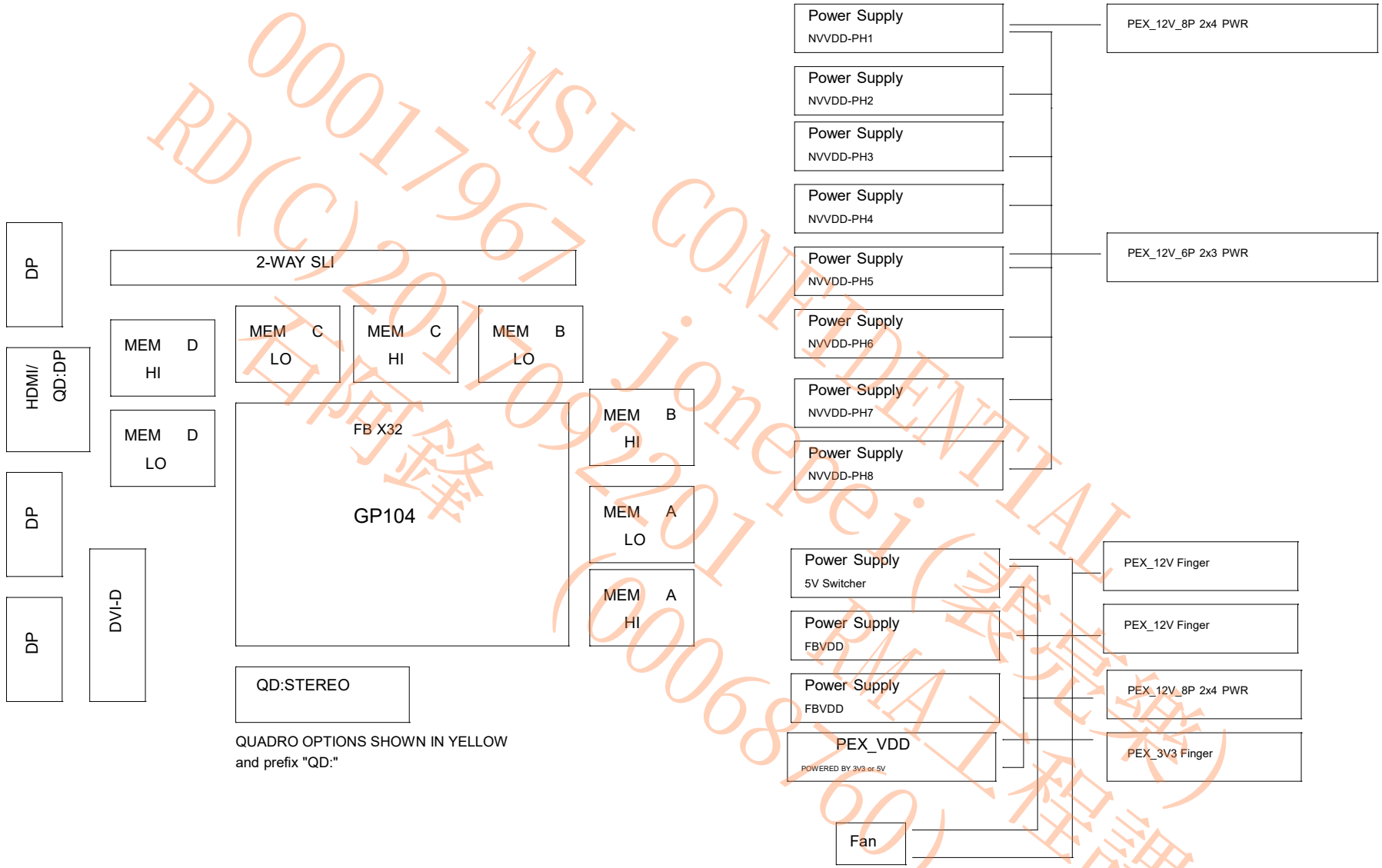
Date: Tuesday, March 28, 2017 | Sheet 1 of 40



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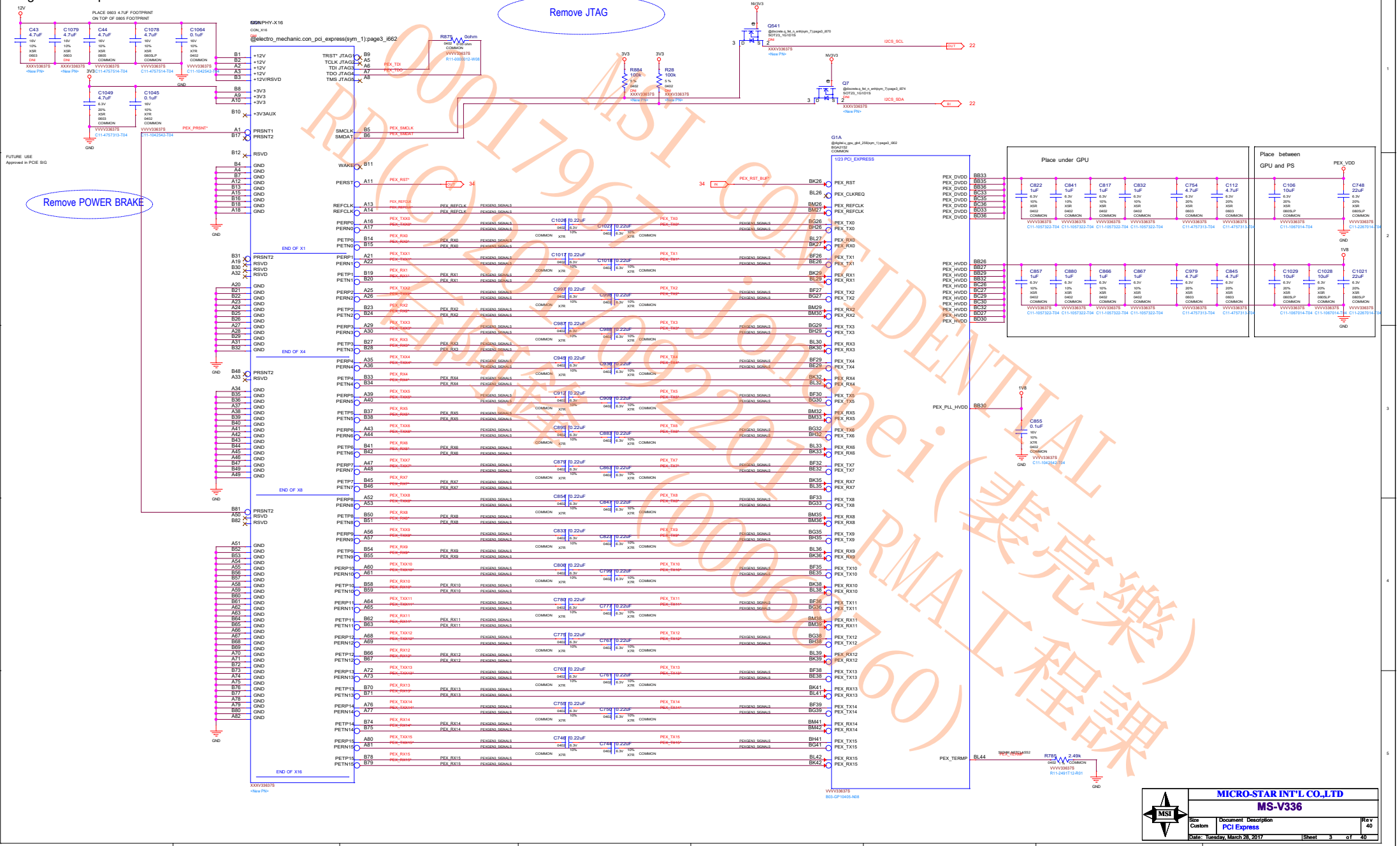
Size: Custom	Document Description: BLOCK DIAGRAM
Rev: 40	
Date: Tuesday, March 28, 2017	Sheet 2 of 40

Page3: PCI Express



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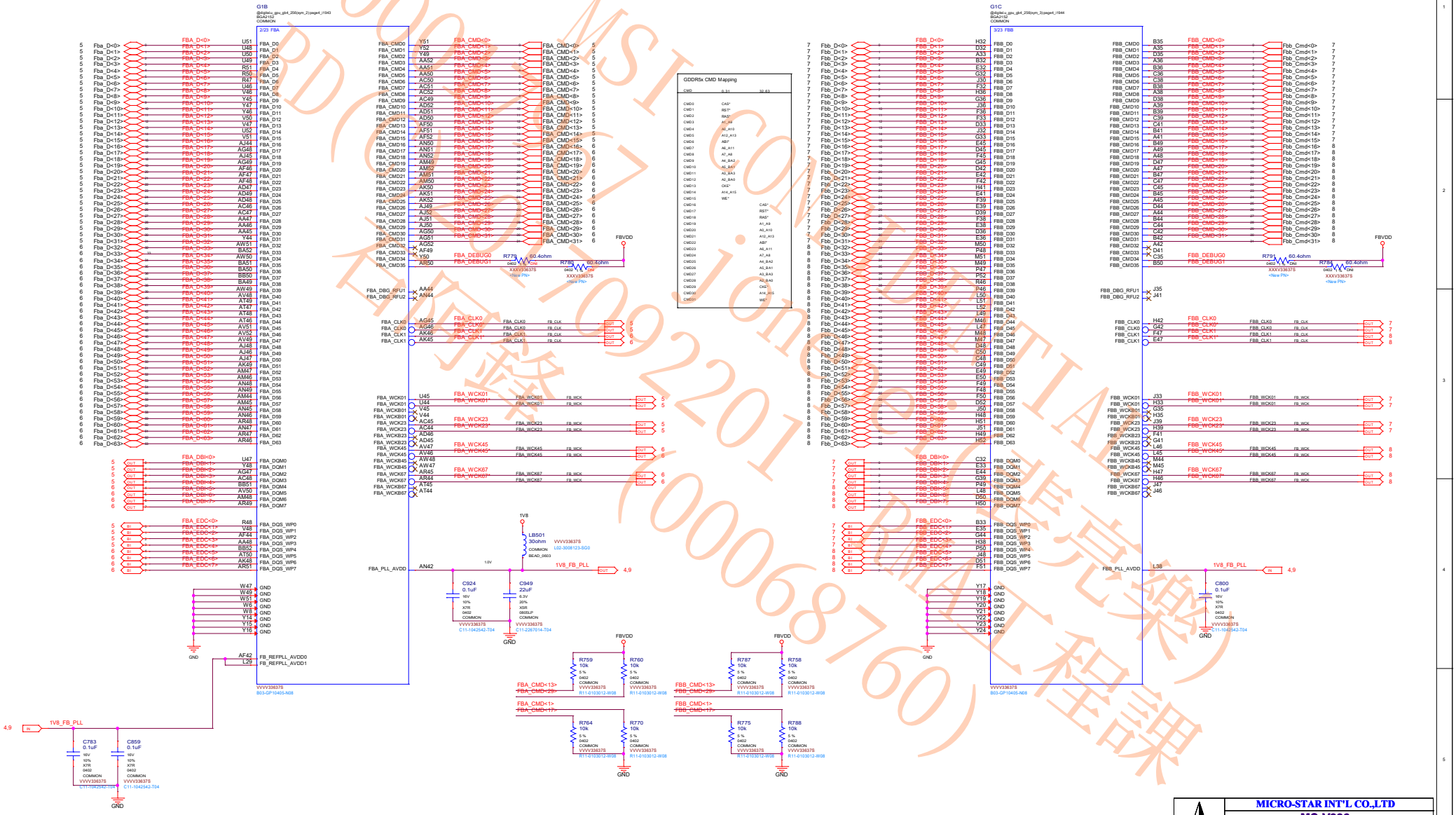
Size: Custom	Document Description: PCI Express
Rev: 40	
Date: Tuesday, March 28, 2017	Sheet 3 of 40

Page4: MEMORY: GPU Partition A/B



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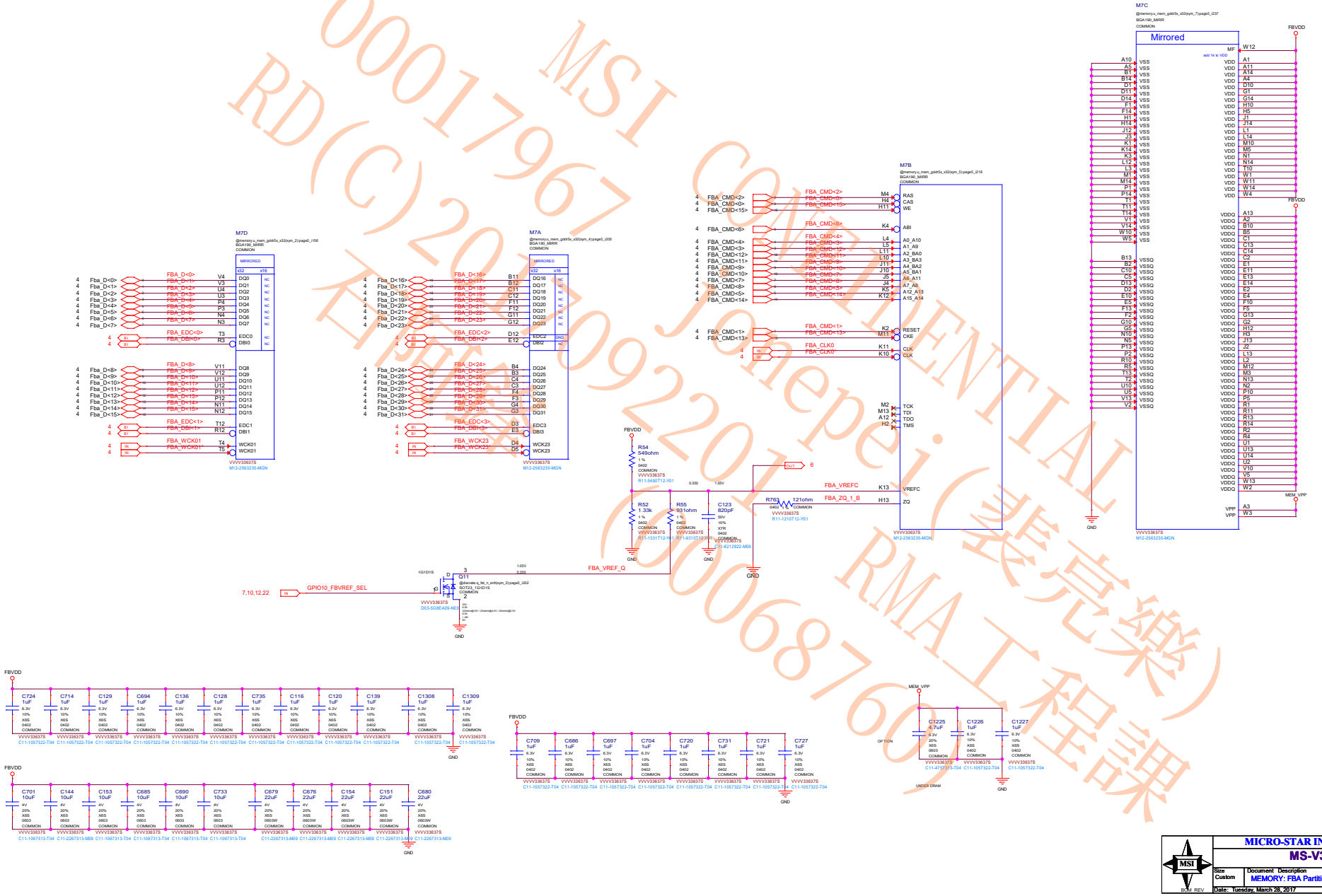
Date: Tuesday, March 28, 2017	Sheet 4 of 40		

Page5: MEMORY: FBA Partition 31..0



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Size: Custom	Document Description: MEMORY: FBA Partition 31..0		Rev: 40
Date: Tuesday, March 28, 2017	Sheet 5 of 40		

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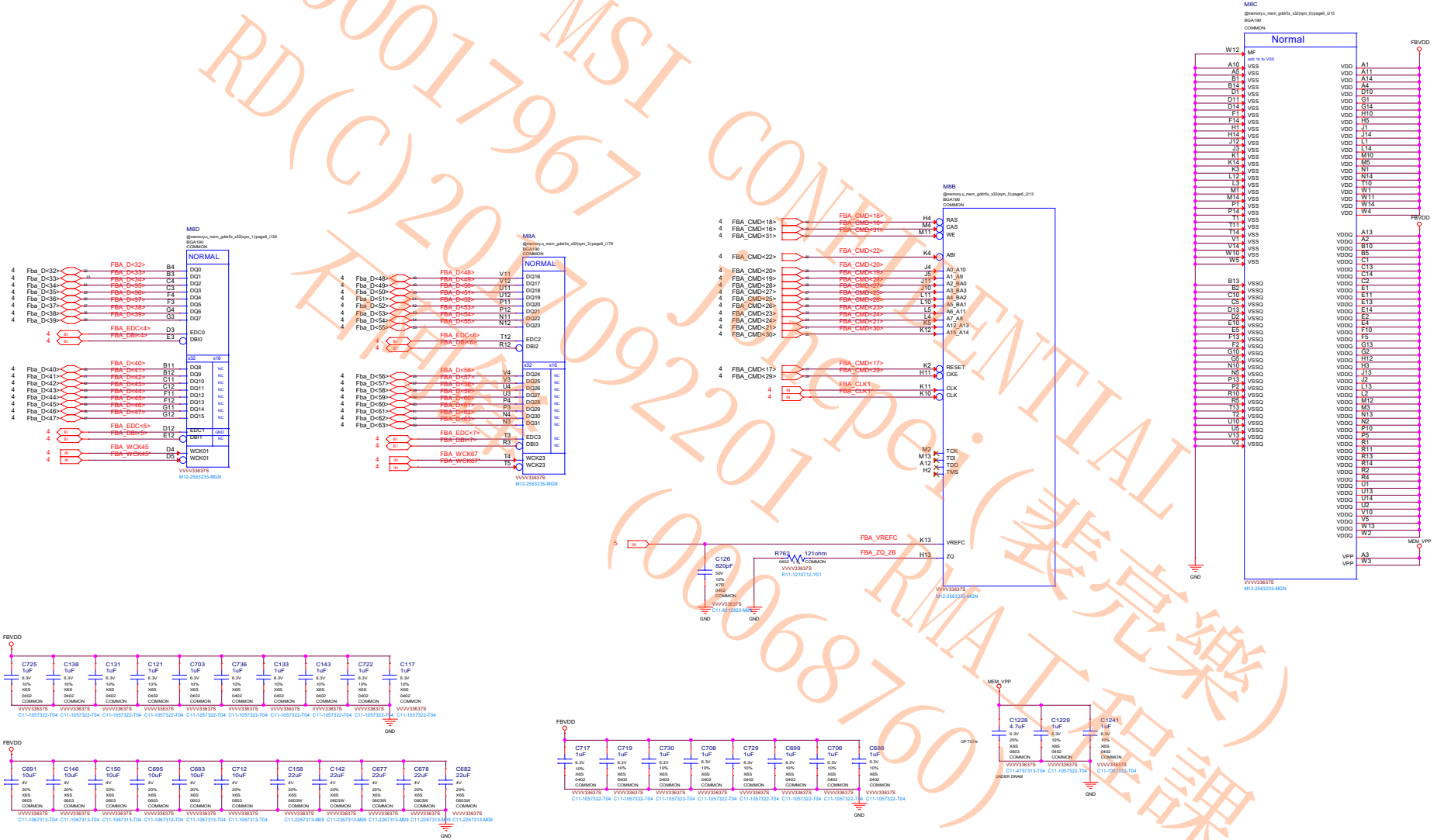

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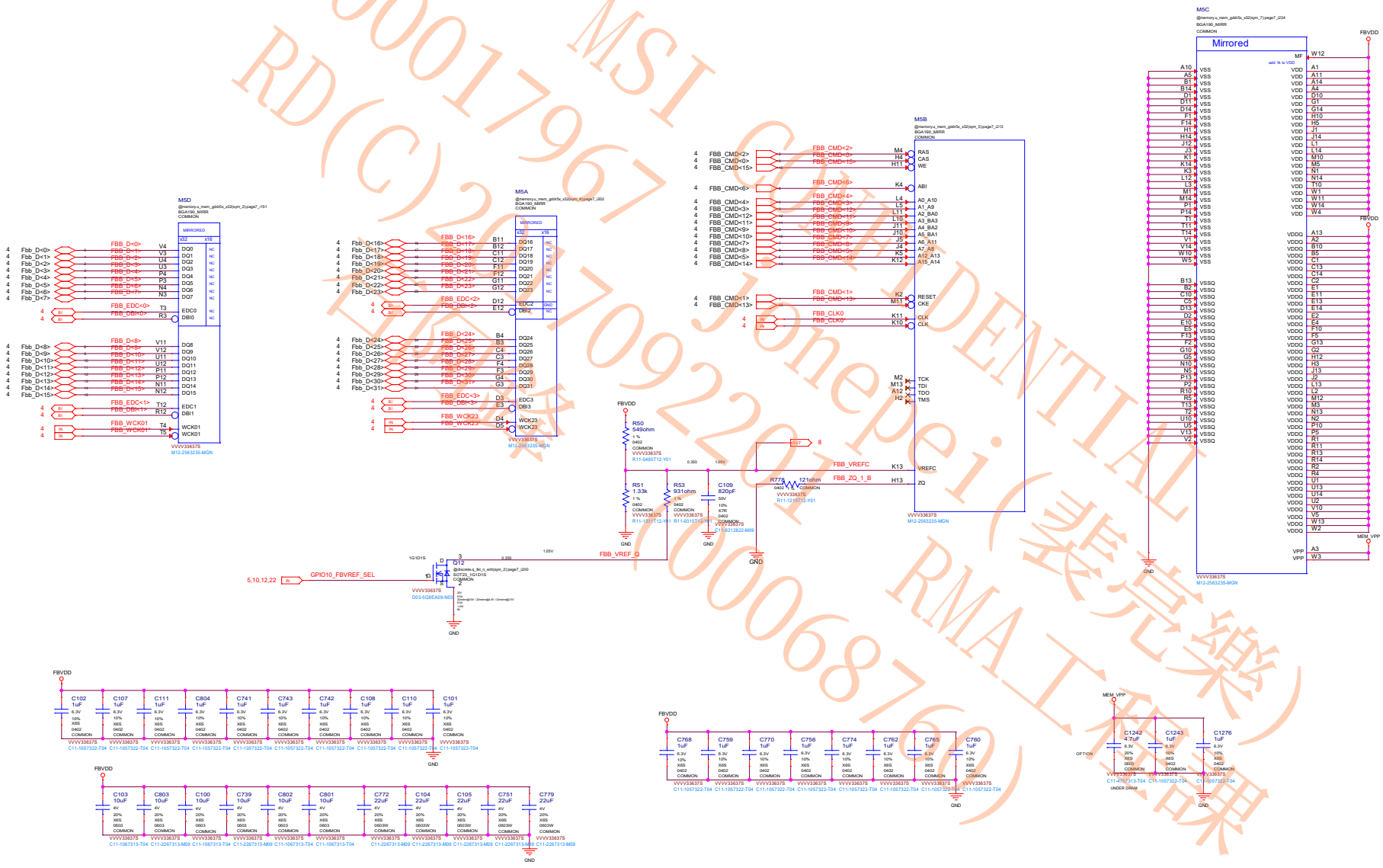
Date: Tuesday, March 28, 2017	Sheet 6 of 40		

Page7: MEMORY: FBB Partition 31..0



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Size: Custom	Document Description: MEMORY: FBB Partition 31..0		Rev: 40
Date: Tuesday, March 28, 2017	Sheet 7 of 40		

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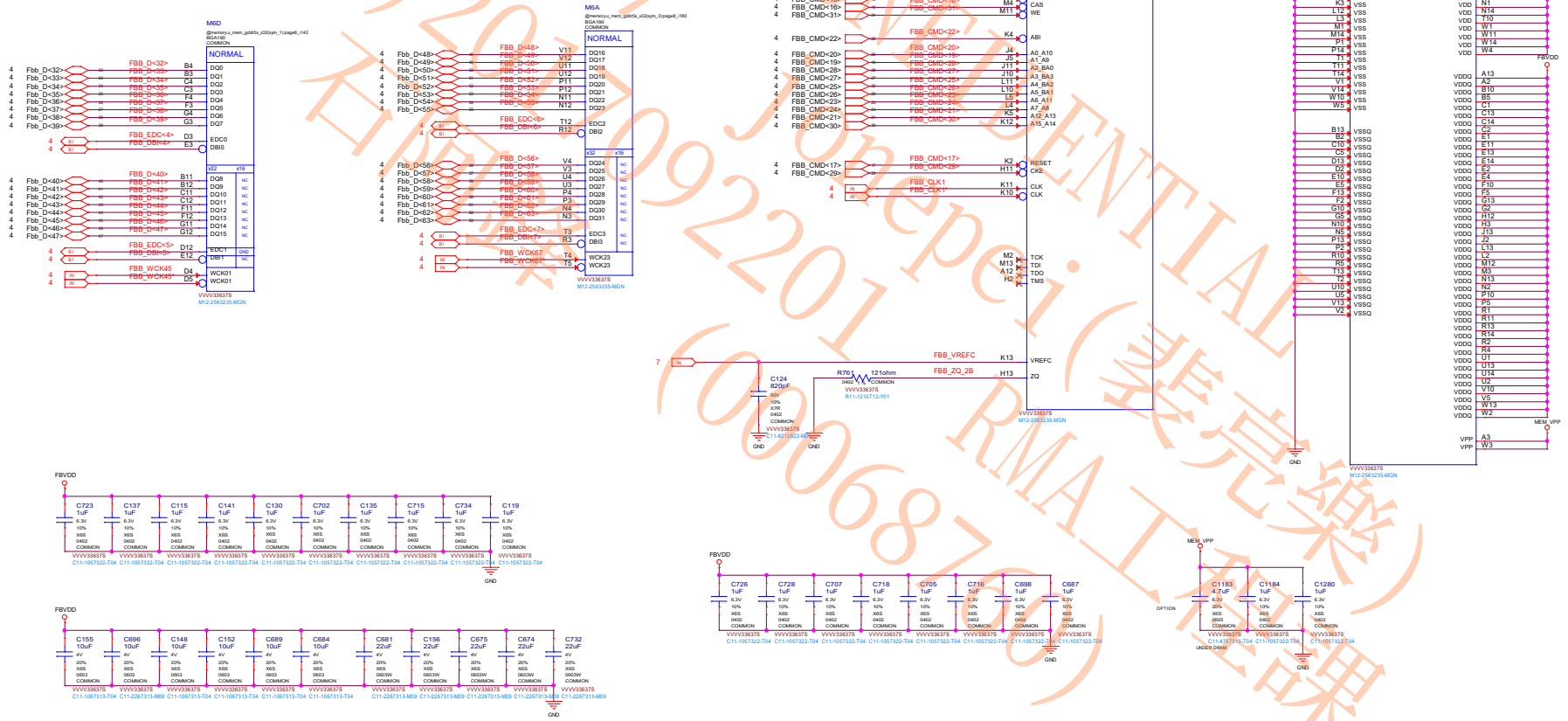

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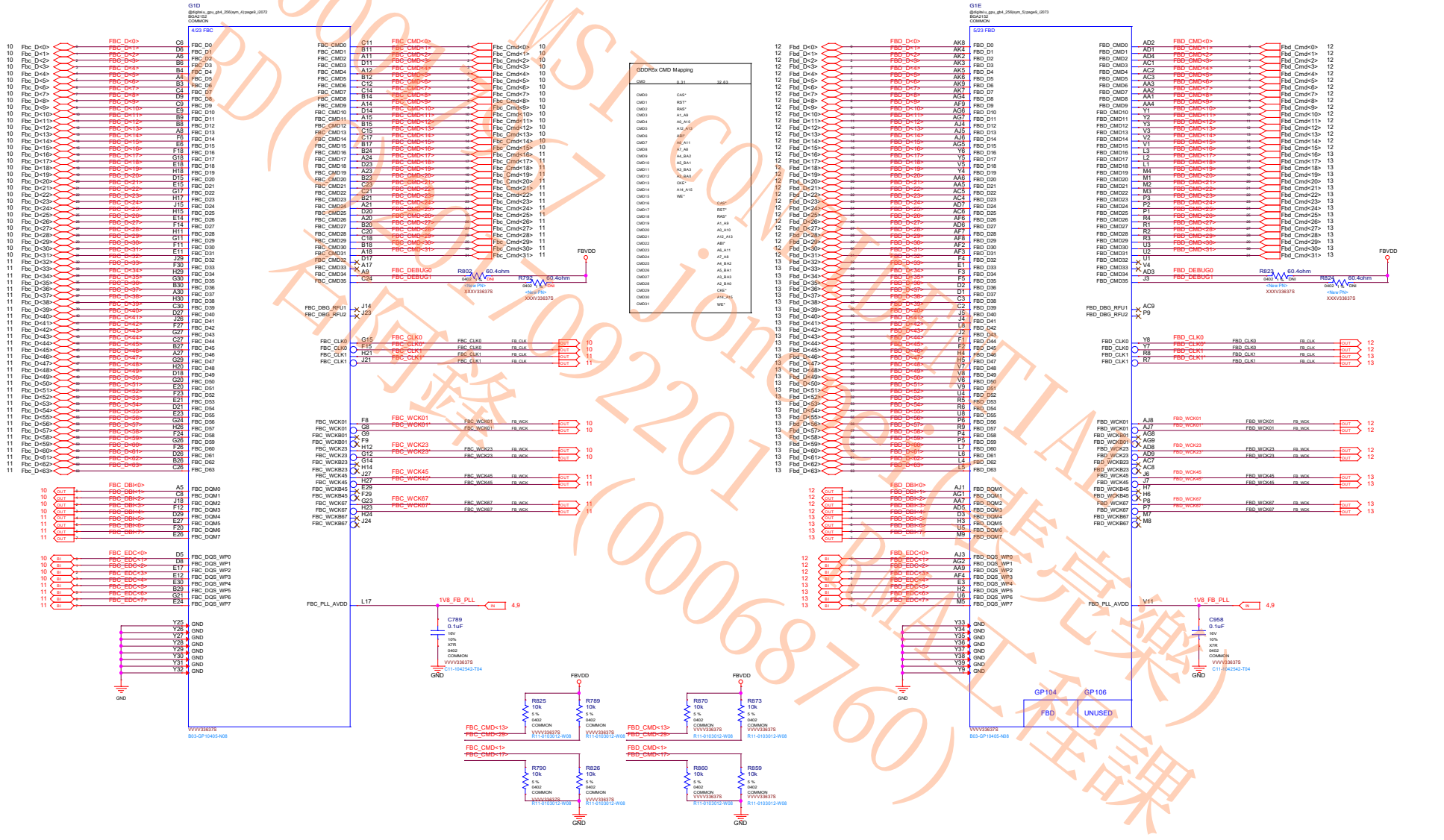
Date: Tuesday, March 28, 2017	Sheet 8 of 40		

Page9: MEMORY: GPU Partition C/D



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Document Description: MEMORY: GPU Partition C/D
Rev: 40
Date: Tuesday, March 28, 2017
Sheet 9 of 40

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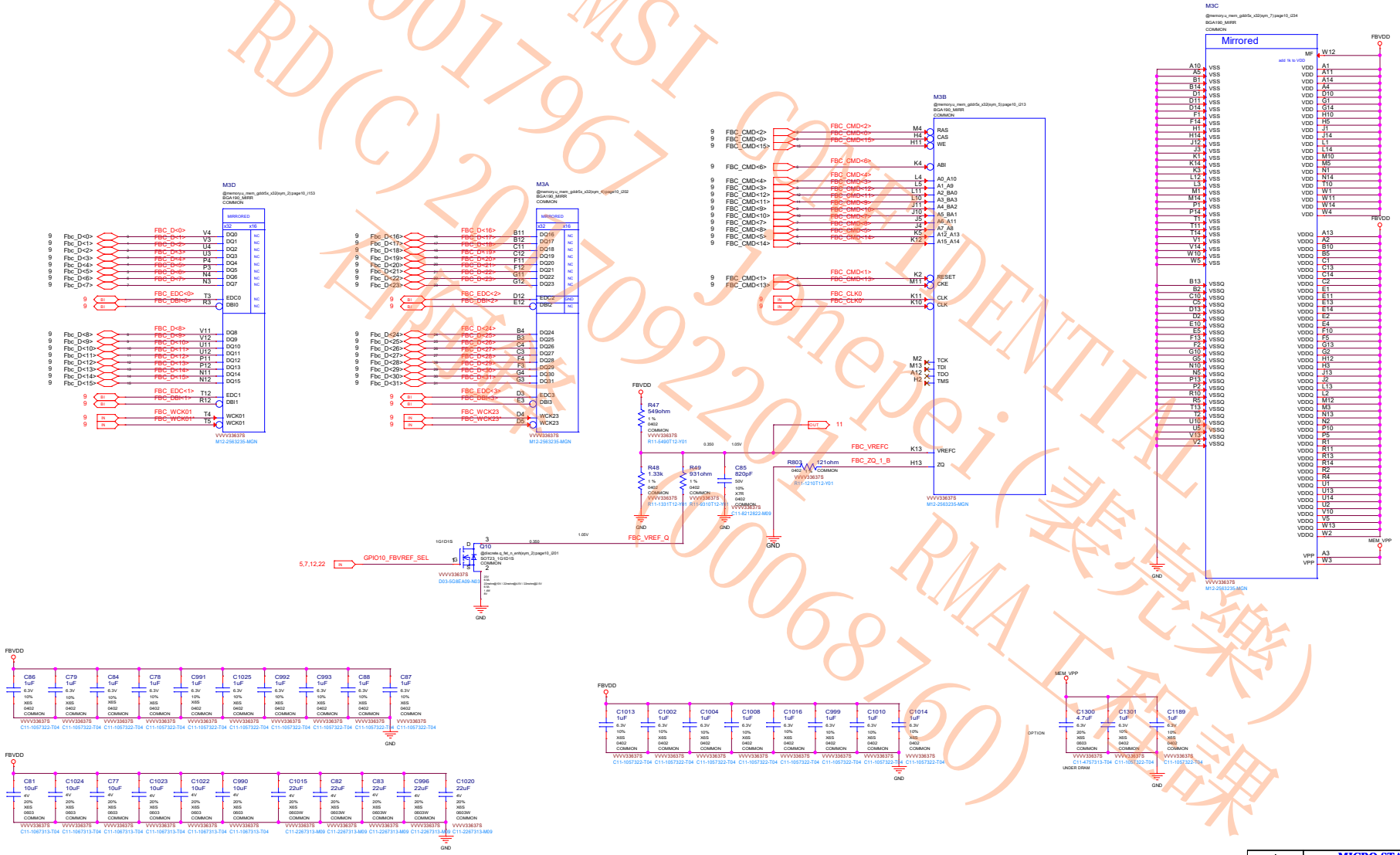

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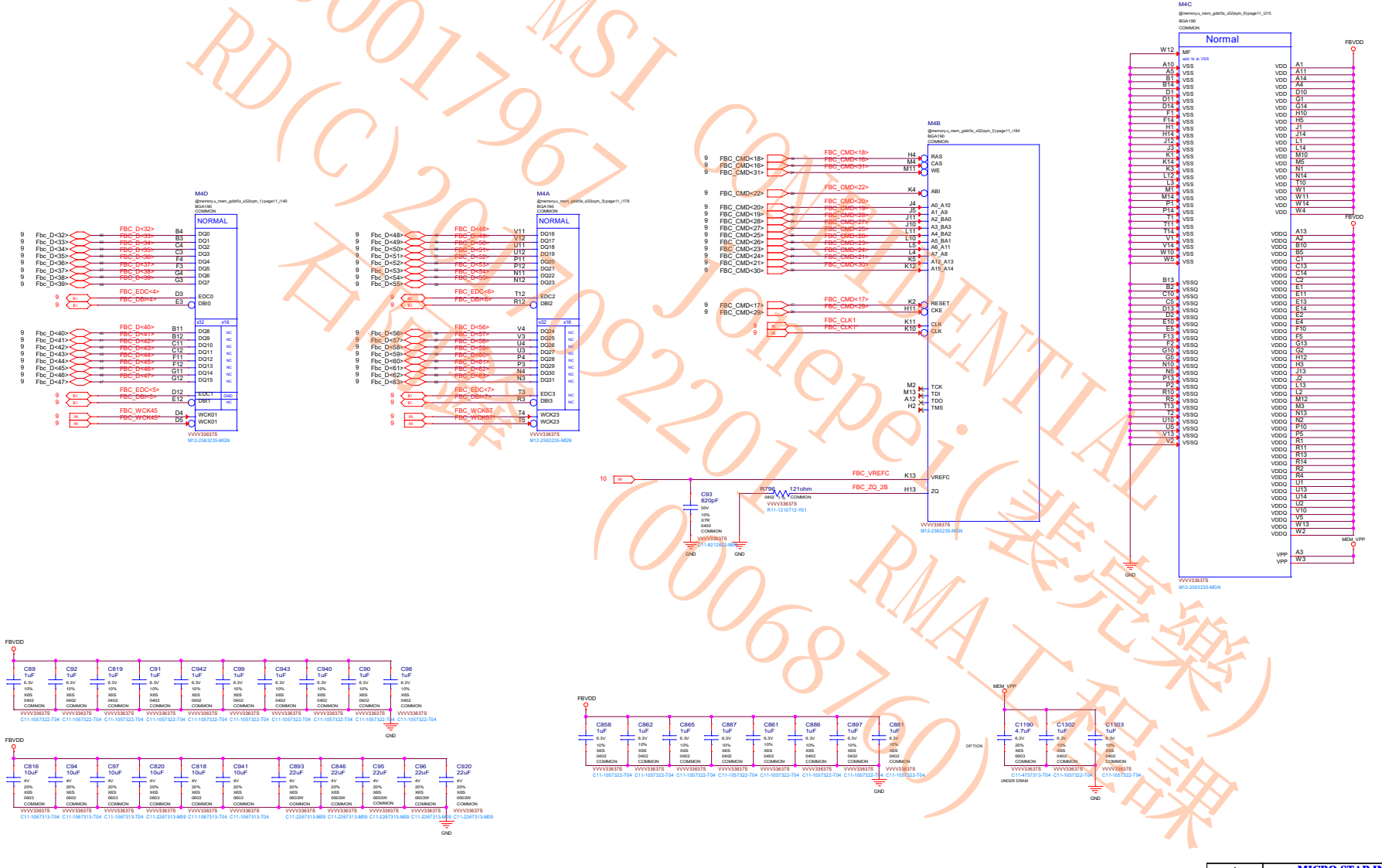
Rev: 40	
Date: Tuesday, March 28, 2017	Sheet 10 of 40

Page11: MEMORY: FBC Partition 63..32



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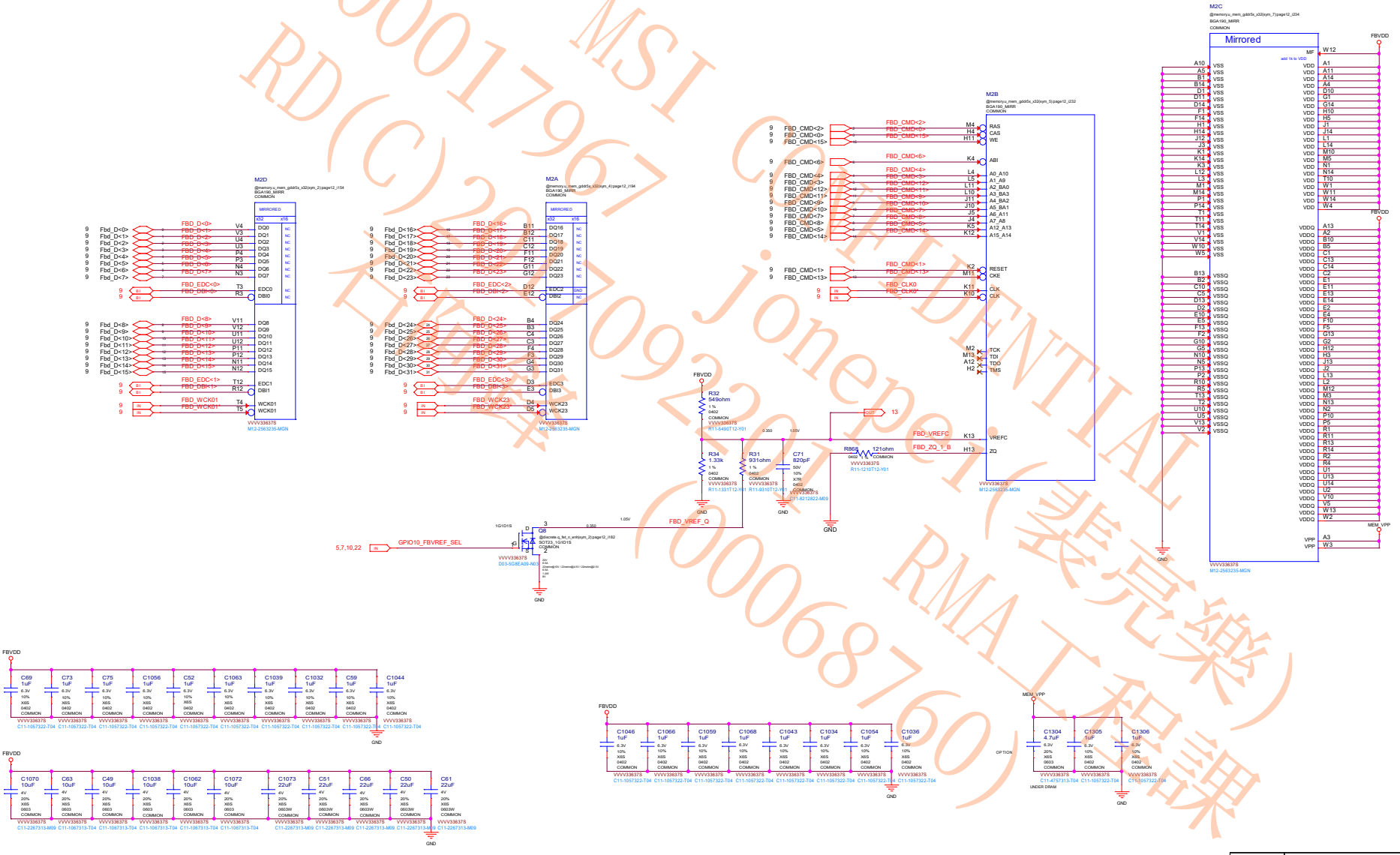
Date: Tuesday, March 28, 2017	Sheet 11 of 40	



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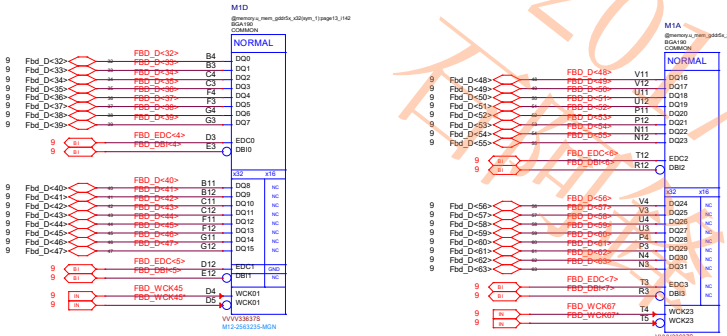
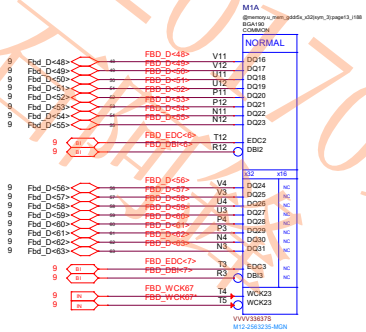
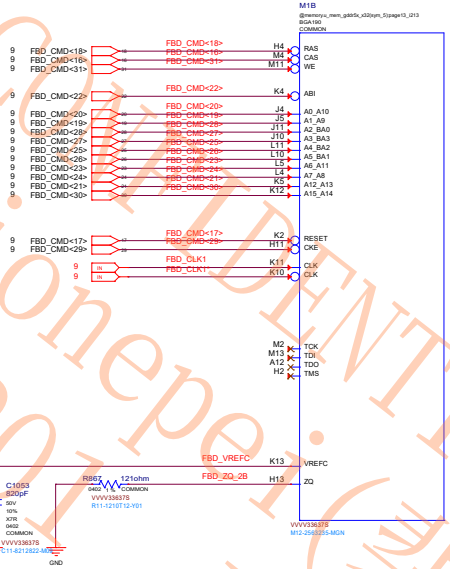
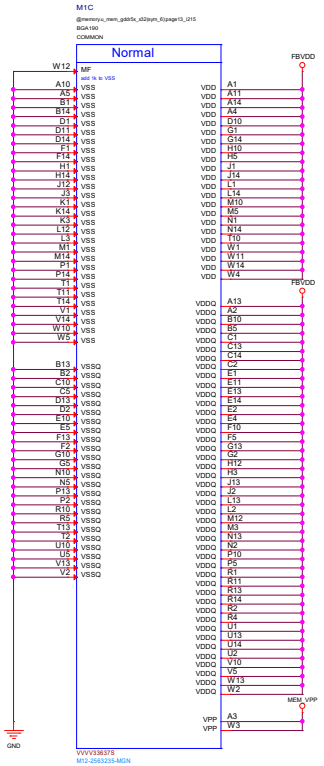
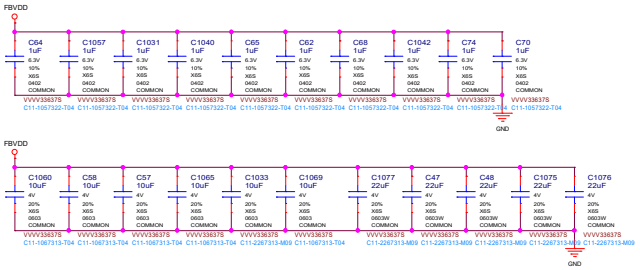
Page13: MEMORY: FBD Partition 63..32

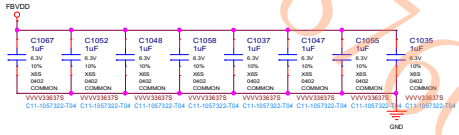


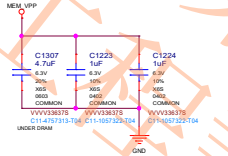












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Size: Custom	Document Description: MEMORY: FBD Partition 63..32	Rev: 40
Date: Tuesday, March 28, 2017	Sheet 13 of 40	

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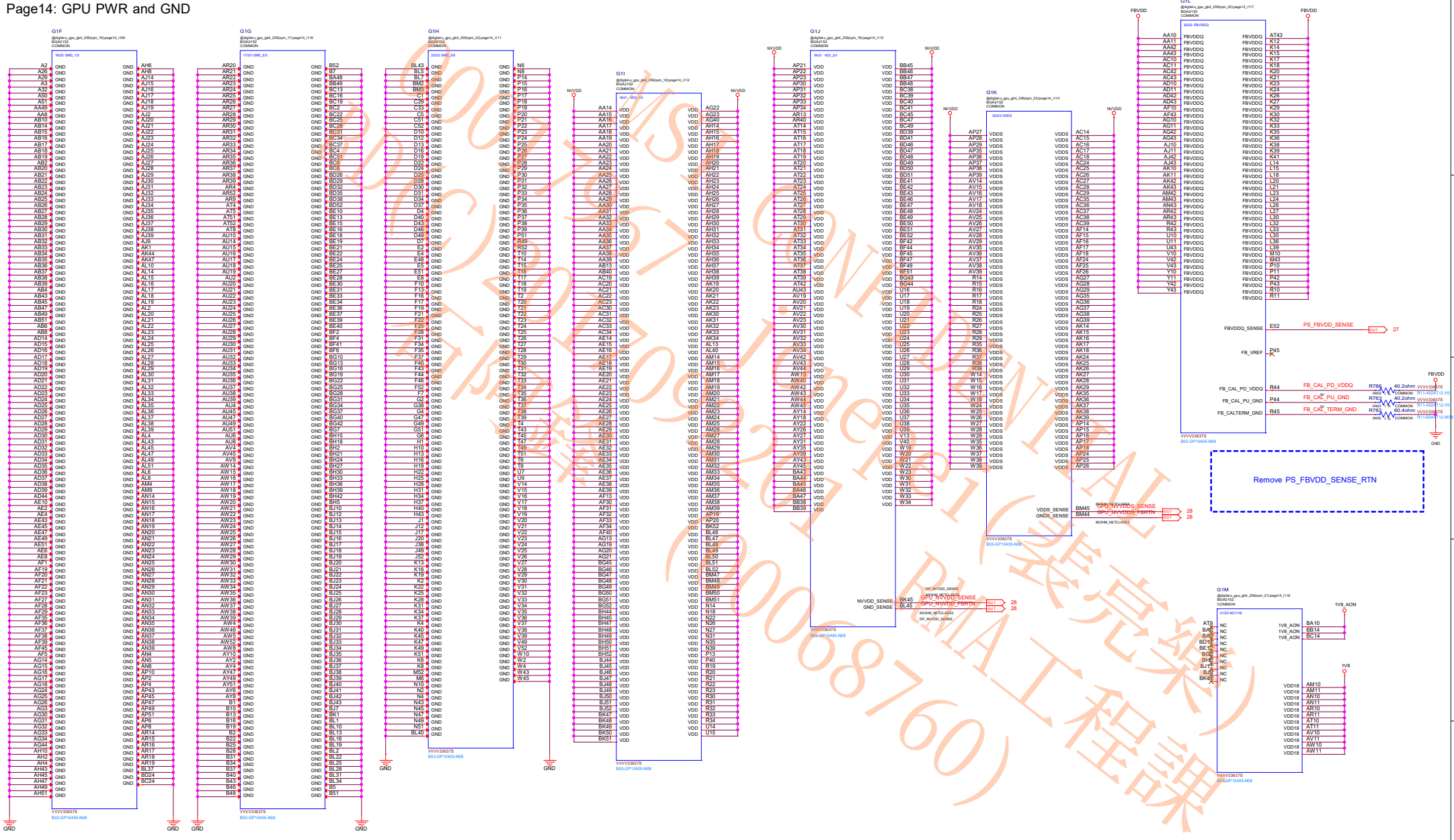
Page14: GPU PWR and GND



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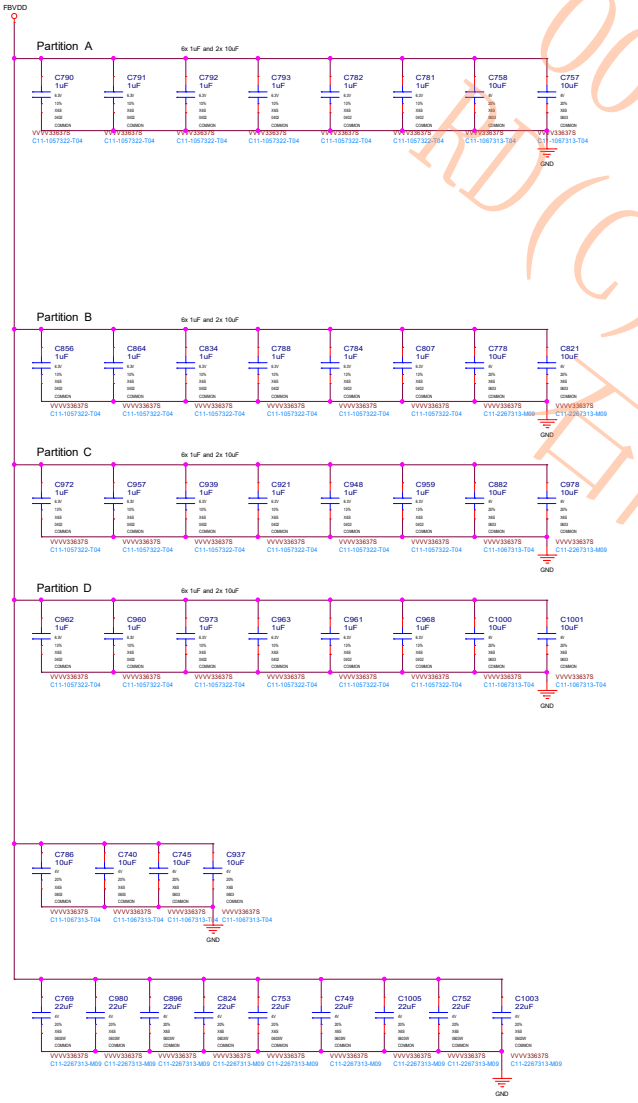
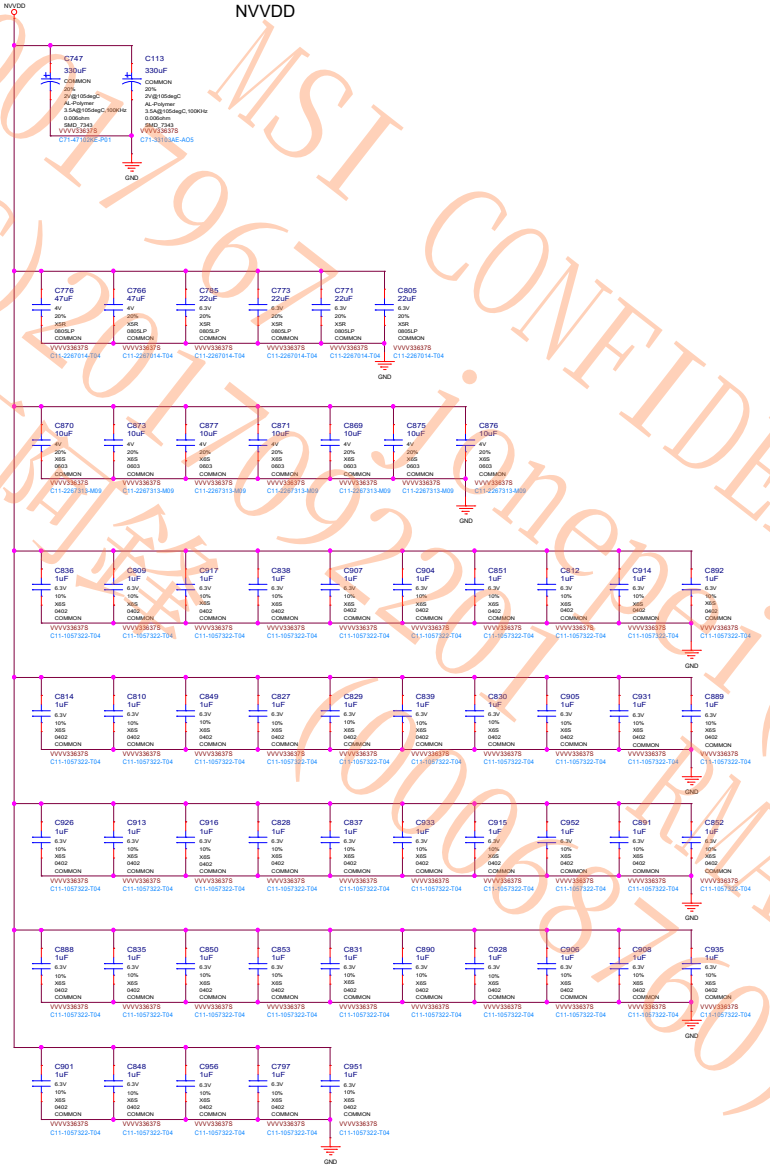
Size Custom
Document Description GPU PWR and GND
Rev 40
Date: Tuesday, March 28, 2017
Sheet 14 of 40

Page15: GPU Decoupling

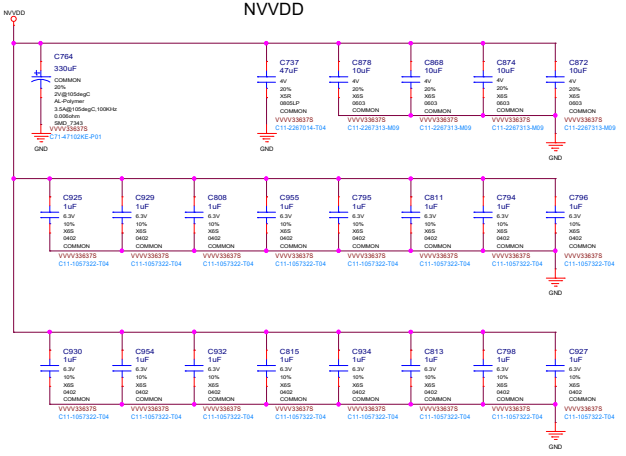
FBVDD

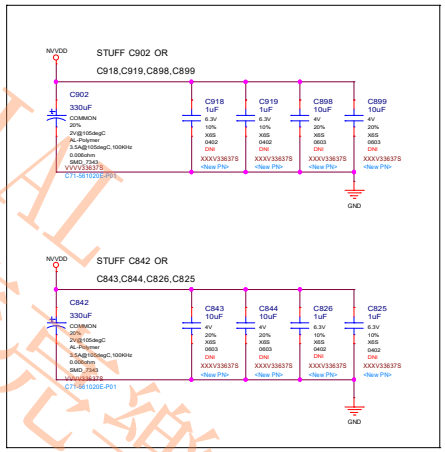


NVVDD



NVVDD





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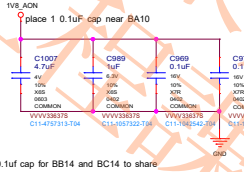
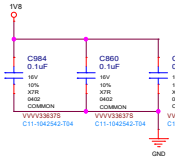


place 1 0.1uf cap for BB14 and BC14 to share

VDD18



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Size: Custom	Document Description: GPU Decoupling	Rev: 40
Date: Tuesday, March 28, 2017	Sheet 15 of 40	

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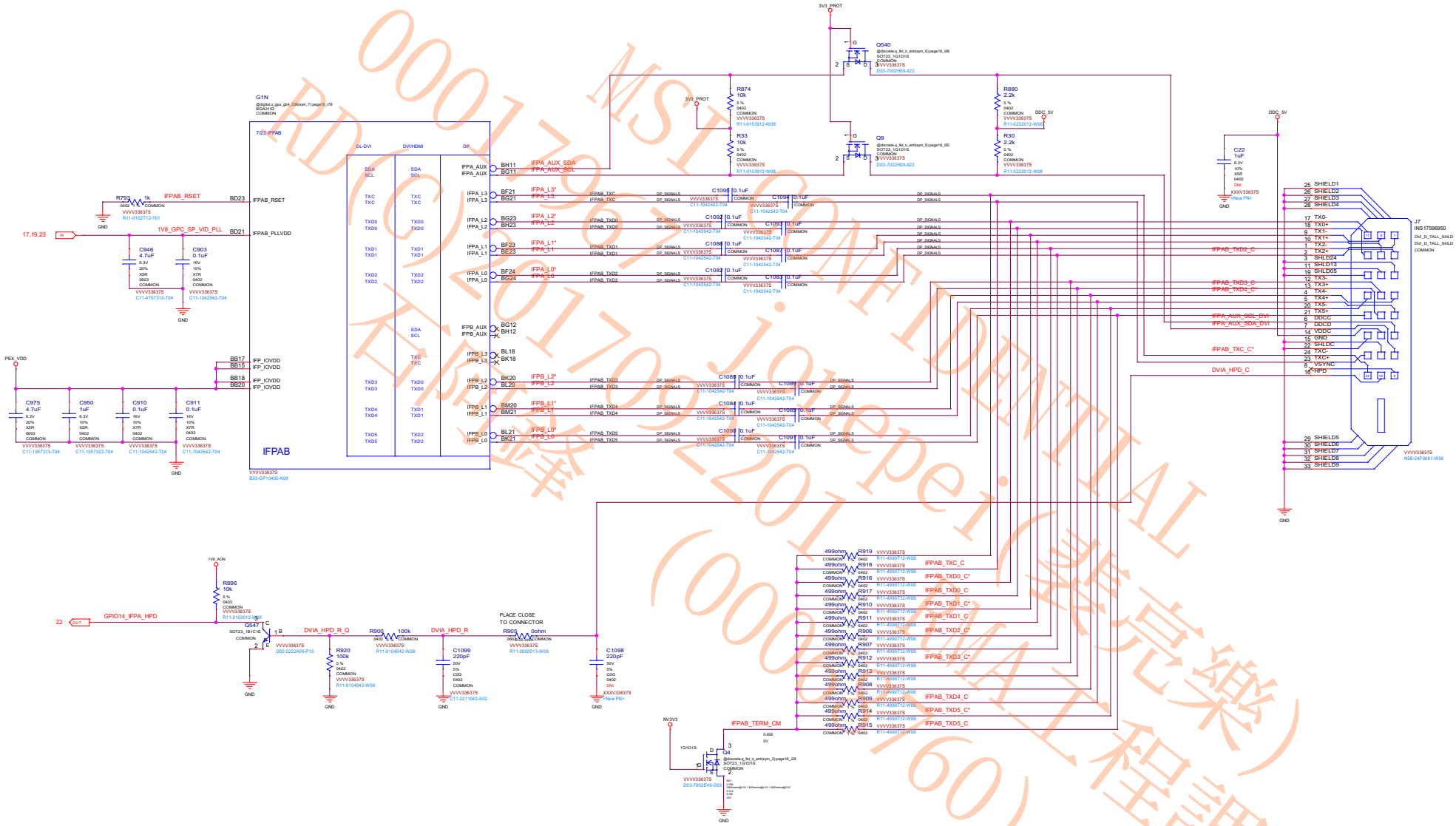

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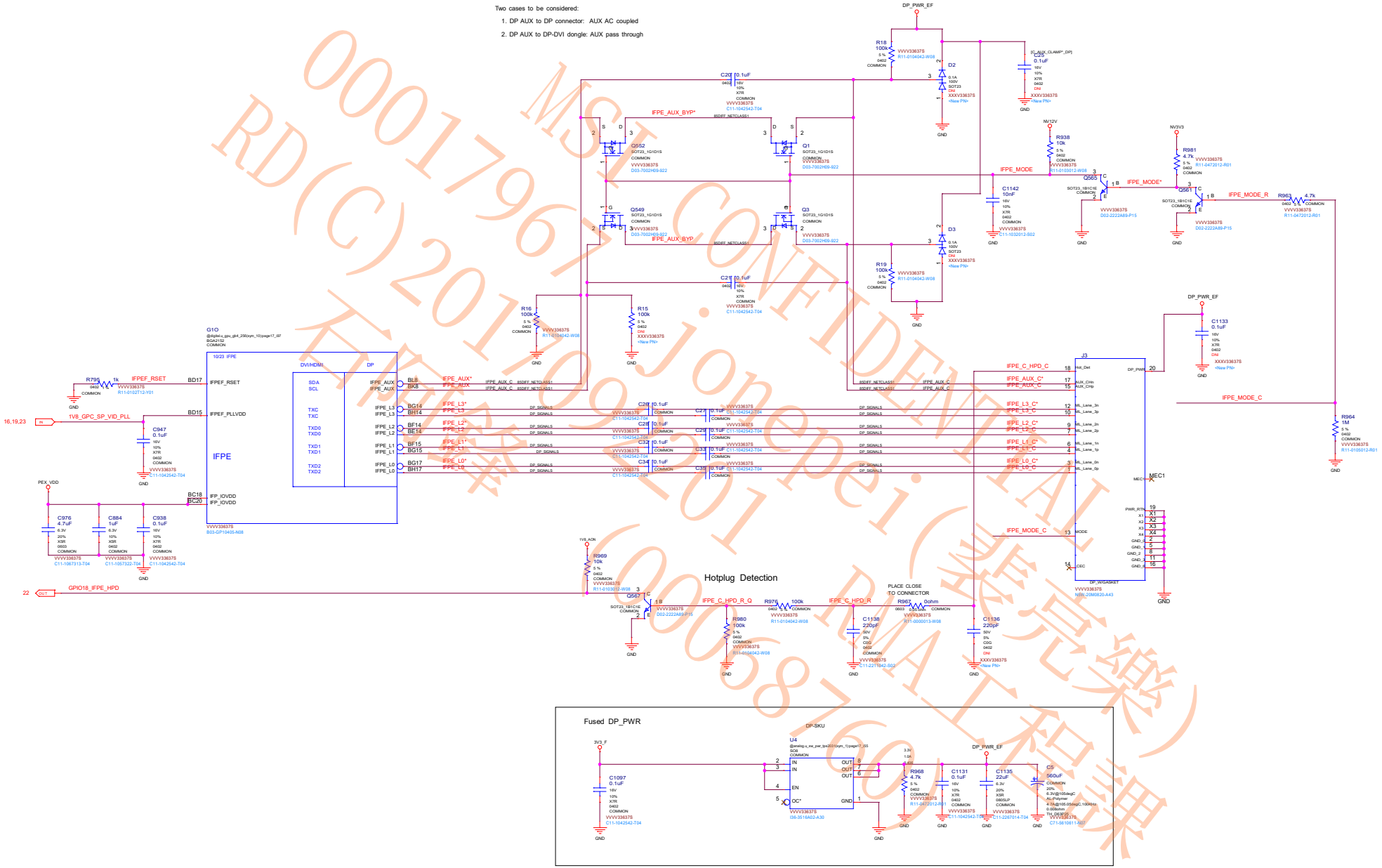
Size: Custom	Document Description: IFPAB DVI-D-DL	Rev: 40
Date: Tuesday, March 28, 2017	Sheet 16 of 40	

Page17: IFPE DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



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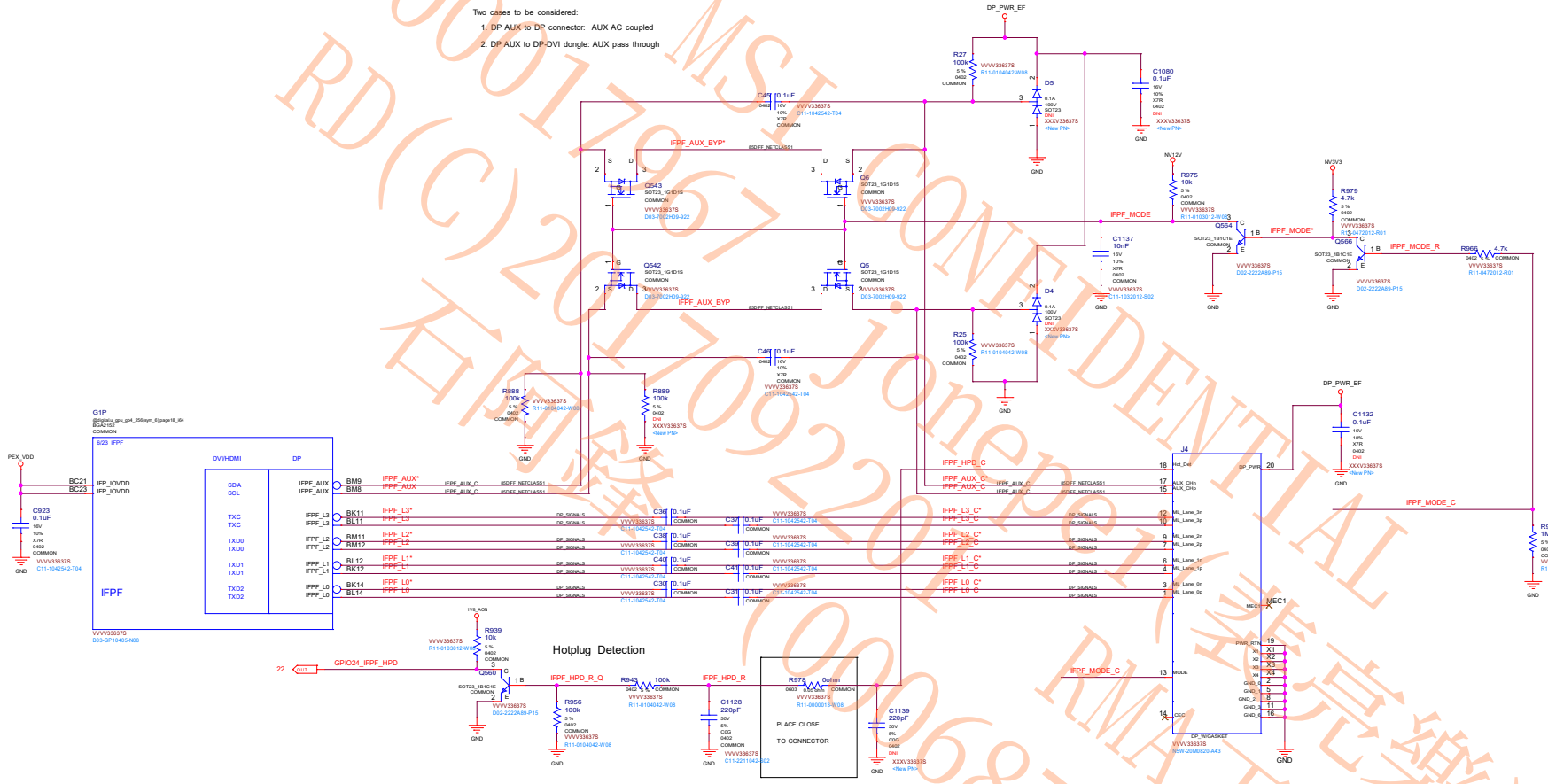
Size: Custom	Document Description: IFPE DP	Rev: 40
Date: Tuesday, March 28, 2017	Sheet 17 of 40	

Page18: IFPF DP



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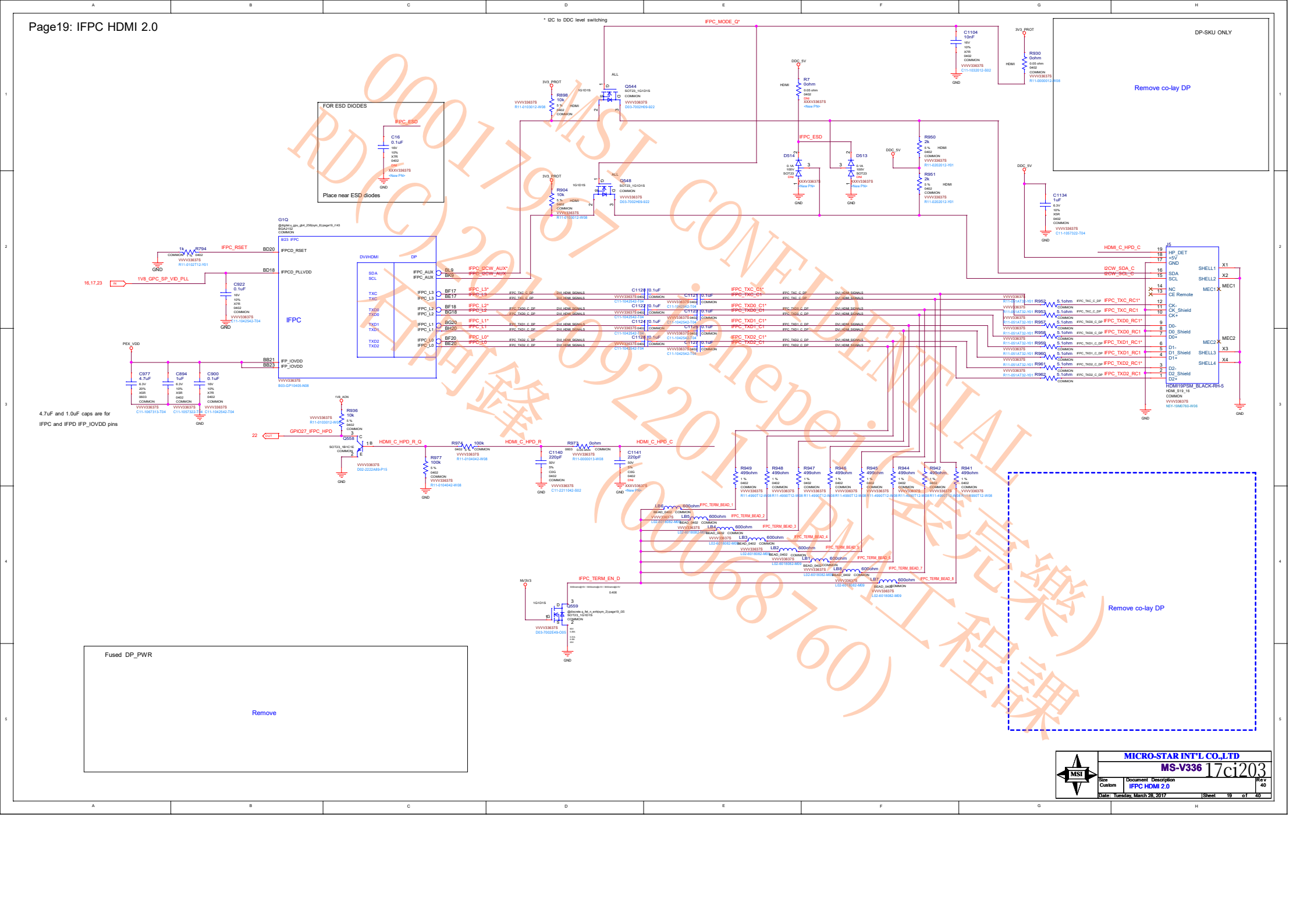
Page19: IFPC HDMI 2.0



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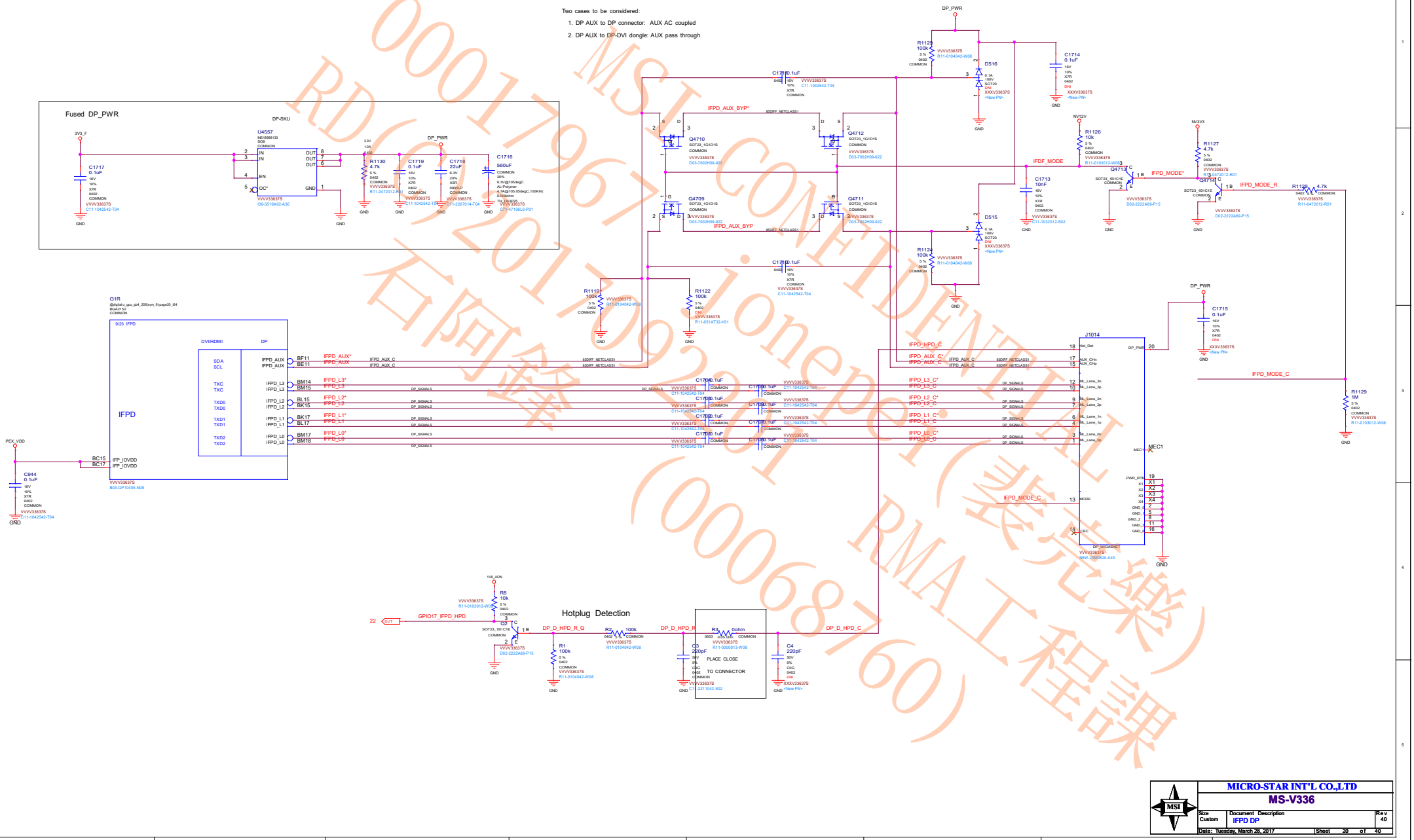
Page20: IFPD HDMI 2.0



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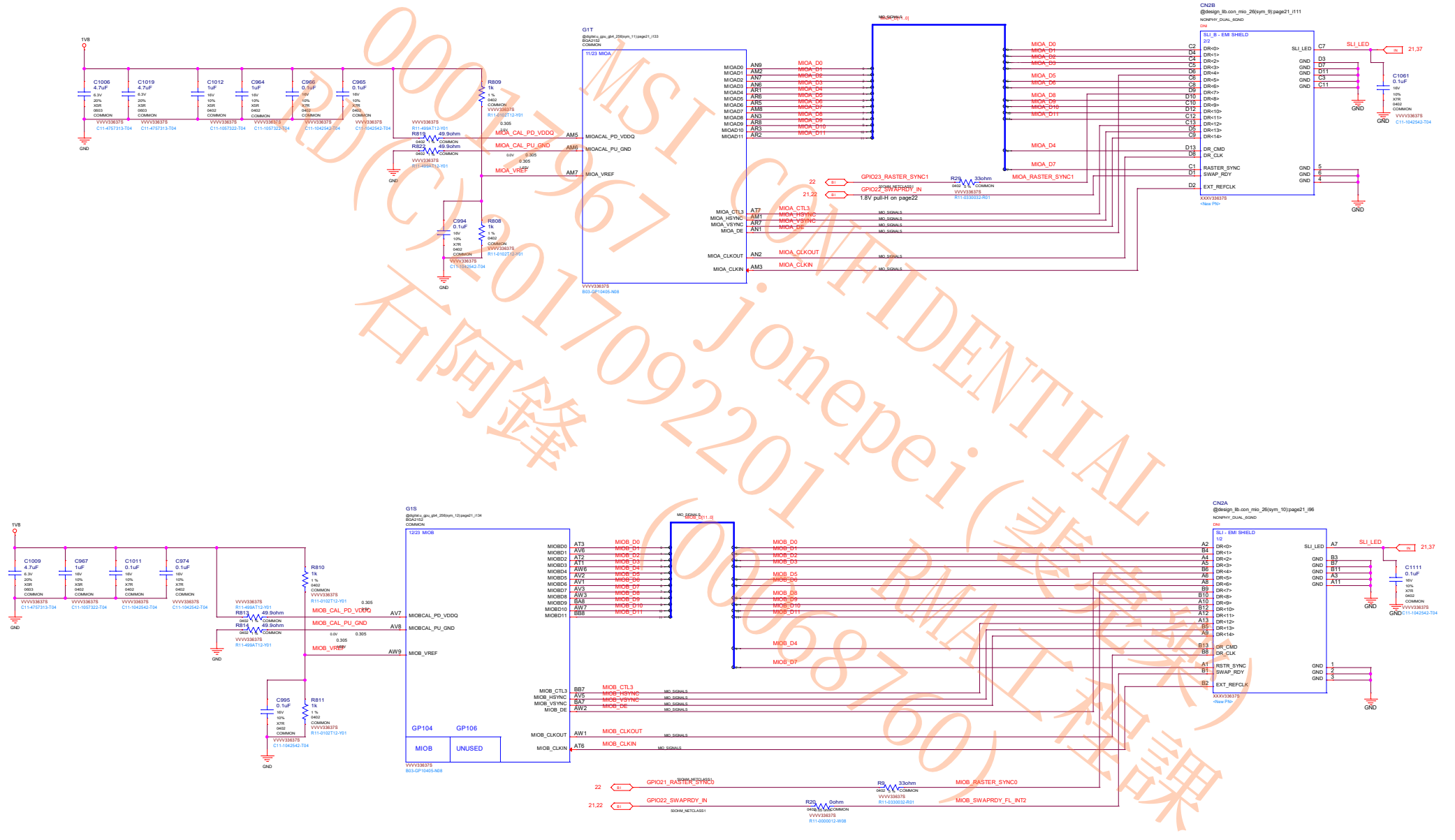
Size: Custom	Document Description: IFPD DP	Rev: 40
Date: Tuesday, March 28, 2017	Sheet 20 of 40	

Page21: MIOA/B Interface



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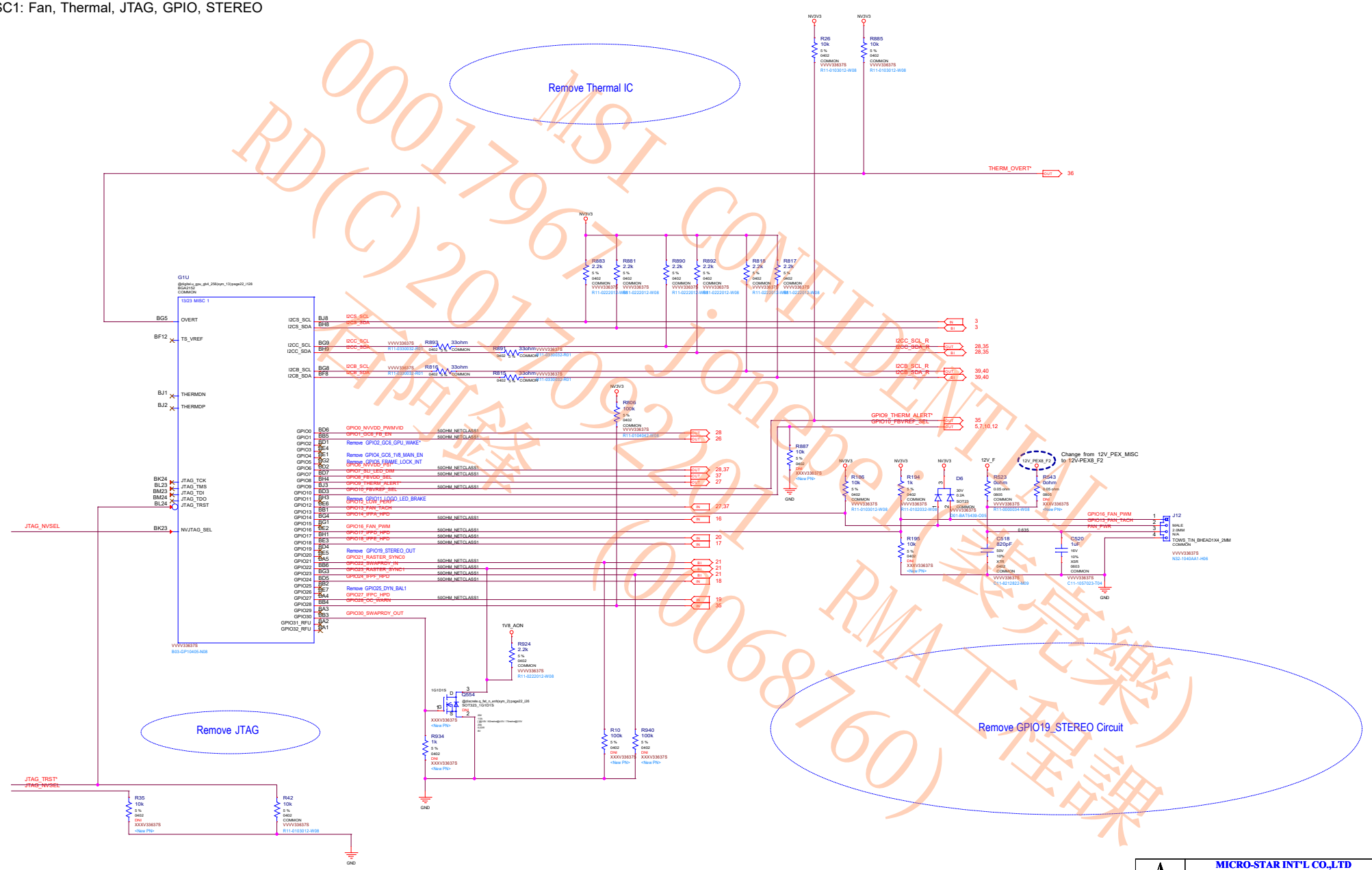
MS-V336		
Size: Custom	Document Description: MIOA/B Interface	Rev: 40
Date: Tuesday, March 28, 2017	Sheet 21 of 40	

Page22: MISC1: Fan, Thermal, JTAG, GPIO, STEREO



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MS-V336	
Size: Custom	Document Description: MISC1: Fan, Thermal, JTAG, GPIO, STEREO
Rev: 40	
Date: Tuesday, March 28, 2017	Sheet 22 of 40

Page23: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

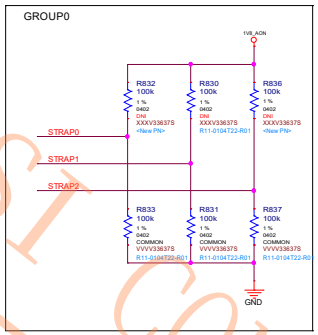
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

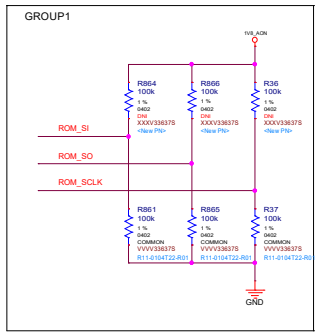
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

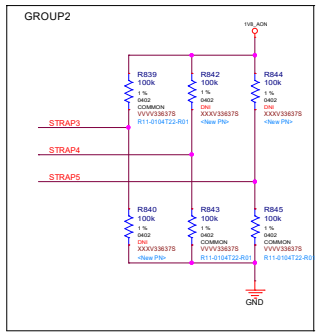
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

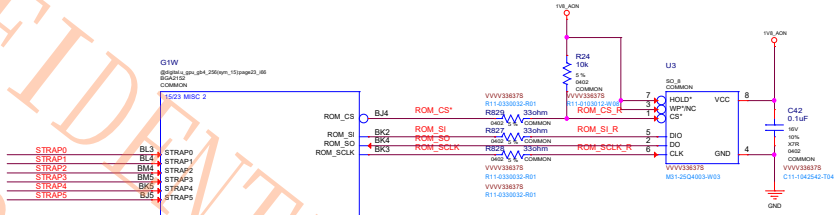
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

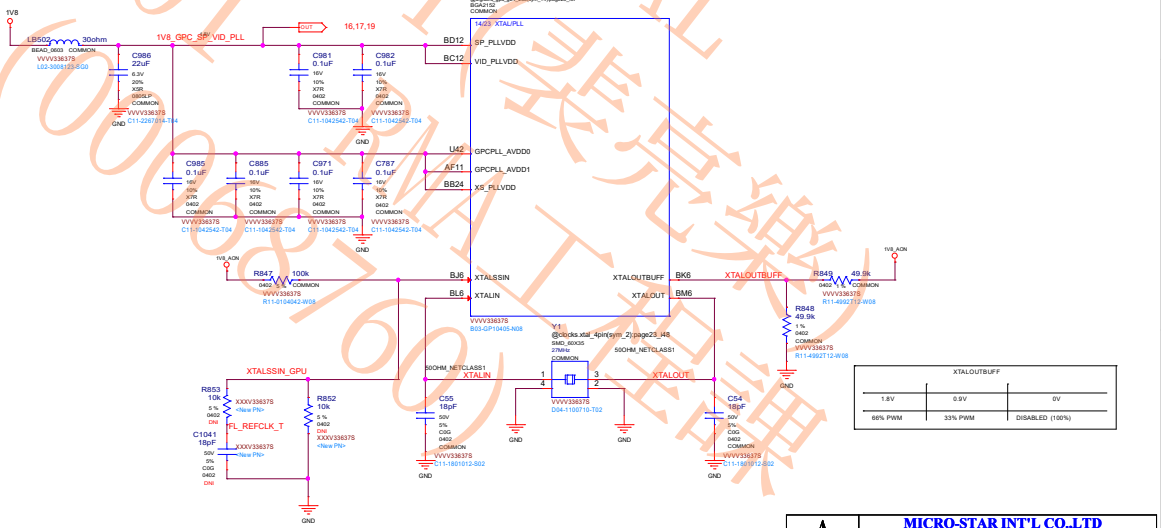






CFG[3:0]	Config	Width	Vendor
0000	256Mx32	256-bit	Micron
0001	Reserved		
0010	Reserved		
0011	Reserved		
0100	Reserved		
0101	Reserved		
0110	Reserved		
0111	Reserved		





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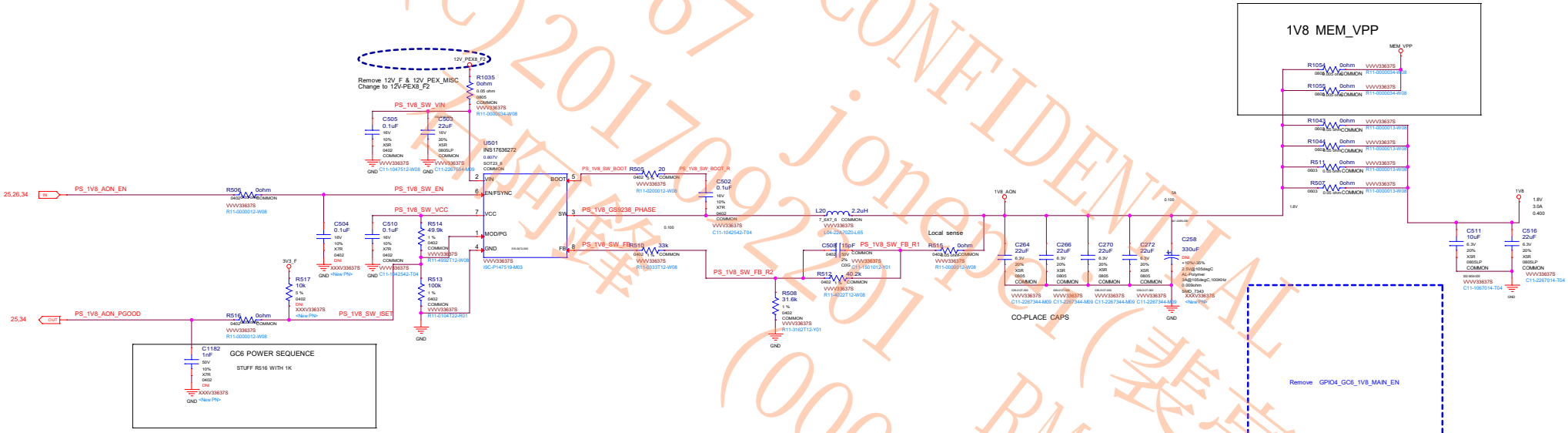
Size: Custom | Document Description: MISC2: ROM, XTAL, Straps | Rev: 40
Date: Tuesday, March 28, 2017 | Sheet 23 of 40

Page24: PS: 1V8, 1V8_AON



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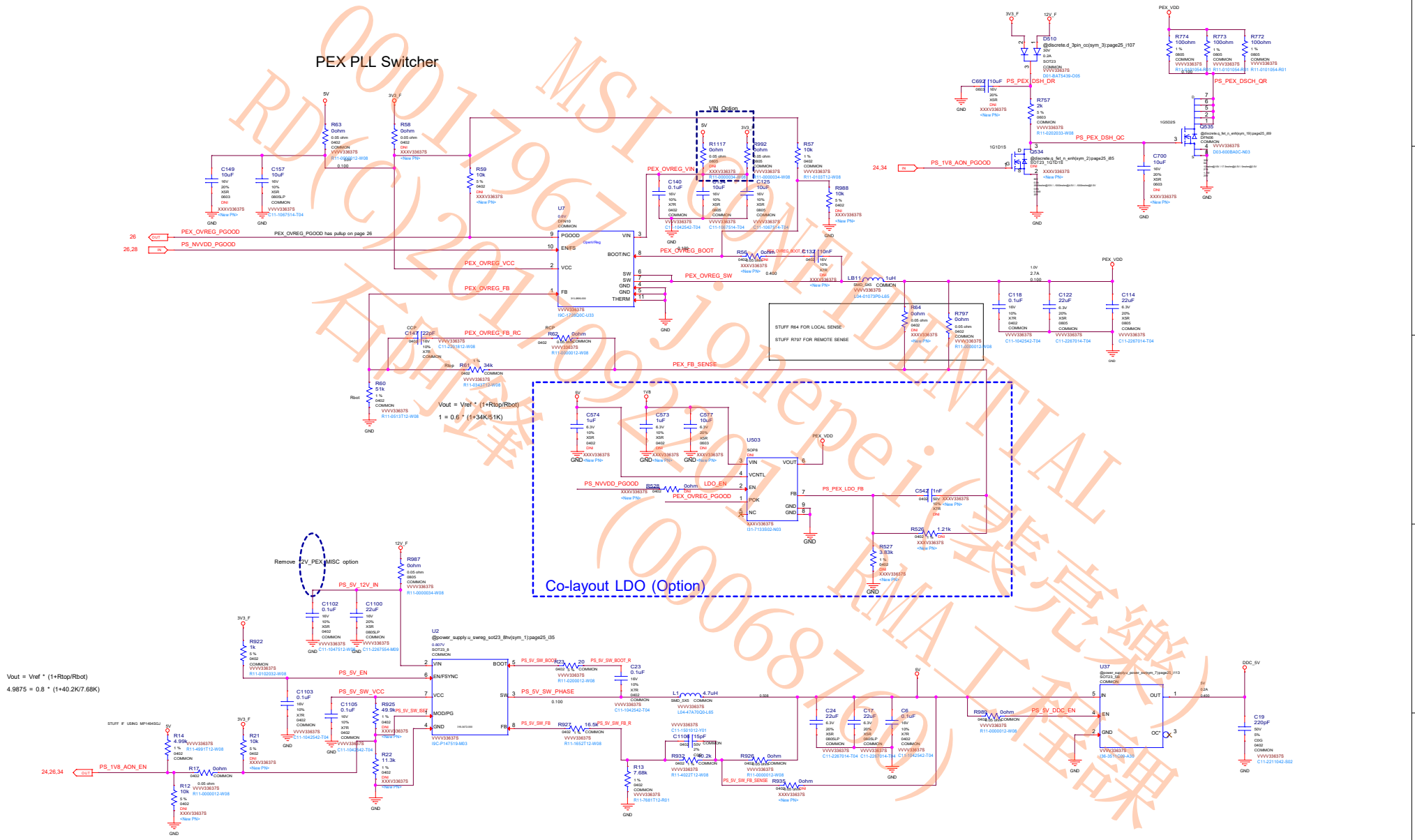
Size: Custom	Document Description: PS: 1V8, 1V8_AON	Rev: 40
Date: Tuesday, March 28, 2017	Sheet 24 of 40	

Page25: PS: 5V, PEX_VDD



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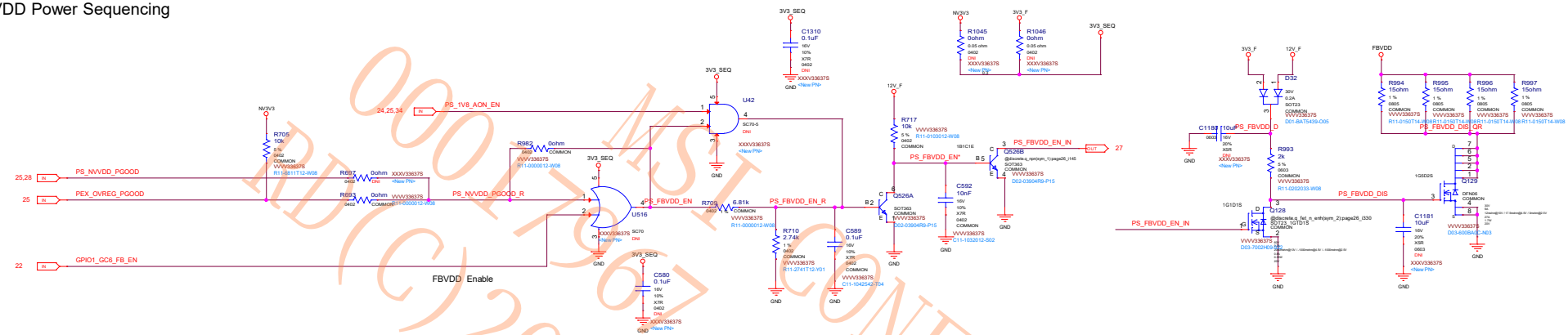
Size: Custom	Document Description: PS: 5V, PEX_VDD
Rev: 40	
Date: Tuesday, March 28, 2017	Sheet 25 of 40

Page26: PS: FBVDD Power Sequencing



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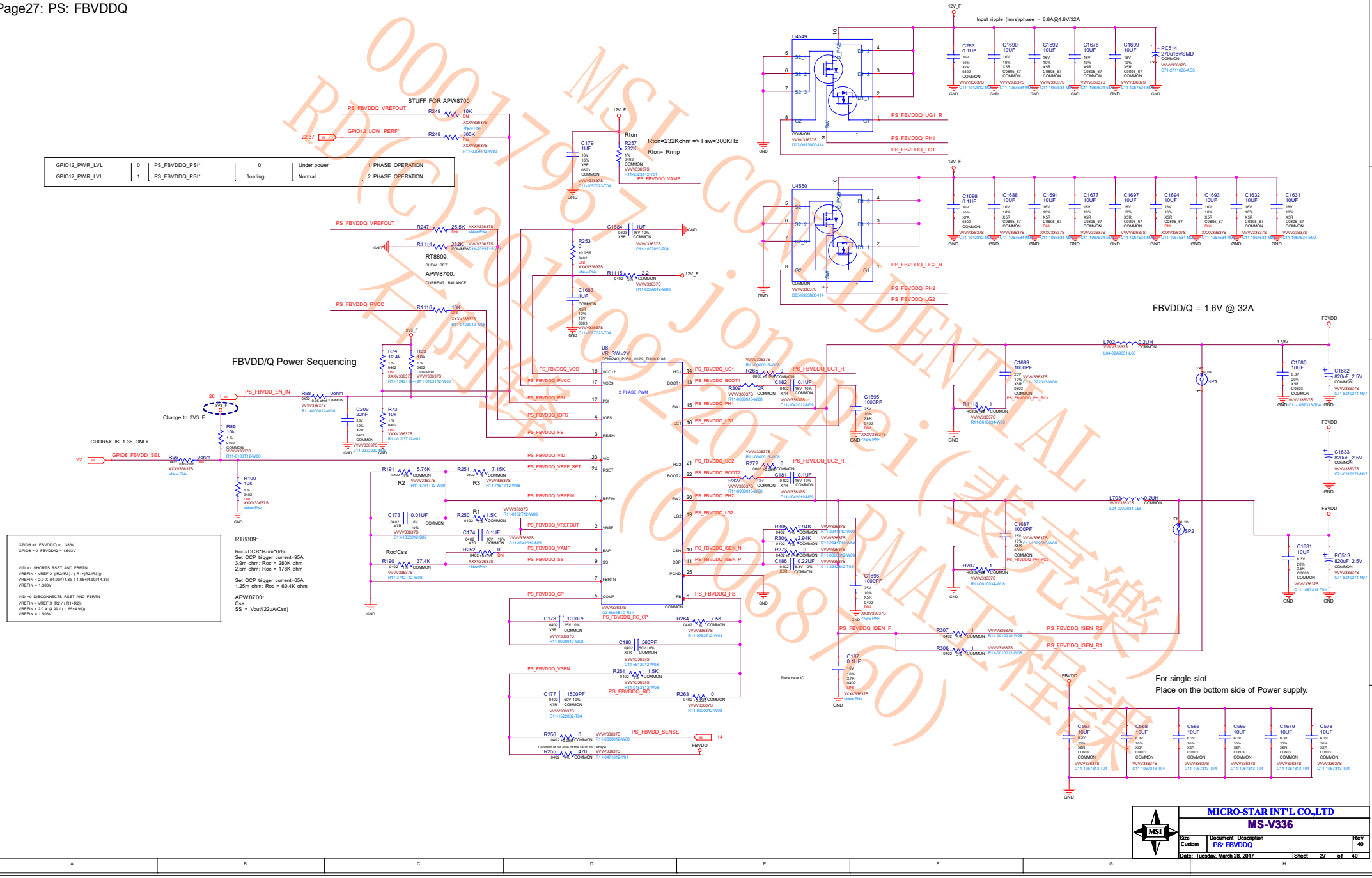
MS-V336	
Size: Custom	Document Description: PS:FBVDD Power Sequencing
Rev: 40	
Date: Tuesday, March 28, 2017	Sheet 26 of 40

Page27: PS: FBVDDQ



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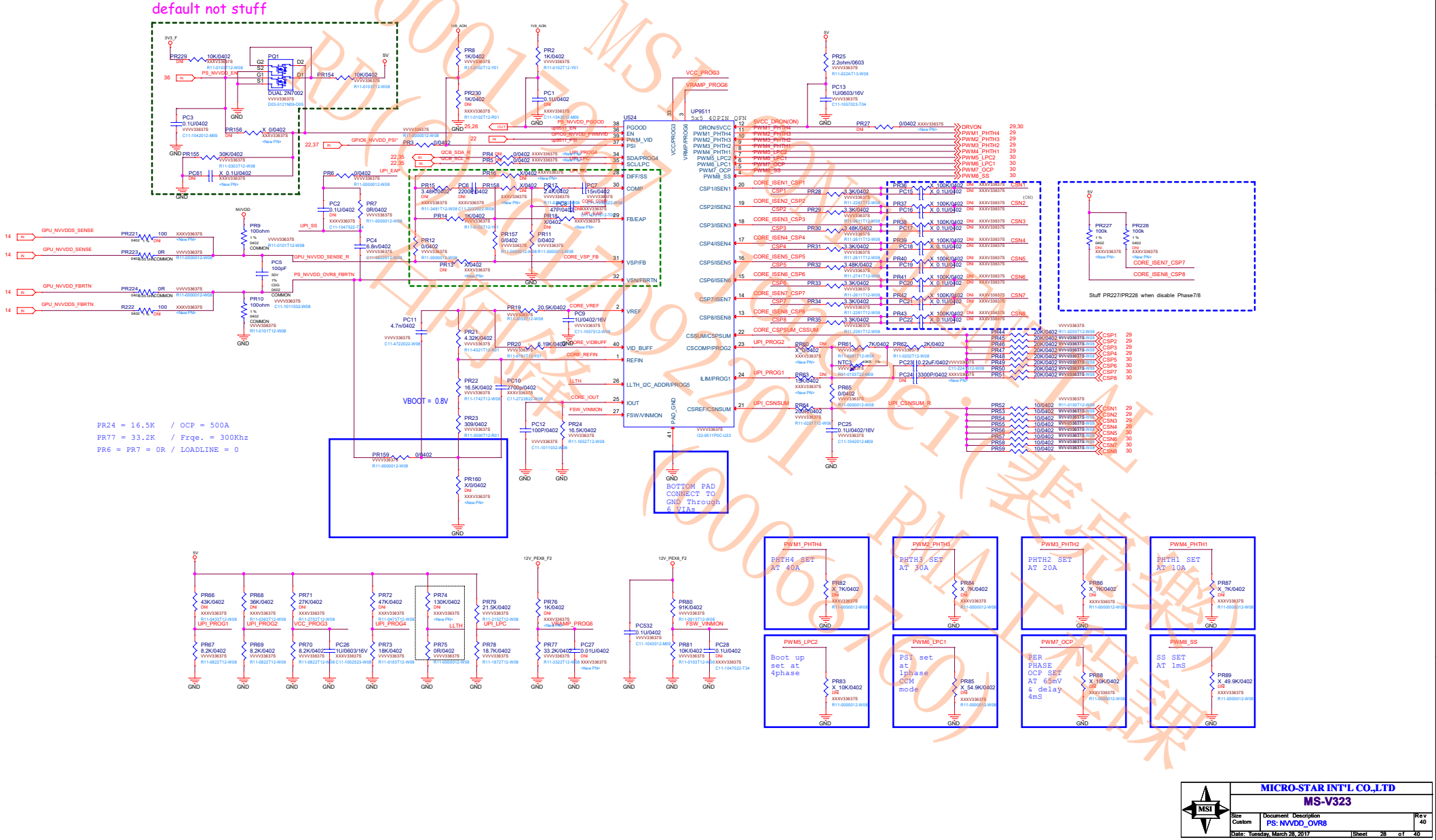
Size	Document Description	Rev
Custom	PS: FBVDDQ	40

Date: Tuesday, March 28, 2017 Sheet 27 of 40



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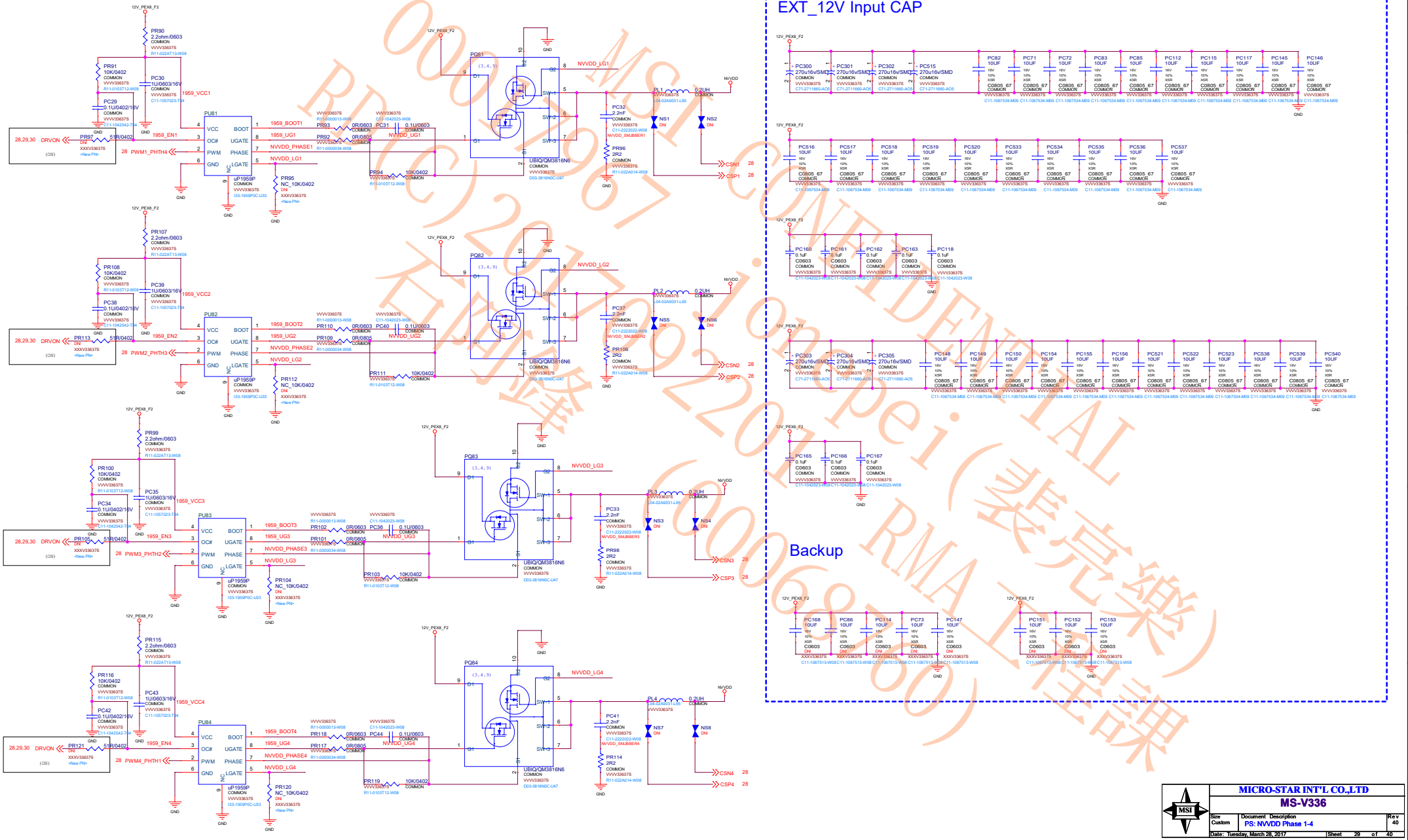
MS-V323			
Size: Custom	Document Description: PS: NVVDD_OVR8		Rev: 40
Date: Tuesday, March 28, 2017	Sheet 28 of 40		



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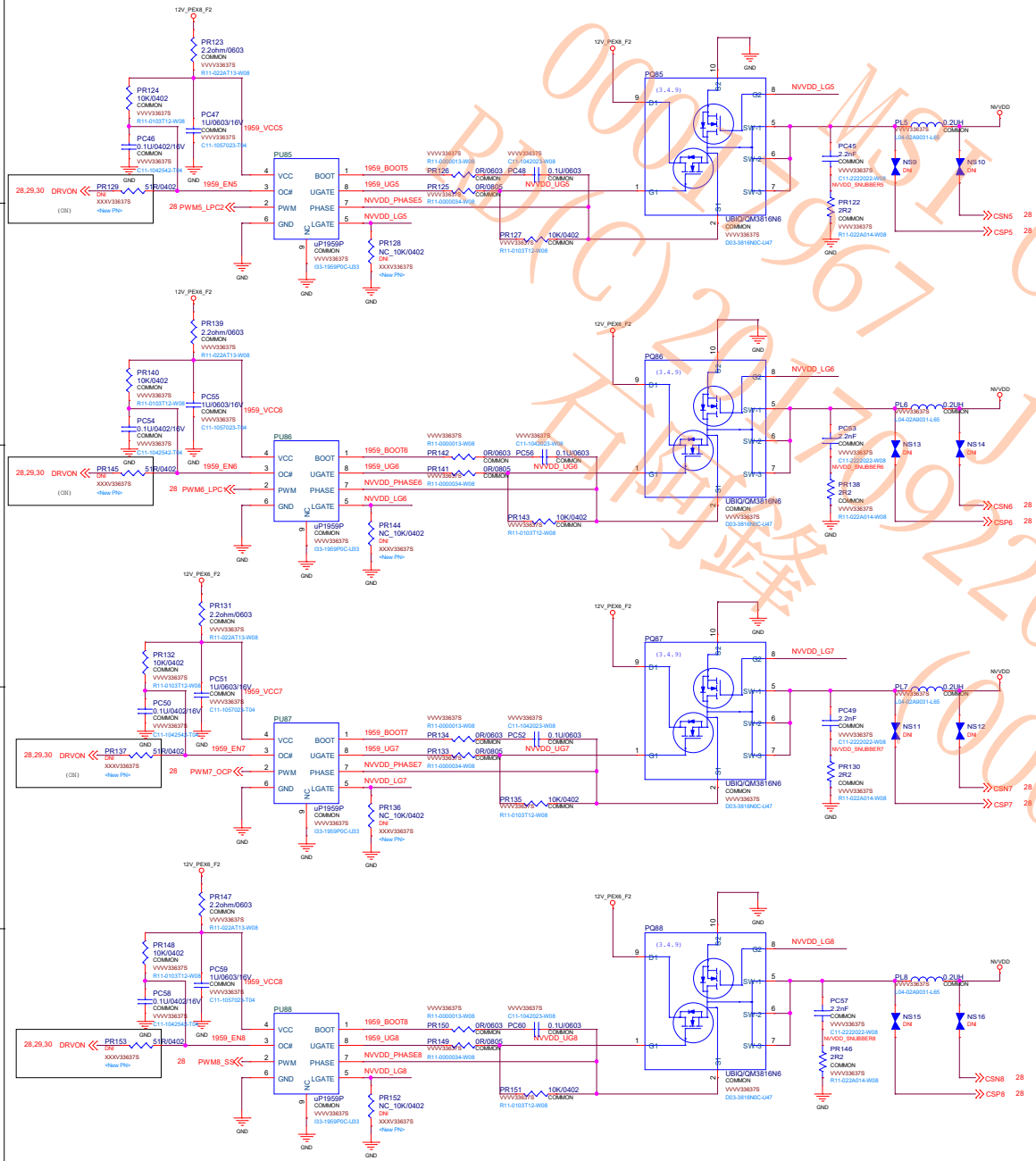
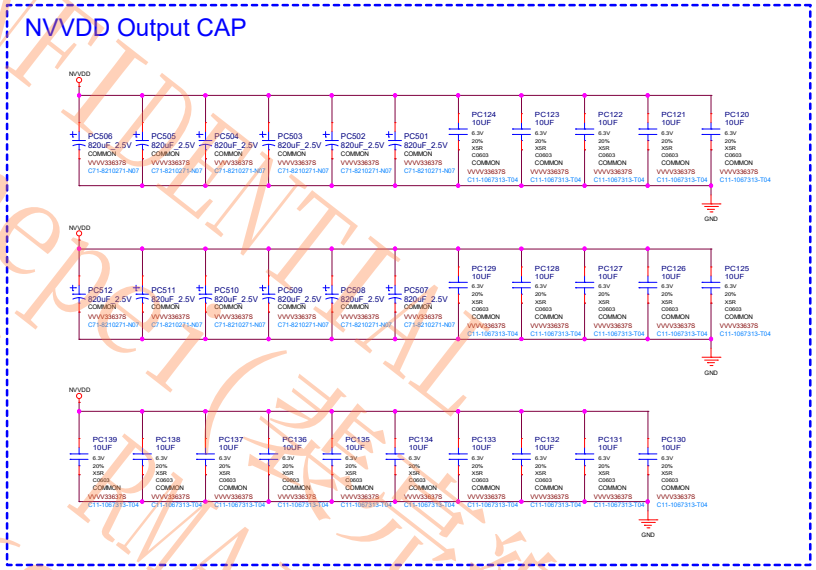
RDC 2017092201 RMA Lab
(0006720)

Page30: PS: NVVDD Phase 5-8





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Size: Custom	Document Description: PS: NVVDD Phase 5-8		Rev: 40
Date: Tuesday, March 28, 2017	Sheet 30 of 40		

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Page31: PS: Blank Page

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Size: Custom | Document Description: PS: Blank Page | Rev: 40
Date: Tuesday, March 28, 2017 | Sheet 31 of 40

Page32: PS: Dynamic Power Balance Phases

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Size	Document Description	Rev
Custom	Dynamic Power Balance Phases	40

Date: Tuesday, March 28, 2017 Sheet 32 of 40

Page33: PS: Dynamic Power Balance Logic

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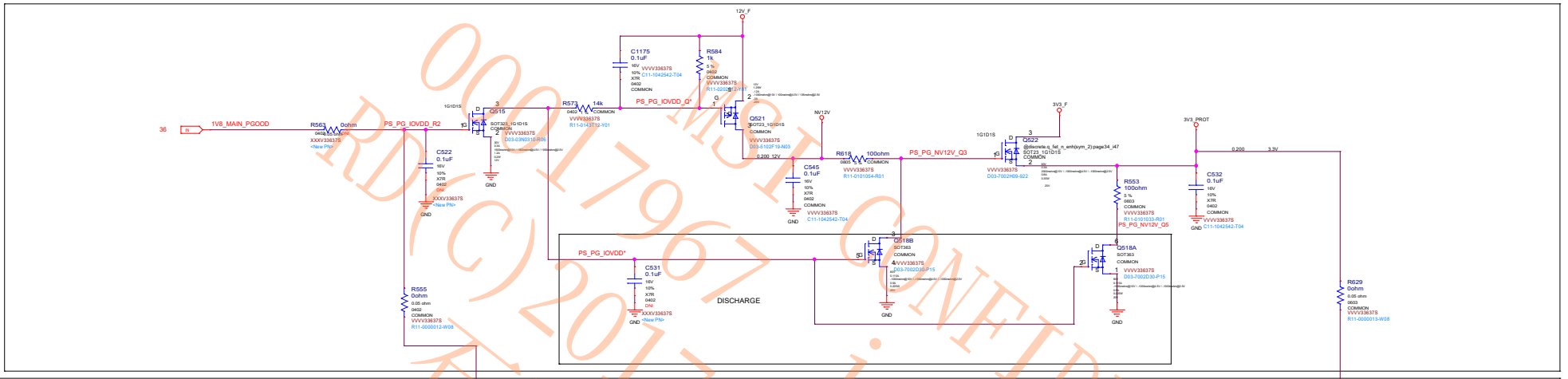
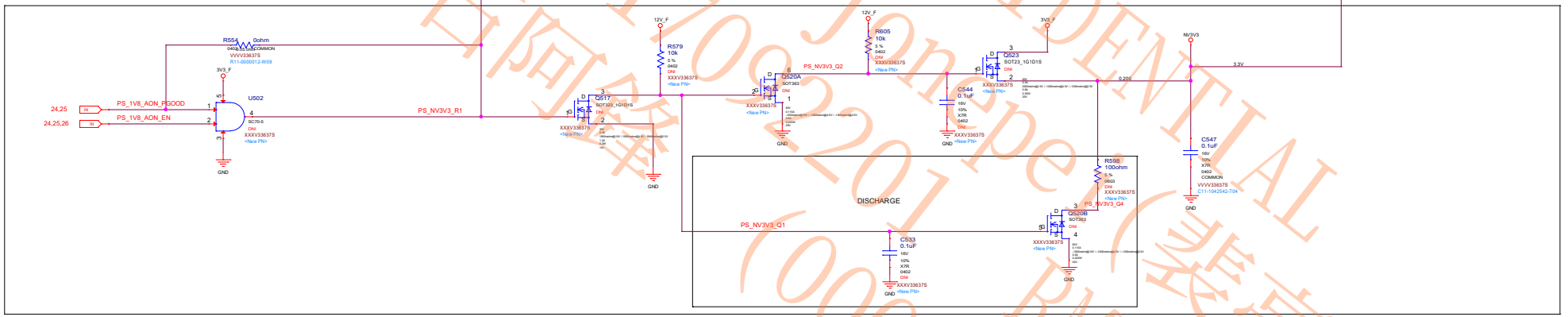
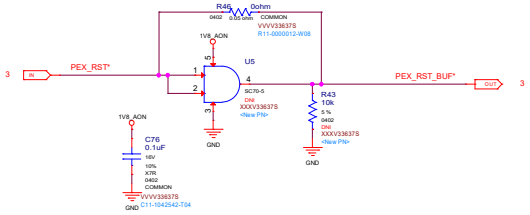
Size: Custom	Document Description: PS: Dynamic Power Balance Logic
Rev: 40	
Date: Tuesday, March 28, 2017	Sheet 33 of 40

Page34:PS: NV3V3, NV12V







Remove

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Size: Custom	Document Description: PS: NV3V3, NV12V	Rev: 40
Date: Tuesday, March 28, 2017	Sheet 34 of 40	

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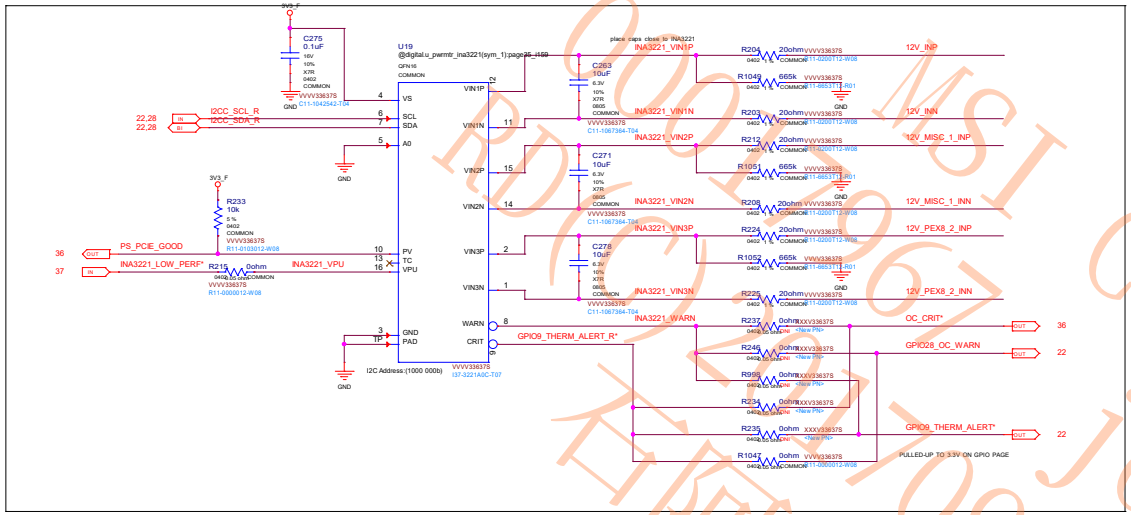
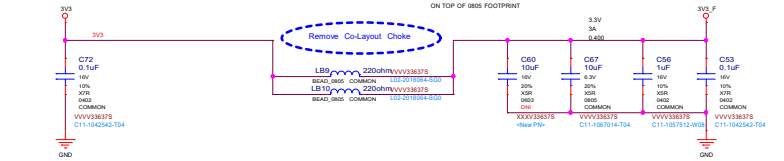
RD(C)20170922 Jonnpe(裝完樂)
石阿伴(0006760) RMA工程課

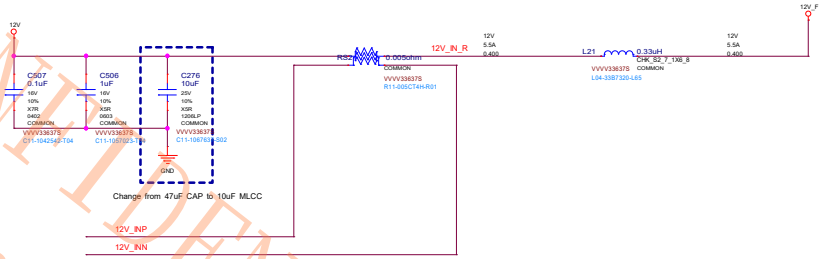
Page35: PS: Inputs, Filtering, and Monitoring

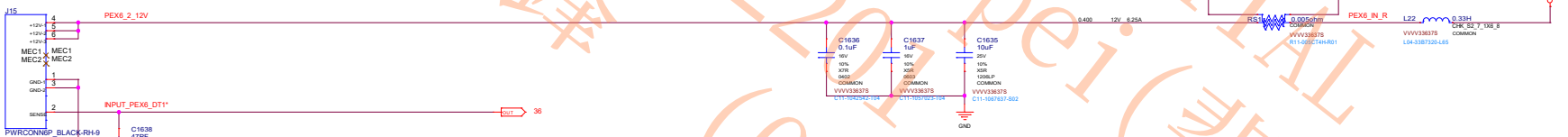


PEX 3V3 INPUT - 10W

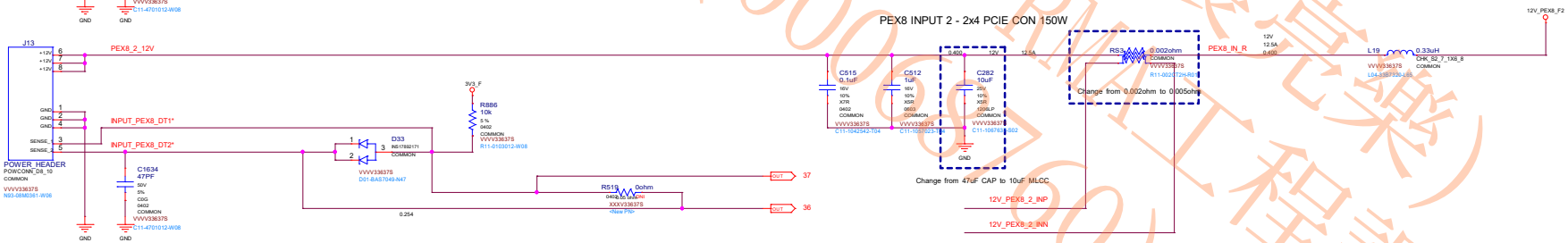


PEX_12V INPUT - 66W





PEX8 INPUT 2 - 2x4 PCIE CON 150W



STUFF FOR 6-PIN CONNECTOR
OR REVERSE CPU 8-PIN CONNECTOR

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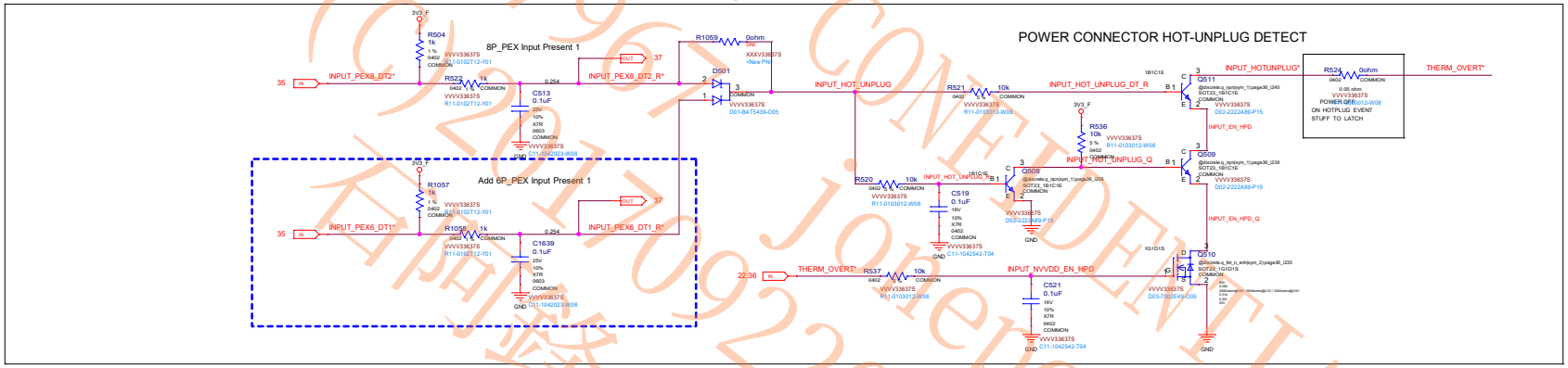
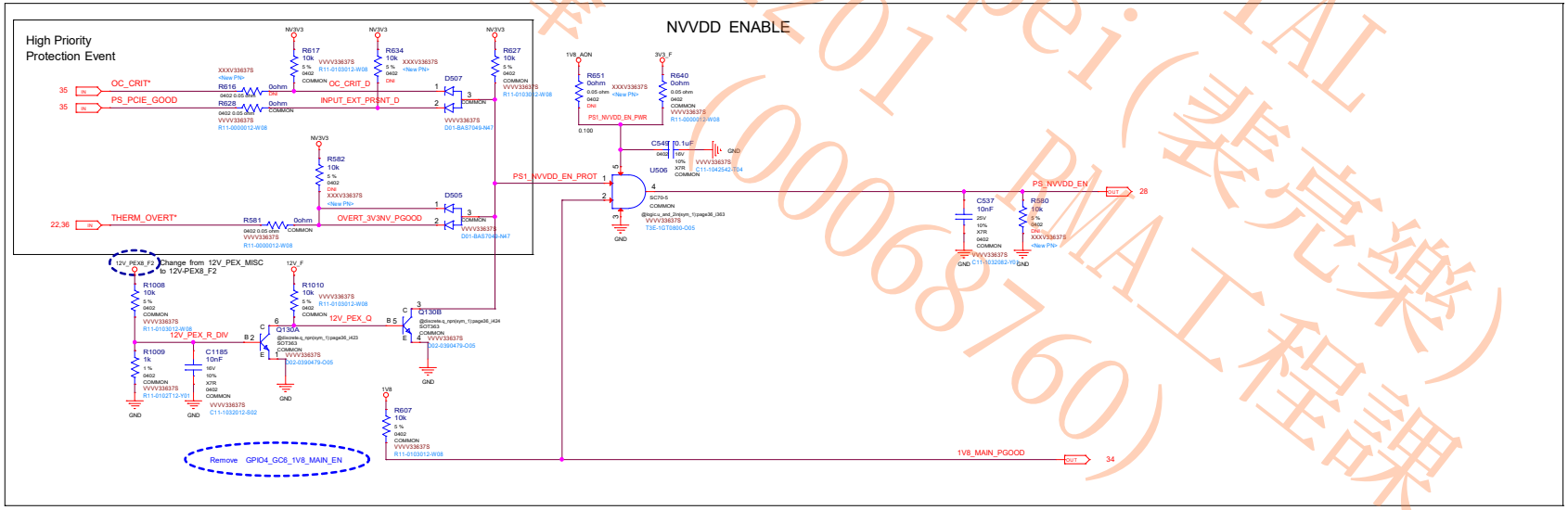
Size: Custom	Document Description: PS: Inputs, Filtering, and Monitoring	Rev: 40
Date: Tuesday, March 28, 2017	Sheet 35 of 40	

Page36: PS: Shutdown and Sequencing





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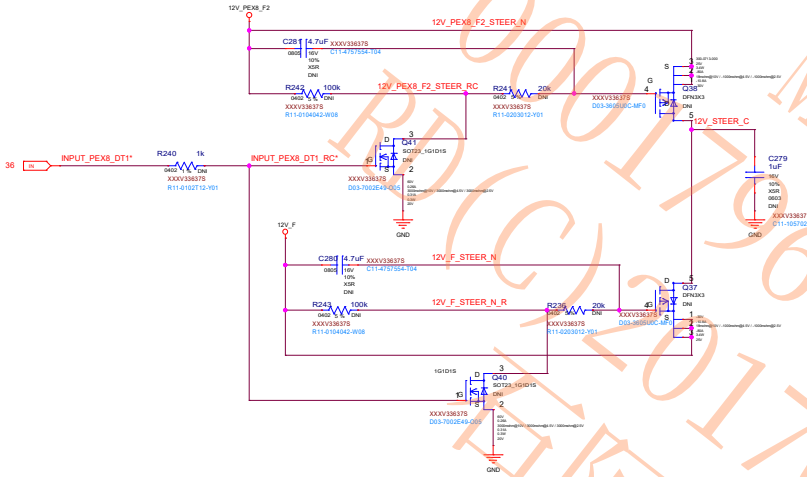
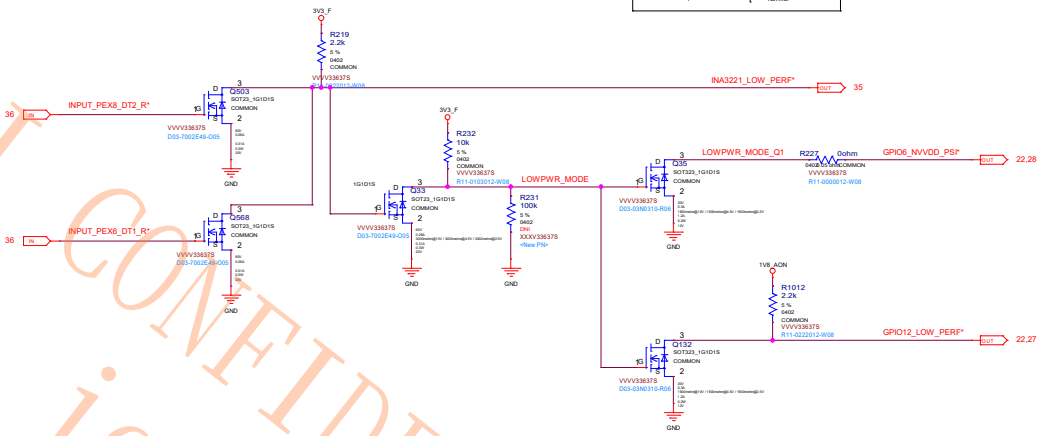
Size: Custom	Document Description: PS: Shutdown and Sequencing
Rev: 40	
Date: Tuesday, March 28, 2017	Sheet 36 of 40

Page37: PS: 12V Current Steering, PSI Control, and LED

PEX Input - 12V Current Steering FETs



PEX Input - Power Level/PSI* Control



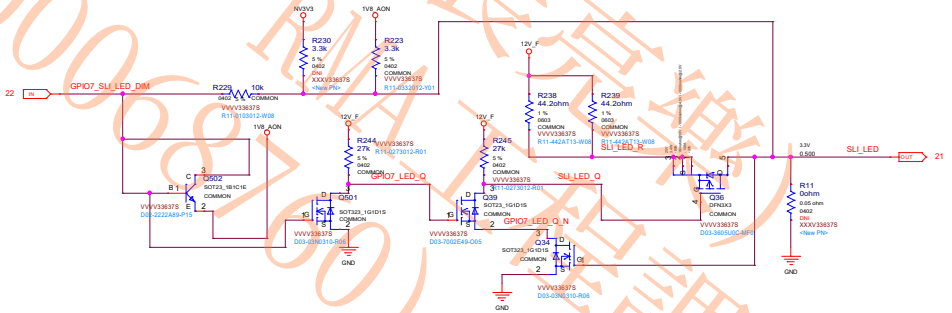
Remove POWER BRAKE

GeForce Logo LED

LED HEADER
(C0MM0N)

Remove Logo LED

SLI LED (GEFORCE ONLY)



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RMA课
(00068760)
RD(C)20170922001
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Size: Custom	Document Description: PS: 12V Current Steering, PSI Control
Rev: 40	
Date: Tuesday, March 28, 2017	Sheet 37 of 40

Page38: Mechanical: Bracket/Thermal Solution

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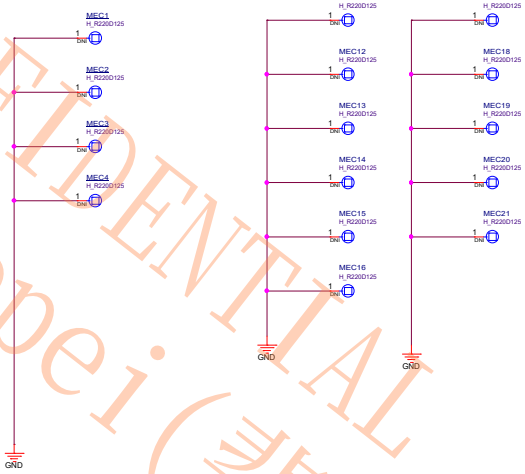
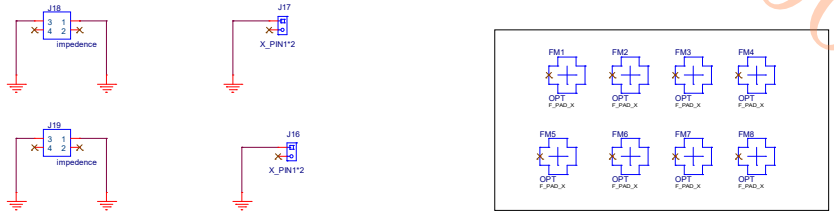
Brackets:

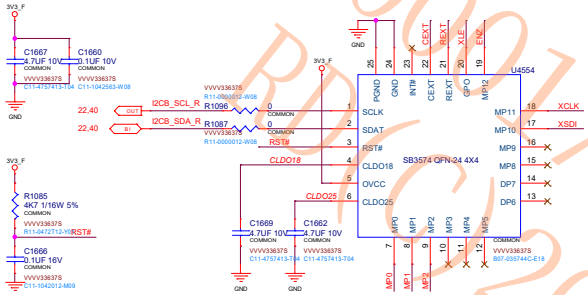
GPU Stiffner

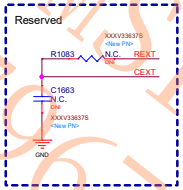


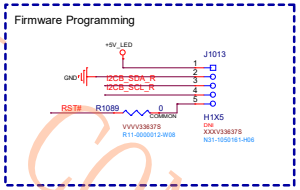


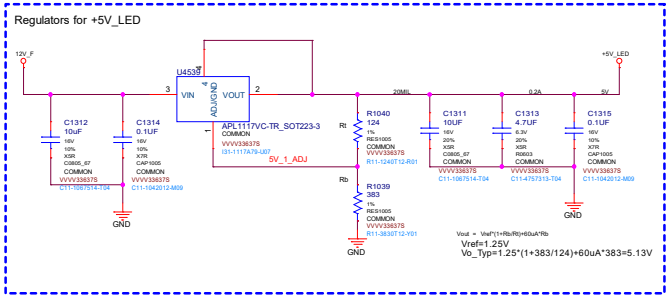
MICRO-STAR INT'L CO.,LTD		
MS-V336		
Size: Custom	Document Description: Mechanical: Bracket/Thermal Solution	Rev: 40
Date: Tuesday, March 28, 2017	Sheet 38 of 40	

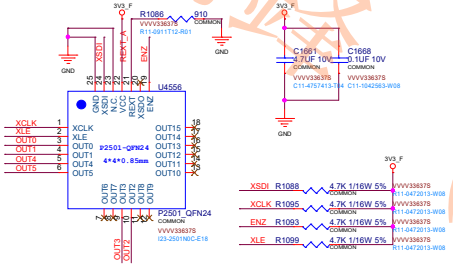
Page39: LED_CONTROLLER_ENE3574

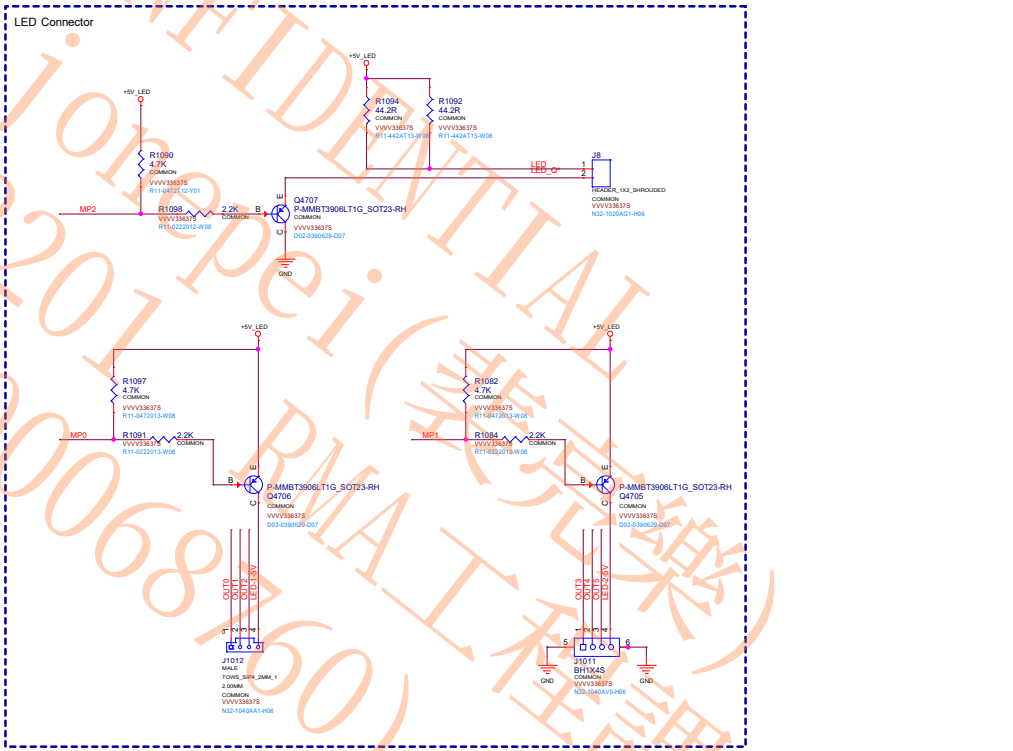












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Size: Custom	Document Description: LED_CONTROLLER_ENE3574	Rev: 40
Date: Tuesday, March 28, 2017	Sheet 39 of 40	

Page40: VOLTAGE SUPERVISOR

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石阿鋒 (00068760)

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Size: Custom	Document Description: VOLTAGE SUPERVISOR — Rev: 40
Date: Tuesday, March 28, 2017	Sheet 40 of 40