ATTRIBUTES

Reference OPSQA70001 for attribute detail:

TRAINING:		DOCUMENT LEVEL:	
Self-Train (Read Doc.)	☒ Yes	Level 2	☐
Originator Training	☐ Yes	Level 3	☒
NV-Learning	☐ Yes	Level 4	☐

NVIDIA Assembly Part Number	Assembly Description
699-1G413-XXXX-XXX	PG413 GP104 Assembly
Top Level Assemblies..................	Refer to 900-BOM per Purchase Order

1. PURPOSE

   1.1. To provide instructions for the manufacturing process associated with the referenced project.

2. SCOPE

   2.1. This procedure applies to all Contract Manufacturers and their respective production area personnel performing assembly of this NVIDIA project.

3. RESPONSIBILITIES

   3.1. **NVIDIA Responsibilities**

      3.1.1. NVIDIA *may* have the responsibility to provide some tooling and process engineering support when requested.

      3.1.2. NVIDIA must qualify the CM per 630-0033-001 QPA Checklist for PCA and OPQ71043 QSA Checklist to fulfill the requirements of 630-0034-001, CM Qualification Procedure per procedure OPSQA70007 Supplier Qualification and Re-Assessment.

      3.1.3. NVIDIA must qualify PCB subcontractors per 630-0037-001 QPA Checklist for PCB and OPQ71043 QSA Checklist to fulfill the requirements of 630-0034-001, CM Qualification Procedure per procedure OPSQA70007 Supplier Qualification and Re-Assessment, if PCA's built with same PCB's are sold directly to NVIDIA.

   3.2. **Contract Manufacturer Responsibilities**

      3.2.1. The CM has the responsibility to provide the product as specified in the NVIDIA Purchase Order.

      3.2.2. The CM is responsible to ensure that all process controls and process materials are both RoHS and Halogen Free, for all NVIDIA products, regardless if the components and PCB meet the same requirements or not.

         3.2.2.1. See NVIDIA Document 630-1067-001 Halogen Free Standard and Test Methods for Flux Residues on PCBA.

      3.2.3. The CM is responsible to ensure that PCB subcontractors are qualified suppliers based on:

         3.2.3.1. PCA's sold to OEM should be built on PCB's fabricated by suppliers listed on the OEM's AVL.

         3.2.3.2. PCA's sold directly to NVIDIA should be built on PCB's fabricated by suppliers listed in 630-0034-001.

         3.2.3.3. PCA's sold to direct channel distribution should be built on PCB's fabricated by suppliers listed on the AIC partners AVL.

            - NVIDIA recommends that AIC partners use a PCB vendor qualification system similar to NVIDIA's. See section 3.1.3.

   3.3. **System-Level (OEM/SB) Responsibilities**

      3.3.1. If the addition of a stiffener to the PCA for shipping is required by the 900 BOM, the CM is responsible for communicating to the CM's customers the following requirement.

         3.3.1.1. The system manufacturer has the responsibility to ensure the board is secured for system-level shipping.

            - Reference System Build Instruction (SBI), 625-90XXX-XXXX-XXX.

4. REFERENCE DOCUMENTS

NOTE: THIS MPI MUST BE USED IN CONJUNCTION WITH THE FOLLOWING FILES AND REFERENCE DOCUMENTS.

Assembly-Specific Documents

NVIDIA Part Number	Description or Reference
699-1G413-00ss-xxx	Bill-of-Material (BOM)
602-1G413-00ss-xxx	Schematics
610-1G413-1000-xxx	Gerber data files
613-1G413-1000-xxx	Test point file
614-1G413-1000-xxx	Centroid data file (X-Y-theta)
618-xxxxx-xxxx-xxx	Manufacturing Diagnostics
621-(See 900-Level BOM)	BIOS part number, version and flash utility information.
628-1G413-00ss-000	Functional Test Procedure
625-5G413-00ss-xxx	Final Configuration Instruction (Workstation Only)
632-1G413-00ss-xxx	ICT Coverage Spec

NVIDIA Reference Documents

NVIDIA Part Number	Description or Reference
IPC-A-600x (Class II)	Acceptability of Printed Circuit's. An IPC publication. (latest revision)
IPC-A-610x (Class II)	ANSI/IPC-A-610 Acceptability of Electronic Assemblies. An IPC publication.(latest revision)
IPC7711	Rework of Electronic Assemblies
IPC7721	Repair and Modification of Printed Boards and Electronic Assemblies
135-00000-0000-001	Label, ESD Warning & Application
136-00000-0000-001	Label, Top PCA, CEM & C of O
136-10000-0000-001	Label, B.C. Date Code & S/N
136-40000-0000-001	Label, BIOS Version
136-00000-0000-003	Label, 600-PCA, revision, CM code & C of O

NVIDIA Part Number	Description or Reference
136-00000-0000-005	Label, Not for EMI Testing
136-80000-0000-001	Label, Sales Sample Model & S/N
363-0000-003	Universal Power Supply Requirements (NV40~NV45)
500-10000-0000-000	Labeling & Packaging, Generic (use for short boards)(up to 8”)
500-10000-0000-100	Labeling & Packaging, Generic (use for long boards)(over 8”)
625-90003-0000-000	System Build Instruction (SBI)
630-0001-001	Techniques for BGA replacement on a PCBA
630-0002-001	PCB Gold Finger Cleaning Procedure
630-0003-001	Cooling Device Attachment/Detachment Procedure
630-0004-001	Design for Testability (DFT) Guidelines and ICT Implementation Policy
630-0009-001	In-Circuit Test (ICT) Release Process
630-0010-001	Printed Circuit Board Fabrication Specifications
630-0011-001	PCA Process Guidelines and Requirements
630-0016-001	PCB: Design for Manufacturing Guidelines
630-0025-001	PCB R.I and 1st Article Procedure
630-0026-001	PCB Checklist for Receiving Inspection
630-0033-001	PCA Process Audit Form
630-0034-001	Approved CEM List
630-0035-001	Guideline for NVIDIA IC Material Handling and Reflow
630-0036-001	Techniques for NVIDIA MAP BGA Replacement on a PCBA
630-0037-001	PCB Process Audit Form
630-0042-001	PCA Equipment Capabilities Agreement
630-0043-001	MAP Manufacturing Process Guide
630-0046-001	Spec., Thermal Grease, Shin-Etsu X23-7762-1G
DA-05931-001	PC Board Strain Measurement Specification
630-0048-001	BGA Re-Balling Procedure
630-0049-001	SLT In-Line GPU Screening Process and Quality Requirements Generic

NVIDIA Part Number	Description or Reference
630-0050-001	Wire Bond Lead-Free Qualification Documents
630-0051-001	Manufacturing Rework Guidelines
630-0053-001	NVIDIA Roadmap RoHS Compliance
630-0055-001	Volterra CSP Application Note
630-0071-001	Quality Systems Audit Checklist
630-0072-001	TAK PAK® Rework Instruction
630-0082-001	RoHS Compliance Program
630-1067-001	Halogen Free Standard and Test Methods for Flux Residues on PCBA
OPSAE72004	Integrated Circuit (IC) Packaging Requirements
OPSBE80016	Supplier Quality Agreement for PCA
OPSMC0016	International PCBA Packaging & Shipping Specification
OPSQA70000	NVIDIA's Quality Manual
OPSQA70001	Proc. Document and Data Control (Agile Database)
OPSQA70003	Corrective and Preventative Action (CAR) Procedure
OPSQA70007	Supplier Qualification and Re-Assessment
ANSI/ESD S20.20-2007	Electro Static Discharge (ESD) Damage Control Specification
OPSQA70022	PCBA Qualification Requirements for Products/Materials and On-Going Reliability Test
OPSQA70026	Customer Return Material Authorization (RMA) Policy for External Use
OPSQA70027	PCBA Source Inspection Specification
OPSQA70030	IQC R.I. Specification for PCA and Components
630-0080-001	NVIDIA COSMETIC STANDARDS FOR FABRICATED PARTS
630-1100-000	NVIDIA Cosmetic Standards for GPU Products
625-9FLUX-RESD-CLN	No Clean Flux Cleaning Procedure for PCAs

5. DEFINITIONS

Acronym	Definition	Acronym	Definition
AGP	Accelerated Graphics Port	**LCR**	(L) Inductance Capacitance Resistance
AIC	Add In Card		Resistance
AKA	Also Known As	**MPI**	Manufacturing Process Instruction
AOI	Automated Optical Inspection	**MRB**	Material Review Board
AQL	Acceptable Quality Level	**MSDS**	Material Safety Data Sheets
ASIC	Application Specific Integrated Circuit	**OBA**	Out of Box Audit
AVL	Approved Vendor List	**OEM**	Original Equipment Manufacturer
BFR	Brominated Flame Retardant	**OQA**	Ongoing Quality Audit
BGA	Ball Grid Array Integrated Circuit	**ORT**	Ongoing Reliability Testing
BIOS	Basic Input Output System	**Pb-Free**	Pb = Lead (Lead Free)
BOM	Bill of Materials	**PCA**	Printed Circuit Assembly
CAD	Computer Aided Design	**PCB**	Printed Circuit Board
CEM	Contract Electronics Manufacturer	**PIP**	Pin In Paste (AKA: Intrusive Reflow)
CFR	Chlorinated Flame Retardant	**QFP**	Quad Flat Pack
CM	Contract Manufacturer	**QPA**	Quality Process Audit
CofC	Certificate of Compliance	**QSA**	Quality Systems Audit
CSP	Chip-Scale Packaging	**RI**	Receiving Inspection
ESD	Electro Static Discharge	**RMA**	Return Material Authorization
FCI	Final Configuration Instruction	**RoHS**	Restriction of Hazardous Substances
FT	Functional Test	**SAC**	Sn (tin), Ag (silver), Cu (copper) alloy solderpaste
FCT	Functional Circuit Test	**SB**	System Build
FTP	Functional Test Procedure	**SBI**	System Build Instruction
GPU	Graphics Processor Unit	**SKU**	Stock Kitting Unit
IC	Integrated Circuit	**SMT**	Surface Mount Technology
ICT	In Circuit Test	**uBGA®**	Micro-Pitch Ball Grid Array
IPA	Isopropyl Alcohol	**VMI**	Visual-Mechanical Inspection
IPC	**I**nstitute for interconnecting and **P**ackaging electronic **C**ircuits	**WIP**	Work In Process
IR	Intrusive Reflow (AKA: Pin In Paste)	**1st Art**	First Article Verification

6. GENERAL/SPECIFIC REQUIREMENTS

6.1. **Documentation: Order of Precedence**

6.1.1. In the absence of clear instructions, NVIDIA's order of document precedence is as follows:

6.1.1.1. Purchase Order

6.1.1.2. Bill-of-Material

6.1.1.3. Assembly Drawing

6.1.1.4. This MPI and associated FTP and/or FCI.

6.2. System Power Requirement

6.2.1. The ATX12V power supply must have 550Watts or higher output power rating for combined +12V, +5V and +3.3V rails. Also sufficient number of peripheral power connectors to make two connections to the PXXX graphic card. Refer to 363-0000-003 (Universal Power Supply Requirements).

6.2.1.1. All test stations must be equipped with the appropriate power supplies.

6.2.1.2. End users must be notified of this requirement.

6.3. **WIP Tracking Requirement**

6.3.1. Tracking the assembly from the start of the assembly process through shipping by PCB serial number is a requirement. Teflon, polyimide or other acceptable label material to withstand the temperatures of the assembly process is required. Refer to subsection for label requirements to support WIP tracking. CM to track defects found from the following areas:

6.3.1.1. Rejection from any visual inspection point during assembly. Including solder paste deposition, post reflow, AOI, manual assembly, post wave solder and mechanical assembly.

6.3.1.2. In-Circuit Test failure.

6.3.1.3. Functional Test failure.

6.3.1.4. PCA Ongoing Reliability Specification.

6.3.1.5. Source Inspection rejection.

6.3.1.6. OQA and/or OBA rejection.

6.3.2. Data to be captured:

6.3.2.1. Reason(s) for rejection. For functional test failure, document the error code specified in the mods.log. This error code is defined in the mods.pdf file contained in the 618 diagnostic zip file provided by NVIDIA.

6.3.2.2. Date of rejection.

6.3.2.3. Date repaired.

6.3.2.4. Describe the rework performed.

6.4. **Process Verification of First Article**

6.4.1. CM to submit process qualification records, i.e., Paste Inspection, AOI results, reflow profiles and in-process inspection results of Top and/or Bottom Side SMT. Final qualification of BGA soldering to include X-Ray inspection report. Prep, Loading, Wave Profile and touch-up inspection reports from through-hole assembly. First pass ICT and FT reports and BGA Rework Station Profile.

6.5. **Electro Static Discharge (ESD) Prevention Program**

6.5.1. Static sensitive components and assemblies must be handled only at static safe workstations.

6.5.2. Personnel must wear the appropriate ESD equipment (static dissipative smock, wrist strap and foot straps). Refer to document ANSI/ESD S20.20-2007.

6.5.3. An ionizer must be installed at the Kapton Tape Removal Station to prevent damage to components from static discharge when tape is removed from the PCBA.

6.6. **Quality Requirements**

6.6.1. Reference OPSBE80016 NVIDIA Supplier Quality Agreement for a Printed Circuit Board Assembly, for quality requirements.

6.6.2. Ensure that PCB's are inspected per IPC-A-600, Class II, 630-0025-001 and 630-0026-001 prior to release for production. All findings shall be documented, maintained on file for a period of one year, and available for review when requested.

6.6.3. During production refer to document IPC-A-610, Class II for PCBA inspection criteria.

6.6.4. Refer to document OPSAE72004 for handling moisture sensitive integrated circuits (IC).

6.6.5. Must enable the SMT machine vision system to check the solder ball count (or size) on the GPU.

6.7. **Test Requirements**

6.7.1. Functional Test (FT) Requirements.

6.7.1.1. Description: Main product-specific functional test run at guardband clocks.

6.7.1.2. Sample size (see **Figure 6.7-1**).

6.7.1.3. Applicability: Applicable to all 600 and/or 690-level Stock Kittable Units (SKU) manufactured by the Contract Manufacturer (CM).

6.7.1.4. Reporting: Part of the weekly Quality reporting process.

6.7.1.5. Documentation: Specific FT procedures can be found in the Functional Test Plan (628-XXXXX-XXXX-XXX) appended to each product-specific Bill of Material (BOM).

6.7.2. Application Test (AT) Requirements.

6.7.2.1. Description: Application test run at BIOS default clocks.

6.7.2.2. Sample size (see **Figure 6.7-1**).

6.7.2.3. Applicability: Applicable to all 600 and/or 690-level SKU manufactured by CM.

6.7.2.4. Reporting: Part of the weekly Quality reporting process.

6.7.2.5. Documentation: Specific APPLICATION TEST PROCEDURE (GENERIC) 628-ATUUT-0000-000 can be found in WindChill.

6.7.3. Ongoing Quality Assurance (OQA) Test Requirements.

6.7.3.1. Description: Simplified FT run at BIOS default clocks.

6.7.3.2. Sample size (see **Figure 6.7-1**).

6.7.3.3. Applicability: Applicable to all 600 and/or 690-level SKUs manufactured by the CM.

6.7.3.4. Reporting: Part of the weekly Quality reporting process.

6.7.3.5. Documentation: Specific OQA test procedures can be found in the Functional Test Plan (628-XXXXX-XXXX-XXX) appended to each product-specific Bill of Material (BOM).

6.7.4. Ongoing Reliability Test (ORT) / Burn-in Requirements.

6.7.4.1. Description: Ongoing test to exercise and stress PCBA functionality at elevated temperatures over a long period of time. Infinite-loop testing is done at 40 degrees C for a 28-day cycle per board. Nvidia ORT engineering must be notified immediately if any failure is encountered after a 10-hour cycle.

6.7.4.2. Test flow: To START, run MODS Test 80 for 10 hours, record the matsinfo log after 10 hours, then loop the FT batch file infinitely for 14 hours. Repeat this process 28 times.

6.7.4.3. Sample size: (see **Figure 6.7-1**).

6.7.4.4. Applicability: Applicable to all 600 and/or 690-level Stock Kittable Units (SKU) manufactured by the Contract Manufacturer (CM).

6.7.4.5. Reporting: Part of the weekly Quality reporting process.

6.7.4.6. Documentation: Modular Diagnostic Software (MODS) log file collected after the 28-day cycle is complete. A total of 28 log files should be collected for each board during the monthly test. Log files are provided to Nvidia by the CM every 10 hours and stored on the Nvidia network.

6.7.5. Ongoing Reliability Test (ORT) / Customer Product Evaluation (CPE) Requirements.

6.7.5.1. Description: Ongoing test to exercise and stress PCBA functionality in constant power-up and down conditions at operating-corner temperatures. Testing is started by simple boot-up to DOS at 55 degrees C, ramping to 0 degrees C in ten minutes, followed by 3 hours at 0 degrees C, and 3 hours at 55 degrees C per board. The operator looks for corruption in the display image quality.

6.7.5.2. Test flow: Power-up; wait 10 seconds; watch the DOS screen for 5 seconds, then power down.

6.7.5.3. Sample size: (see **Figure 6.7-1**).

6.7.5.4. Applicability: Applicable to all 600 and/or 690-level Stock Kittable Units (SKU) manufactured by the Contract Manufacturer (CM).

6.7.5.5. Reporting: Part of the weekly Quality reporting process.

6.7.5.6. Documentation: Modular Diagnostic Software (MODS) log file is collected after each 6-hour cycle is complete. Records are stored on the Nvidia network.

6.7.6. Windows Application Buy-off Requirements.

6.7.6.1. Description: Designed to stress the PCBA by running Windows gaming applications for a minimum of 2 hours. Start by booting 10 times to Windows, then run the following tests in succession: MONTEST, SROLL_32 Test, VIEWPERF (workstations), or SS DEMO (desktops), 3DMark06, ATI Tool, PUNISH, SWITCHBLADE, GLOBE, SPEC gl perf 3.1.2. Then run the WAKE-UP test, and finish by playing a Blue Ray DVD.

6.7.6.2. Sample size: (20 boards).

6.7.6.3. Applicability: Applicable to all 600 and/or 690-level Stock Kittable Units (SKU) manufactured by the Contract Manufacturer (CM).

6.7.6.4. Reporting: Part of the weekly Quality reporting process.

6.7.6.5. Documentation: Specific WinApps test procedures can be found in OPSBE80043. Any deviations from, or changes to, the requirements specified in OPSBE80043 for product release shall be documented in the Quality Management Plan (QMP) for that respective product.

Figure 6.7-1

TEST	TEST FILE	TEST TIME/BOARD	SAMPLE SIZE					
			NPI 1-250		PILOT 251-1250		MASS PRODUCTION 1251+	
			DIRECT	OEM	DIRECT	OEM	DIRECT	OEM
FT	PXXX.CMFT	see 900level BOM for specific 618 file.	1x100%	1x100%	1x100%	1x100%	1x100%	1x100%
AT	Unigine, 3DMark, ATItool	30 min	1x100%	N/A	1x100%	N/A	According to NV SQE recommended test plan	0.15AQL
OQA	PXXX.MFG	see 900level BOM for specific 618 file.	5x100%	5X100%	5x100%	5X100%	According to NV SQE recommended test plan	0.065AQL
OBA	ATItool-20' 3DMark06-5' Badaboom-2' Nurien-2' Fluid-2'	31 min	1x100%	n/a	1x100%	n/a	According to NV SQE recommended test plan	0.15AQL
OEM OBA	GLOBE2.1-5' (DELL only) ATItool-20' 3DMark06-5' Badaboom-2' Nurien-2' Fluid-2'	36 min	n/a	5X100%	n/a	5X100%	n/a	n/a
ORT/BURN-IN	PXXX.MFG looping	28 days	3		2		1/1000	
ORT/CPE	PWR ON/OFF cycling	6 hours	5		5		1/1000	
SYS/APPS	refer to	30 hours	12		8		4/1000	

	OPSBE 80043.				

6.8. Lead-Free / Halide-Free Compliance per RoHS Standards

6.8.1. All NVIDIA BOM's will be RoHS compliant starting January 2005. Refer to 630-0053-001 NVIDIA Roadmap to RoHS compliance.

6.8.2. As RoHS compliance became a legal requirement, effectively starting July 2006, all products and the processes used will be compliant as of that date.

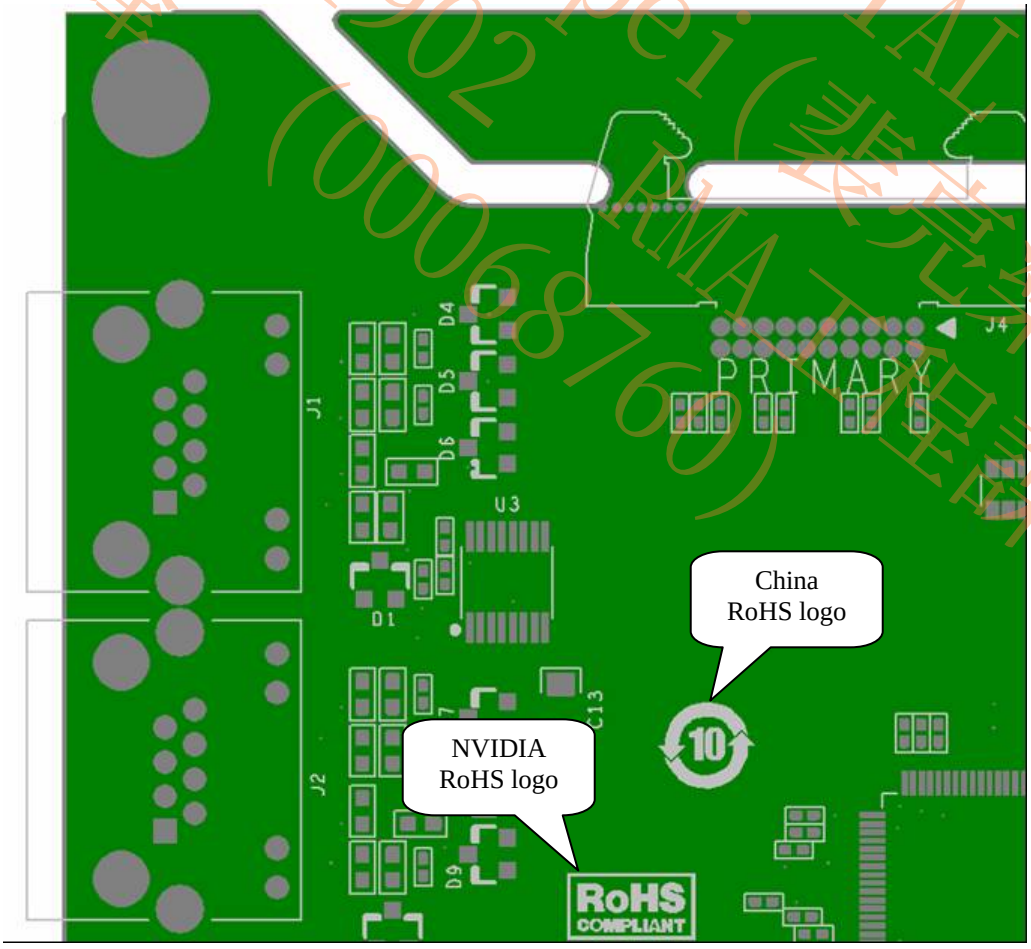
6.8.3. NVIDIA recommends that all the components used in the manufacture of the product be verified as RoHS compliant prior to advertising the product as "Green" or "RoHS Compliant".

6.8.4. Lead free solder shall be used at all SMT, Wave Solder and Rework Stations to comply with RoHS requirements.

- Refer to section 9.5 for reflow considerations for both Pb-Free and mixed technology Pb- Free/eutectic soldering profile and processing considerations.

6.8.5. Board identification – RoHS Compliance or Non-RoHS Compliance.

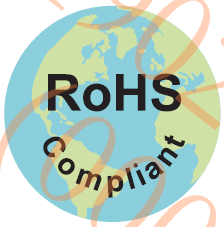
6.8.5.1. Silkscreen marking on fab. No additional label require if RoHS compliant PCBA.



6.8.5.2. Silkscreen marking NOT found on fab or non-RoHS compliant PCBA, add label to bottom side of PCBA on an open space. Or apply to top side if no space available on bottom.

6.8.5.2.1. Non-RoHS compliant PCBA – Apply label 135-0000-001. Note: if silkscreen marking found, apply this label on top of one logo and cover the other with a size-fit blank label.

6.8.5.3. RoHS compliant PCBA – Apply label 135-0000-002 and 135-0000-003.



AND

6.8.6. Halogen Free (<900PPM BFR's / <900 CFR's and <1500PPM BFR's & CFR's Combined) is a voluntary program and is not legislated by any governing body. As a good "corporate citizen" NVIDIA wants to ensure that our products meet standards that satisfy our customer's requests and be a part of the Halogen Free community.

6.8.6.1. Halogen Free does not over-ride nor supersede RoHS compliance requirements.

6.8.7. NVIDIA's target date for Halogen Free implementation across all products is Jan 1, 2009.

6.8.7.1. Halogen Free "process materials" will be used on all NVIDIA products in the manufacturing process starting Oct 1, 2008. This mainly applies to "flux residues".

6.8.7.2. Flux residues are a homogeneous subcomponent of any assembly as defined by all acceptance standards criteria for Halogen Free compliance, regardless if it is on the Bill of Materials or not.

6.8.8. Products that meet the HF requirements should be labeled with an HF in the white silk screen legend of the PCB, or have a label added with "HF" printed on it.

7. MATERIAL/EQUIPMENT

7.1. **All Graphic Card prototype and control run processes MUST be RoHS Compliant and use SAC (Lead Free) solder paste, wave solder and touch-up solder, starting Jan 2006 to ensure that all materials and design considerations are compatible for Product Launches which will occur in the months to follow**.

7.2. **All Graphic Card prototype and control run processes MUST be Halogen Free (HF) Compliant. All soldering fluxes must be rated as HF compliant for SMT Solder Paste, Wave Solder Spray Flux, Liquid Flux used in Touch-Up and Flux Core Wire Solder used in Touch-Up.**

7.3. If PCB's are shipped to NVIDIA, a Certificate of Compliance (CofC) stating you (CM) verified the shipment per IPC-A-600, Class II; NVIDIA documents 630-0025-001 and 630-0026-001. A copy of the CofC and PCB First Article Inspection Checklist, 630-0026-001 must be included with each shipment. Components to be verified via LCR meter to ensure against mislabeling. This may be performed at kit audit or during in-process setup.

7.4. Assembly and rework equipment to be of technological standard required to produce high yield product repeatability per 630-0042-001.

7.5. During the normal process of touching up solder joints after SMT, the operator performing the touch up should be IPC 7711 & 7721 certified in the proper technique to perform the touch up operation, inspection after the touch up and proper selection of materials and equipment used.

8. SAFETY

8.1. Always practice approved production safety methods when building product and using equipment.

8.1.1. Ensure that safety methods are compliant with OSHA Standards, Federal Regulations and corporate policy.

8.1.2. When using chemicals refer to the Material Safety Data Sheets (MSDS) provided in the production area.

9. PROCEDURE **(Contract Manufacturer Requirements)**

9.1. **Bill-of-Material and Materials Verification**

9.1.1. Refer to document OPSAE72004 for handling moisture sensitive integrated circuits (IC).

9.1.2. CEM is responsible to check the BOM for part type and process compatibility. And, submit an AMR (alternate material request) if required.

9.1.2.1. Note: RoHS compliance does NOT imply high temperature. Only that the part does not contain restricted levels of hazardous substances. Reference 630-0082-001

9.1.2.2. For CEM's that use intrusive reflow (pin in paste) process of through-hole components, check the BOM for the high temp alternate part.

9.1.3. Verify qualified Controller (i.e., BGA) on specified location. Refer to BOM for correct NVIDIA part number and, if applicable, substitute part number(s). Refer to Centroid data for X-Y-theta location.

9.1.4. Verify qualified Memory on specified locations. Refer to BOM. CM cannot mix different memory manufacturers on a board. Refer to BOM for correct NVIDIA part number and, if applicable, substitute part number(s). Refer to Centroid data for X-Y-theta locations.

9.1.4.1. PLEASE NOTE: Some memory suppliers have already converted to Pb-Free (RoHS compliant) BGA device configurations and **do not offer a eutectic alternative**. Refer to section 9.5 for reflow profile recommendations.

9.1.5. Refer to document IPC-A-600, Class II, 630-0025-001 and 630-0026-001 for PCB inspection criteria. CM can mix different PCB manufacturers per manufacturing lot if the PCB is the same NVIDIA part number and revision level.

9.1.5.1. If HASL (Hot Air Solder Level) PCB's are NOT ALLOWED for use in any NVIDIA designed products.

9.1.6. If “intrusive reflow” AKA: PIP (pin in paste) is the preferred manufacturing process:

9.1.6.1. Ensure that the high temperature versions of component options are selected.

9.2. **Component Preparation**

9.2.1. The Serial Number Label should be applied to the PCB prior to entering the process.

9.2.1.1. See subsection on LABELS for instructions on label fabrication and placement.

9.2.2. The PCB gold finger connections should be covered with Kapton® tape if wave soldering is applicable to the processing of this assembly.

9.2.2.1. After the assembly process, the removal of the Kapton tape must be done at a Kapton Tape Removal Station equipped with an ionizer.

9.2.3. Pre-cut any component leads that will not meet IPC610, Class II specification after soldering.

9.2.3.1. Ensure that clipping projectiles are kept safely away from automated assembly and test operations.

9.2.4. Contact NVIDIA Program Manager for SLT process requirements.

9.2.4.1. Refer to NVIDIA document 630-0049-001 as a guideline for SLT development.

9.2.4.2. After SLT testing is completed make sure to reseal the GPU bag or control the exposure time so as not to violate the requirements of the proper handling of moisture sensitive devices, refer to OPSAE72004 and NVIDIA document 630-0049-001, Section 6.4 for environmental requirements.

9.3. **Solder Paste Stencil Printing** (use recommendations that apply)

9.3.1. Solder paste flux formulation to be rated Halogen Free.

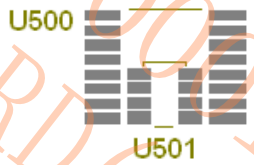
9.3.2. Solder paste stencil considerations:

9.3.2.1. All apertures to have trapezoidal openings and be electro-polished for improved solder paste release to PCB pads. See 630-0011-001 for example.

9.3.2.2. Improved process yield for solderability of micro-pitch (0.5mm) resistor networks may result from increased length of aperture (AKA:"over-printing the toe"). For uRnet aperture, refer to 630-0011-001 for recommended triangular apertures.

9.3.2.3. All micro-BGA memory apertures to be .016” square-openings per 630-0011-001, PCA Process Guidelines & Requirements. Please note .006” radius in each corner of the square apertures.

9.3.2.4. For multi-component land pattern designs on PCB, only open the solder paste stencil for the component actually used. Printing solder paste for all component pads can cause solder bridging issue. Remove all unused apertures from the solder paste stencil. DO NOT APPLY SOLDER PASTE TO UNUSED PADS.



Multi-component land pattern designs only open the solder paste stencil for the component actually used. Printing solder paste for all component pads can cause solder bridging issue.

Option I: Do NOT open 8-pin device (U501) if 16-pin device (U500) loaded. To avoid any solder bridging underneath the component.

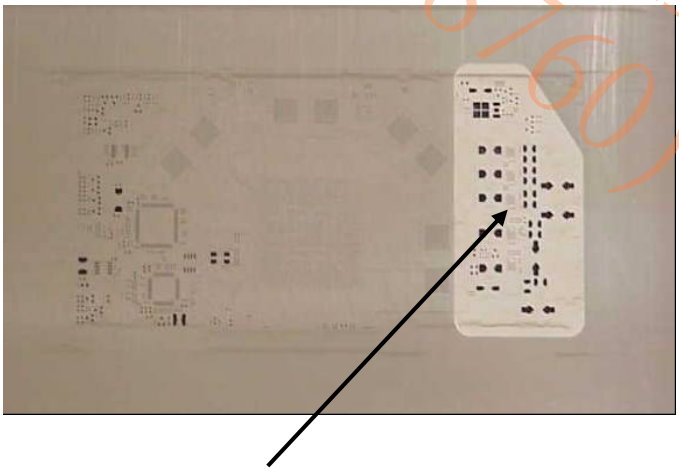
Option II: Open stencil for both devices if 8-pin device (U501) loaded. To avoid any oxidation on outside pads.

- Remove center pad aperture for inductors that do not have that feature on the part itself.
- Confirm per BOM all component locations that have “multiple overlapping pad designs” intended for optional part package size or substitutions. Select aperture for current build and loading prior to stencil manufacture.
- CM may adjust the solder mask layer of the Gerber file to cover unused pad areas per the component specified by the BOM version being utilized.

9.3.2.5. If intrusive reflow, PIP is the preferred process, ensure that aperture openings for through-hole components are calculated for the proper volume of solder paste and offset for wicking activity.

9.3.2.6. For CSP components; Micro-BGA (uBGA) type regulators and/or other 0.5mm ~ 0.65mm pitch components, follow the step-down recommendation as shown below:

- Reference NVPN630-0055-001; Page 3, Figure 6 for solder stencil design guidelines.



Example of stencil with step down from 5 mils to 4 mils in the uBGA area. Step-down on top side ONLY.

9.3.3. Solder paste stencil printer considerations:

9.3.3.1. Environmental control 18ºC to 24ºC is critical to ensure proper paste release from the stencil to the PCB pads.

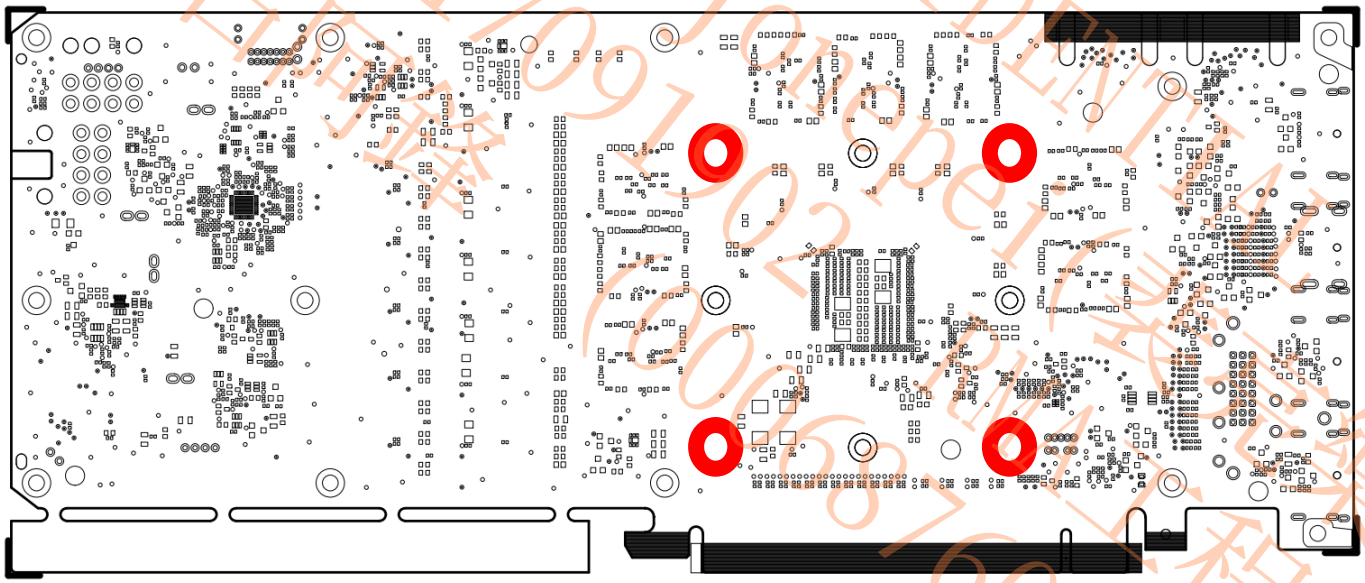
- Improper paste release is problematic for micro-pitch devices, such as uBGA's, 0.8mm pitch and 0.5mm pitch QFP's and 0.5mm pitch resistor networks (uRnet).

9.3.3.2. Stencil cleaning technique and frequency requires feed back from in-process inspection of solder paste deposition.

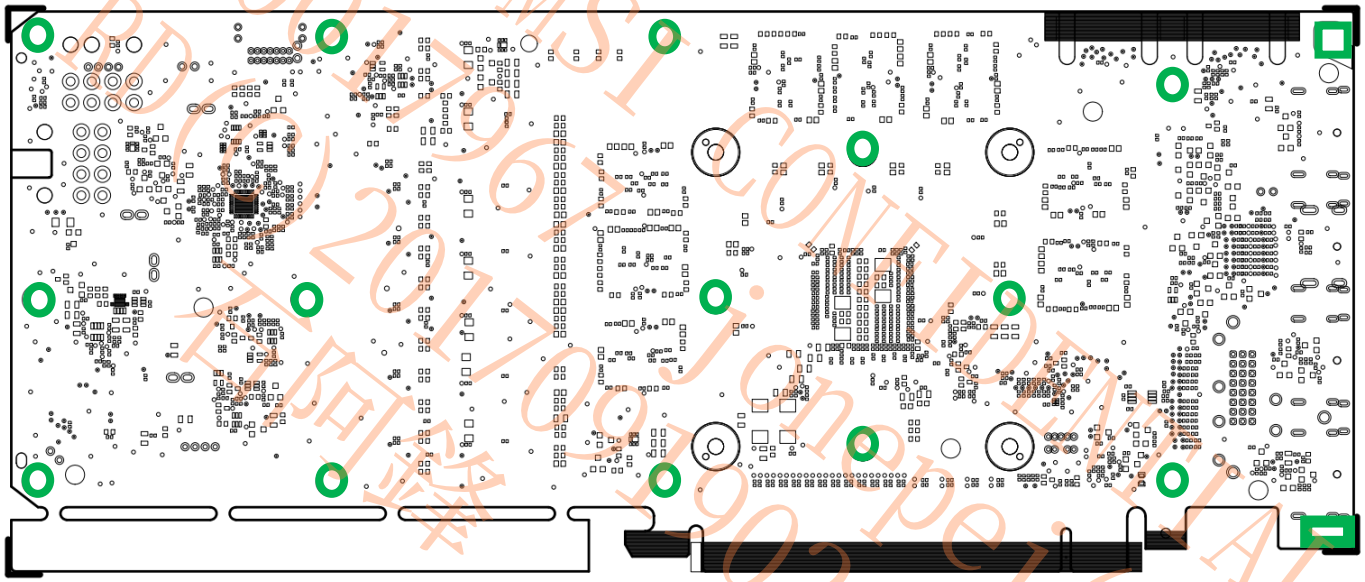
- Automated "In-Line" 2D paste inspection equipment is required for high volume production quantities.
- Manual inspection with 10X microscope is allowable for low volume production quantities.

9.3.4. Open stencil for mounting holes. Refer to doc 630-0225-001 for more info.

9.3.4.1. Cooler mounting holes (4X, bottom side only) - 35 mils round aperture, 50 mils minimum pitch with openings spaced evenly. 10 mils clearance from drill edge.



9.3.4.2. Cooler & Bracket mounting holes (16X) – 15 mils round aperture, 30 mils minimum pitch with openings spaced evenly. 10 mils clearance from drill edge. Note: open bottom side ONLY as shown below.



9.3.5. Open stencil for test points. Refer to doc 630-0225-001 for more info.

9.3.5.1. Open for both top and bottom sides.

9.3.5.2. Two (2) mils reduction of the **pad diameter**.

9.4. Component Placement

9.4.1. Ensure that equipment maintains accuracy of placement as defined by X-Y Centroid data.

9.4.2. The component values must be verified with an LCR meter to ensure that the correct reels are installed onto the feeders.

9.5. Reflow

9.5.1. Thermal profiling is required to verify the actual temperatures at critical points of the assembly. Separate profiles are required for each side with regard to double-sided SMT assemblies. Refer to 630-0011-001 and 630-0035-001 for detailed descriptions.

9.5.1.1. Thermal couple attachments for BGA devices must be accessed by drilling through the PCB.

- The NVIDIA ASIC requires one center ball and one corner ball (pin 1).
- The component package temperature of the NVIDIA ASIC should be verified.
- If uBGA memory is present: one center ball and one corner ball.
- If intrusive reflow is incorporated the junction of the lead and through-hole needs to be verified.
- Volterra's CSP should have a thermocouple, reference NVPN630-0055-001.

9.5.2. With regard to uBGA process requirements.

9.5.2.1. Ensure that ramp-up rate is between 1.5ºC/sec and 2.5Cº/sec to avoid over-drying the flux.

9.5.2.2. Control the “soak time” (flux activation period) typically (145°C to 183°C eutectic) (145°C to 217°C Pb-Free) to the solder paste manufacturers recommended minimum requirement.

- Avoid burning off all the flux prior to solder reaching liquidus condition to prevent oxidation.
- If voids occur in BGA solder balls, then flux activation “soak time” is too short.
- Note: when applying mixed technology (ie; SAC solderpaste and eutectic BGA balls) profile optimization may be required to reduce voids in BGA balls. In some cases a change of suppliers or flux formulations of the solderpaste may be required to reduce voids.

9.5.2.3. Control time over liquidus between 60 and 90 seconds.

- Eutectic solderpaste with eutectic BGA balls, liquidus = 183°C
- SAC Pb-Free solderpaste with Pb-Free BGA balls, liquidus = 217°C
- SAC Pb-Free solderpaste with eutectic BGA balls, liquidus = 217°C
  - ✓ Not Recommended.
- Eutectic solderpaste with Pb-Free BGA balls, liquidus = 183°C
  - ✓ Note: Also control time above 217°C at 25 seconds minimum for SAC BGA balls. And, time above 183°C may be slightly over 90 seconds.

9.5.2.4. Ideal peak temperature: (the following recommendations give best results)

- Eutectic solderpaste with eutectic BGA balls, 215°C ±5C
- Pb-Free solderpaste with Pb-Free BGA balls, 245°C ±5C
  - ✓ Note: If **temperature sensitive RoHS components exhibit problems** due to reflow temperatures, then the peak may be reduced to 225°C to preserve the integrity of the component.
- Pb-Free solderpaste with eutectic BGA balls, 230°C ±5C
  - ✓ **Not Recommended**.
- Eutectic solderpaste with Pb-Free BGA balls, 230°C ±5C
  - ✓ Apply to BGA center and edge balls only. Other features of the assembly would not be taken into consideration.

9.5.2.5. Ensure that ramp-down rate does not exceed –2.5°C/sec.

9.6. **Manual Assembly**

9.6.1. Ensure that similar component bins are kept apart to reduce mixed loading/wrong location.

9.6.2. If using PIP or intrusive reflow, the through-hole components are inserted prior to SMT reflow.

9.7. **Wave Soldering** (Disregard if following intrusive reflow methods)

9.7.1. Spray Flux Dispensers must use Halogen Free rated flux.

9.7.2. Selective wave soldering fixtures, carriers and breakers must be serialized and have record of maintenance.

9.7.3. Thermal Profiling is required for wave soldering process. Refer to 630-0011-001 for additional details.

9.7.3.1. Note: There are two types of wave solder equipment and profiling techniques will vary for each configuration.

- Machines which do NOT have a “chip wave” or “lambda wave”. **This is the preferred configuration**. Particularly for the higher temperatures of the RoHS (Pb-Free) soldering process.
  - ✓ This allows the smooth “laminar wave” to be positioned as close to the preheater side of the solder tank as possible and keeps the PCB from cooling between preheat and the wave.
  - ✓ This also allows the conveyor to run at a slower rate and increase the dwell time in the wave solder and improve solder fill.
- Machines which DO have a “chip wave” or “lambda wave”. This feature is only useful for bottom side SMD components which are glued onto the PCB and soldered simultaneously with the PTH devices. **Not Preferred**.
  - ✓ The “chip wave” only takes up space and the PCB has to travel across a 10” ~ 12” (25cm ~ 30cm) space after leaving the preheater before reaching the solder wave. This causes the PCB to cool down below an acceptable level prior to wave entry.
  - ✓ Techniques such as speeding up the conveyor to cross this cold zone in less time and increasing the pre-heat and solder tank temperatures accordingly have been successful. But, this becomes even more difficult in the RoHS (Pb-Free) soldering environment.
  - ✓ Solder bridges and incomplete PTH barrel fill are directly related to the temperature of the PCB prior to wave entry.

9.7.3.2. The temperature profile should be monitored by a thermal couple set at the junction of the PTH component lead just inside the PCB PTH barrel on the “solder side” to verify:

- Ramp rate of the preheat section, not to exceed 2.5°C/sec.
- Verify Peak Pre-Heat temperature for flux activation.
  - ✓ Flux Mfg recommends 110°C ~ 125°C on the top surface of the PCB
  - ✓ Translated to the bottom surface is 140°C ~ 150°C
  - ✓ Many of the wave solder carrier/fixtures shield such a high percent of the PCB surface that it’s difficult to get correct readings by the methods prescribed by the flux suppliers.
- Cold Zone (space between pre-heat and solder wave) “thermal dip” and time must be kept to the absolute minimum. (for machines with chip waves only)
  - ✓ This is best achieved by running the conveyor speed as fast as possible, with higher pre-heater thermal settings, considering other profile characteristics.
  - ✓ Thermal Spike should not exceed 100°C from cold zone to solder wave entry.

- The temperature profile should be monitored by a thermal couple set at the top surface of the PCB under the PTH component, but not touching either PTH barrel on the "circuit side" to verify:
  - ✓ Flux Mfg recommends 110°C ~ 125°C on the top surface of the PCB.
- The temperature profile should be monitored by a thermal couple set at the junction of the PTH component lead just inside the PCB PTH barrel on the "component side" to verify:
  - ✓ To verify solder fill, the thermal couple should reach 240°C ~ 260°C by the end of the duration of the solder joint engagement in the solder wave.

9.7.4. Verify there are no flux, solder or smears on gold fingers. Protect the gold fingers by covering them with Kapton tape. Refer to document IPC-A-610, Class II for specific workmanship guidelines.

9.7.4.1. Removal of Kapton tape must be done at a Kapton Tape Removal Station equipped with an ionizer.

9.7.4.2. Adhesive residue from Kapton tape must be cleaned off gold finger contacts with IPA and a lint free cloth or equivalent. Reference 630-0002-001, PCB Gold Finger Cleaning Procedure.

9.7.5. Inspect solder joints per IPC-A-610, Class II.

9.7.5.1. **Note that some component symbols have dual foot-print designs and the holes from "common nets" will be very close or even have overlapping pads. After soldering the two holes may bridge or appear to be bridged, but are perfectly acceptable.**

9.8. General Touch-up and Rework Requirements:

9.8.1. Touch-up & Rework to be performed in accordance with IPC 7711 & 7721.

9.8.1.1. Solder Fountain (mini-wave) with adequate controls (impeller speed, dwell time, etc...) and fixture set-up for removal of multi-leaded PTH components.

9.8.1.2. Solder stations must have grounded tip (ESD safe) and controlled temperature. Metcal brand is preferred for tamper-proof temperature control and dynamic load response.

9.8.1.3. Soldering Iron tips to match the component types and lead sizes being assembled.

9.8.1.4. Flux core wire solder must be compatible with the no-clean flux used in preceding processes.

- All Flux must be rated Halogen Free

9.8.1.5. Liquid flux dispensers must be capable of selectively applying flux to very small areas (needle tip is preferred).

- Liquid flux must be compatible with the no-clean flux used in preceding processes.
- All Flux must be rated Halogen Free

9.8.2. BGA Rework to be performed in accordance with 630-0001-001.

9.8.2.1. Hot Air rework station to have the following capabilities:

- SRT 1100 or equivalent with vacuum nozzle pick-up and placement, split screen video camera alignment, bottom side pre-heater, computer controlled (ramp-up,

soak, peak temp dwell and ramp-down), profile capability & storage and file management for each PCA & device.

9.8.3. Flux residue acceptability and cleaning requirements:

9.8.3.1. No-Clean flux residue "on the solder joint" does not require cleaning.

9.8.3.2. Flux residue deposited via selective wave solder fixture openings or from touch-up operation on board surface requires cleaning.

9.8.3.3. CM may be required to clean flux residues on PTH solder joints used as “test points” to improve yield with regard to false contact failures at ICT.

9.8.3.4. White residues on the PCB surface, which sometimes occur from improper cleaning of No-Clean flux, are not acceptable.

9.8.3.5. Excessive flux residue, which typically occurs from adding liquid flux for rework, is not acceptable (if it is migrating across the solder mask surface).

9.8.3.6. Cleaning Practice:

- The cleaning solution must be effective to remove excessive no-clean flux residue. Consult the flux manufacturer or use ECO Cleaner 500 by YIK SHING TAT Industrial Co., Ltd or use Enviro-Gold #816 by EnviroSense.
- Use mild brushing action to loosen flux. **ONLY ESD SAFE** brushes are allowed for cleaning.
- To remove loosened flux residue and cleaning solution form the PCB surface, use Chem-Wipes or rinse with DI water.
- Suck drily with cotton cloth and blow with compressed air.
- Then bake the board.

9.9. **In Circuit Test** (If required)

9.9.1. NVIDIA requires 100% completed assemblies to be ICT tested and Boundary Scan tested, prior to functional test.

9.9.2. If the CM is responsible for ICT fixture and program development, refer to the following document number:

9.9.2.1. Design for Testability Guidelines, NVIDIA document numbers 630-0004-001 and 630-0009-001.

9.9.2.2. The Boundary Scan test port must be accessible. Do NOT cover the Boundary Scan Test Port with any “in-process labels. See **Figure X.**

9.9.3. NVIDIA *may* provide the first ICT fixture. CM to supply additional ICT fixtures as capacity dictates.

9.9.4. NVIDIA to provide CM with the design files (e.g., CAD file for Fabmaster) and/or design assistance to support ICT development.

9.9.5. CM is required to maintain and service the ICT fixture and program to NVIDIA specifications regardless of who provided the fixture and program.

9.9.6. CM is required to mark all assemblies that pass ICT and Boundary Scan test.

9.9.6.1. The mark must display the phrase “ICT” or “ICT Pass” and must be marked on the bottom-side of the assembly.

9.9.6.2. Do NOT apply test stamp over regulatory agency markings or other important silkscreen legends.

9.9.7. Assemblies that **FAIL** ICT:

9.9.7.1. **Must not** be marked “ICT” or “ICT Passed”.

9.9.7.2. CM must repair the individual assembly based upon the defect information supplied by the ICT tester or Boundary Scan test module.

9.9.7.3. CM must make such repair to the individual assembly within one week of failure or manufacturing date.

9.9.7.4. NVIDIA will provide replacements for defective Controllers on a one-for-one basis under the NVIDIA RMA policy/program. Please contact your NVIDIA sales person for RMA details. Reference OPSQA70026, Customer Return Material Authorization (RMA) Policy for External Use.

9.9.7.5. Individual assemblies known to have failed ICT three times may not be shipped to NVIDIA.

9.10. **Labels**

9.10.1. General Labeling Requirements:

9.10.1.1. Always refer to the Final Configuration Instructions (FCI) for workstation products for final label requirements. Customer specific SKU’s may also replace NVIDIA generic labels with OEM specific labels.

9.10.2. In-Process Labels:

9.10.2.1. Special care must be exercised to ensure that “In-Process” labels NEVER cover Test Points, Boundary Scan Test Port, Through-Hole Pads, Silk Screen Legends or “Etched Information” in the Bare Board Fab Artwork.

9.10.2.2. In-Process Labels must be made from non-conductive High Temperature materials, such as polyimide or Teflon. Note: Metallized labels must never be used.

9.10.2.3. The NVIDIA serial number label or OEM serialized ID labels MUST be affixed to the bare PCB before the assembly process. This will facilitate WIP tracking of the assembly through the SMT, post-SMT processes and RMA traceability. Refer to section 6.3.1.

- Traceability Label with equivalent information.

9.10.2.4. NVIDIA Serial Number (S/N) label: Refer to specification 136-10000-0000-001 on how to create it. Refer to **Figure 1a** for label placement location on the PCA.

9.10.2.5. During prototype or control lot build schedules; **replace** the standard NVIDIA S/N Label with NVIDIA Model & Sales Sample S/N Label 136-80000-0000-000.

- **During a Proto or Control Build, use the “scribed number” as found on the NVIDIA supplied graphic controller chip (BGA) to enter the “SSS” information into the label. Ensure that the numbers match.**

9.10.3. Post Operation Labels:

9.10.3.1. Post operation labels must never be applied until after the PCA has passed Functional Test. The BIOS Label must not be affixed until after successful BIOS flash.

9.10.3.2. BIOS version label: Refer to specification 136-40000-0000-001 to create this label. Refer to FCI documentation and 900-Level BOM for any changes to label placement location and printed information (see **Figure 1a**).

- **BIOS Version information is located in 621-10MMM-xxxx-xxx of the 600-Level-BOM.**
- If pad-printing technique is preferred, pre-programmed EEPROM's or Serial Flash Memory may have the BIOS version pre-printed directly on the IC body with permanent white ink.
- Re-Programming of EEPROM's or Serial Flash Memory requires the use of a label to cover previous version printing if applicable.

9.10.3.3. Functional Assembly Part Number (P/N) Label 136-00000-0000-003: Refer to specification 136-00000-0000-002 to create this label. See **Figure 1a**.

- Refer to 630-0034-001 for CEM code and Country of Origin.
- Some OEM customers may choose to substitute this label with their own label. This can only be allowed if the country name is clearly recognizable, not coded.

9.10.3.4. FCC/CE Disclaimer Label: **(Prototype and Control lot ONLY)** 136-00000-0000-005. Refer to spec 136-00000-0000-004 to create label "not for EMC testing".

- Ensure that the FCC/CE disclaimer label covers the silkscreen compliance logo until agency approvals are received (see **Figure 1a**).

9.10.3.5. Regulatory Agency Labels: Refer to the 900-Level-BOM to determine which labels should be required. Refer to the Final Configuration Instruction (FCI) to verify placement location.

9.11. **General Mechanical Assembly Requirements:**

9.11.1. Micro-Strain Testing:

9.11.1.1. Refer to the current IPC/JEDEC-9704 Guideline for the strain gage test method and allowable strain limits

9.11.1.2. All mechanical assembly operations need to be tested based on the NVIDIA DA-05931-001 specification. Recent investigations have revealed that stressed, cracked and broken solder joints are often a result of mechanical strain.

9.11.1.3. Free-Hand operations that cause an excess of allowable strain limit must be converted to fixtured operations.

9.11.1.4. Fixtured operations need to verify stress points, which may exceed allowable strain limit. Fixtures must be modified to support strategic locations to ensure that stress points do not exceed allowable strain limit. Key operations that need to be examined are:

- Kapton tape removal
- Heatsink, Fansink, Blower installation
- Bracket attach

- ICT fixture

  NOTE: The CM has the responsibility for providing the required fixtures

9.11.1.5. All final mechanical assembly and second operations must be completed prior to routing the product to functional test.

9.11.1.5.1. It is important to minimize the possibility of handling damage post FT.

9.11.1.6. All torque drivers used to assemble NVIDIA products must be calibrated before every shift to the value specified for each operation. The calibrated readings should be documented.

9.11.1.6.1. Ensure that the speed selection is set on “Low” for torque specifications below 2.5in-Lb.

9.11.1.6.2. Torque drivers must be purchased based on the following torque ranges:

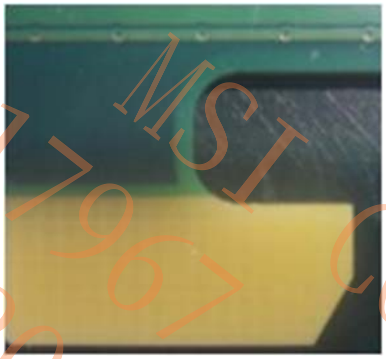
- Range 0.5 ~ 4.5 in-Lb for screw torque requirements 0.75 ~ 1.75 in-Lb
- Range 1.0 ~ 6.5 in-Lb for screw torque requirements 1.75 ~ 4.0 in-Lb.
- Range 1.7 ~ 10 in-Lb for screw torque requirements 4.0 ~ 6.0 in-Lb.

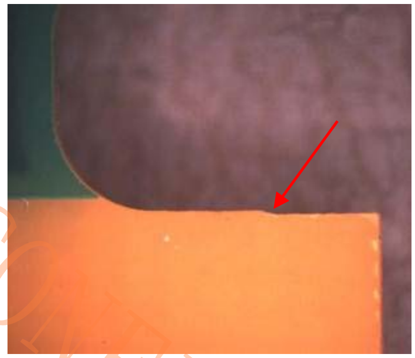
9.11.2. Breakaway Tab Requirements:

9.11.2.1. If any v-score tabs or v-score depanelization should be required, a proper cutting machine is required. DO NOT break by hand.

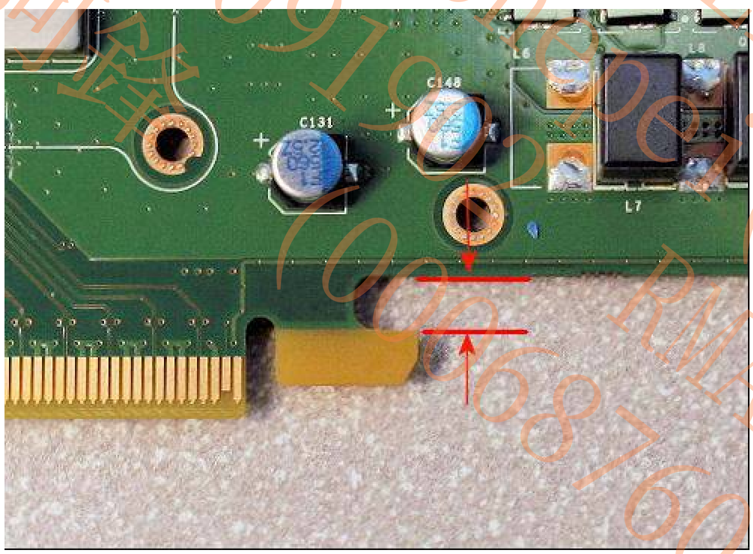
9.11.2.2. The latch blocker tail should be removed unless specified otherwise in FCI (625-50XXX-XXXX-XXX) documentation. To removed the latch blocker tail, use the following process:

- Remove using a router or equivalent.
- Jagged surface is NOT acceptable.


ACCEPTABLE


NOT ACCEPTABLE W/ JAGGED SURFACE

- Maintain at 4.80 +/-.13mm. See figure below.



9.11.3. <u>Bracket, Stiffener, Extender, and Hardware</u>

Note: The thermal solution (heatsink/fansink) MUST be installed before the bracket attachment. **Please review Thermal Solution Installation before performing this task.**

9.11.3.1. Insert the South trim to a fansink base slots as shown in **Figure 2a.**

9.11.3.2. Install M2.5x4.0mm socket head screws (2X, silver color) to temporary hold it to the fansink base as shown in **Figure 2b**. The screws should be loose, not tighten.

9.11.3.3. Insert the North trim to a fansink base slots as shown in **Figure 2c.**

9.11.3.4. Install M2.5x4.0mm socket head screws (2X, silver color) to temporary hold it to the fansink base as shown in **Figure 2d**. The screws should be loose, not tighten.

9.11.3.5. Align and gently place the TOP COVER-RIGHT on baseplate as shown in **Figure 2e.**

9.11.3.6. At the bottom of the fansink base, secure the cover-right to baseplate with M2.5x5.0mm Philips wafer head screws (2X, black nickel). Torque screws to 3.0~3.5 in-lbf in sequence as shown in **Figure 2f**.

9.11.3.7. Secure cover-right to baseplate with M2.5x5.0mm Philips wafer head screws (2X, black nickel). Torque screws to 3.0 ~ 3.5 in-lbf in sequence as shown in **Figure 2g**.

9.11.3.8. Remove adhesive protection sheet from a LED Logo, then align and affix it to Center Cover. Check and ensure LED Logo firmly stays on Center Cover and no paint is chipped or scraped as shown in **Figure 2h.**

9.11.3.9. Align and install assembly center cover (with LED Logo) to fansink base as shown in **Figure 2i**.

9.11.3.10. Secure center cover to baseplate with M1.6x4.5mm LONG PHILLIPS WAFER HEAD (4X, black nickel). Torque screws to 1.5 ~ 1.7 in-lbf in sequence as shown in **Figure 2j**.

9.11.3.11. Connect the LED wire to a two pins header on the main board as shown in **Figure 2L**.

9.11.3.12. Twist (approx. one full twist per centimeter) and insert fan power cable to the 4-pin header as shown in **Figure 2m**.

9.11.3.13. Align the baseplate on topside of the board with orientation as shown in **Figure 2n**.

9.11.3.14. Then install M2.5xL2.7mm standoffs (14X, black Zn) through PCB holes to the baseplate, torque screws to 2.2~2.6 in-Lb in sequence as shown in **Figure 2o**.

9.11.3.15. Align and gently install the TOP COVER-Left to the baseplate as indicated in **Figure 2s**.

9.11.3.16. Secure right and left cover to center cover with M2.5x4.0mm socket head screws (4X, silver color). Torque screws to 3.0~3.5 in-lbf in sequence as shown in **Figure 2t**.

9.11.3.17. Install M2.5x4mm socket screws (2x, black zinc) to baseplate. Torque screws to 3.0~3.5 in-lbf in sequence. See **Figure 2u**.

9.11.3.18. Now secure the north and south trims to baseplate by torqueing the socket screws to 3.0~3.5 in-lbf as shown in **Figure 2v**.

9.11.3.19. Align back cover (SKU fixed) screw holes on bottom side standoffs with orientation as shown in **Figure 2x**.

9.11.3.20. Then install M1.4x3mm flat head screws (6X, black Zn) through the back cover holes to the standoffs, torque screws to 0.5 +/-0.05 in-Lb in sequence as shown below in **Figure 2y**.

9.11.3.21. Align Back cover (SKU removable) on bottom side of the standoffs with orientation as shown in **Figure 2z**.

9.11.3.22. Then install M1.4x3.0mm Flat HEAD screws (8X, black Zn) through the back cover holes to the baseplate, torque screws to 0.5 +/-0.05 in-Lb in sequence as shown in **Figure 2aa.**

9.11.3.23. Align bracket to the board assembly. Secure bracket to the DP connectors with M2.0x4.0mm PHILLIPS FLAT HEAD screws (3x, black nickel). Torque to 1.5 ~ 1.7 in-lbf in sequence as indicated in **Figure 2ab**. **Caution:** Make sure the DP and HDMI connectors (the Springs/tabs) no bend/damaged.

9.11.3.24. Then install M2.5x6mm Philips flat head screws (2x, black nickel) to the baseplate through bracket. Torque to 3.0 ~ 3.5 in-lbf in sequence as shown in **Figure 2ac**.

9.11.3.25. Then install Jackscrew (2X), torque all Jackscrews using a calibrated torque driver to 6.0~7.0 in-lbf in sequence as shown in **Figure 2ad**.

9.11.3.26. Push the bracket inward as necessary to align the hole of the bracket tab with PCB mounting hole. Then secure the tab to the PCBA and cooler with M2.5x7mm Philips flat head screws (2x, black Zn). Torque to 4.0 ~ 4.5in-lbf as shown in **Figure 2ae**.

9.12. **Thermal Solution Installation:**

Note: Only boards that have passed ICT may have the heatsink or fansink installed.

9.12.1. Thermal Solutions that require Thermal Grease:

9.12.1.1. Always perform a First Article inspection to ensure that the thermal grease is making full contact with the GPU die surface.

- After assembly of the First Article samples, remove the thermal solution and verify that the GPU die is fully coated with thermal grease and that there is a full impression of the GPU die in the grease on the heatsink surface. If the result is not acceptable, notify NVIDIA engineering.

9.12.1.2. If a heatsink/fansink needs to be removed from a graphic card for debug, etc… then the original thermal grease needs to be cleaned off and new thermal grease needs to be applied.

- NVIDIA recommends the use of a stencil, per 630-0003-001 when applying replacement thermal grease.

9.12.1.3. NVIDIA recommends ShinEtsu X23-7762 thermal grease to form a new thermal interface with the GPU die when thermal solutions are removed and replaced.

9.12.2. Thermal Solutions that require Thermal Putty, Thermal Cushion, or Thermal T-FLEX Material:

9.12.2.1. Always perform a First Article inspection to ensure that the thermal putty/cushion/T-FLEX is making full contact with the memory and/or power regulator devices surface. If the result is not acceptable, notify NVIDIA engineering.

9.12.2.2. Thermal Putty, Thermal cushions, or Thermal T-FLEX are to be applied to the memory and/or power regulator devices of the PCA prior to fansink and/or heatsink installation. See **Figures 2k and 2w**.

- When handling the ~1/2” size pads, typical for memory devices, always use X-Acto #18 chisel blade.
- When handling the ~1/4” size pads, typical for regulator devices, always use X-Acto #17 chisel blade.

9.12.3. Thermal Solution attachment with Screws:

9.12.3.1. Refer to document 630-0003-001 for general heatsink attachment process requirements.

9.12.3.2. Installation fixture(s) are mandatory for this operation. The fixture must provide proper support and alignment for the hardware installation.

9.12.3.3. Before installing heatsink modules, check and ensure foam strip is pre-installed on each GPU cooler module as shown in **Figure 2p**.

9.12.3.4. Ensure that the heatsink/fansink is aligned to the correct orientation as shown in **Figure 2q**.

9.12.3.5. Always install screws around the GPU prior to installing the other screws around the memory portion of the fansink.

- Install the baseplate first, then GPU heat sink module.

9.12.3.6. Follow the torque sequence as shown in **Figure 2r**.

- Add Loctite 242 Threadlocker (3~5 threads from tip) if any screw doesn't come with Nylok coating.
- Set the torque to 4.0~4.5 in-Lb for baseplate screw
- Set the torque to 3.0~3.5 in-Lb for GPU heatsink module spring screw
- Check the interface between the heatsink and the memory devices to ensure that there is no air gap between them
  - ✓ If a gap is found, check to see if there is any component interference or if the spring may have entered the PCB hole with the screw and notify NVIDIA engineering.

9.12.3.7. Check for excess thermal interface material (TIM). Ensure no TIM outside the perimeter of the cooler.

9.12.4. Connecting, Dressing and Securing the service loop of the fan power cord:

9.12.4.1. Ensure that enough "service loop" is present to un-plug the fan connector if required.

9.12.4.2. Ensure that the fan wires are twisted. Approx. 1 full twist per centimeter.

9.12.4.3. Before connecting the fan wire to PCBA header, check and ensure fan wires straighten and properly hold down by clamp, not interfered with the cooler fan. See **Figure 2m**.

9.12.4.4. Install fansink power plug into the 4-pin header on the board as shown in **Figure 2m**.

9.12.4.5. Dress the service loop in a manner that keeps the wires away from the gold fingers, inside the perimeter of the PCB and away from noise sensitive circuitry.

9.12.4.6. Ensure the cable wire route as shown in **Figure 2L and 2m**. Keep the wire away from the fan.

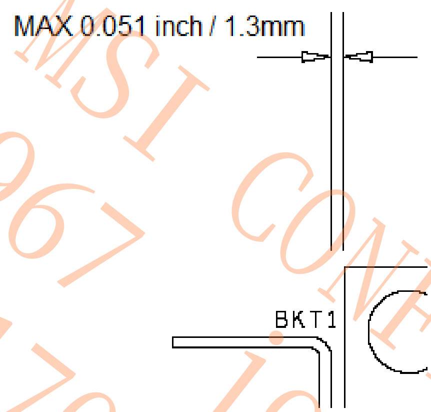
9.13. **CM Final Inspection**

9.13.1. Perform 100% Visual—Mechanical Inspection (VMI) on all PCA's using IPC-A-610, Class II guidelines and this MPI.

9.13.2. Verify there are no flux, solder or smears on gold fingers. Refer to document IPC-A-610 for specific workmanship guidelines. If cleaning of gold fingers is required, refer to document 630-0002-001 or the Addendum to this MPI.

9.13.3. Inspect to ensure no loose hardware exists. Bracket hardware torque must be 4.2~5.2 inch lbs. and the bracket must be applied 90 degrees to the AGP edge connector.

9.13.4. Measure the gap between the front edge of the PCB and the backside of the bracket with a feeler gauge. The dimension should be no more than 0.051 inch or 1.3mm for PCI-E. See Figure below



Gap allowance, front edge of the PCB and backside of the bracket.

9.13.5. Verify labels applied to this board comply with SKU requirements of the 900 level assemblies you are building.

9.13.6. Verify the BIOS label displays the version to which this board was flashed.

9.14. Packing

9.14.1. PCA Packaging: (refer to 900-BOM and Final Configuration Instructions)

9.14.1.1. ESD bag and ESD label as shown in **Figure 4**.

9.14.1.2. Use ESD bag per part number sub BOM 500-10000-xxxx-xxx.

9.14.1.3. Insert bracket-end of board into metalized ESD bag and fold bag (Do Not Staple).

9.14.1.4. Apply ESD label 135-00000-0000-001 to bag per IPC-A-610 and industry standards.

NOTE: DO NOT cover important "bar code readable" PCA labels on the product contained within the ESD bag.

9.14.2. Out of the Box Audit (OBA) - This inspection shall be done prior to shipping carton sealing.

9.14.2.1. Perform OBA using a sampling plan of 0.065%AQL LII.

- Lot size of 0 - 200, sample size = 100%
- Lot size of 201 – 10,000, sample size = 200 units.
- Pull random samples from the shipping carton. If (1) defect is found the entire lot must be re-screened.

9.14.2.2. Verify labels against the customer requirement.

- Perform bar code test using bar code scanner (if applicable).

- Review all documents (if applicable) accompanying the lot for accuracy.

9.14.3. Final Packaging: (refer to 900-BOM and Final Configuration Instructions)

9.14.3.1. Refer to sub BOM 500-10000-xxxx-xxx generic Shipping carton specification.

9.14.3.2. Apply Shipping Label per the 900 SKU you are shipping.

9.14.3.3. Board quantities/carton are packed per 900-BOM requirements unless otherwise specified by customer file, or PO.

9.14.3.4. Cartons are to be sealed with either an NVIDIA approved tamper evident tape, or with standard tape and application of tamper evident over-label. Reference NVIDIA document OPSMC0016. See **Figure 5**.

- Part Numbers for the tamper evident tape and tamper evident over-label available on the NVIDIA 500-Level BOM.

9.14.3.5. If shipping cartons are palletized, ensure boxes are cross-weaned for stability in shipping.

9.14.3.6. If shipping ORT units, the packaging will be labeled clearly on the outside as “ORT UNITS”.

- These units are to be shipped to:

  NVIDIA Corporation

  920 George Street

  Santa Clara, CA. 95054-2705

  Attention: Terence Daquioag

9.14.3.7. Please forward Tracking Information to NVIDIA Reliability Engineering or Quality Management on each shipment.

10. RECORDS

10.1. All quality data, ship-to data, repair data and RMA data are to be maintained by the CM for the duration of the warranty period.

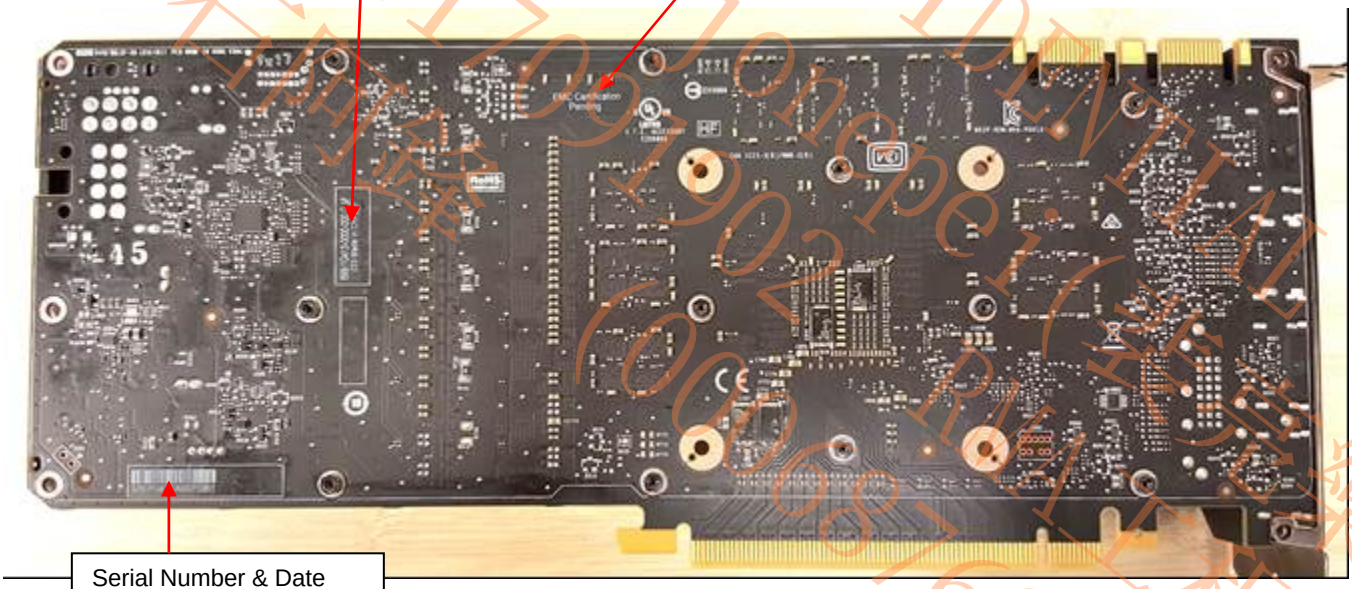
11. APPENDIX

11.1. Process Figures (**Figures 1** through **5)**

Appendix

(Refer to the FCI for the SKU that you are building for final label requirements)

Figure 1a: PG413 bottom-side showing label placement.



Note: If the labels on fab are covered, add another set of PN and SN labels outside on back cover as shown.

Figure 1c: To avoid PTH lead interferes with all back covers assembly. Ensure all PTH leads protrusion length NOT exceed 1.20 mm. Trim the lead where necessary. Note: No need to cut the plastic pins.

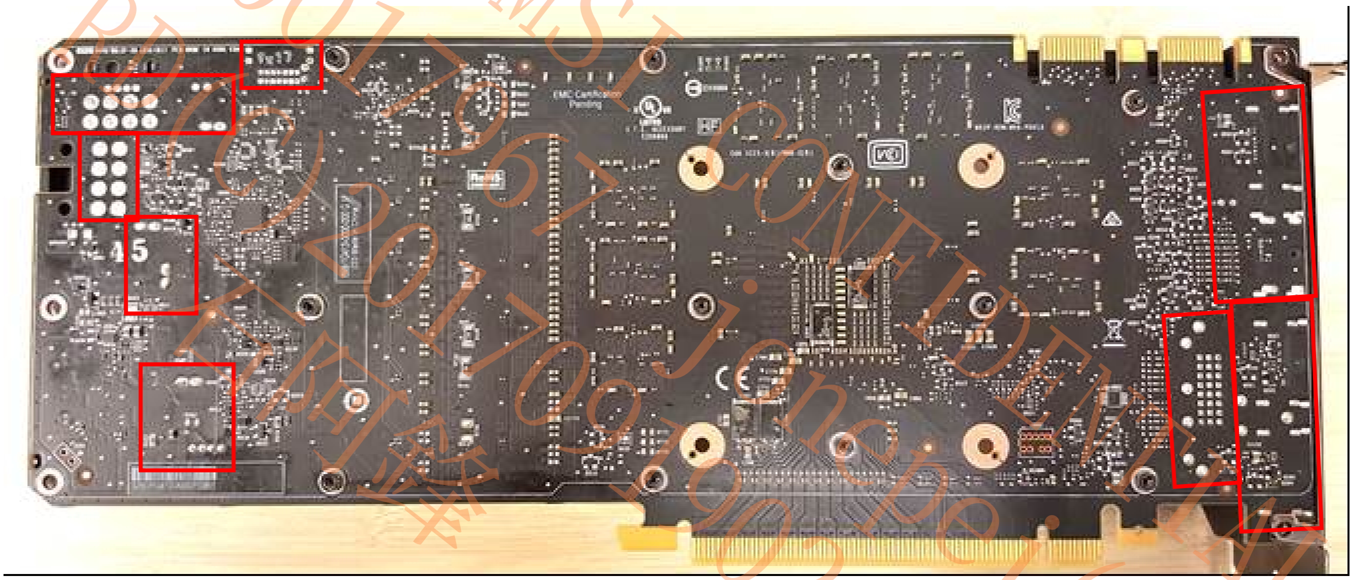
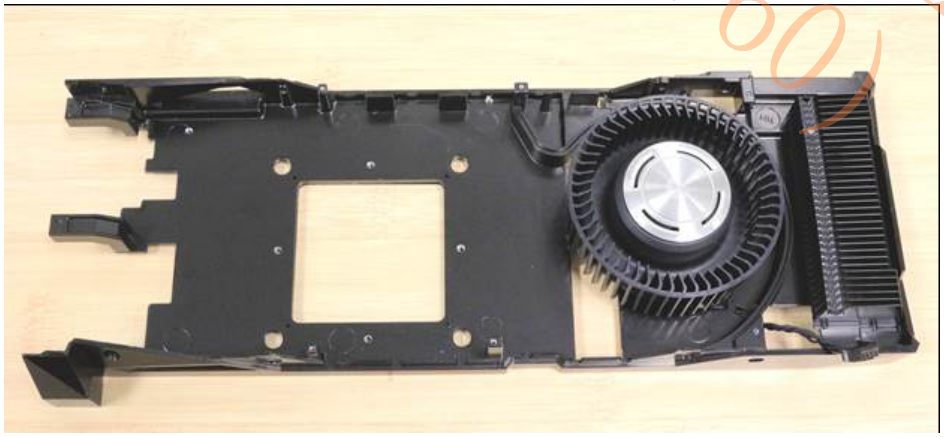


Figure 1d: I/O bracket parts list

Figure 1e: Cooler parts list

Fansink base:

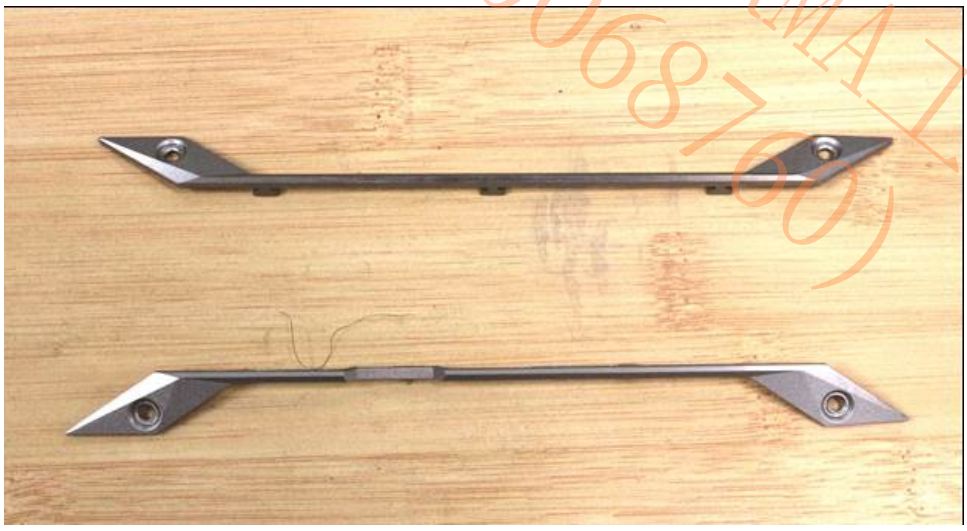


Back covers:

Heatsink Modules:

Top Covers (Center/Left/Right):

Trim Covers (North & South):



LED Logo:

Figure 2a: Insert the South trim to a fansink base slots as shown.

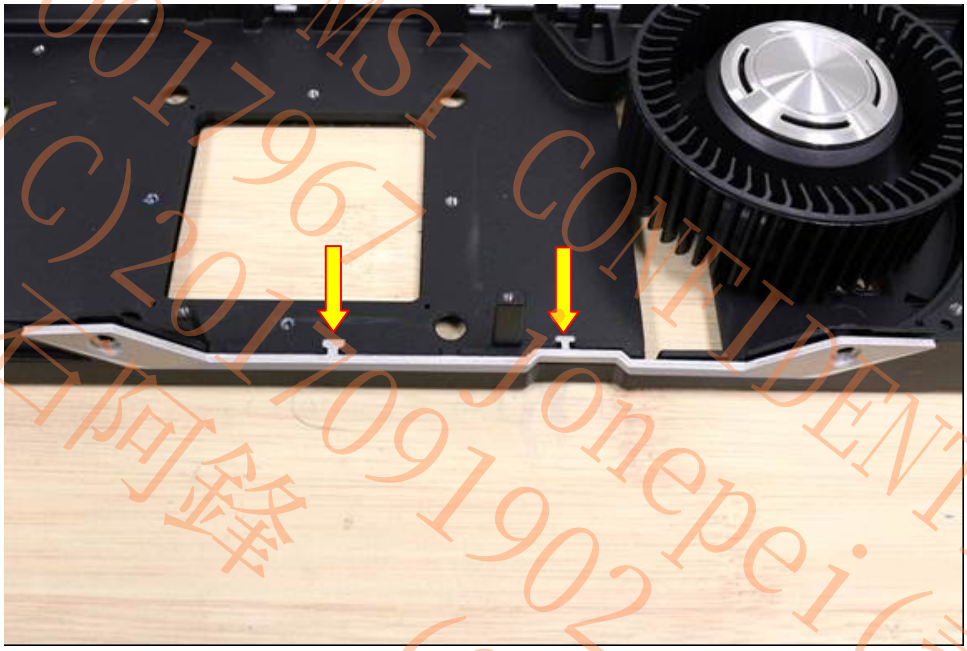


Figure 2b: Install M2.5x4.0mm socket head screws (2X, silver color) to temporary hold it to the fansink base. The screws should be loose, not tighten. **Note:** add Loctite 242 Threadlocker (3~5 threads from tip) if screws aren't come with Nylok coating.

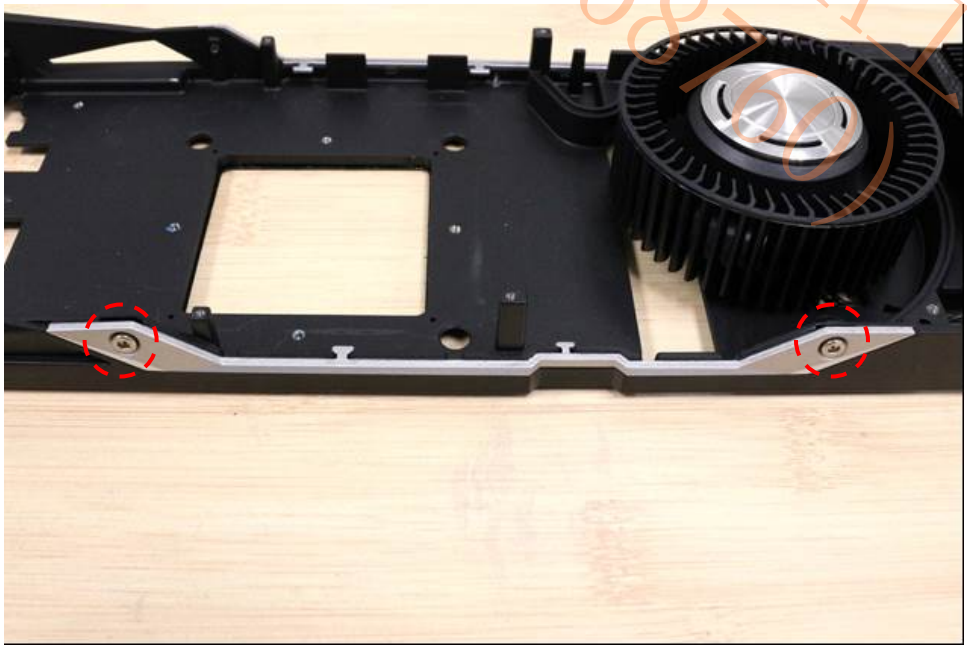


Figure 2c: Insert the North trim to the fansink base slots as shown.

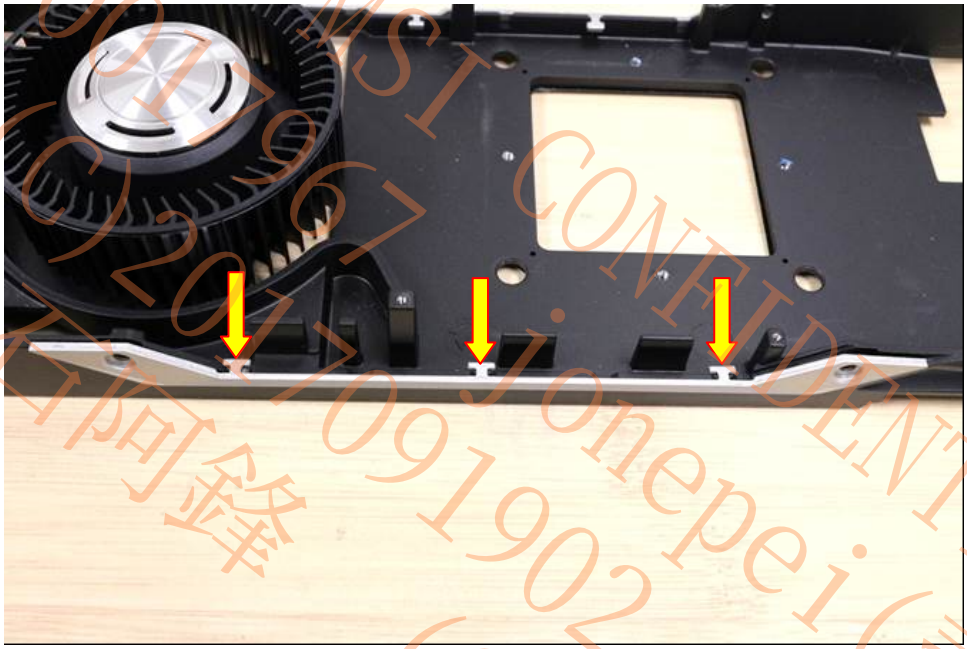


Figure 2d: Install M2.5x4.0mm socket head screws (2X, silver color) to temporary hold it to the fansink base. The screws should be loose, not tighten. **Note:** add Loctite 242 Threadlocker (3~5 threads from tip) if screws aren't come with Nylok coating.

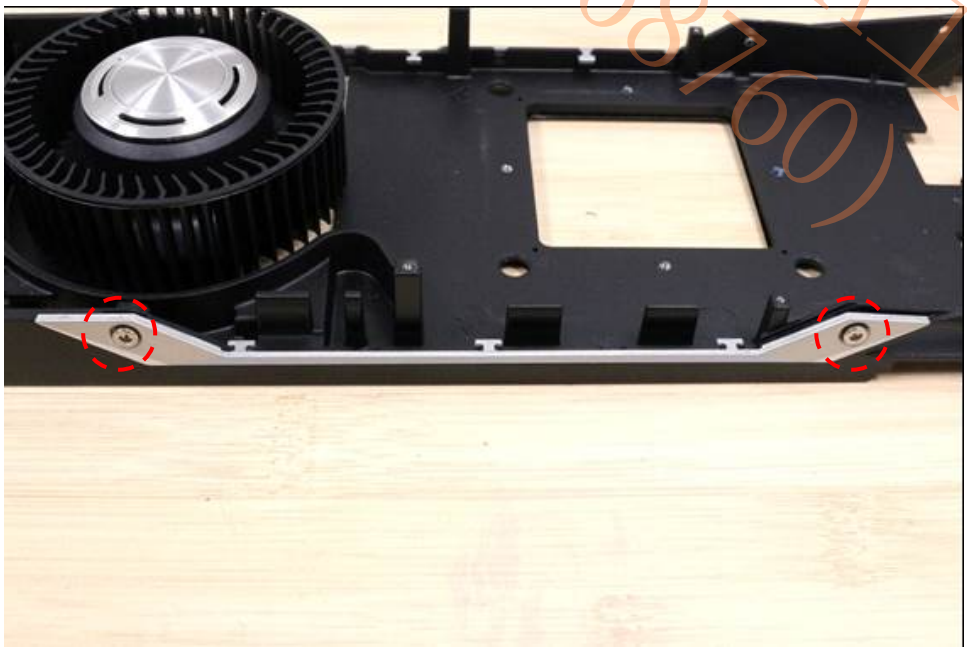


Figure 2e: Align a Top Cover-Right on top of the Fansink base as shown.

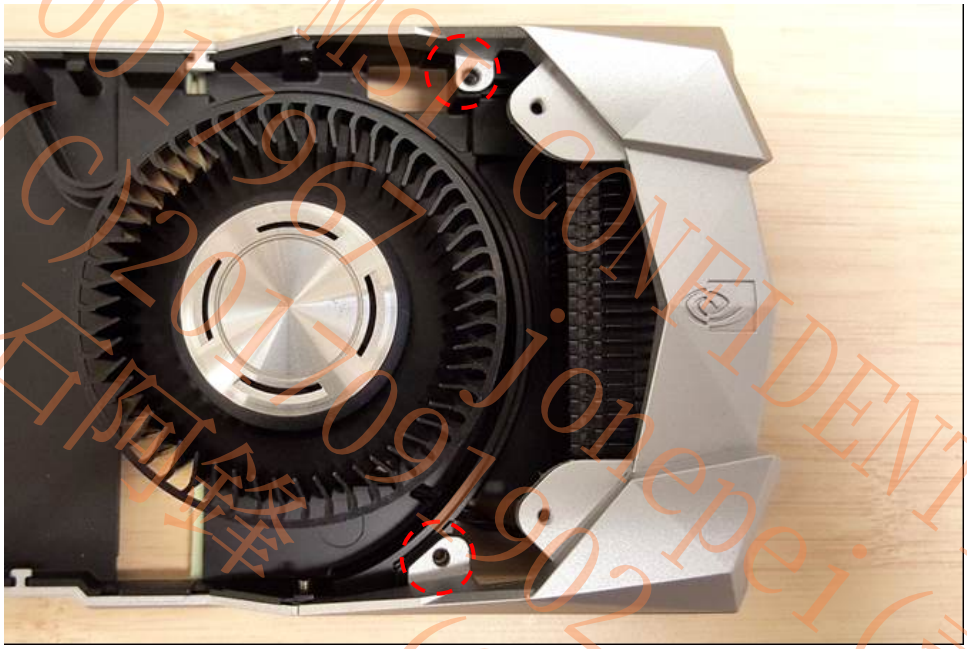


Figure 2f: At the bottom of the fansink base, secure the cover-right to baseplate with M2.5x5.0mm Philips wafer head screws (2X, black nickel). Torque screws to 3.0~3.5 in-lbf in sequence as indicated. Note: add Loctite 242 Threadlocker (3~5 threads from tip) if screw doesn't come with Nylok coating.

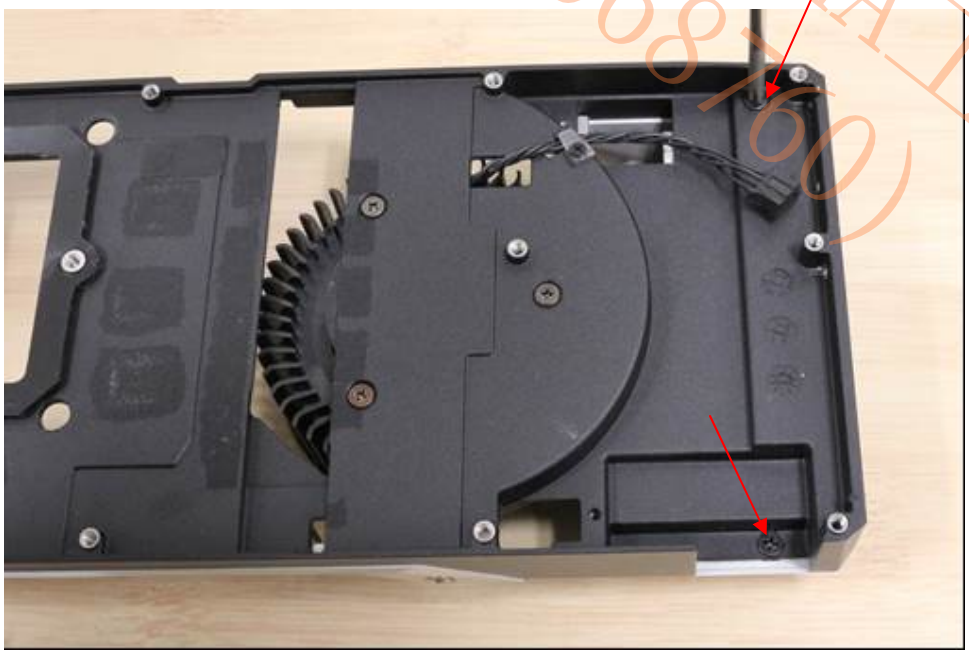
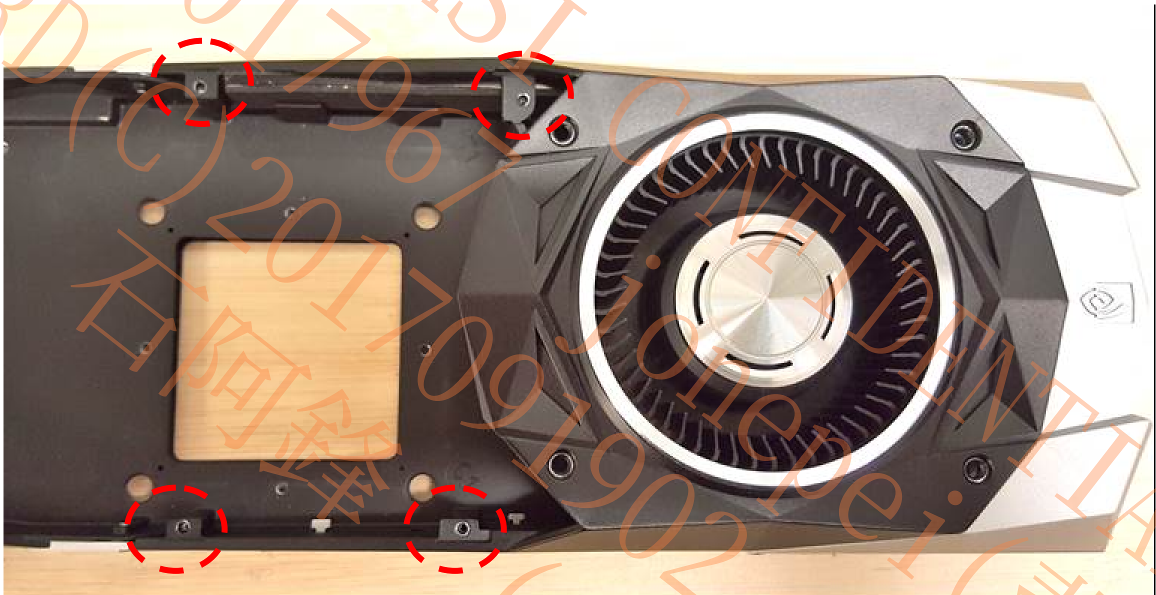
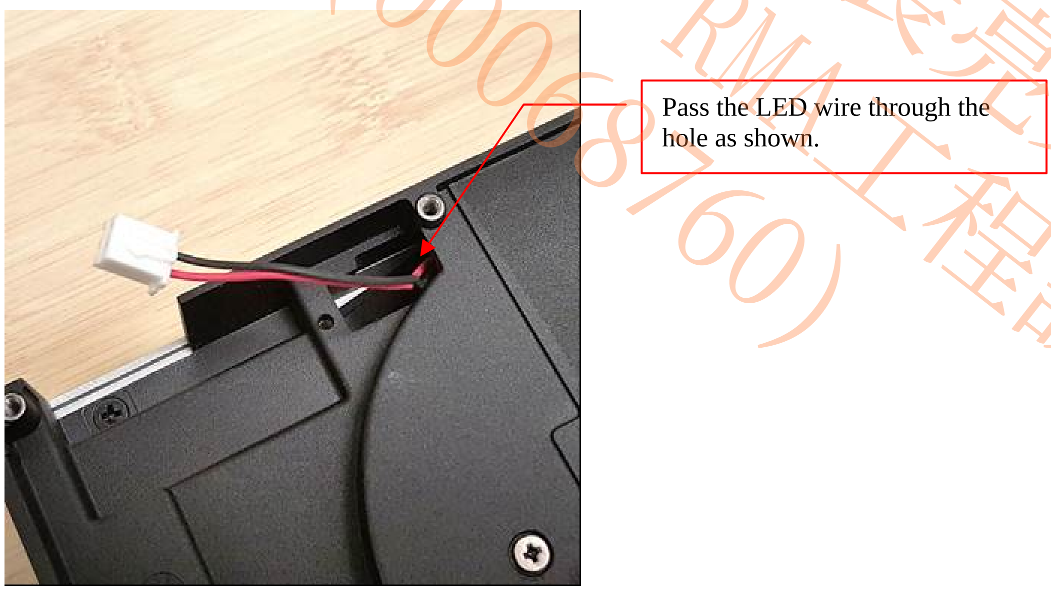


Figure 2g: Install M2.5x5.0mm Philips wafer head screws (2X, black nickel) through top cover holes align to the baseplate, torque screws to 3.0 ~ 3.5 in-Lb in sequence as shown below. Note: add Loctite 242 Threadlocker (3~5 threads from tip) if screw doesn't come with Nylok coating.

Figure 2h: Remove adhesive protection sheet from a LED Logo, then align and affix it to Center Cover. Check and ensure LED Logo does firmly stay on Center Cover and no paint is chipped or scraped.

Figure 2i: Align and install assembly center cover (with LED Logo) to fansink base. ***Note: a) Ensure the LED cable is not caught between the center cover wall and fansink base. 2) The LED Logo tape should not be seen outside the fansink base after assembly.***





While the center cover placing on top of the baseplate, ensure the fan wires do **not** come out the wall. Otherwise they are going to be smashed in between of the cover and baseplate.

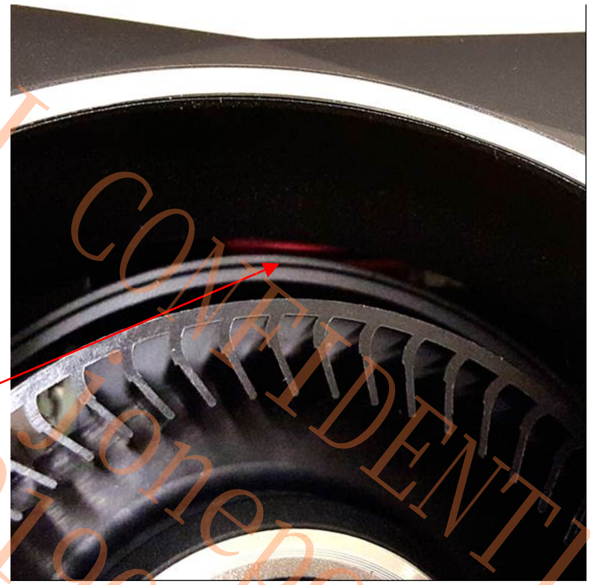


Figure 2j: Secure center cover to baseplate with M1.6x4.5mm PHILLIPS WAFER HEAD (4X, black nickel). Torque screws to 1.5 ~ 1.7 in-lbf in sequence as shown below. **Note:** add Loctite 242 Threadlocker (3~5 threads from tip) if screws aren't come with Nylok coating.

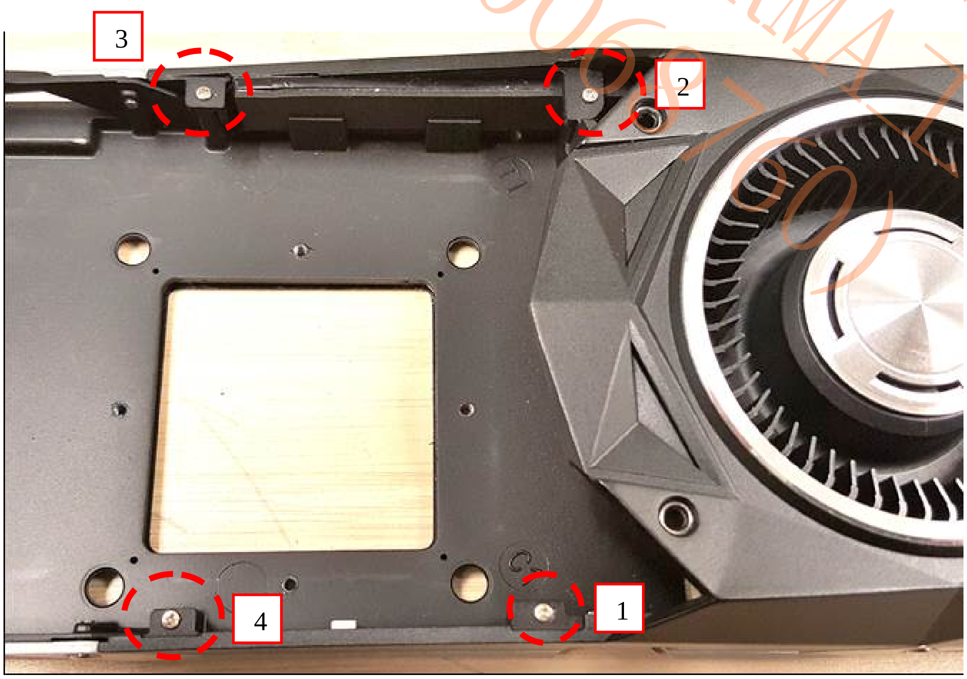


Figure 2k: Install Thermal Interface Material (TIM) center on top of Memories, FET, and others components.
Note: a) Always check against latest BOM/Cooler Spec for correct P/N, QTY, and Location.
b) Some of the TIMs are very close to each other, make sure they do **not** overlap on top of each other.
c) Clean mating surfaces on the components with isopropyl alcohol and let them dry prior the TIMs installation.

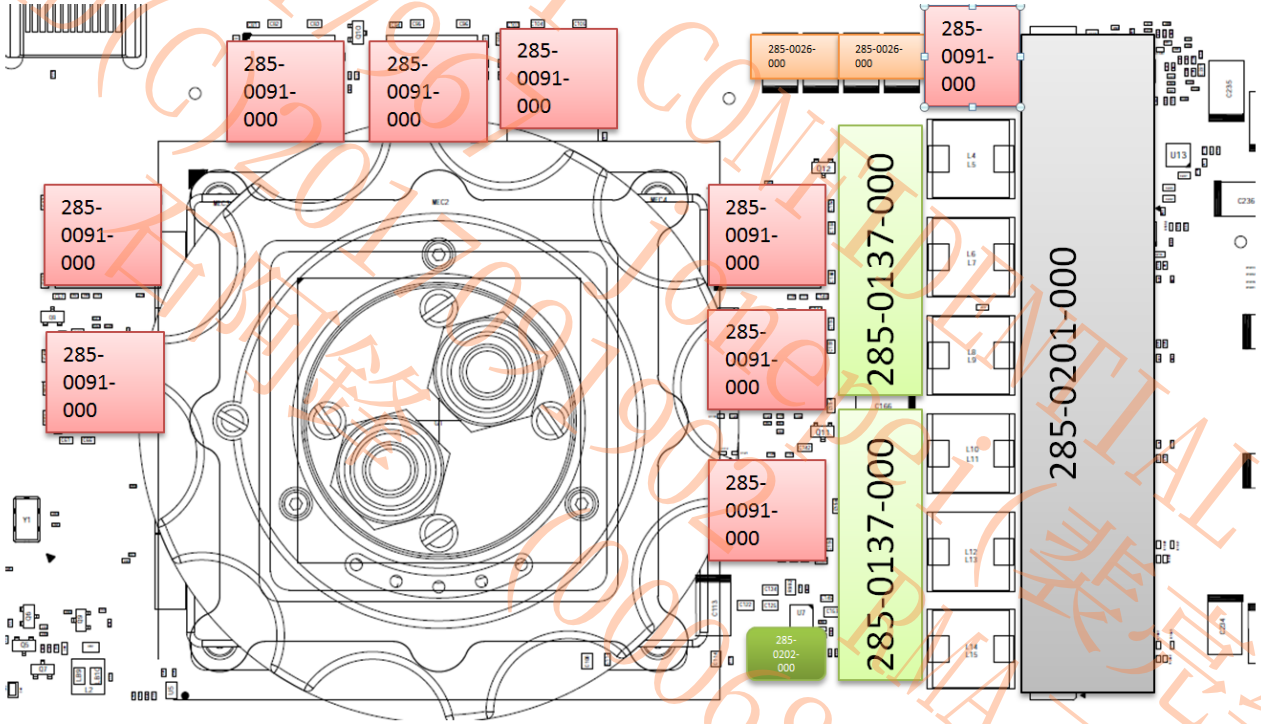
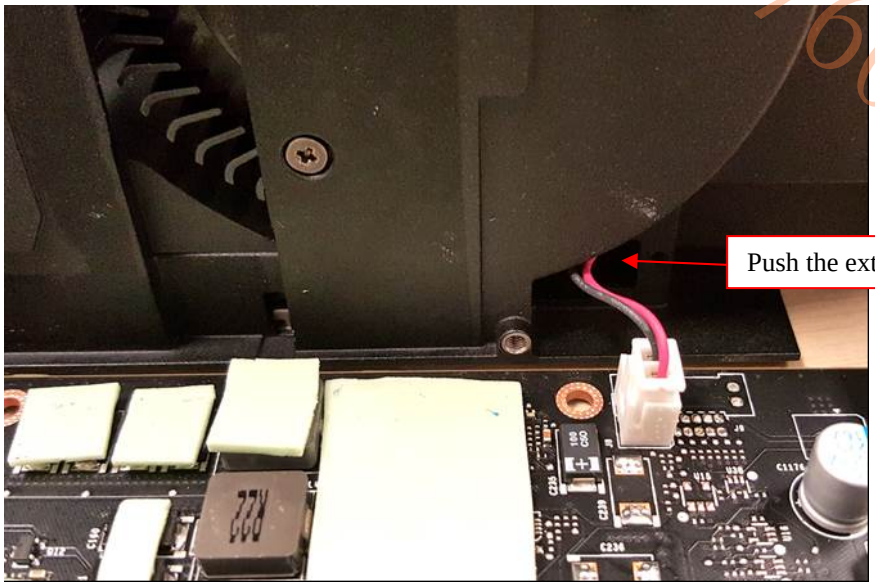
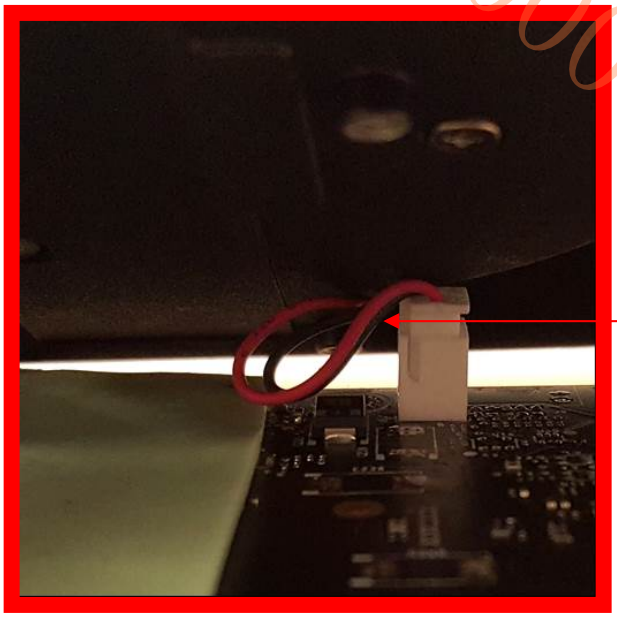


Figure 2L: Connect the LED wire to a two pins header on the main board as shown.



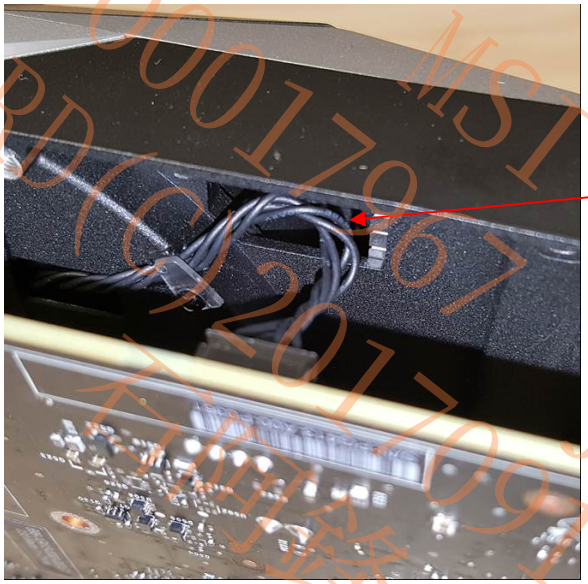
While the fansink base coming down to the main board, ensure the led wires are going inside the hole, not in between of the basepate and the main board.

Good – LED wires are going inside the hole.



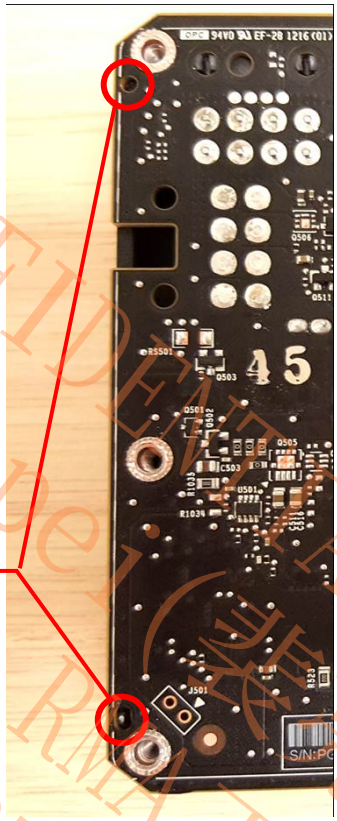
Bad – LED wires are sitting in between of the baseplate and the main board.

Figure 2m: Twist (approx. one full twist per centimeter) and insert fan power cable to the 4-pin header.

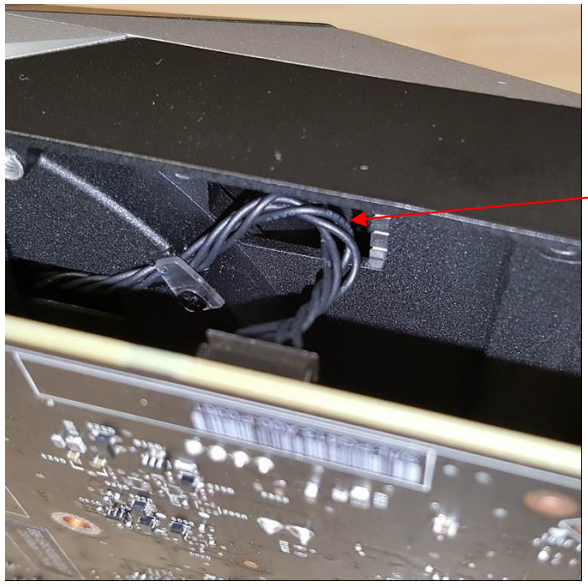


While the baseplate continuely going down on the main board, use a finger to guide the fan cable through the baseplate hole. The cable should not sit in between of the baseplate and the board.

Figure 2n: Align the baseplate on topside of the board with orientation as shown. ***Note: Do NOT hold/hit the fan at anytime during assembly. Recommend to use a supporting fixture. Handle with care is required.***



Align the two pins with the board.



While the baseplate continuely going down on the main board, use a finger to guide the fan cable through the baseplate hole. The cable should not sit in between of the baseplate and the board.

Figure 2o: Then install M2.5xL2.7mm standoffs (14X, black Zn) through PCB holes to the baseplate, torque screws to 2.2~2.6 in-Lb in sequence as shown below. **Note:** add Loctite 242 Threadlocker (3~5 threads from tip) if screw doesn't come with Nylok coating. ***Note: Do NOT hold/hit the fan at anytime during assembly. Recommend to use a supporting fixture. Handle with care is required.***

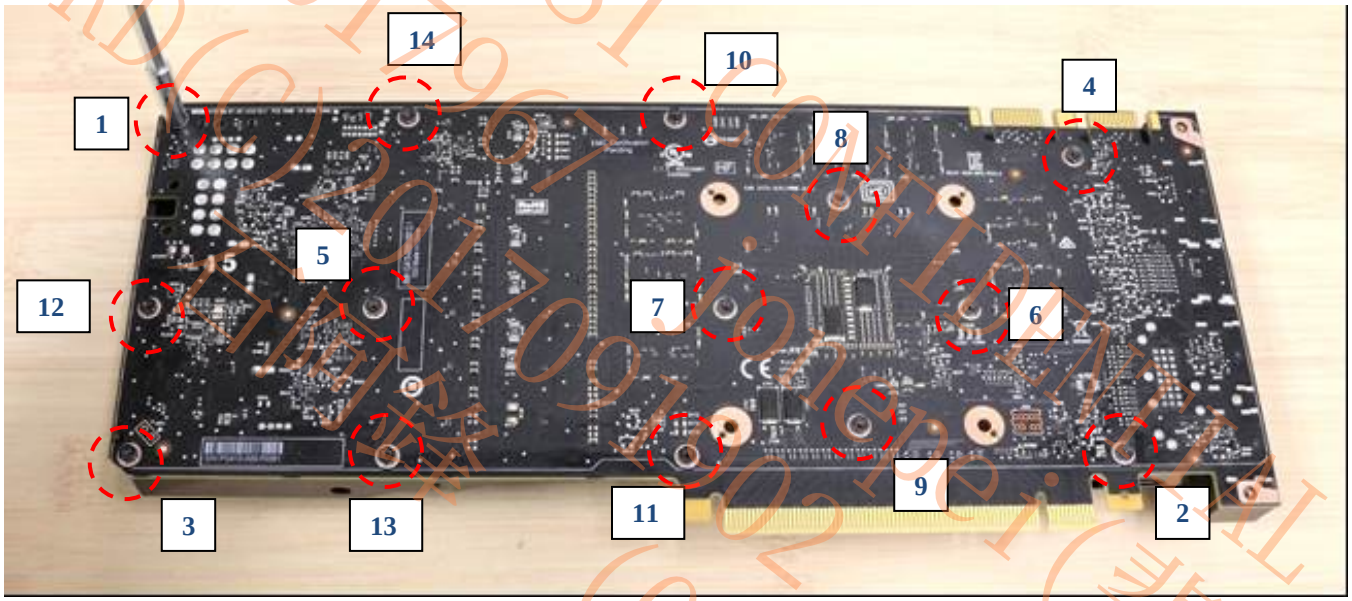


Figure 2p: Before installing heatsink modules, check and ensure sponges are pre-installed on the module as shown.

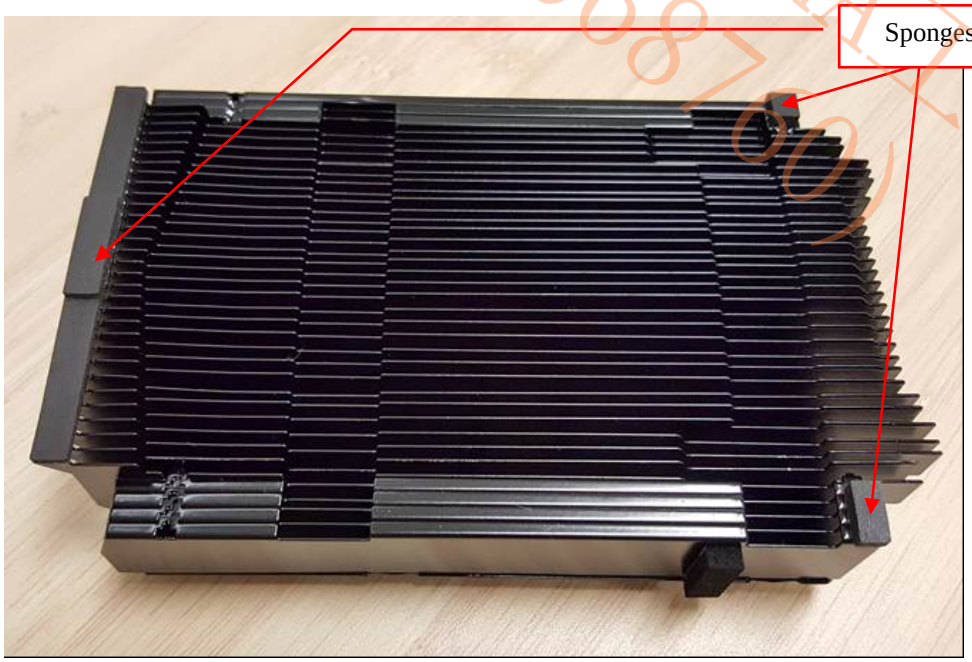
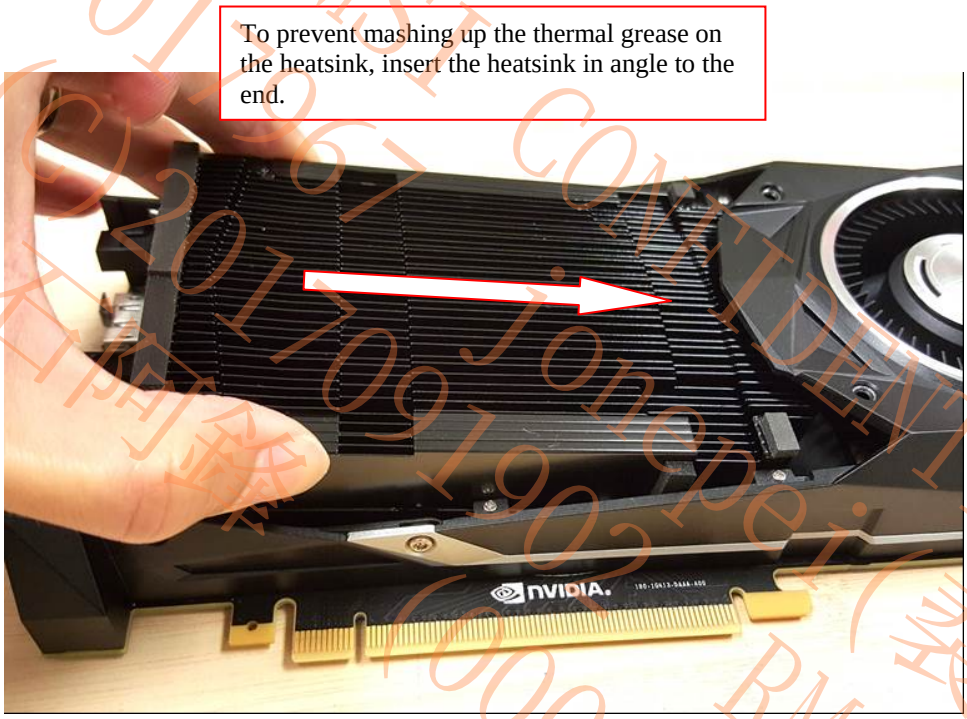


Figure 2q: Align and gently place heatsink module on top of GPU as shown. **Note:** Check and make sure heatsink module comes with pre-printed thermal grease before putting on board.



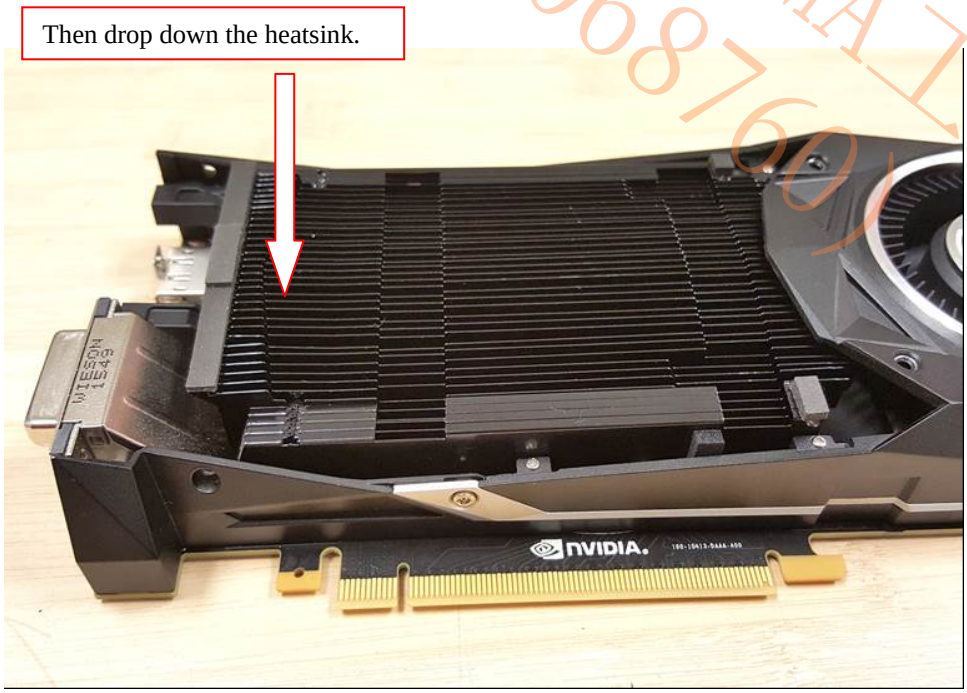


Figure 2r: Install shoulder screws w/ springs through PCB hole (bottom side) and baseplate align to GPU heatsink module as shown in 4 steps. ***Caution: to disassembly, GPU heatsink modules MUST be removed before the baseplate removal.***

Step 1 – Install all screws without tightening.
Step 2 – Continue tightening each screw in the sequence as shown to 1 in-lbf or until finger tight.
Step 3 – Fully torque all screws to 3.0~3.5 in-lbf using the same alternating sequence.
Step 4 – Make sure all screws are fully installed and shoulder screw bottoms out against GPU heat sink module stand-offs.

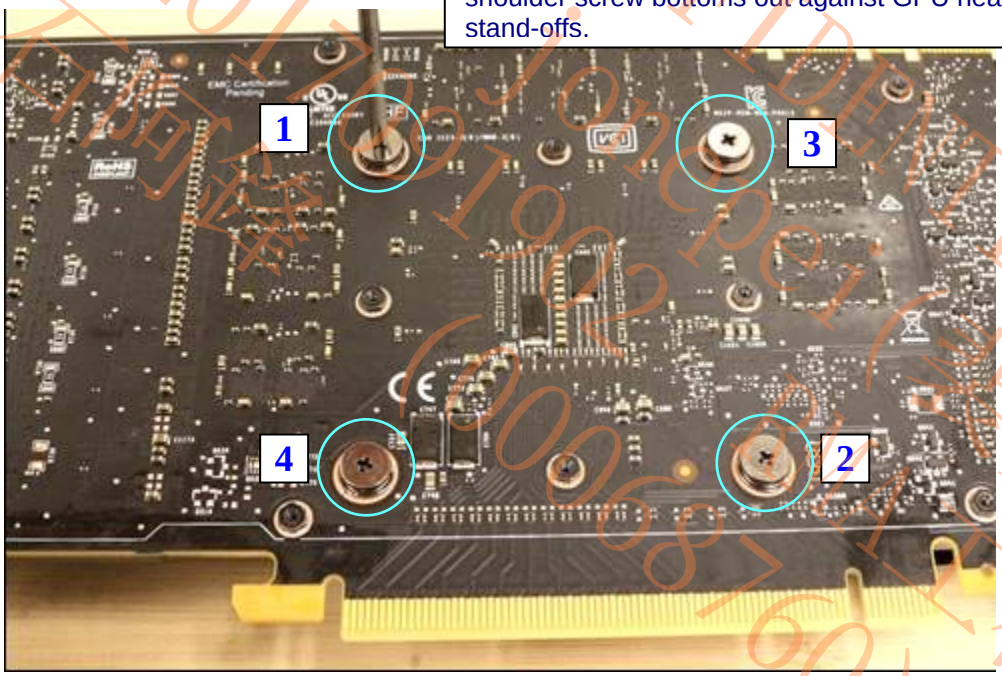


Figure 2s: Align and gently insert the TOP COVER-Left in angle to the baseplate as shown.

Figure 2t: Secure right and left cover to center cover with M2.5x4.0mm socket screws (4X, silver color). Torque screws to 3.0~3.5 in-lbf in sequence as indicated. **Note:** add Loctite 242 Threadlocker (3~5 threads from tip) if screw doesn't come with Nylok coating.

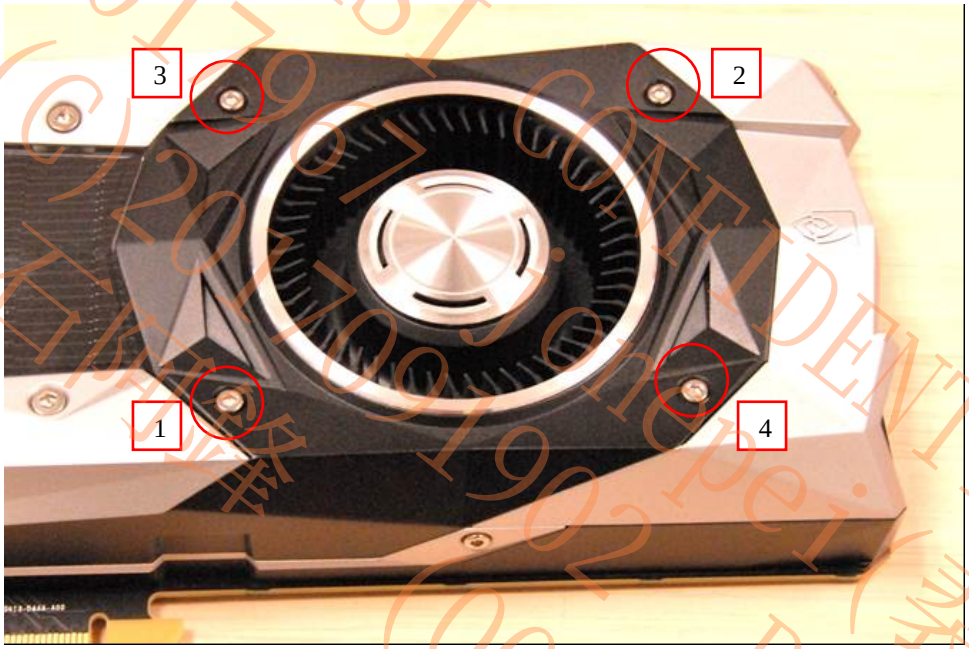
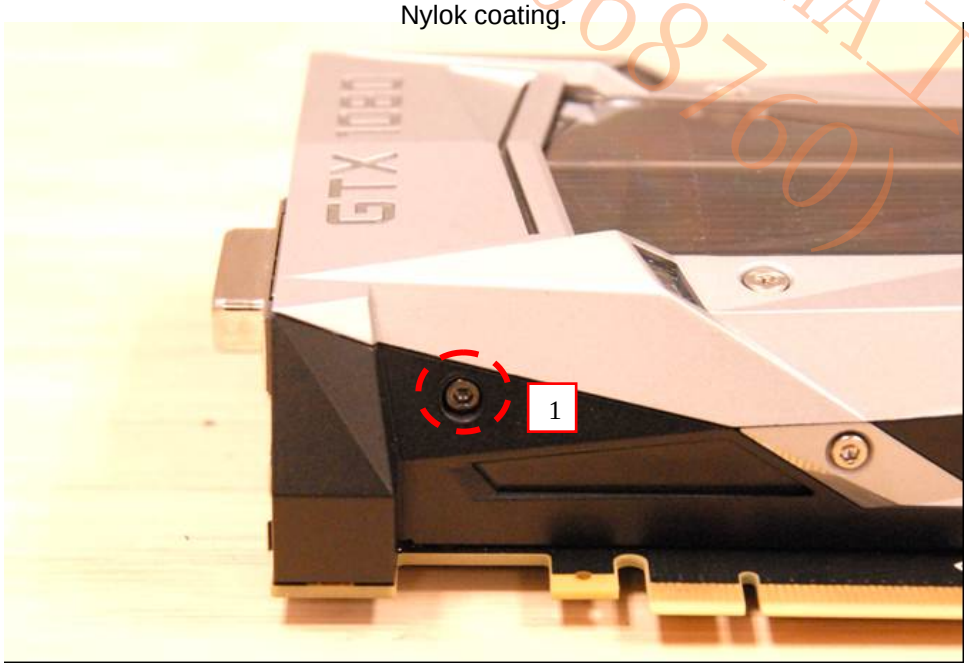


Figure 2u: Install M2.5x4mm socket screws (2x, black zinc) to baseplate. Torque screws to 3.0~3.5 in-lbf in sequence as indicated. **Note:** add Loctite 242 Threadlocker (3~5 threads from tip) if screw doesn't come with Nylok coating.



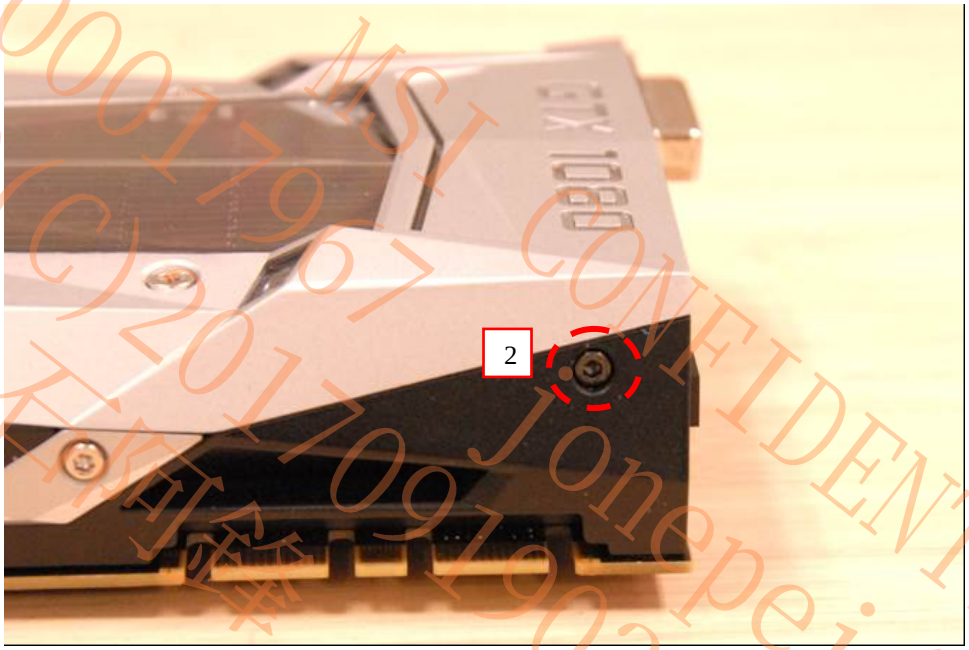


Figure 2v: Now secure the north and south trims to baseplate by torqueing the socket screws to 3.0~3.5 in-lbf.

Figure 2w: Install Thermal Interface Material (TIM) center on top of components.
Note: a) Always check against latest BOM/Cooler Spec for correct P/N, QTY, and Location.
b) Clean mating surfaces on the components with isopropyl alcohol and let them dry prior the TIMs installation.

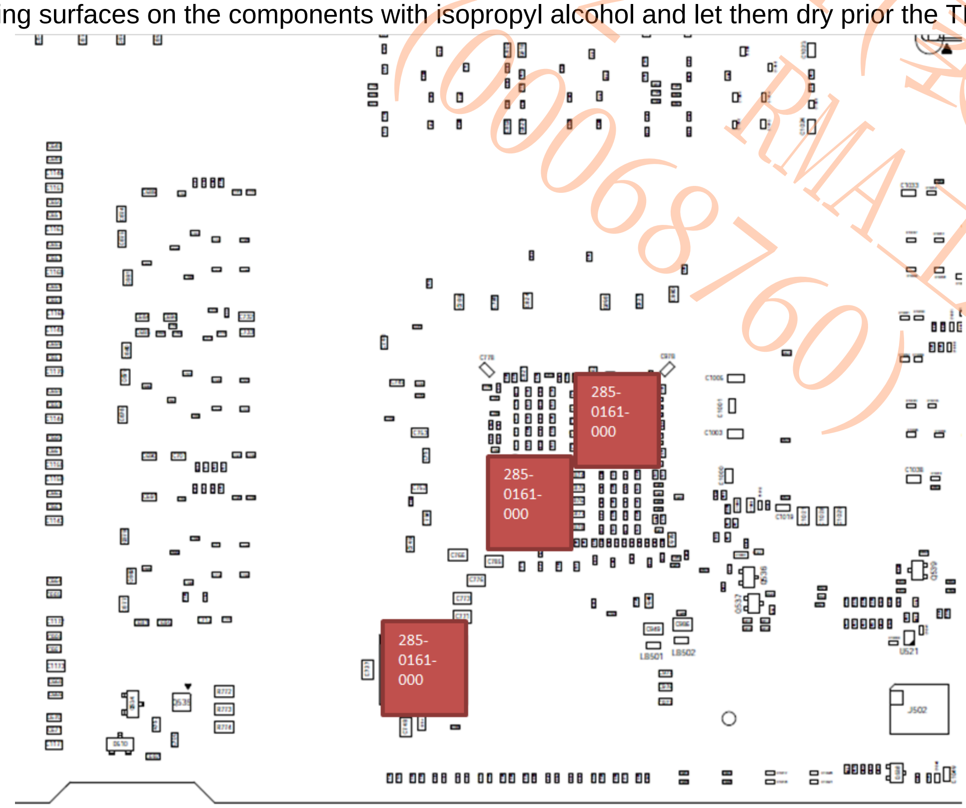


Figure 2x: Align back cover (SKU fixed) screw holes on bottom side standoffs with orientation as shown. ***Note: a) Do NOT hold/hit the fan at anytime during assembly. Recommend to use a supporting fixture. Handle with care is required.***

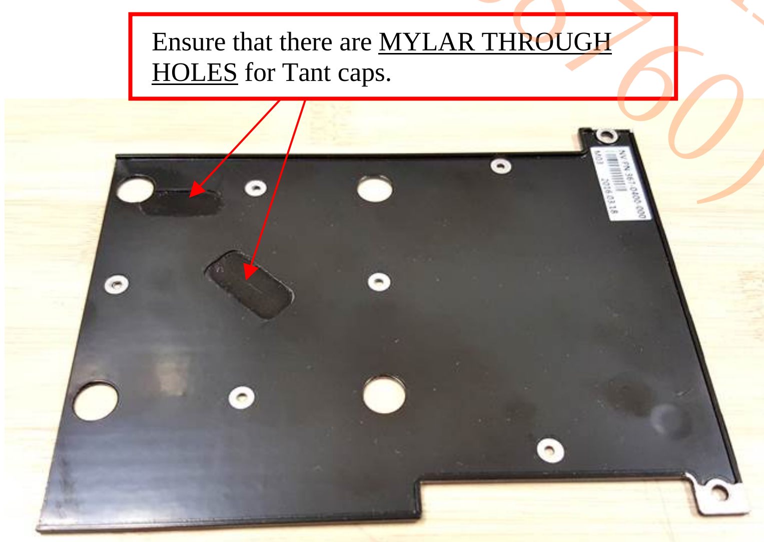


Figure 2y: Then install M1.4x3mm flat head screws (6X, black Zn) through the back cover holes to the standoffs, torque screws to 0.5 +/-0.05 in-Lb in sequence as shown below. **Note:** add Loctite 242 Threadlocker (3~5 threads from tip) if screw doesn't come with Nylok coating.

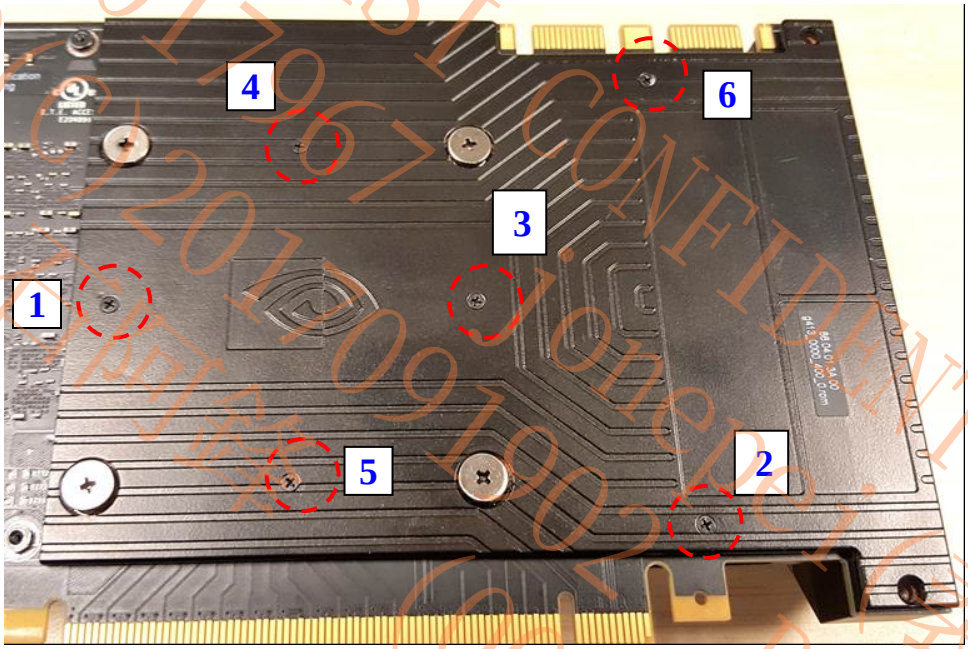


Figure 2z: Align Back cover (SKU removable) on bottom side of the standoffs with orientation as shown. ***Note: a) Do NOT hold/hit the fan at anytime during assembly. Recommend to use a supporting fixture. Handle with care is required.***

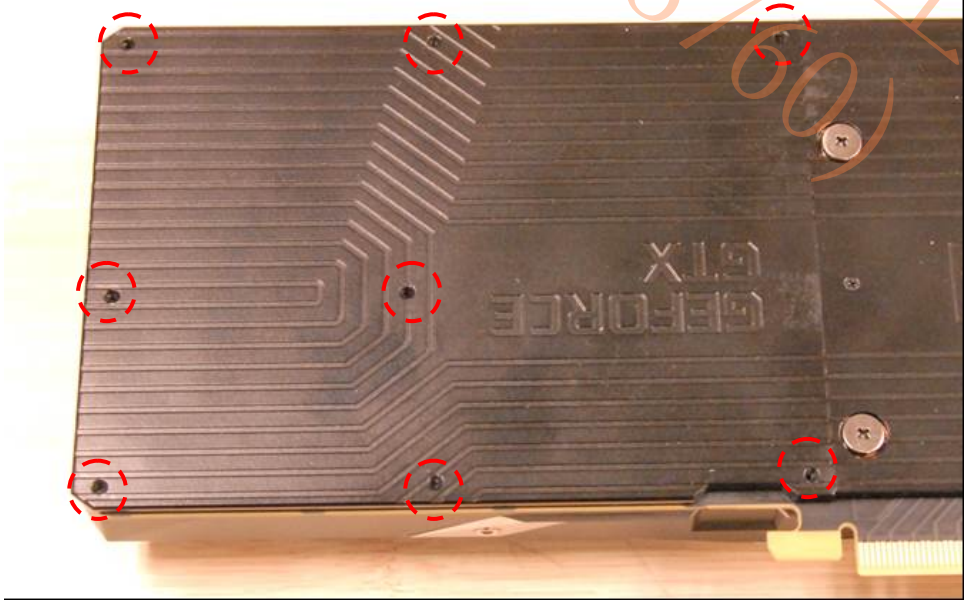


Figure 2aa: Then install M1.4x3.0mm Flat HEAD screws (8X, black Zn) through the back cover holes to the baseplate, torque screws to 0.5 +/-0.05 in-Lb in sequence as shown below. **Note:** add Loctite 242 Threadlocker (3~5 threads from tip) if screw doesn't come with Nylok coating.

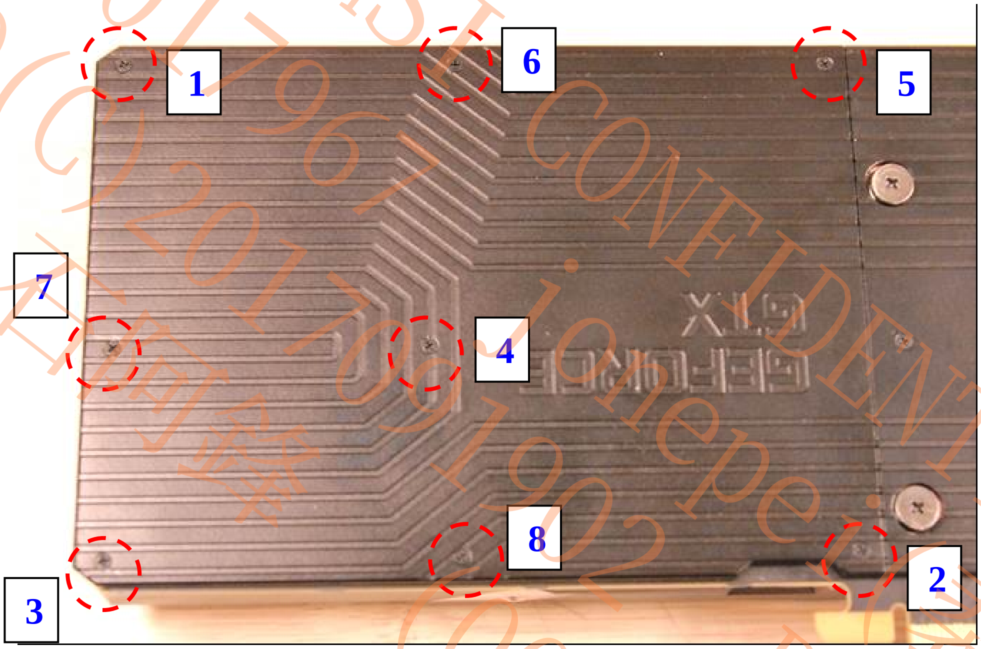


Figure 2ab: Align bracket to the board assembly. Secure bracket to the DP connectors with M2.0x4.0mm PHILLIPS FLAT HEAD screws (3x, black nickel). Torque to 1.5 ~ 1.7 in-lbf as shown in sequence below. **Caution:** Make sure the DP and HDMI connectors (the Springs/tabs) no bend/damage. **Note:** add Loctite 242 Threadlocker (3~5 threads from tip) if screw doesn't come with Nylok coating.

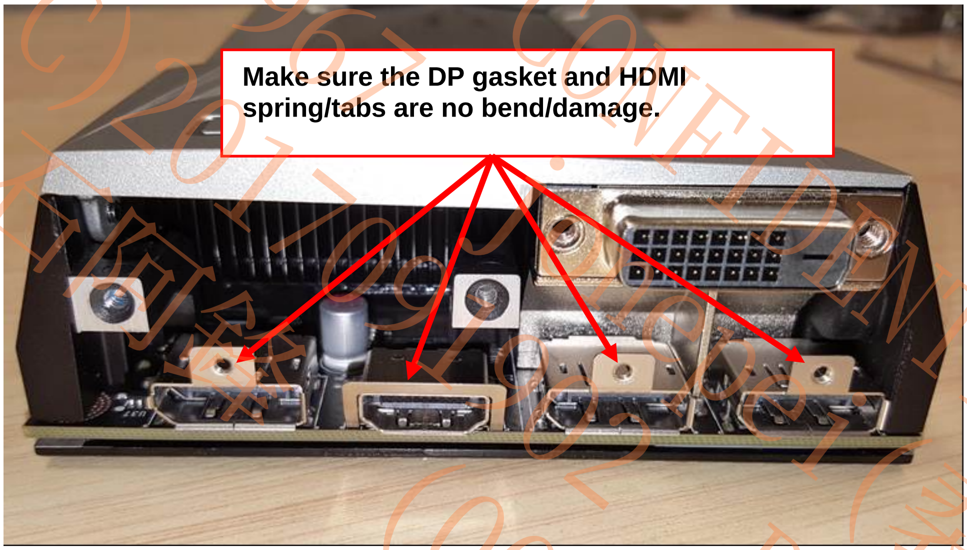


Figure 2ac: Then install M2.5x6mm Philips flat head screws (2x, black nickel). Torque to 3.0 ~ 3.5 in-lbf as shown in sequence below. **Note:** add Loctite 242 Threadlocker (3~5 threads from tip) if screw doesn't come with Nylok coating.

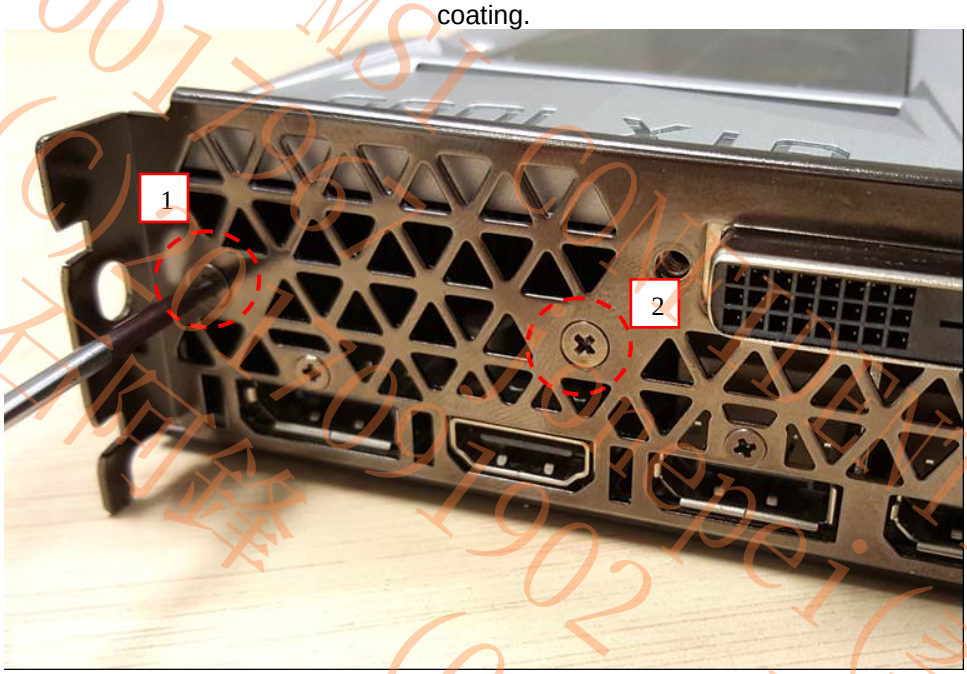


Figure 2ad: Then install Jackscrew (2X), torque all Jackscrews using a calibrated torque driver to 6.0~7.0 in-lbf in sequence as indicated.

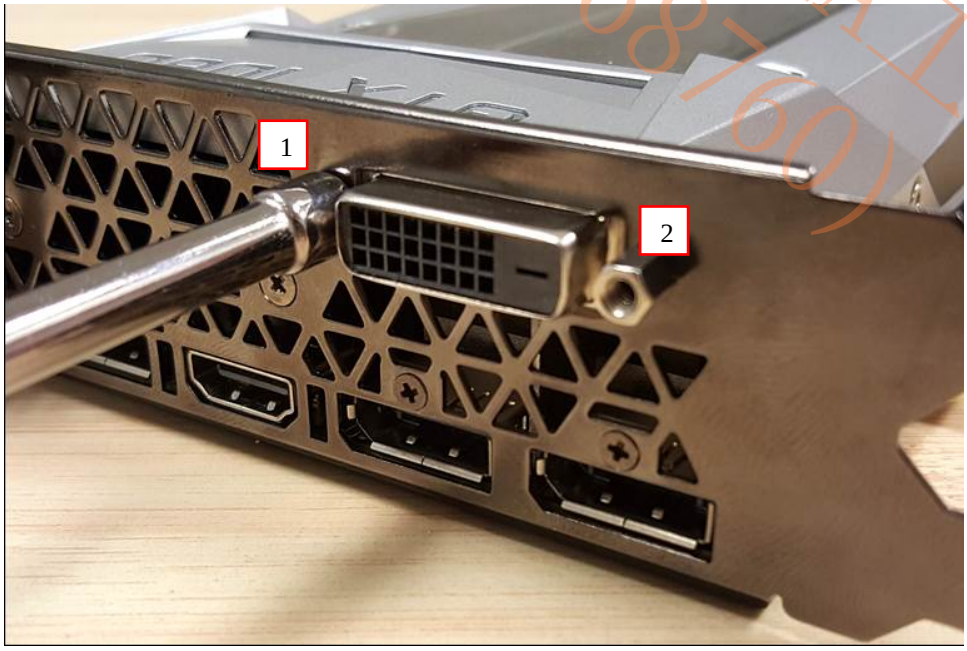


Figure 2ae: Push the bracket inward as necessary to align the hole of the bracket tab with PCB mounting hole. Then secure the tab to the PCBA and cooler with M2.5x7mm Philips flat head screws (2x, black Zn). Torque to 4.0 ~ 4.5in-lbf. Note: add Loctite 242 Threadlocker (3~5 threads from tip) if screw doesn't come with Nylok coating.

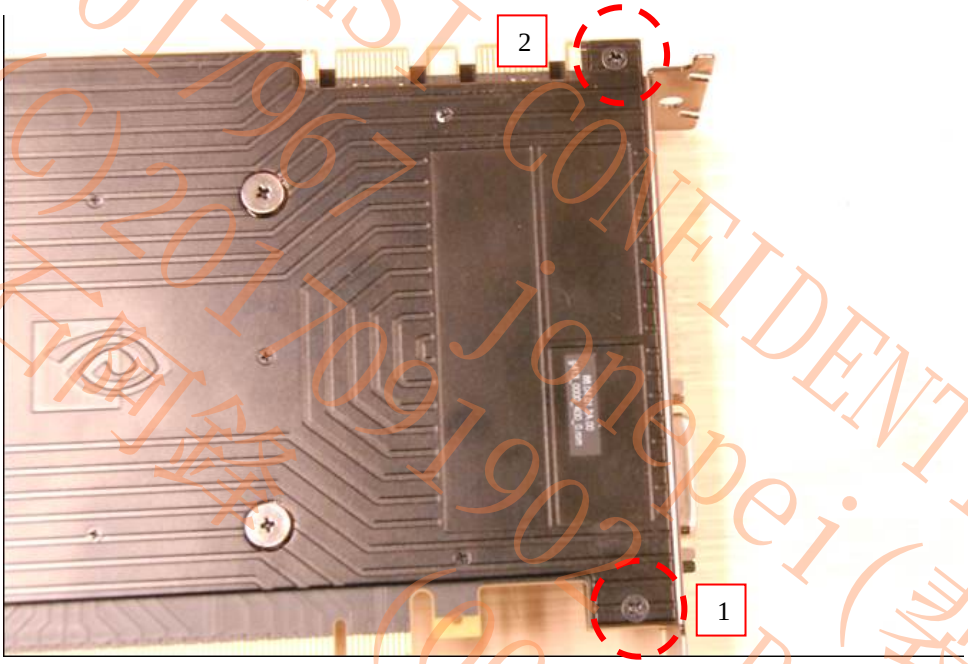
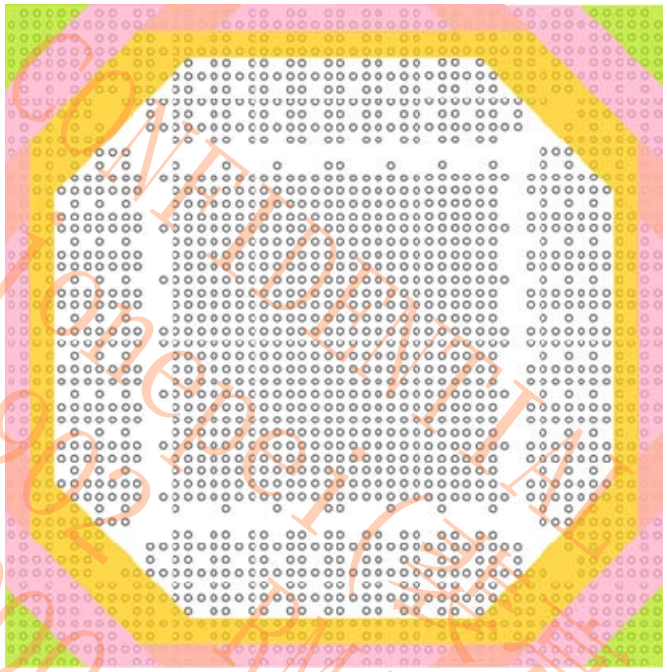


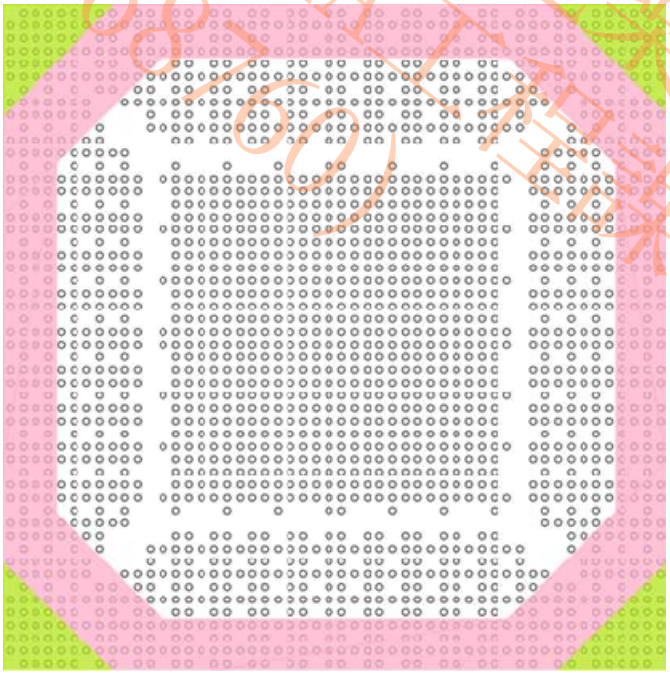
Figure 3: Process highlights.

- Stencil apertures opening recommendation for GP104 (37.5 mm x 37.5mm, no stiffener and heat spreader)

Option A: (4 zone) more compatible with other u-pitch components.
Thickness: 0.10mm
White = 0.30 mm Sq.
Orange = 0.35 mm Sq.
Pink = 0.40 mm Sq.
Green = 0.45 mm Sq.

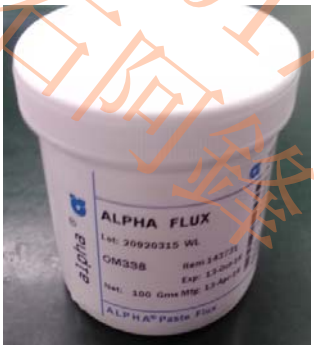


Option B: (3 zone) OK if other components are not u-pitch
Thickness: 0.12mm
White = 0.35 mm Sq.
Pink = 0.40 mm Sq.
Green = 0.45 mm Sq.

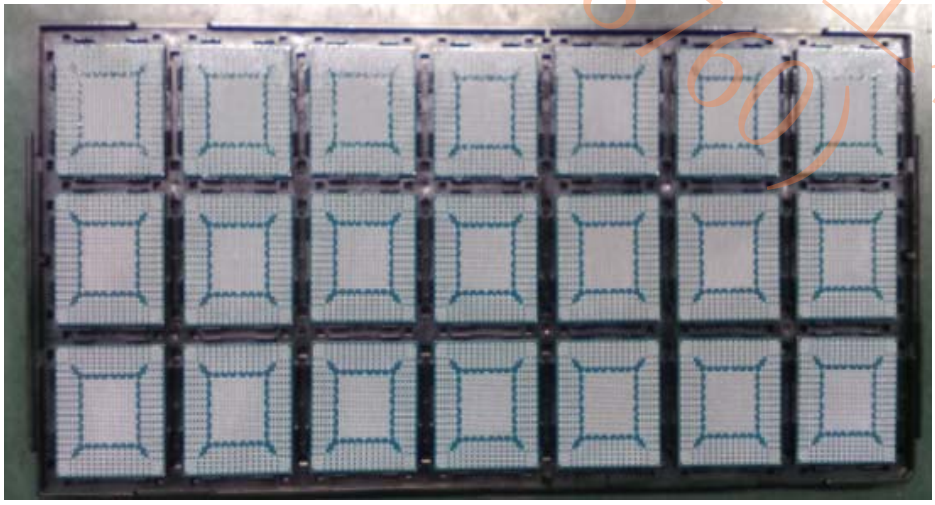


- Apply flux gel to GPU balls before SMT placement as necessary
  - Tooling – Nylon brush w/ width 18~20mm

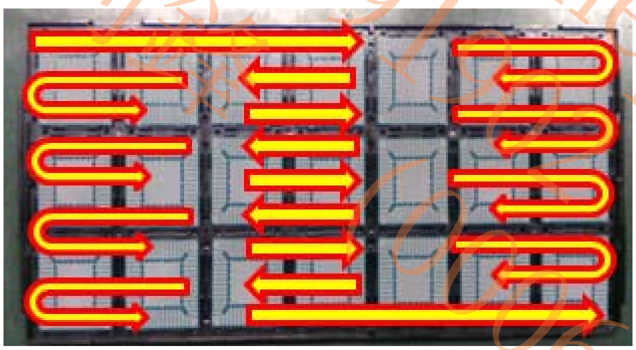
  - Material – Flux gel/paste (ALPHA FLUX OM338 or equivalent)

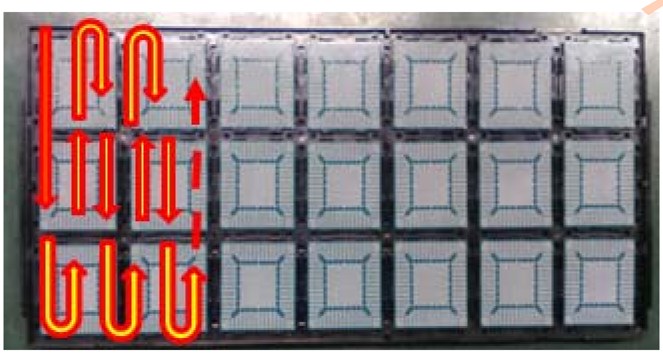


  - Procedures
    - Turn the whole tray of GPU chips with solder ball side upward

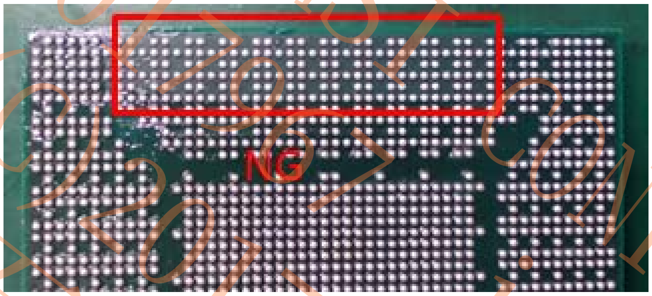


- Use the bush to apply flux gel on GPU balls evenly in the track flow as shown. Note: repeat 3 or 4 times for each track traveling.

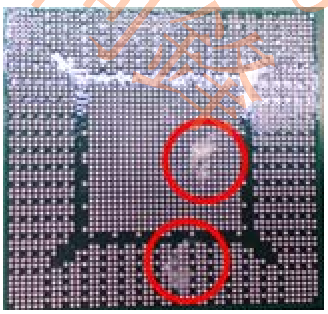




- Inspect and ensure no missing flux gel or accumulation issue found.
  - Missing Flux



  - Accumulation of Flux



- Turn the whole tray of GPU chips over with top (die) side upward. Check and ensure no flux contamination. Clean with non-dust cloth if any found.

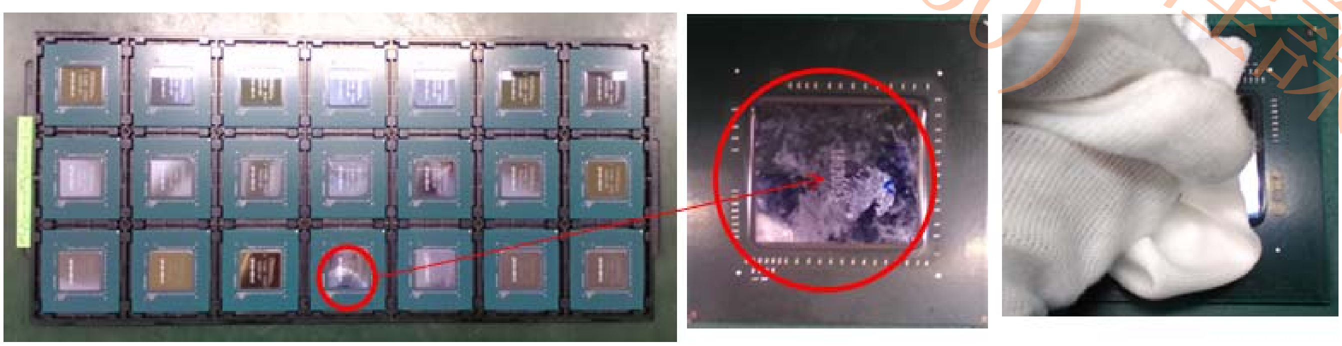


Figure 4: ESD Bag and ESD Label Orientation

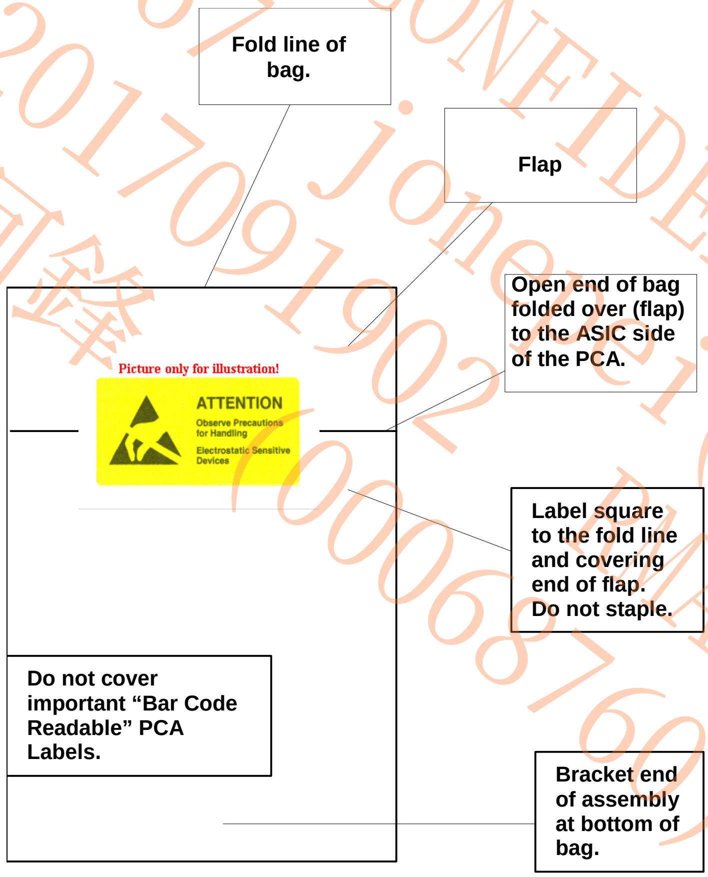


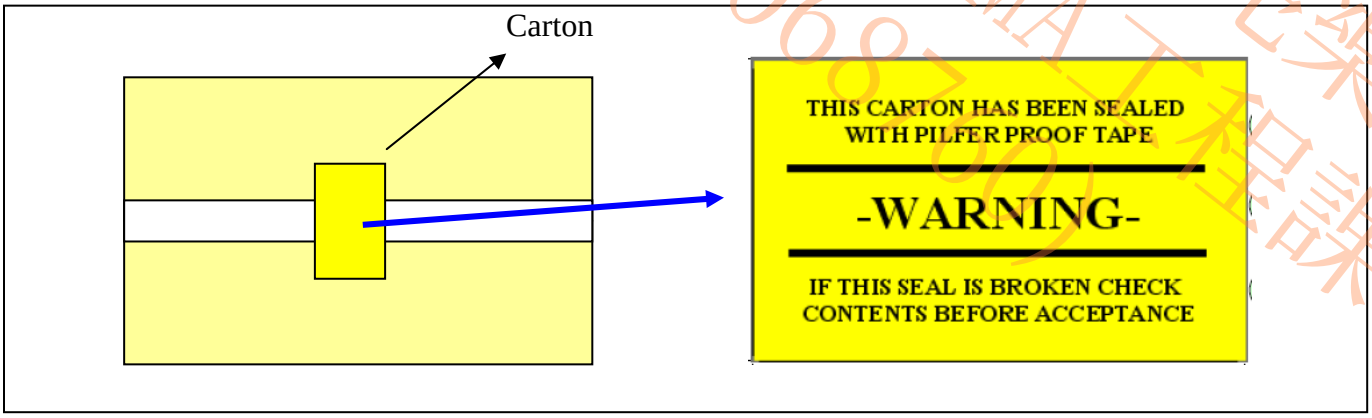
Figure 5: Tamper Evident Tape Specifications.

1) Water activated tape or Mylar is acceptable
2) Marking (below to be repeated every 6 inches)

THIS CARTON HAS BEEN SEALED
WITH PILFER PROOF TAPE
-WARNING-
IF THIS SEAL IS BROKEN CHECK
CONTENTS BEFORE ACCEPTANCE

.

OR Tamper Evident Over-label



The Tamper Evident Over-Label needs to stick on top of the Tamper Evident Tape and sticks it perpendicularly.

REVISION HISTORY

REV. LEVEL	EFFECTIVE DATE	ECO No.	DESCRIPTION OF CHANGE	ORIGINATOR
A	4/21/16	ECO220763	Initial Release	A. Koo
B	5/11/16	ECO221940	• Revise the screw installation sequence for top right cover • Revise the torque value setting for back covers • Add brush flux paste procedures • P-Release	E. Wong