

PG611 A00

10GB GDDR5X, 320b, 256Mx32
DP + DP + HDMI/DP + DP

TABLE OF CONTENTS

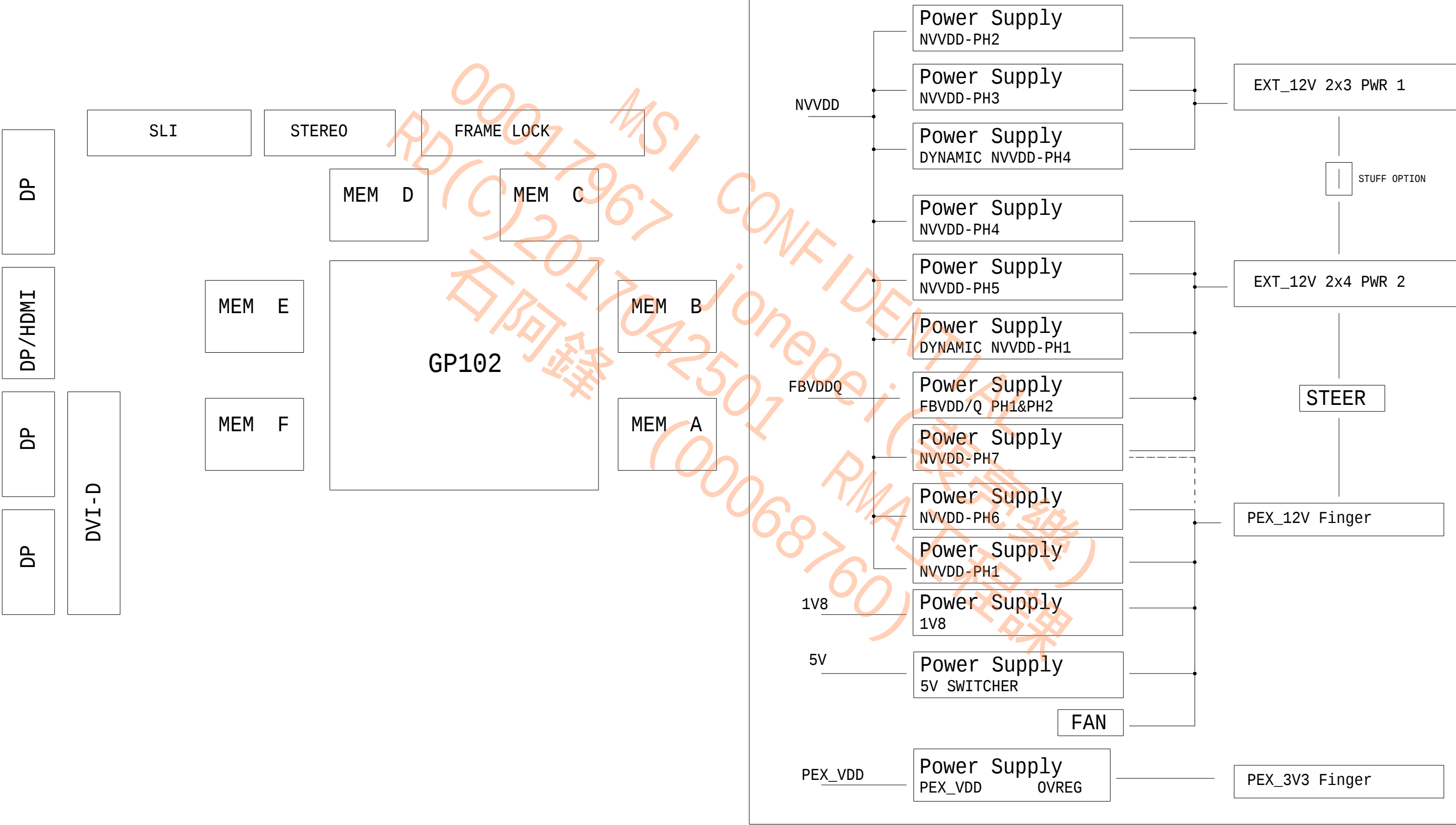
Page Description

1	Table of Contents
2	BLOCK DIAGRAM
3	PCI EXPRESS
4	MEMORY: GPU PARTITION A/B
5	MEMORY: FBA PARTITION[31:0]
6	MEMORY: FBA PARTITION[63:32]
7	MEMORY: FBB PARTITION[31:0]
8	MEMORY: FBB PARTITION[63:31]
9	MEMORY: GPU PARTITION C/D
10	MEMORY: FBC PARTITION[31:0]
11	MEMORY: FBC PARTITION[63:32]
12	MEMORY: FBD PARTITION[31:0]
13	MEMORY: FBD PARTITION[63:32]
14	MEMORY: GPU PARTITION E/F
15	MEMORY: FBE PARTITION[31:0]
16	MEMORY: FBE PARTITION[63:32]
17	MEMORY: FBF PARTITION[31:0]
18	MEMORY: FBF PARTITION[63:32]
19	GPU PWR AND GND
20	GPU DECOUPLING
21	IFPAB DVI-D-DL
22	IFPE DP
23	IFPF DP
24	IFPC HDMI/DP
25	IFPD DP

Page Description

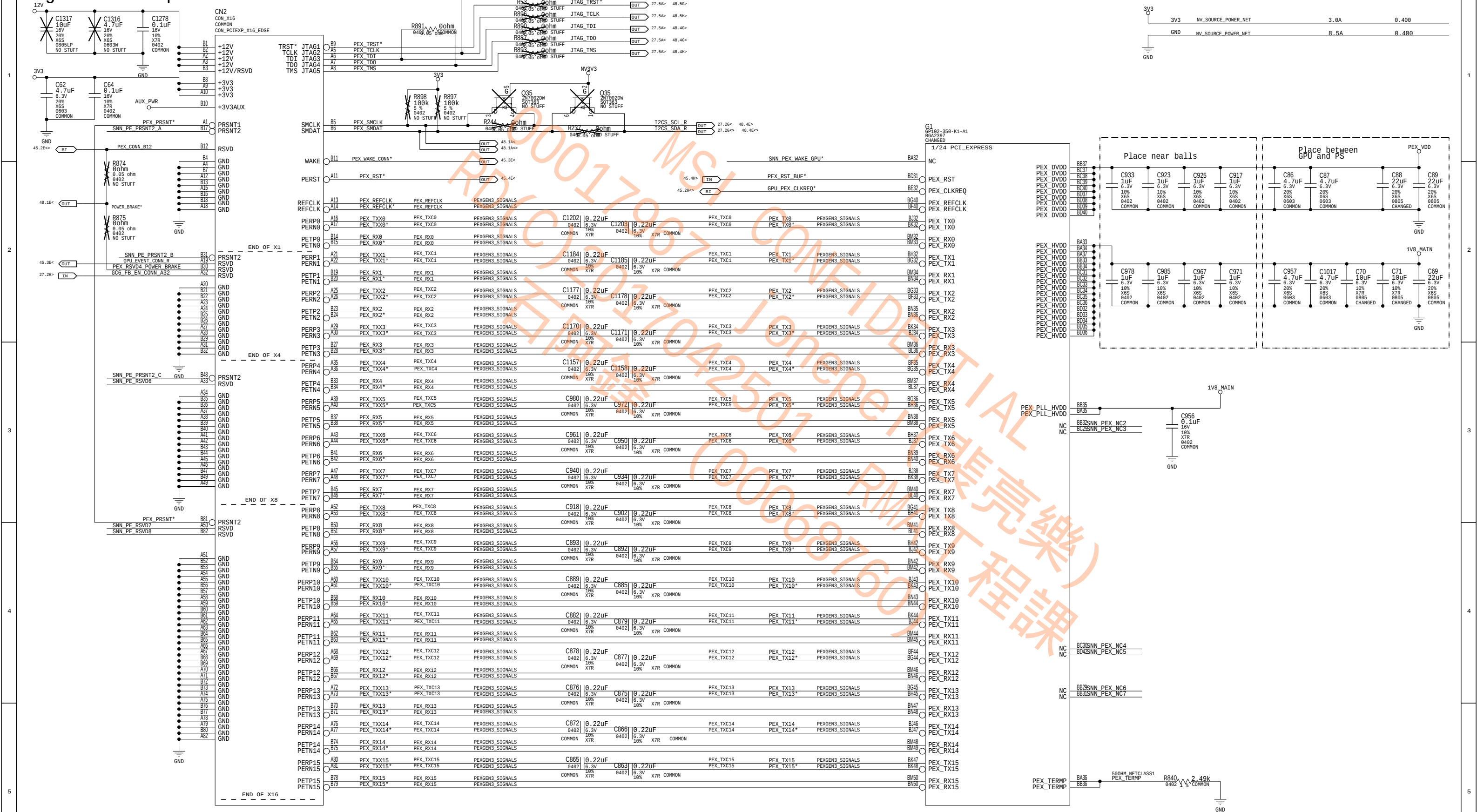
26	MIOA/B INTERFACE & FRAME LOCK
27	MISC: FAN, THERMAL, JTAG, GPIO, STEREO
28	MISC: ROM, STRAPS
29	MISC: XTAL, PLL
30	PS: 5V, PEXVDD
31	PS: 1V8 Rails
32	PS: FBVDDQ
33	PS: NVVDD Controller_OVR8
34	PS: NVVDD Controller_PWR-MODULE
35	PS: NVVDD Phase 1, 2
36	PS: NVVDD Phase 3, 4
37	PS: NVVDD Phase 5
38	PS: NVVDD Phase 6, 7
39	PS: Dynamic power balance phase
40	PS: Dynamic power balance logic
41	PS: Input, filtering, and Monitoring
42	PS: Current Sterring, Hot Unplug
43	PS: NVVDD ENABLE
44	PS: GC6 MISC
45	GEFORCE LED AND SLI LED
46	PS: NV3V3, NV12V
47	PS: MCU
48	MECH
49	VR Thermal Protection

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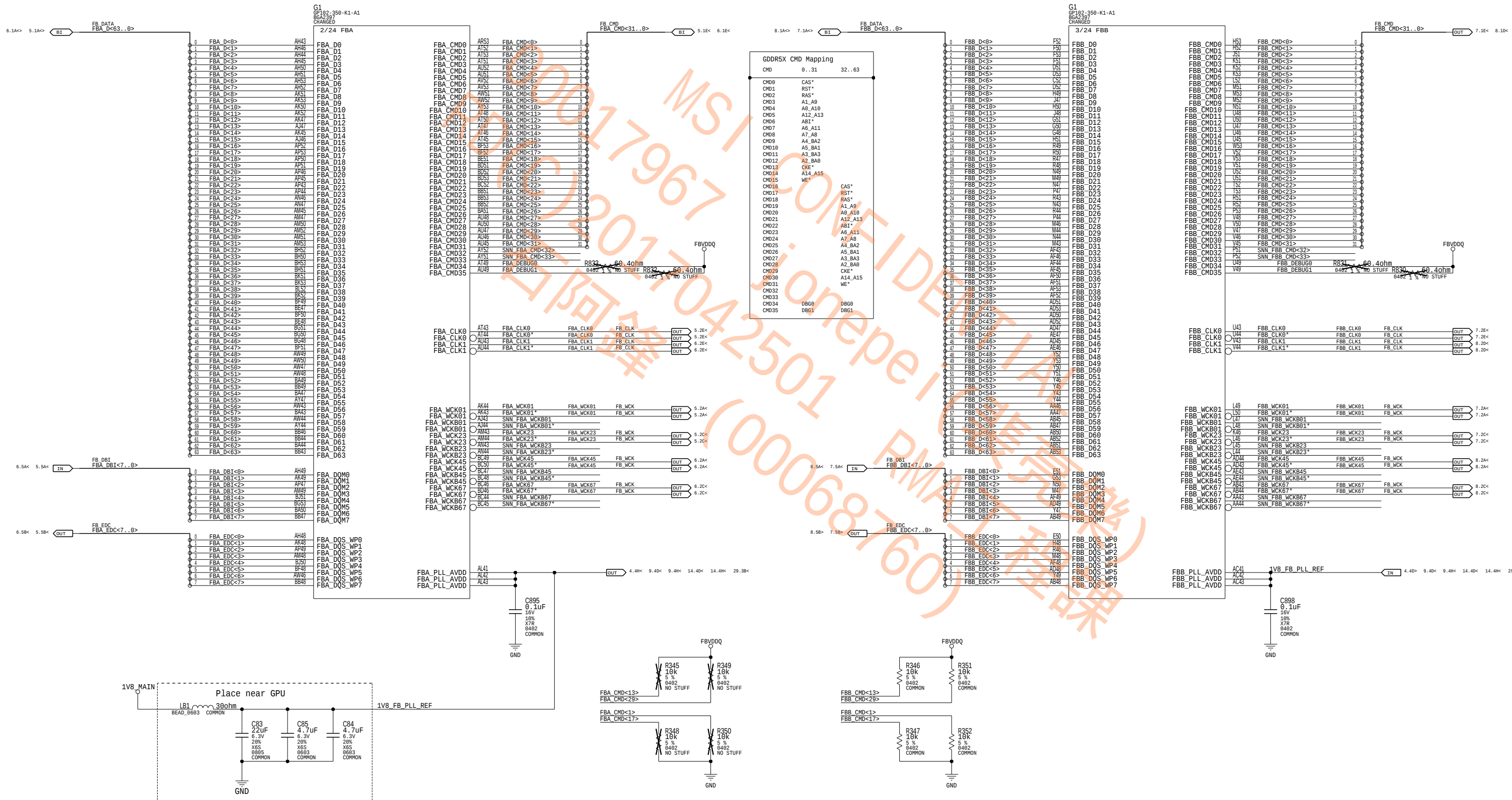
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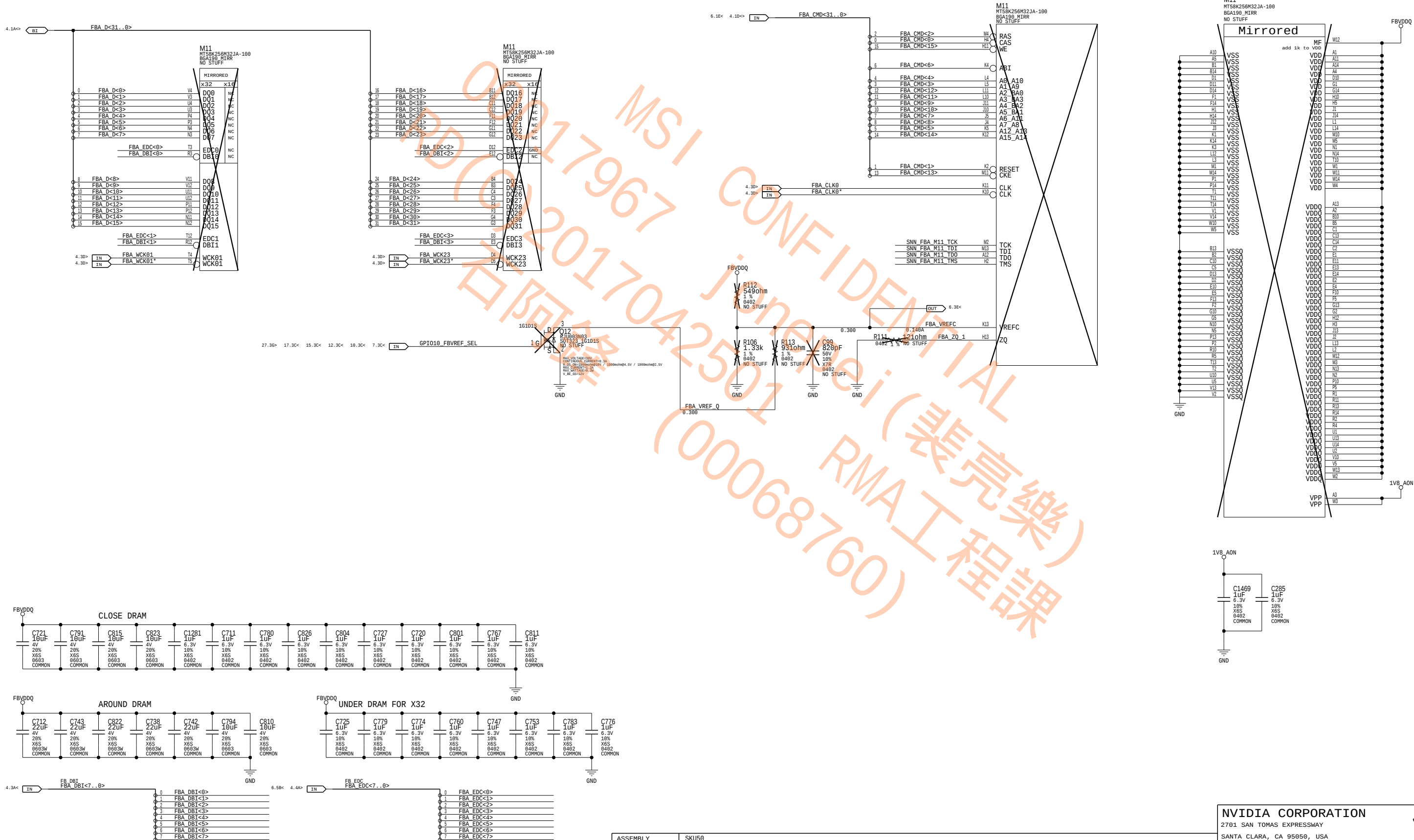
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ASSEMBLY	SKU50
PAGE DETAIL	PCI EXPRESS

Page4: MEMORY: GPU Partition A/B



Page5: MEMORY: FBA Partition 31..0



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ASSEMBLY	SKU50
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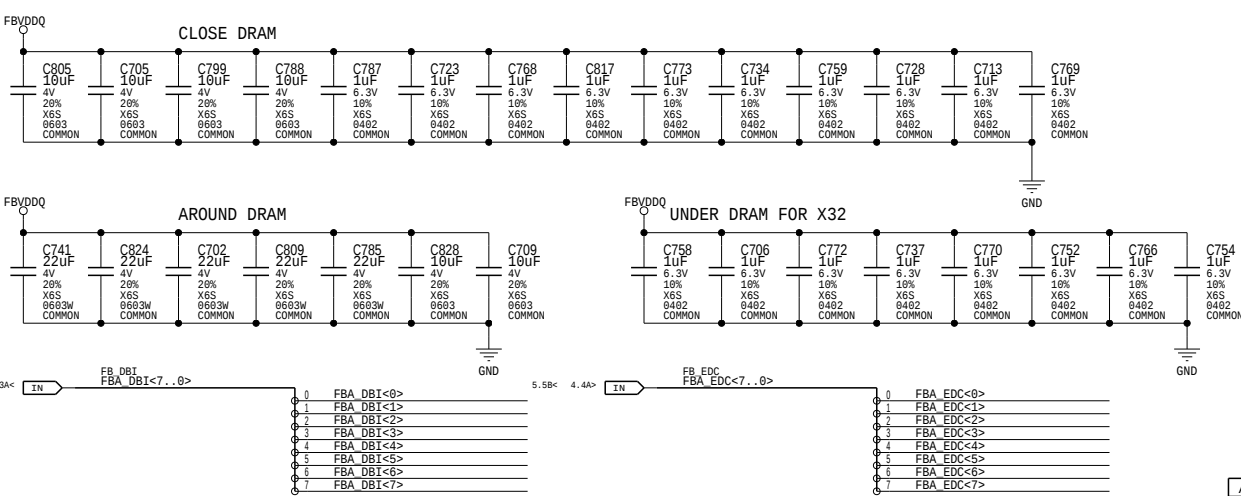
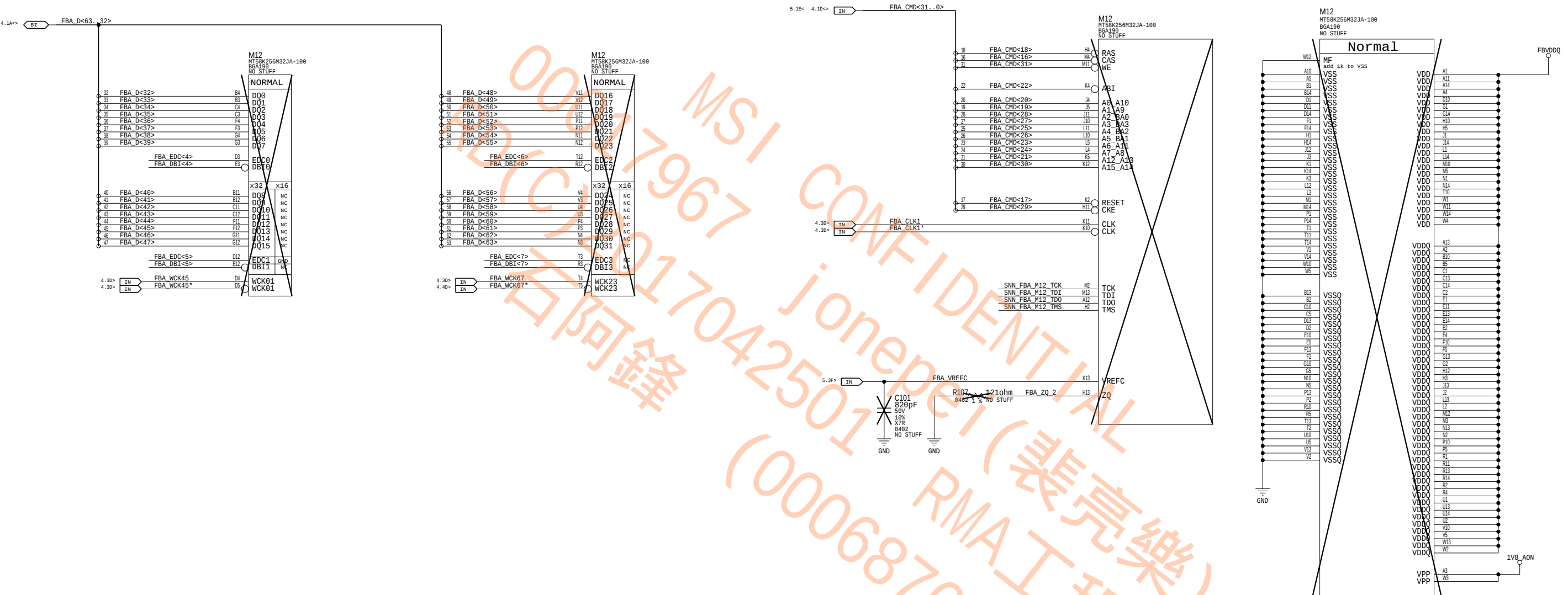
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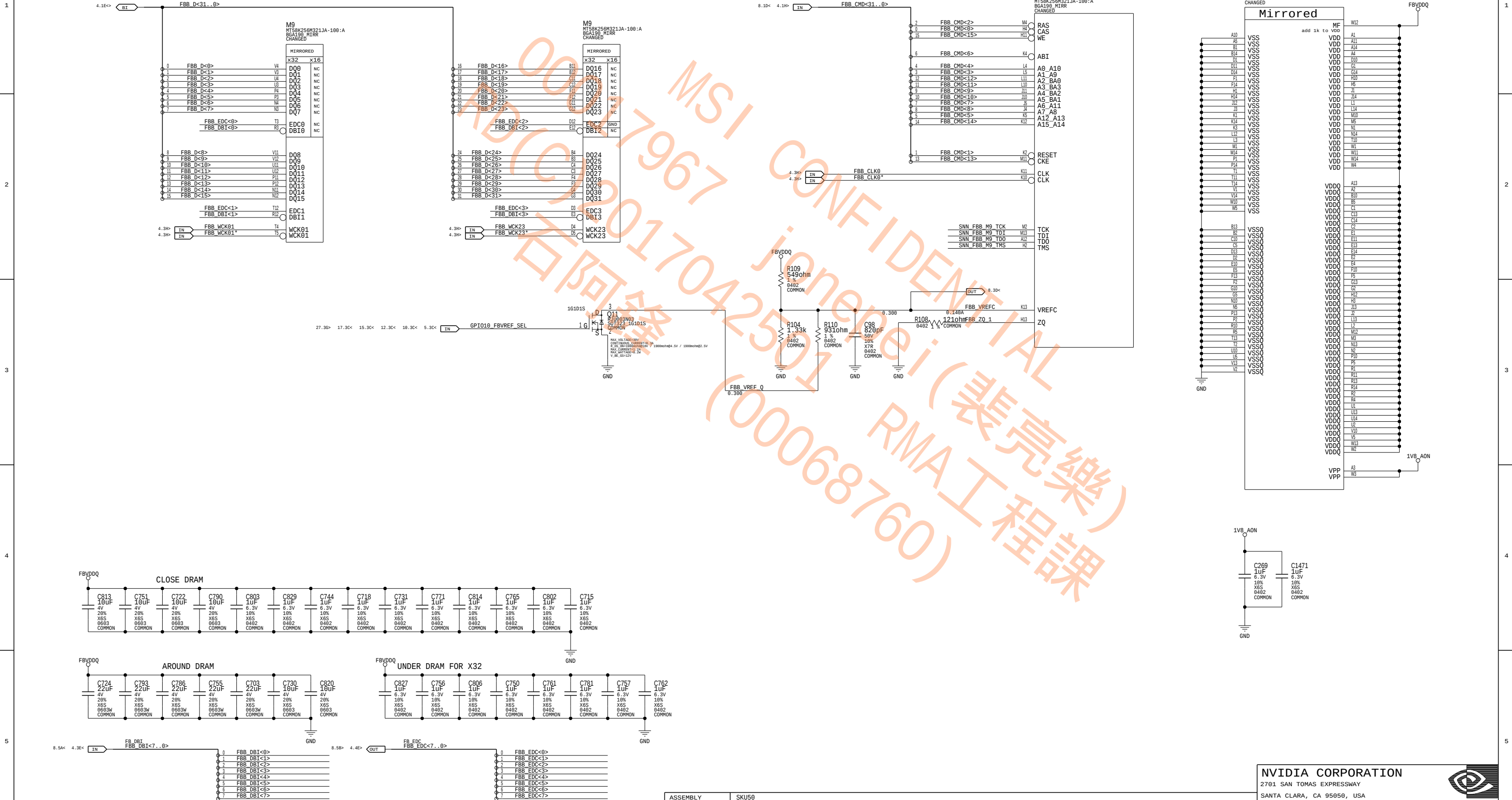


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PCB REV	PG611-A00	PAGE	5 OF 49
BOM REV	A	DATE	15-FEB-2017

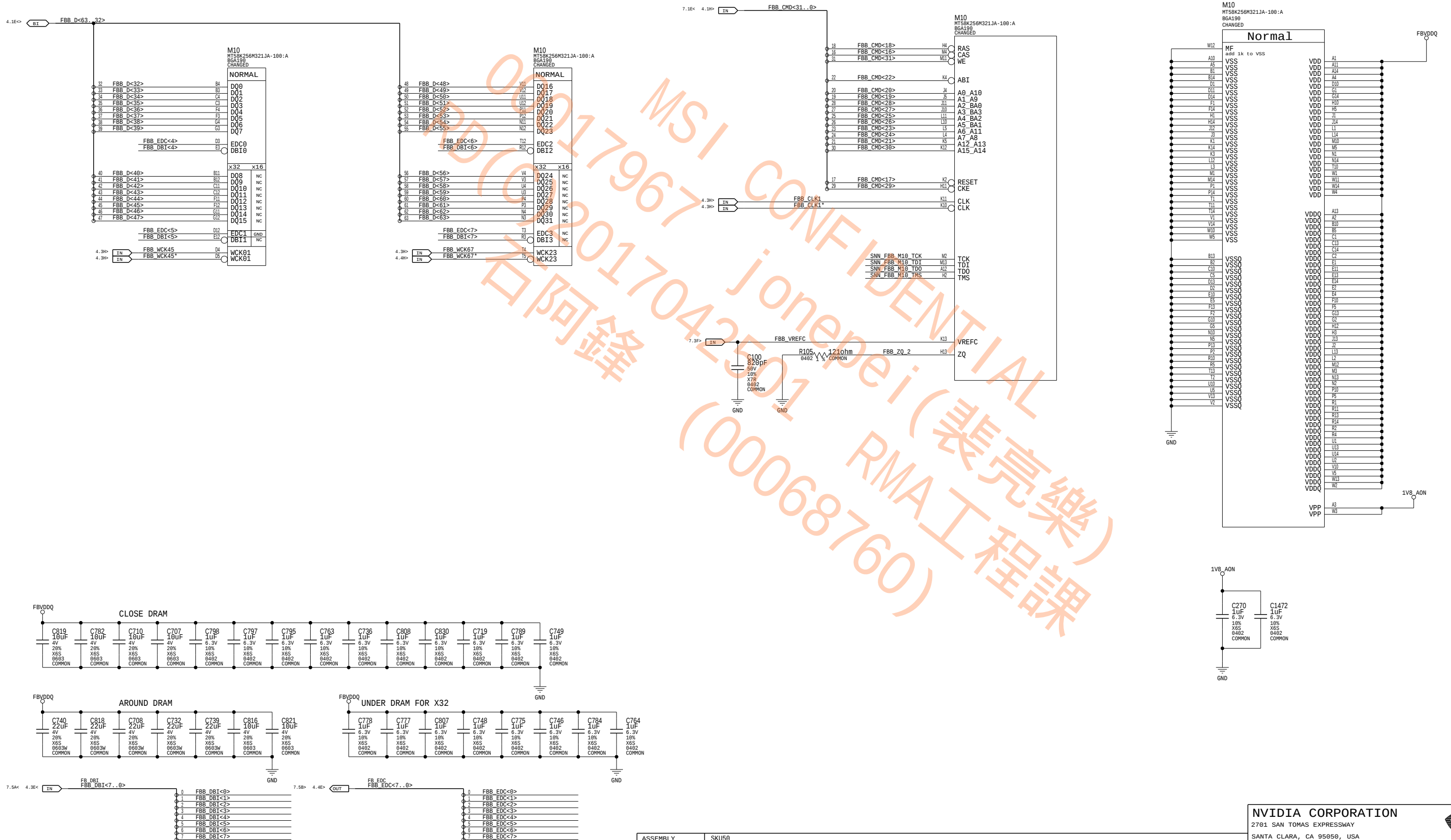


Page7: MEMORY: FBB Partition 31..0

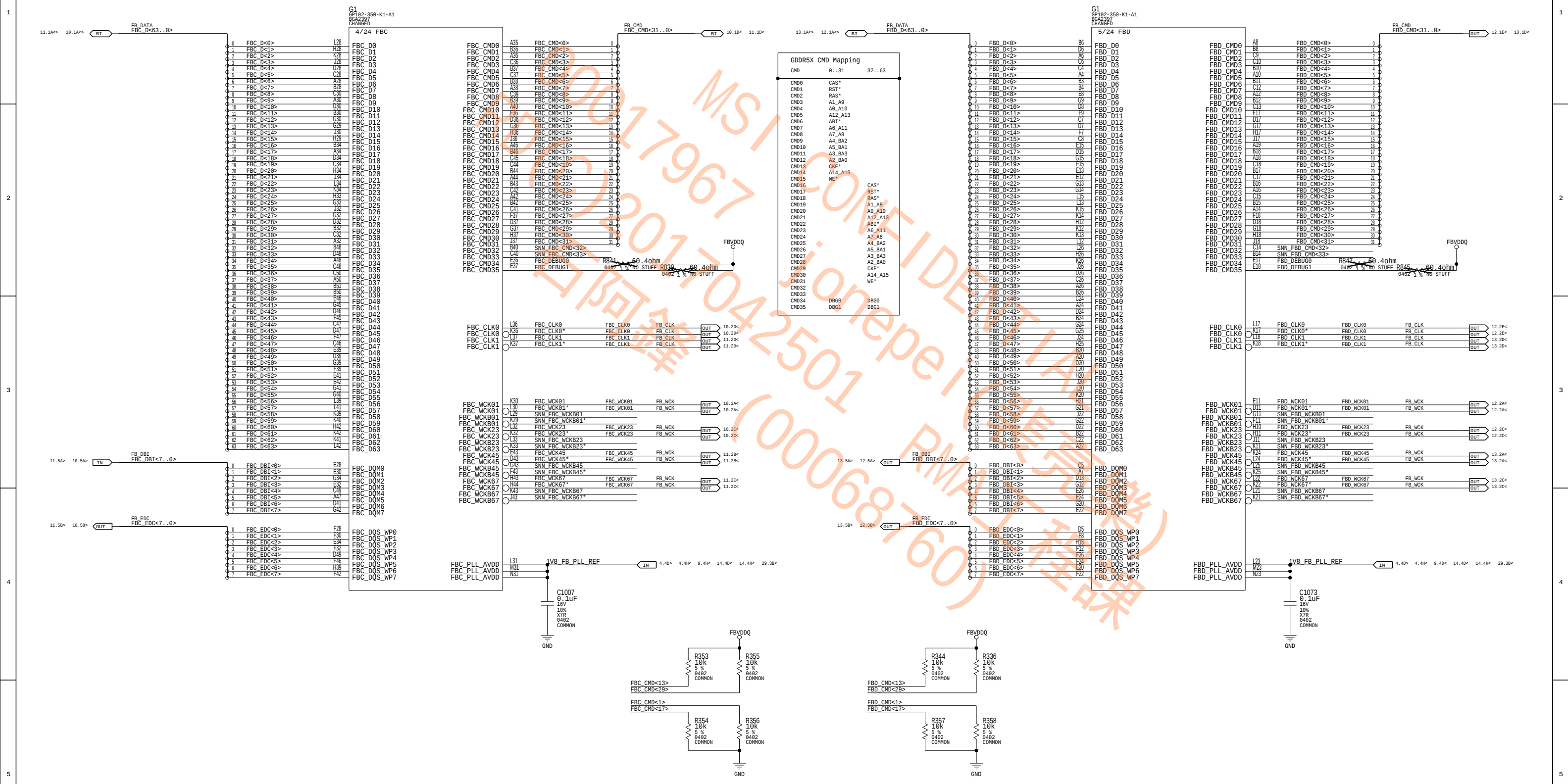


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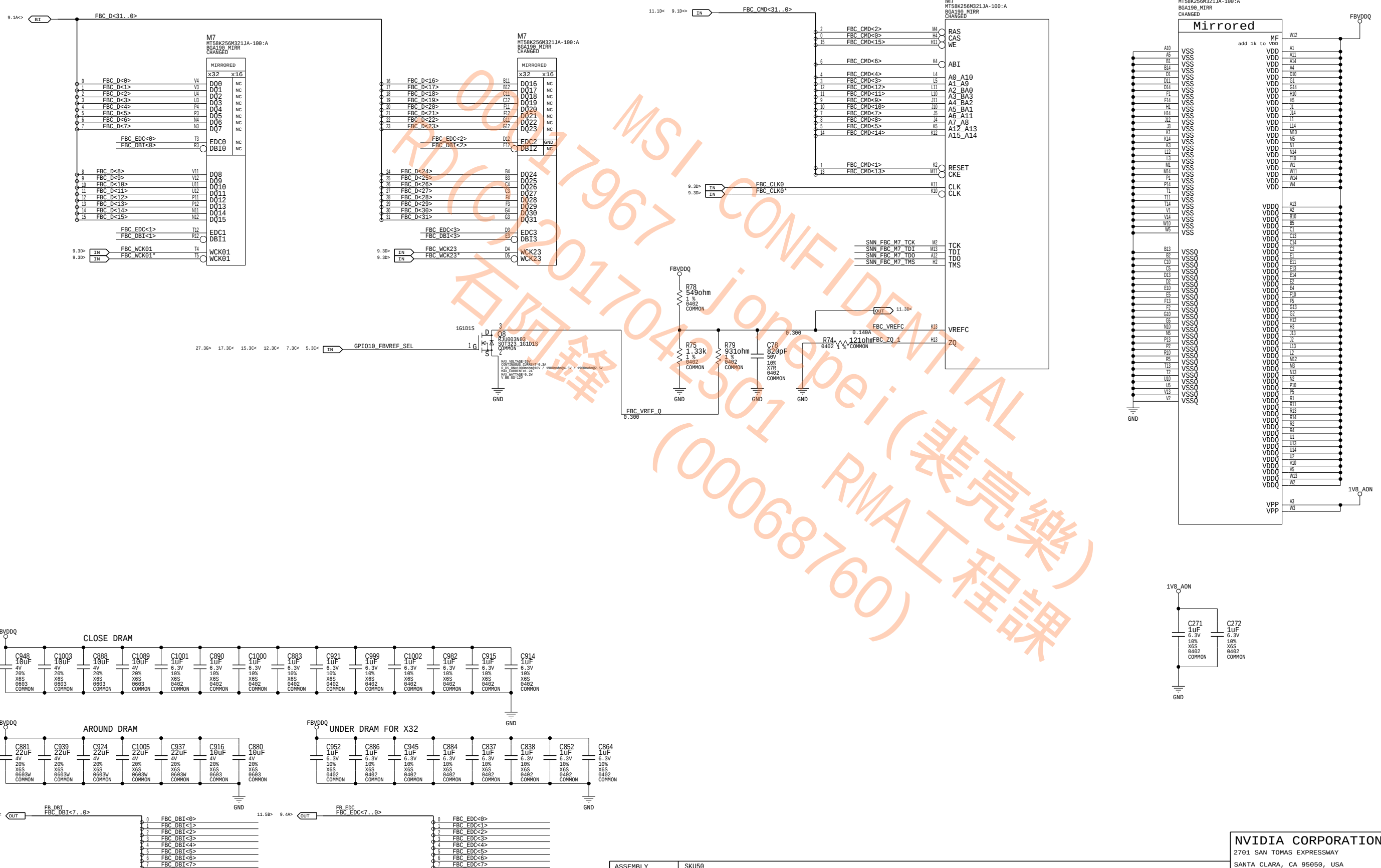
Page8: MEMORY: FBB Partition 63..32



Page9: MEMORY: GPU Partition C/D



Page10: MEMORY: FBC Partition 31..0



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ASSEMBLY	SKU50
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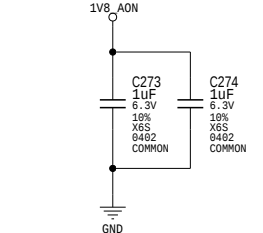
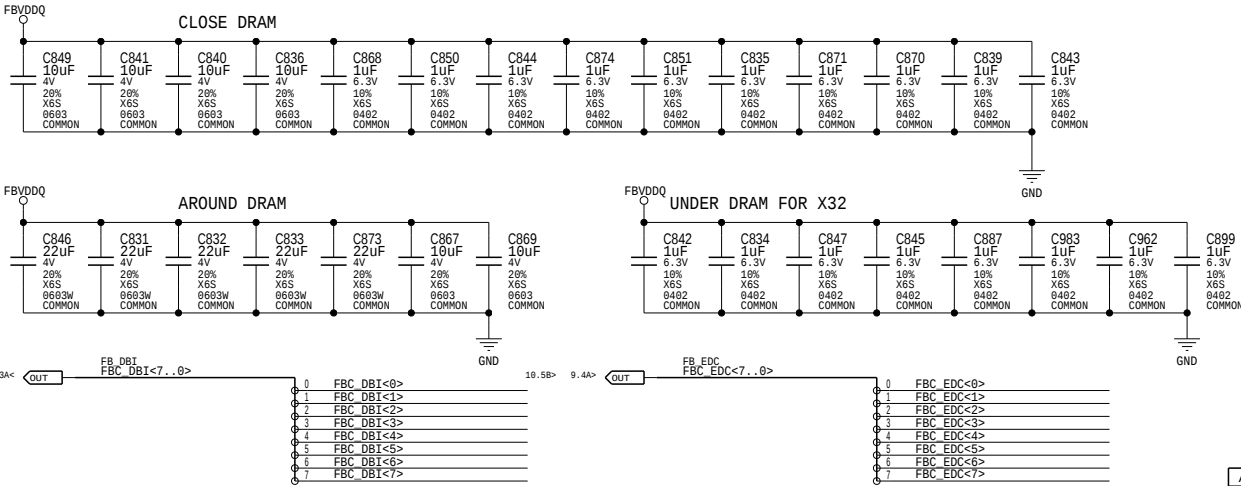
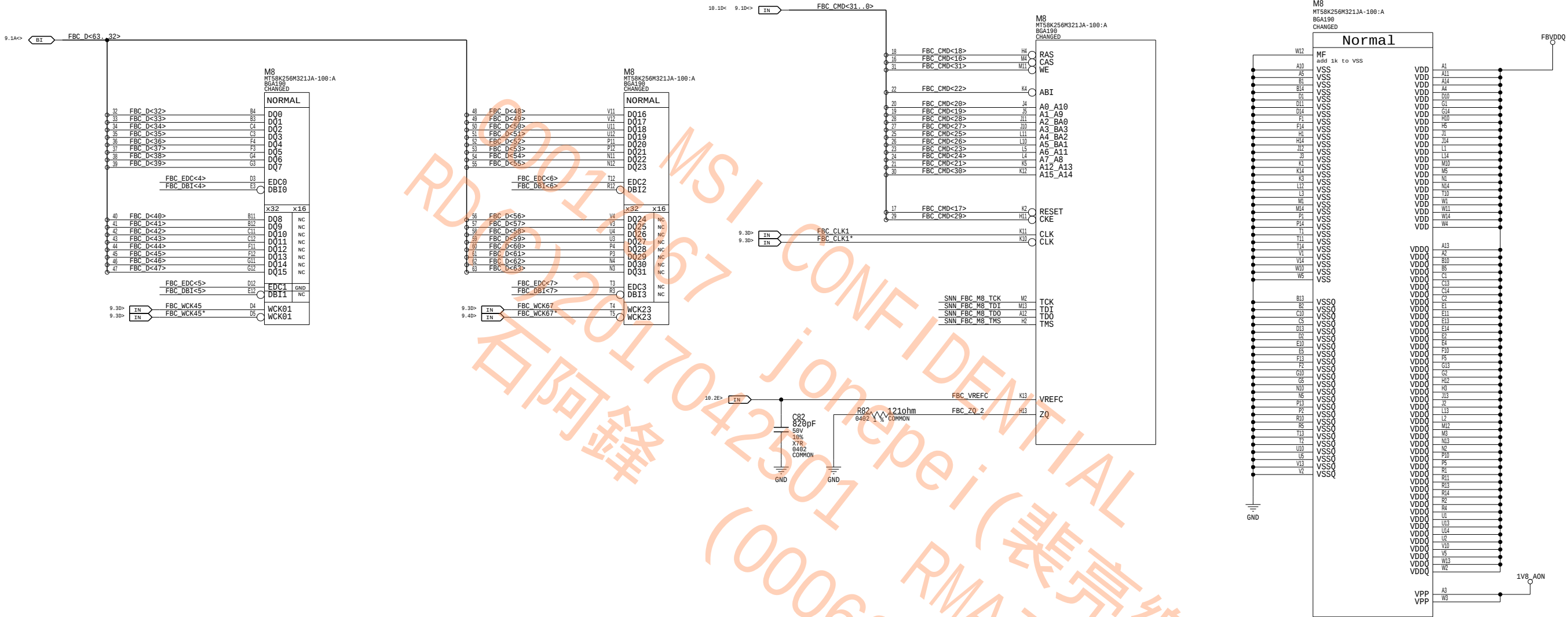
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NV_PN	600-1G611-0050-QS1
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PCB REV	PG611-A00	PAGE	10 OF 49
BOM REV	A	DATE	15-FEB-2017

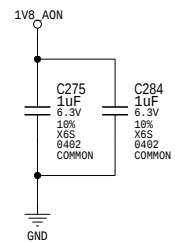
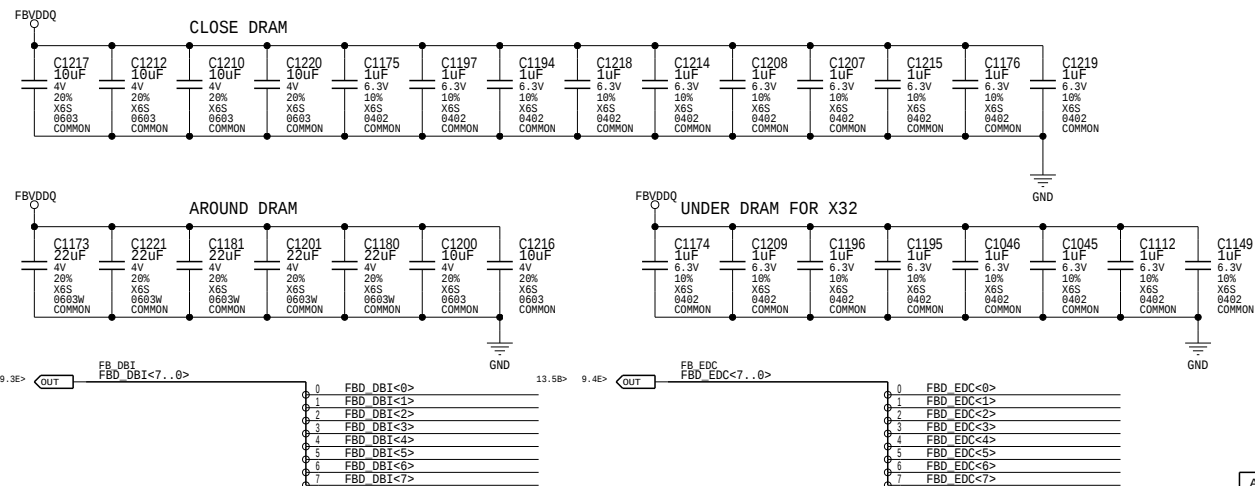
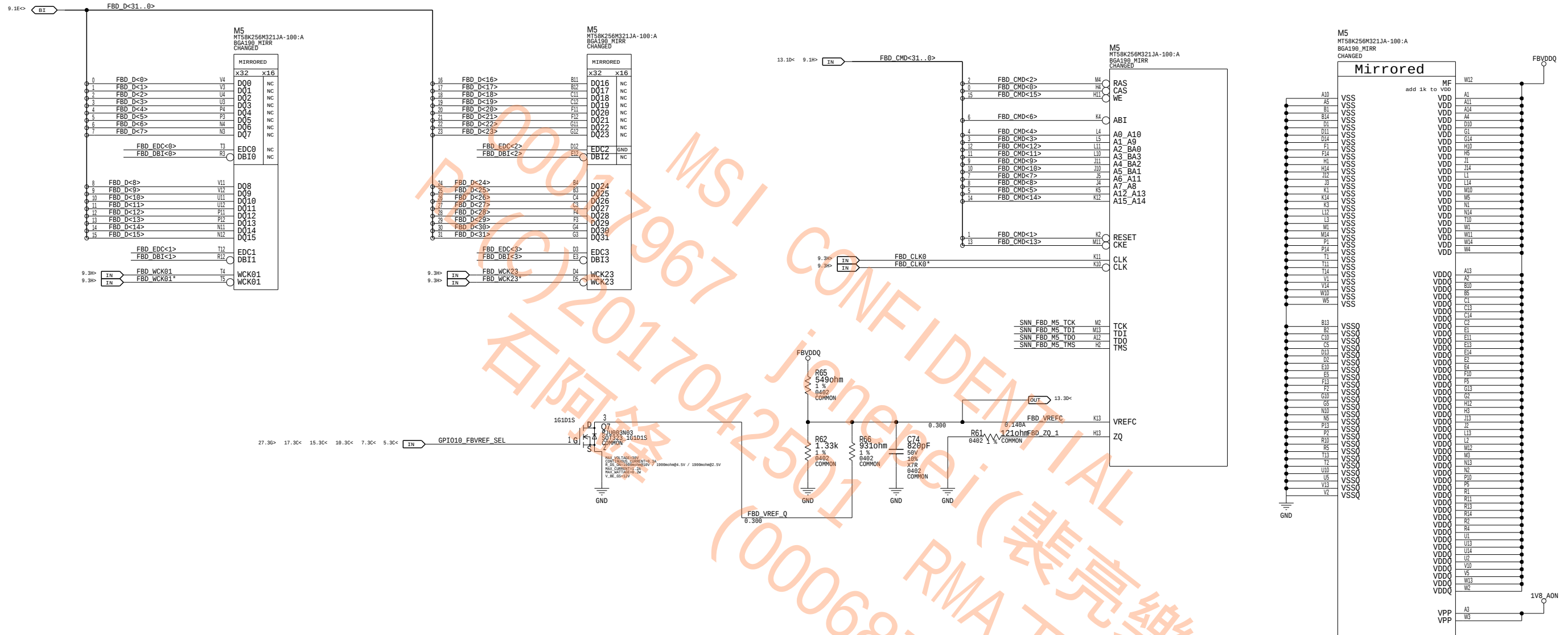




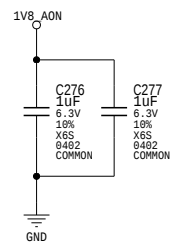
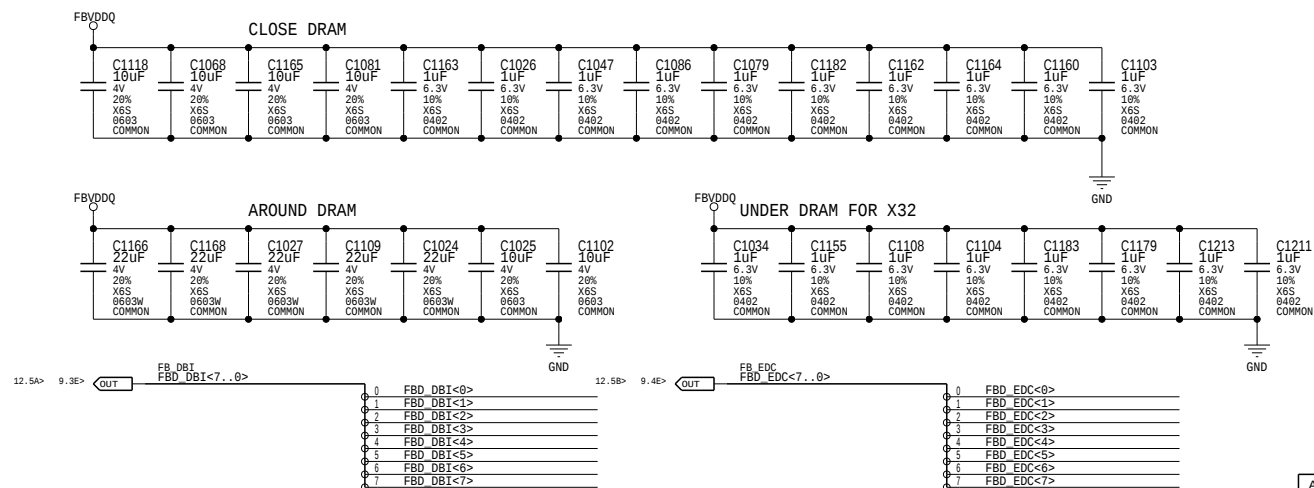
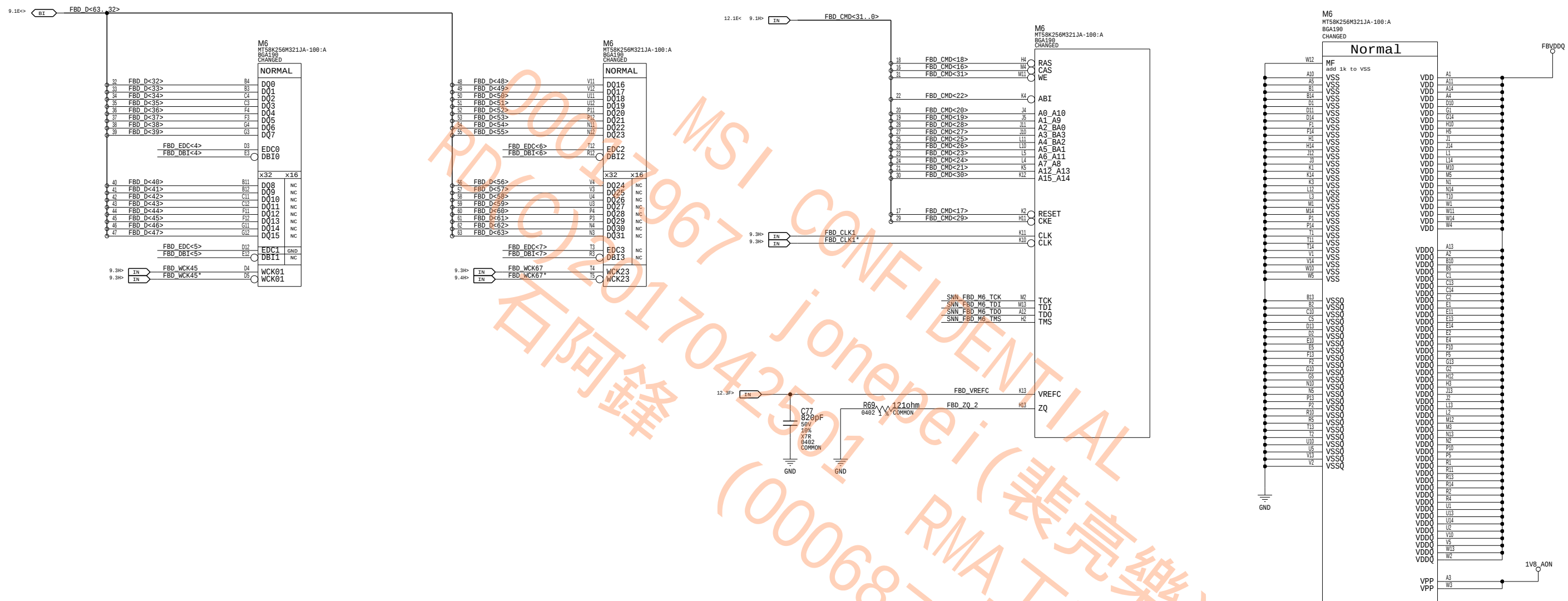
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NV_PN	600-1G611-0050-QS1		
PCB REV	PG611-A00	PAGE	11 OF 49
BOM REV	A	DATE	15-FEB-2017

Page12: MEMORY: FBD Partition 31..0

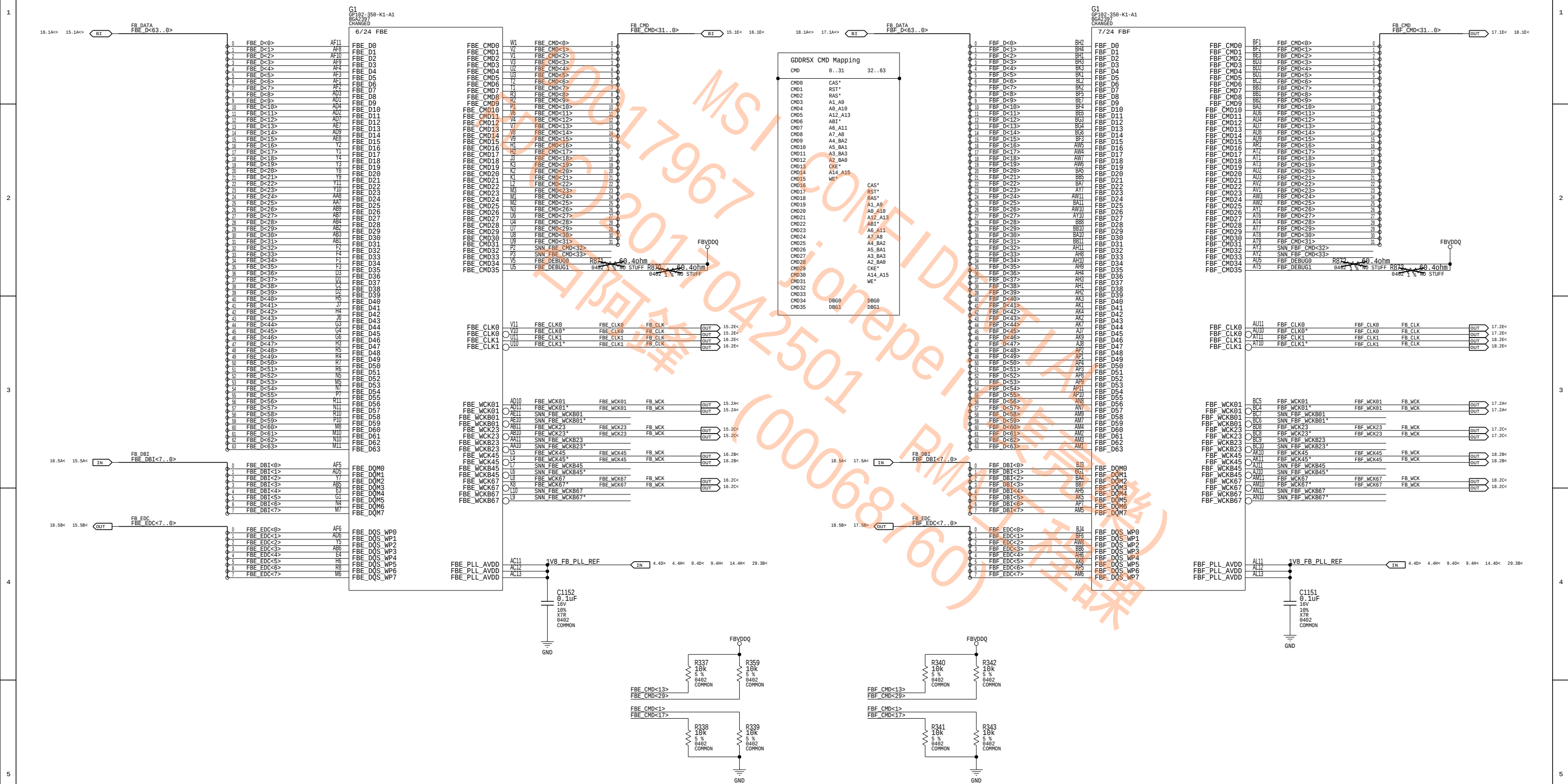


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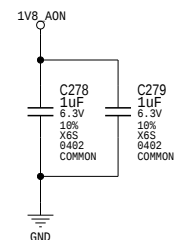
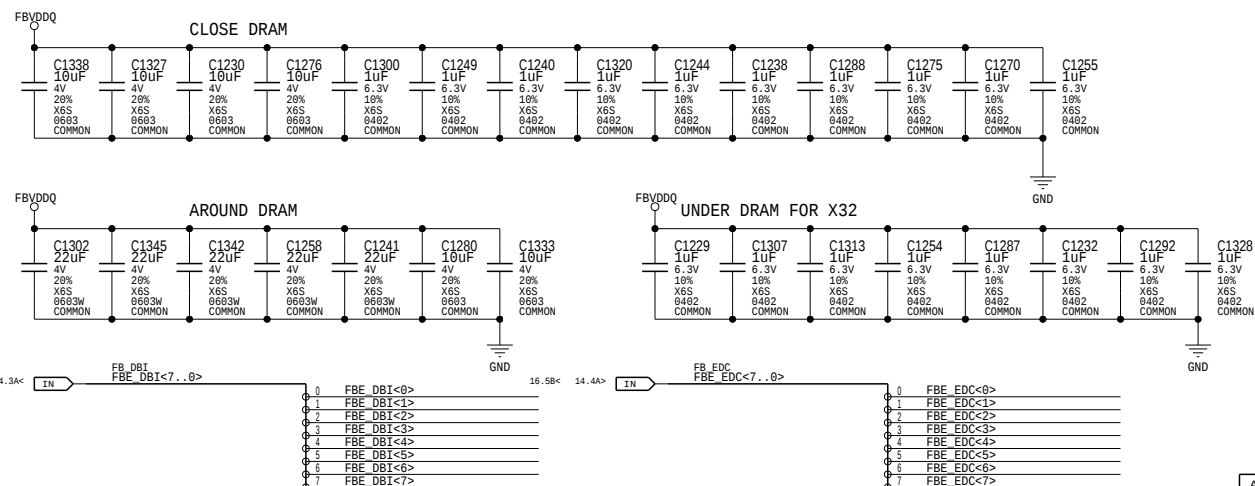
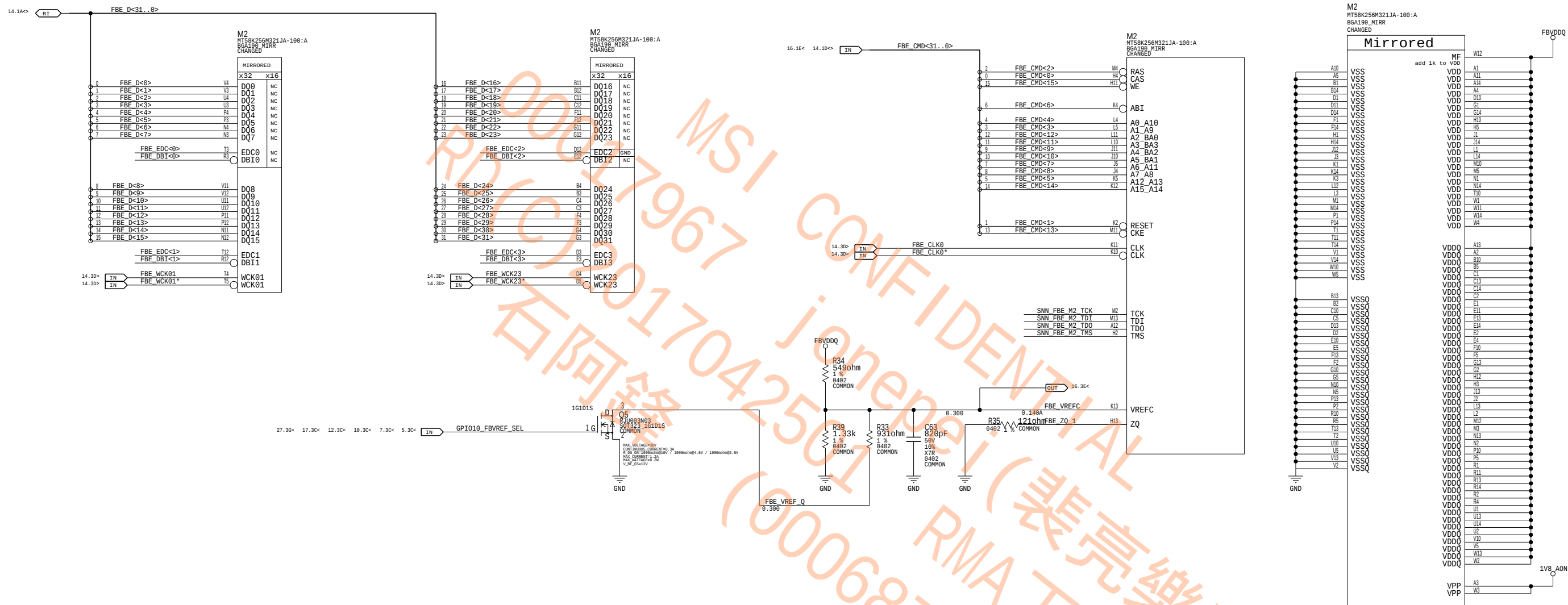


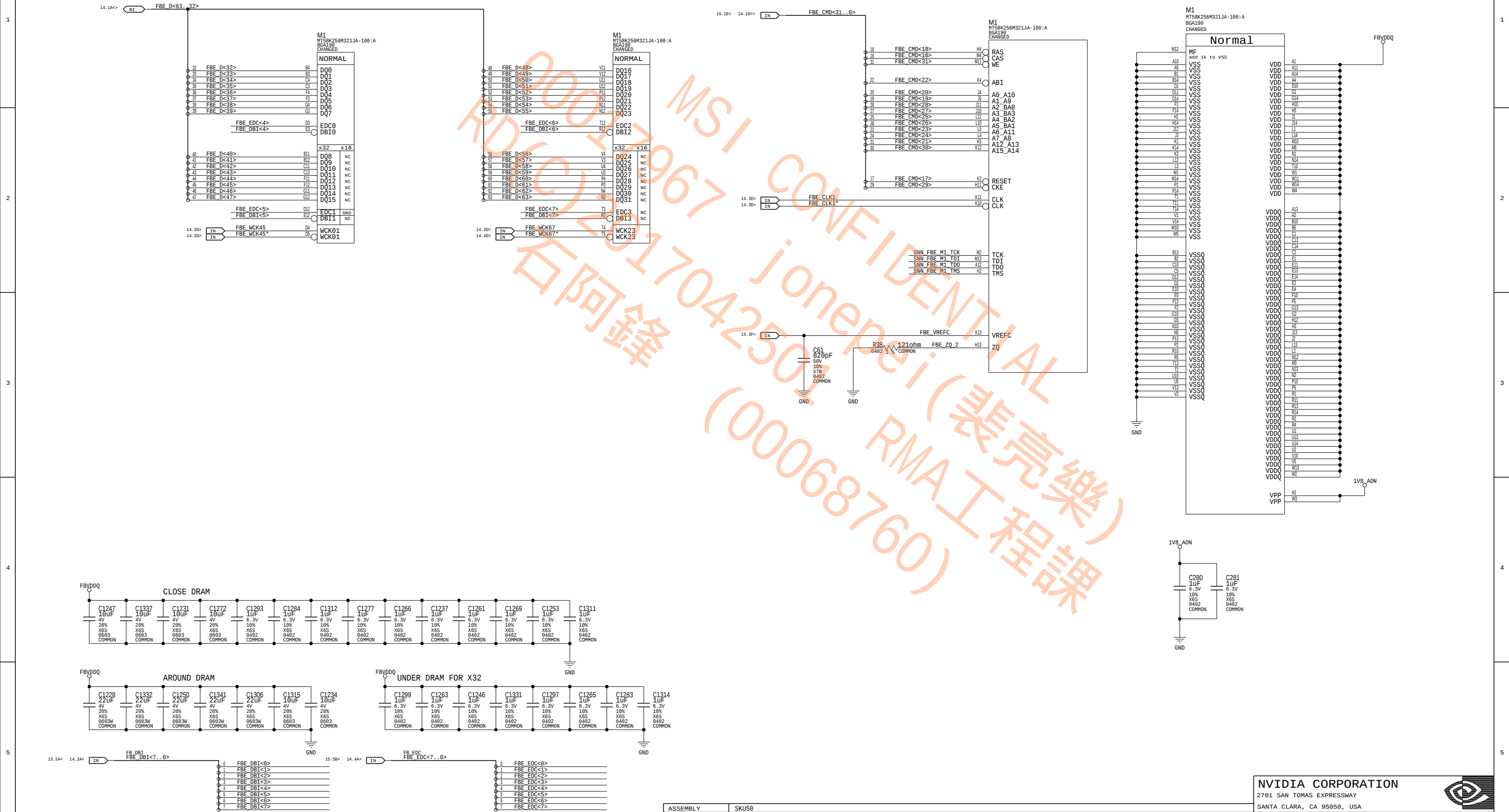
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NV_PLN		600-1G611-0050-QS1		
PCB REV	PG611-A00	PAGE	13 OF 49	
BOM REV	A	DATE	15-FEB-2017	

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Page15: MEMORY: FBE Partition 31..0

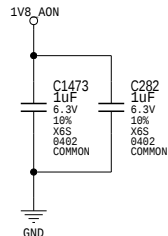
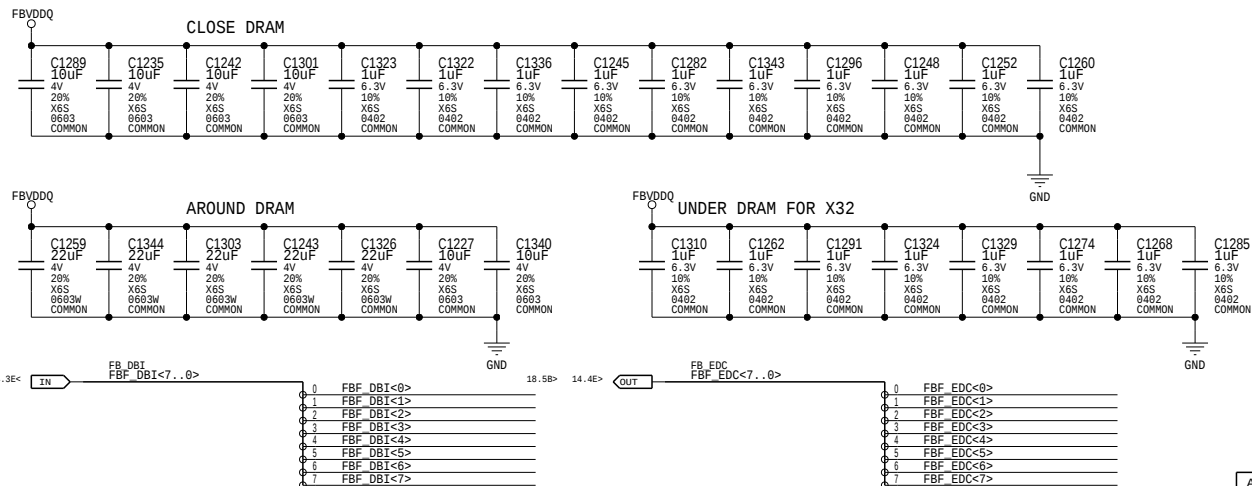
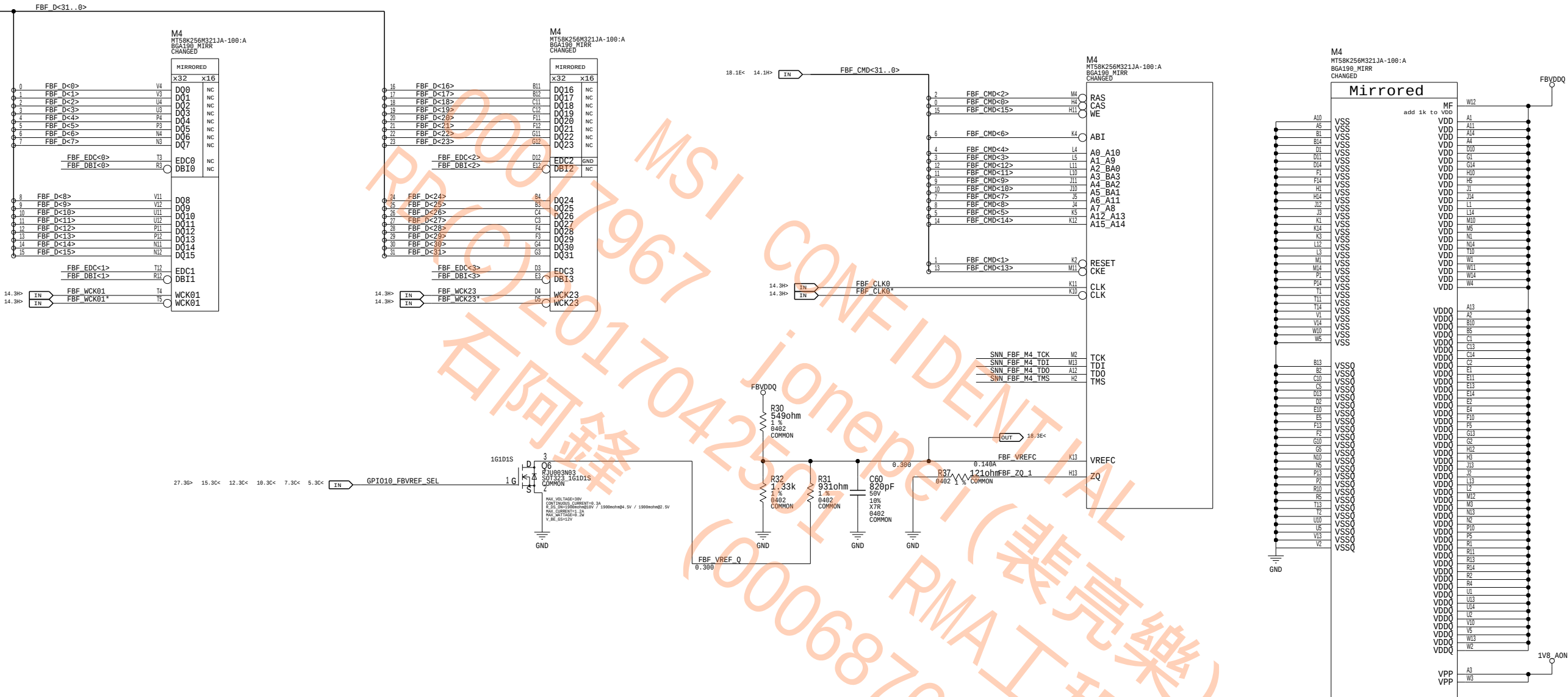


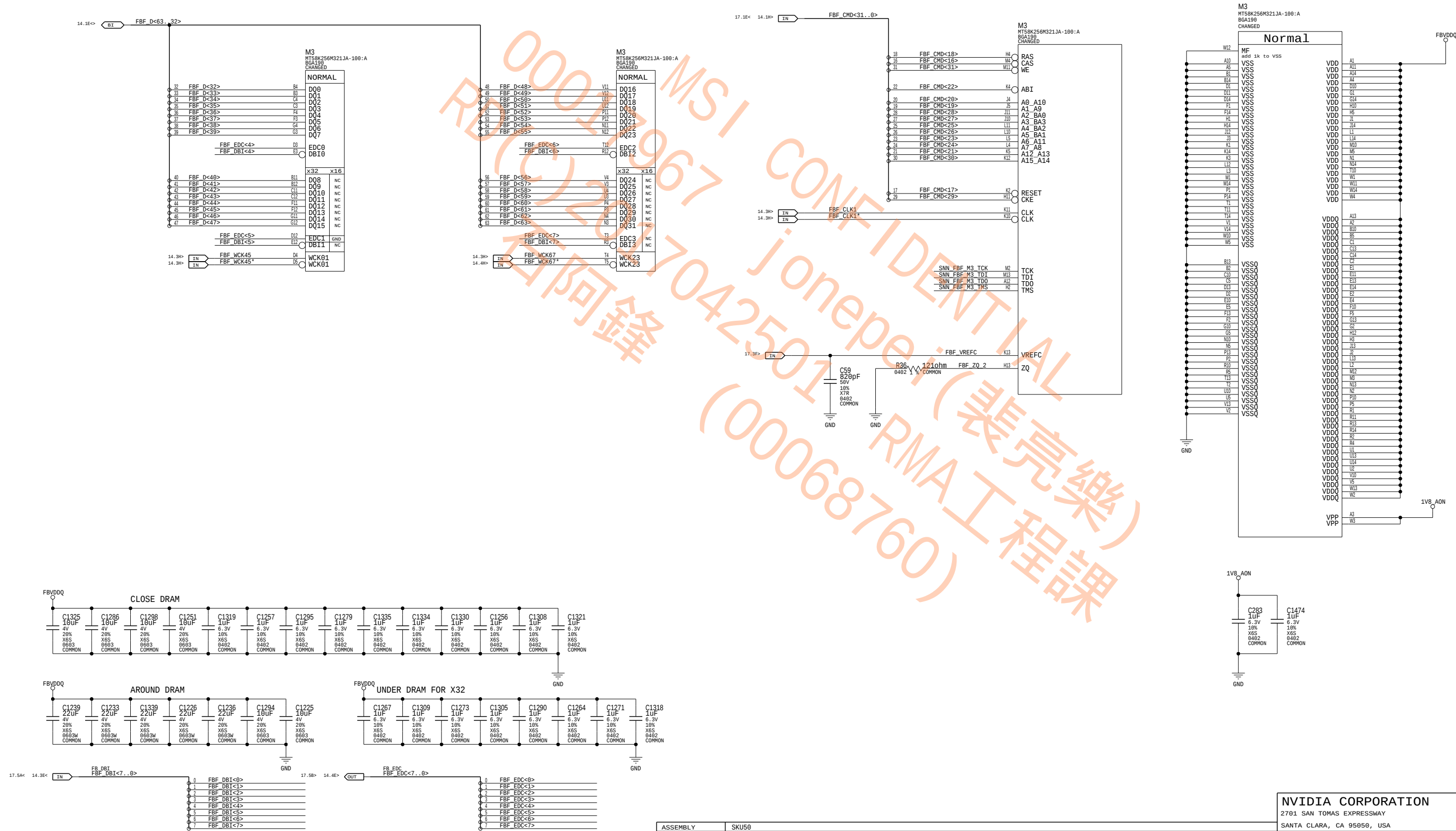


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NV_PN	600-1G611-0050-QS1		
PCB REV	P6611-A00	PAGE	16 OF 49
BOM REV	A	DATE	15-FEB-2017

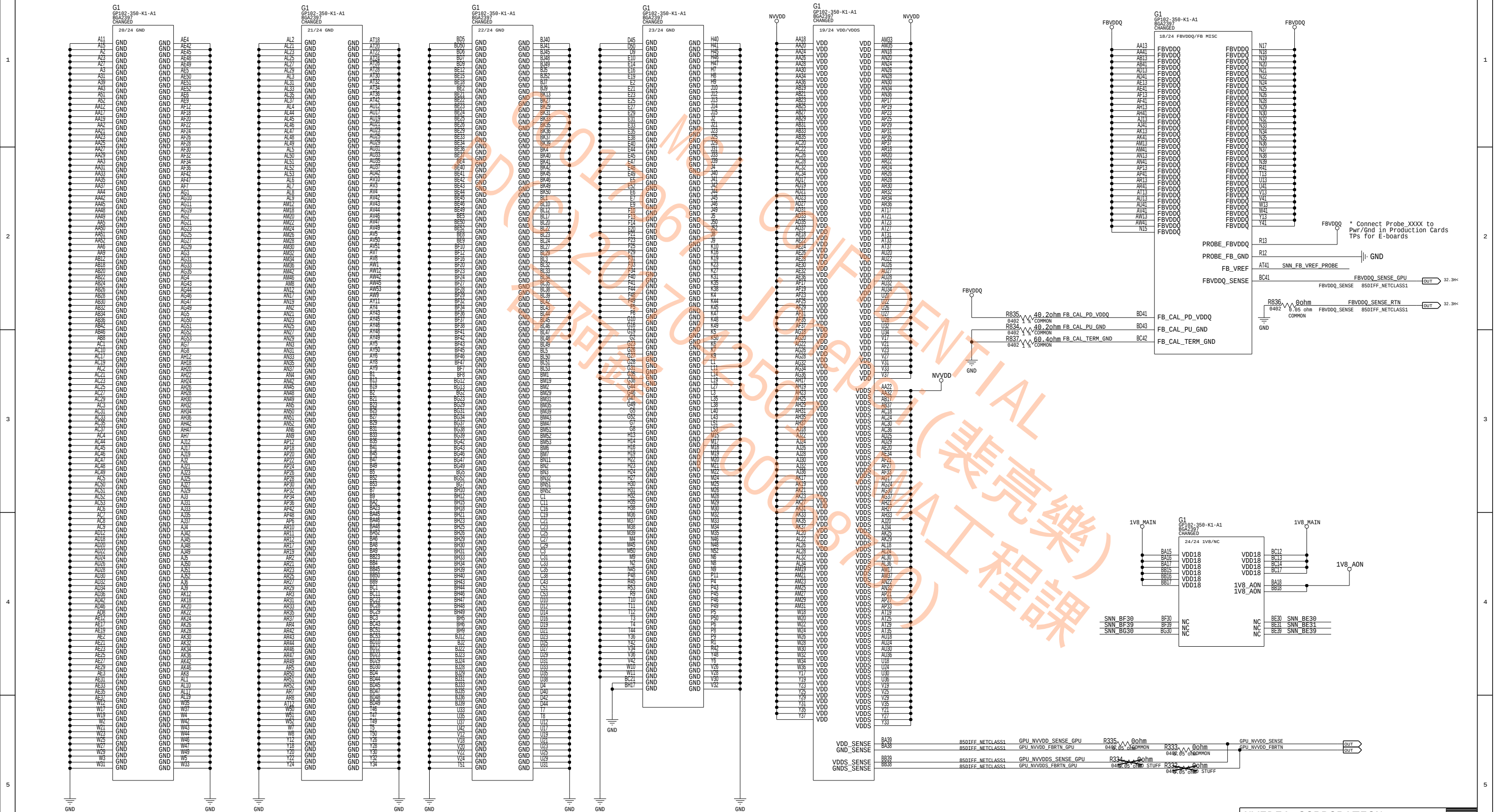
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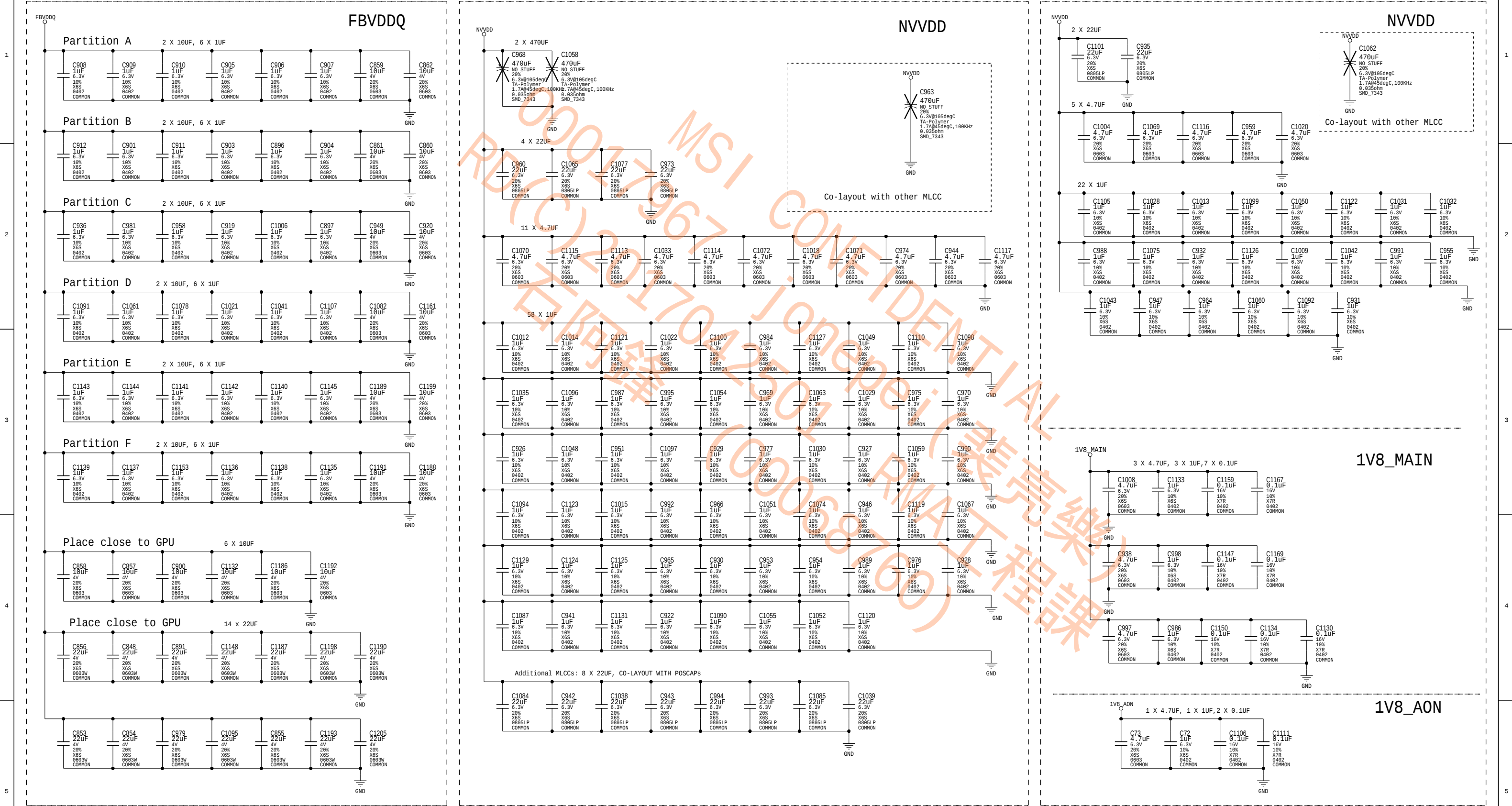




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Page19: GPU PWR and GND





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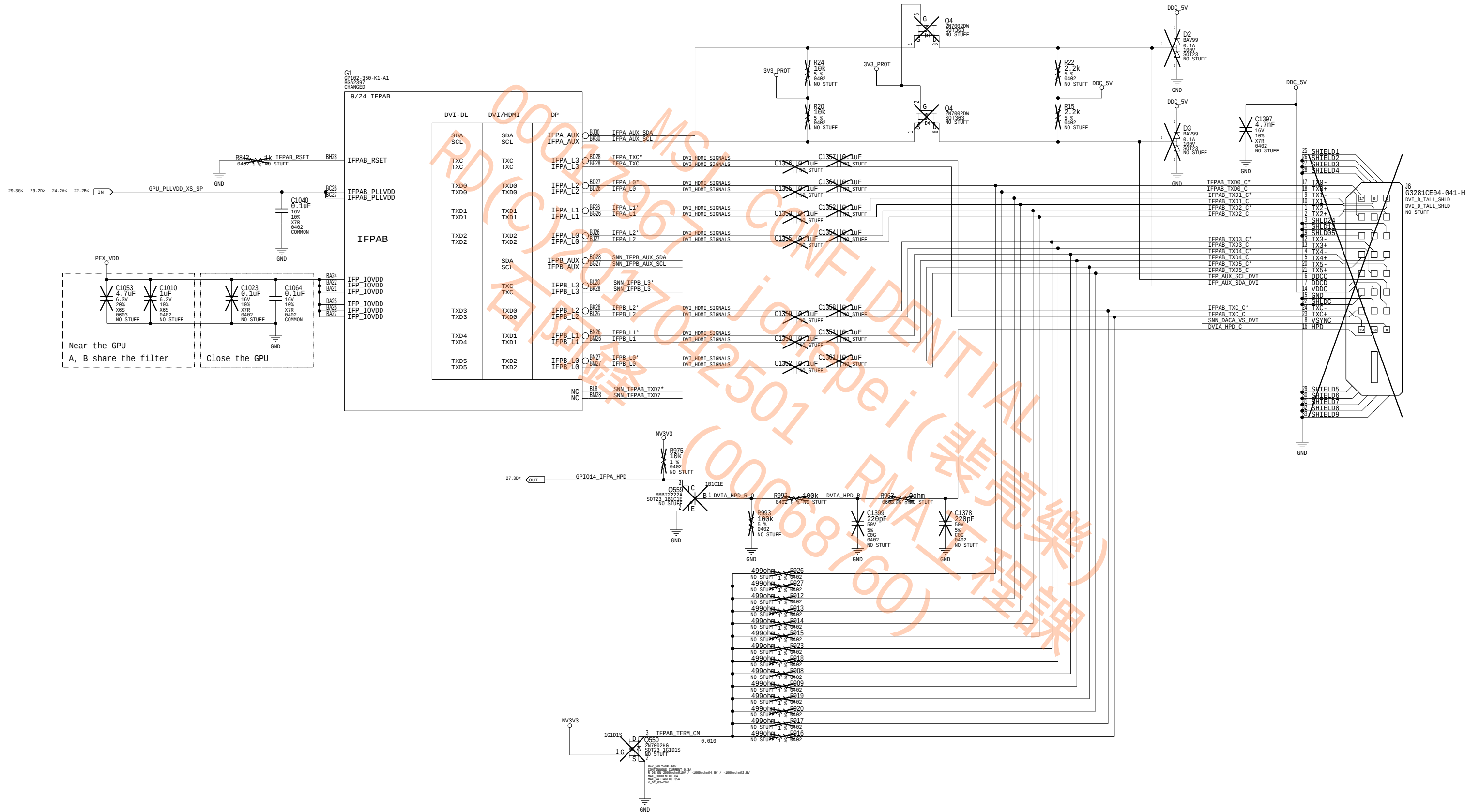
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BOM REV A

PAGE 20 OF 49

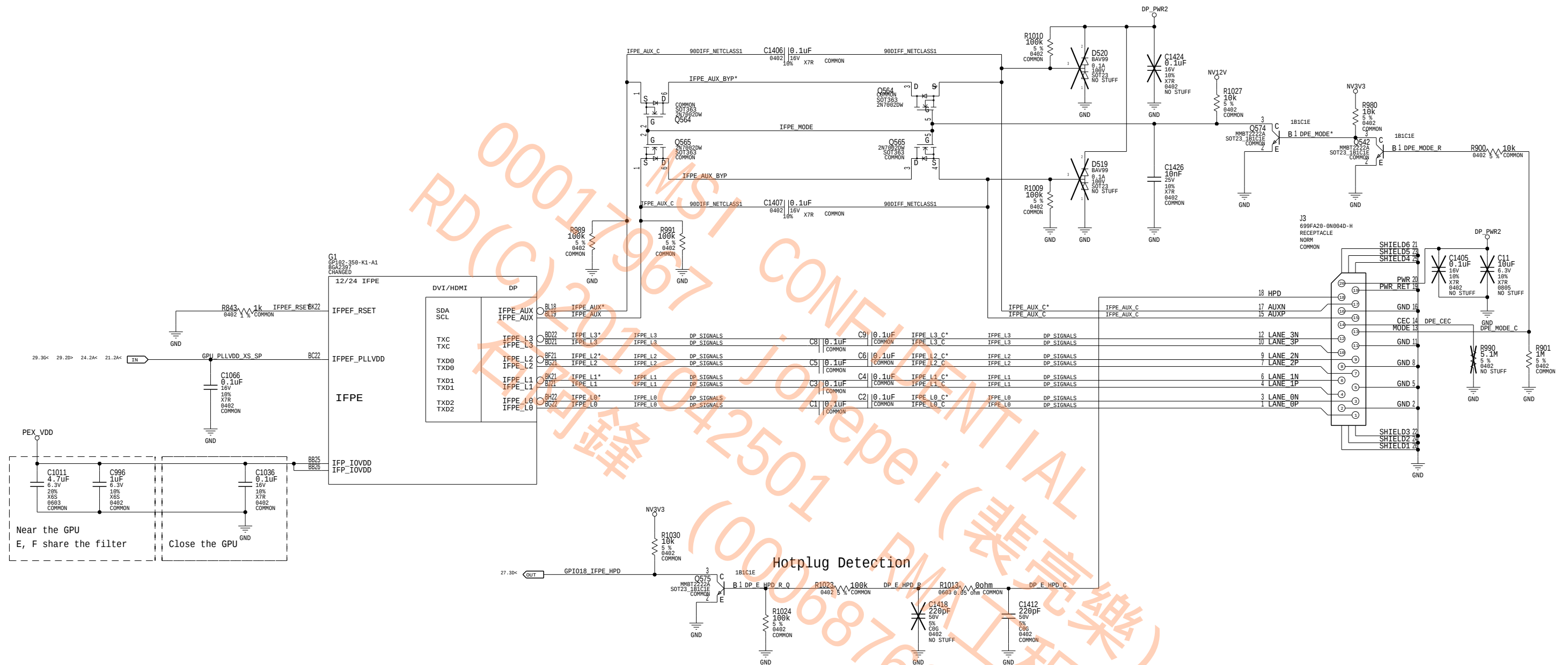
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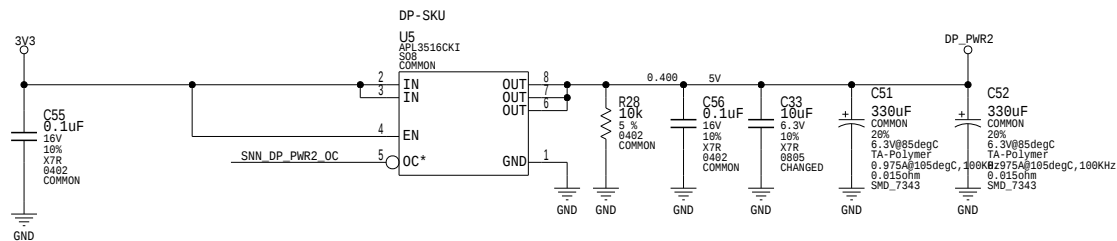
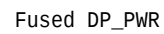
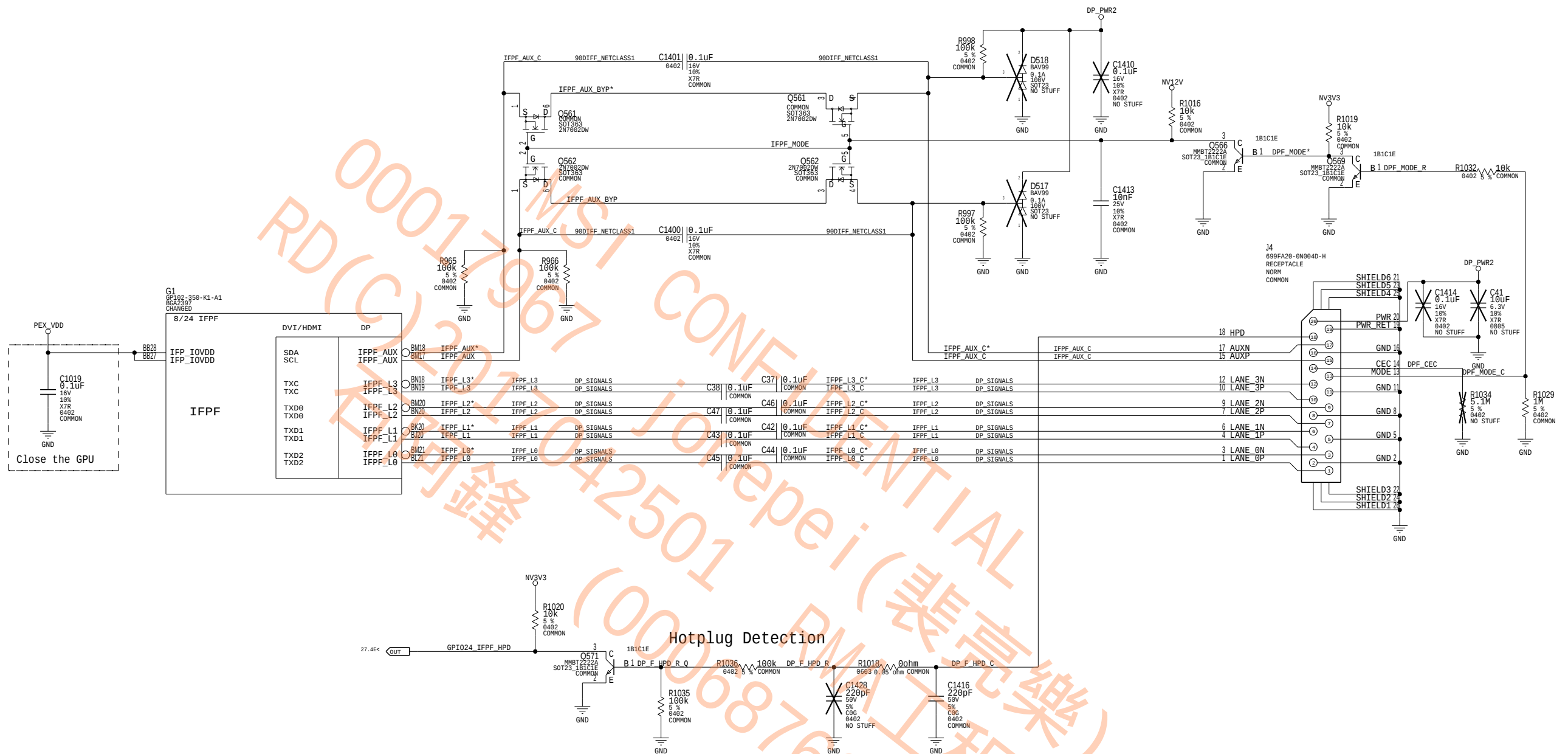




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PAGE DETAIL	IFPAB DVI-D-DL

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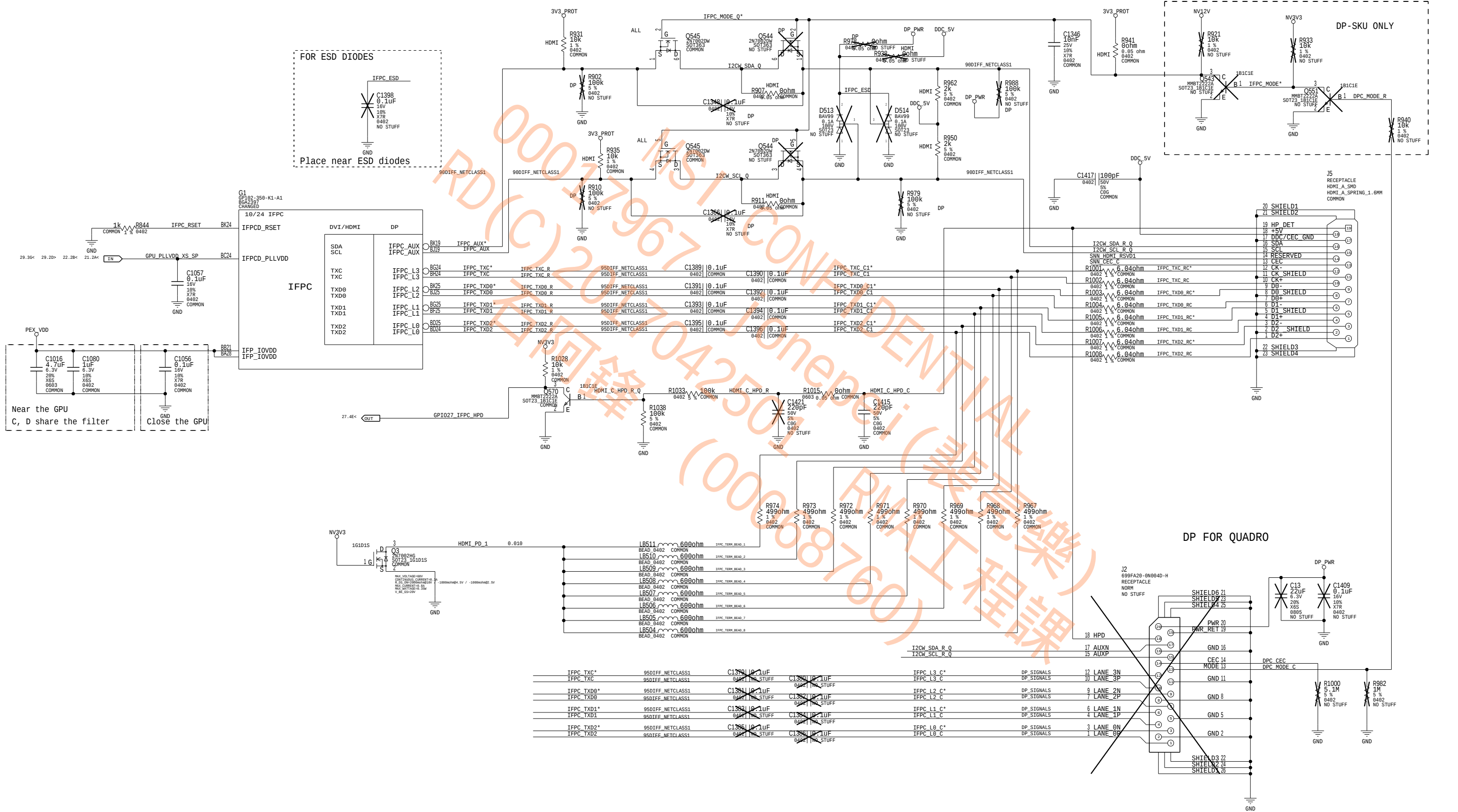




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NV_PN	600-1G6111-0050-QS1		
PCB REV	PG6111-A00	PAGE	23 OF 49
BOM REV	A	DATE	15-FEB-2017



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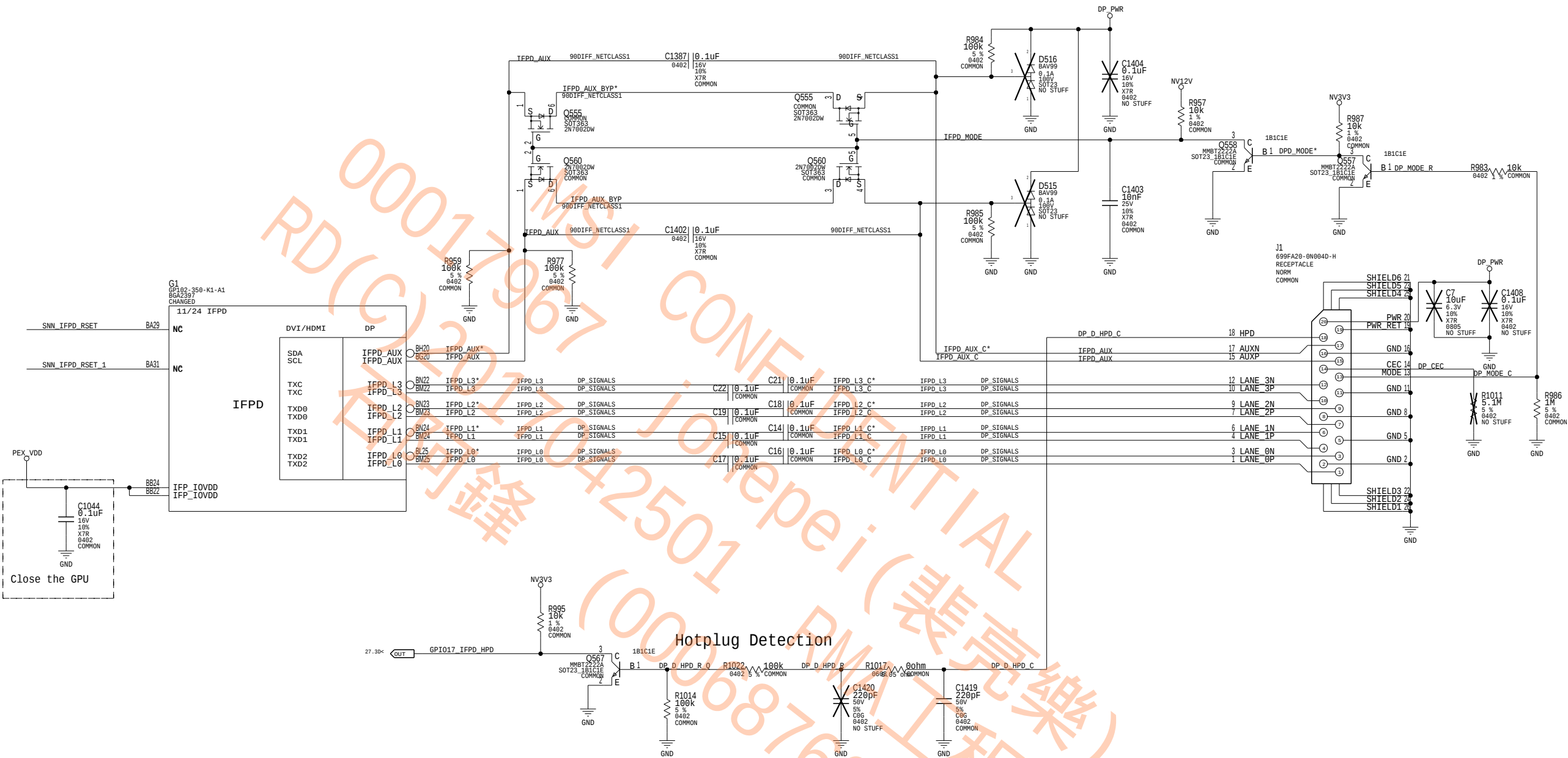
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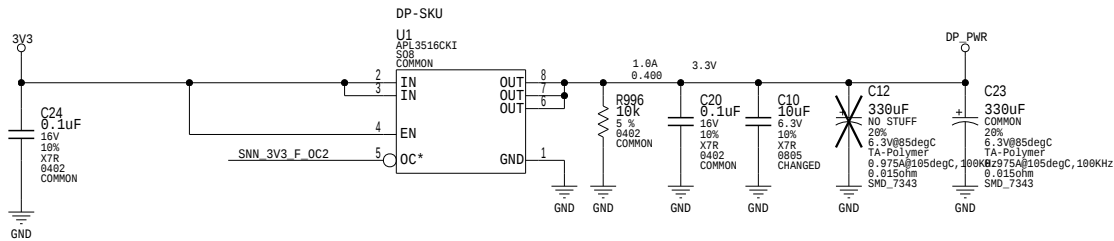
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PCB REV P6611-A00 PAGE 24 OF 49

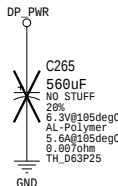
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Fused DP_Pwr



OPTION



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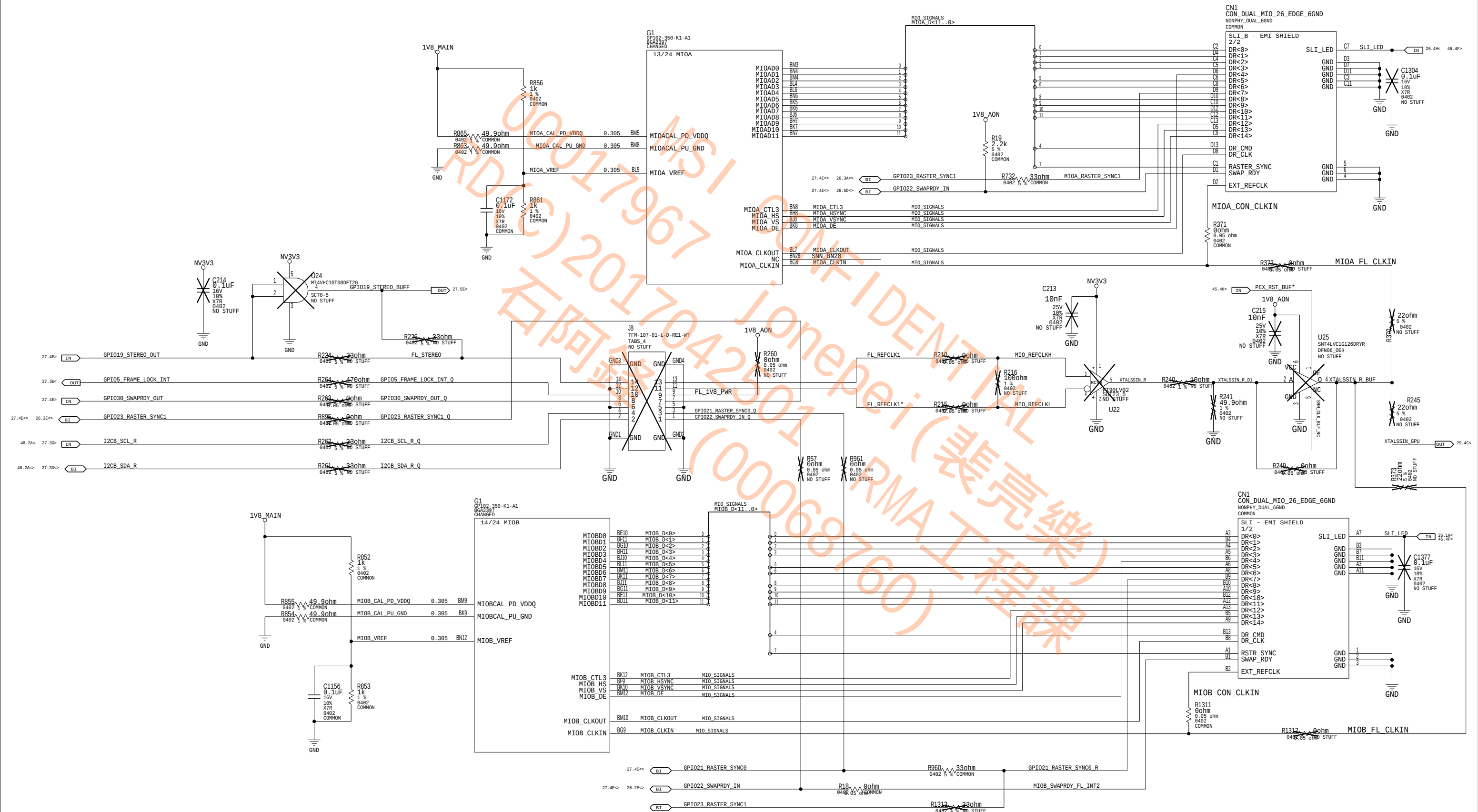
PAGE 25 OF 49

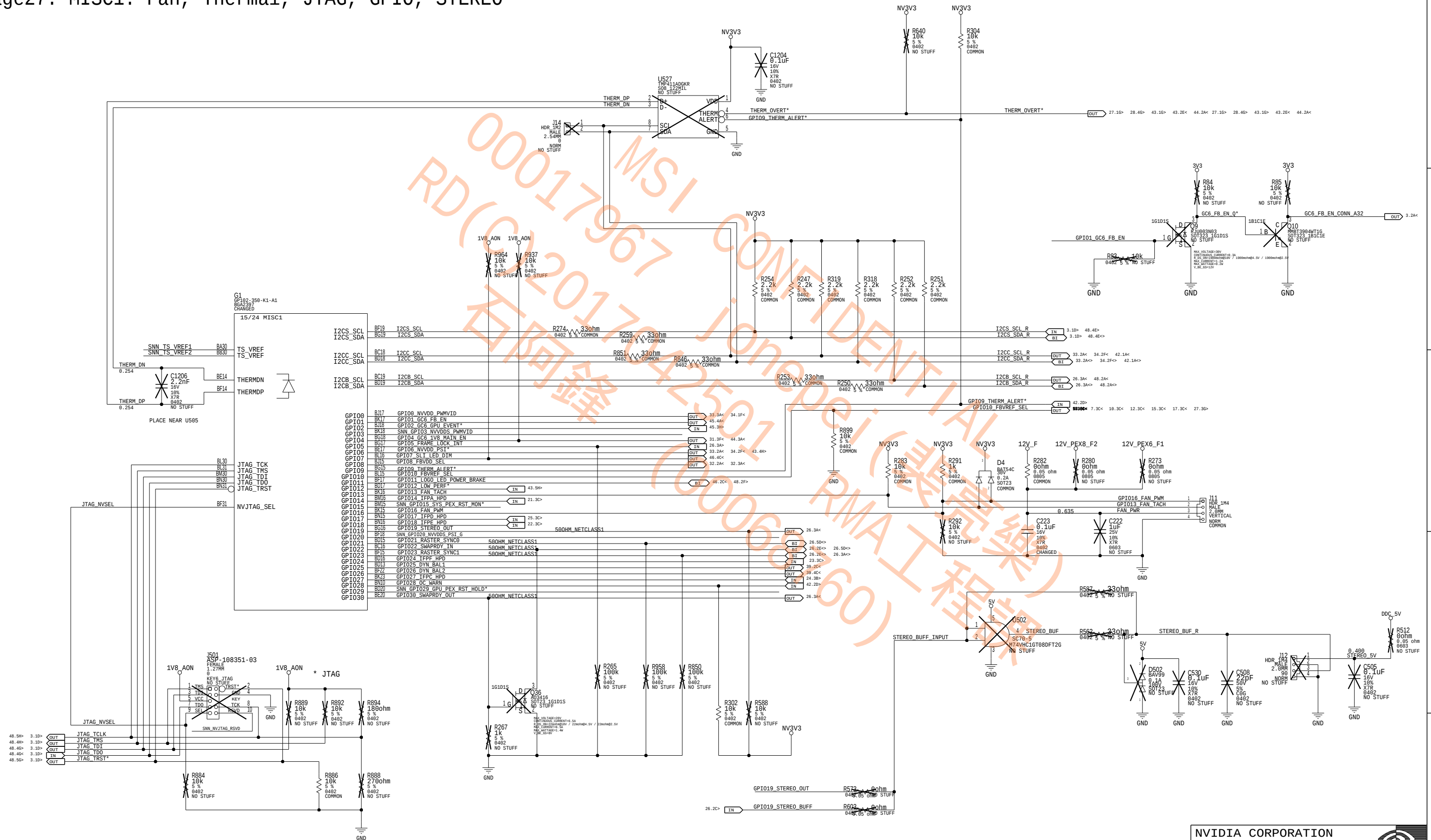
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Page26: MIOA/B Interface and FRAME LOCK





ASSEMBLY	SKU50
PAGE DETAIL	MISC: FAN, THERMAL, JTAG, GPIO, STEREO

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NV_PN	600-1G611-0050-QS1
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PCB REV	PG611-A00	PAGE	27 OF 49
BOM REV	A	DATE	15-FEB-2017

Page28: MISC2: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	L	L	00100
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0] 1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT SOR0/1/2/3 ENABLE
L	L	H	1110
L	H	L	1101
L	H	H	1100
H	L	L	1011
H	L	H	1010
H	H	L	1001
H	H	H	1000
L	L	M	0111
L	M	L	0110
L	M	H	0101
L	H	M	0100
H	L	M	0011
H	M	L	0010
H	M	H	0001
H	H	M	0000

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

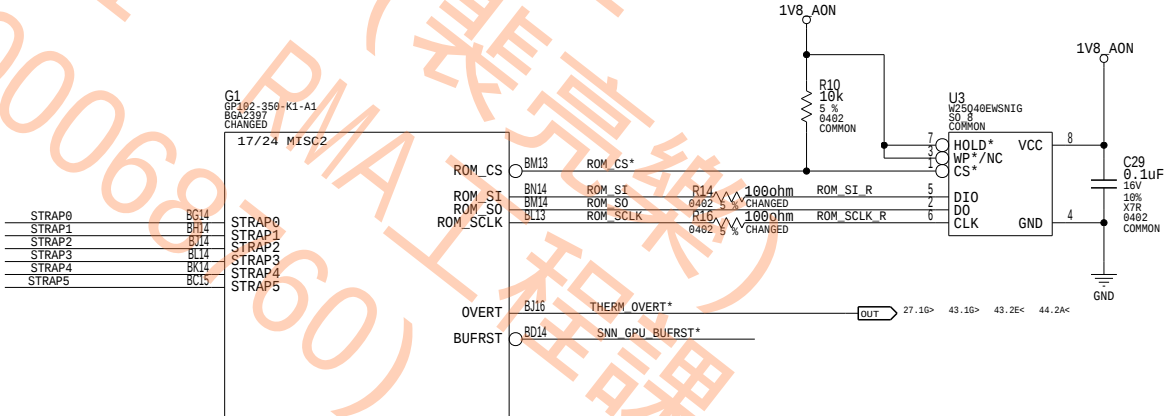
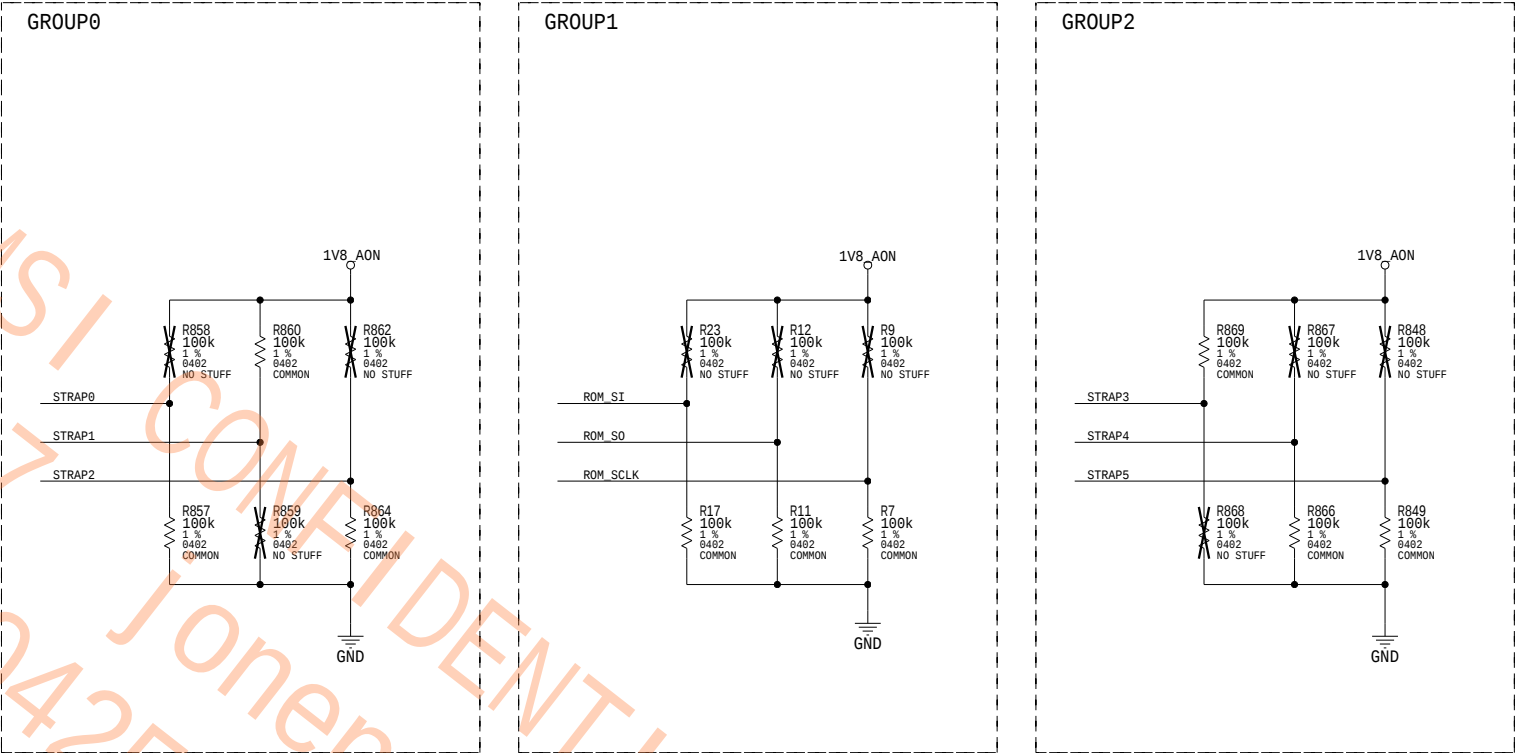
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

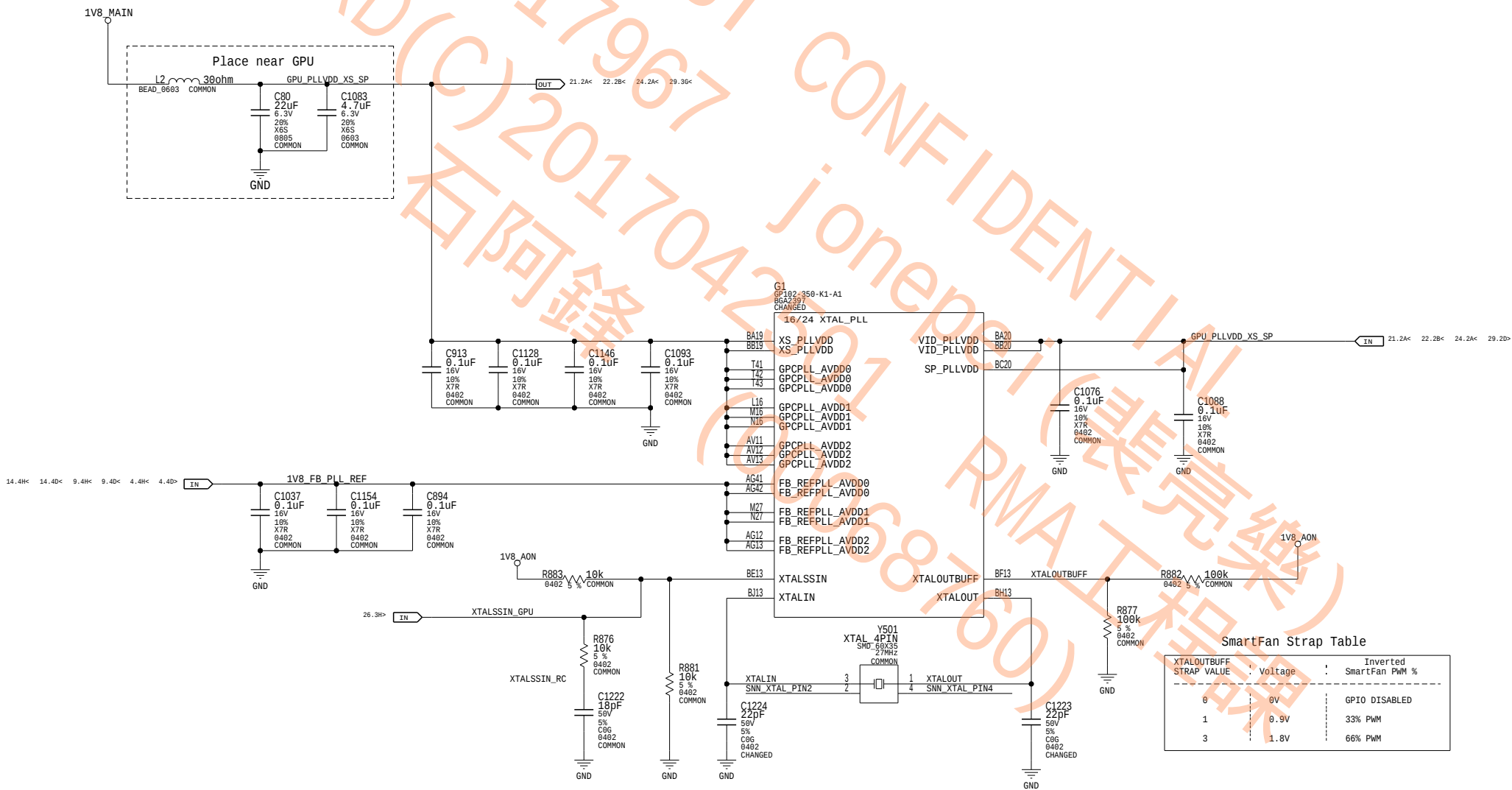
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

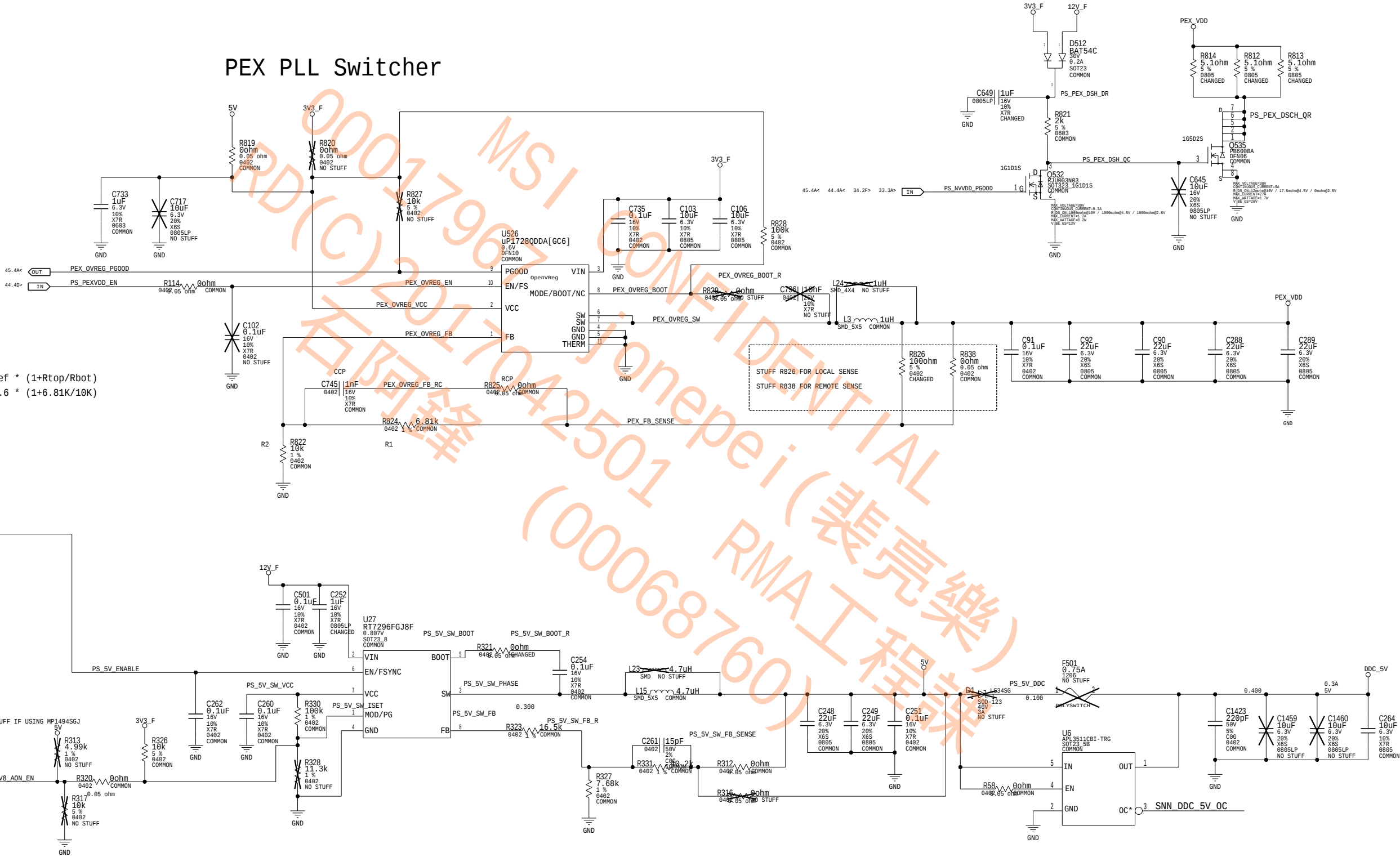
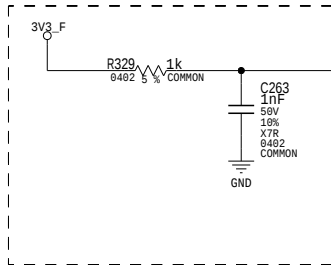


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PEX PLL Switcher

$V_{out} = V_{ref} * (1 + R_{top}/R_{bot})$
 $1.008 = 0.6 * (1 + 6.81K/10K)$



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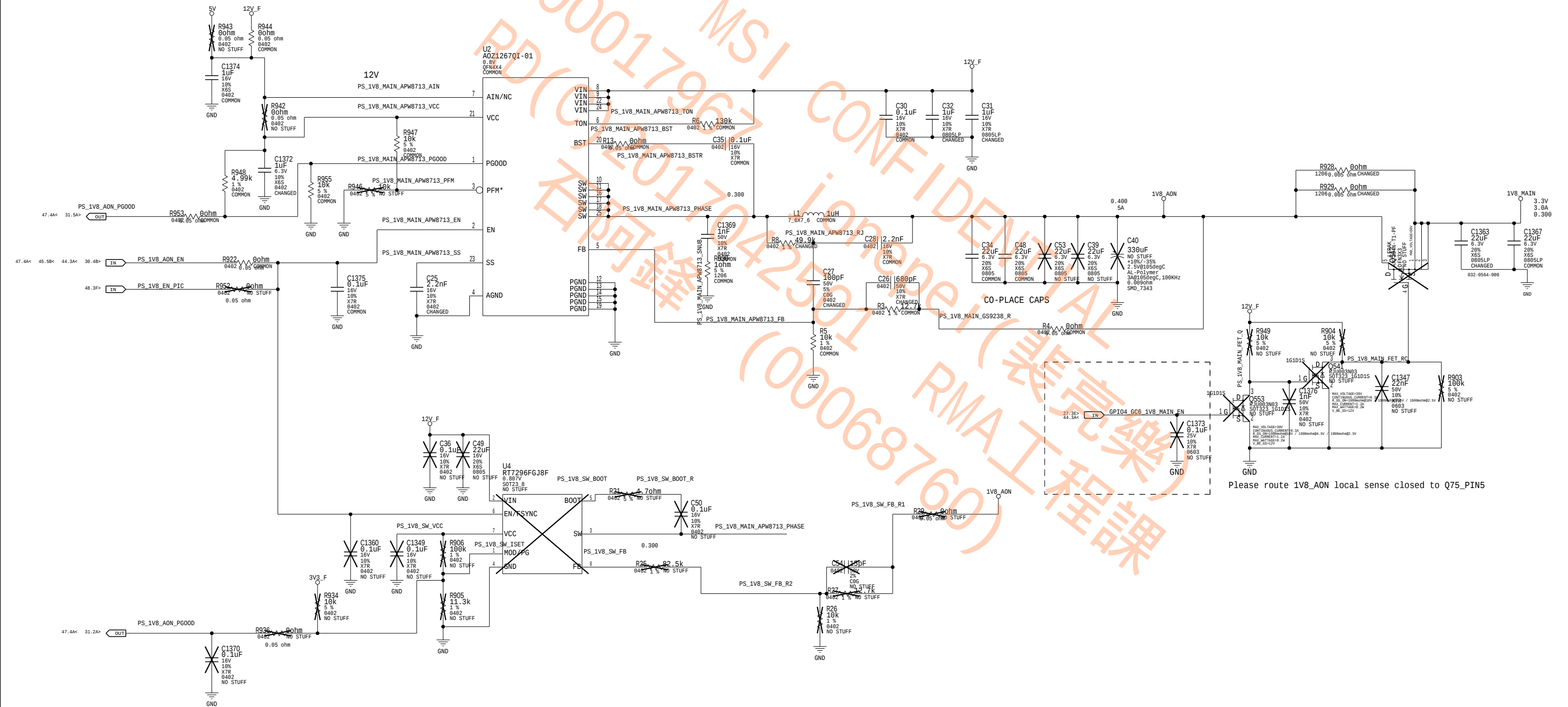


NV_PN 600-16611-0050-QS1

PCB REV	PG611-A00	PAGE	30 OF 49
BOM REV	A	DATE	15-FEB-2017

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Page31: PS: 1V8 Rails



$$1.8 = 0.8 * (1 + 18.7K/15K)$$

$$V_{out} = V_{ref} * (1 + R_{top}/R_{bot})$$

ASSEMBLY	SKU50
PAGE DETAIL	PS: 1V8 Rails

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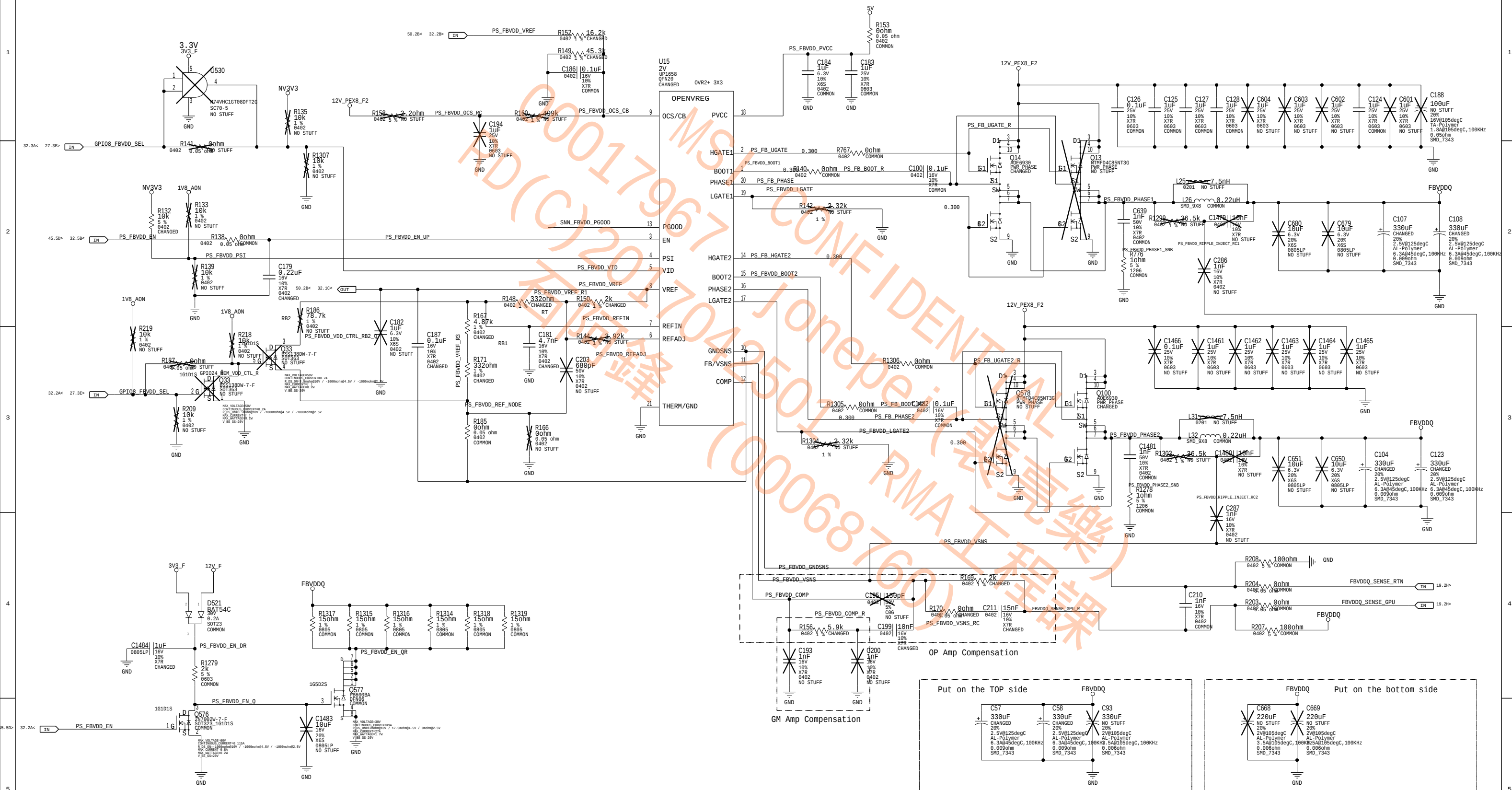
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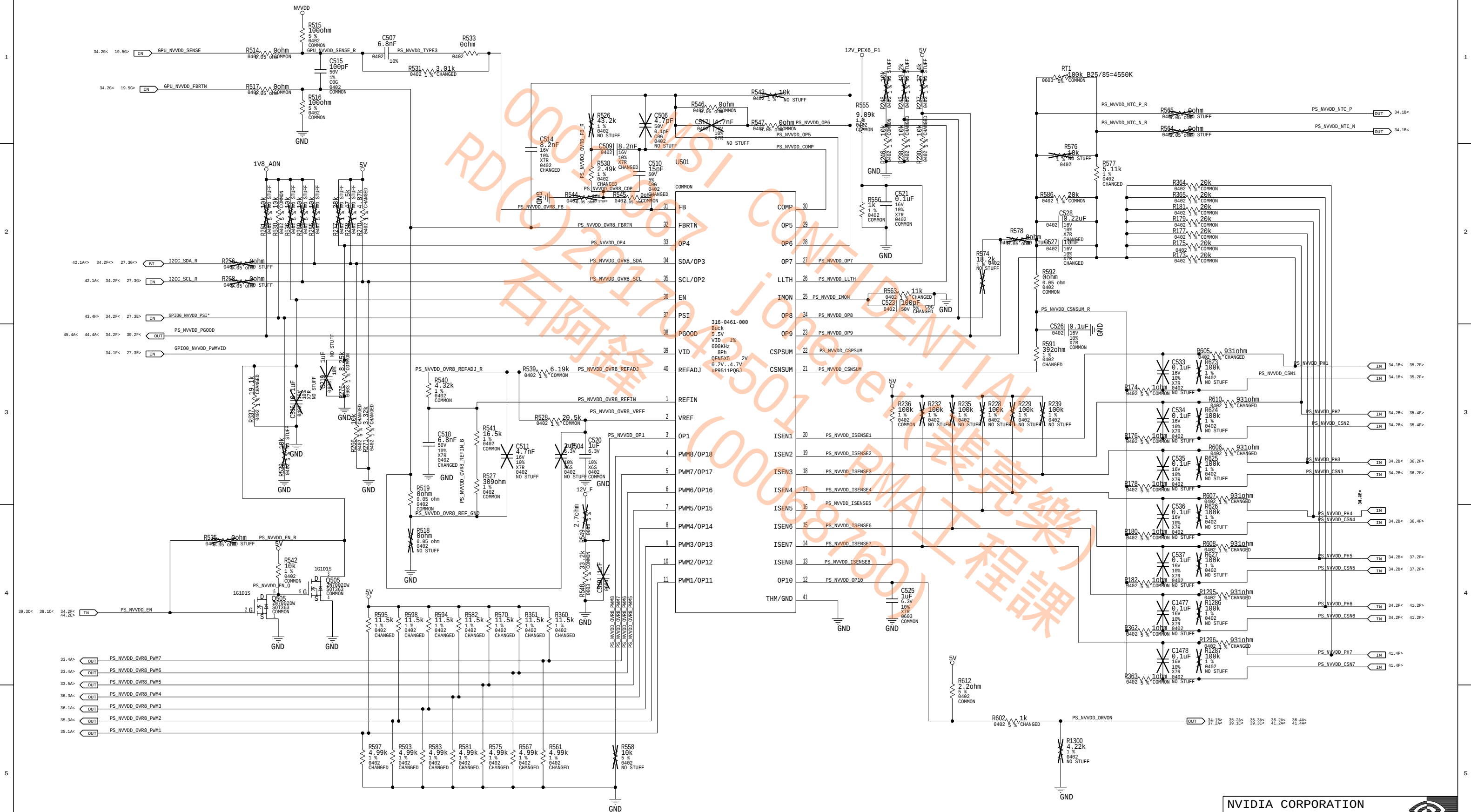
NV_PN	600-1G611-0050-QS1
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PCB REV	PG611-A00	PAGE	31 OF 49
BOM REV	A	DATE	15-FEB-2017





Page33: PS: NVVDD Controller_OVR8



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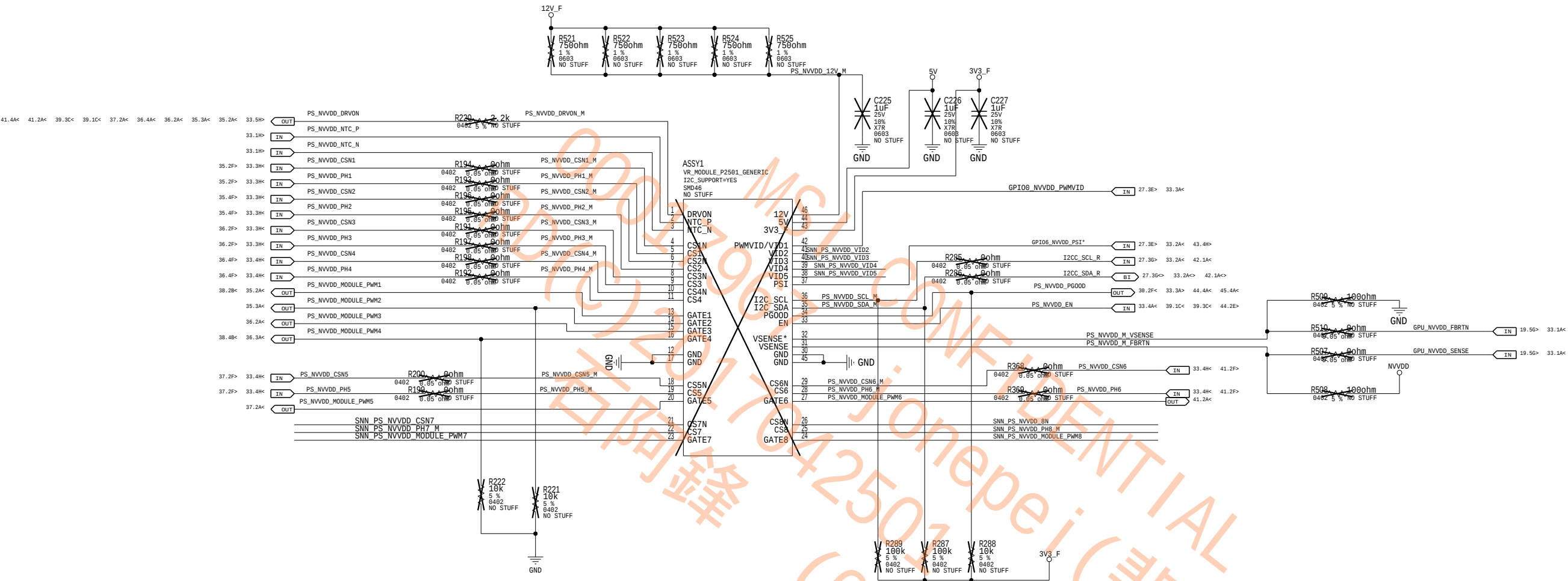
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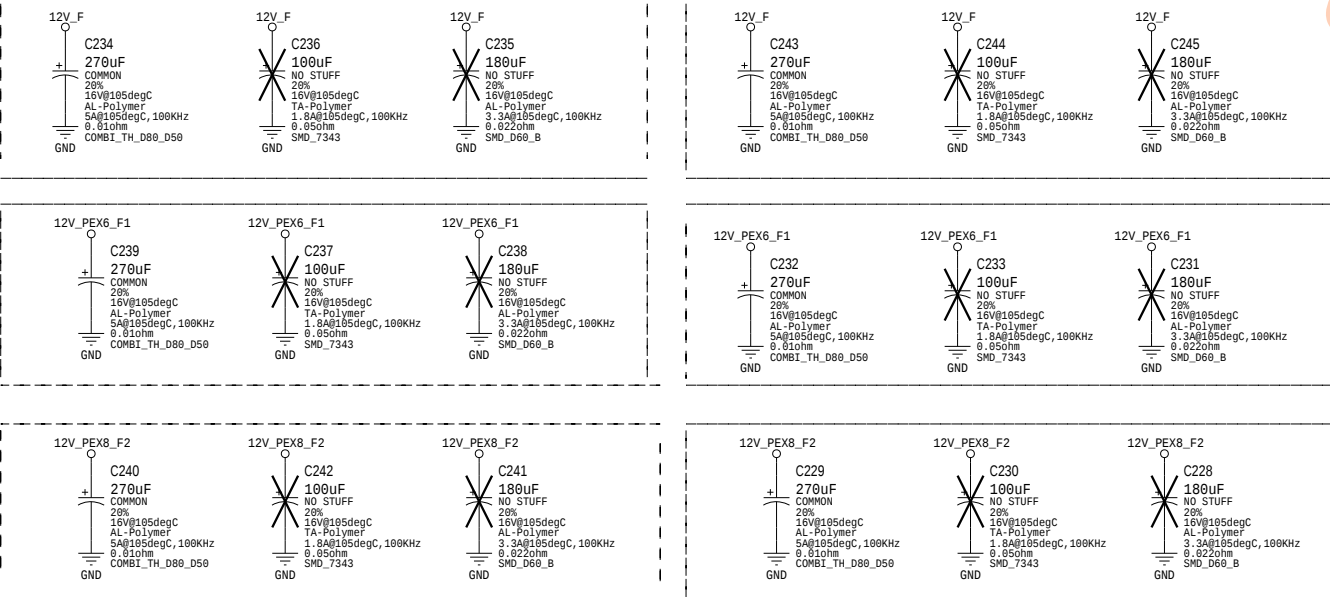
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PCB REV	PG611-A00	PAGE	33 OF 49
BOM REV	A	DATE	15-FEB-2017

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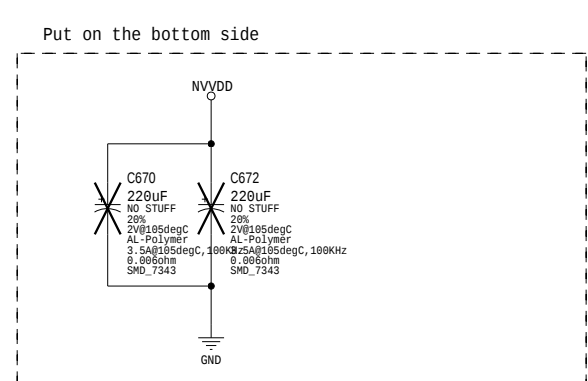
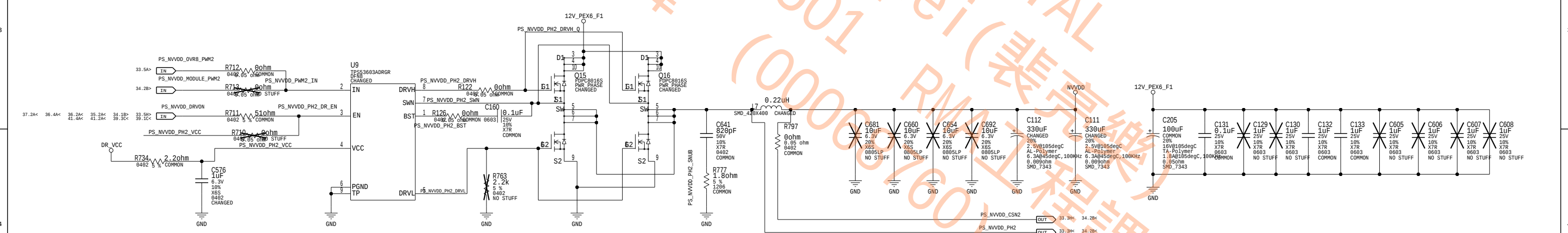
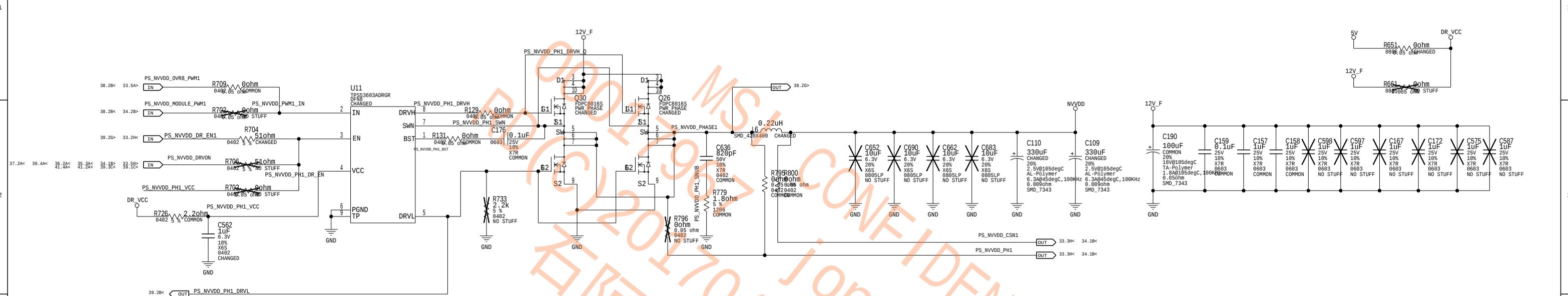


CO-LAYOUT: CHOOSE ONE ONLY



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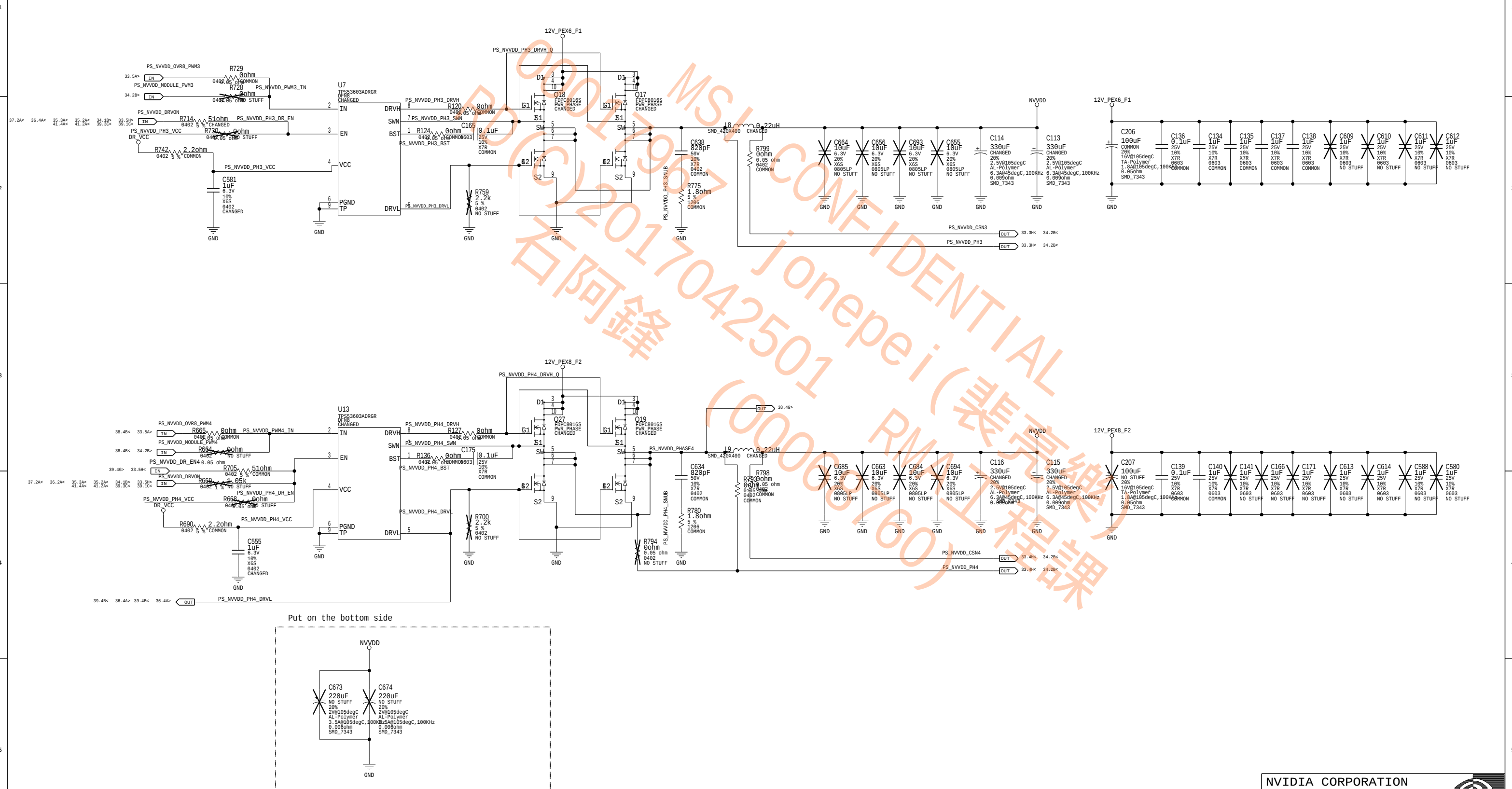
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PCB REV	PG611-A00	PAGE	34 OF 49
BOM REV	A	DATE	15-FEB-2017



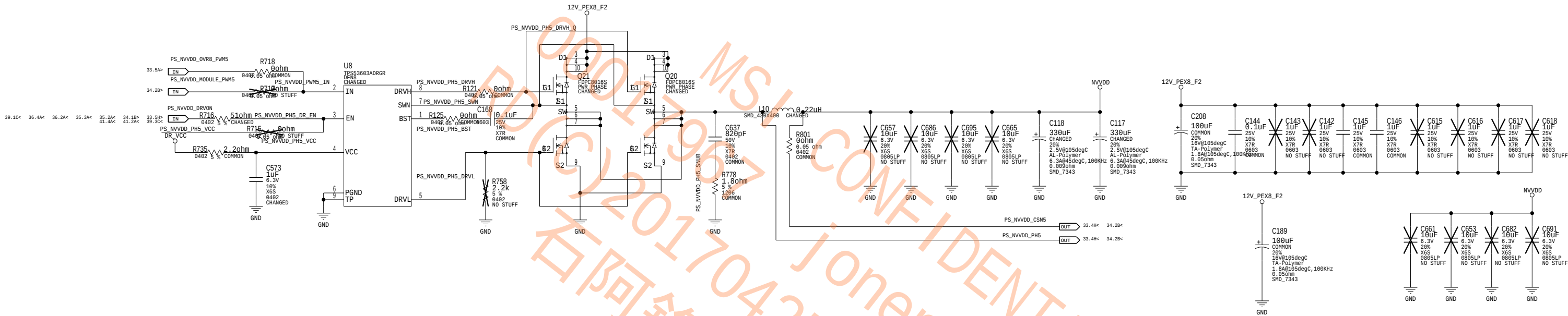
ASSEMBLY	SKU50
PAGE DETAIL	PS: NVVDD Phase 1, 2

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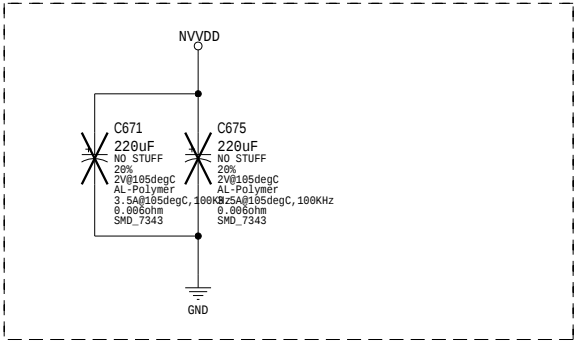
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PCB REV		P6B11-A00		PAGE	35 OF 49
BOM REV		A		DATE	15-FEB-2017



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NV_PN	600-1G611-0050-QS1		
PCB REV	P6G11-A00	PAGE	36 OF 49
BOM REV	A	DATE	15-FEB-2017



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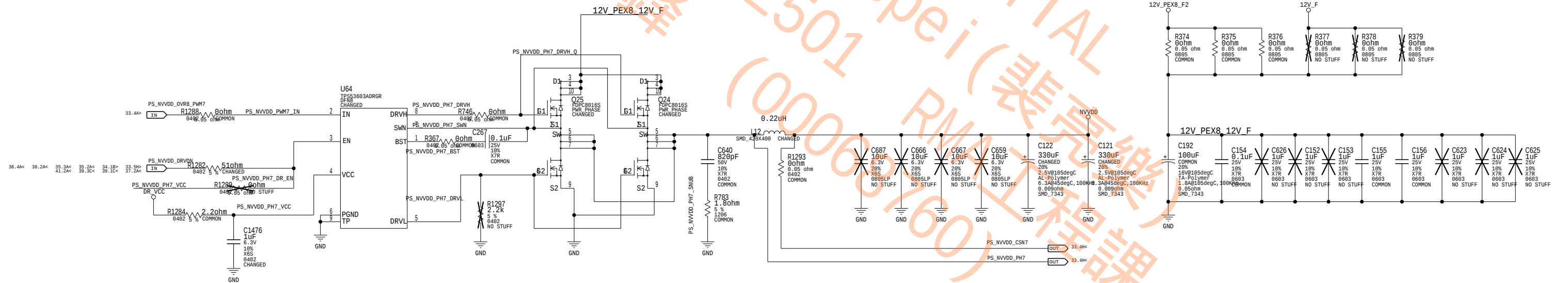
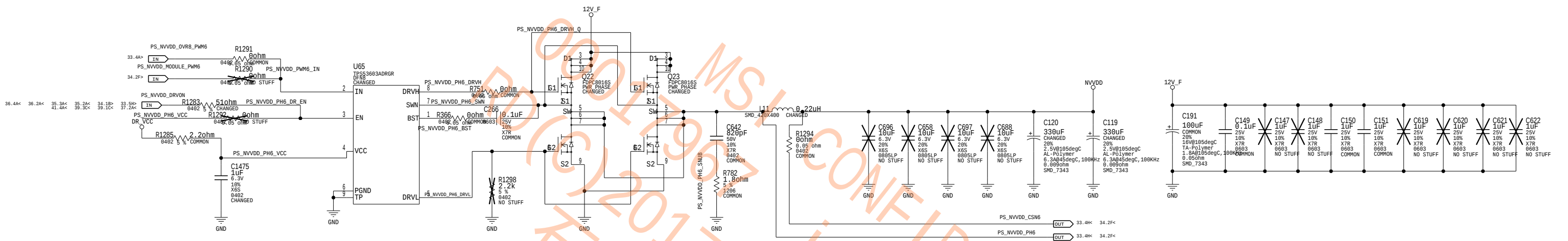
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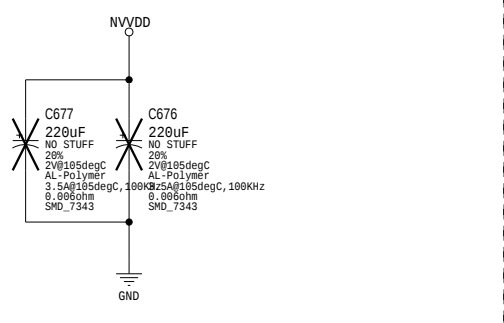
37 OF 49

DATE

15-FEB-2017



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ASSEMBLY	SKU50
PAGE DETAIL	PS: NVDD Phase 6, 7

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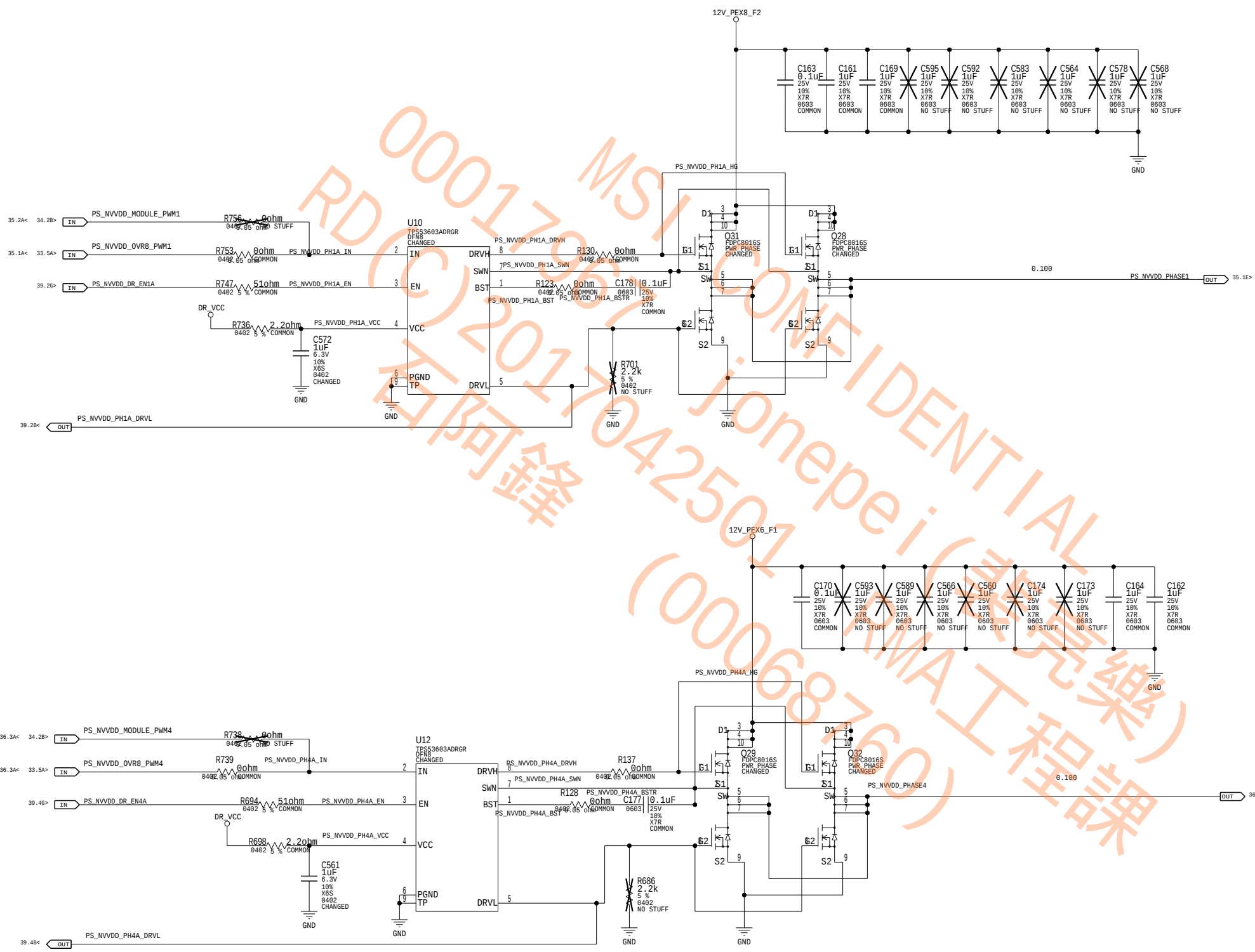
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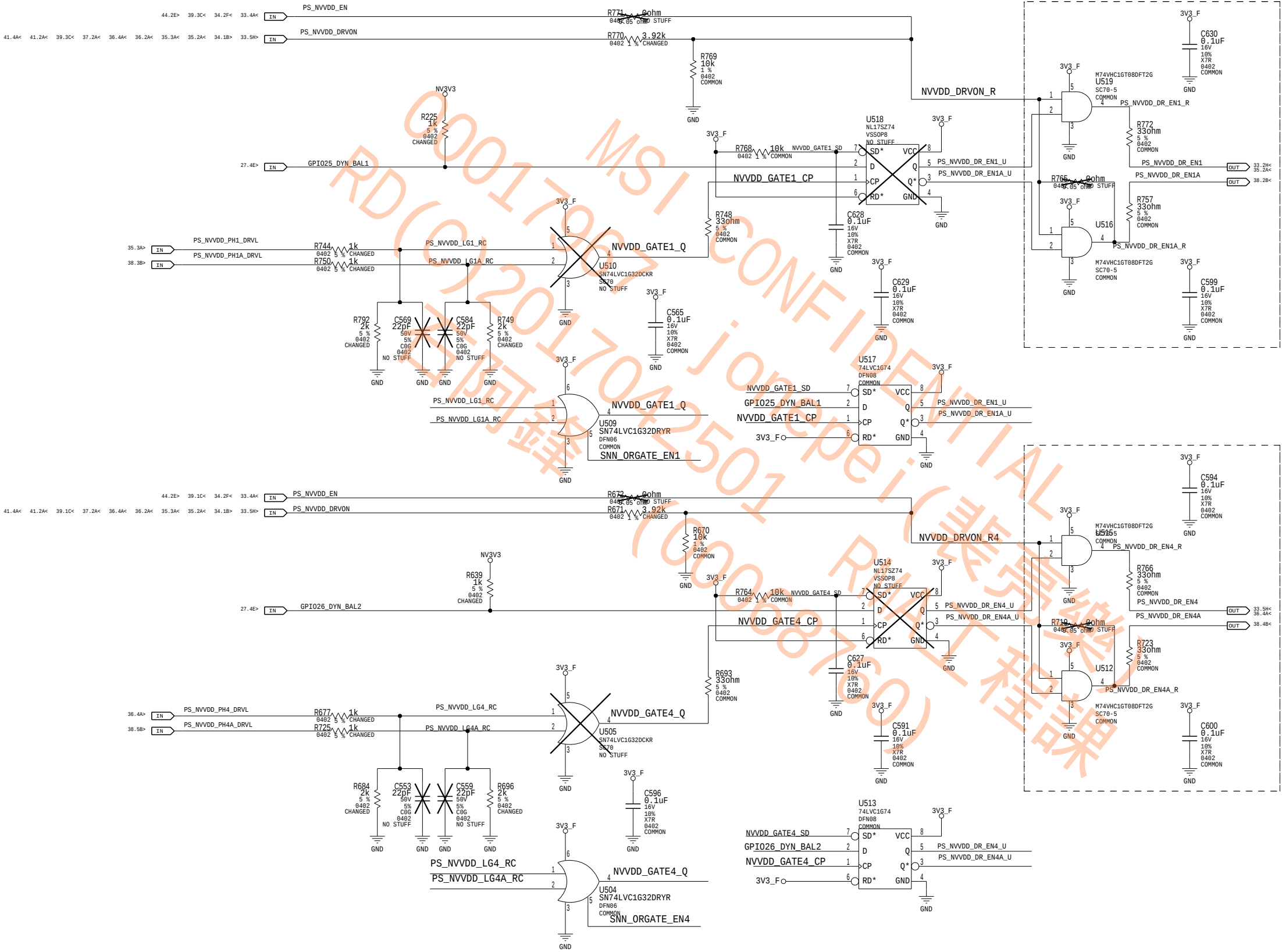
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PCB REV	PG611-A00	PAGE	38 OF 49
BOM REV	A	DATE	15-FEB-2017



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Page40: PS: Dynamic Power Balance Logic



ASSEMBLY		SKU50
PAGE DETAIL		PS: Dynamic power balance logic
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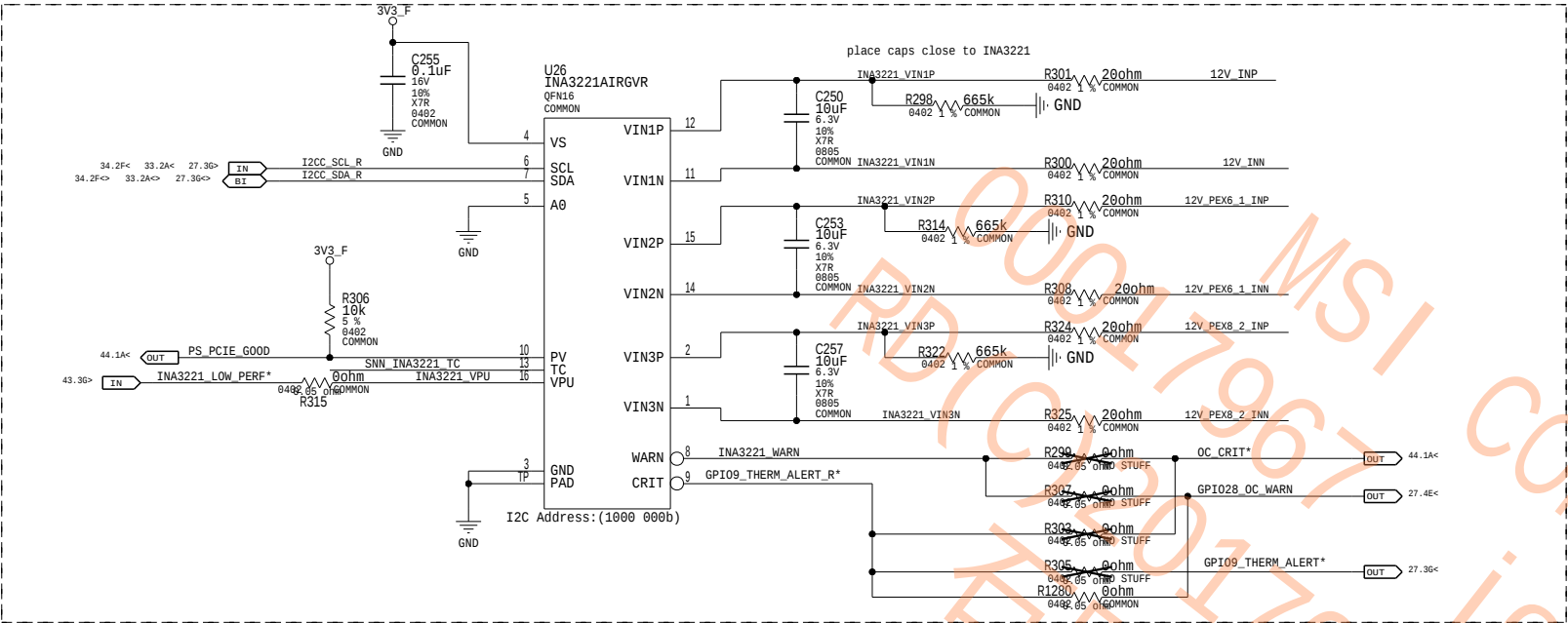
PAGE

40 OF 49

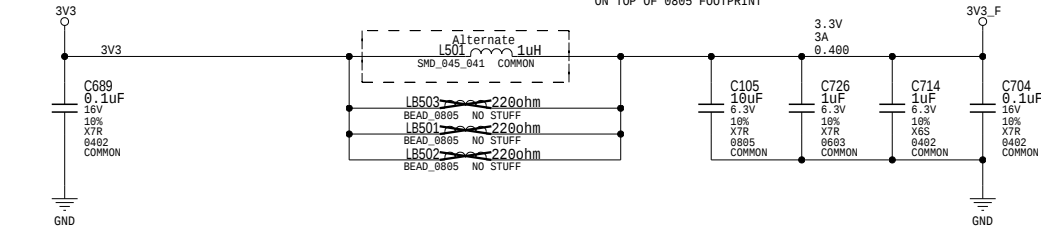
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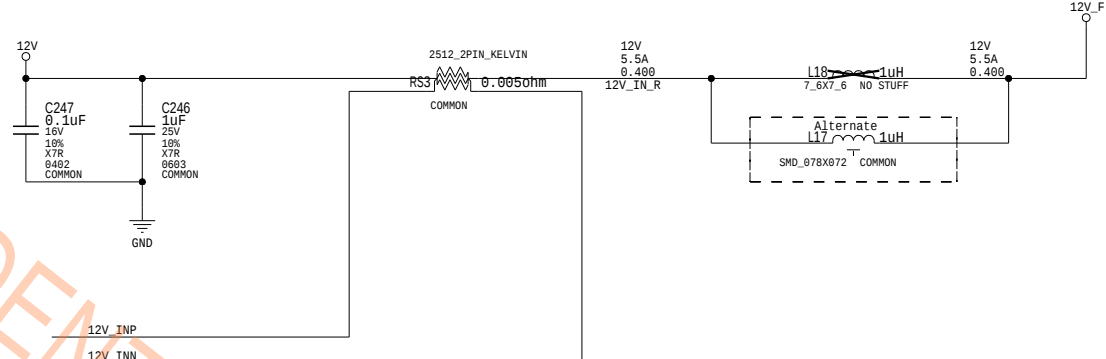
Page41: PS: Inputs, Filtering, and Monitoring



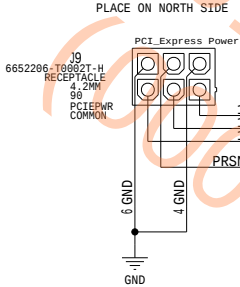
PEX 3V3 INPUT - 10W



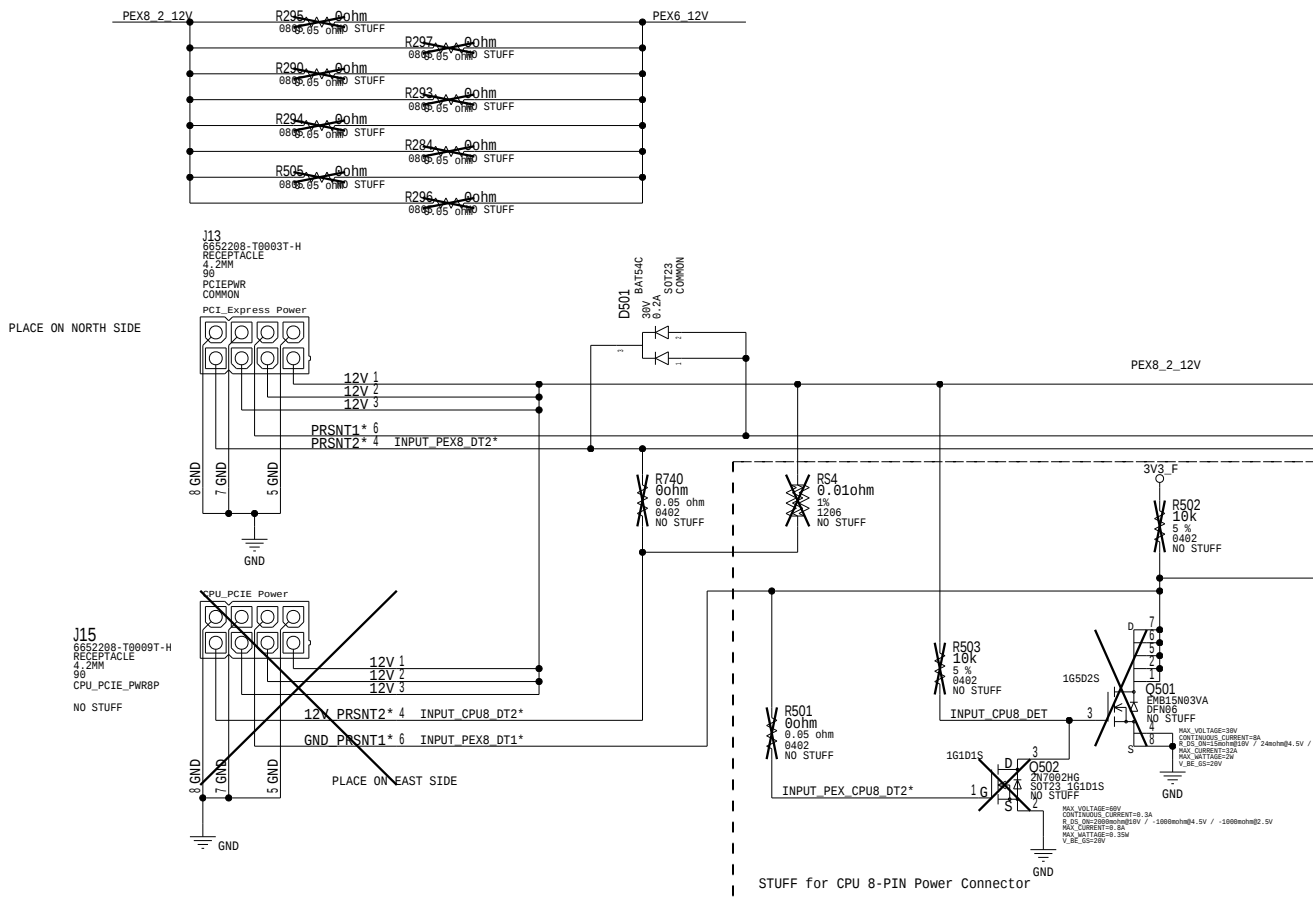
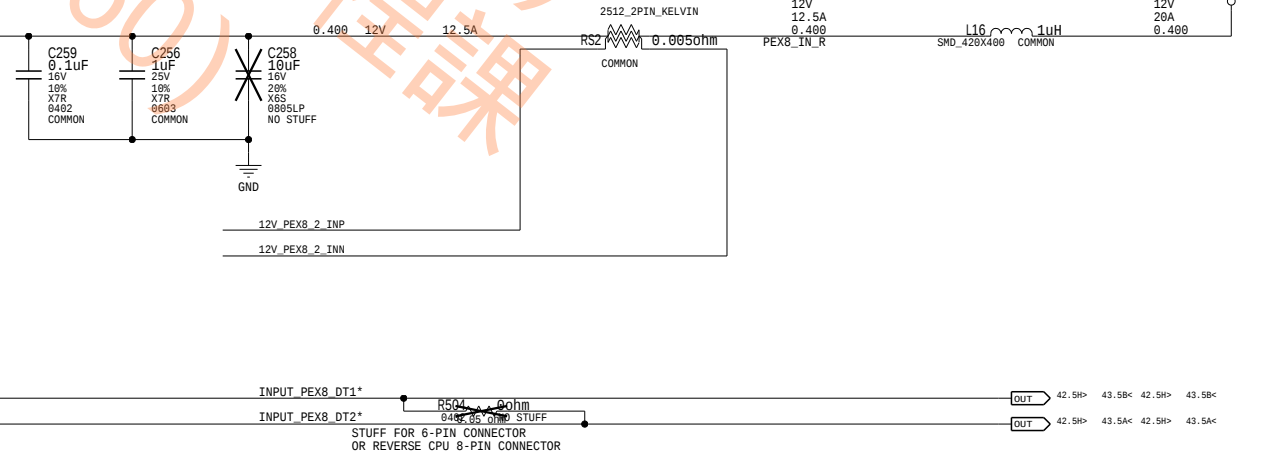
PEX_12V INPUT - 66W



PEX6 INPUT 1 - 2x3 PCIE CON 75W



PEX8 INPUT 2 - 2x4 PCIE CON 150W



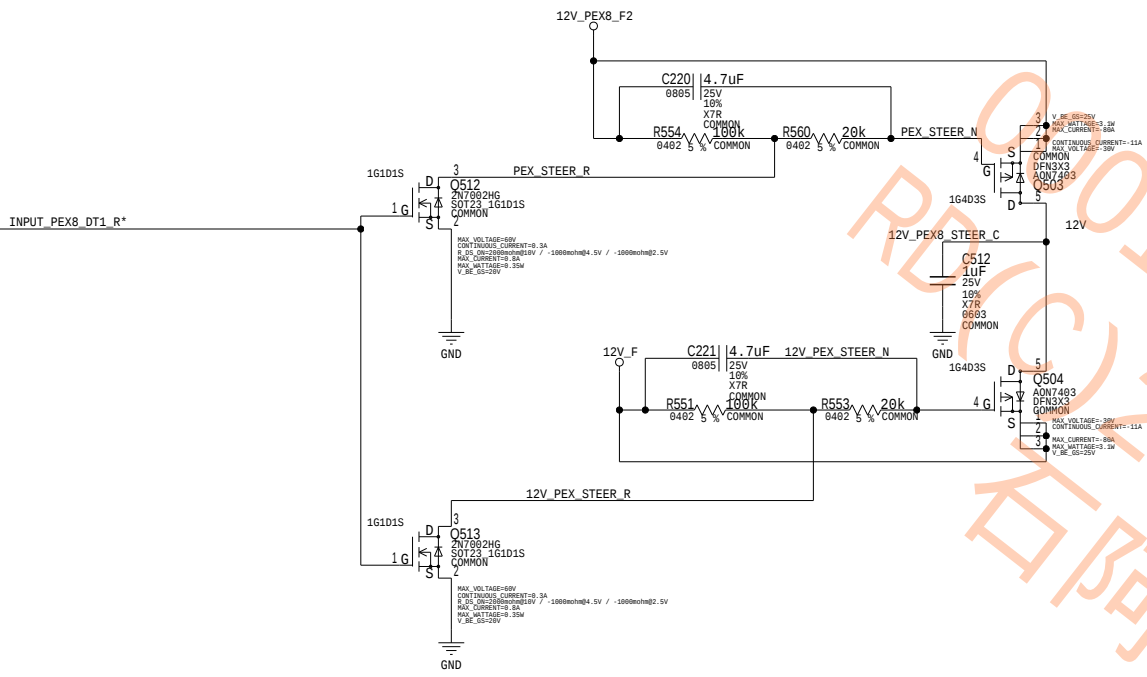
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NV_PN	600-16611-0050-QS1		
PCB REV	P6611-A00	PAGE	41 OF 49
BOM REV	A	DATE	15-FEB-2017

Page42: PS: 12V Current Steering & Hot Unplug Detect

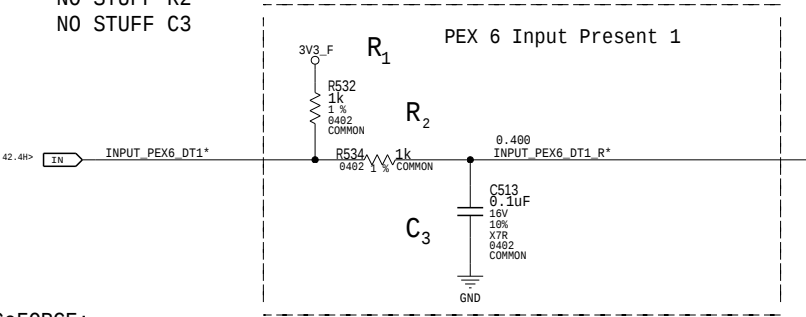
QUADRO/TESLA:
12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

For OpenVreg Type4 + Phase Doubler, 2 phase PSI mode



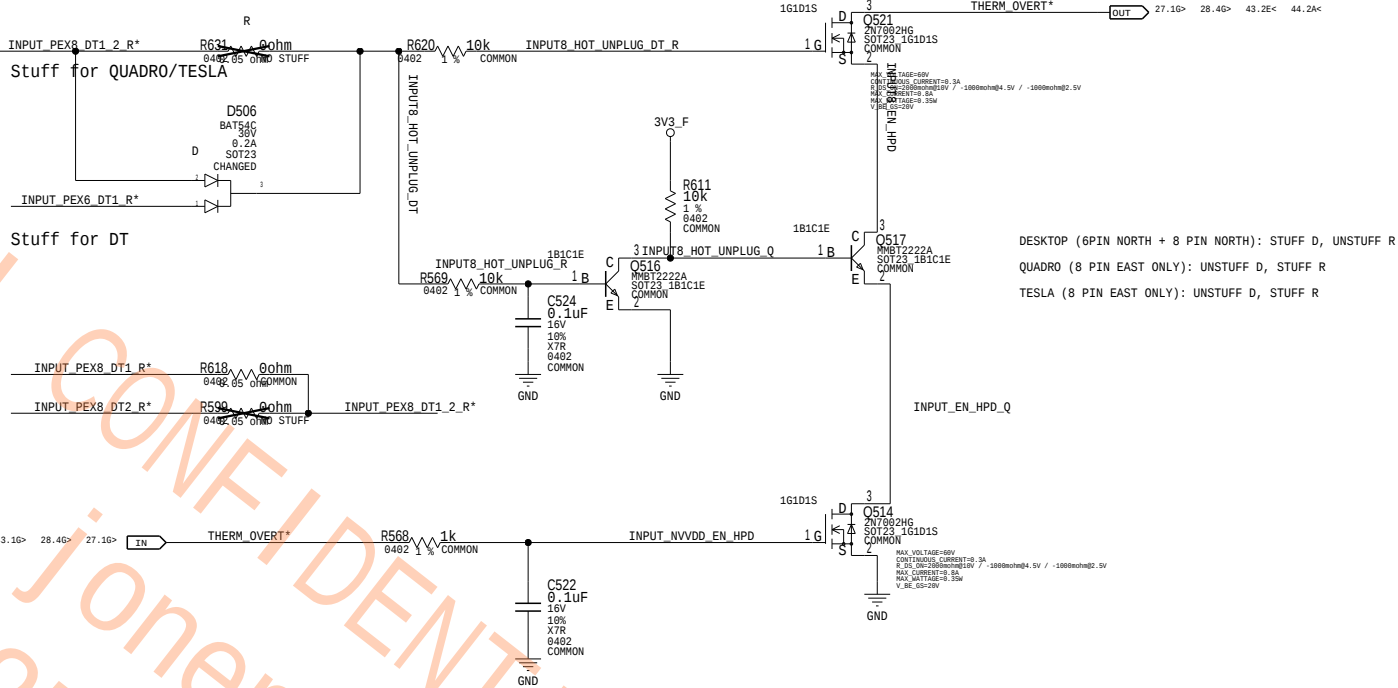
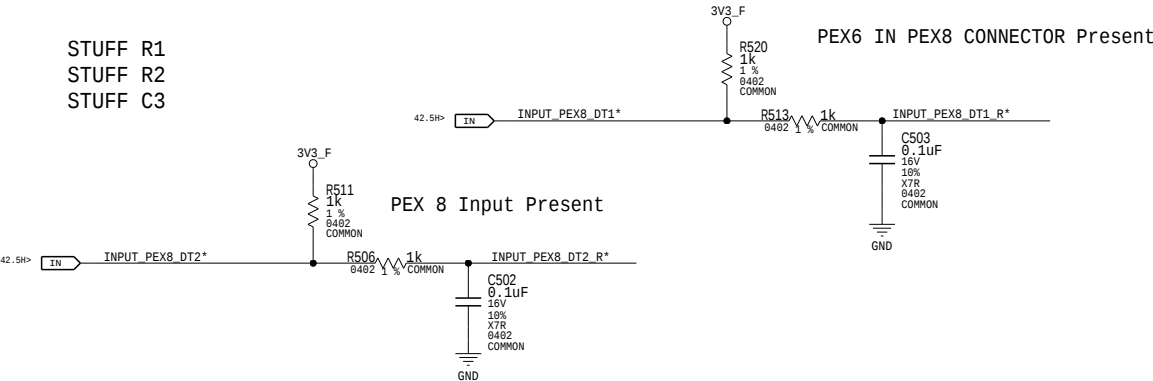
PEX 6 INPUT CONNECTOR IS NOT LOADED
PEX 6 INPUT DETECT MUST BE DISABLED
PEX 8 INPUT DETECT MUST BE USED TO CONTROL STEERING

NO STUFF R1
NO STUFF R2
NO STUFF C3



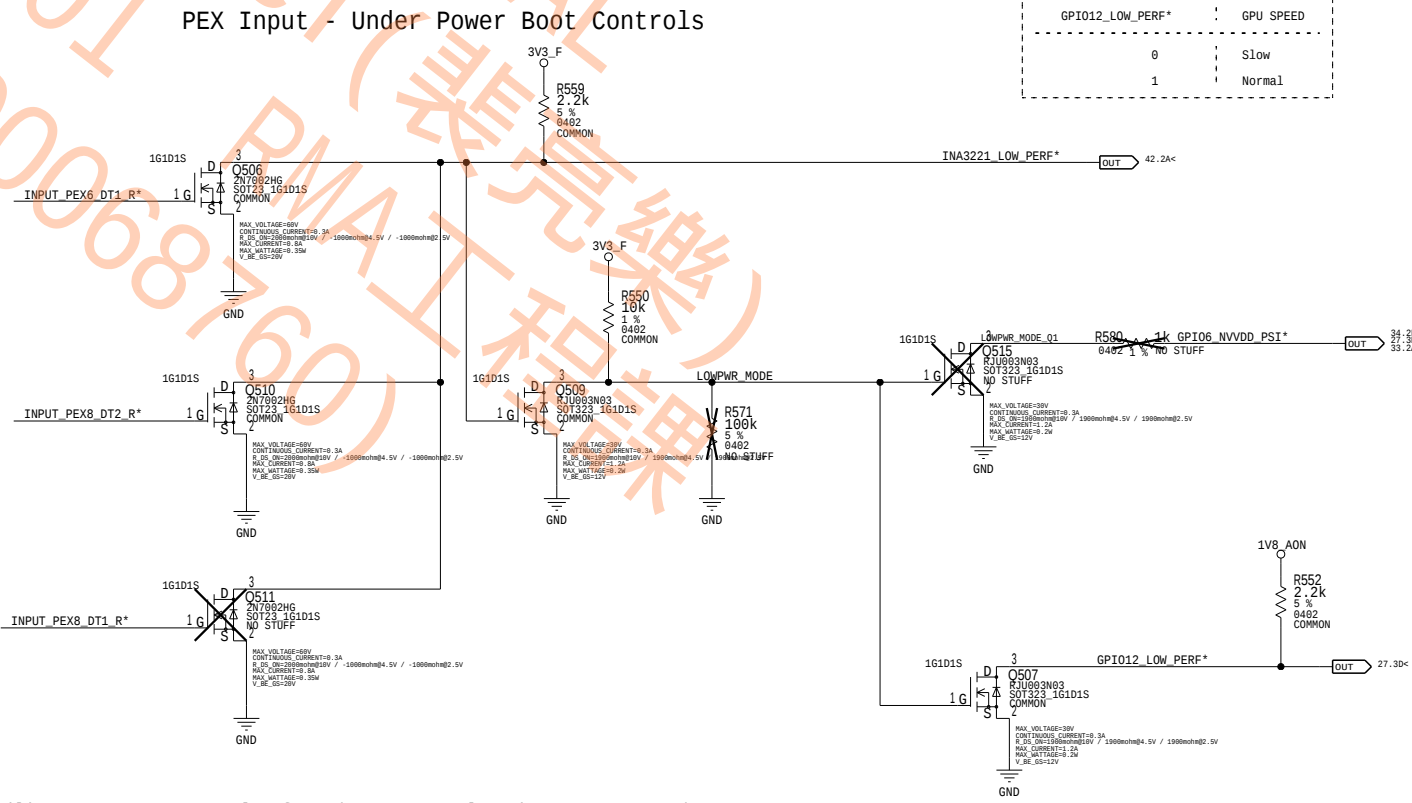
GeFORCE:
PEX 6 INPUT CONNECTOR IS LOADED
PEX 6 INPUT DETECT MUST BE USED TO CONTROL STEERING

STUFF R1
STUFF R2
STUFF C3



DESKTOP (6PIN NORTH + 8 PIN NORTH): STUFF D, UNSTUFF R
QUADRO (8 PIN EAST ONLY): UNSTUFF D, STUFF R
TESLA (8 PIN EAST ONLY): UNSTUFF D, STUFF R

PEX Input - Under Power Boot Controls



A 2 x 4 auxiliary power connector plug from the power supply unit must not use the 75 W sense coding (Sense1=Open and Sense0=Ground) to avoid end-user confusion.

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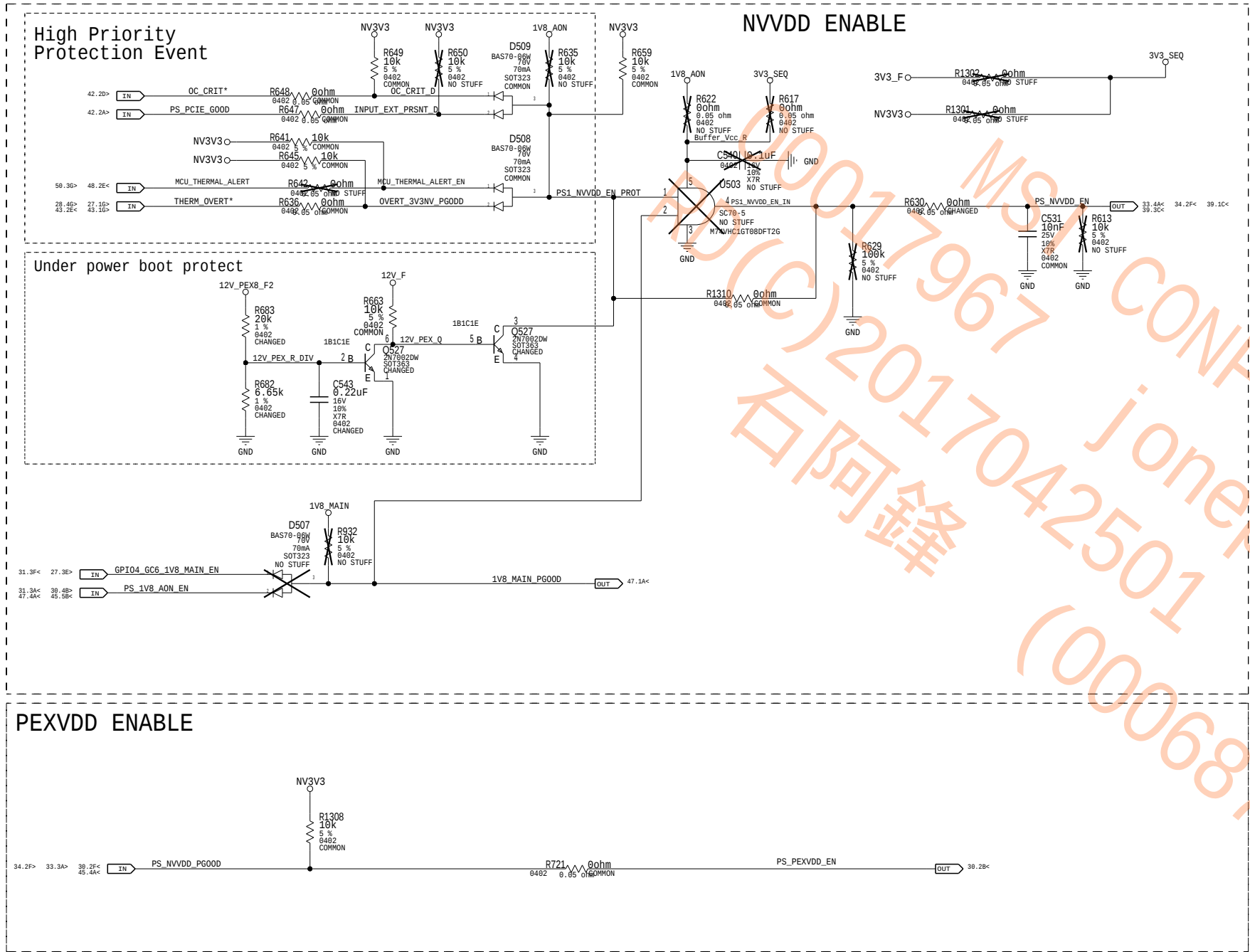


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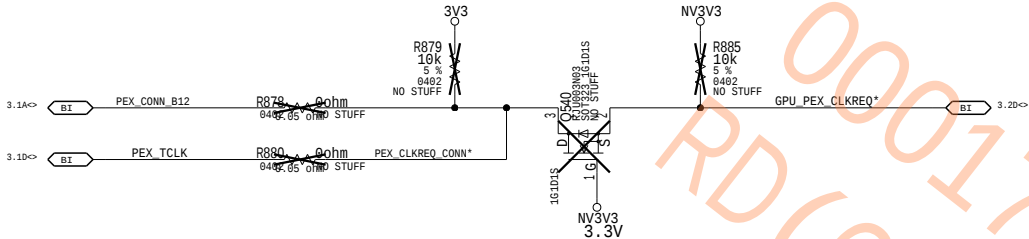
PAGE 42 OF 49
DATE 15-FEB-2017

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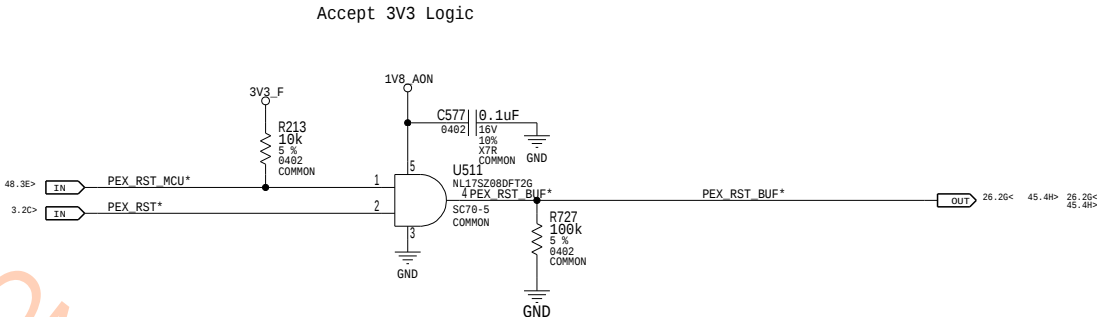


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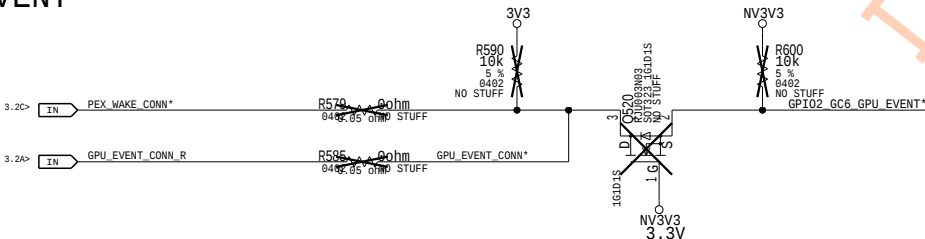
PEX_CLKREQ*



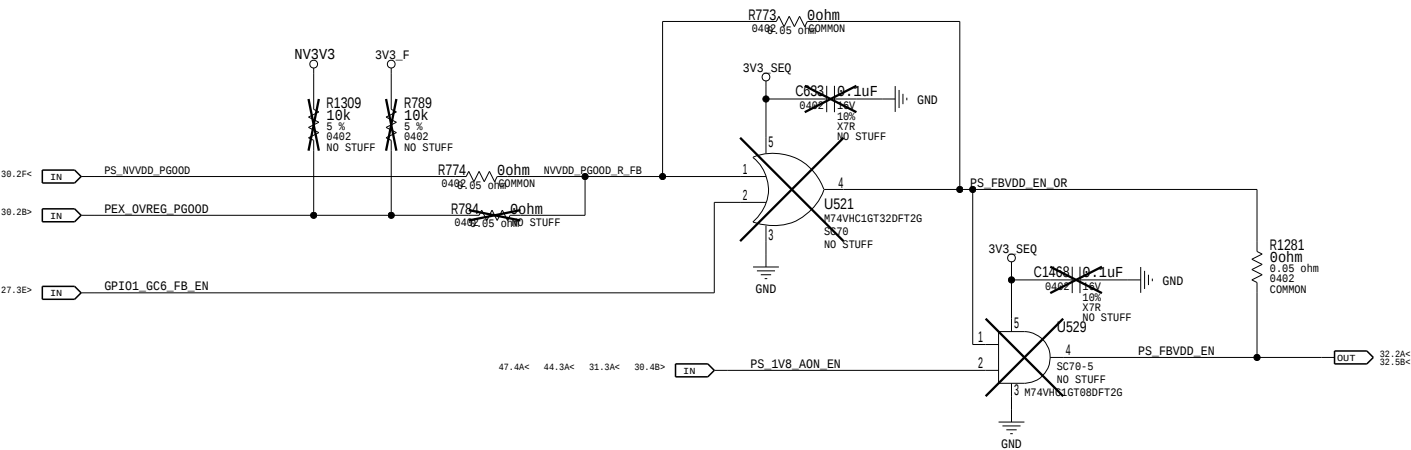
PEX_RST# LOGIC



GPU_EVENT*



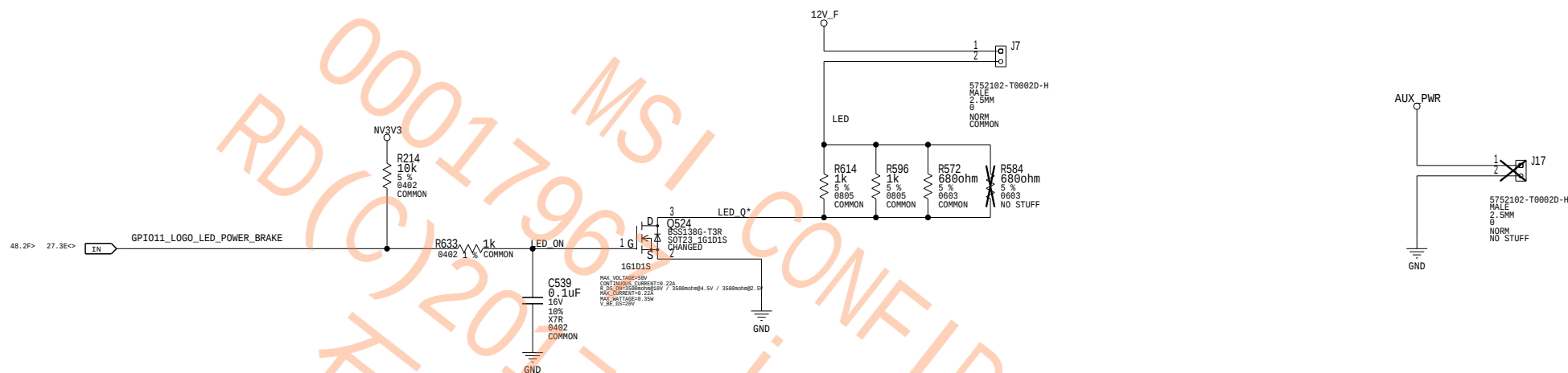
FBVDD/Q ENABLE



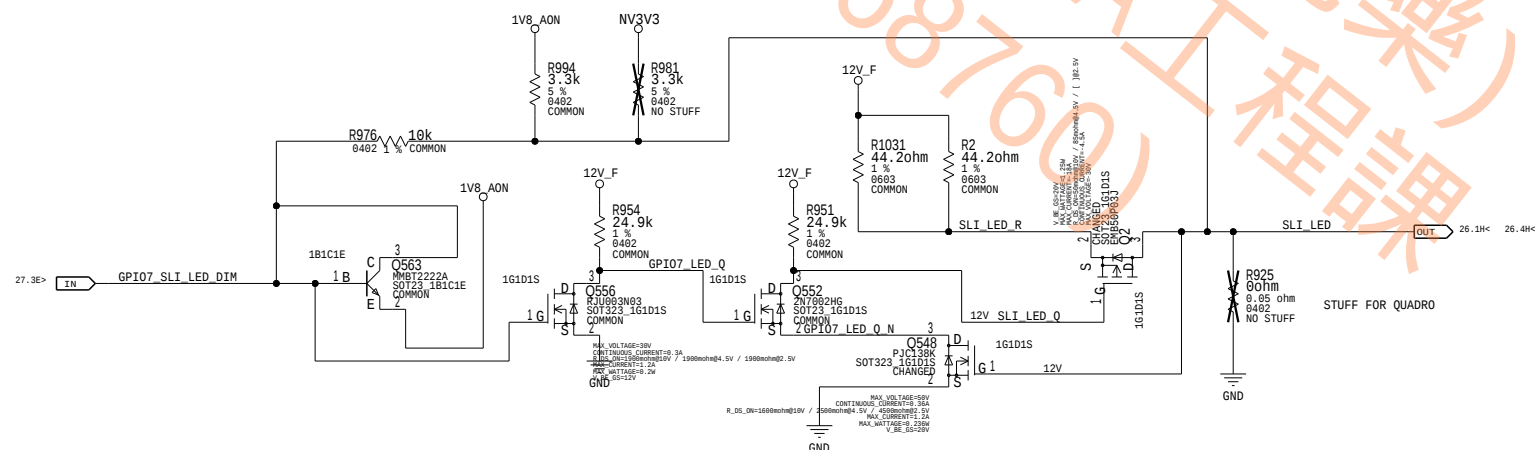
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NV_PN	600-1G611-0050-QS1		
PCB REV	PG611-A00	PAGE	44 OF 49
BOM REV	A	DATE	15-FEB-2017

LED HEADER(GEFORCE ONLY)



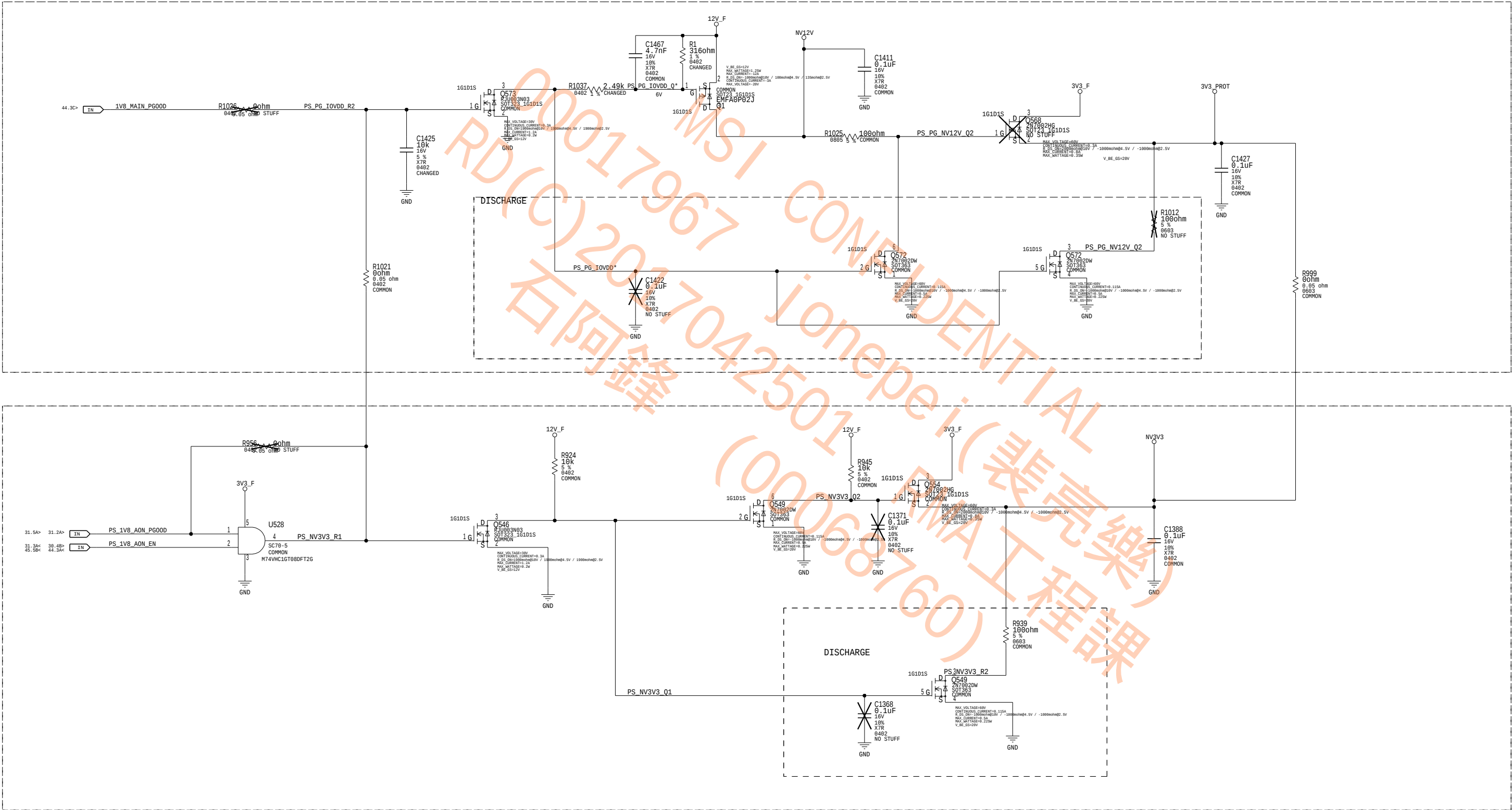
SLI LED (GEFORCE ONLY)



ASSEMBLY	SKU50
PAGE DETAIL	GEFORCE LED AND SLI LED

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NV_PN	600-1G611-0050-QS1			
PCB REV	PG611-A00	PAGE	45 OF 49	
BOM REV	A	DATE	15-FEB-2017	



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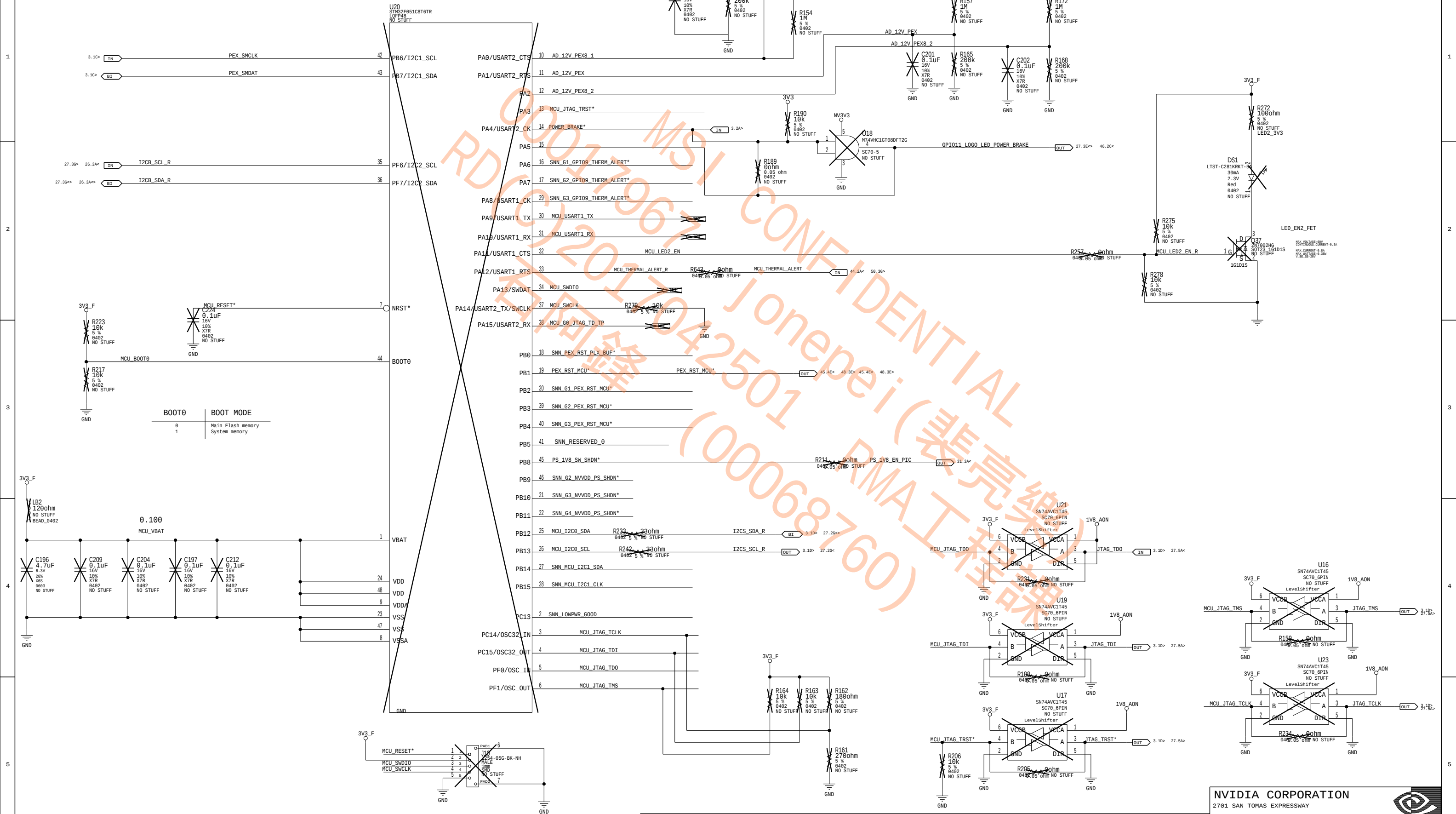
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46 OF 49

DATE

15-FEB-2017

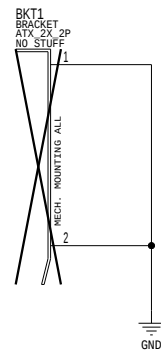
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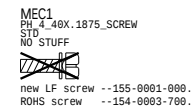
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NV_PN	600-1G611-0050-QS1		
PCB REV	P6111-A00	PAGE	47 OF 49
BOM REV	A	DATE	15-FEB-2017

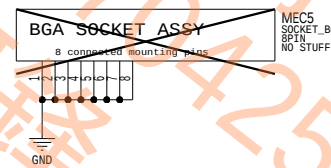
Brackets:



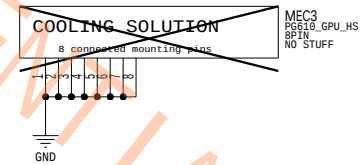
Bracket Screw



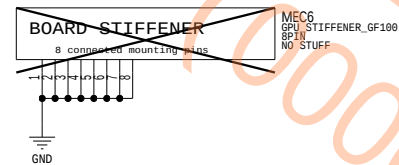
GPU SOCKET



GPU HEATLINK



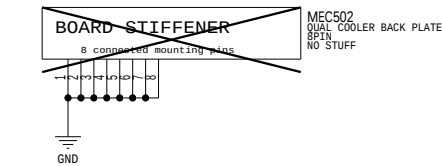
GPU Stiffener (BRING-UP COOLER)



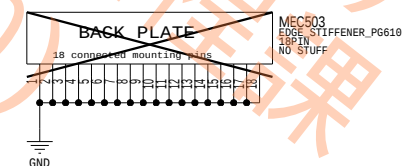
STIFFENER



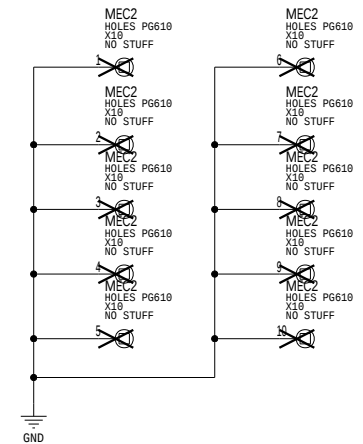
QUAL COOLER STIFFENER



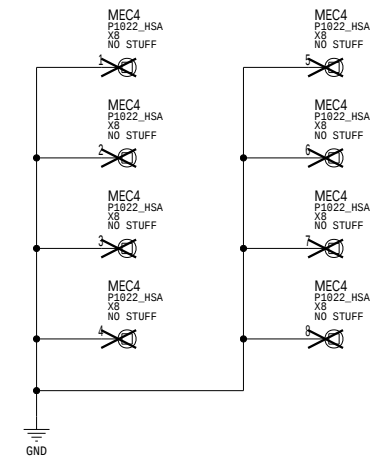
BOARD BACK PLATE



Mechanical Holes Symbol



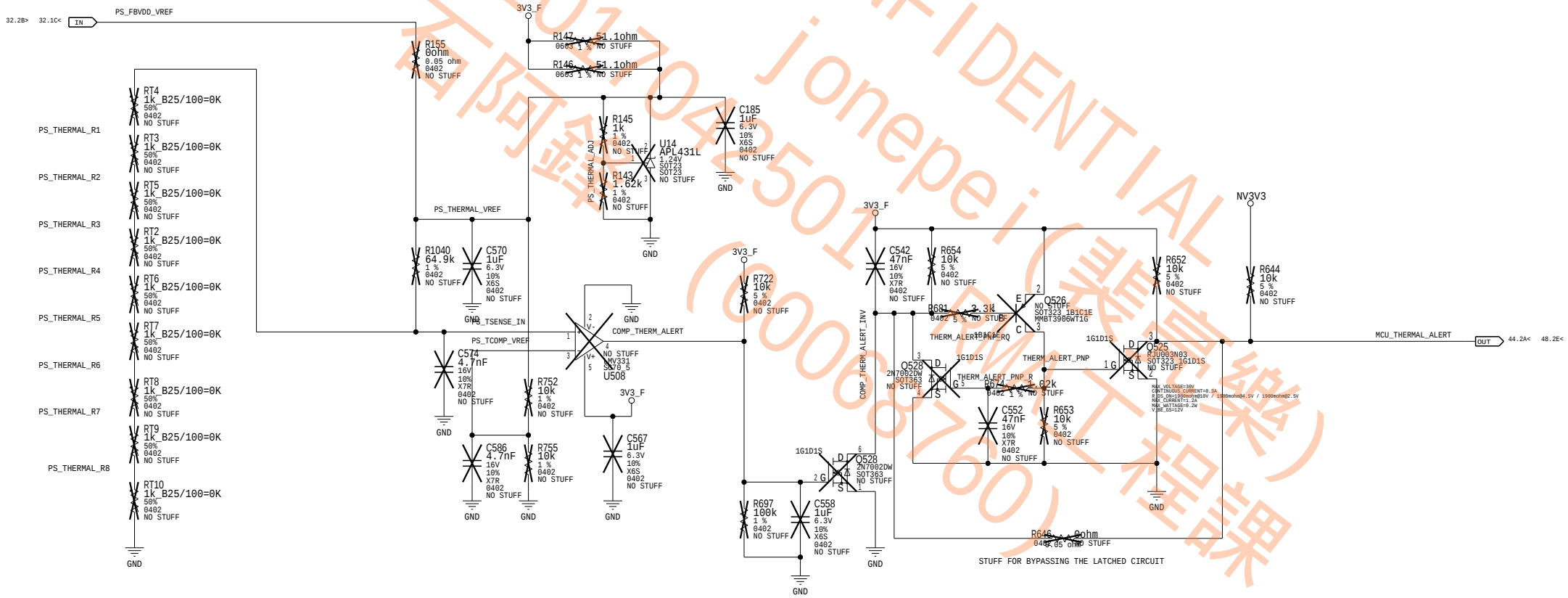
GPU HOLES SYMBOL



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PAGE DETAIL	MECH

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NV_PN		600-1G611-0050-QS1		
PCB REV		P611-A00		PAGE
BOM REV		A		48 OF 49
		DATE		15-FEB-2017



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