PG166-A02

TU116,192b GDDR6 2CHx16,90W/120W
DVI-D DL + HDMI + DP

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
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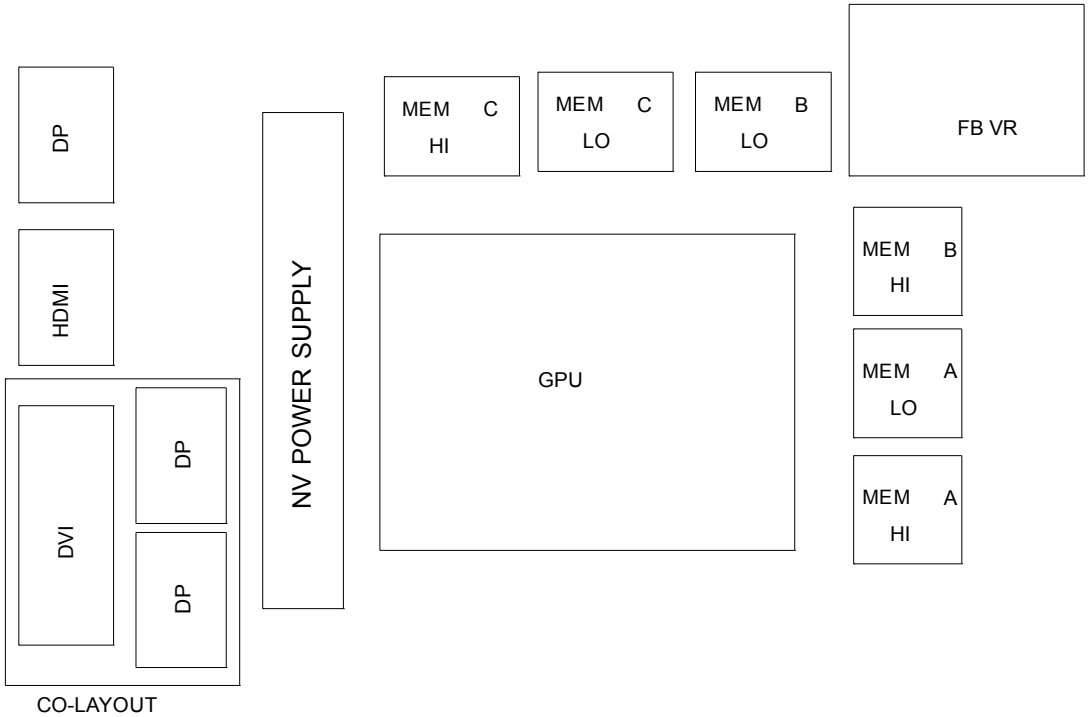
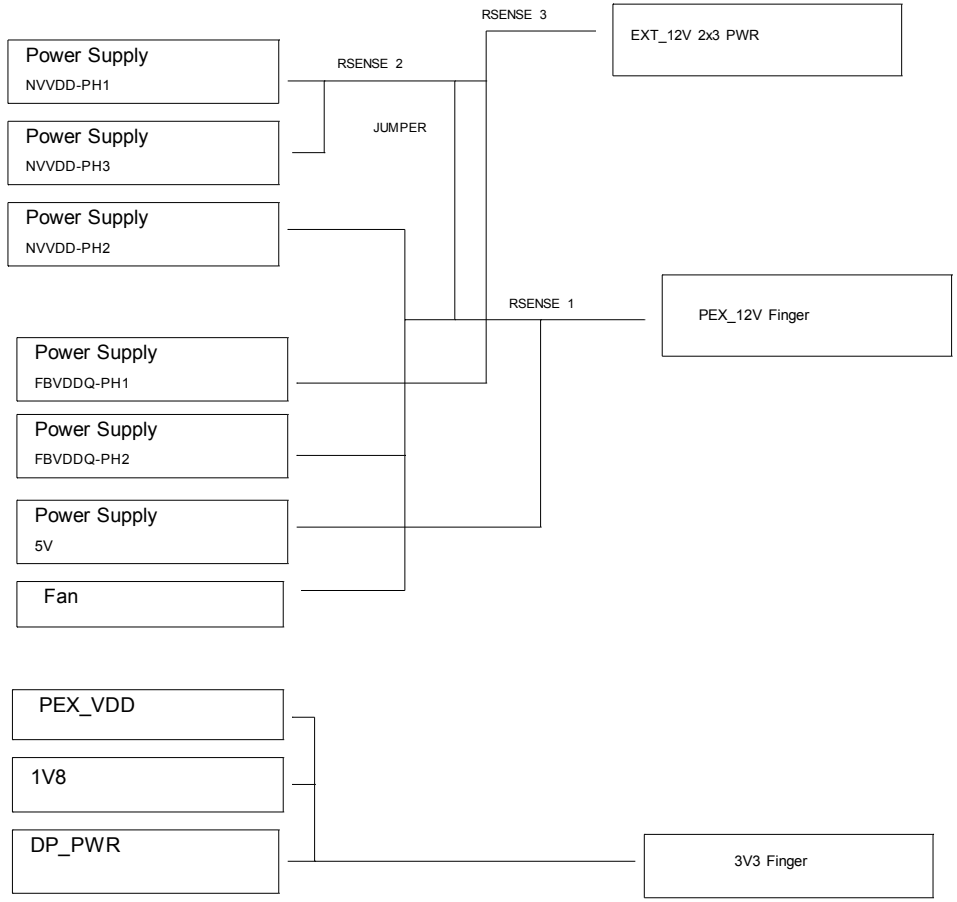
Page2: Block Diagram



Power Supply:

NVVDD = RSENSE 2 * 3/2
FBVDD = (RSENSE 3-RSENSE 2)
TGP = RSENSE 1 + RSENSE 3



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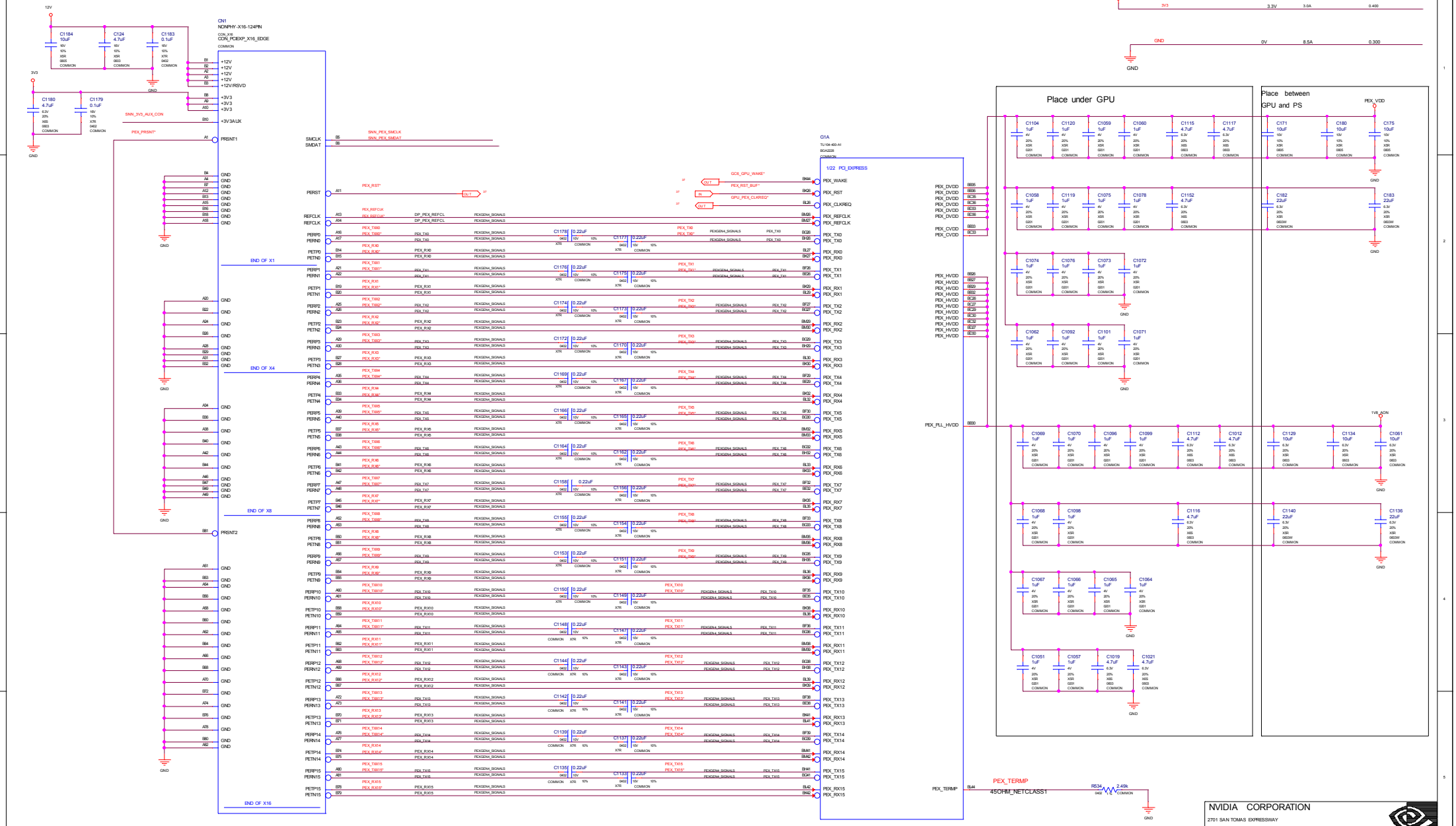
Page3: PCI Express



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PAGE DETAIL	PCI Express

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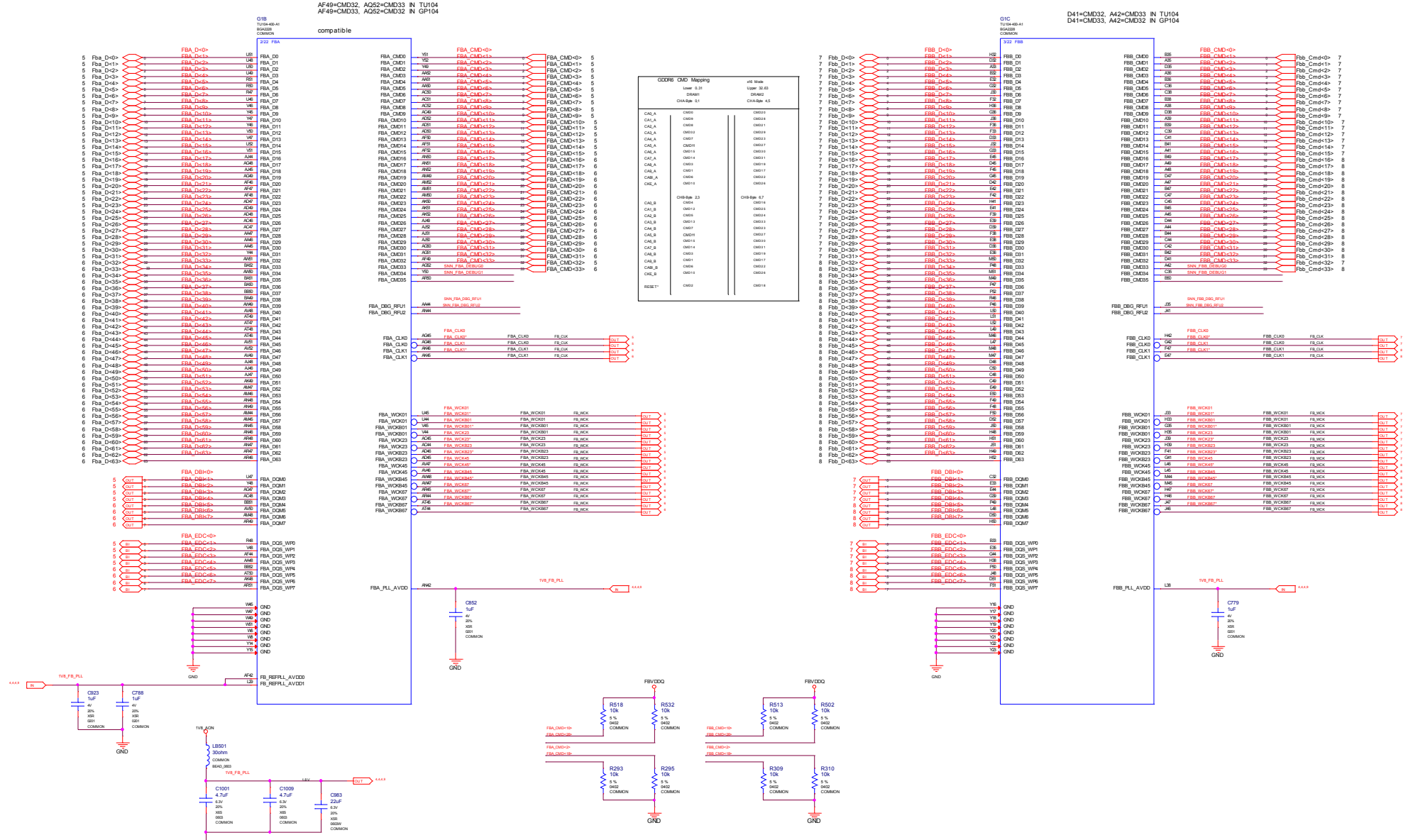
Page4: MEMORY: GPU Partition A/B



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PAGE DETAIL	MEMORY: GPU FB_AB

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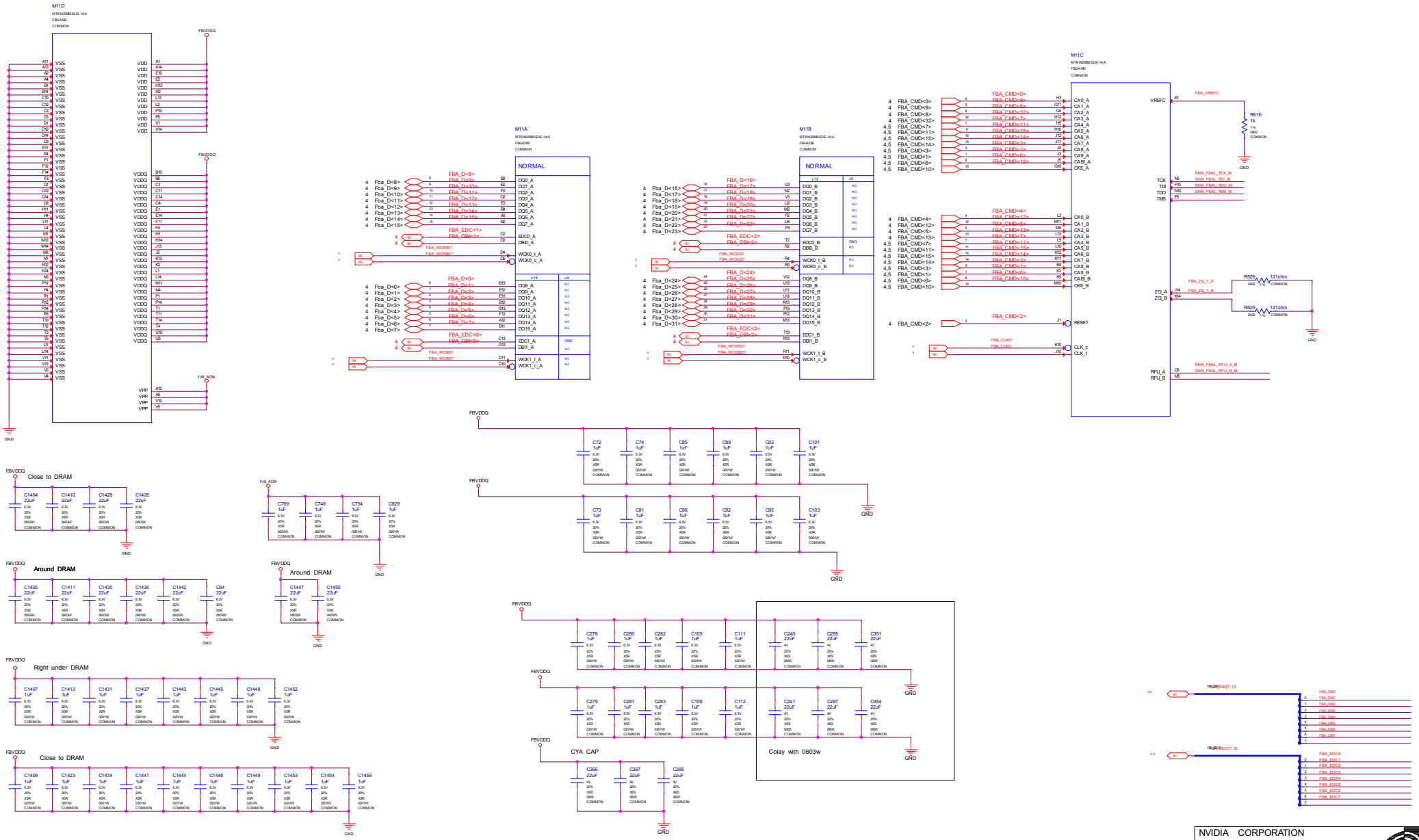
Page5: MEMORY: FBA Partition 31..0



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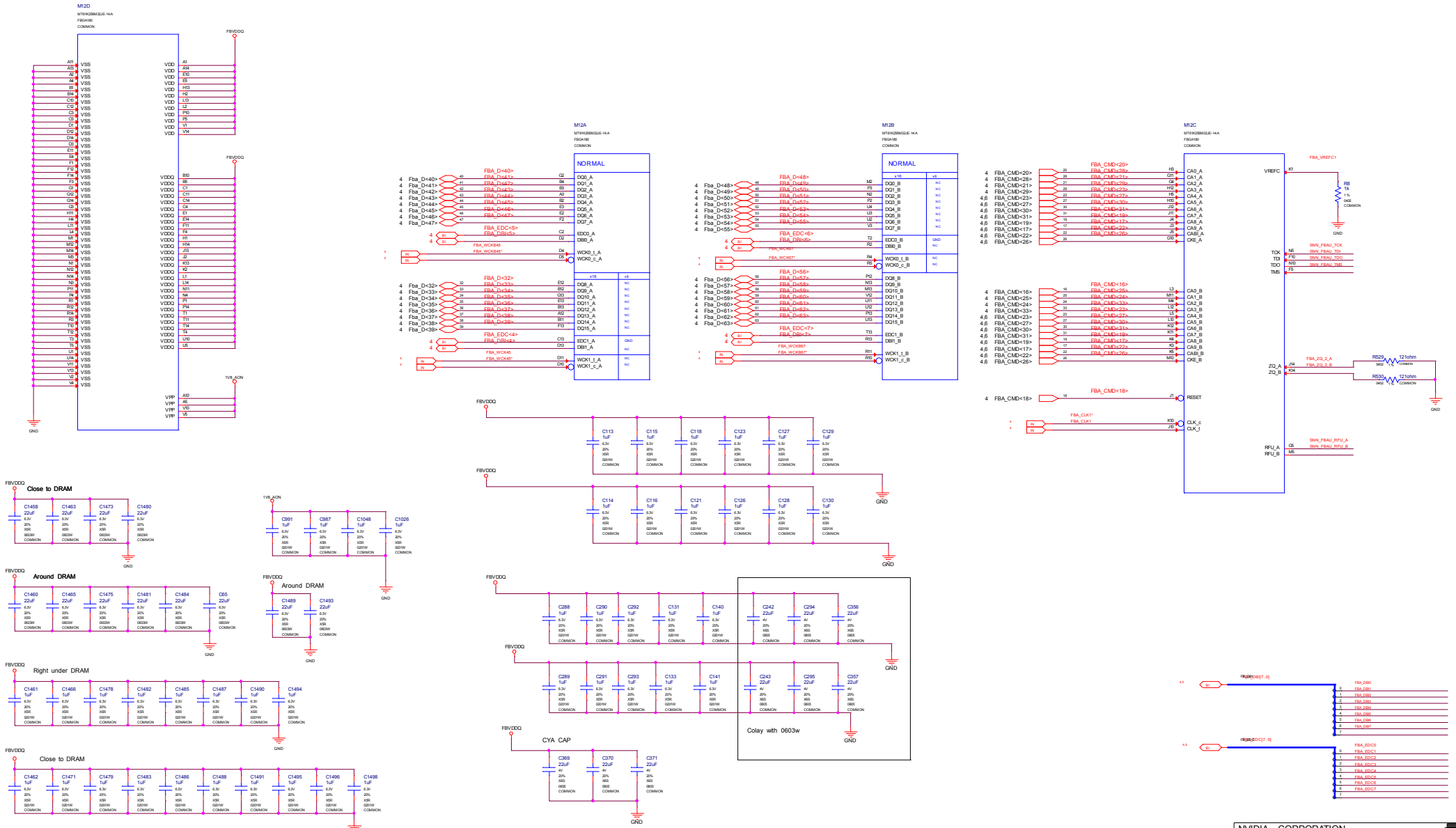
Page6: MEMORY: FBA Partition 63..32



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PAGE DETAIL	MEMORY: FBA[63:32]

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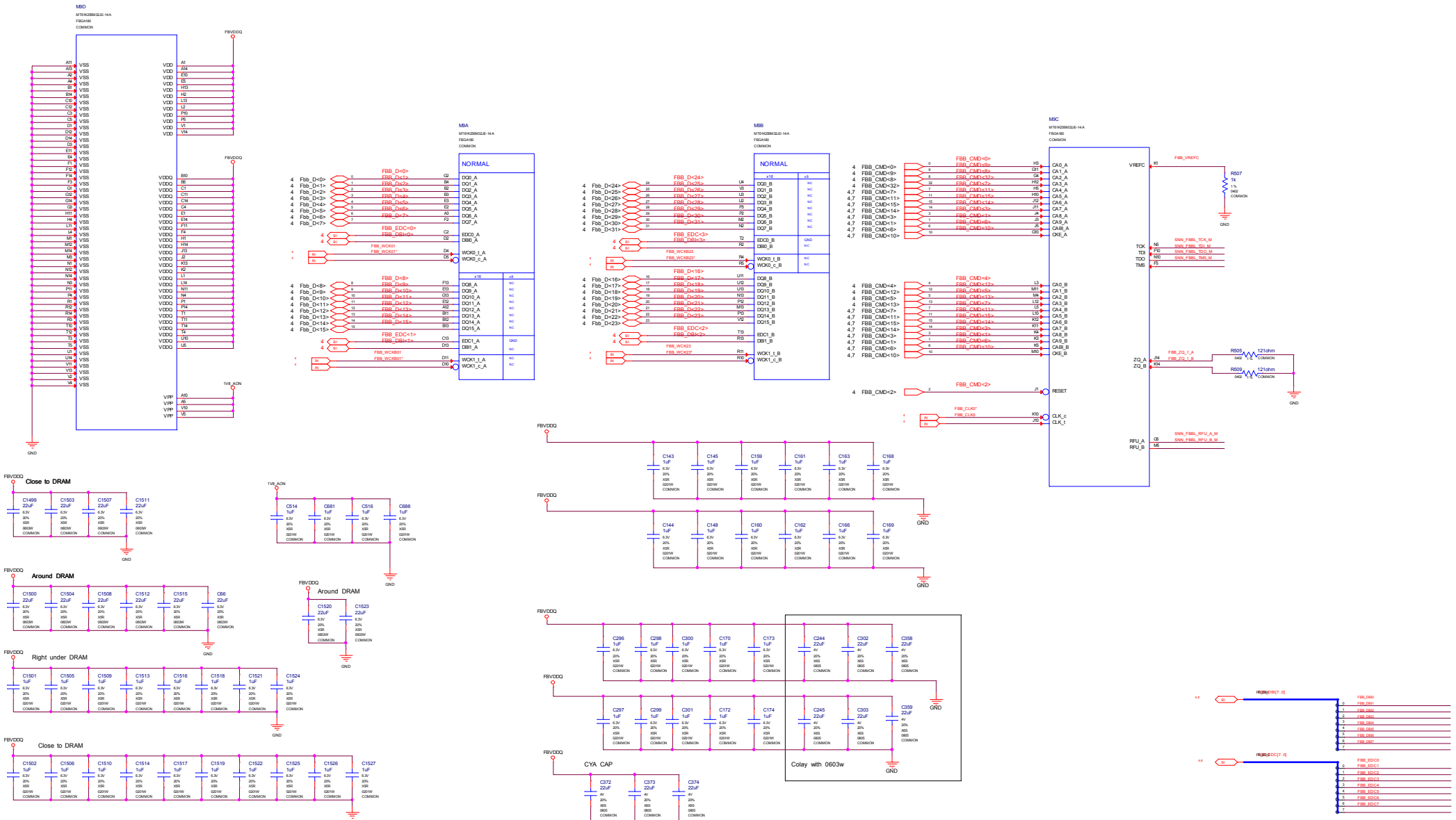
Page7: MEMORY: FBB Partition 31..0



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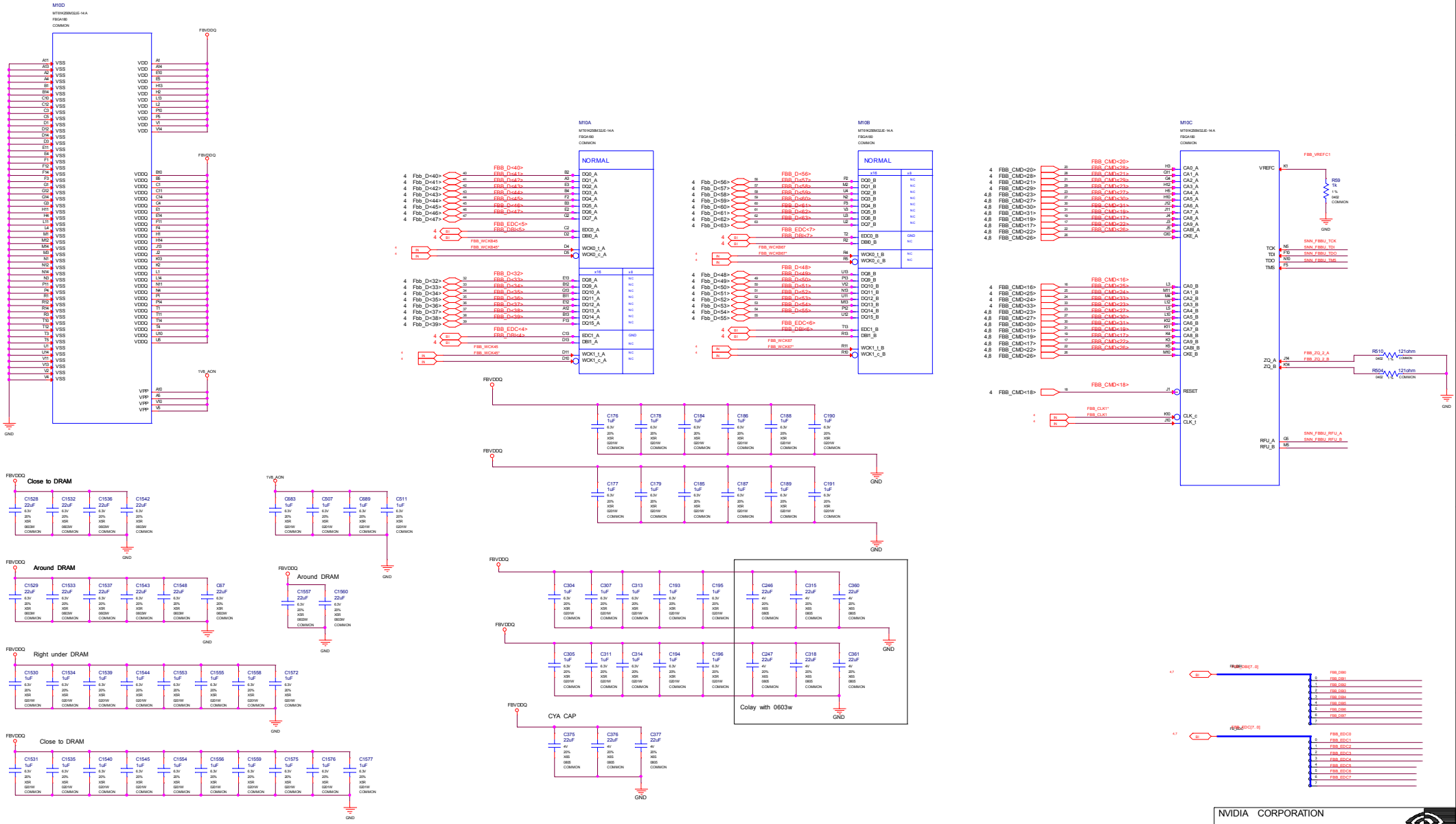
Page8: MEMORY: FBB Partition 63..32



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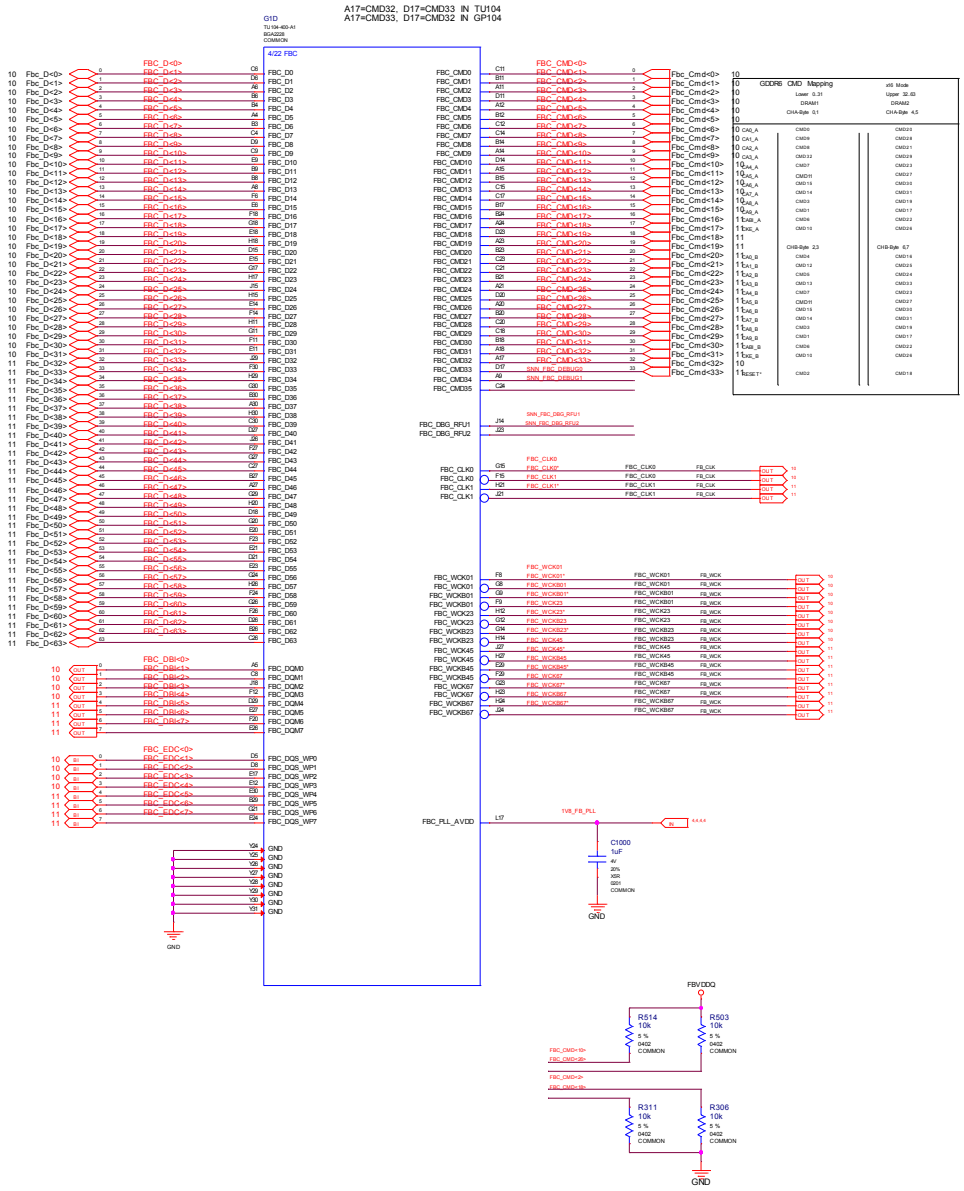
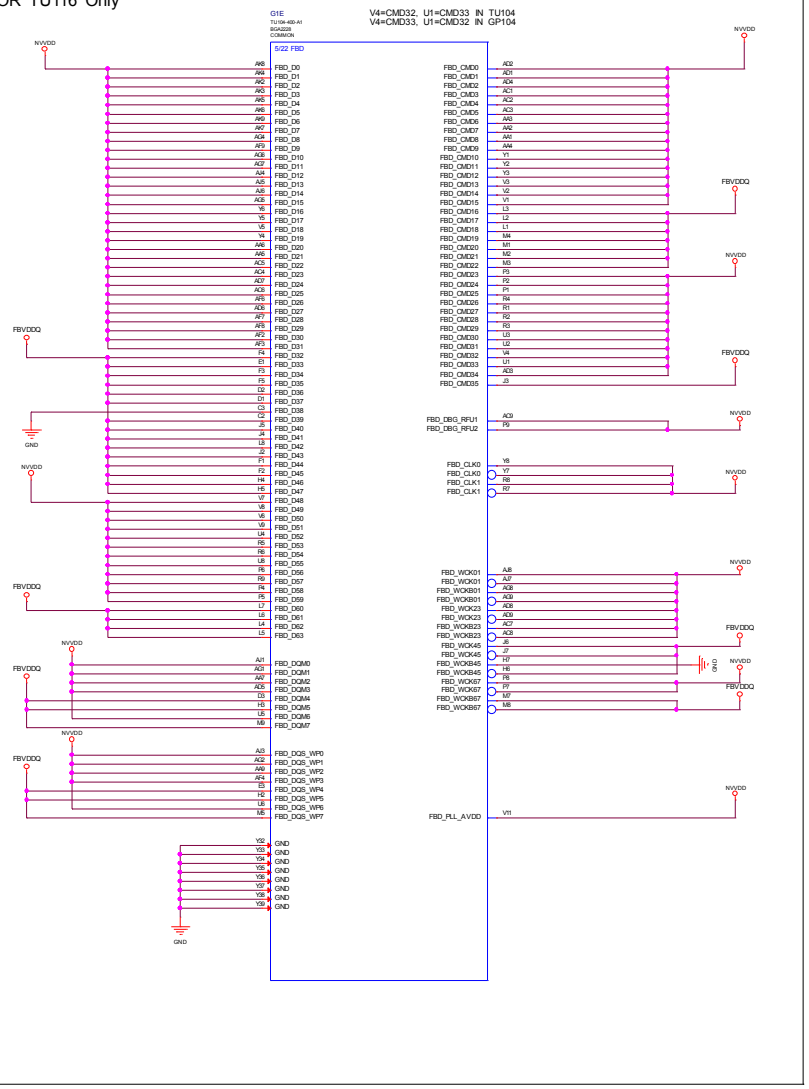
Page9: MEMORY: GPU Partition C/D



Use NC pin to Improve NVVDD,FBVDDQ,1V8 PDN
FOR TU116 Only



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PAGE DETAIL	MEMORY: GPU FB_CD

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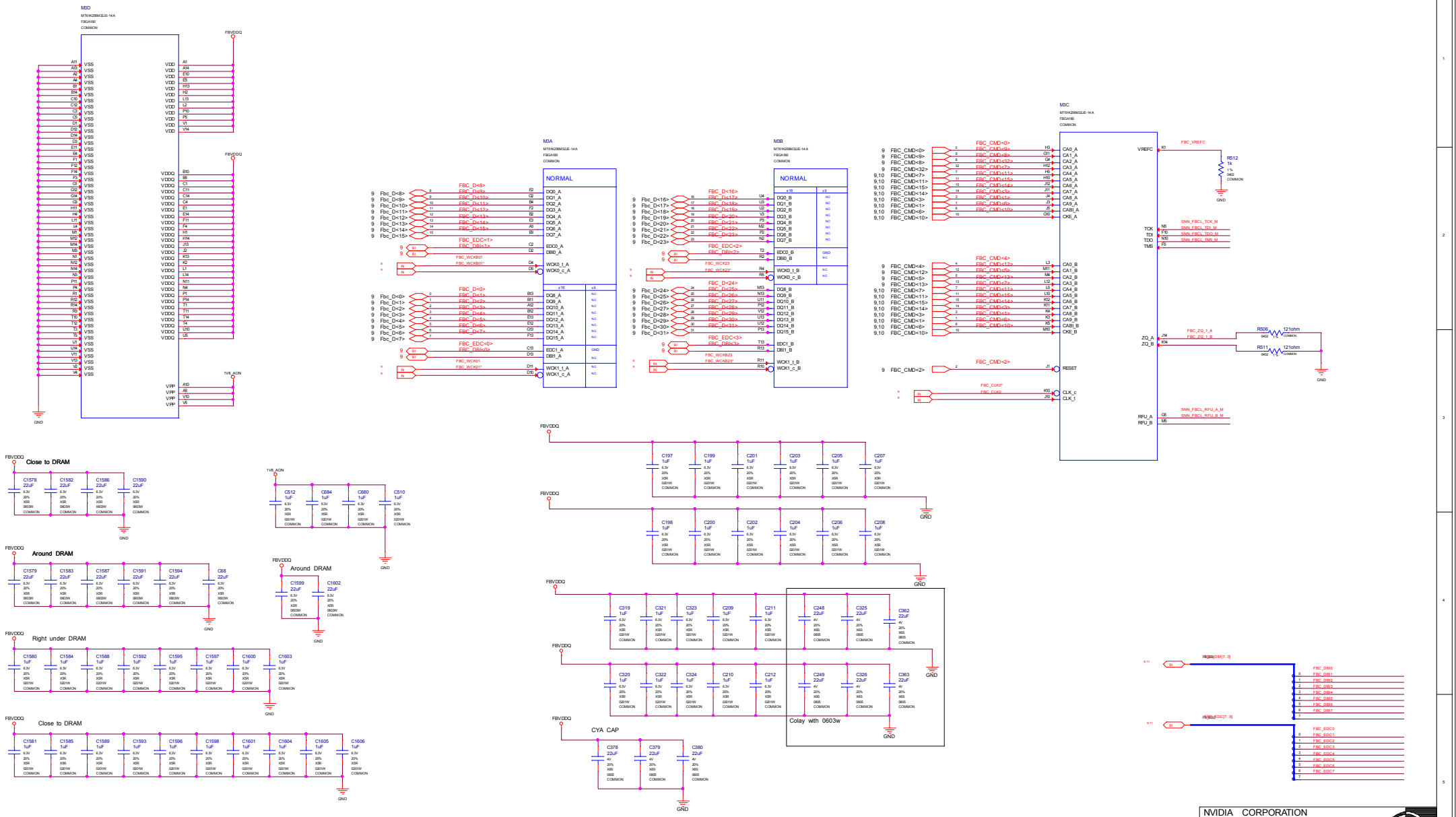
Page10: MEMORY: FBC Partition 31..0



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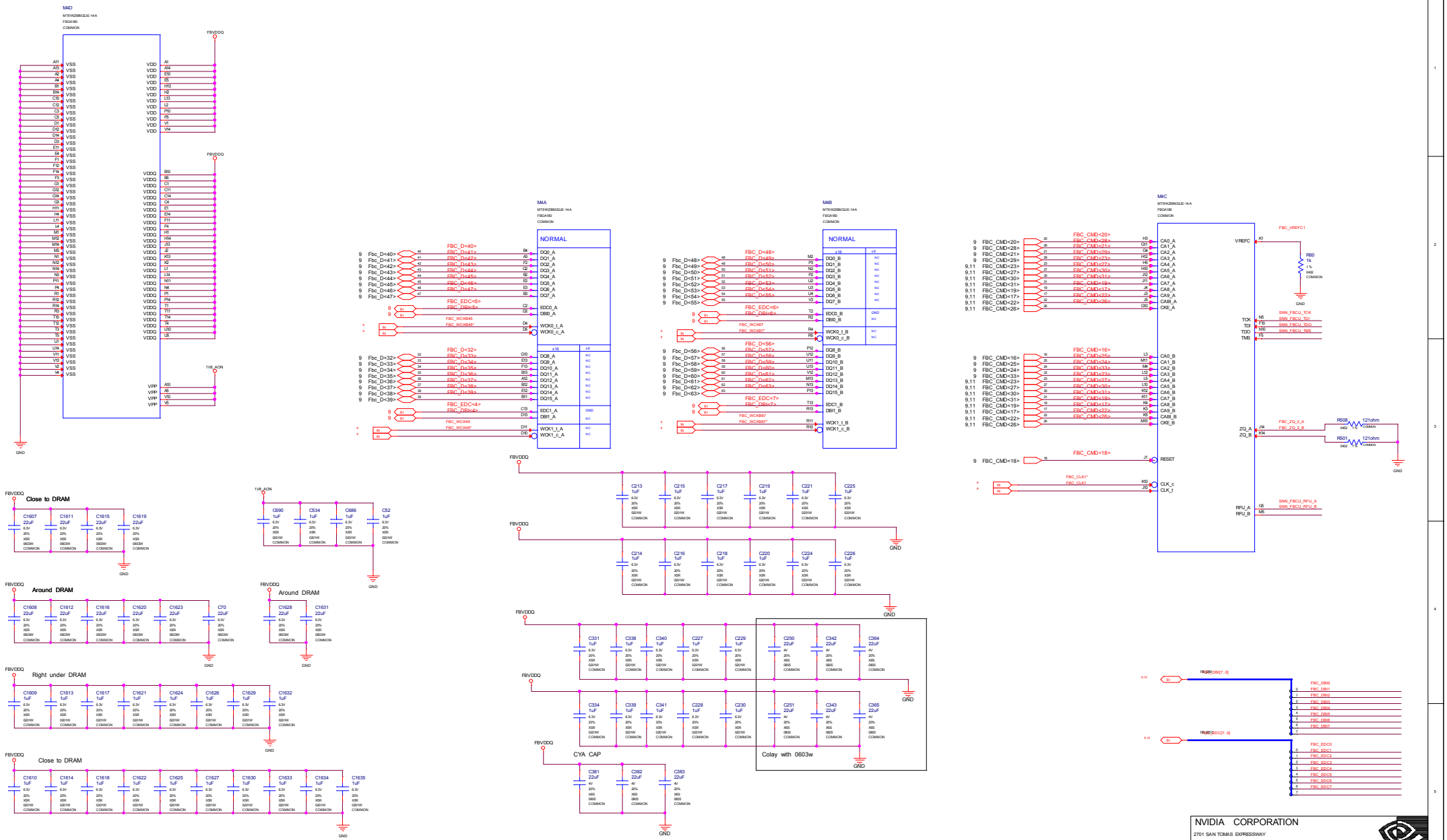
Page11: MEMORY: FBC Partition 63..32



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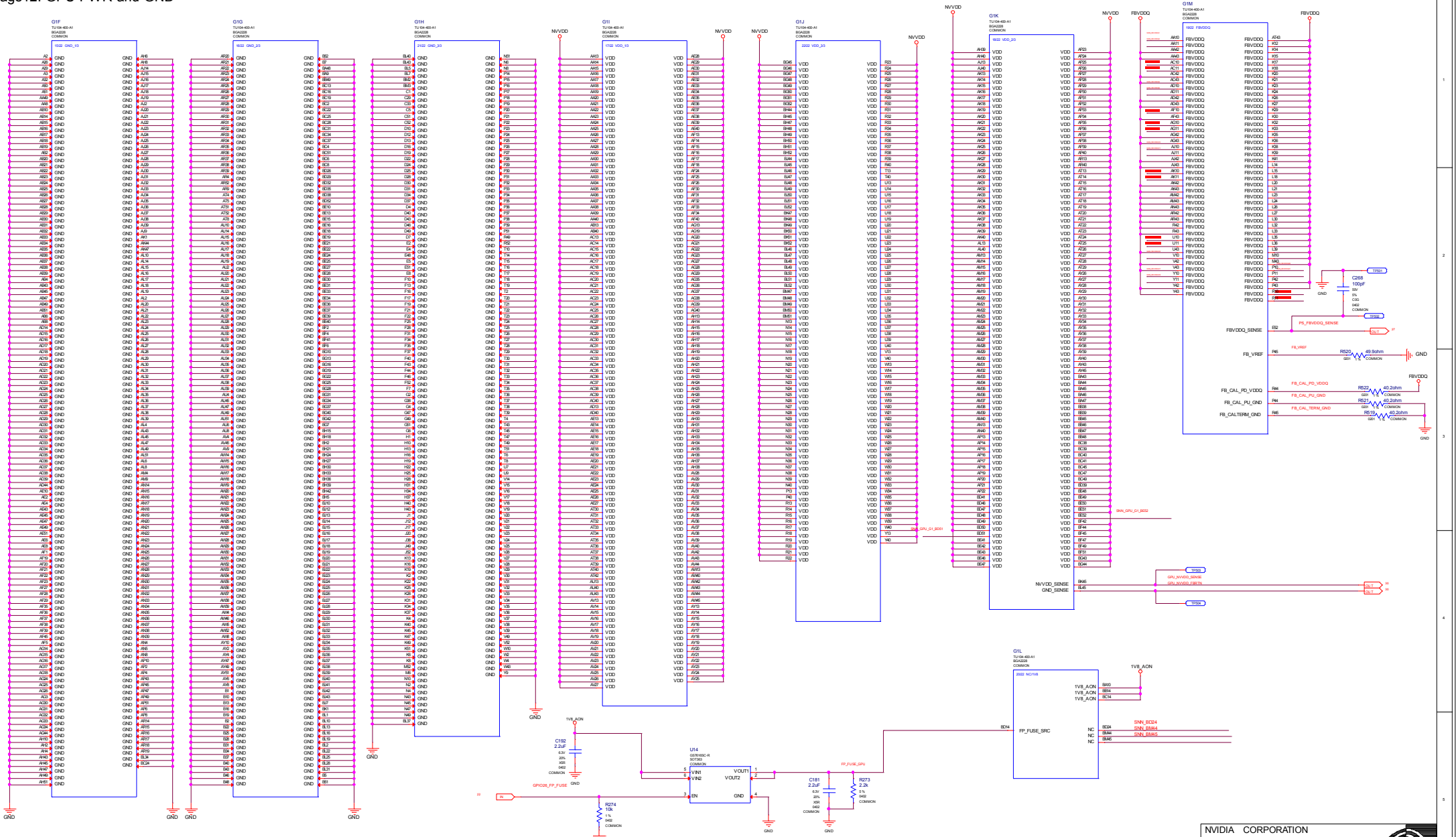
Page12: GPU PWR and GND



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU PWR & GND

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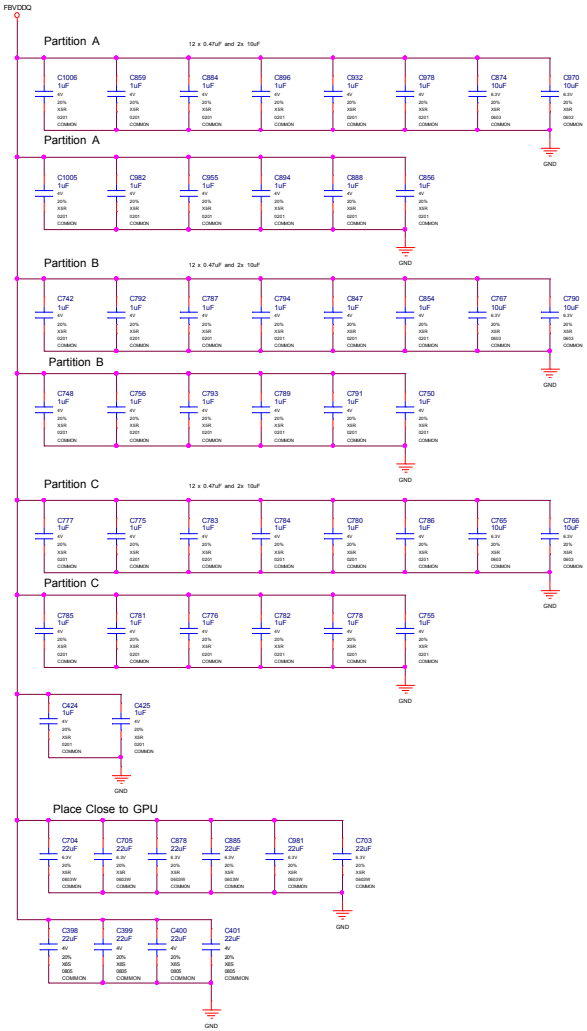
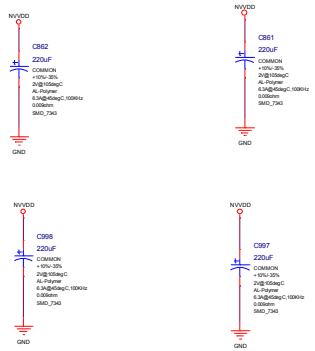
Page13: GPU DECOUPLING 1

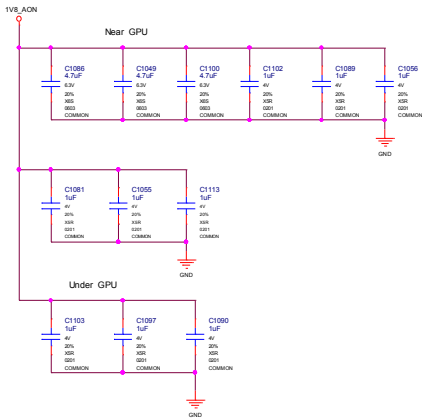
FBVDDQ



NVVDD



1V8_AON



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU DECOUPLING 1

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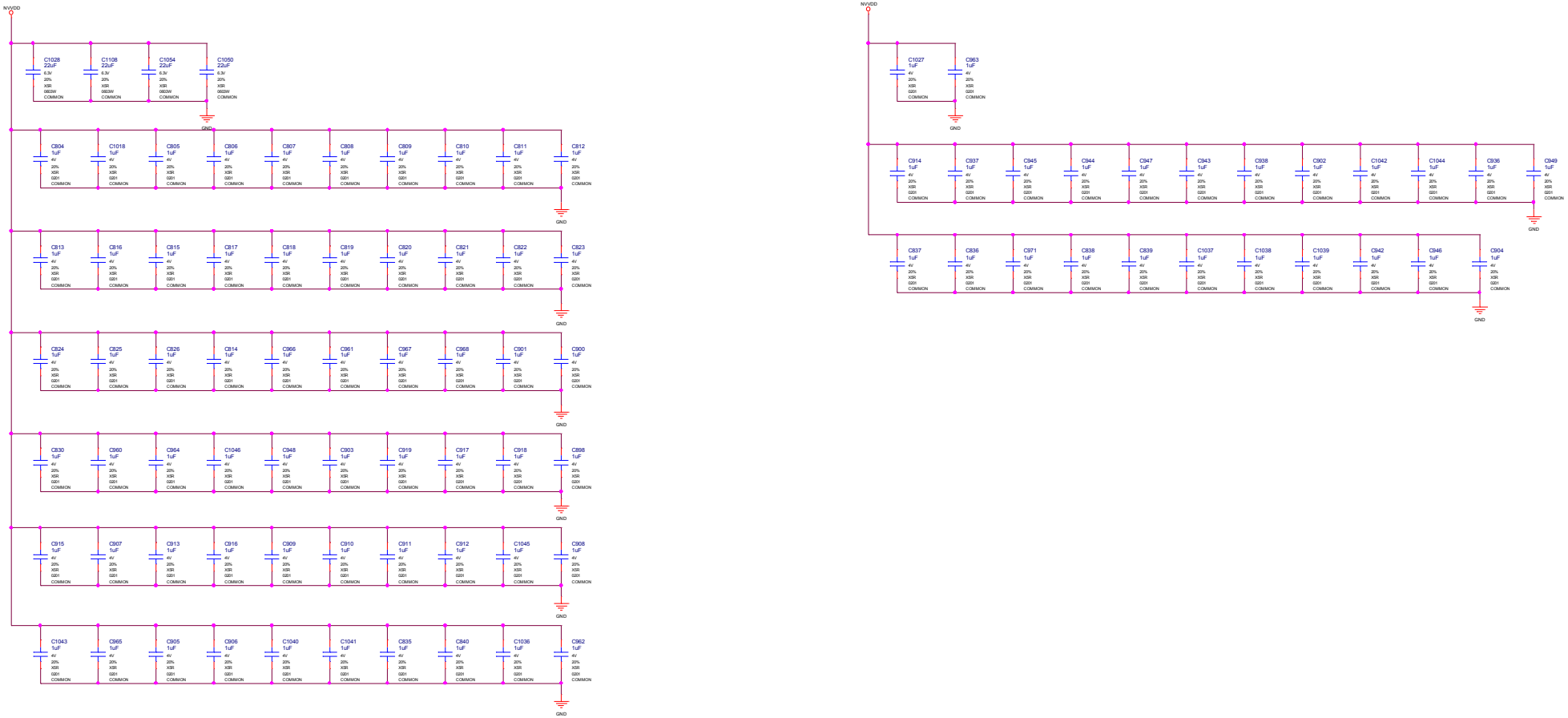
Page14: GPU DECOUPLING 2

NVVDD



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PAGE DETAIL	GPU DECOUPLING 2

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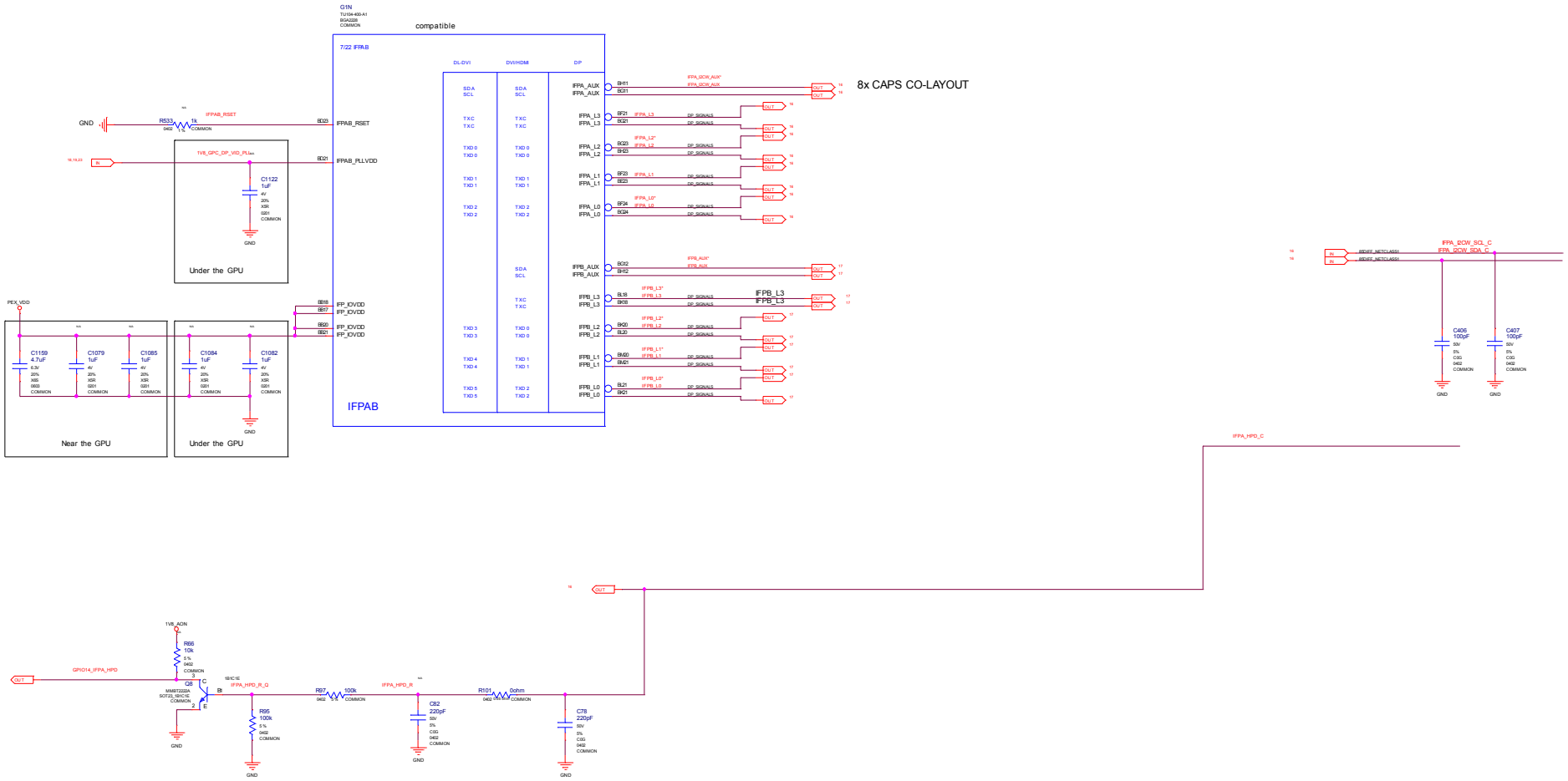
Page15: IFPAB DVI-D-DL



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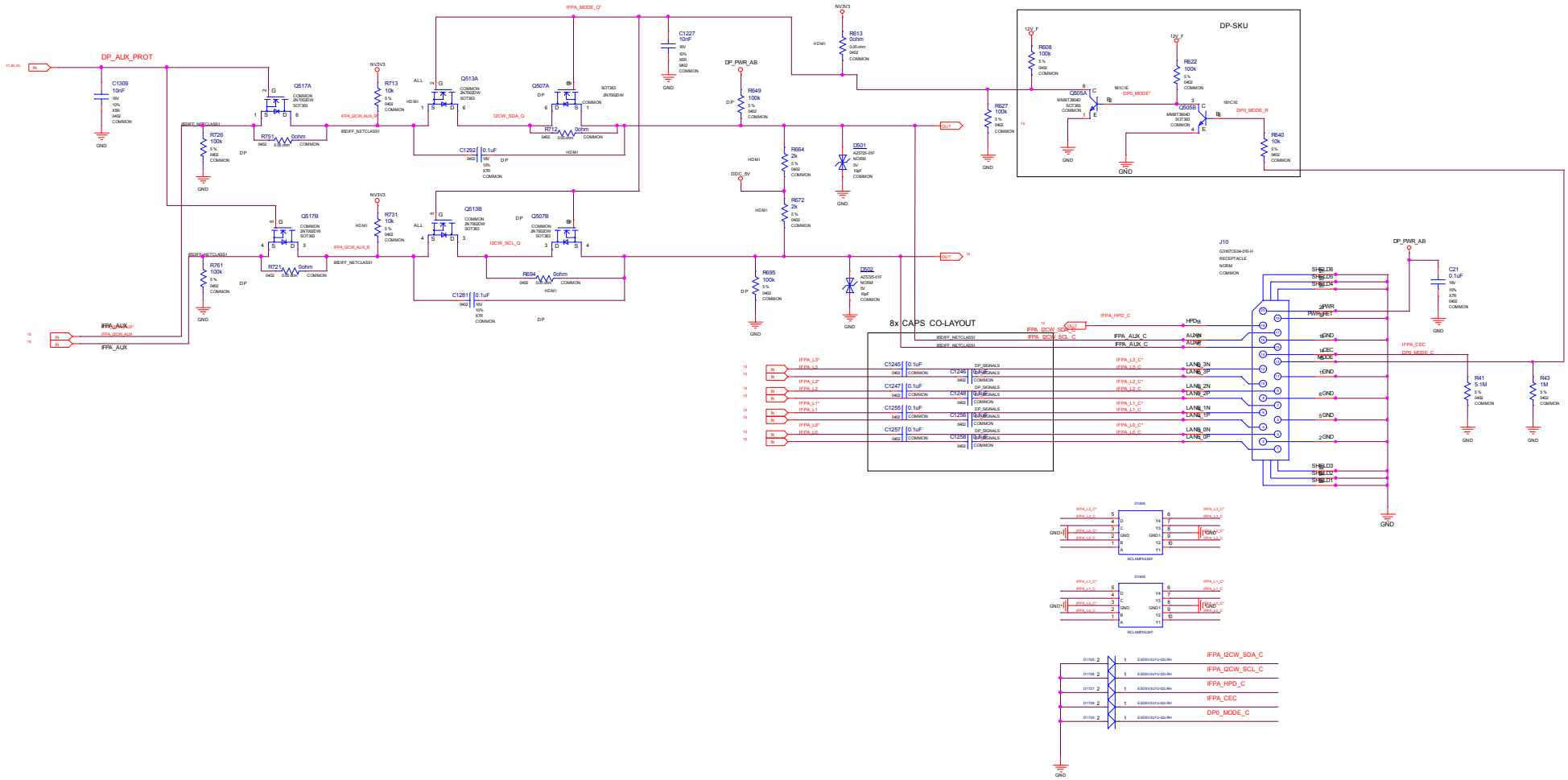
Page16: IFPA DP



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PAGE DETAIL	ID: IFPA DP

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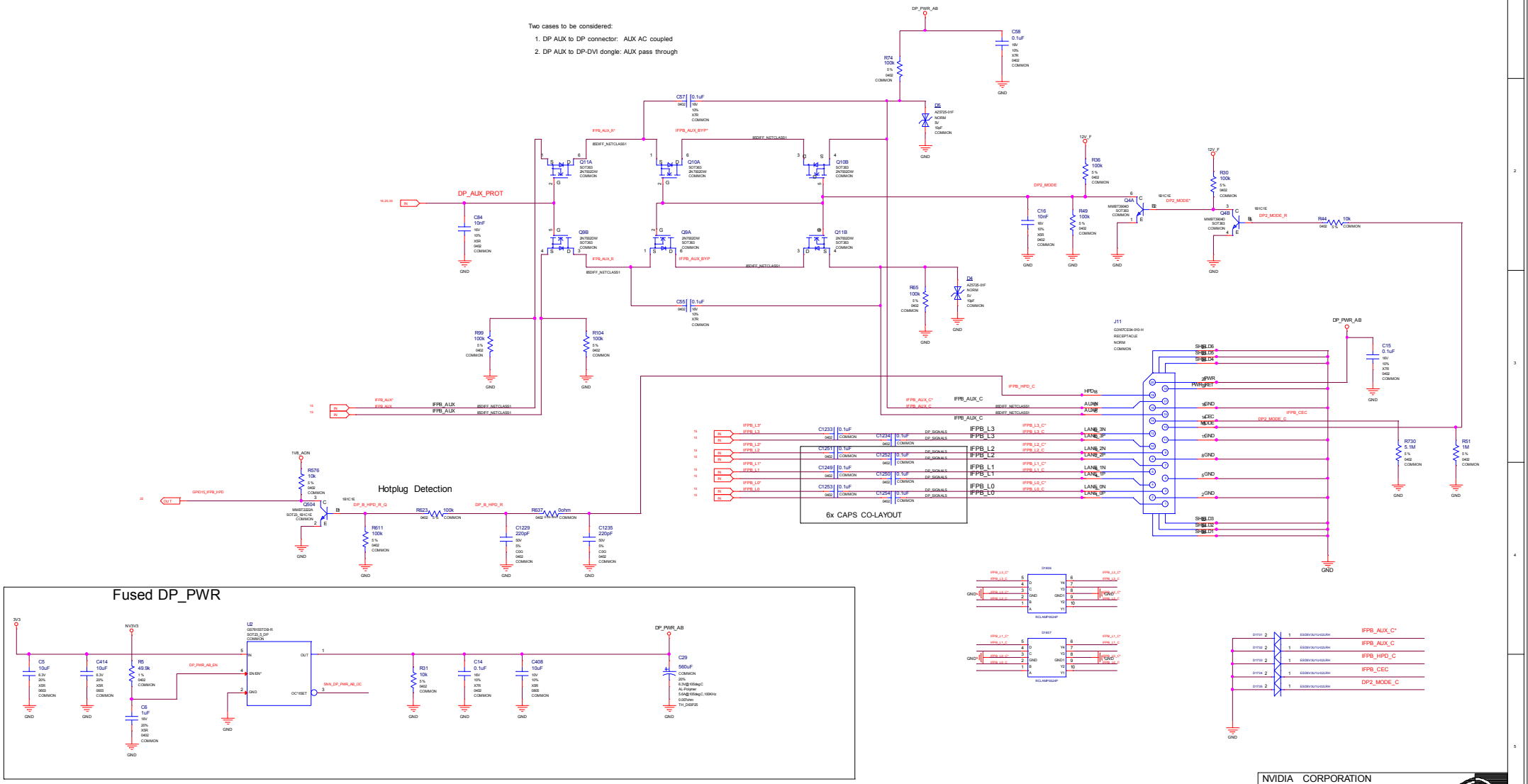
Page17: IFPB DP



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PAGE DETAIL	ID: IFPB DP

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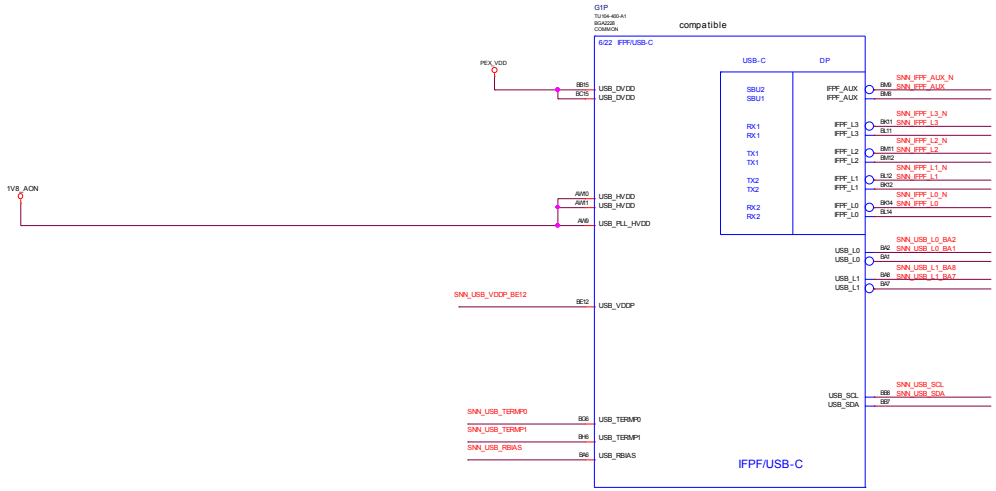
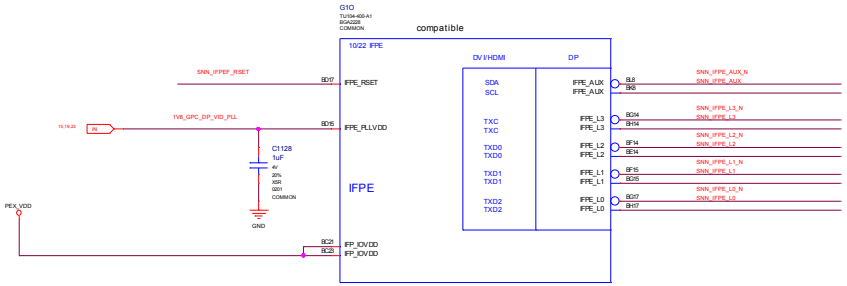
Page18: IFPE & IFPF NC





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IC: IFPE & IFPF NC

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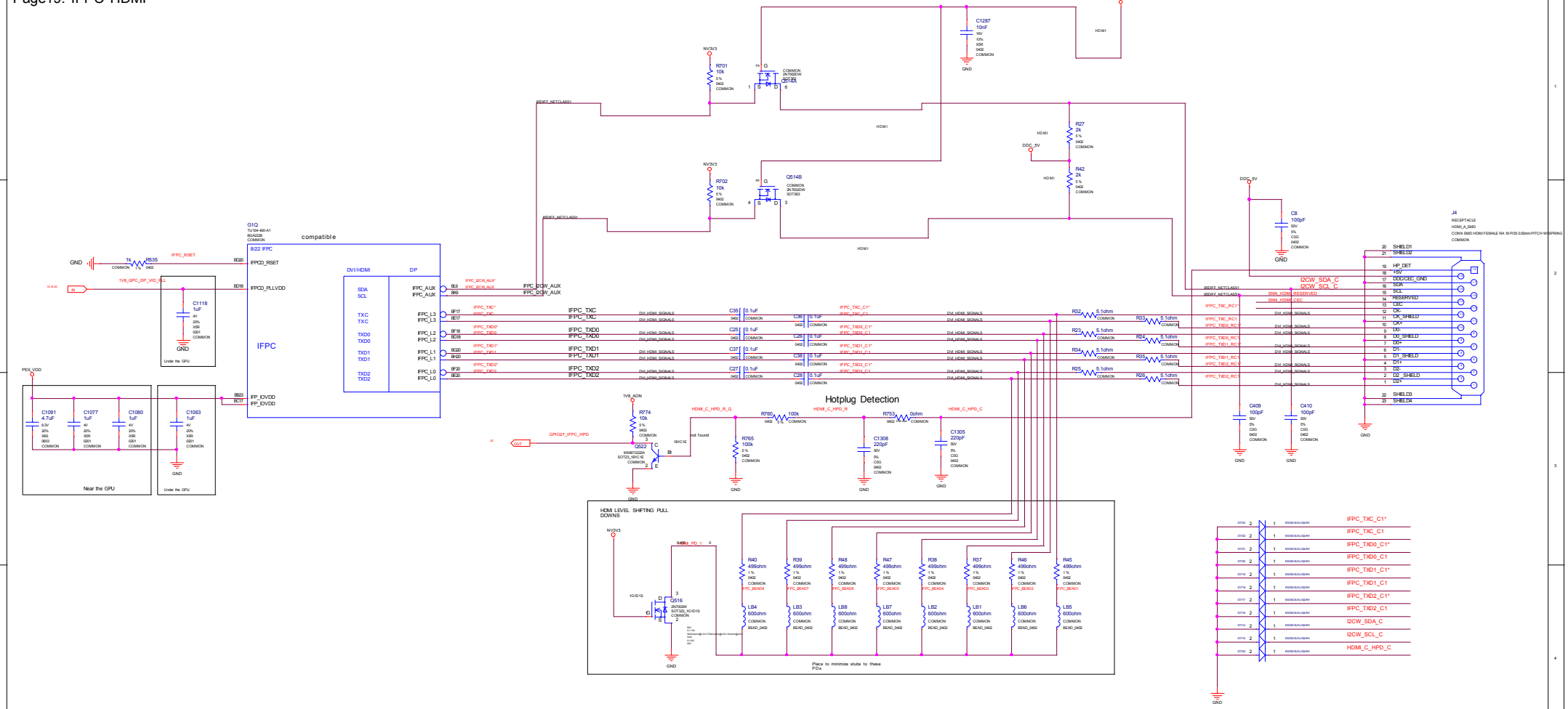
Page19: IFPC HDMI



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFPC HDMI

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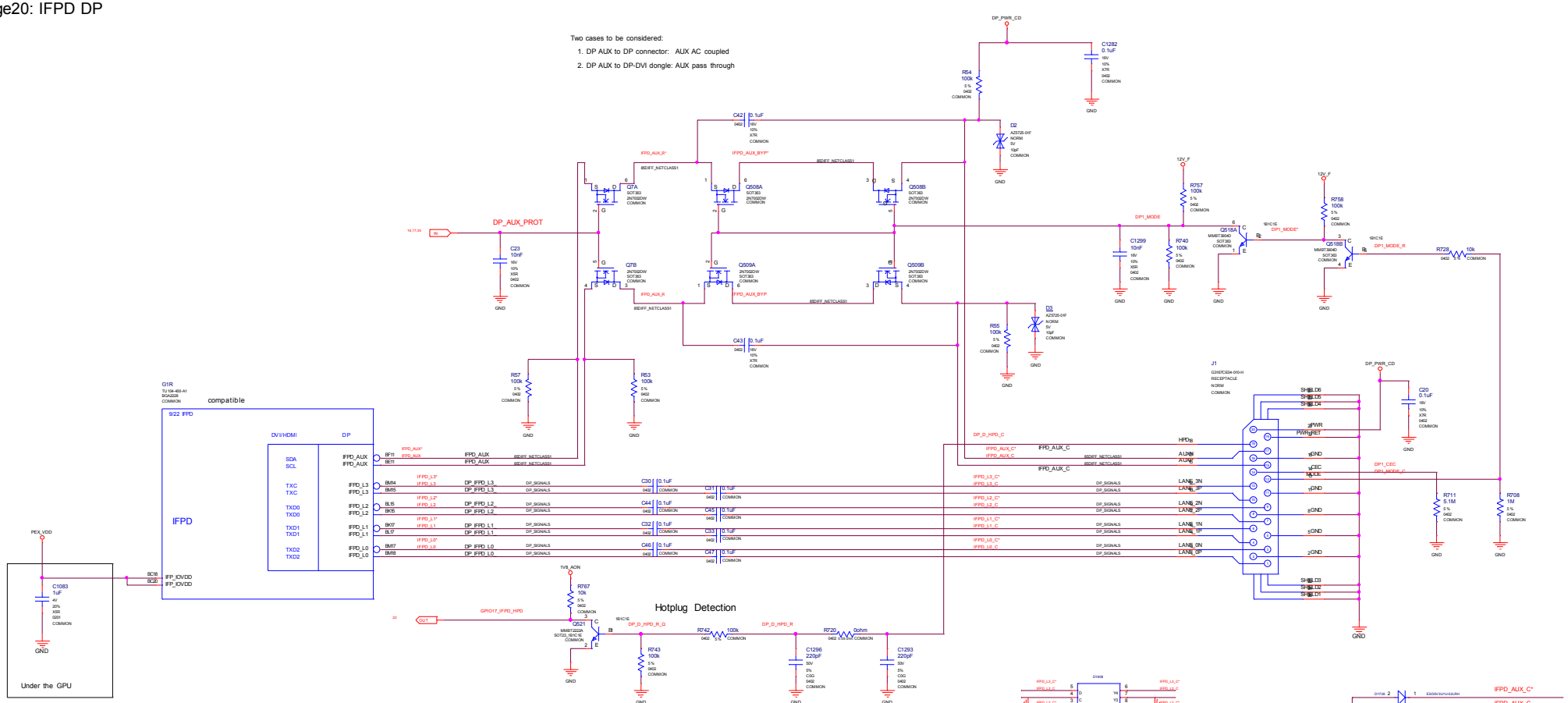
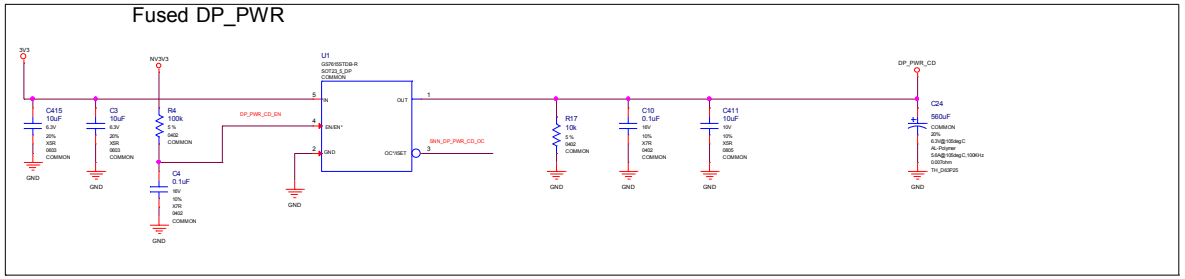
Page20: IFPD DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



Fused DP_PWR



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFPD DP

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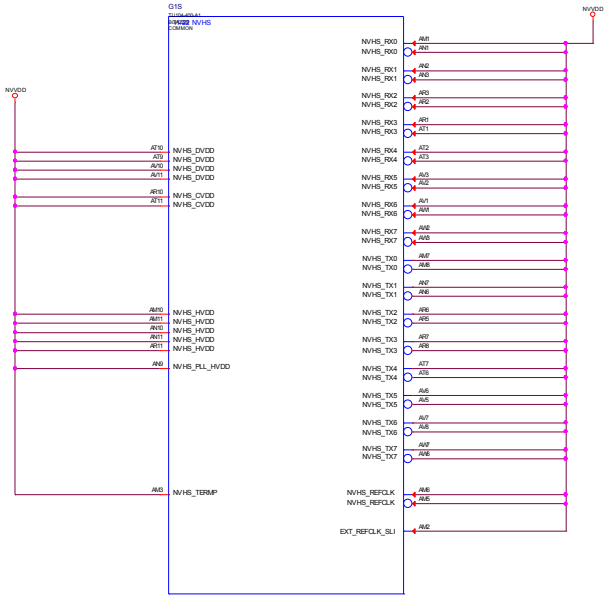
Page21: NVHS INTERFACE AND FRAME LOCK

Use NC pin to Improve NVVDD,FBVDDQ,1V8 PDN

For TU116 Only



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: NVHS INTERFACE AND FRAME LOCK

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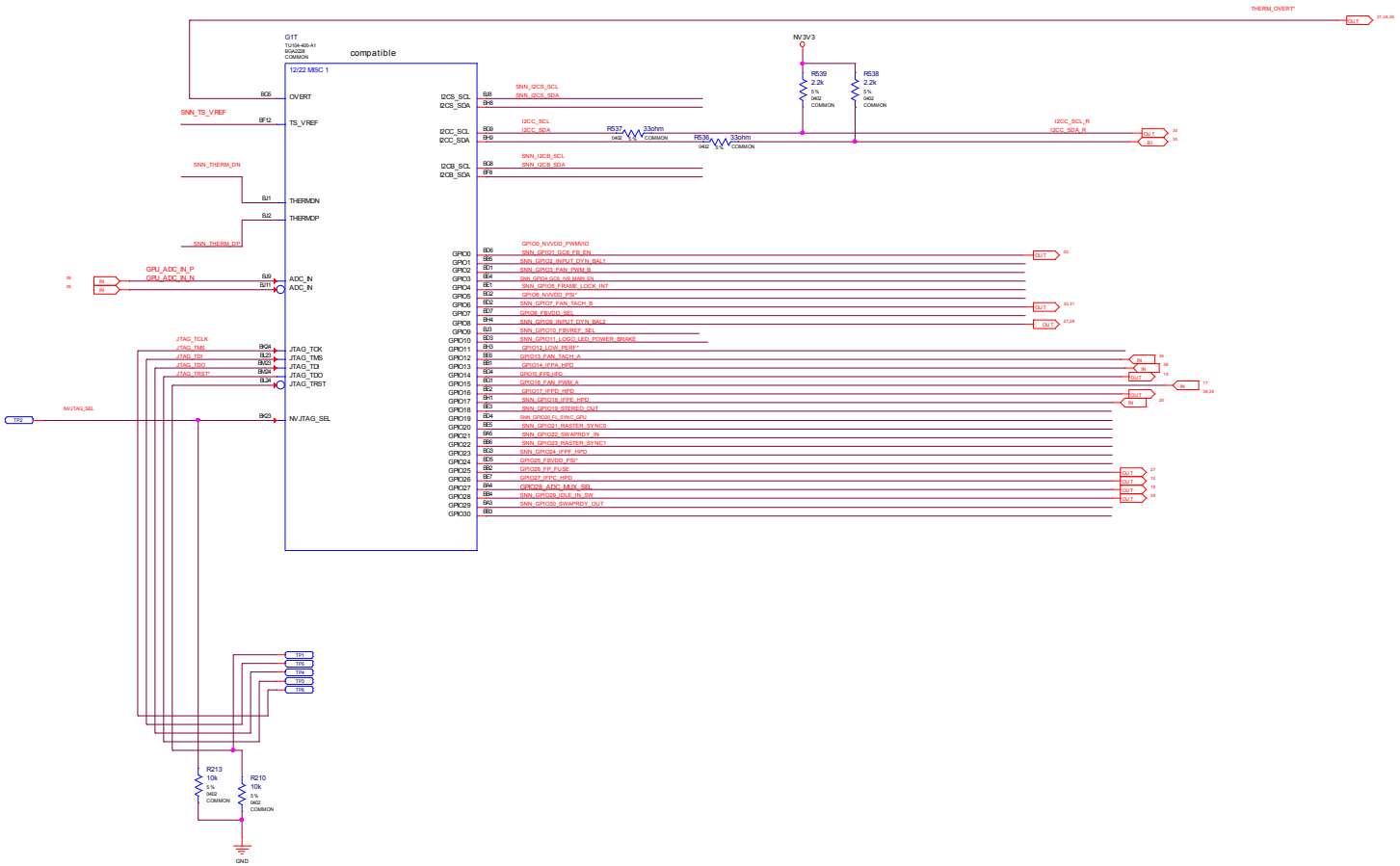
Page22: MISC1: JTAG, GPIO, ADC, I2C, OVERT



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC1: JTAG,GPIO,ADC,I2C,OVERT.

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Page23: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	Samsung 8Gb 256Mx32 K4Z80325BC-HC14
L	L	H	0001	Micron 8Gb 256Mx32 MT61K256M32JE-14:A
L	H	L	0010	Hynix 8Gb 256Mx32 H56C8H24MJR-S2C
L	H	H	0011	Samsung 8Gb 256Mx32 K4Z8032BC-HC12
H	H	L	0110	
H	H	H	0111	
L	L	M	1000	
L	M	L	1001	

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

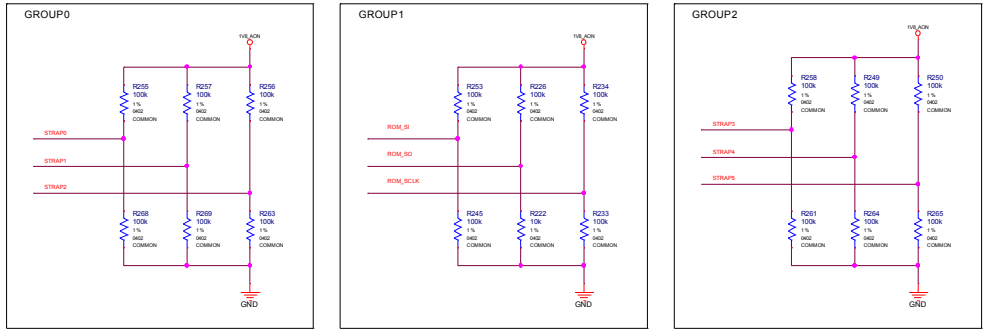
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

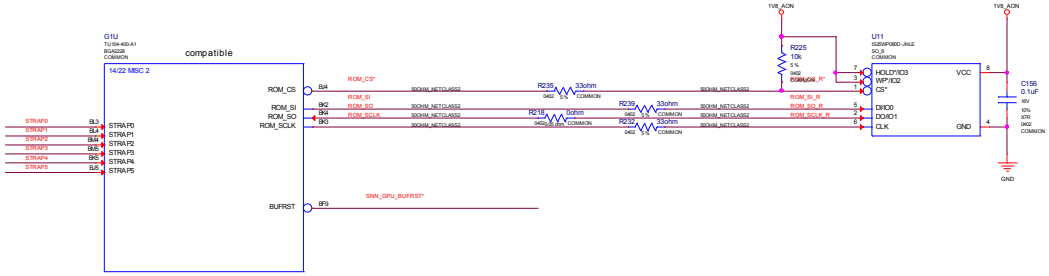
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

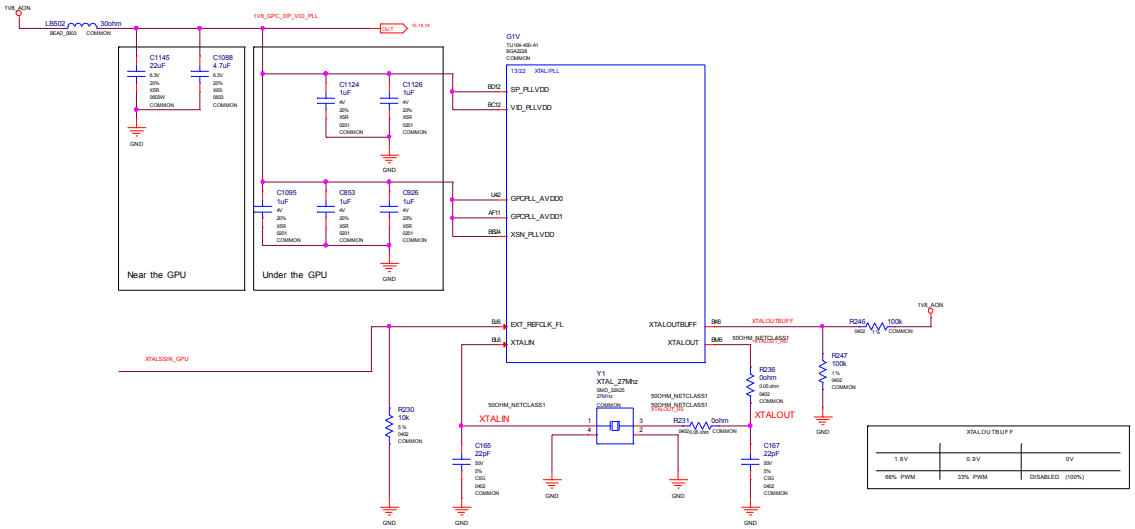
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE







ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC2: ROM, XTAL,STRAPS

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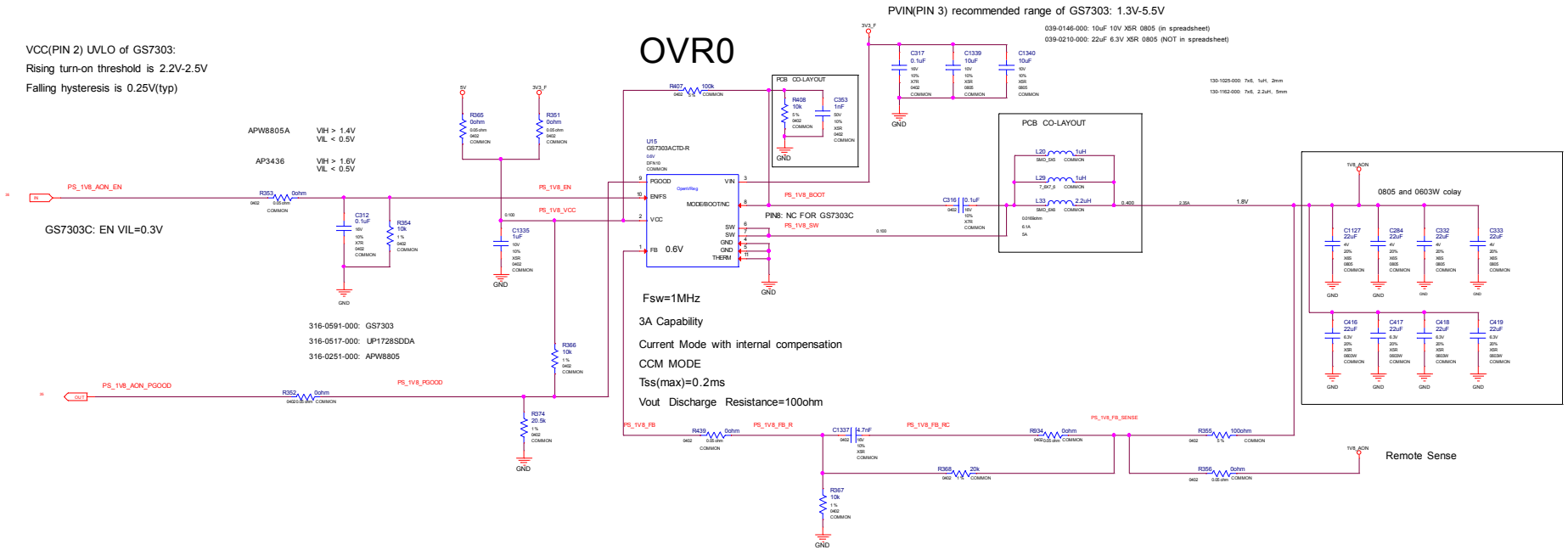
Use 5V as 1V8 OVR0 VCC(PIN 2), can make 1V8_AON power down later(hold more time during power down).
And no glitch on 1V8_PGOOD.

1v8 Switcher



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PAGE DETAIL	PS: 1V8_AON

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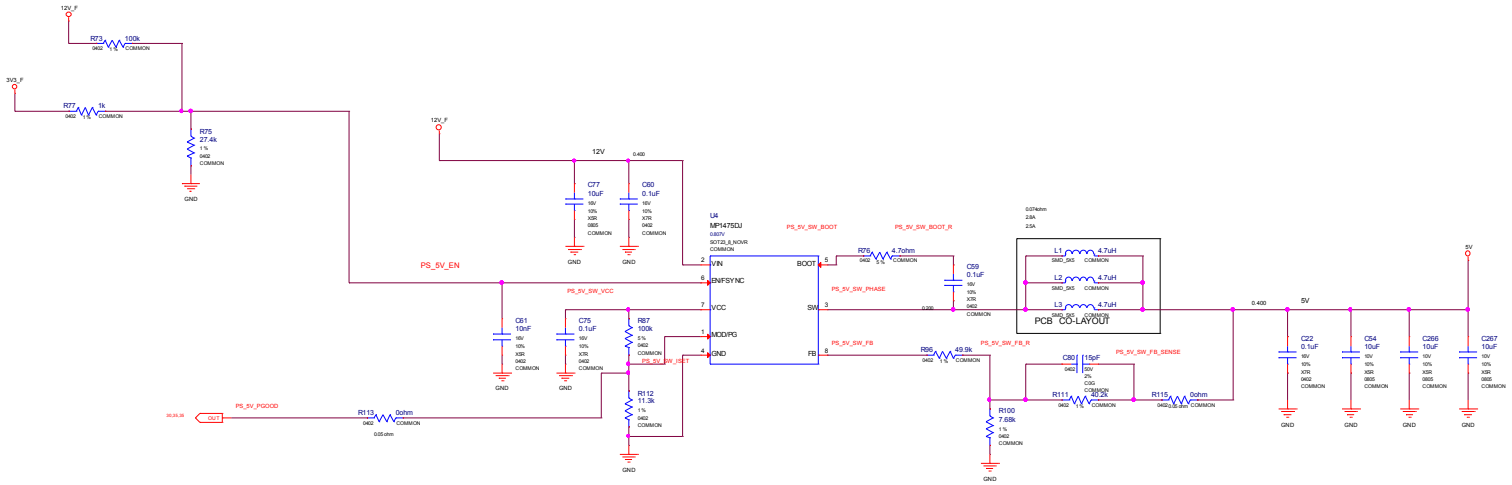
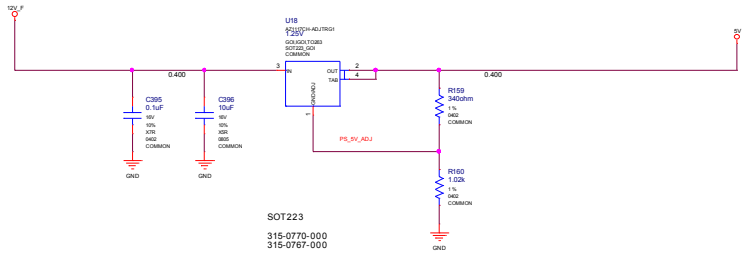
Page25: PS: 5V



0.8V*(1+40.2K/7.68K)=4.9875V



SOT223

315-0770-000
315-0767-000

Vout=1.25*(1+1020/340)+60uA*1020=5.06V

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: 5V

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DUE

Use 5V as PEX_VDD OVR0 VCC(PIN 2),
enable PEX_VDD OVR0 internal discharge(100ohm typ), making PEX_VDD power down faster.

PEX_VDD Switcher

ADD 3 MORE MLCC
3V3_F is Far Away From Source

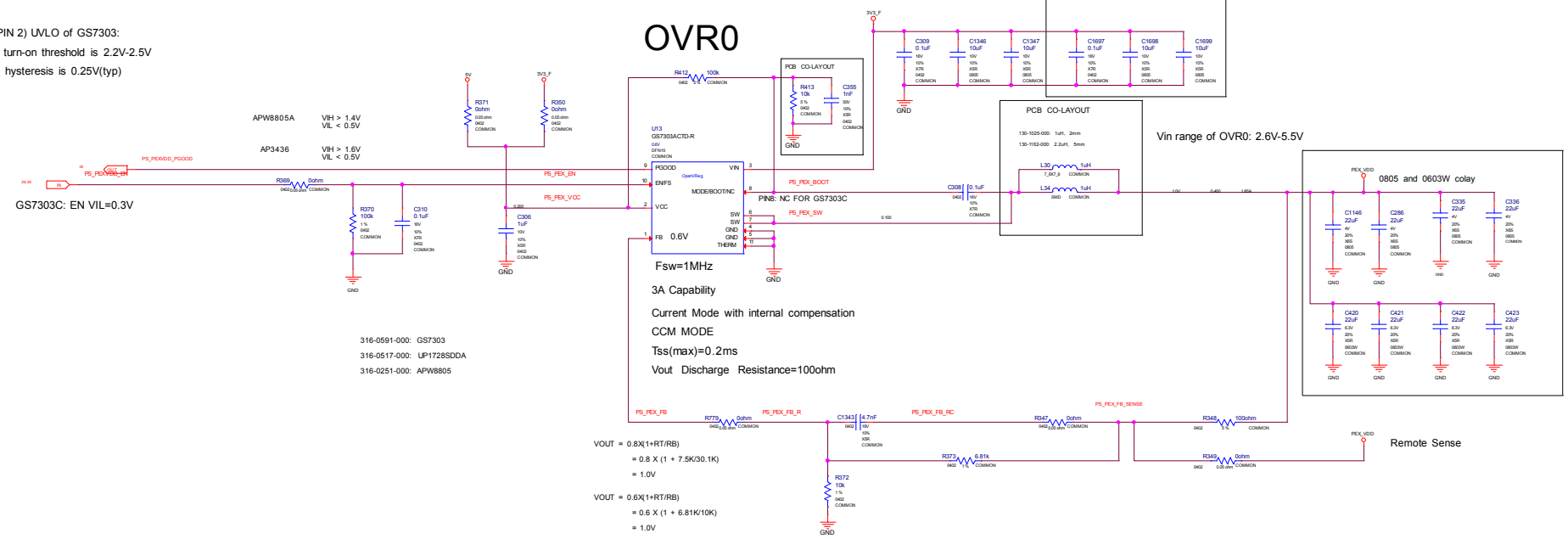
VCC(PIN 2) UVLO of GS7303:
Rising turn-on threshold is 2.2V-2.5V
Falling hysteresis is 0.25V(typ)

APW8805A VIH > 1.4V VIL < 0.5V

AP3436 VIH > 1.6V VIL < 0.5V

GS7303C: EN VIL=0.3V

OVR0



Fsw=1MHz

3A Capability

Current Mode with internal compensation

CCM MODE

Tss(max)=0.2ms

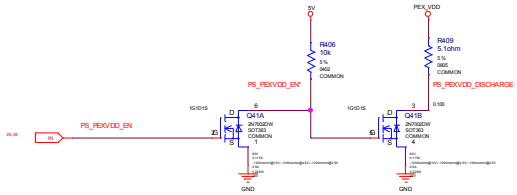
Vout Discharge Resistance=100ohm

316-0591-000: GS7303
316-0517-000: UP1728SDDA
316-0251-000: APW8805

VOUT = 0.8X(1+RT/RB)
= 0.8 X (1 + 7.5K/30.1K)
= 1.0V

VOUT = 0.6X(1+RT/RB)
= 0.6 X (1 + 6.81K/10K)
= 1.0V

0.6V*(1+6.81K/10K)=1.008V



PEX_VDD DISCHARGE(DEFAULT NO STUFF)

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: PEXVDD

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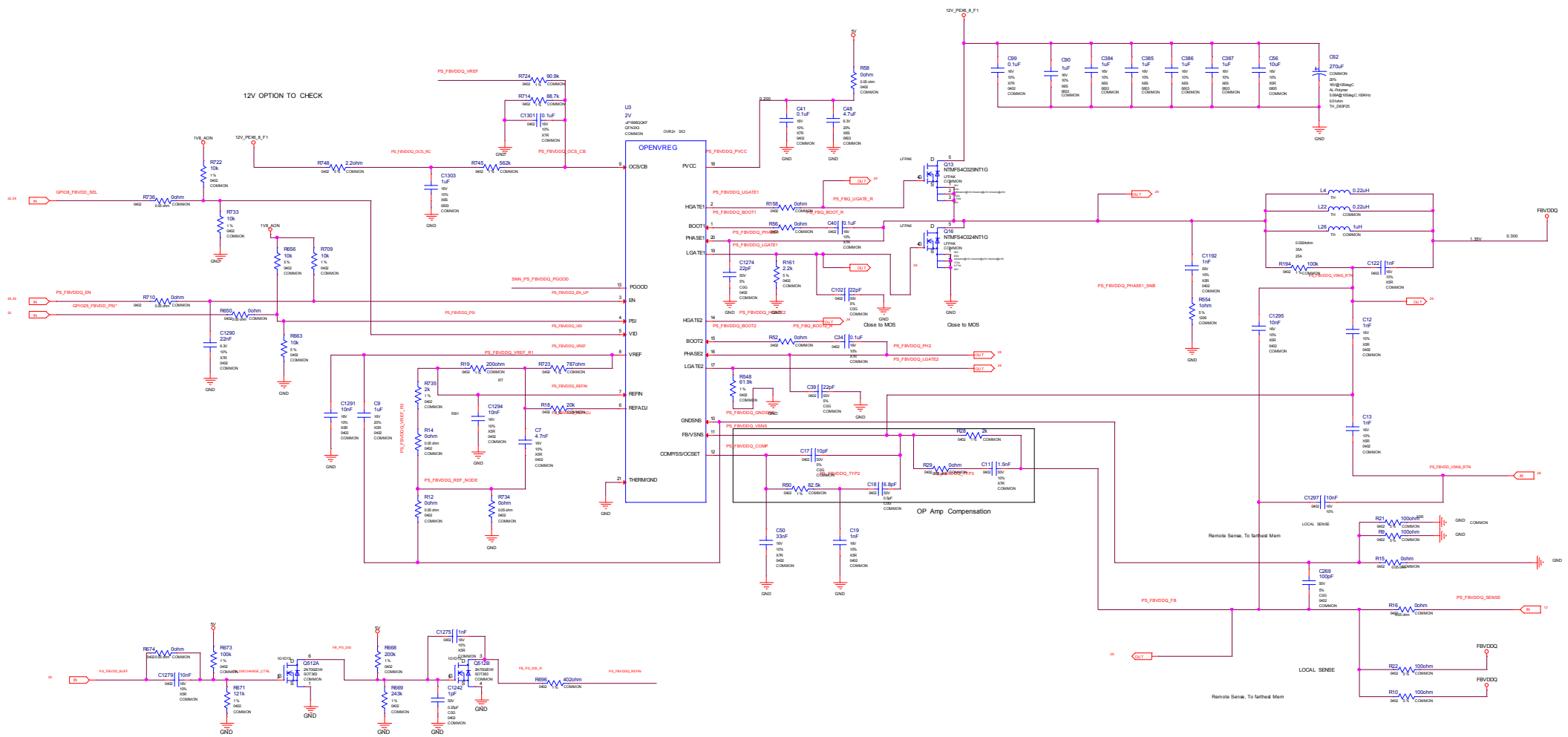
Page27: PS: FBVDDQ



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: FBVDDQ

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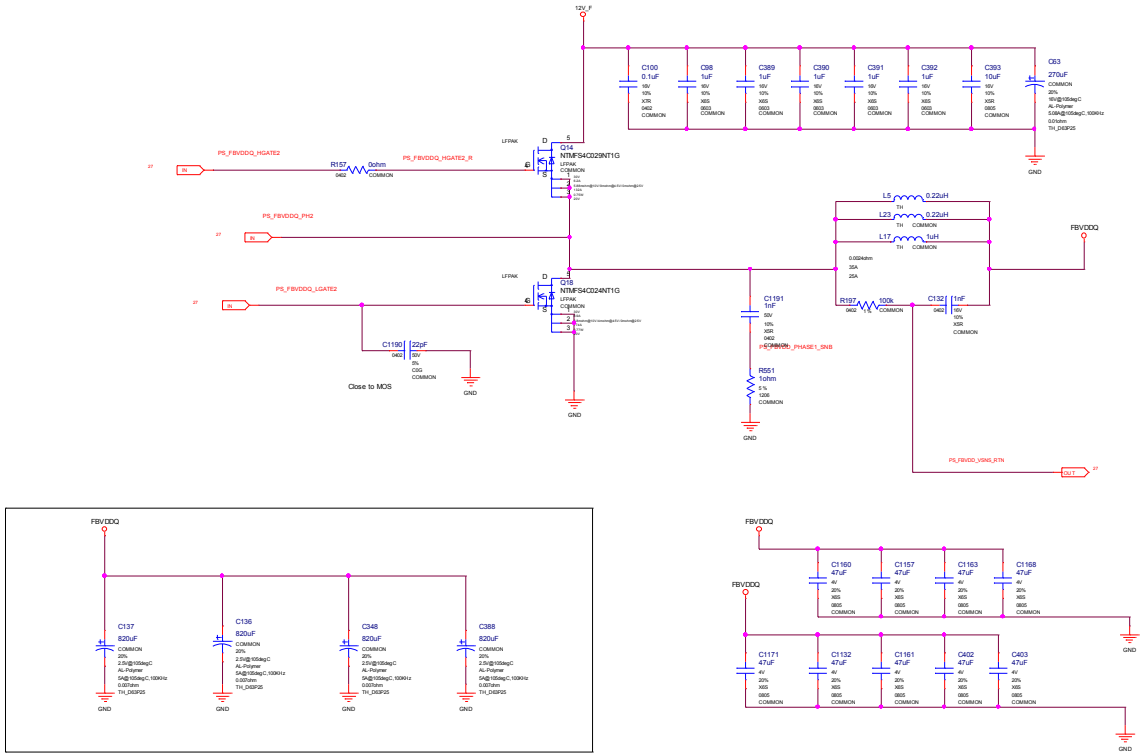
Page28: PS: FBVDDQ PH2



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: FBVDDQ PH2

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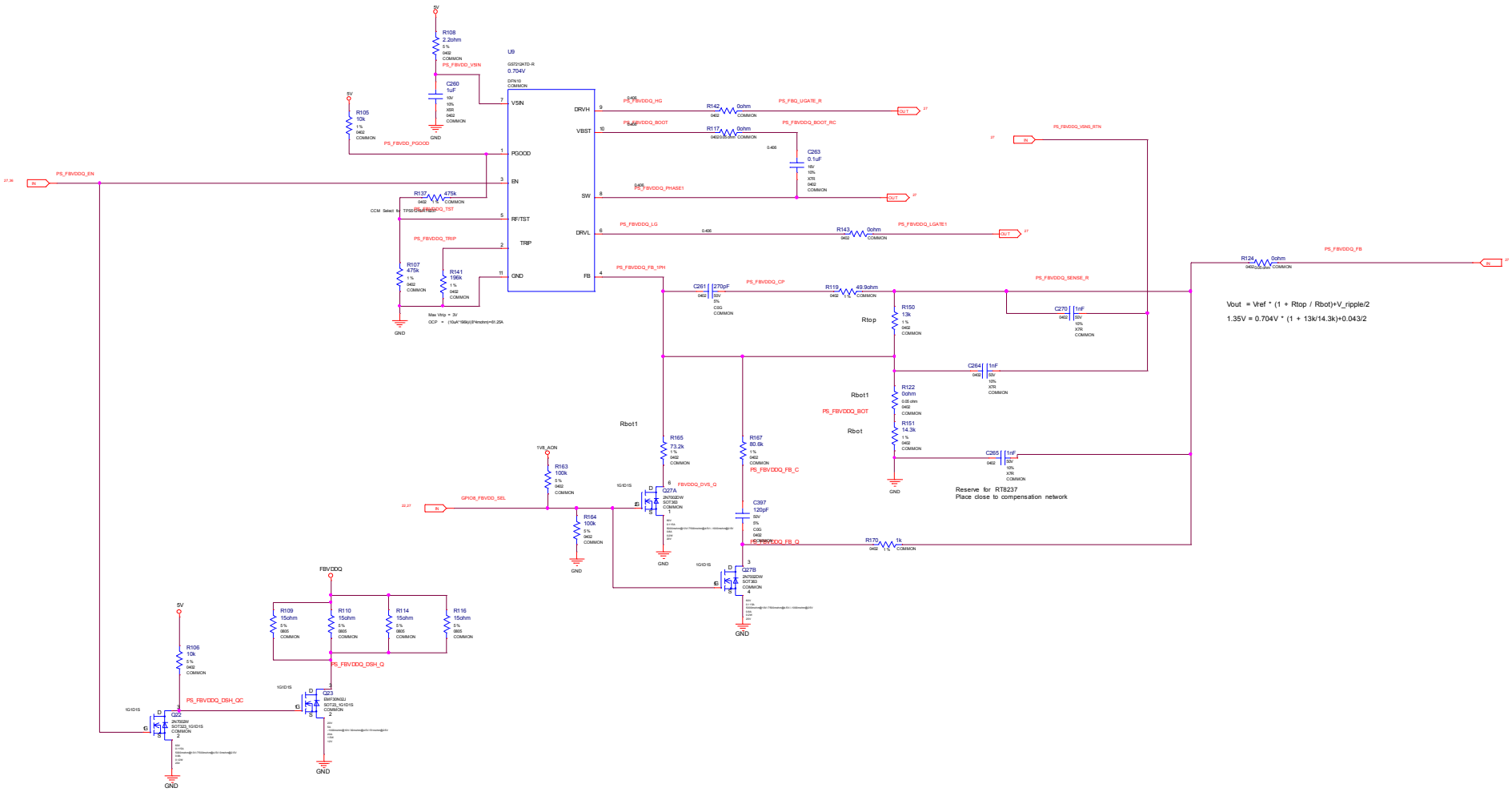
Page29: PS: FBVDDQ



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: FBVDDQ VR option

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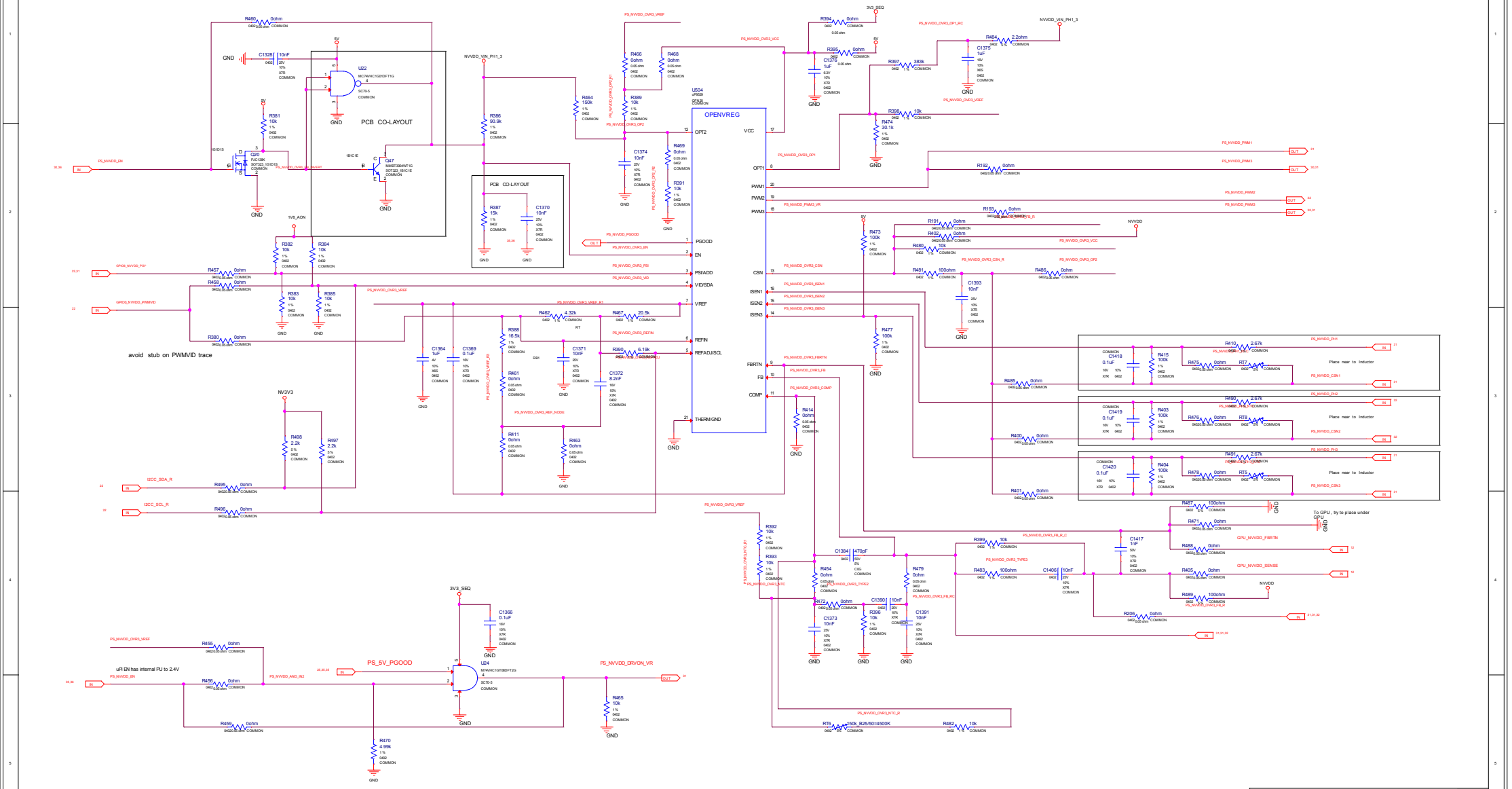
Page30: PS: NVVDD CTR



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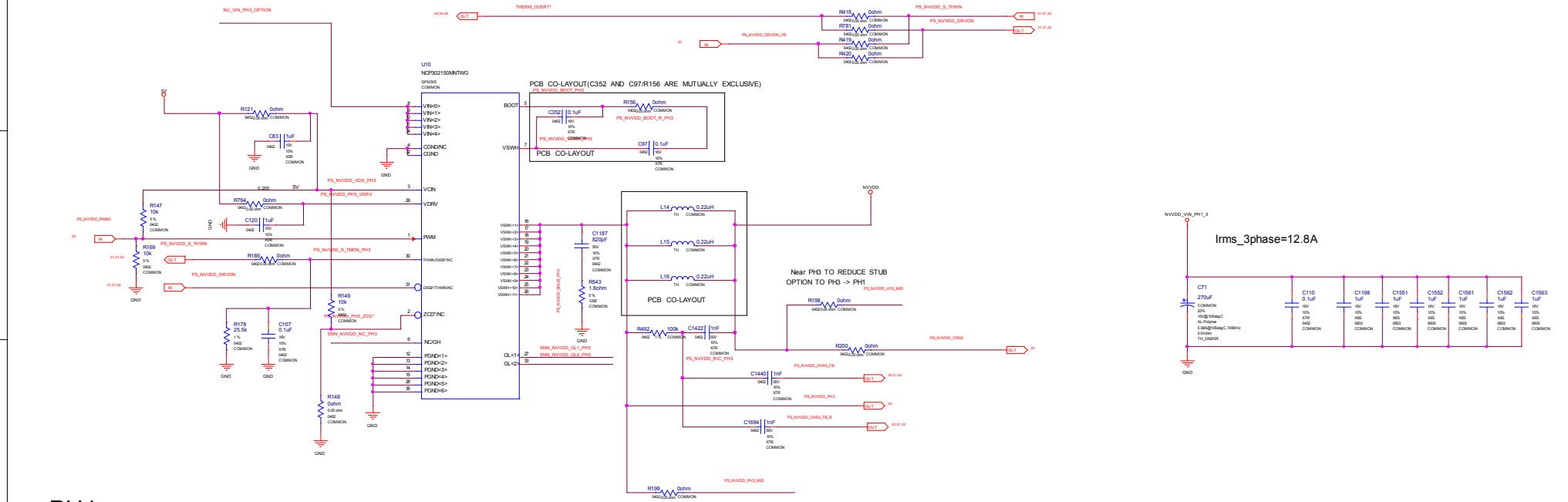
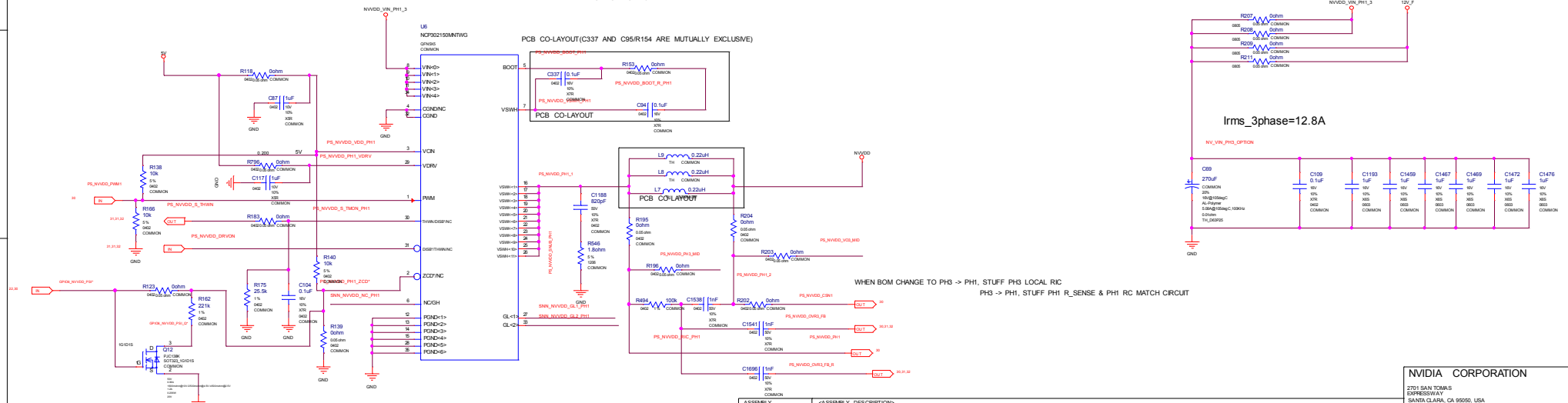
PH3



PH1



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD Phase 1,3

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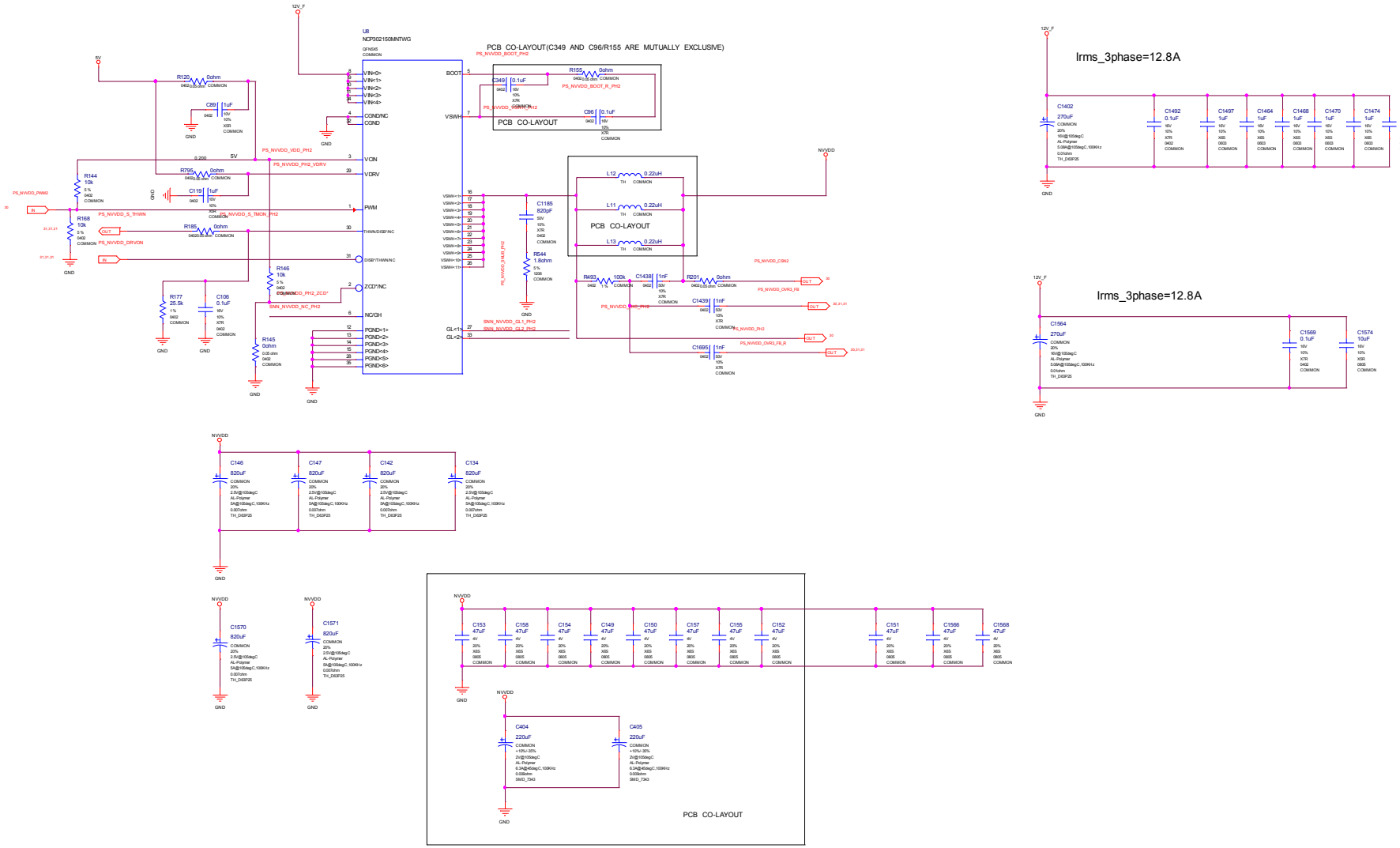
Page32: PS: NVVDD PH2



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD Phase 2

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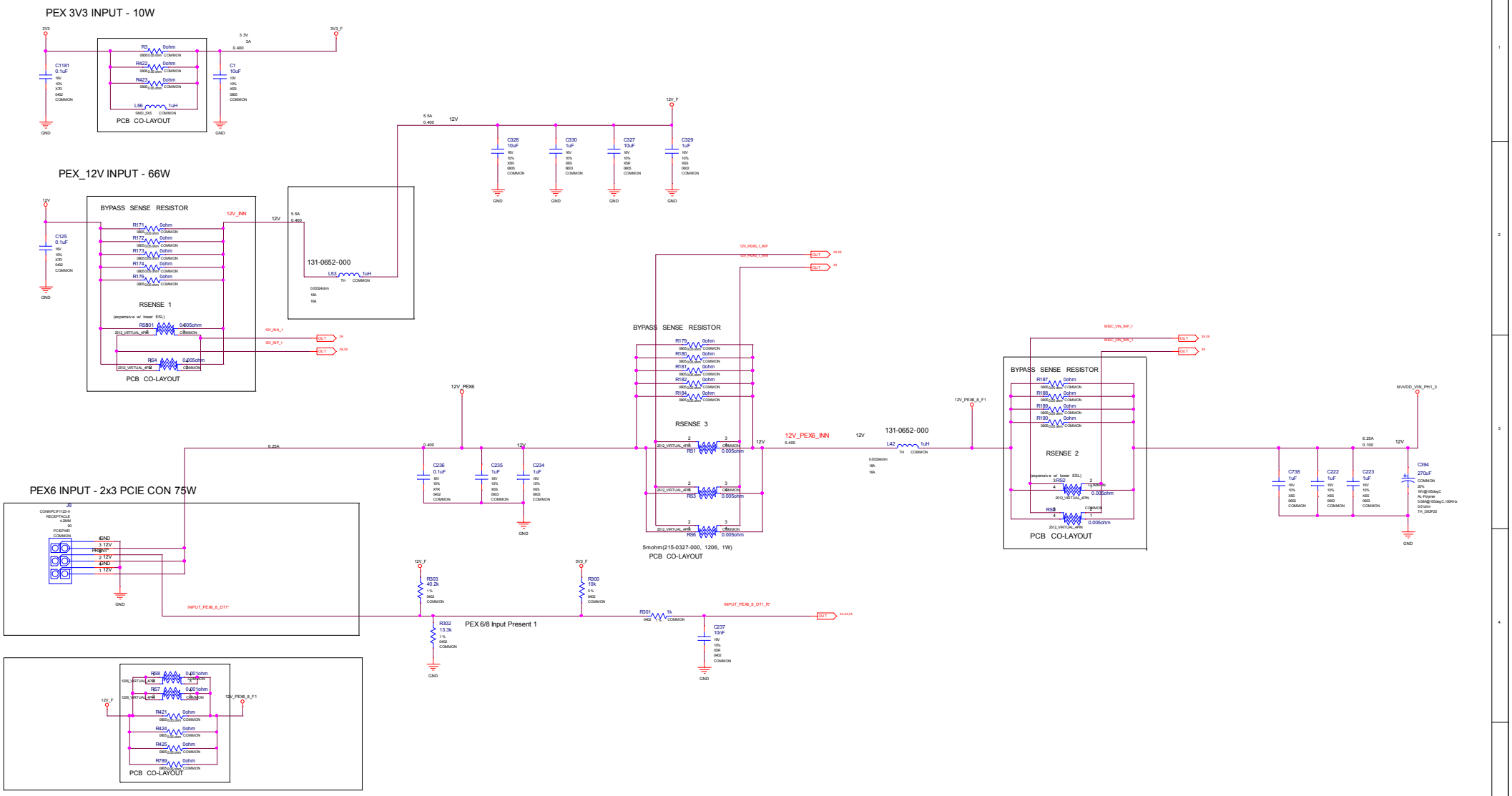
Page33: PS: Inputs, Filtering, and Monitoring



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Inputs, Filtering, and Monitoring

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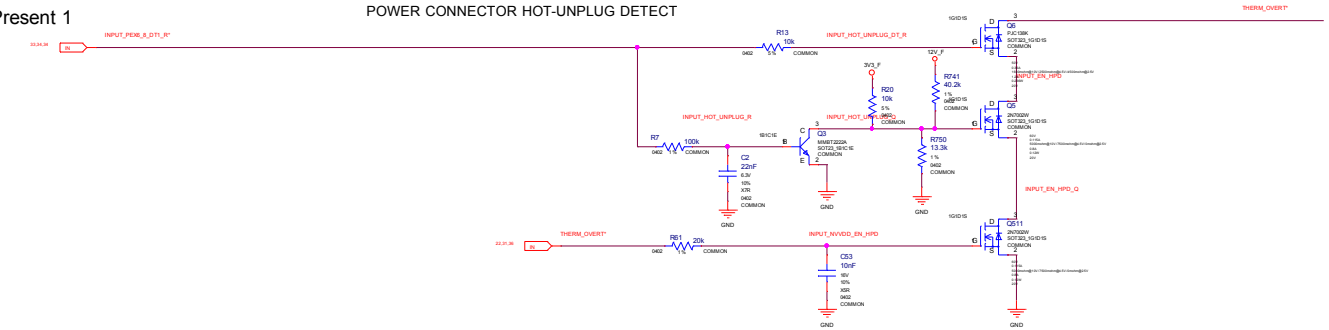
Page34: PS: HOT-UNPLUG, UNDER POWER BOOT, CURRENT STEERING

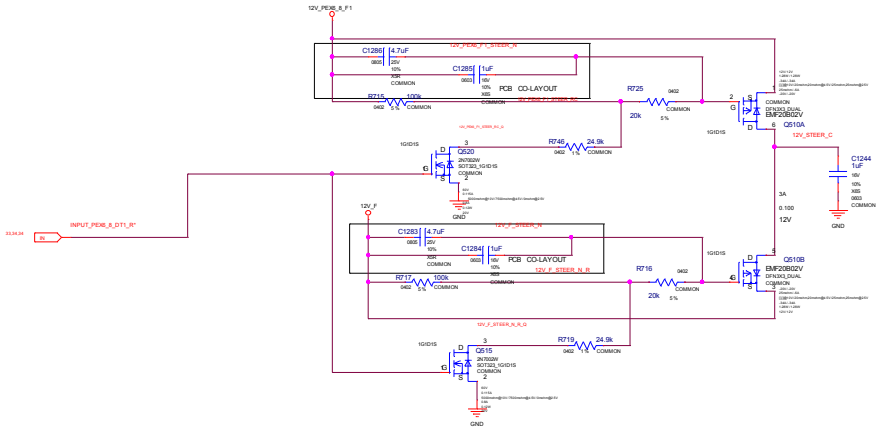
PEX Input Present 1

POWER CONNECTOR HOT-UNPLUG DETECT

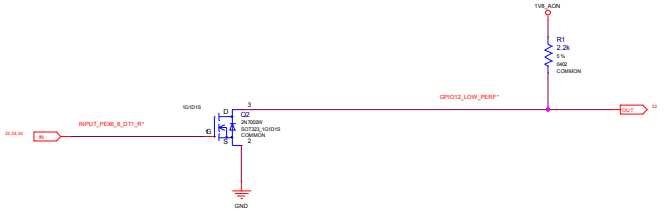


12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA



PEX Input - Power Level/PSI* Control



GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: STEERING, UPB & HOT-UNPLUG

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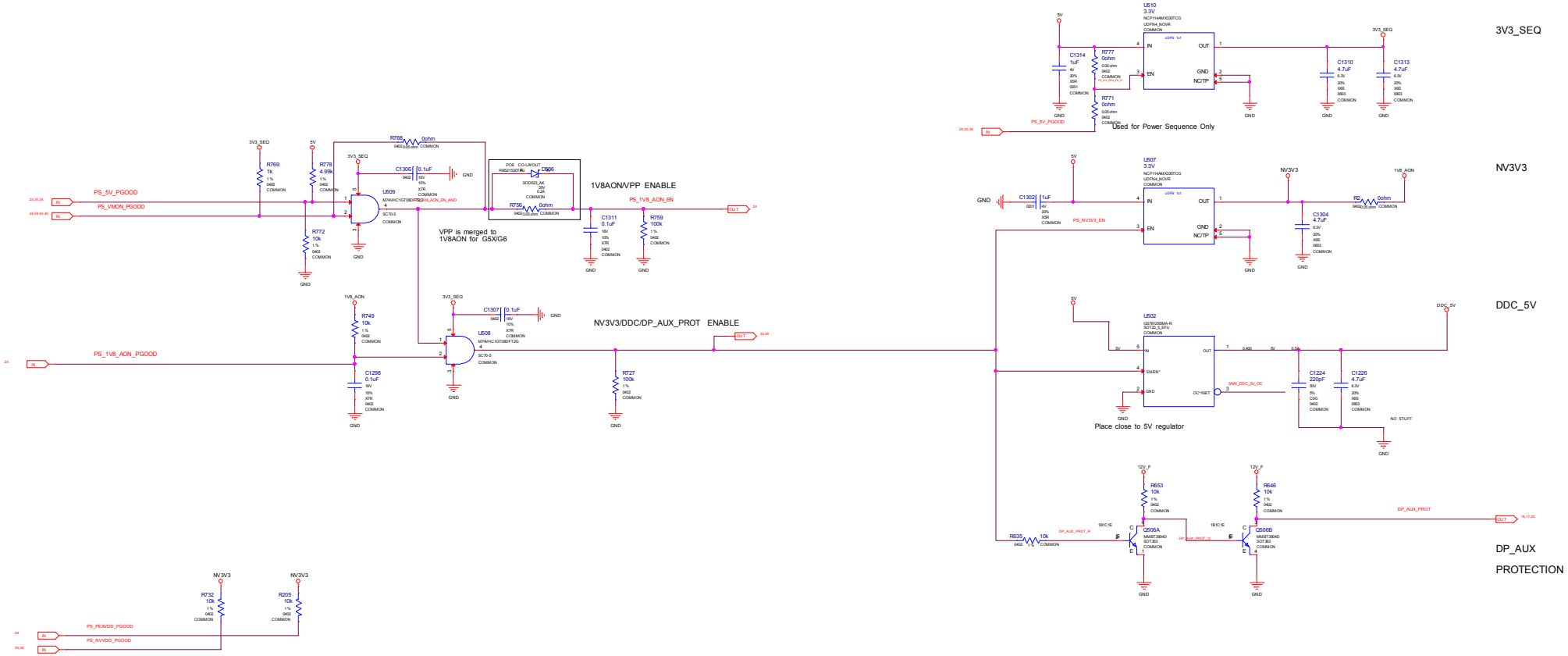
Page35: SEQ:1V8_AON, 3V3_SEQ, NV3V3, DDC_5V, DP_AUX_PROT



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PAGE DETAIL	SEQ: 1V8_AON, 3V3_SEQ, NV3V3, DDC_5V, DP_AUX_PROT

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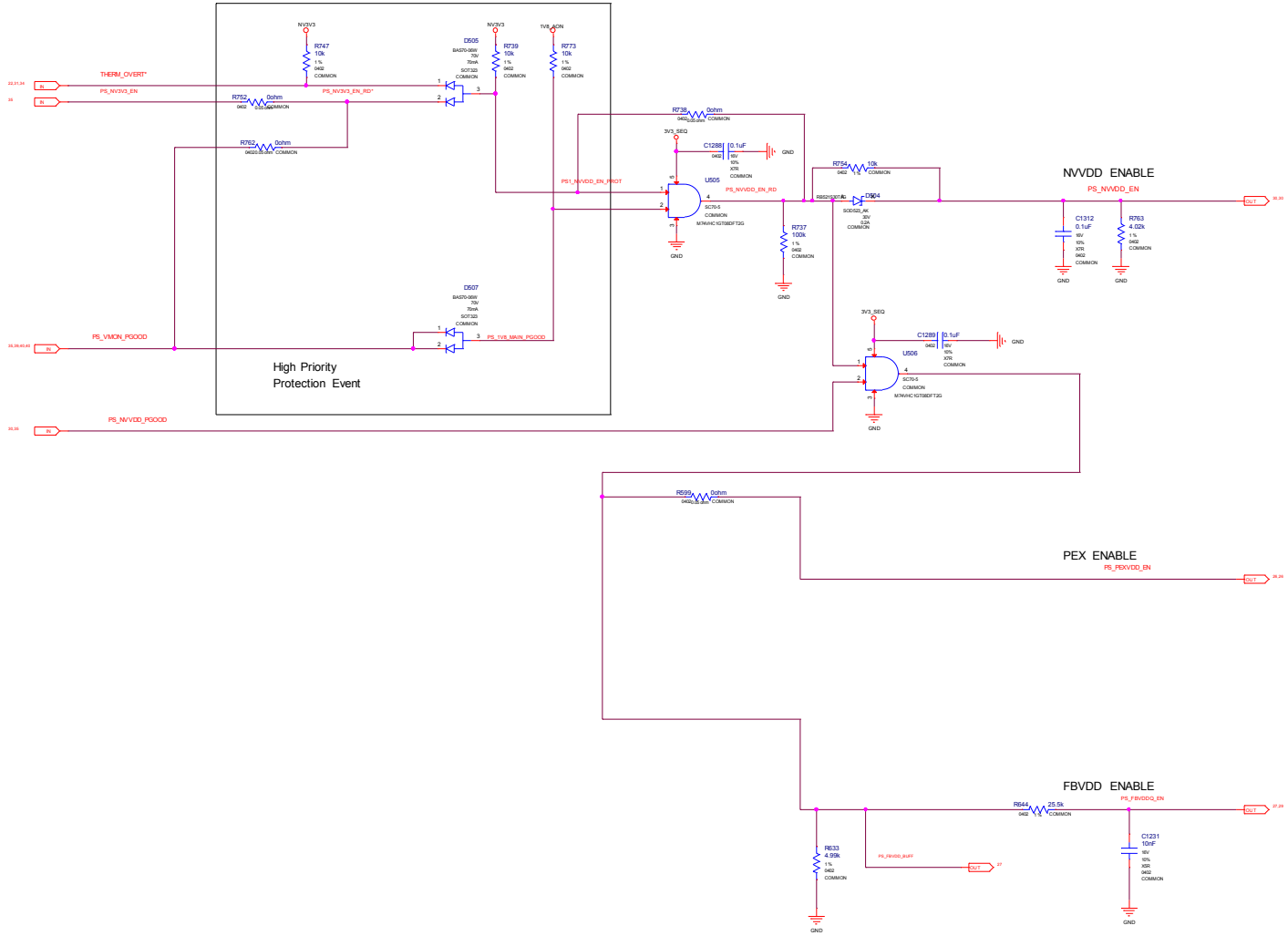
Page36: SEQ:NVVDD, PEX, FBVDDQ ENABLE



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQ: NVVDD, PEX, FBVDDQ ENABLE

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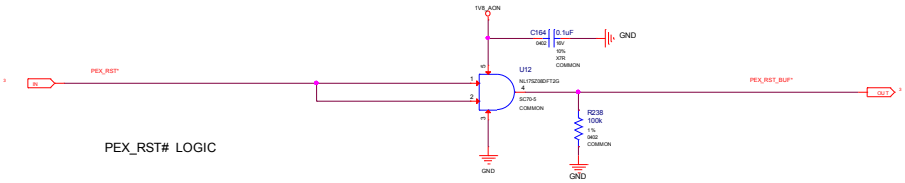
Page37: SEQ:MISC

PU ON GPU SIDE
NC ON GOLD FINGER SIDE

PU ON GPU SIDE
NC ON GOLD FINGER SIDE



PEX_RST# LOGIC

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
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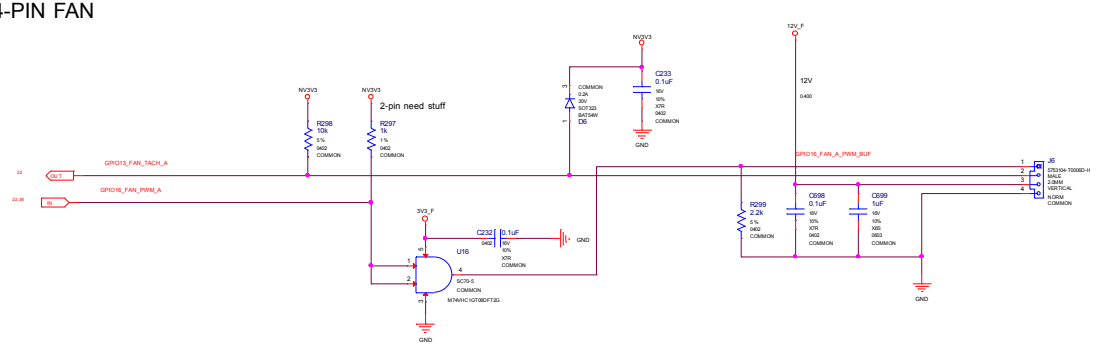
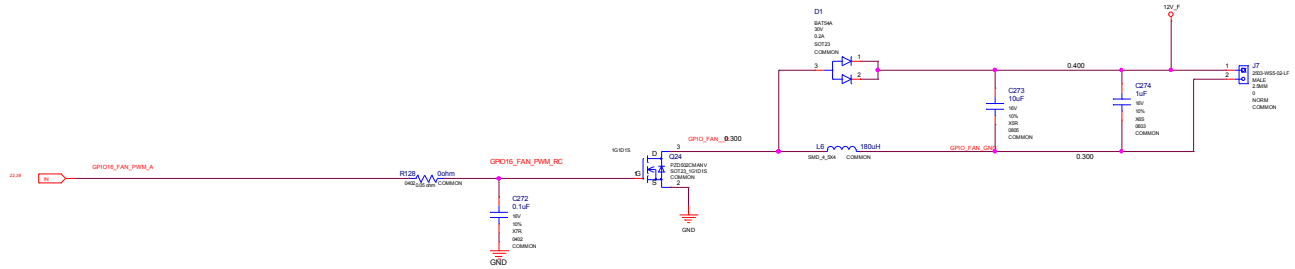
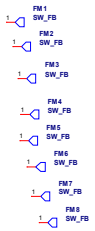
Page38: FAN

4-PIN FAN



2-PIN FAN





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PAGE DETAIL	FAN

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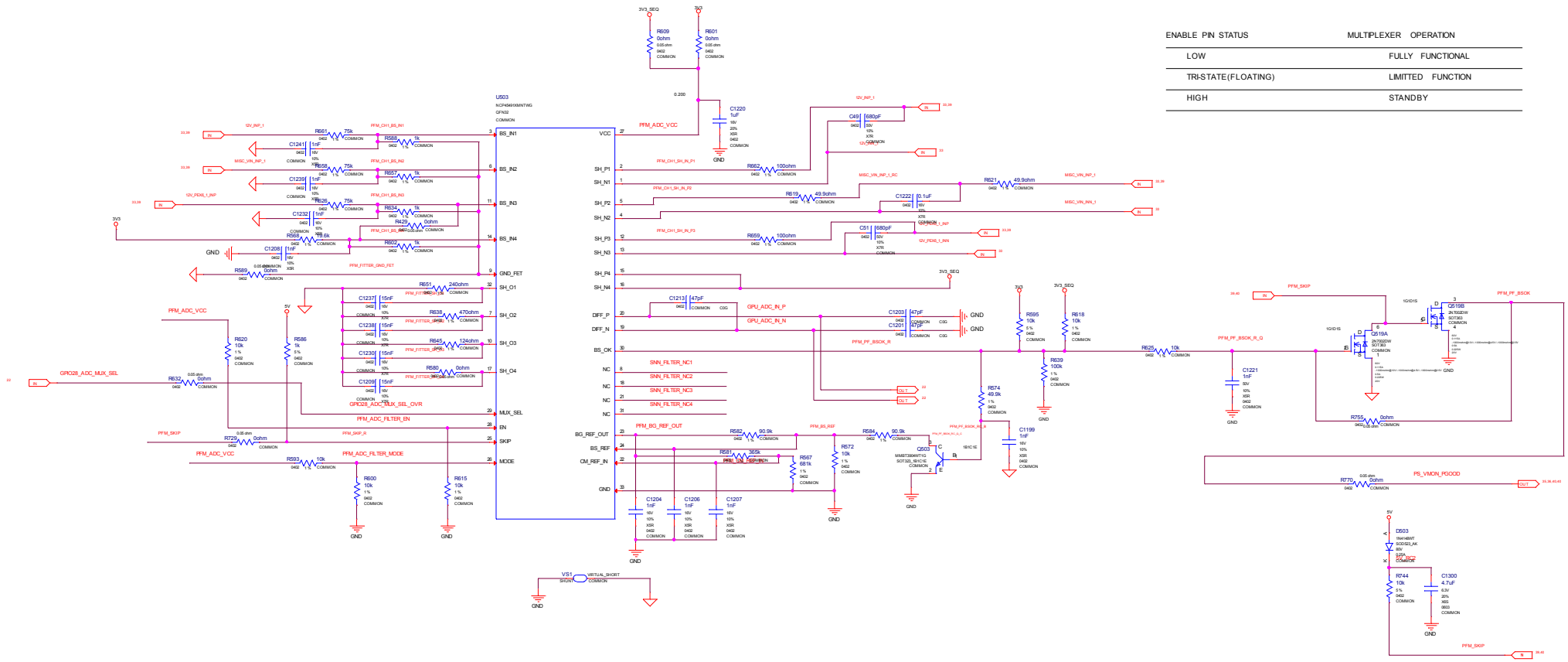
Page39: OVRM_PWR SENSE

MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITTED FUNCTION
HIGH	STANDBY



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PAGE DETAIL	PS: OVRM_PWR SENSE

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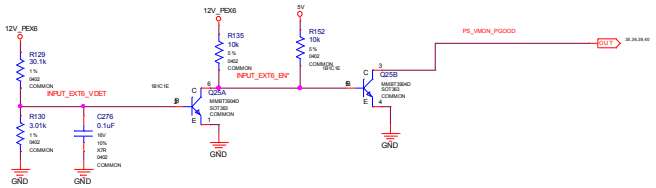
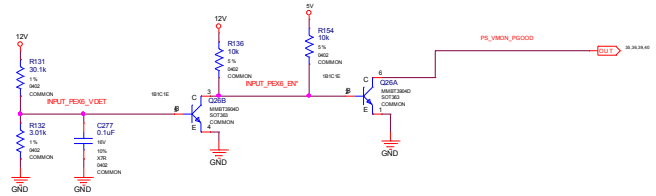
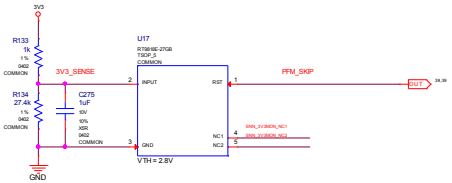
PAGE40:SEQUENCE:Voltage Monitor





Route the trace to PEX Golden Finger



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS:Voltage Monitor

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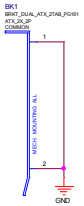
Page41: MECH

Bracket:



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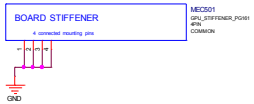

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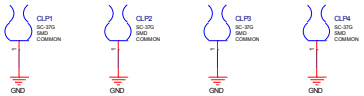

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MECH

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