PG160-B02

8GB GDDR6, 256b, X16
Tall DVI-D + USBC/DP + DP + HDMI/DP + DP

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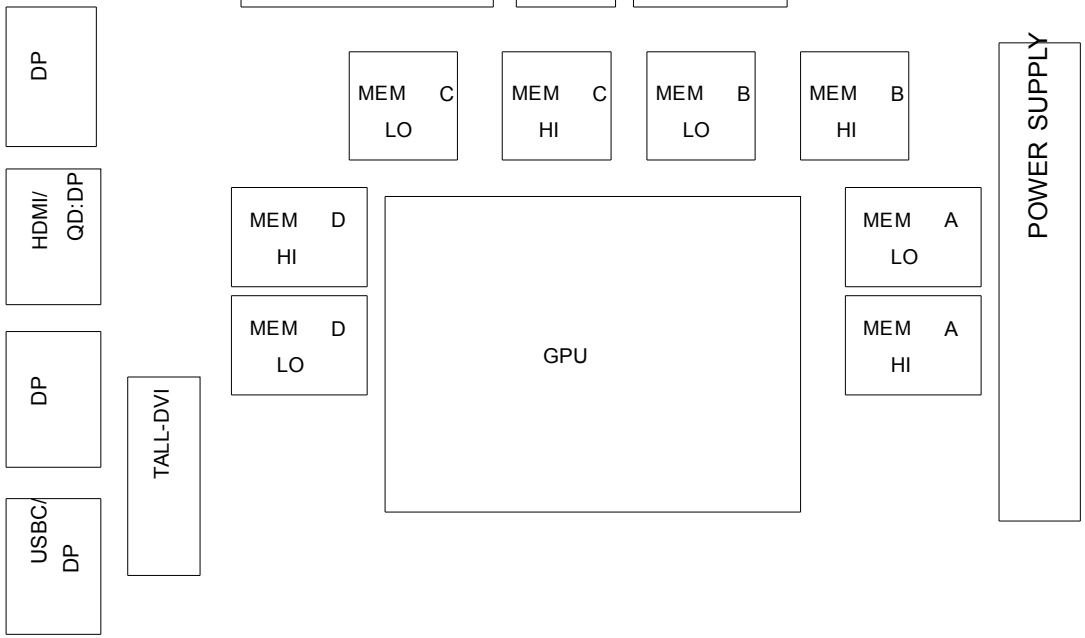

Power Supply:

- Power Supply NVVDD-PH6
- Power Supply NVVDD-PH5
- Power Supply NVVDD-PH4 → EXT_12V 2x3/4 PWR
- Power Supply NVVDD-PH3
- Power Supply NVVDD-PH2 → SW
- Power Supply NVVDD-PH1
- Power Supply FBVDDQ-PH2 → PEX_12V Finger
- Power Supply FBVDDQ-PH1 → SW
- Power Supply 5V
- PEX_VDD → SW → 3V3_A
- 1V8
- USB Open_Vreg option
- Fan → PEX_12V Finger, EXT_12V 2x3/4 PWR
- DP_PWR → 3V3 Finger

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Page3: PCI Express

add 12V_BUS Fuse

delete SMBUS

delete PEX_WAKE*

delete 3V3_AUX_CON MLCC

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
12V	12V	5.5A	0.406
3V3	3.3V	3.0A	0.400
GND	0V	8.5A	0.300

Place under GPU

Place between GPU and PS

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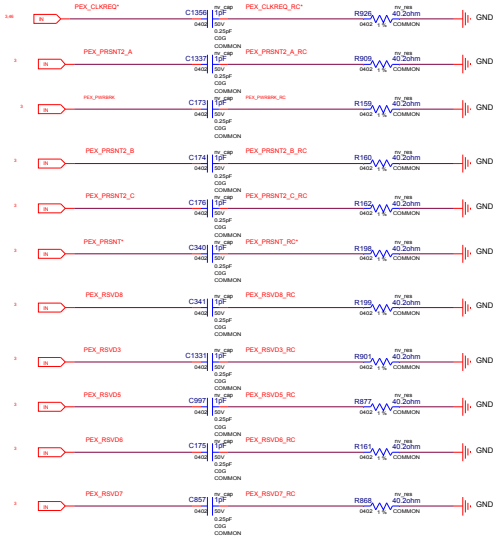
Page4: PCIE RC TERM



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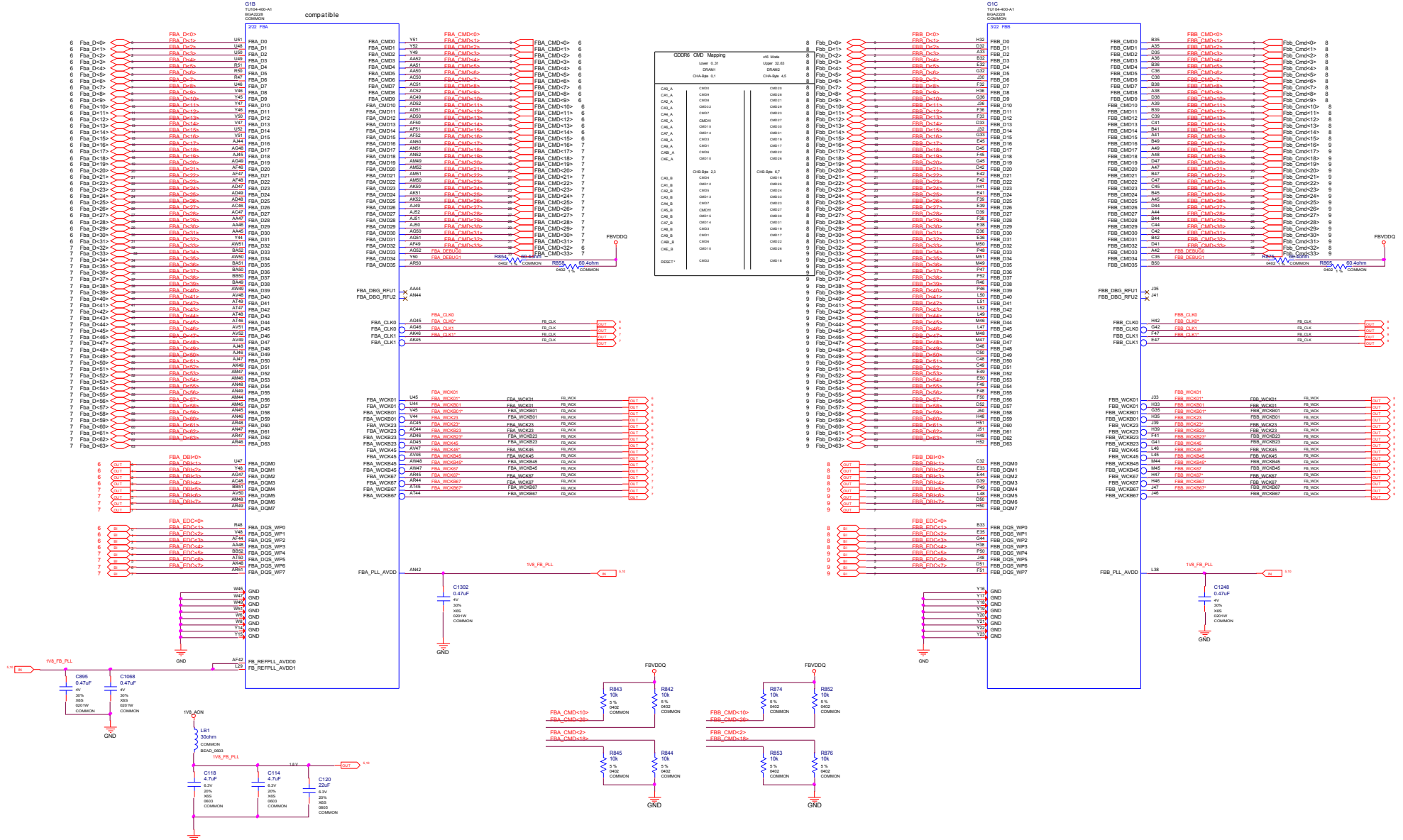
Page5: MEMORY: GPU Partition A/B



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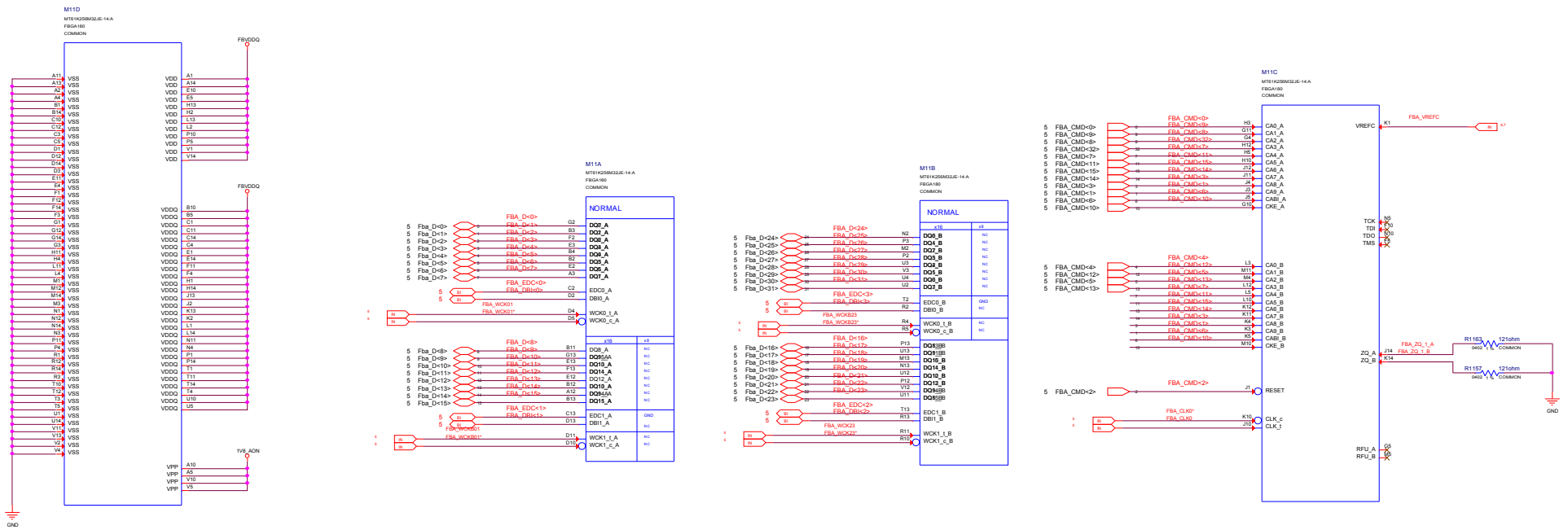
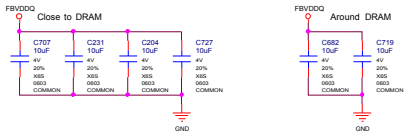
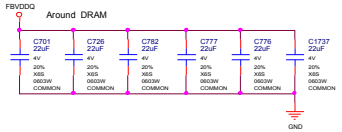
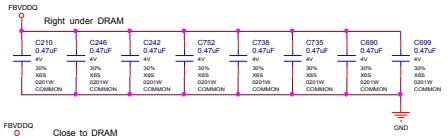
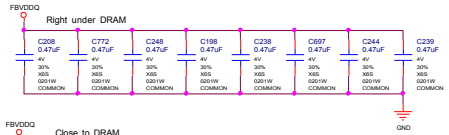
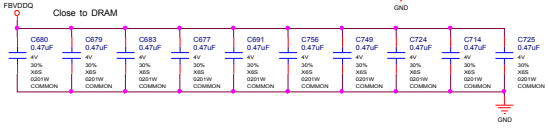


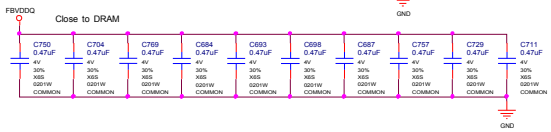




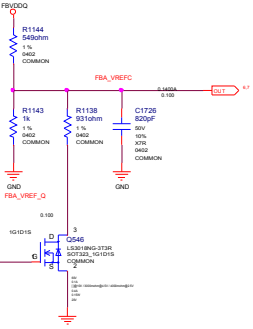


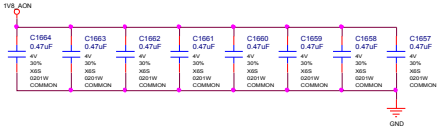






VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR R106





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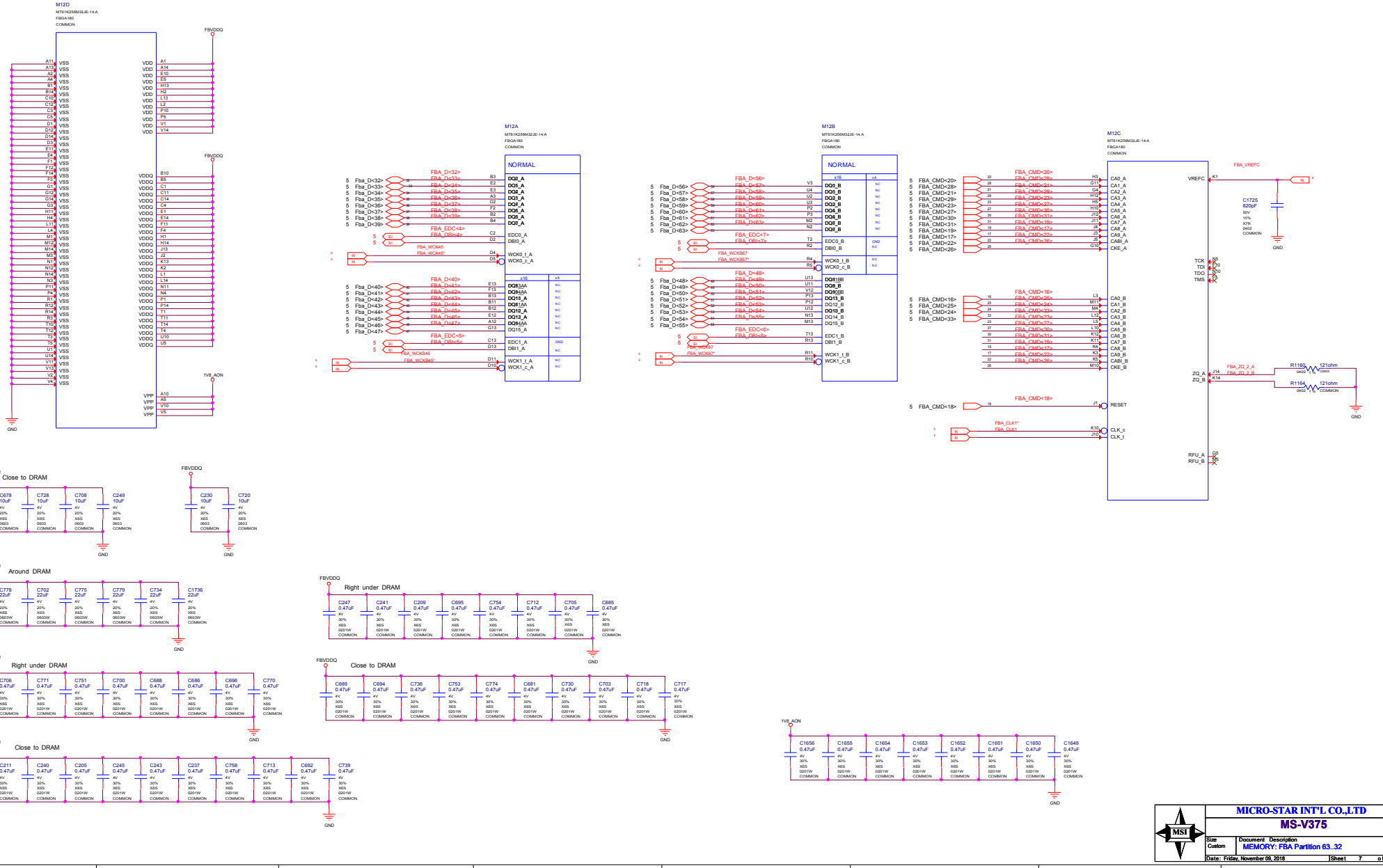
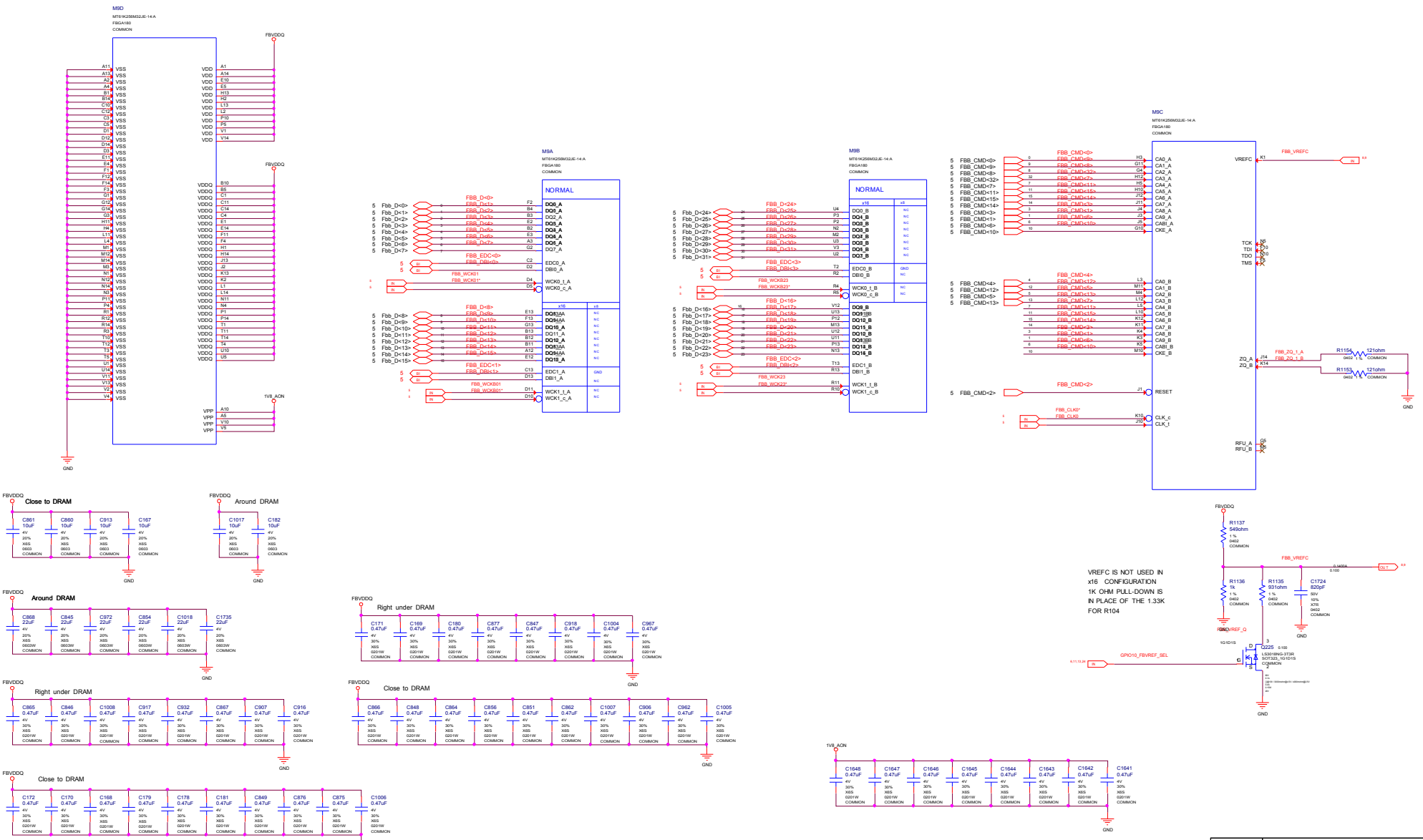
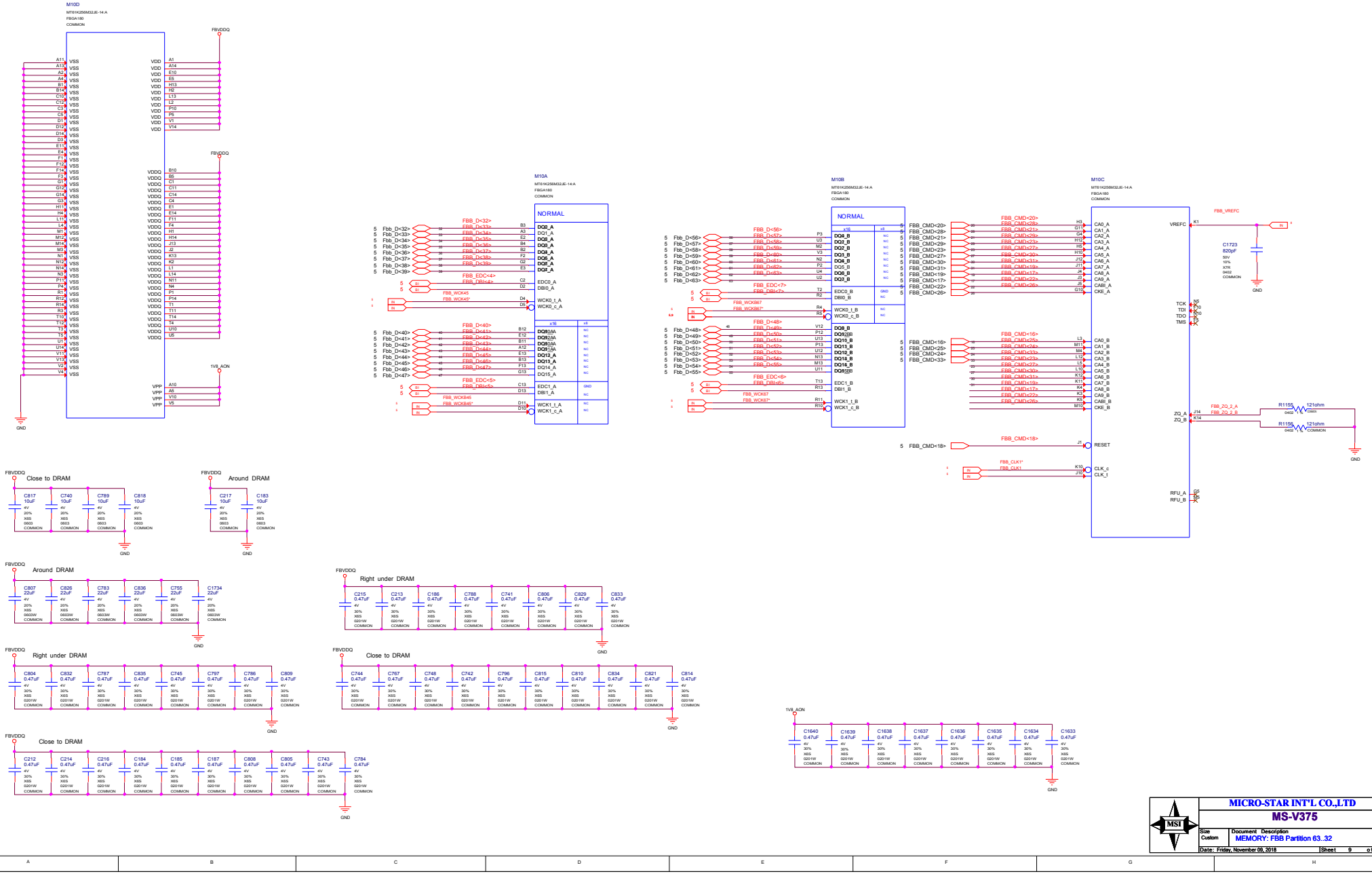


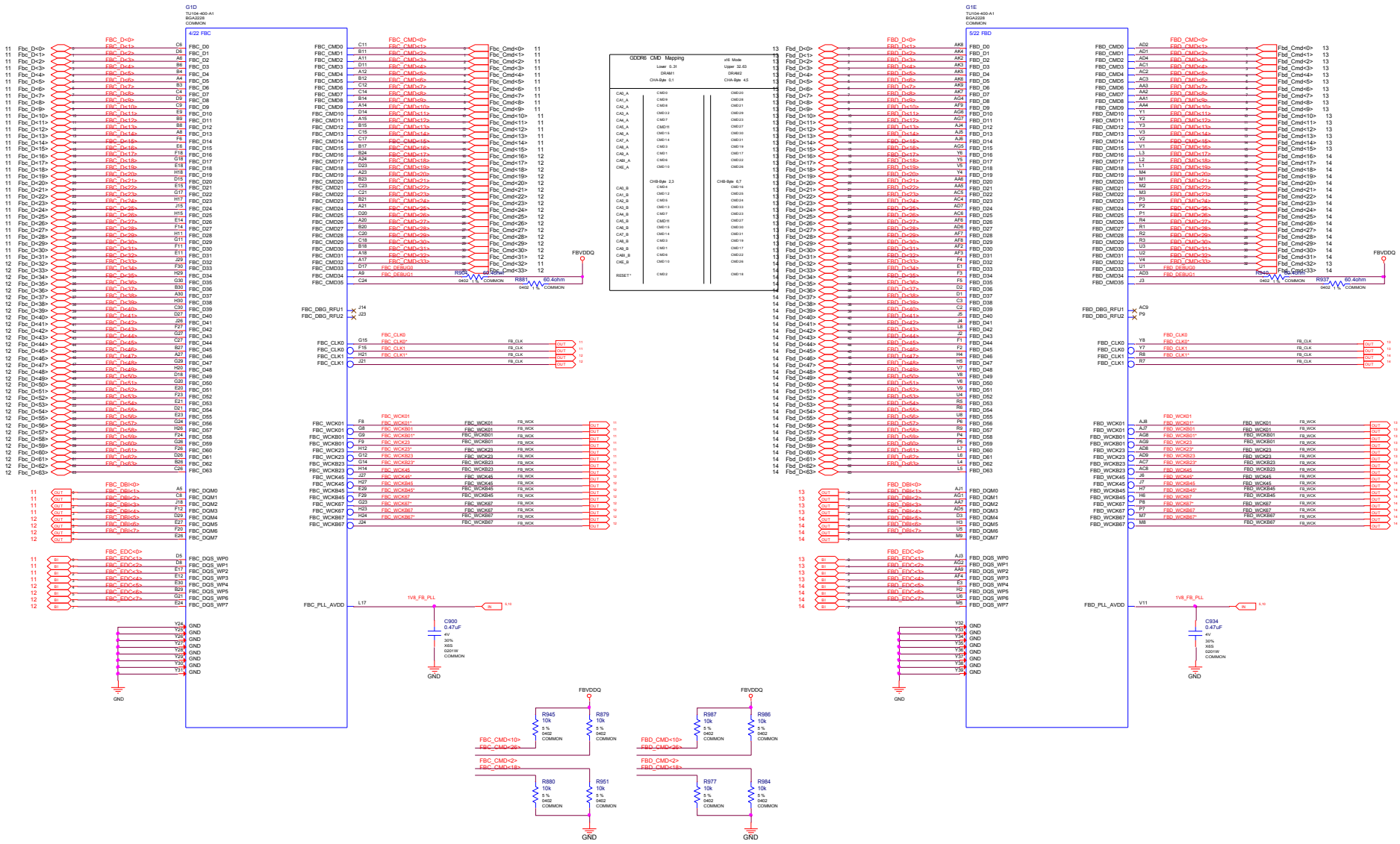
Page8: MEMORY: FBB Partition 31..0



Page9: MEMORY: FBB Partition 63..32



Page10: MEMORY: GPU Partition C/D



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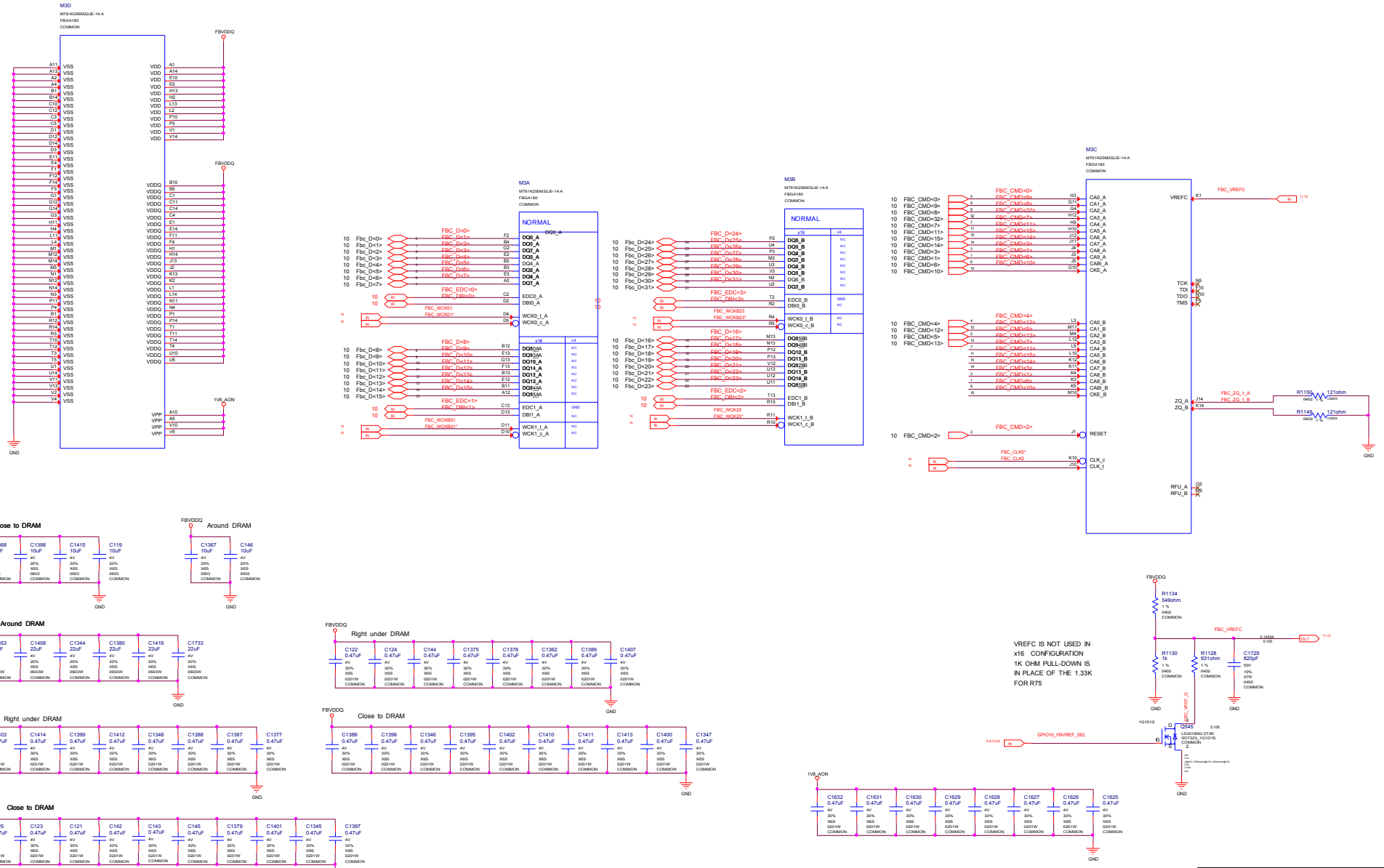

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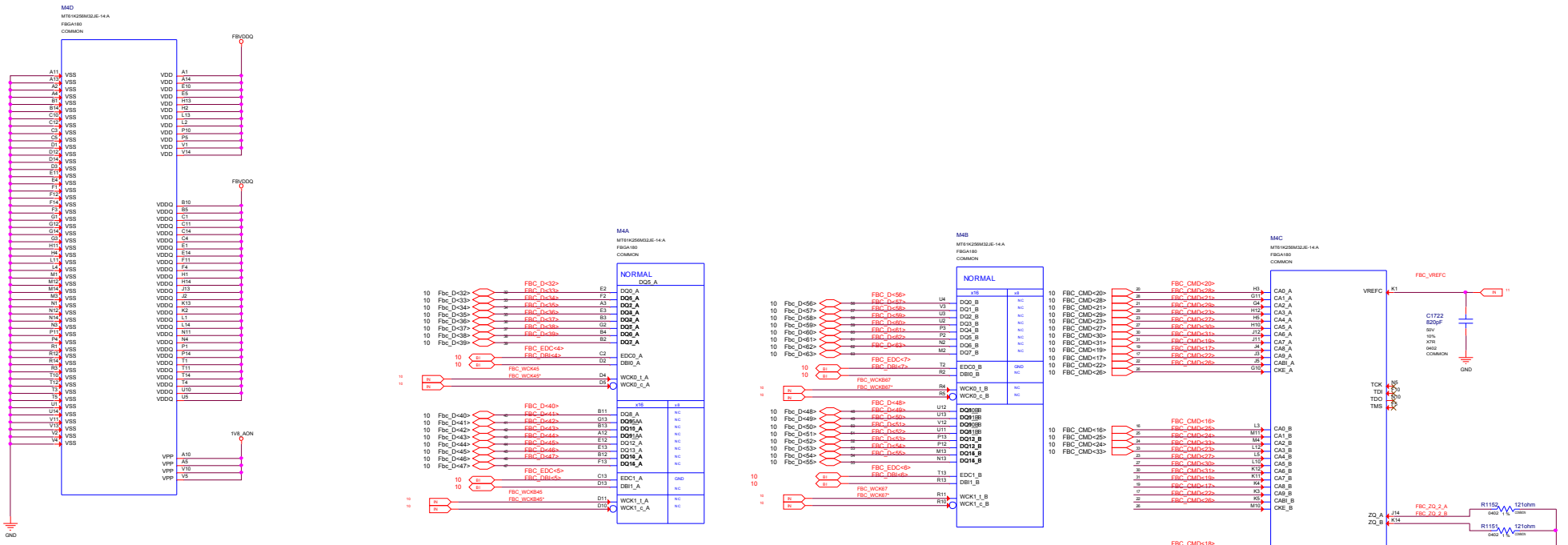

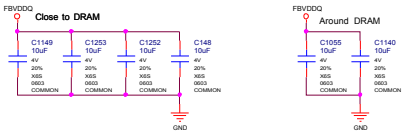

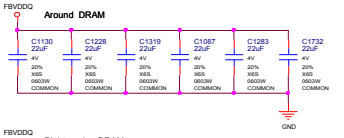

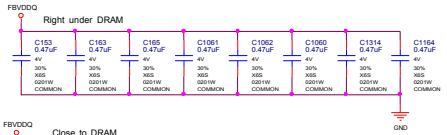

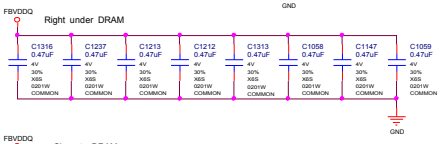

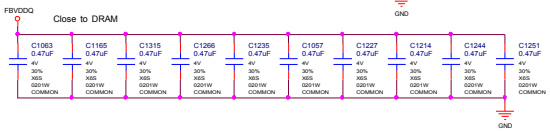

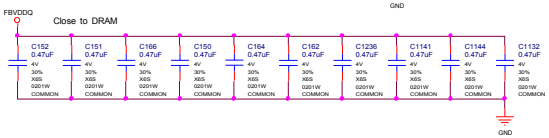

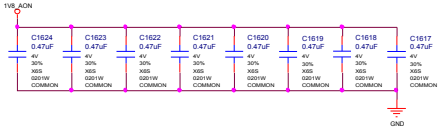

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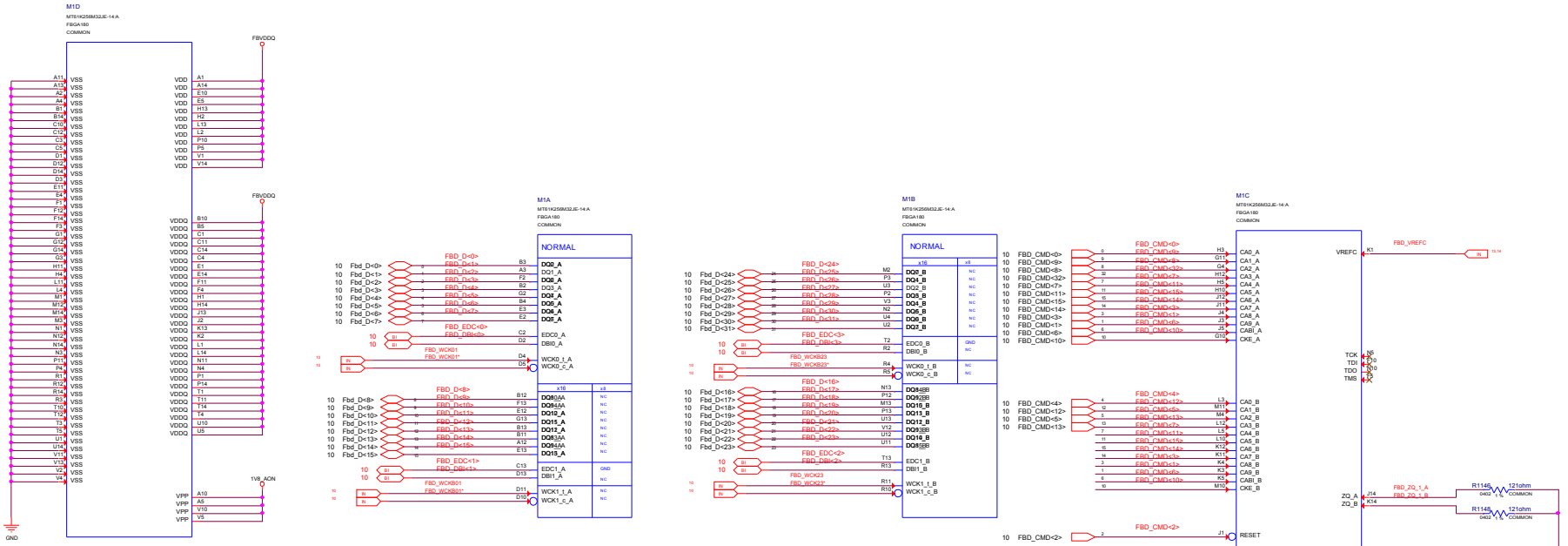
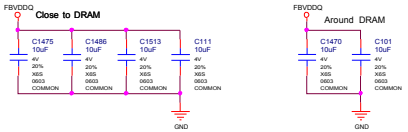
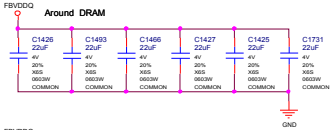
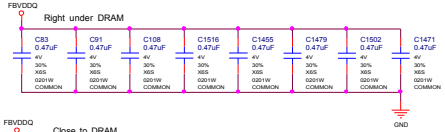
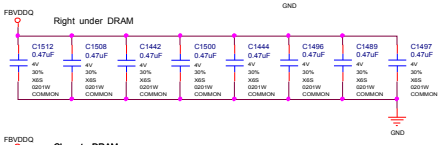
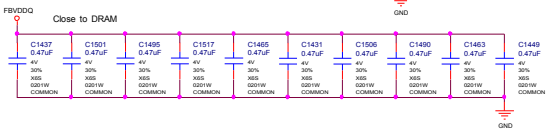


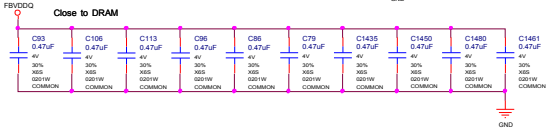




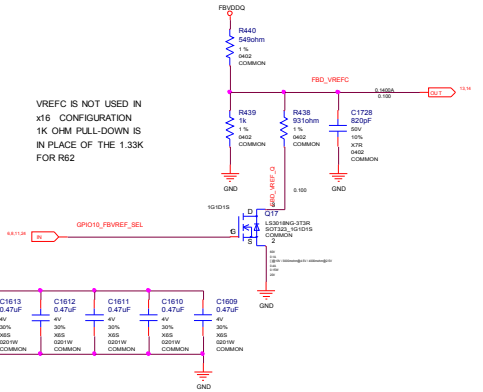








VREFC IS NOT USED IN x16 CONFIGURATION 1K OHM PULL-DOWN IS IN PLACE OF THE 1.33K FOR R62



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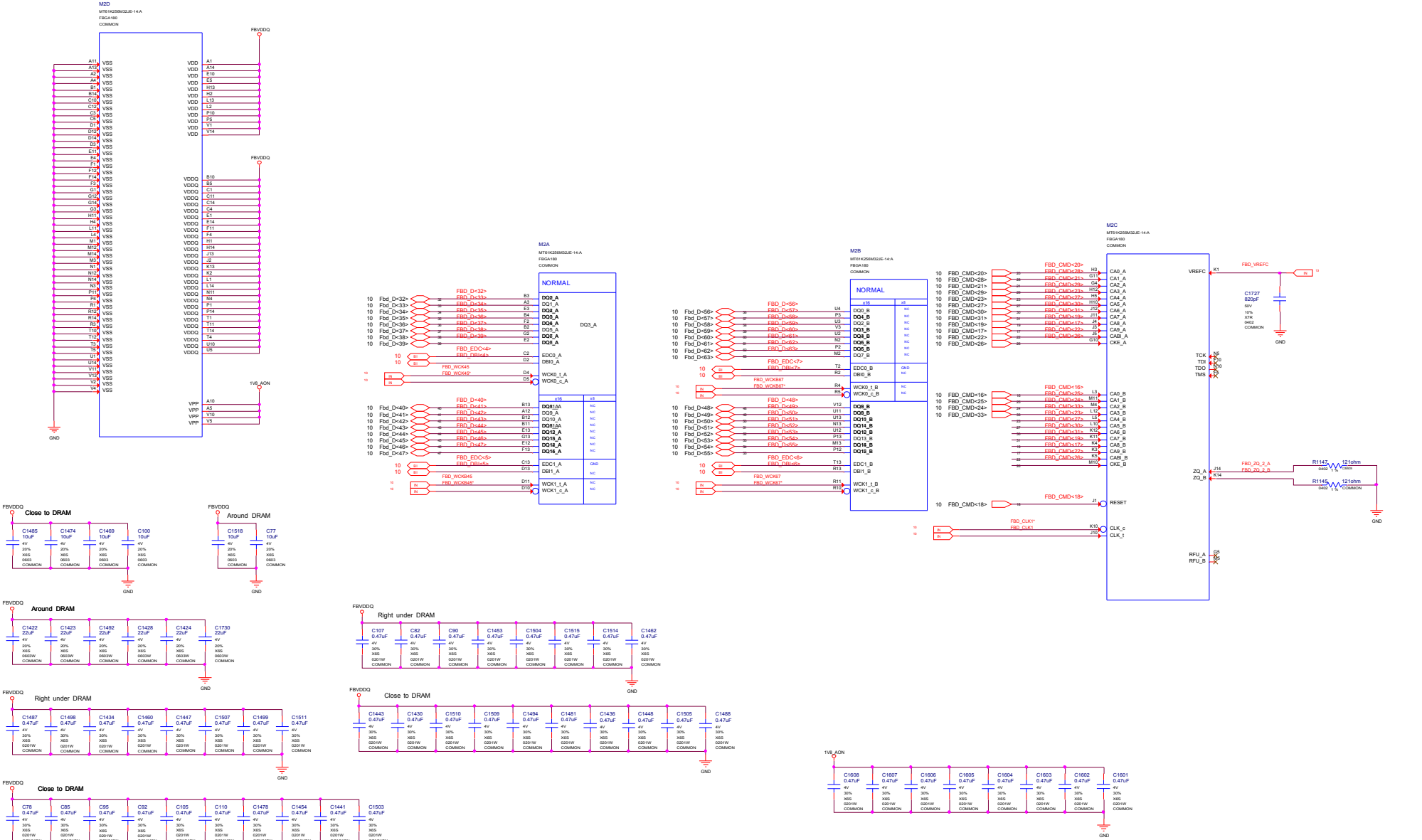

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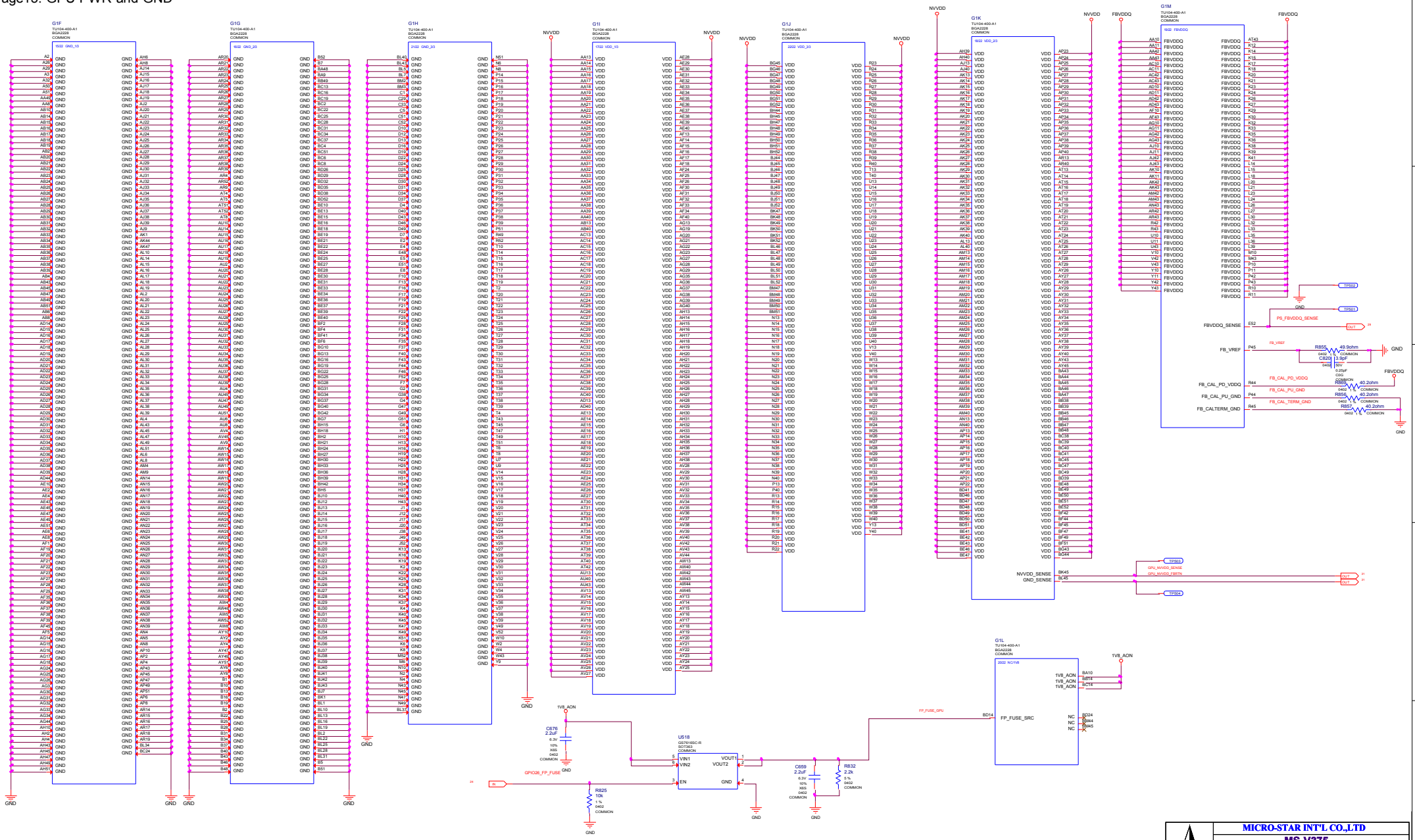
Page15: GPU PWR and GND



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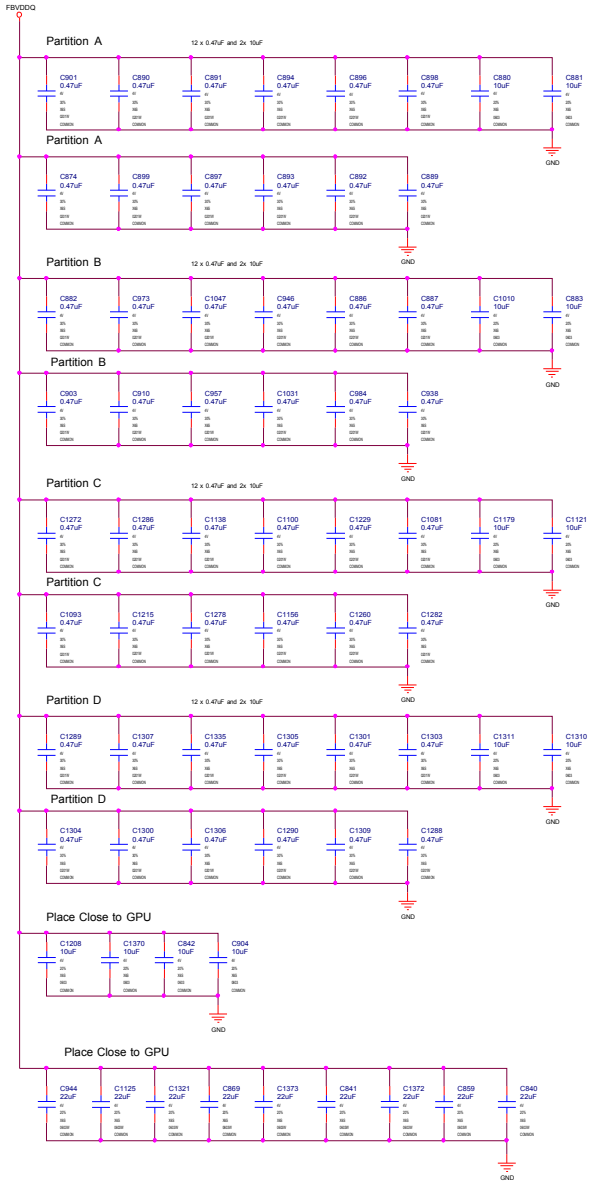
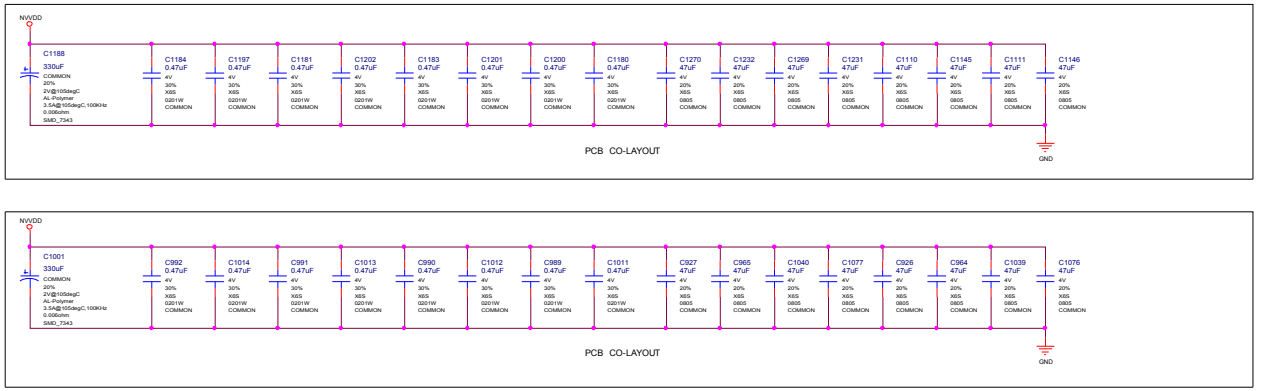
Page16: GPU Decoupling 1

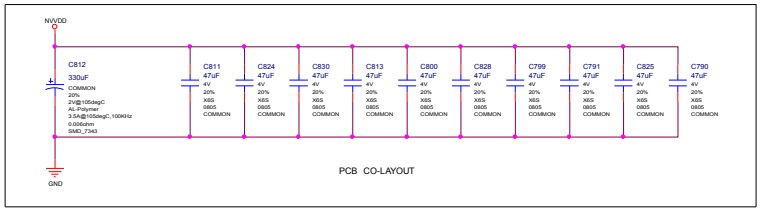
FBVDDQ

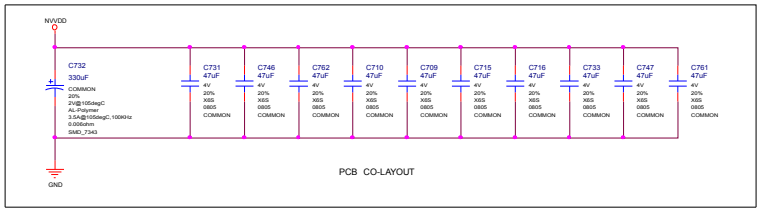


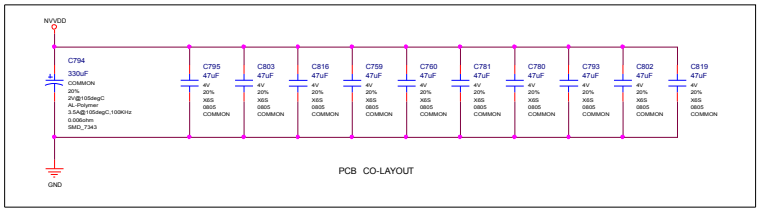
Under GPU



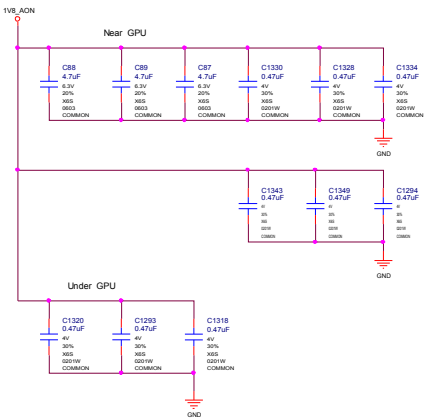
Near GPU







1V8_AON



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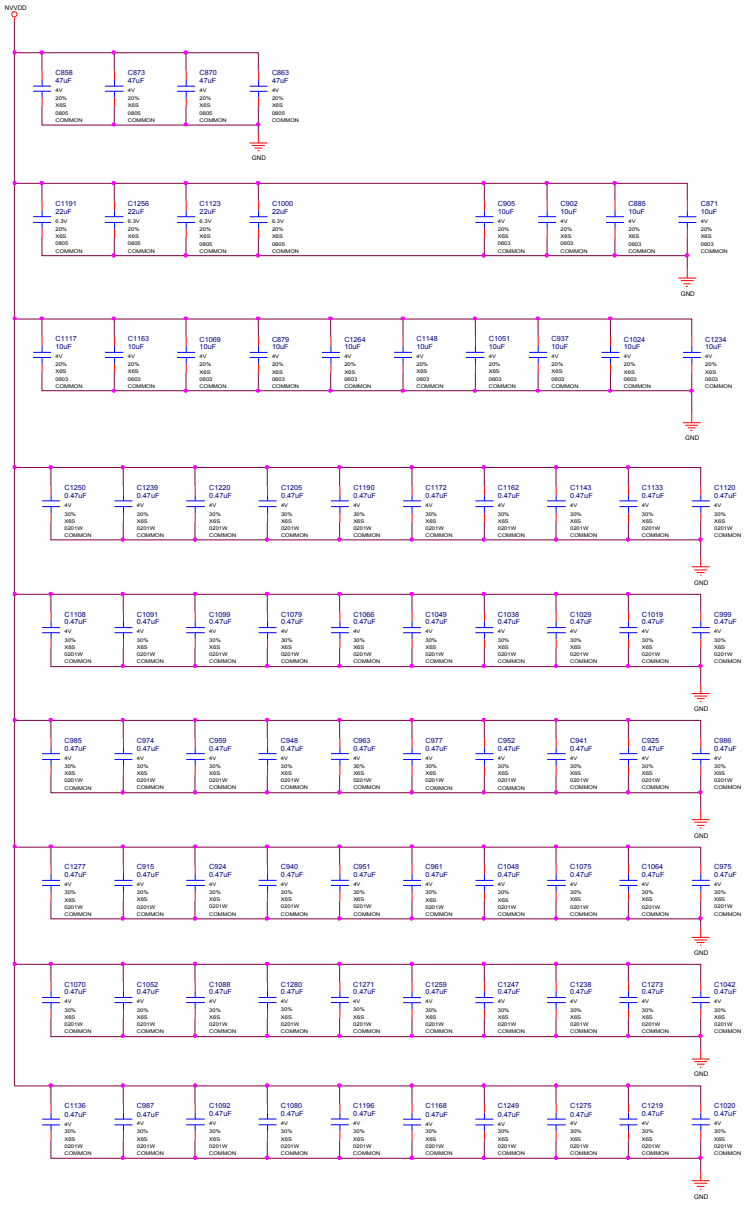
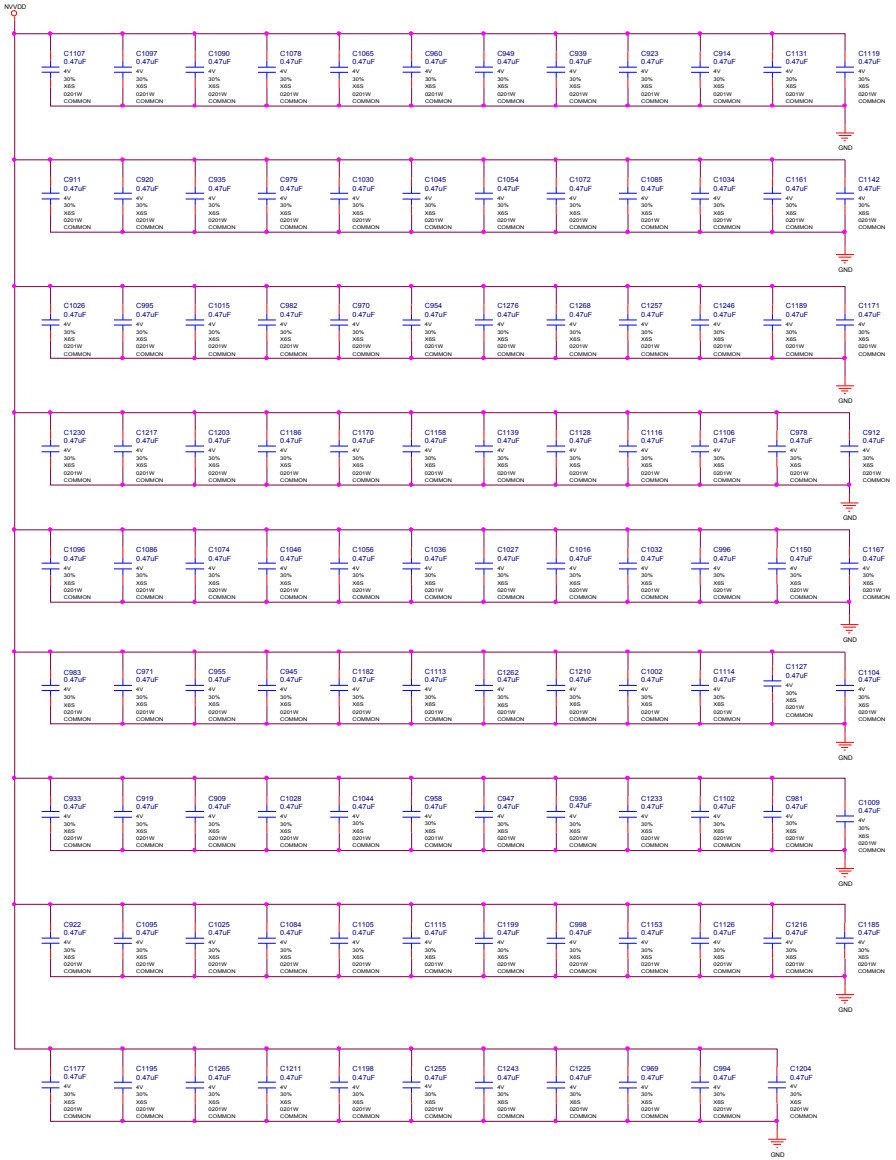
Page17: GPU Decoupling 2

NVVDD





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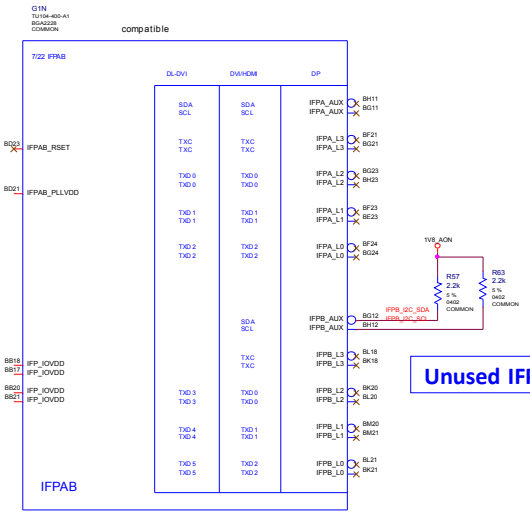
delete Link AB ◦



Unused IFPB_I2C* leaving Pull high resistor to 1.8V ◦

9.3 UNUSED PINS

If an IFP link is unused, in general it should be left unconnected. This includes Main and Aux links. IFPxy_RSET and IFPxy_PLLVDD (xy=AB,CD,EF) can be left unconnected if neither of IFPx /IFPy is in use. For example, If neither link of the IFPA/IFPB macro is to be used, then IFPAB_PLLVDD and IFPAB_RSET should be left disconnected, and all signals and references associated with Link A and Link B should also be left unconnected.

IFP_IOVDD rail can be unconnected if no IFP link is used.If any IFP is used, all IFP_IOVDD balls must be connected to power rail.

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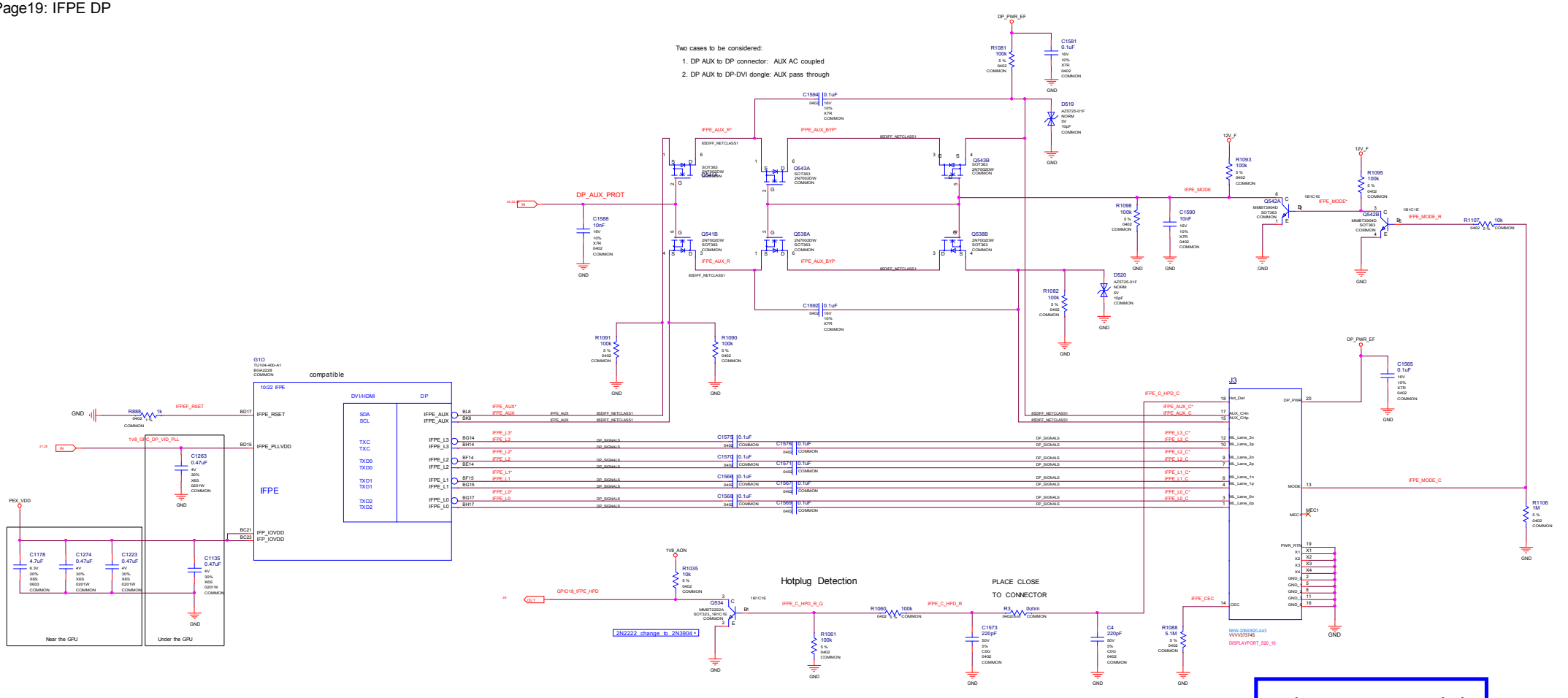

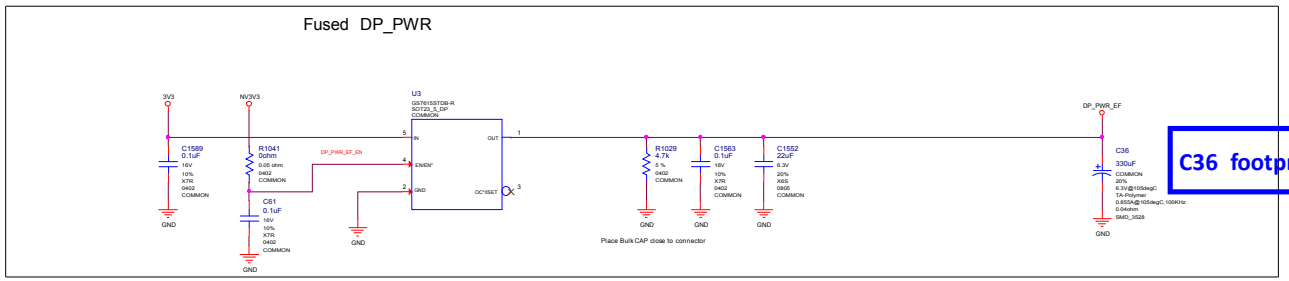

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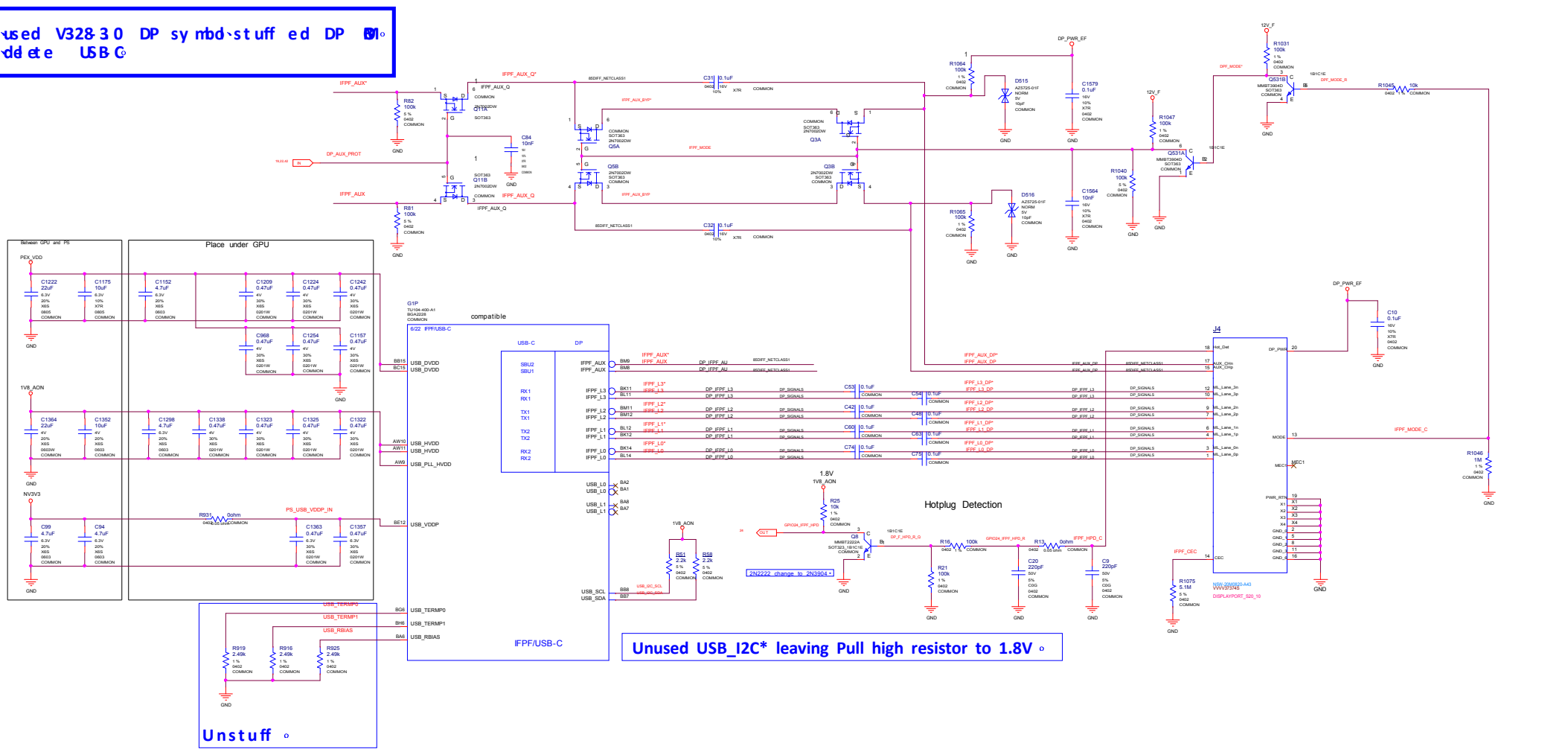
Page20: IFPF USB-C

1 Used V328-30 DP symbol stuff ed DP MI
2 Add ete USB C



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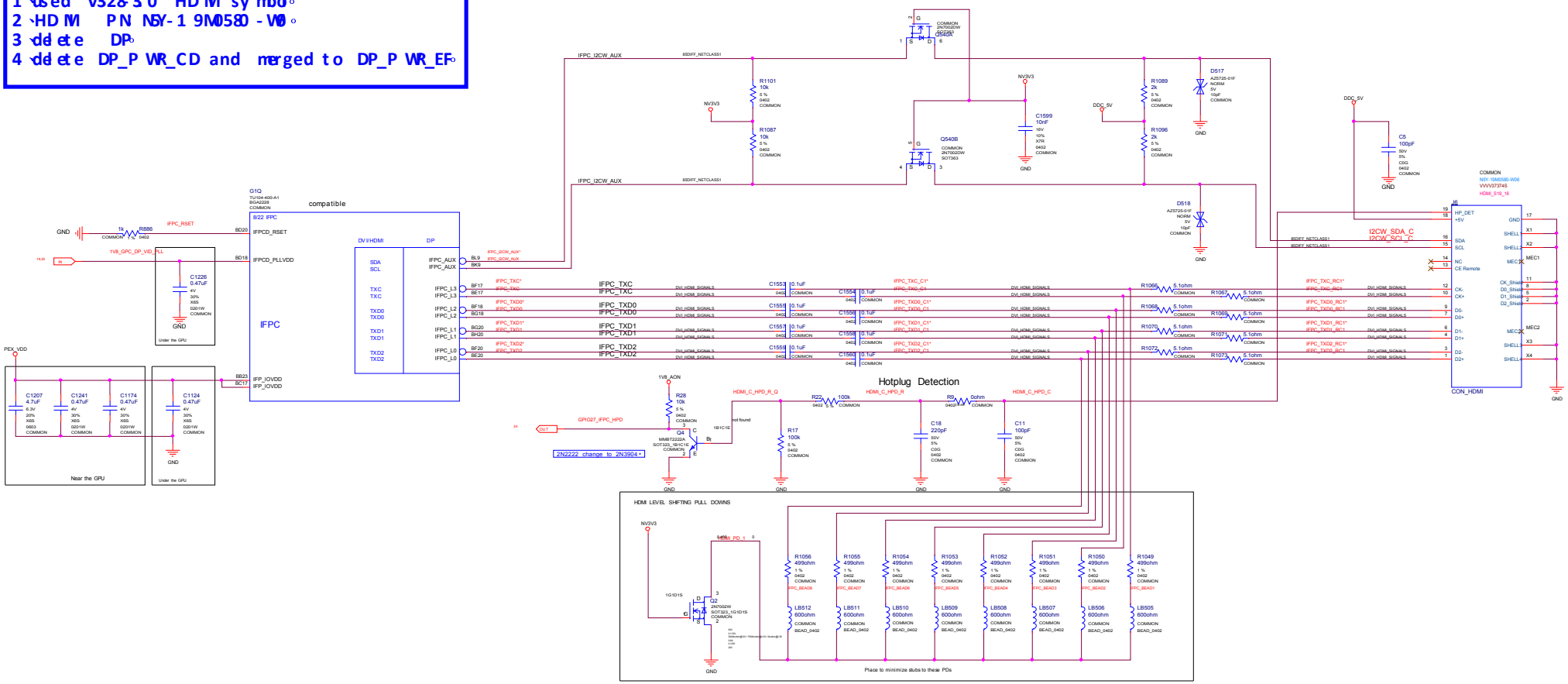
Page21: IFPC HDMI/DP

1. used V328-30 HDMI symbol.
2. HDMI PN NSY-19M058D-W0.
3. delete DP.
4. delete DP_PWR_CD and merged to DP_PWR_EF.



Page22: IFPD DP

merged to DP_PWR_EF ◦

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through

merged to DP_PWR_EF ◦

used V328-3.0 DP symbol ◦

Hotplug Detection

compatible

Under the GPU

MICRO-STAR INT'L CO.,LTD		
MS-V375		
Size: Custom	Document Description: IFPD DP	Rev: 4.0
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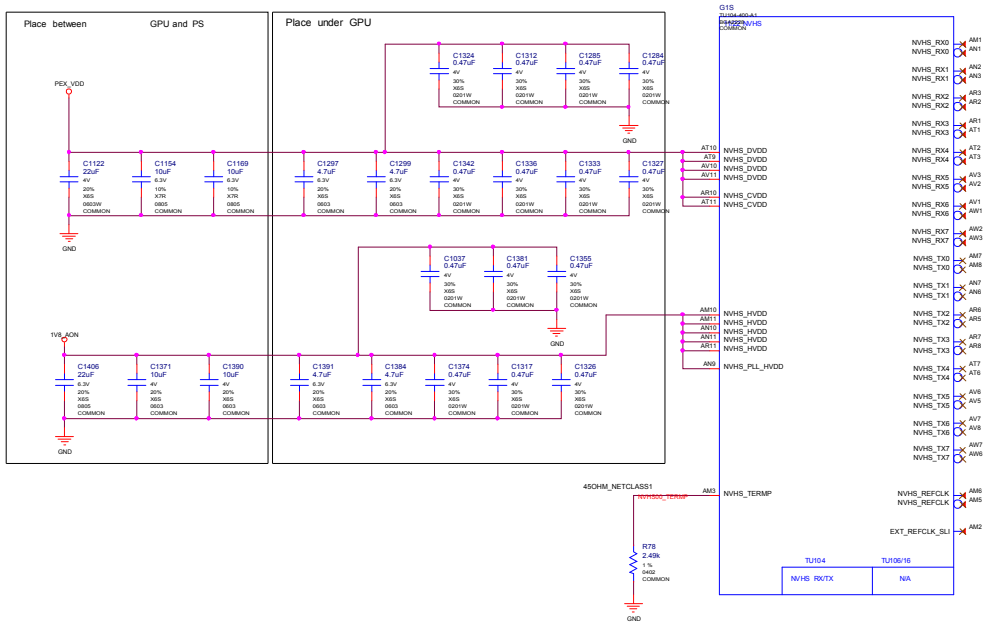
Page23: NVHS Interface and Frame Lock



delete Frame Lock。

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V375	
Size: Custom	Document Description: NVHS Interface	Rev: 4.0
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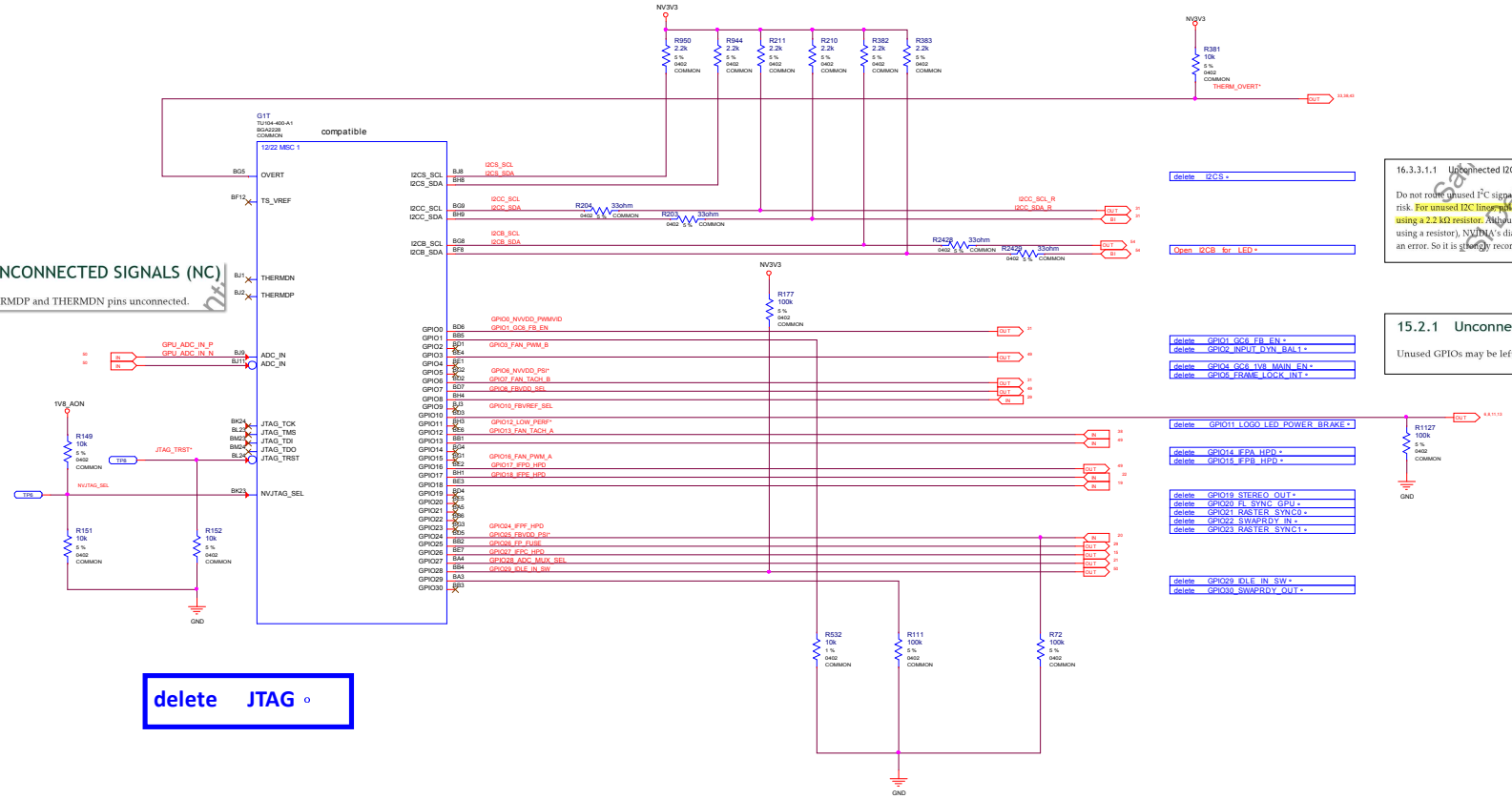
Page24: MISC1: Fan, Thermal, JTAG, GPIO



14.5 UNCONNECTED SIGNALS (NC)

Leave the THERMDP and THERMDN pins unconnected.

16.3.3.1.1 Unconnected I2C Pins

Do not route unused I²C signals on the PCB in order to protect the GPU from outside ESD risk. For unused I2C lines, pull up both the I2Cx_SCL and I2Cx_SDA lines to 1.8V or 3.3V, using a 2.2 kΩ resistor. Although unused I2C lines can be soft-grounded (that is, grounded using a resistor), NVDIA's diagnostic program expects them to be pulled up and will flag an error. So it is strongly recommended that unused I2C lines be pulled up.

15.2.1 Unconnected Signals

Unused GPIOs may be left floating (NC) on the board design.

delete JTAG ◦

Unused delete STEREO ◦

Unused delete GPIO11_LOGO_LED_POWER_BRAKE ◦

MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: MISC: Fan, Thermal, JTAG, GPIO, STEREO	Rev: 4.0
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Page25: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	DEFAULT
L	L	L	0	0	0	0	

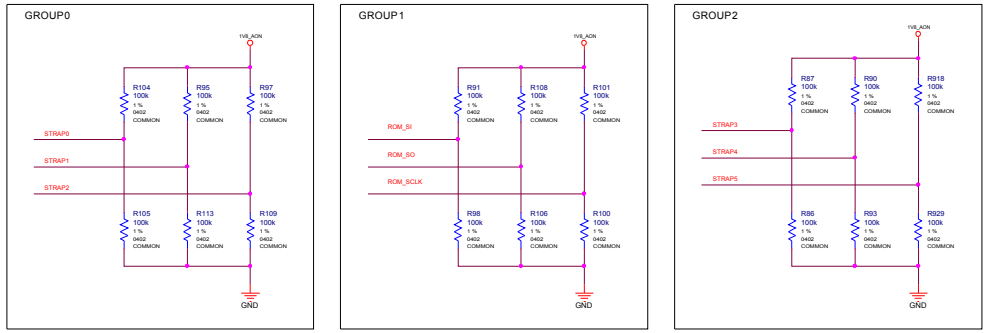
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

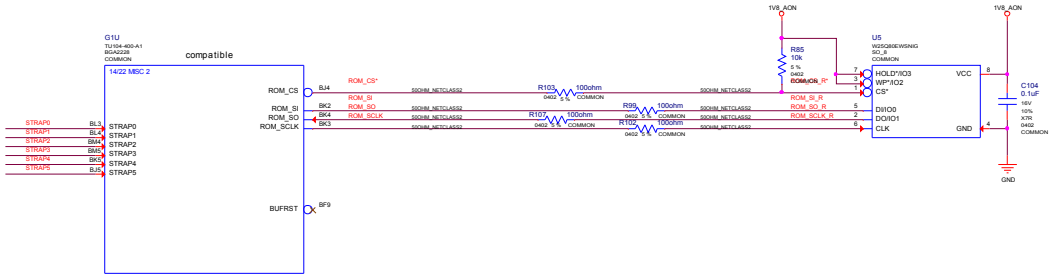
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

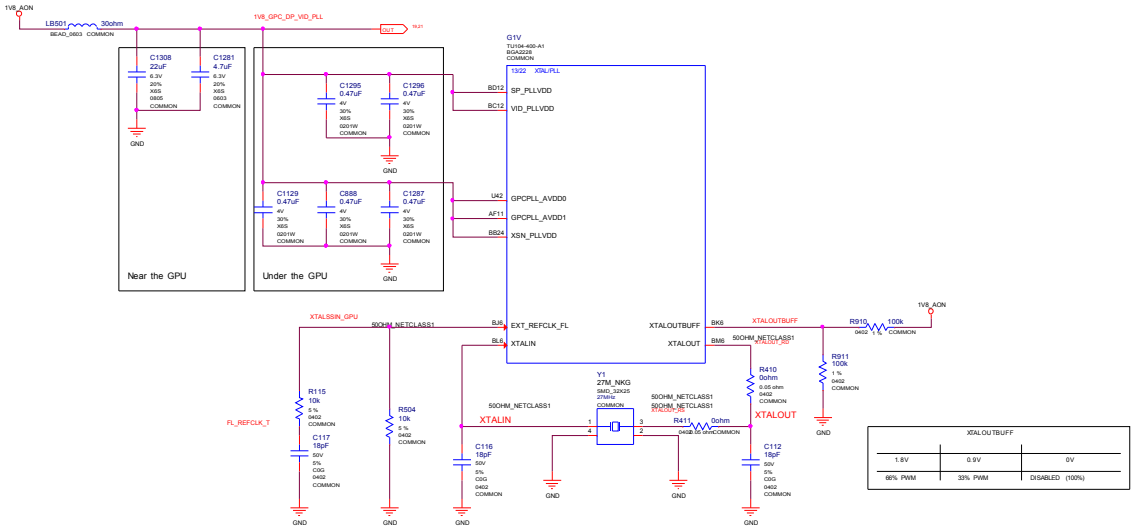
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE







MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: MISC: ROM, Straps	Rev: 4.0
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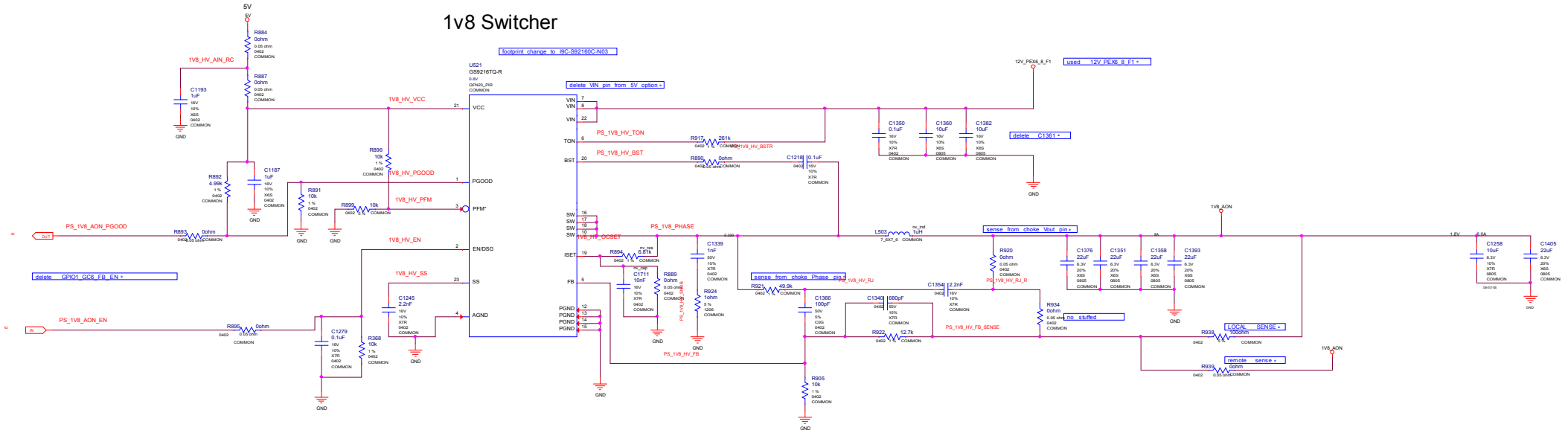
Page26: PS: 1V8 PLL, 1V8_AON



1 L503 PN L04-010740-L65 / footprint : CHK_S2_7_3X6_61
2 delete colayout PWM ouput choke
3 delete 1V8_MAIN and merged to 1V8_AON

MICRO-STAR INT'L CO.,LTD		
MS-V375		
Size: Custom	Document Description: PS: 1V8 PLL, 1V8_AON	Rev: 4.0
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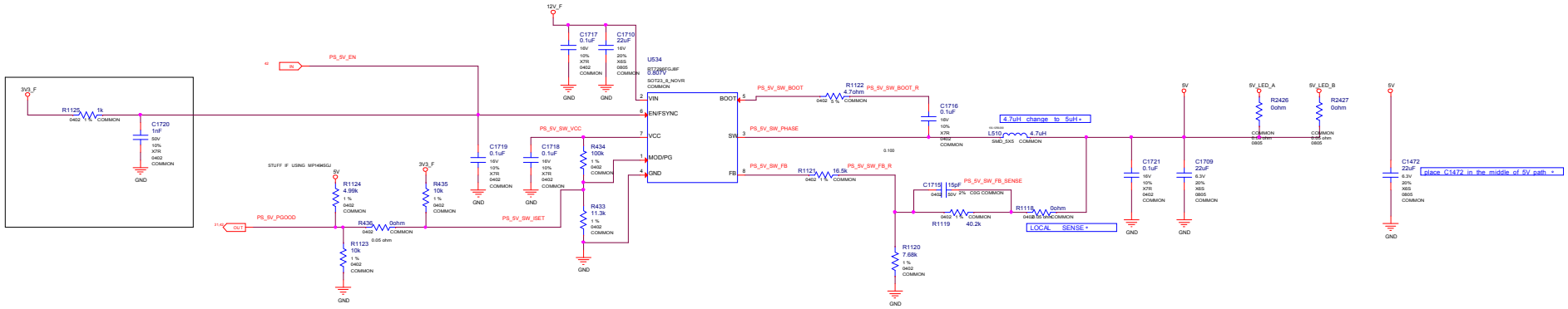
Page27: PS: 5V

1 L510 P/N L04-0507010-L65 / footprint : CHK_S2_5_4X5_23
2 delete colayout PWM ouput choke.
3 unused RTD3 delete Buck-Boost regulator.



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	MS-V375	
Size: Custom	Document Description: PS: 5V	Rev: 4.0
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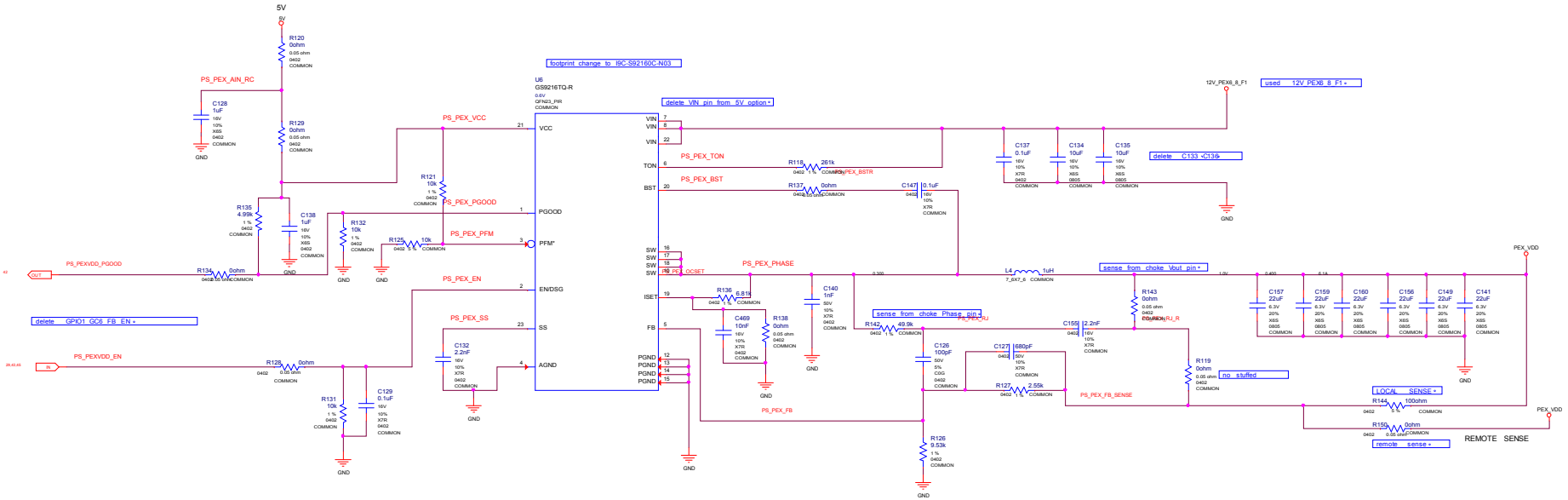
PEX Switcher



1 L4 PN L04-010740-L65 / footprint : CHK_S2_7_3X6_61
2 delete colayout PWM ouput choke

MICRO-STAR INT'L CO.,LTD		
MS-V375		
Size: Custom	Document Description: PS: PEXVDD	Rev: 4.0
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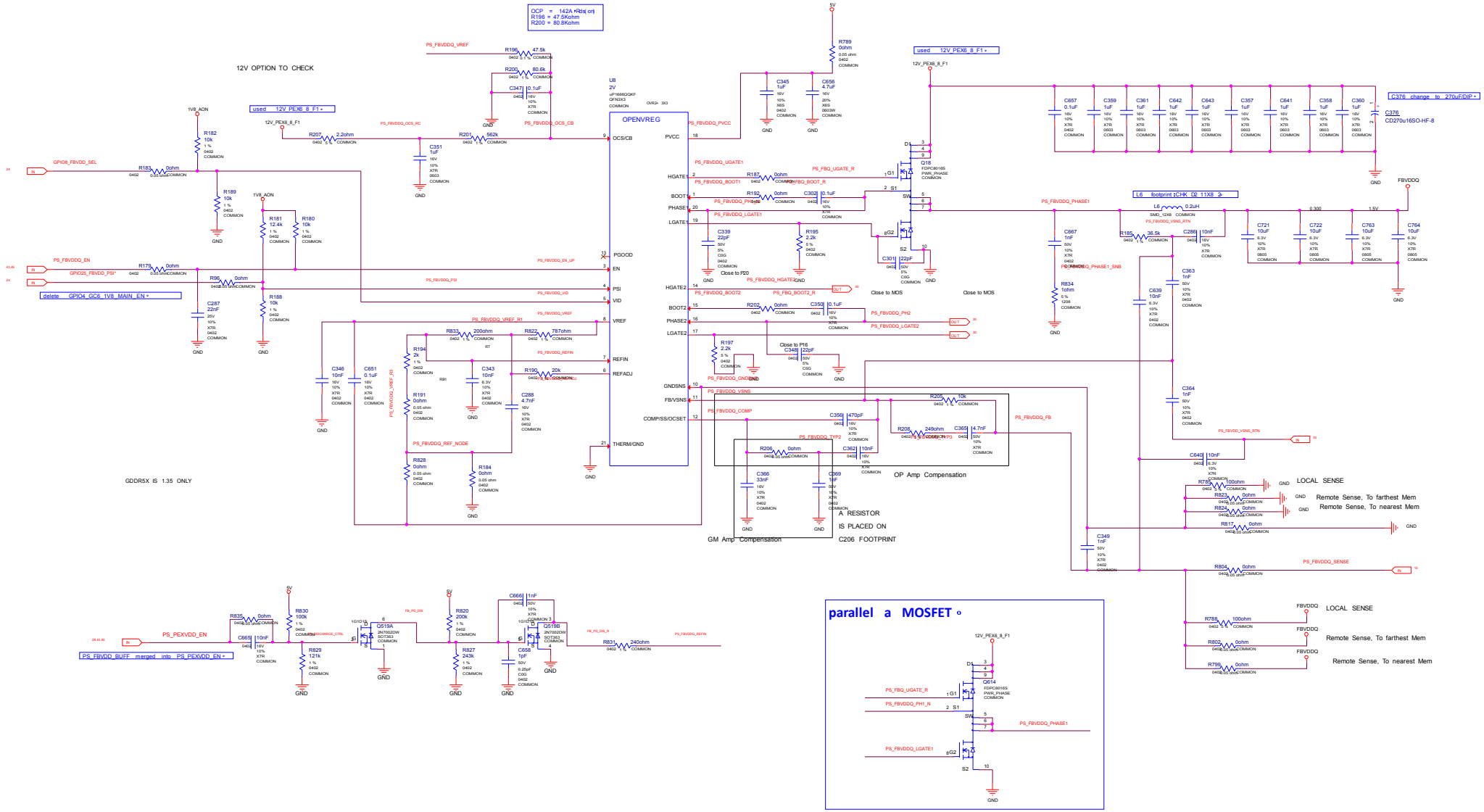
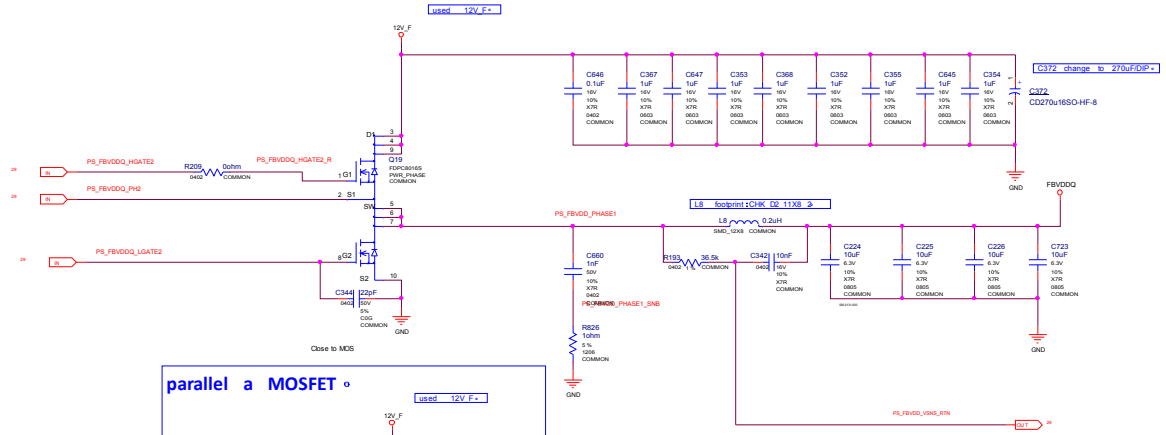
Page29: PS: FBVDDQ

2. OPTION TO CONNECT FBVDD+FBVDDQ



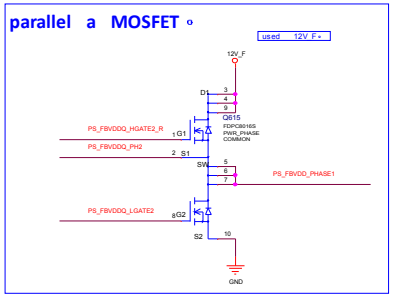
MICRO-STAR INT'L CO.,LTD	
MS-V375	
Size: Custom	Document Description: PS: FBVDDQ
Rev: 4.0	
Date: Friday, November 09, 2018	Sheet 29 of 54

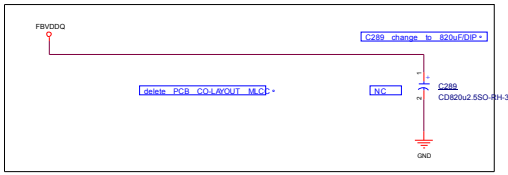
Page30: PS: FBVDDQ PH2

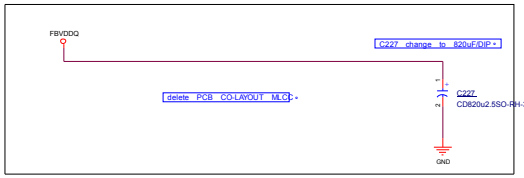


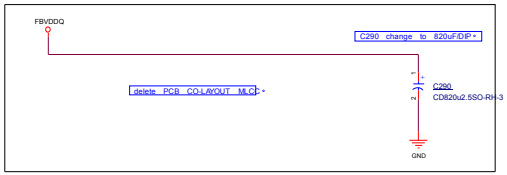
delete RTD3 backdrive

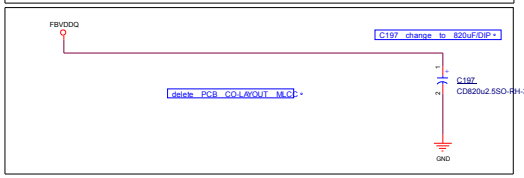
parallel a MOSFET

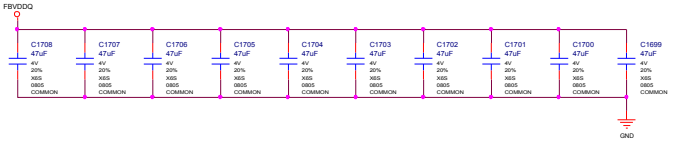












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Size	Document Description	Rev
Custom	PS: FBVDDQ PH2	4.0

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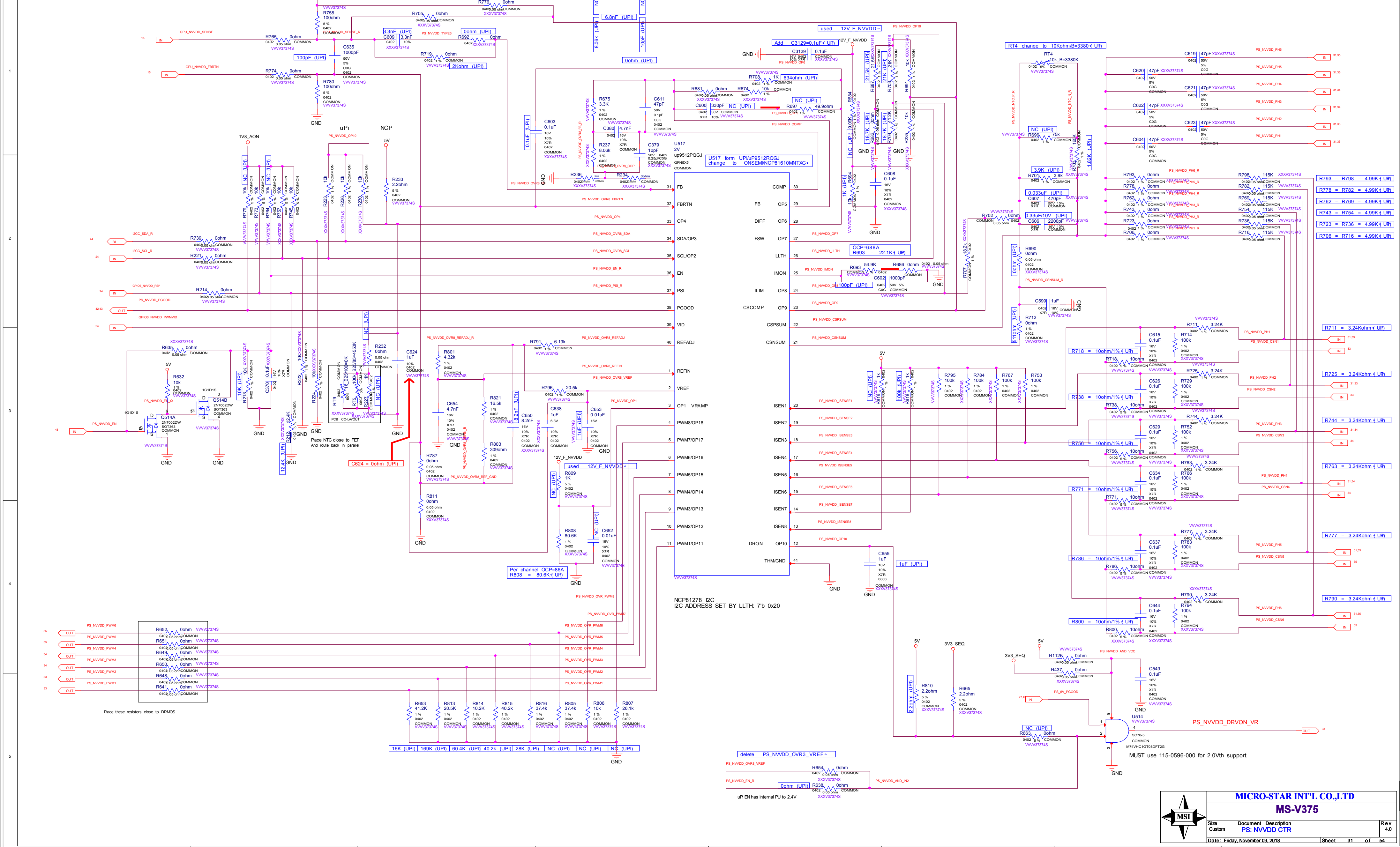
Page31: PS: NVVDD CTR



Page32: PS: NVVDD CTR OVR3i

delete all unused

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Size	Document Description	Rev
Custom	PS: NVVDD CTR OVR3i	4.0

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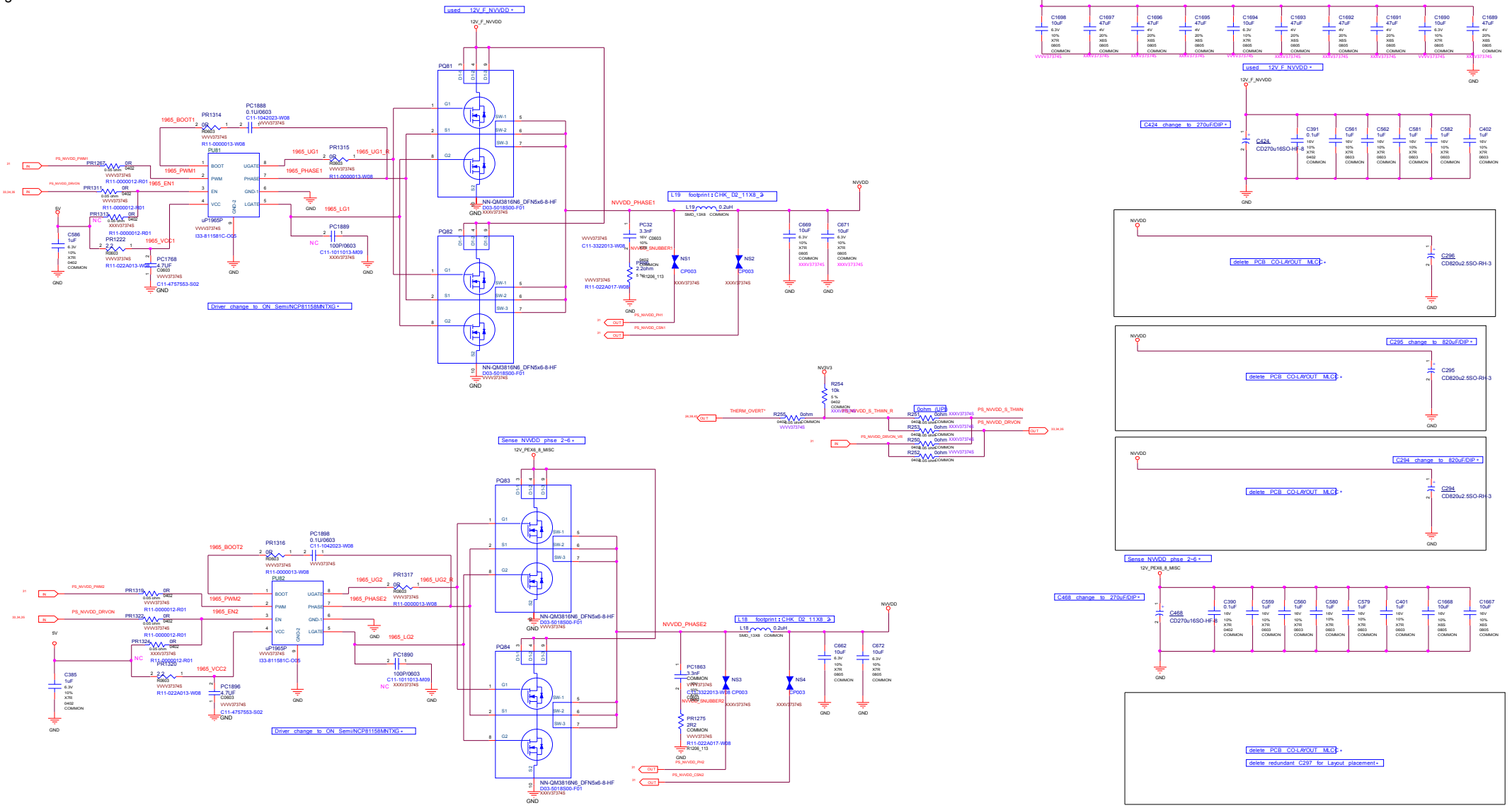
Page33: PS: NVVDD PH1&2



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Size: Custom	Document Description: PS: NVVDD PH1&2
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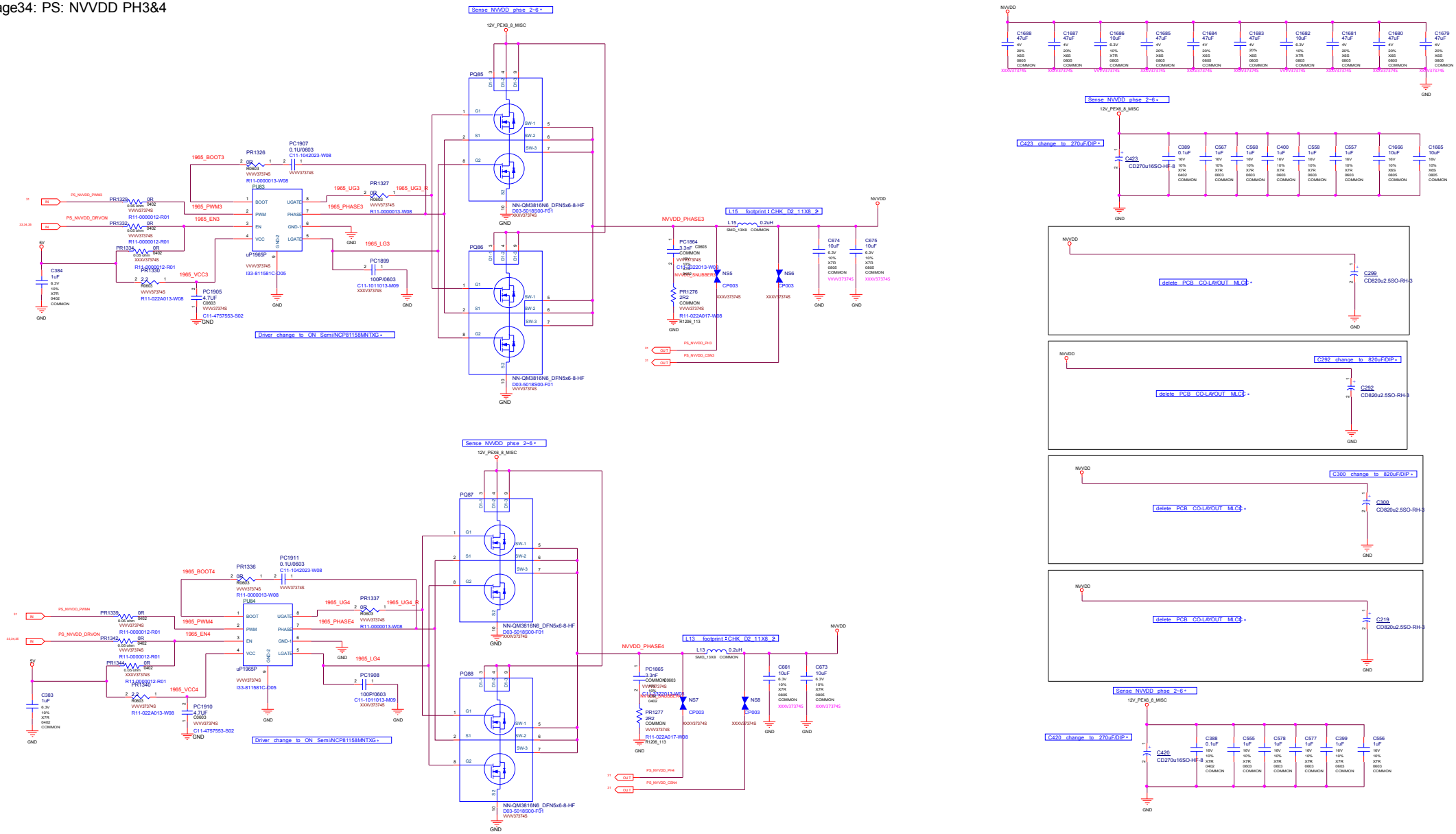
Page34: PS: NVVDD PH3&4



MICRO-STAR INT'L CO.,LTD	
MS-V375	
Size: Custom	Document Description: PS: NVVDD PH3&4
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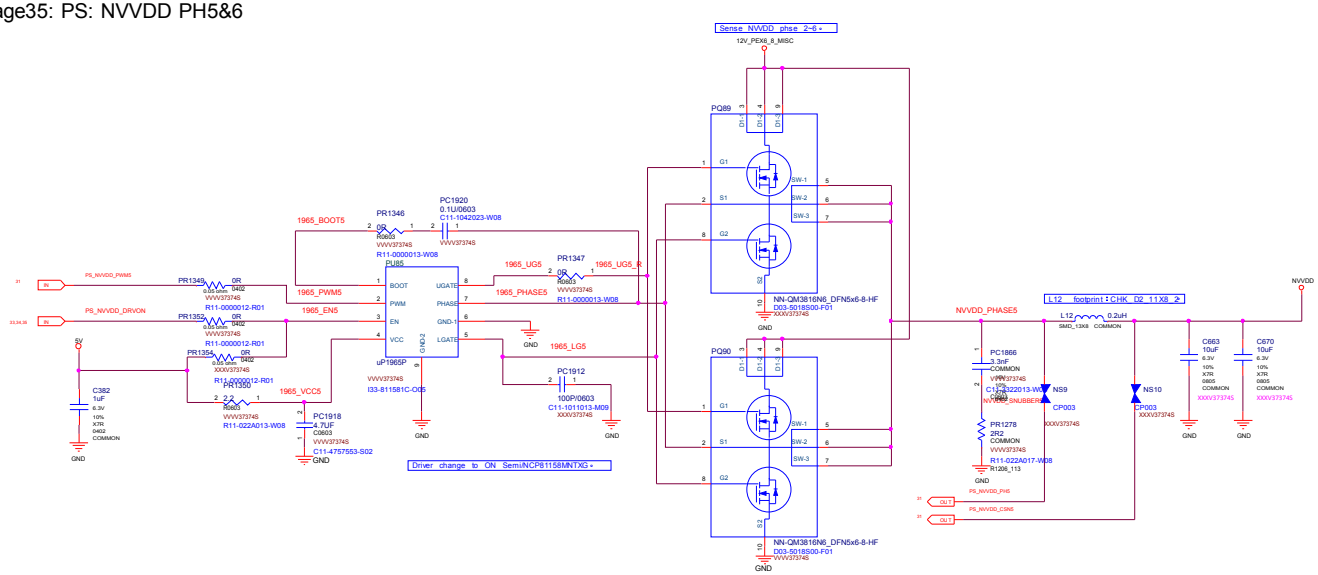
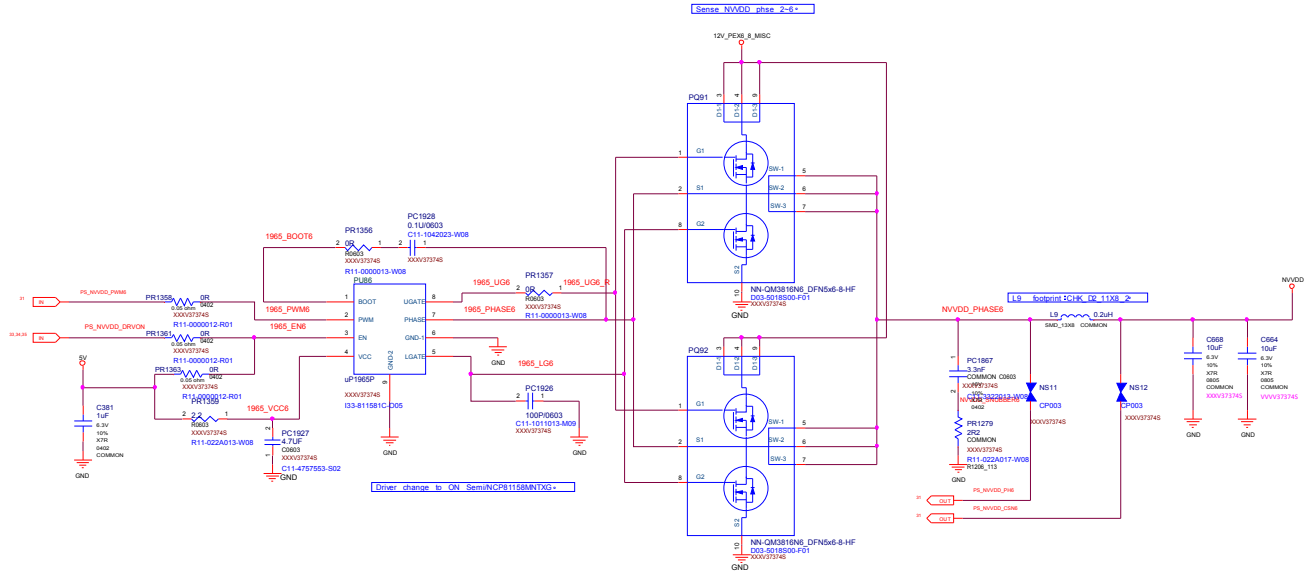
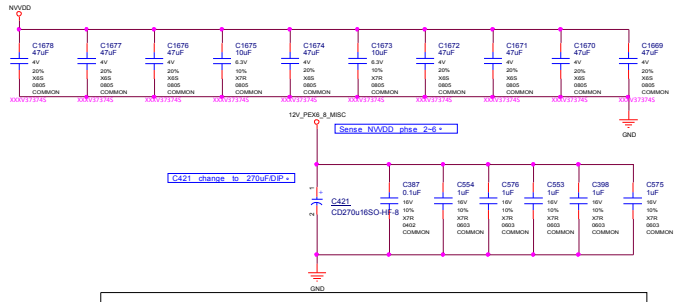
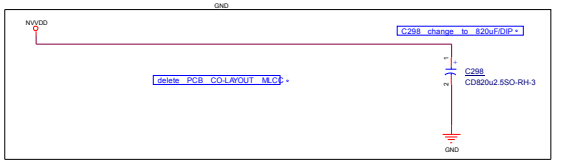
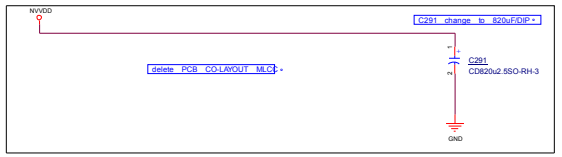
Page35: PS: NVVDD PH5&6

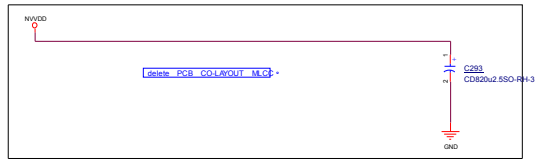


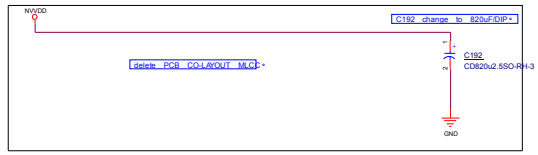


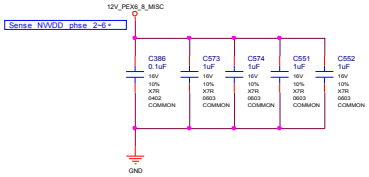












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Size: Custom	Document Description: PS: NVVDD PH5&6	Rev: 4.0
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Page36: Input Power Balancing Switcher

removed U511 for fixed NVVDD 12Vi nput:
1、merged 3V3_AON to 3V3_F。
2、unused and delete 3V3_AUX。
3、unused and delete 3V3_AUX_CON。
4、NVVDD_DYN_VIN merged to 12V_PEX6_8_F1。

delete GPIO2_INPUT_DYN_BAL1 。

delete INPUT_PEX6_DT1_STEER 。

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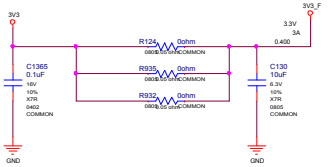
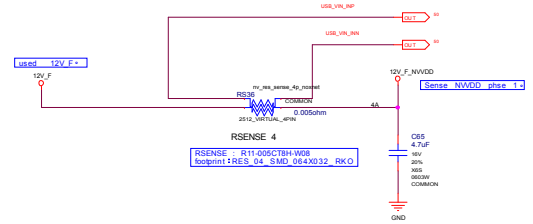
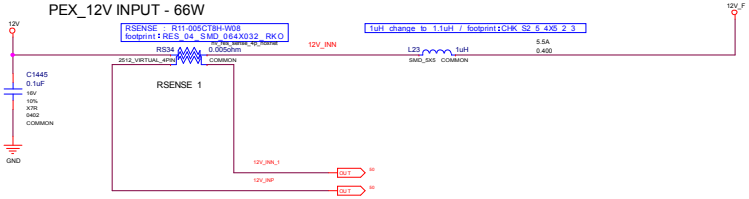
1 changed EXT 12V 8pin PN and footprint.
2 add EXT 12V 8pin Fuse.
3 delete unused parts.
4 RSENSE 3 change to sense NVVDD PEX 12V.
5 RSENSE 4 change to sense NVVDD EXT 12V.
6 change RSENSE parts and footprint.

PEX 3V3 INPUT - 10W

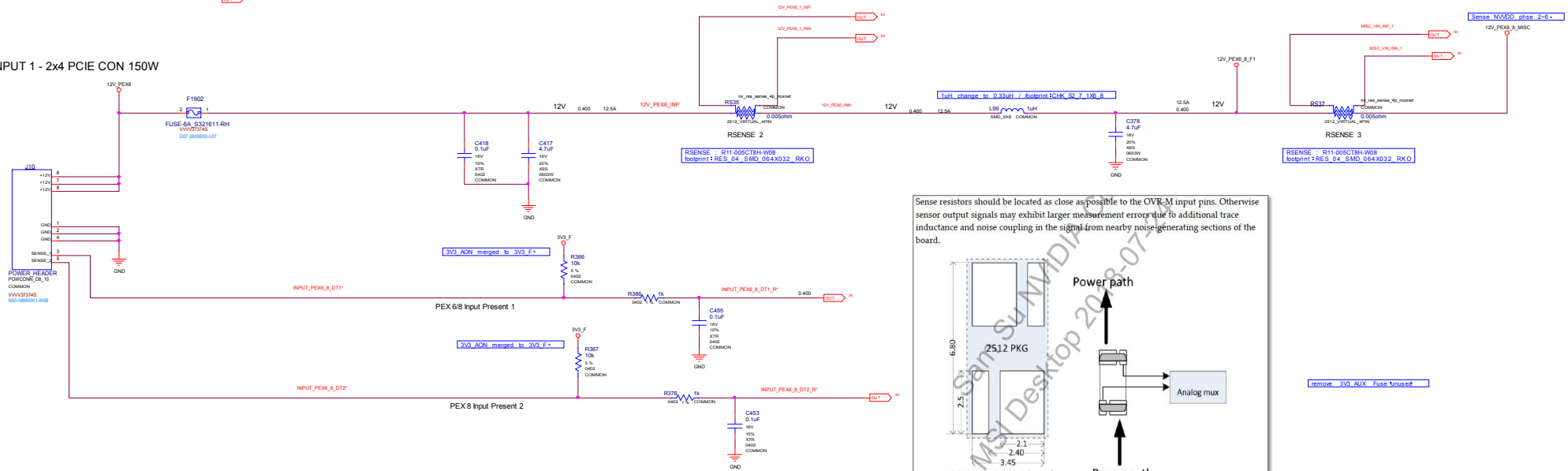




PEX_12V INPUT - 66W



PEX8 INPUT 1 - 2x4 PCIE CON 150W



Sense resistors should be located as close as possible to the OVR-M input pins. Otherwise sensor output signals may exhibit larger measurement errors due to additional trace inductance and noise coupling in the signal from nearby noise-generating sections of the board.

Figure 5.10 Connection for 2-Pin Sense Resistor (2512 Package)

If customer prefers using a 2-pin sense resistor instead, we recommend implementing a 4-pin footprint with two large PADs for the high current path and two small PADs for sensing line, to emulate the functionality of a 4-pin resistor.

Note: Two-pin sense resistor can be used, but the sensing signal MUST connect to resistor pad directly. Connect the sensing signal to nearby power plane may cause large measurement error.

remove 3V3_AUX Fuse *unused*

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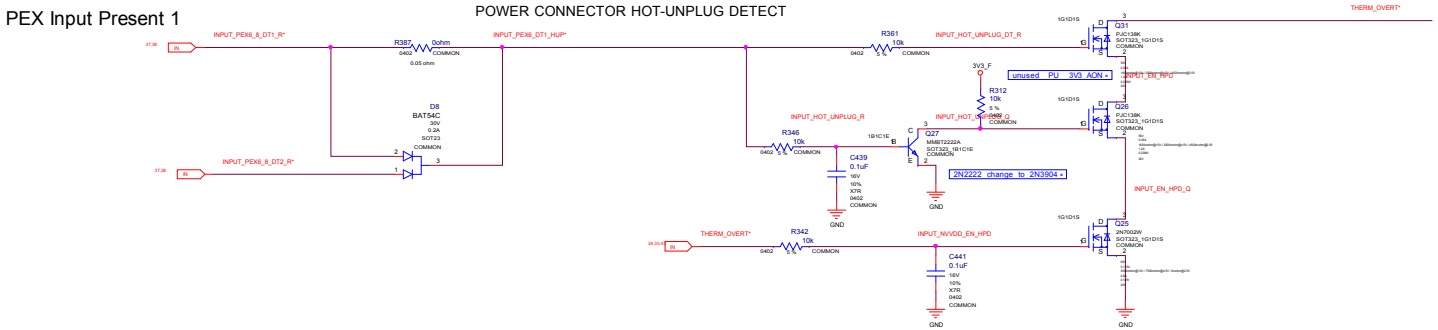
Page38: PS: STEERING, UNDER POWER BOOT & HOT-UNPLUG

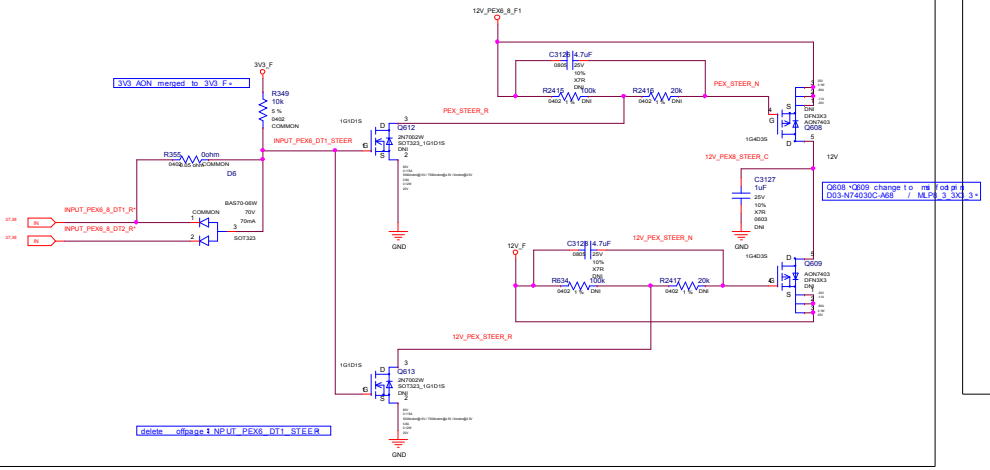
PEX Input Present 1



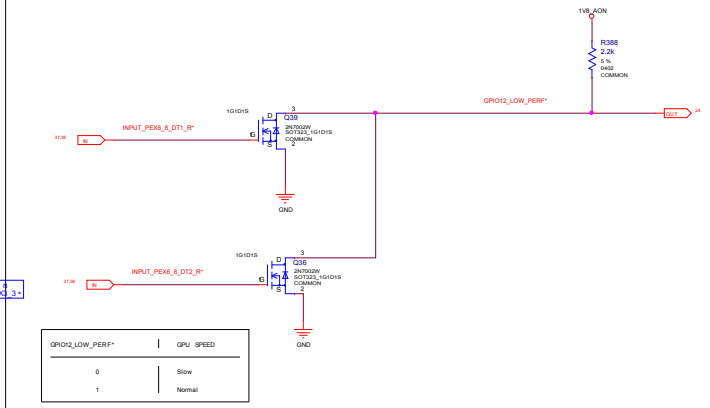
12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA

copied 12V CURRENT STEERING from V373-2.0 and BOM stuff ed



PEX Input - Power Level/PSI* Control



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Size: Custom	Document Description: PS: STEERING, UNDER POWER BOOT & HOT-UNPLUG	Rev: 4.0
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Page39: BUCKBOOST

delete regulator for USBC_VBUS ◦

Unused USB_I2C* leaving Pull high resistor to 1.8V ◦

MICRO-STAR INT'L CO.,LTD

MS-V375

Size	Document Description	Rev
Custom	BUCKBOOST	4.0

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Page40: PPC

delete PPC ◦

Unused USB_I2C* leaving Pull high resistor to 1.8V ◦

delete PEX_RST_BUF* ◦

delete GPIO1_GC6_FB_EN ◦

Unused IFPB_I2C* leaving Pull high resistor to 1.8V ◦

delete GPIO24_IFPF_HPD ◦

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MS-V375

Size: Custom | Document Description: PPC | Rev: 4.0

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Page41: 12V & 3V3_A SWITCHER

unused and delete all ◦

delete GPIO1_GC6_FB_EN *

delete GPIO29_IDLE_IN_SW *

delete off-page 2PS_RTD_SWT.CH

unused and delete C404 *

MICRO-STAR INT'L CO.,LTD

MS-V375

Size	Document Description	Rev
Custom	12V & 3V3_A SWITCHER	4.0

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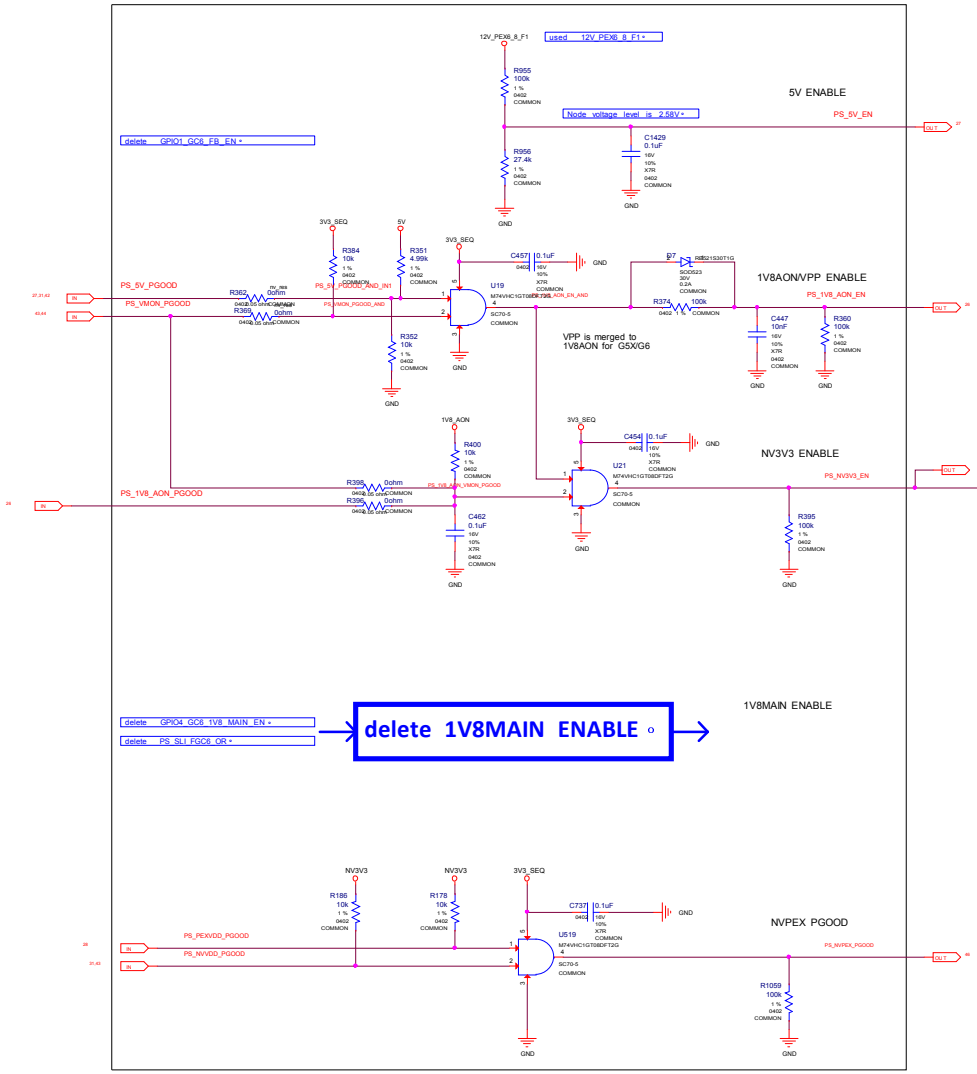
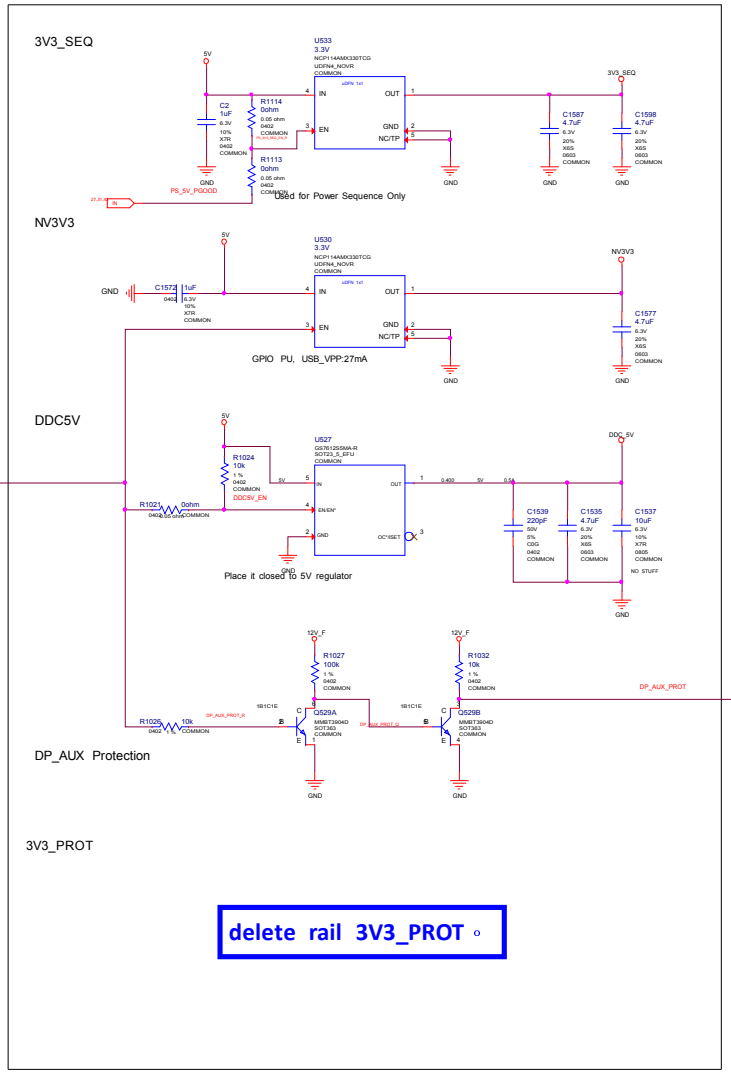
Page42: SEQ:5V,1V8,NV3V3 ENABLE





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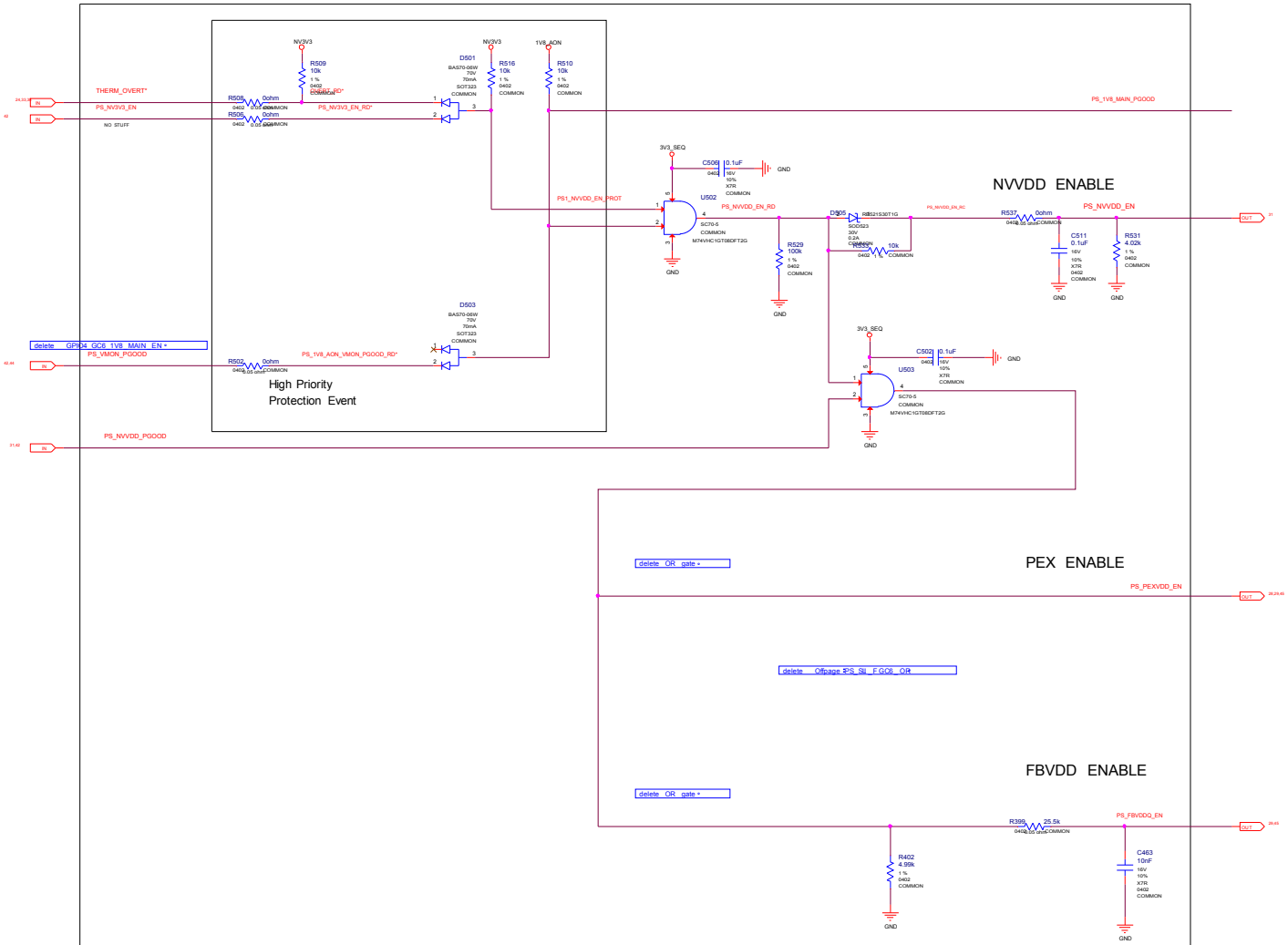
Page43: SEQ:NV,PEX,FB ENABLE



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V375	
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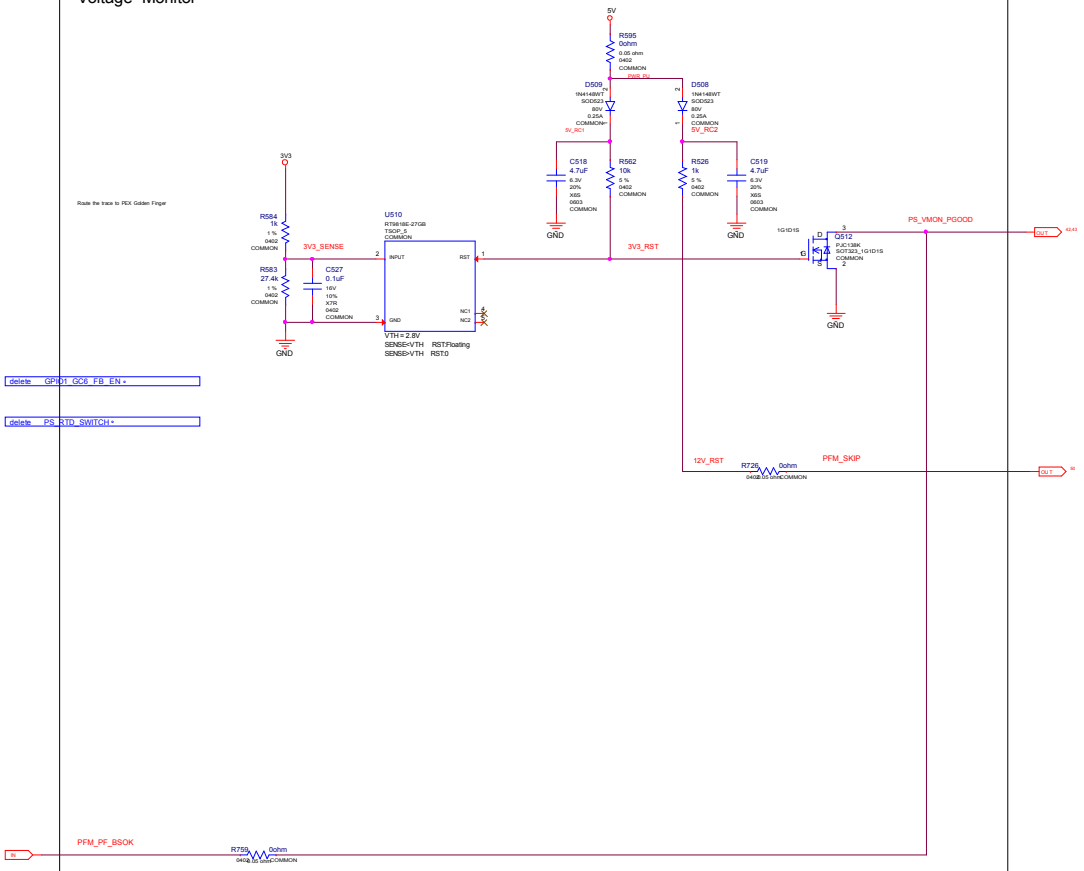
Page44: SEQUENCE:Voltage Monitor

delete unused parts。

Voltage Monitor



Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)

BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter	Pre-Filter	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

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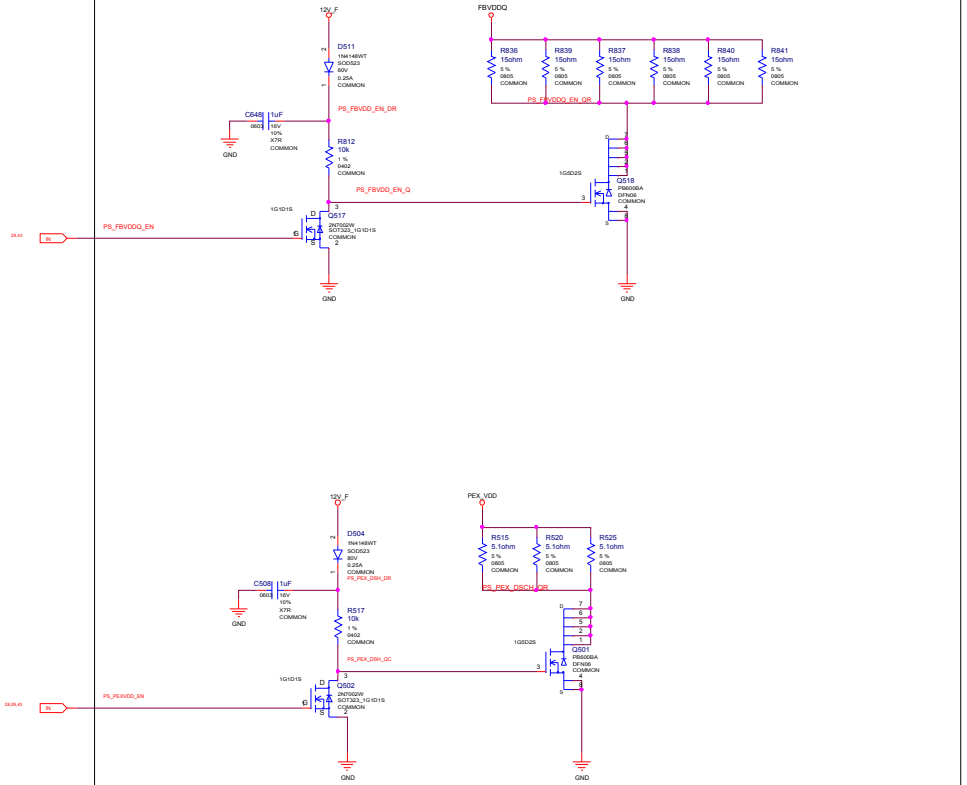
Page45: SEQUENCE:Discharge



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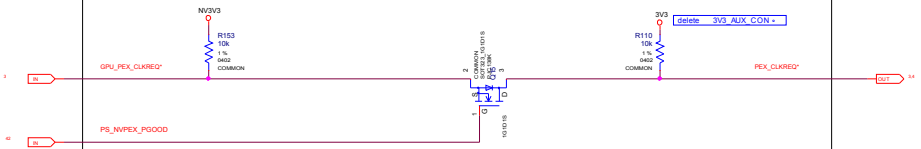
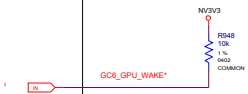
Page46: SEQUENCE:MISC

PEX_CLKREQ*



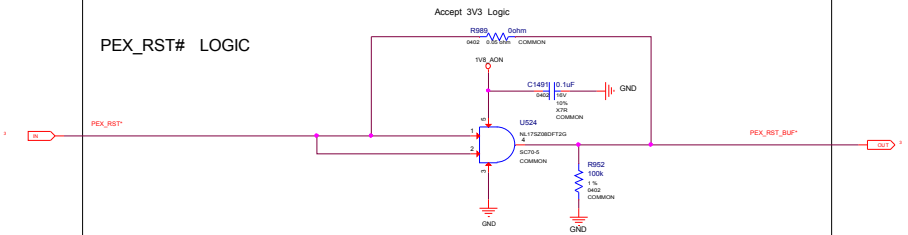
GPU_WAKE*



delete GPU_WAKE* o

PEX_RST# LOGIC

Accept 3V3 Logic



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Page47: LOGO LED

delete all unused

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Page48: LED DRIVER & Boost

delete all unused

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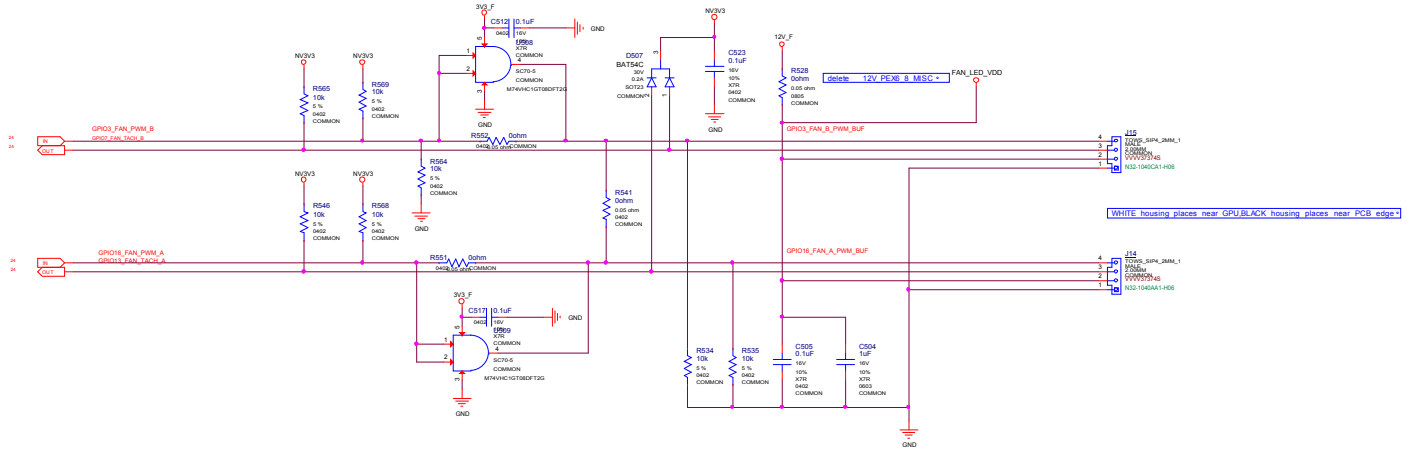
Page49: DUAL FAN

copied V373-2.0 housing PN and footprint。



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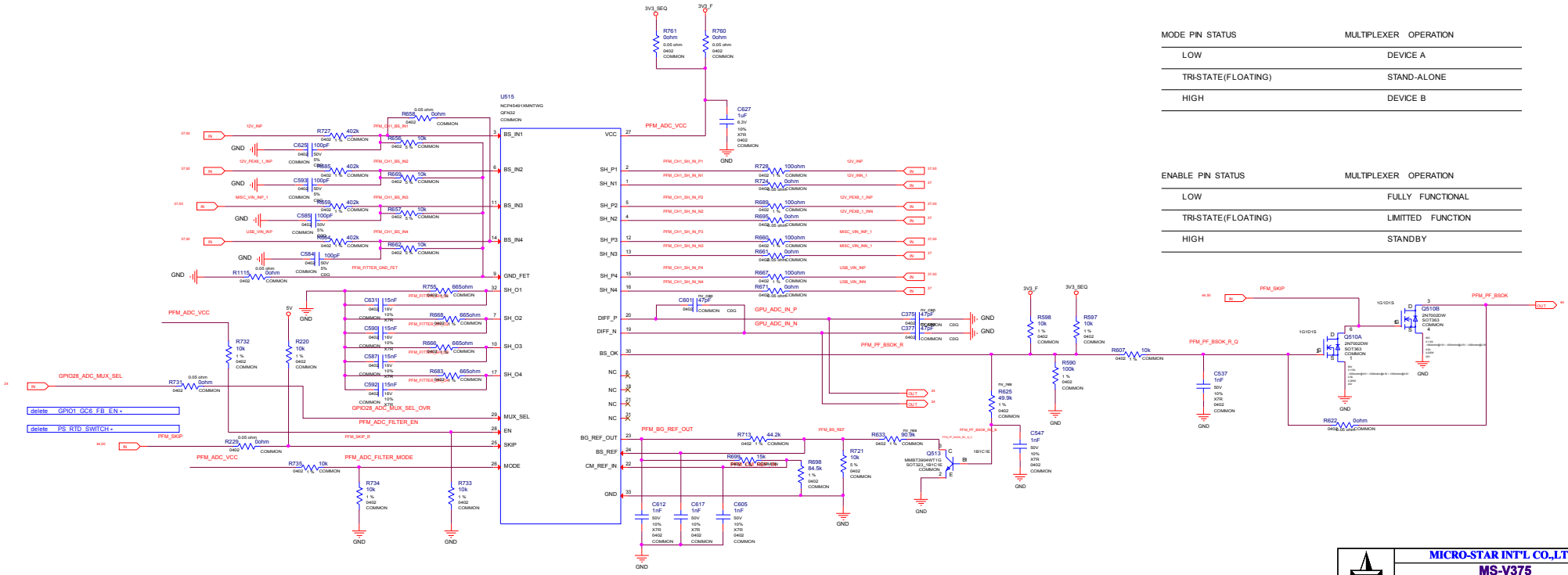
Page50: PWR SENSE



MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITTED FUNCTION
HIGH	STANDBY

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Page51: MECH

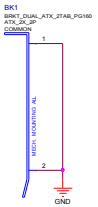
HDMICOVER1
STIFFNER
NO PINS
XXXV37374S
E24-V330030-P09

DPCOVER1
STIFFNER
NO PINS
XXXV37374S
E24-V330010-P09

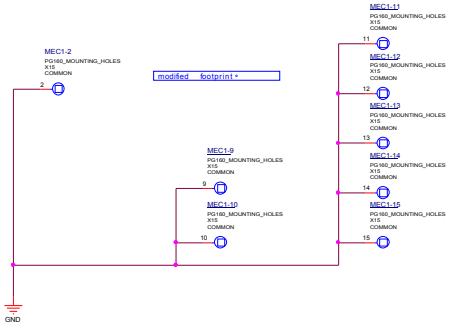
DPCOVER2
STIFFNER
NO PINS
XXXV37374S
E24-V330010-P09

DPCOVER3
STIFFNER
NO PINS
XXXV37374S
E24-V330010-P09

Brackets:



MOUNTING HOLES FOR HS:



Bracket Screw

BKTSCREW1
VWV37374S
E41-1304010-H75

HDMISCREW1
VWV37374S
E43-1303004-H75

BKTSCREW2
VWV37374S
E41-1304010-H75

PCB1
PCB
109-GN982-00A
COMMON
VWV37374S
PD0-0V37340-E48

HDMI_FEE1
HDMI
HDMI_FEE
COMMON
VWV37374S
Y01-RHDMI03-000

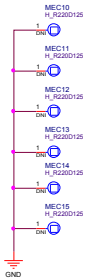
FAN1
STIFFNER
NO PINS
VWV37374S
E32-0406290-A87

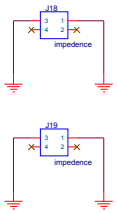
HS1
STIFFNER
NO PINS
VWV37374S
E31-0566110-A87

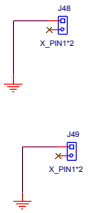
HS2
STIFFNER
NO PINS
VWV37374S
E93-0000171-A87

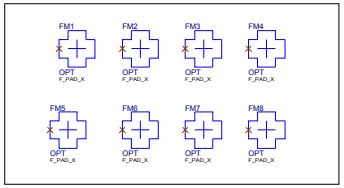
PCIE1
STIFFNER
NO PINS
VWV37374S
E24-V330020-P09

Mechanical Holes Symbol









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Page52: PTC

improved FBVDDQ PSU parts don't require a PTC

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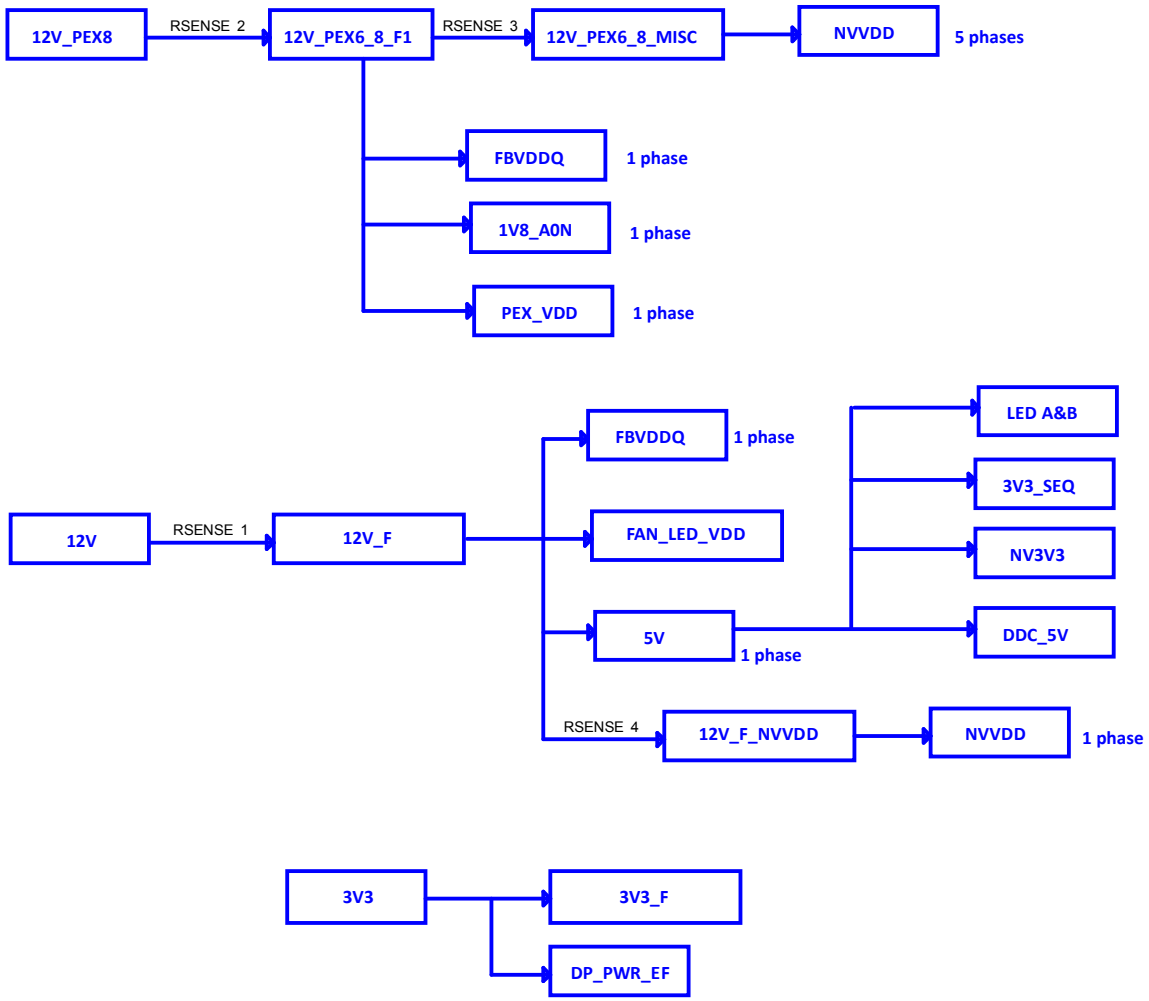
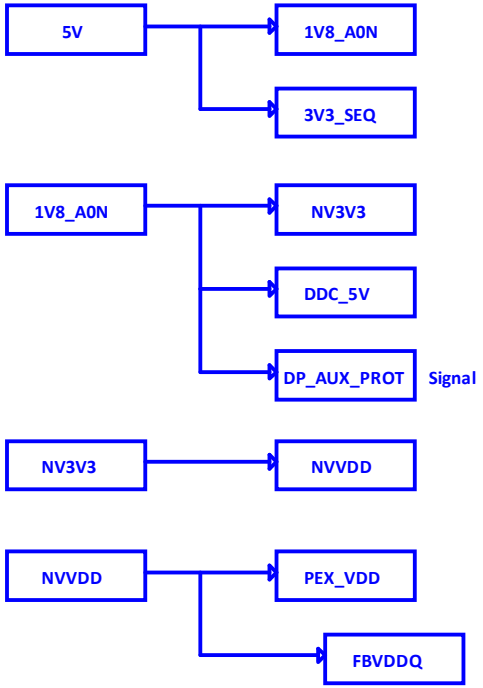


Power on Sequence



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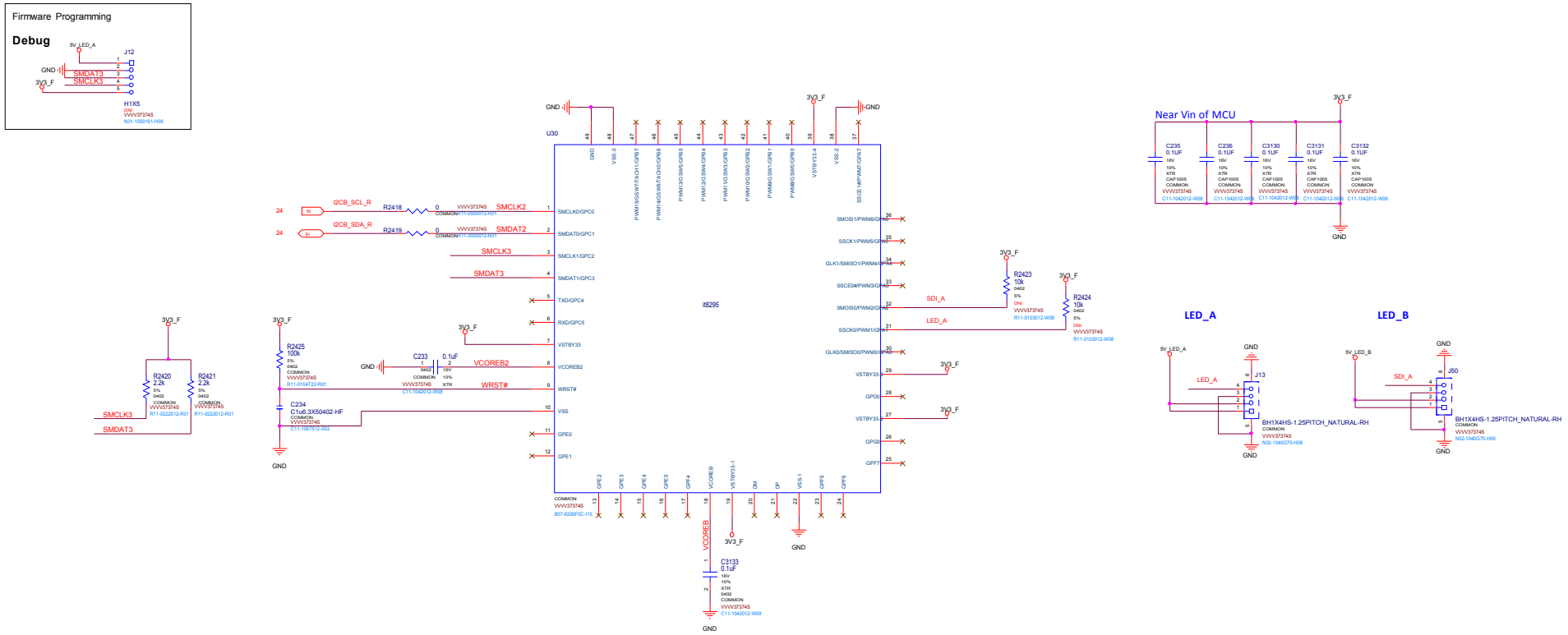
Page54: LED_CONTROLLER_IT8295



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