PG161-A01

TU106 6GB GDDR6, 192b, X16
DVI-D/DP + DP + HDMI

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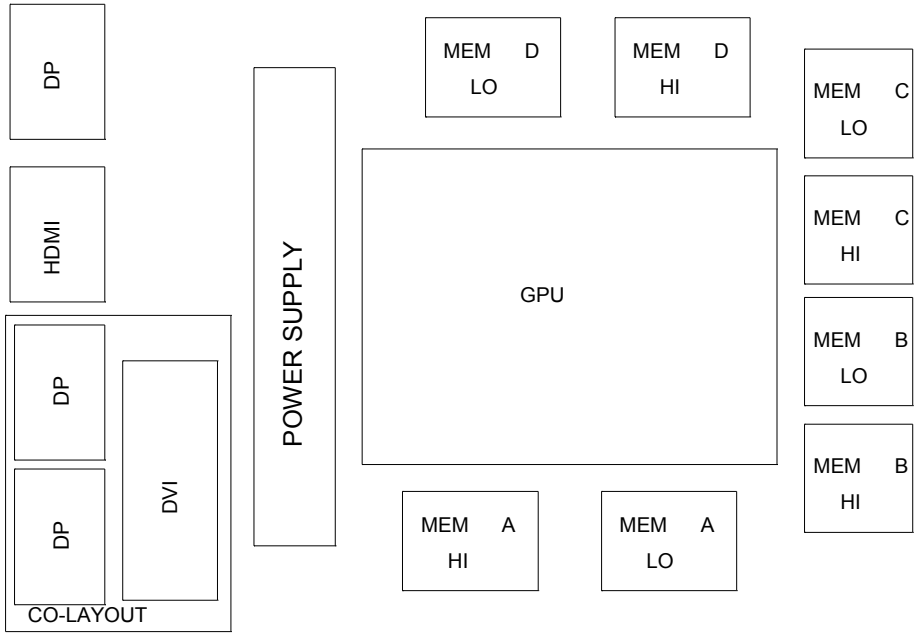
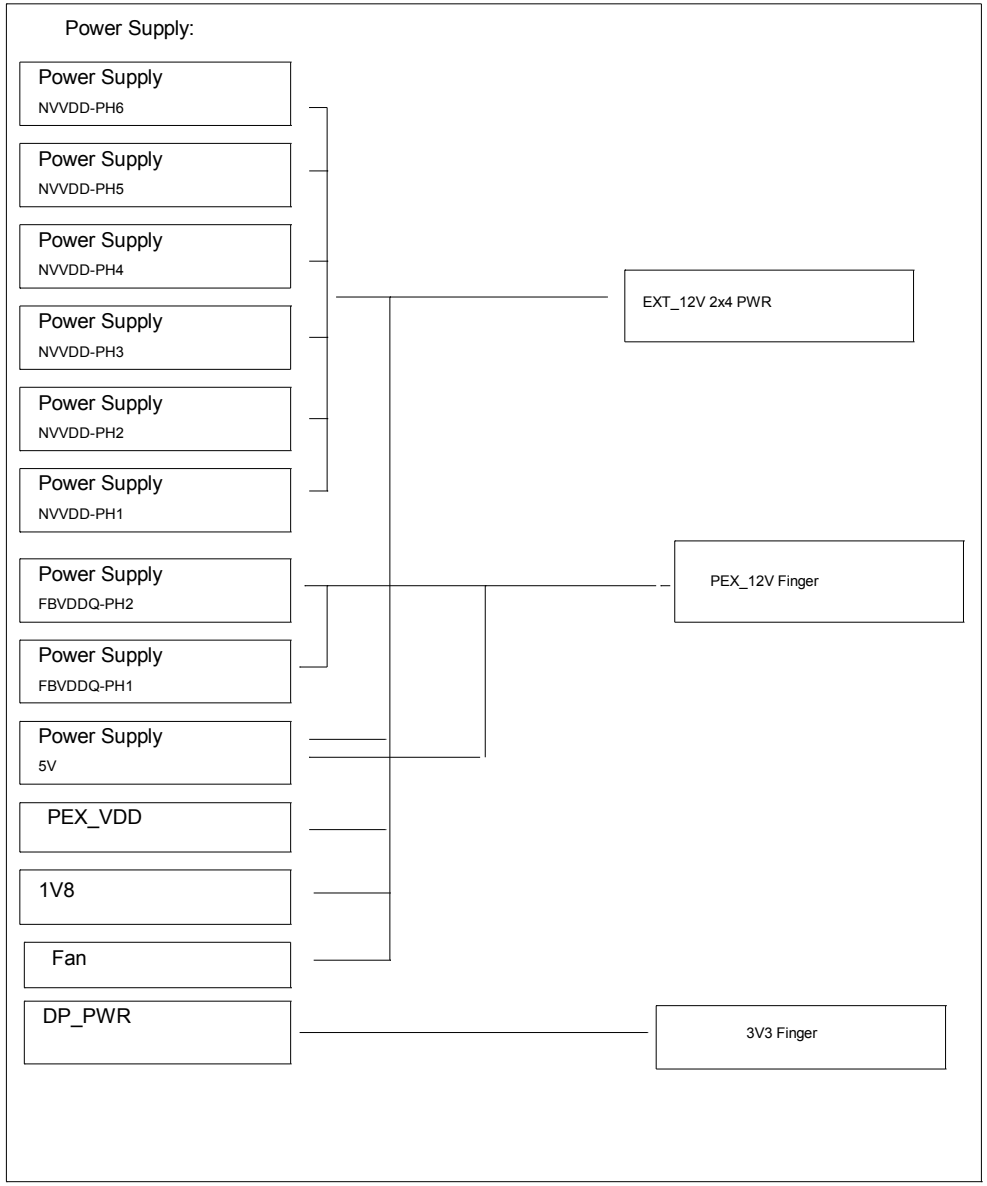
Page2: Block Diagram





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PAGE DETAIL	Block Diagram

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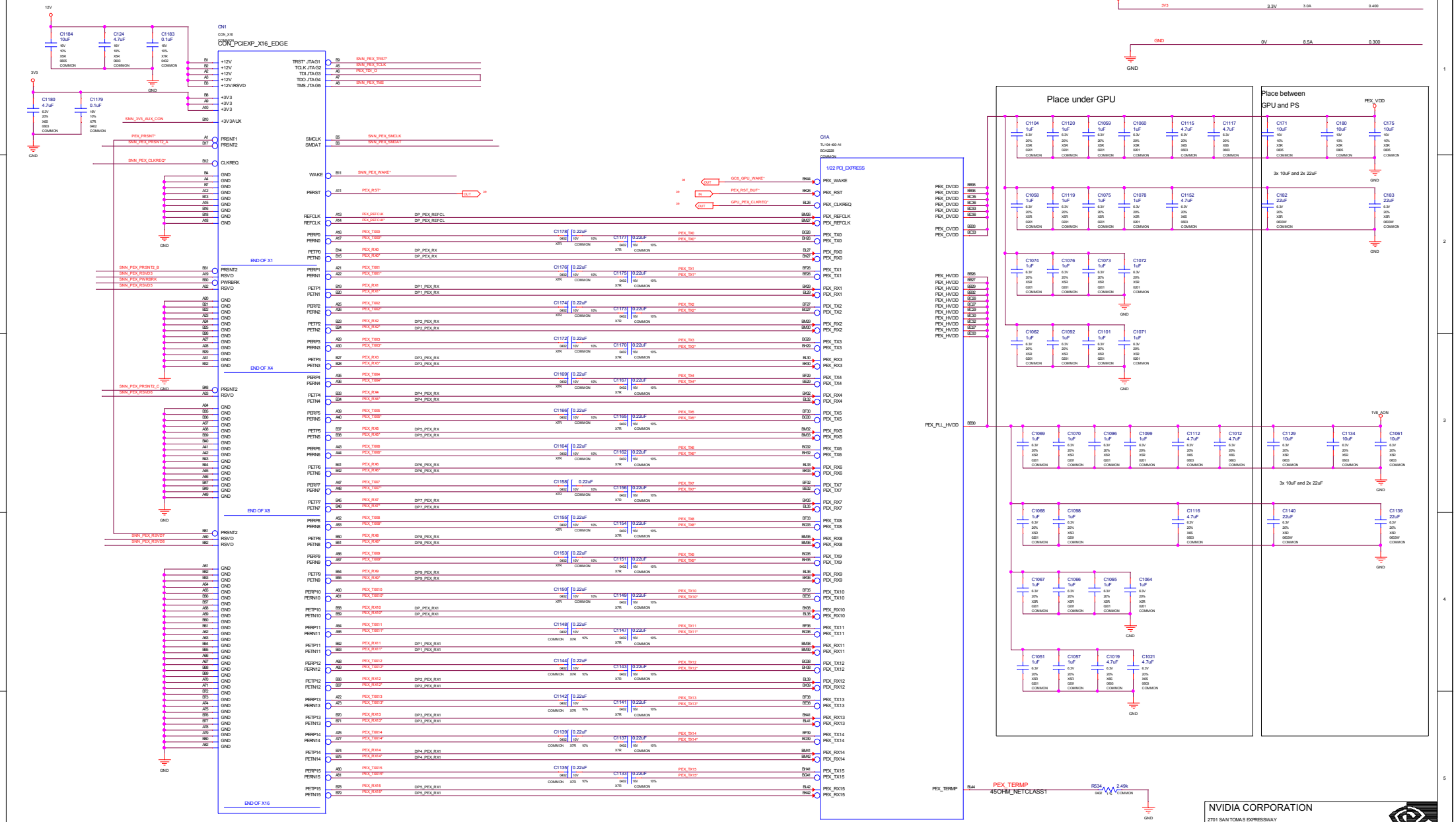
Page3: PCI Express



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3.3V	3.0A	0.400
0V	8.5A	0.300

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PCI Express

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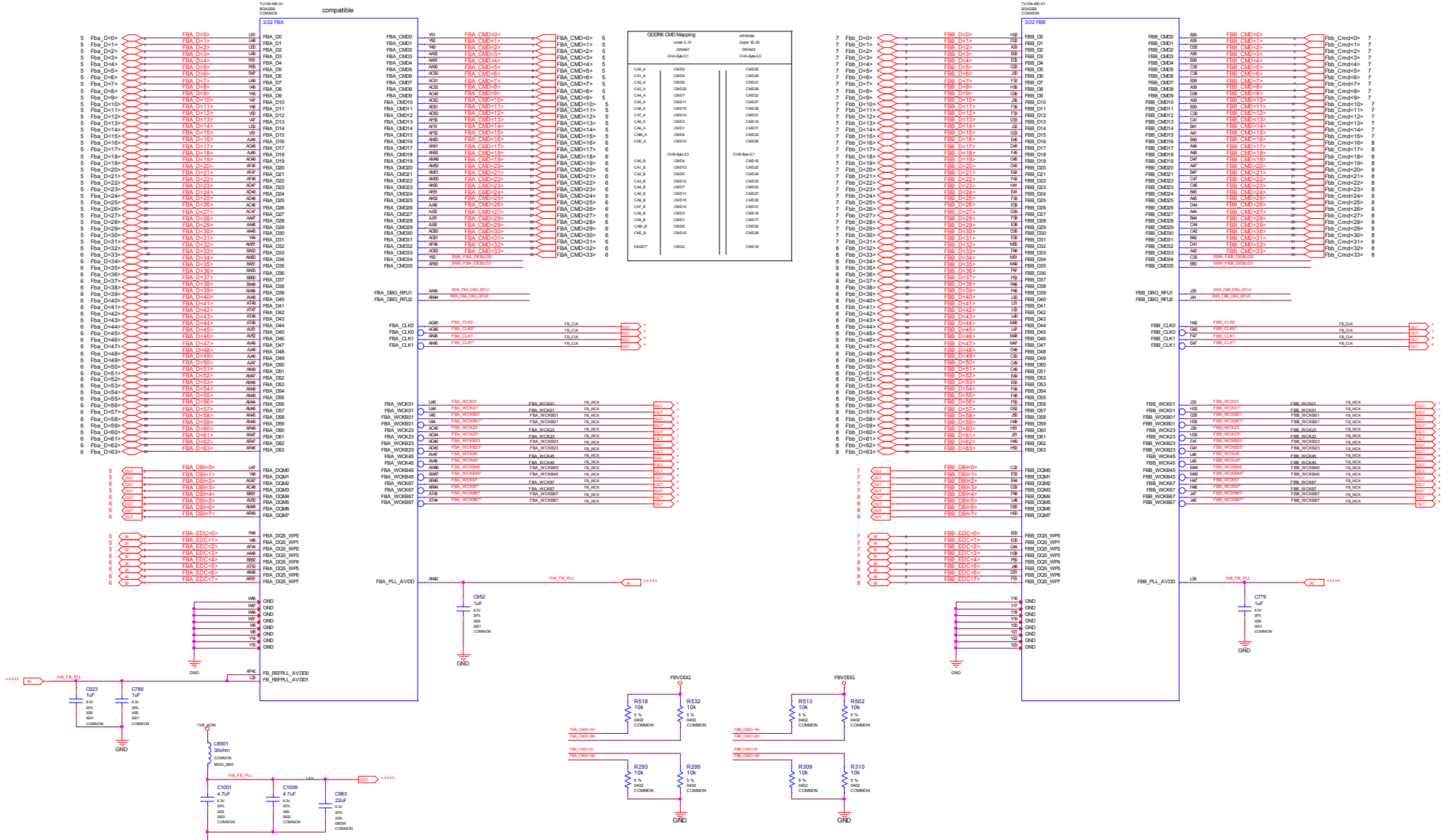
Page4: MEMORY: GPU Partition A/B



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PAGE DETAIL	MEMORY: GPU FB_AB

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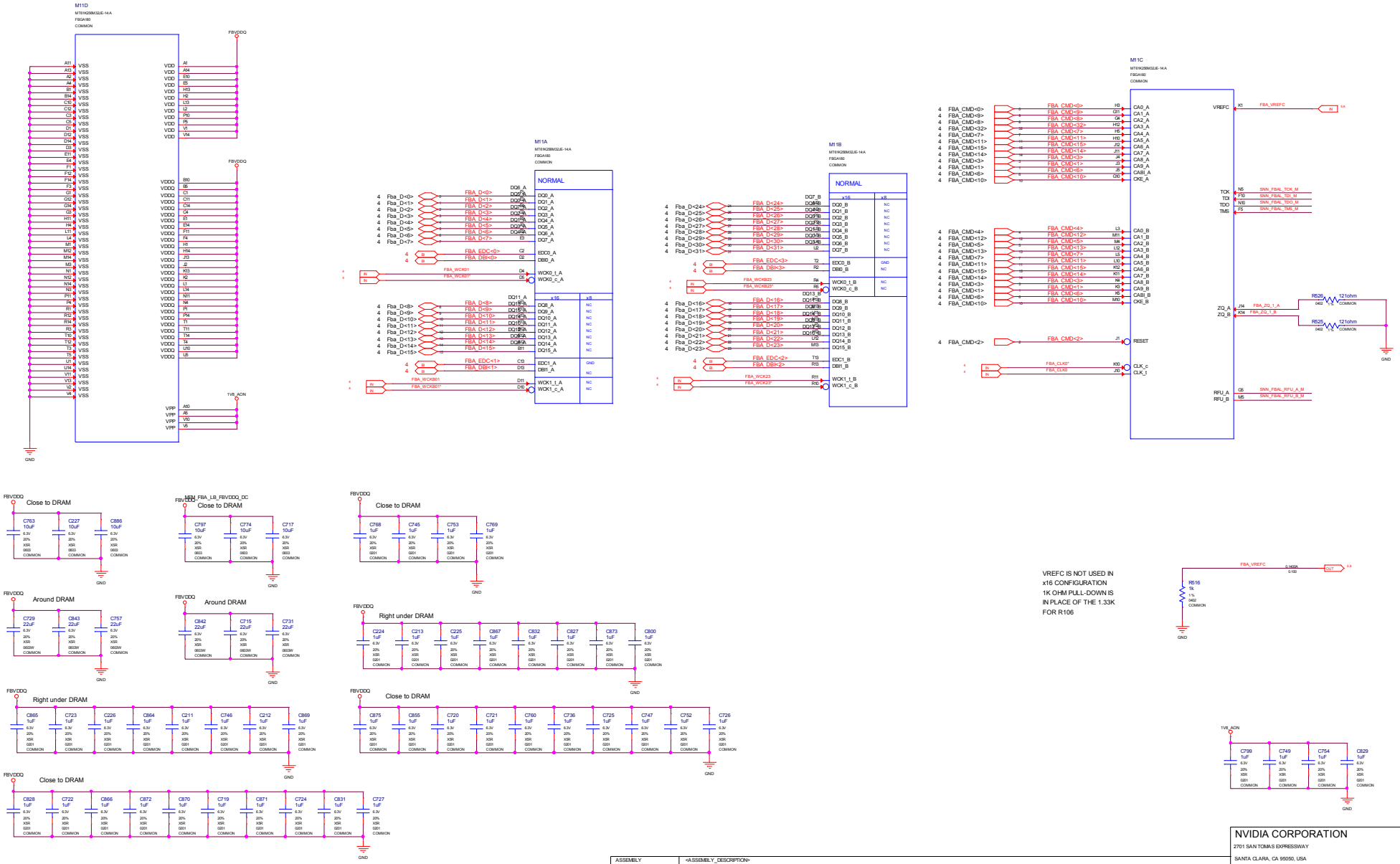
Page5: MEMORY: FBA Partition 31..0



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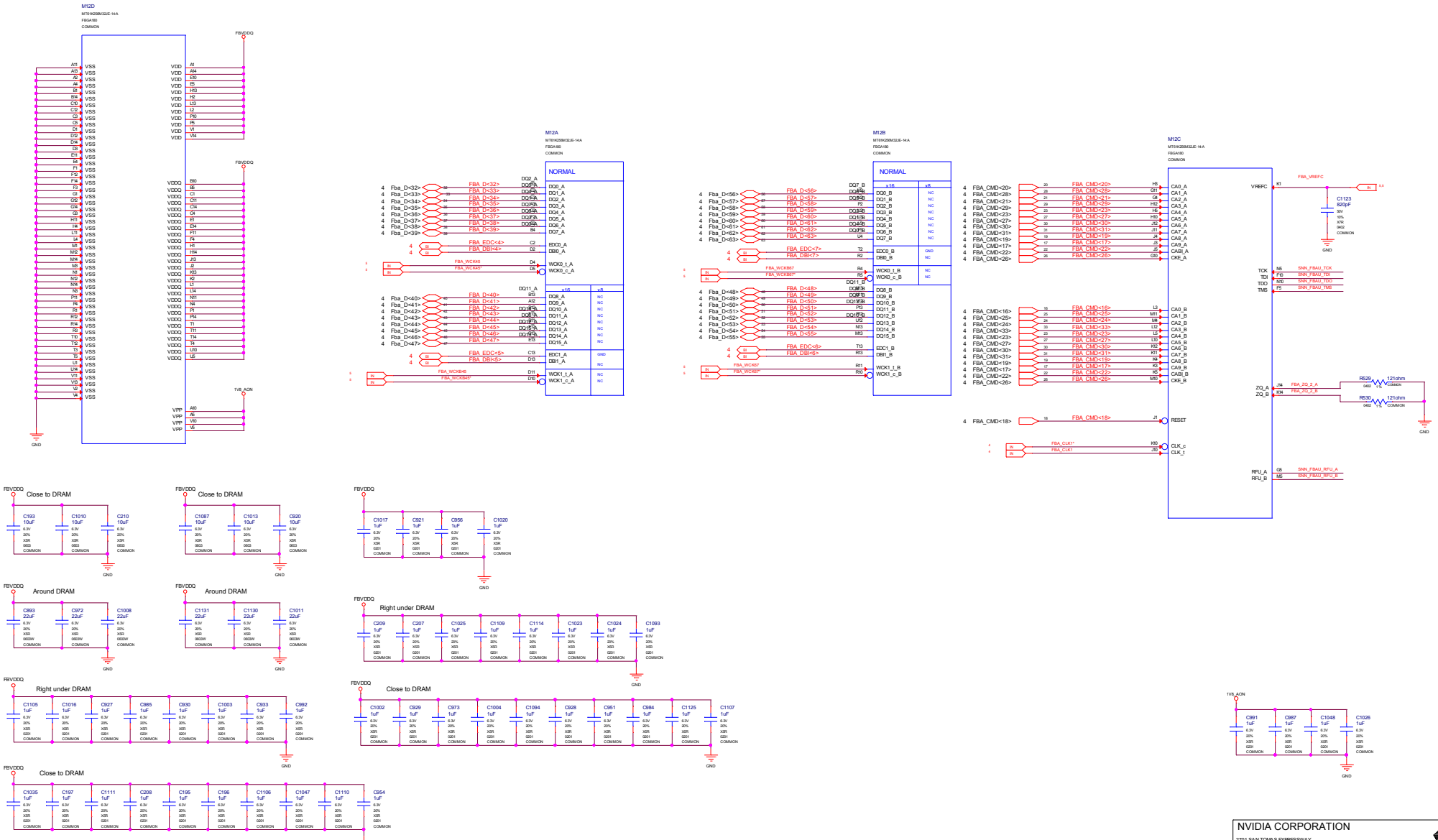
Page6: MEMORY: FBA Partition 63..32



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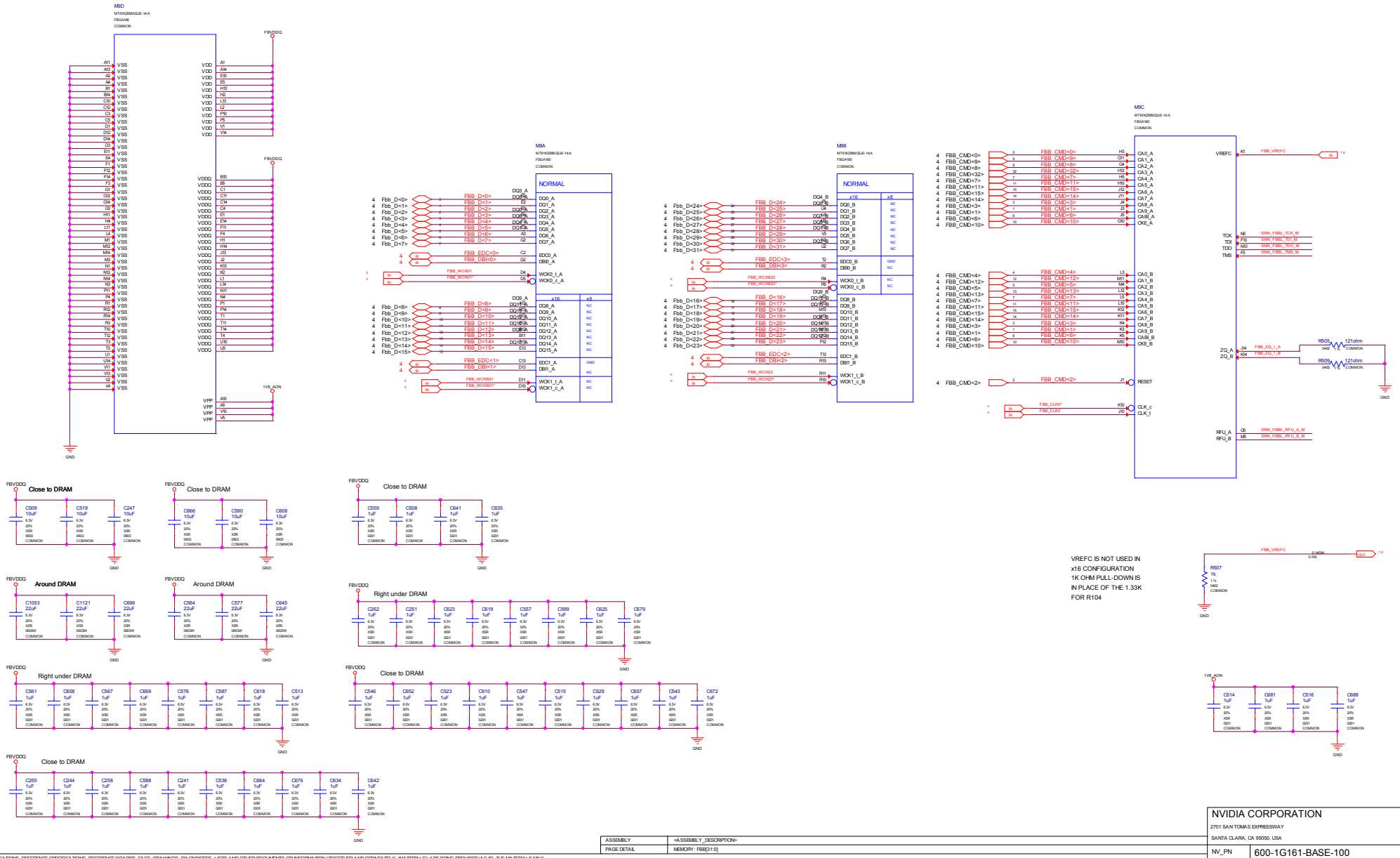
Page7: MEMORY: FBB Partition 31..0



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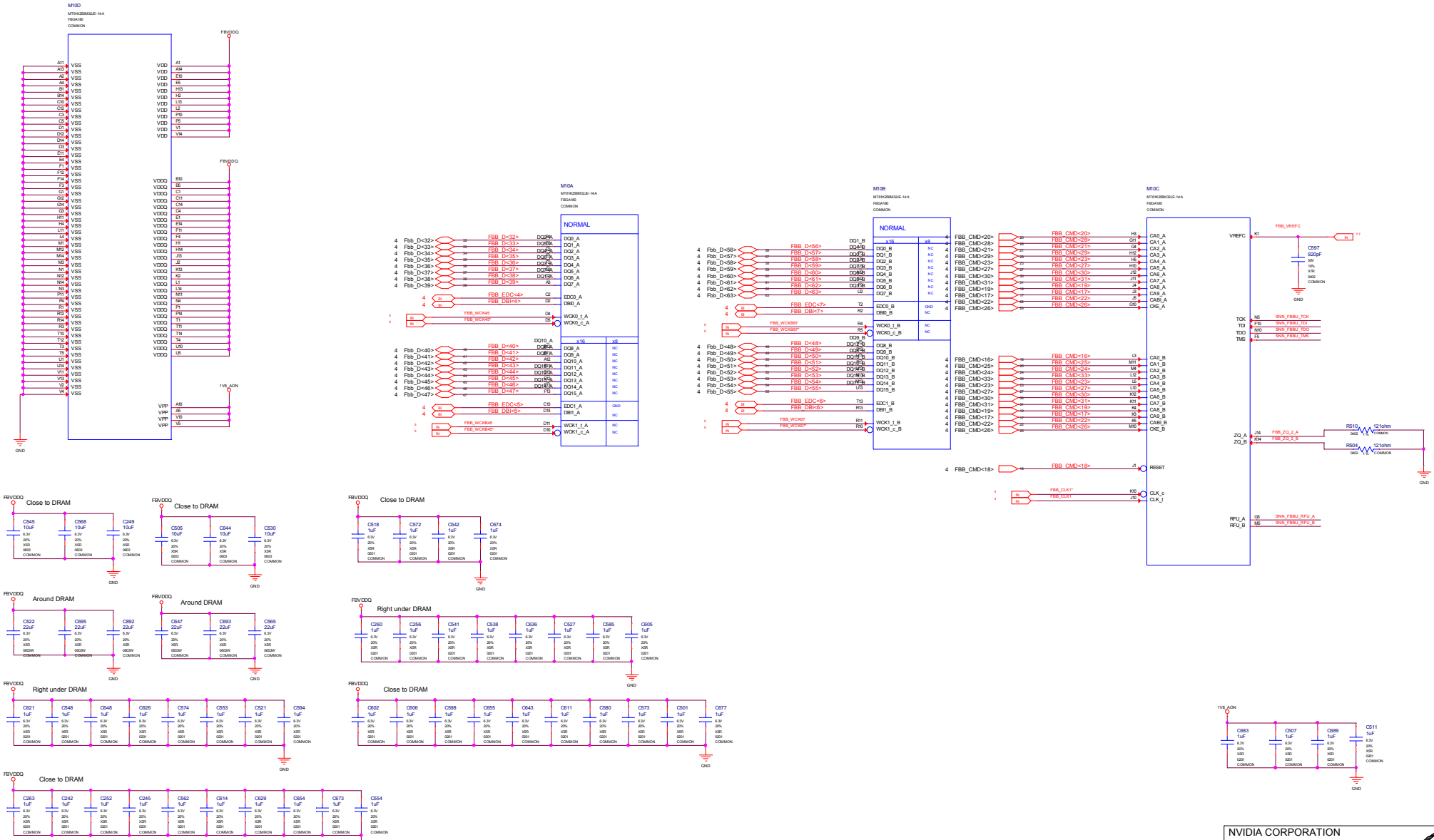
Page8: MEMORY: FBB Partition 63..32



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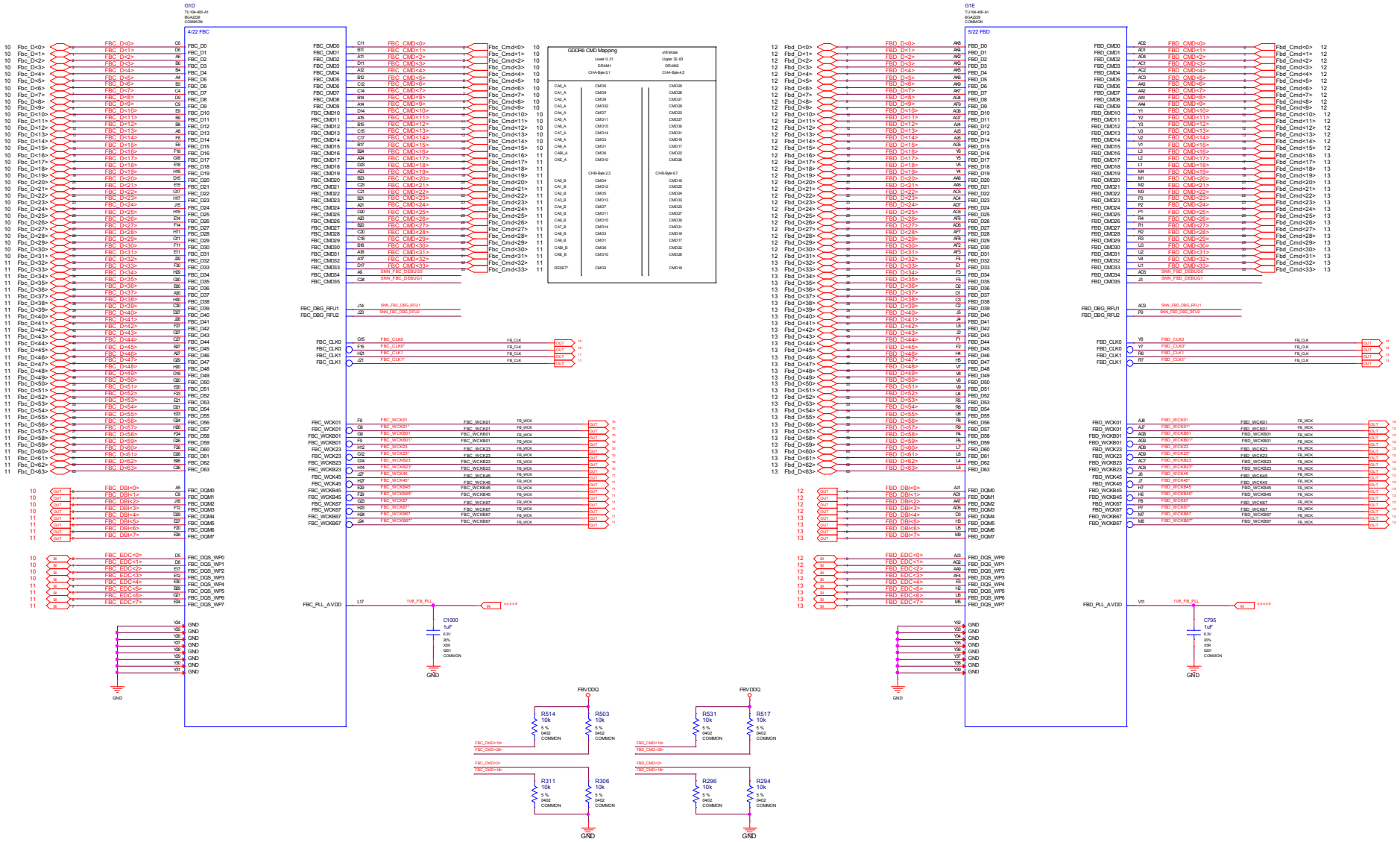
Page9: MEMORY: GPU Partition C/D



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PAGE DETAIL	MEMORY: GPU FB_CD

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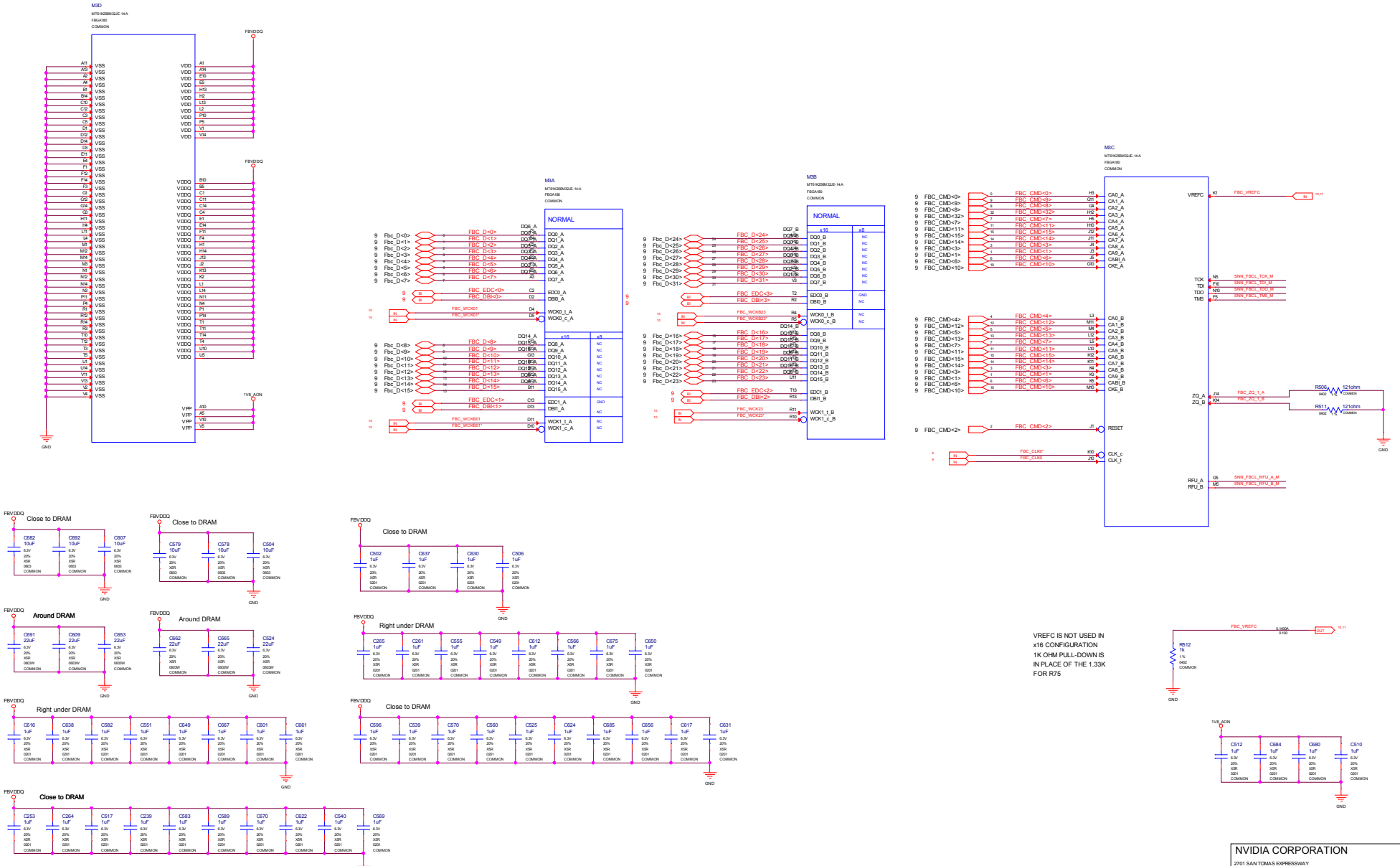
Page10: MEMORY: FBC Partition 31..0



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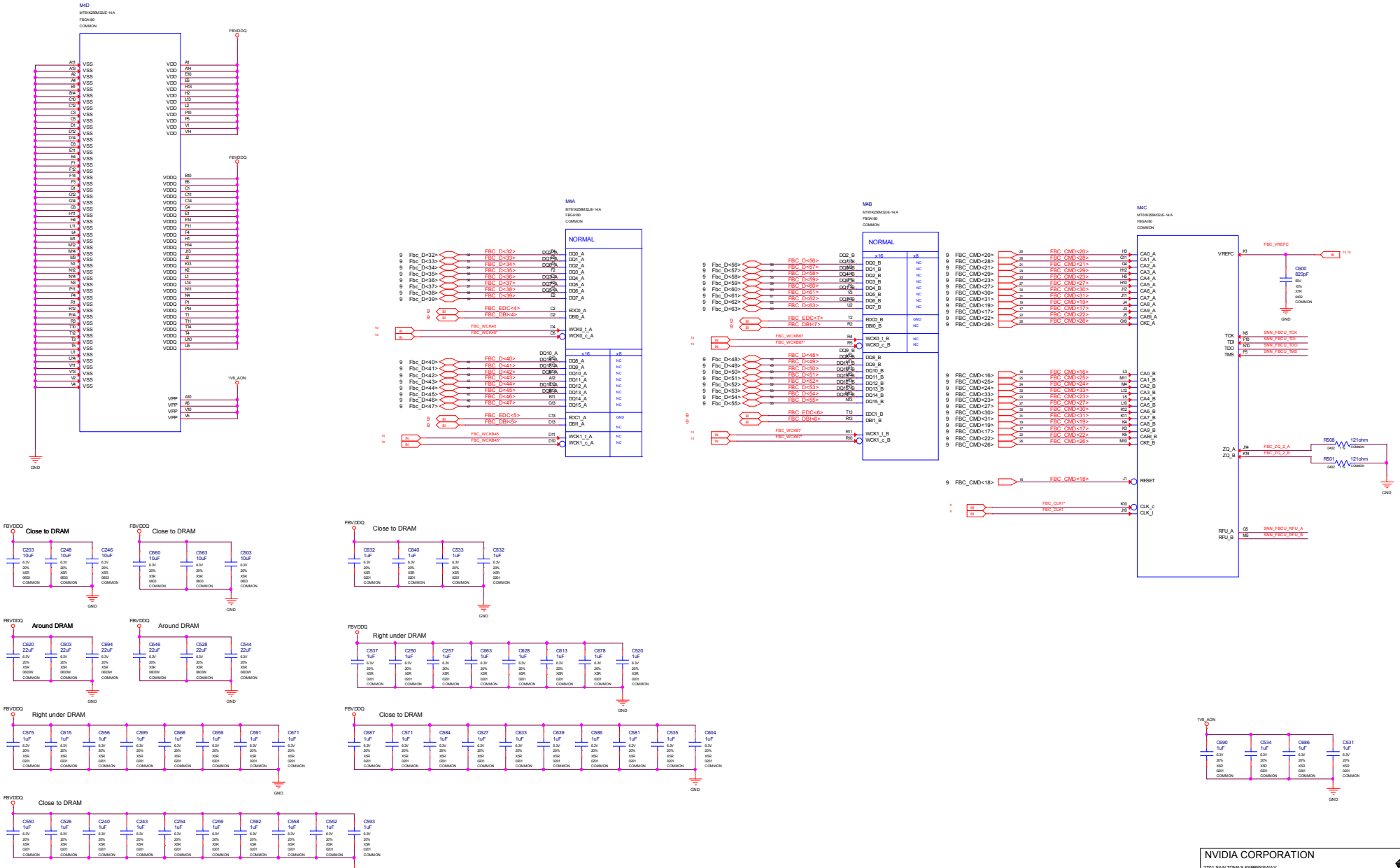
Page11: MEMORY: FBC Partition 63..32



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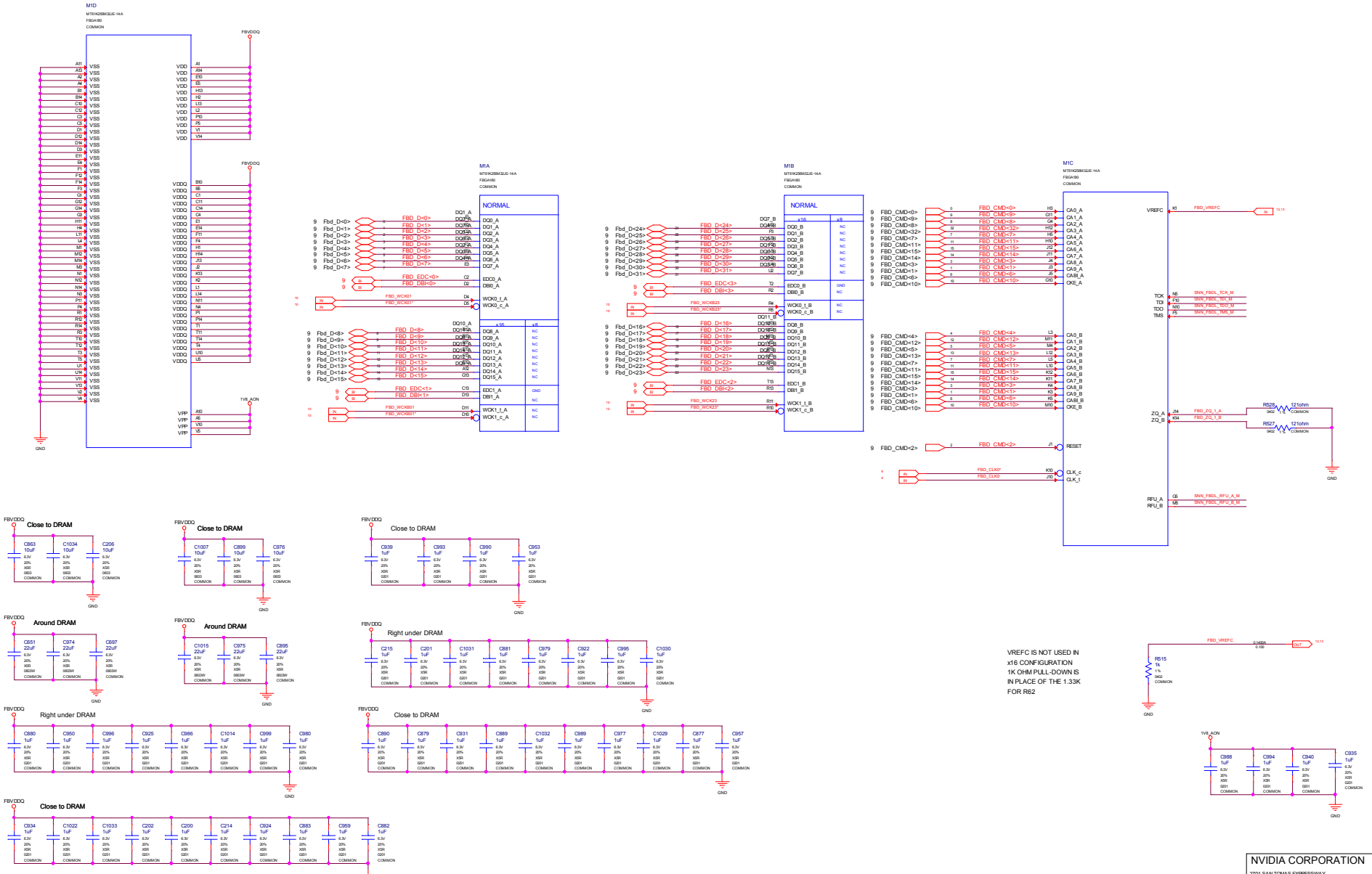
Page12: MEMORY: FBD Partition 31..0



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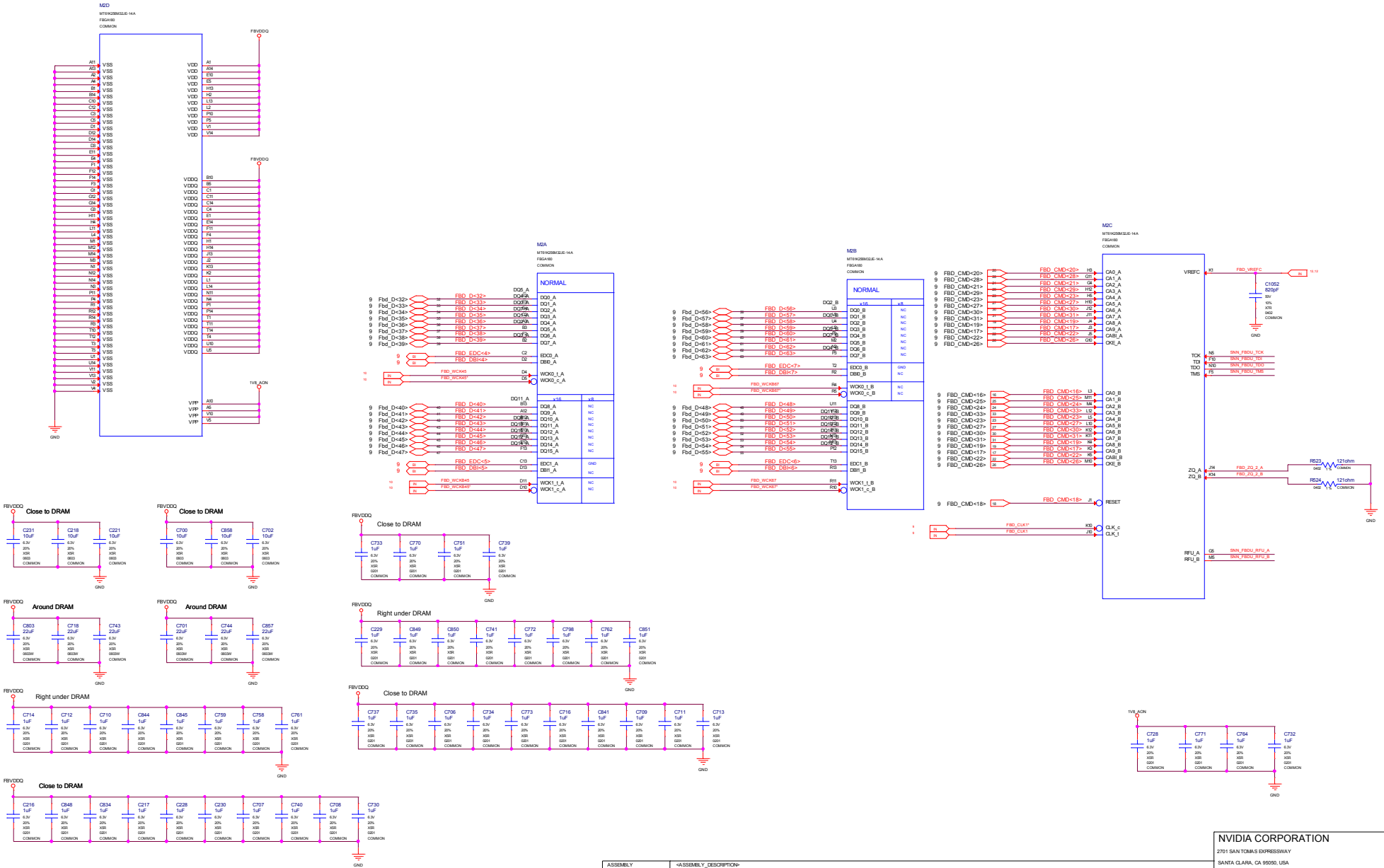
Page13: MEMORY: FBD Partition 63..32



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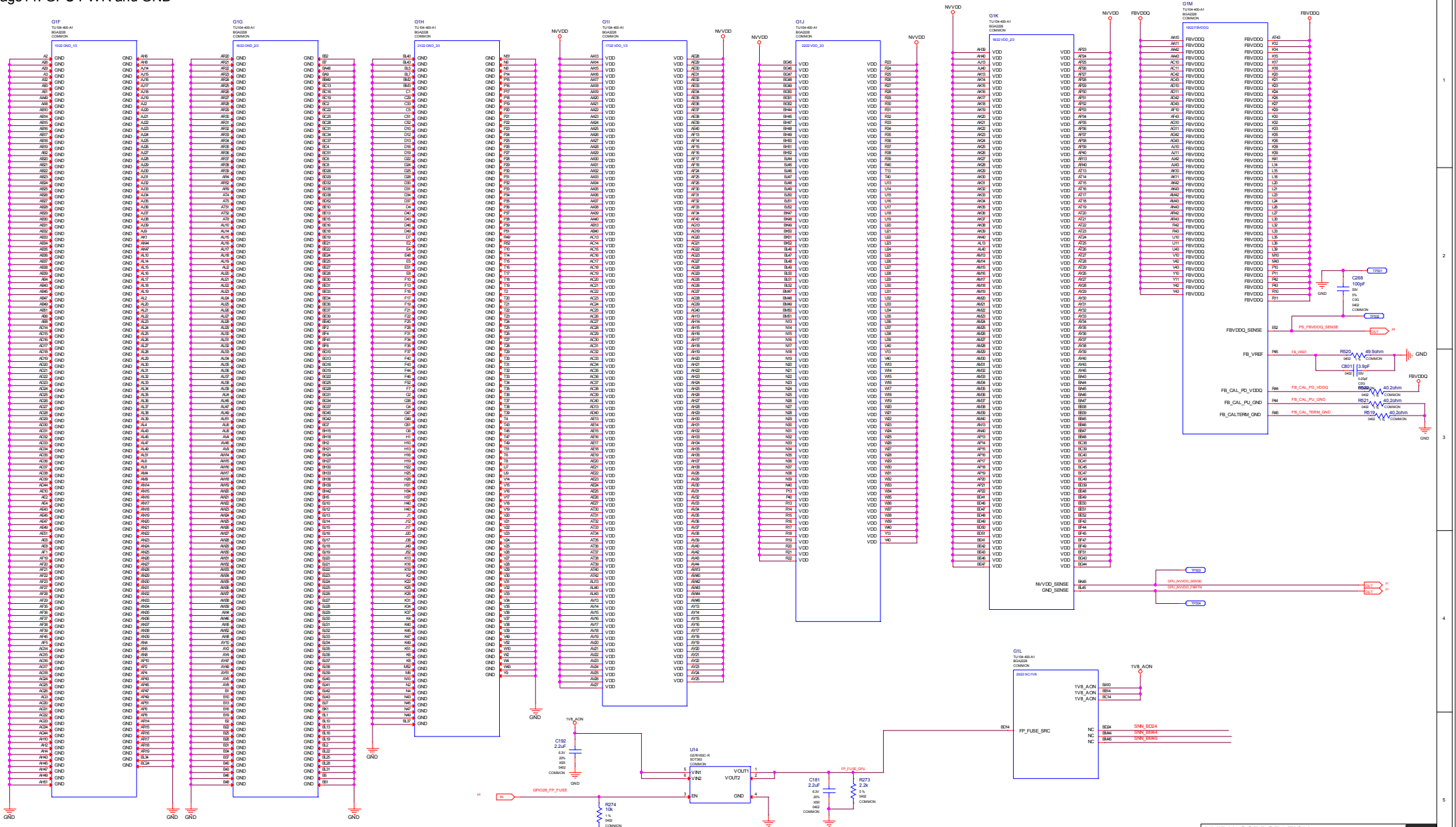
Page14: GPU PWR and GND



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU PWR & GND

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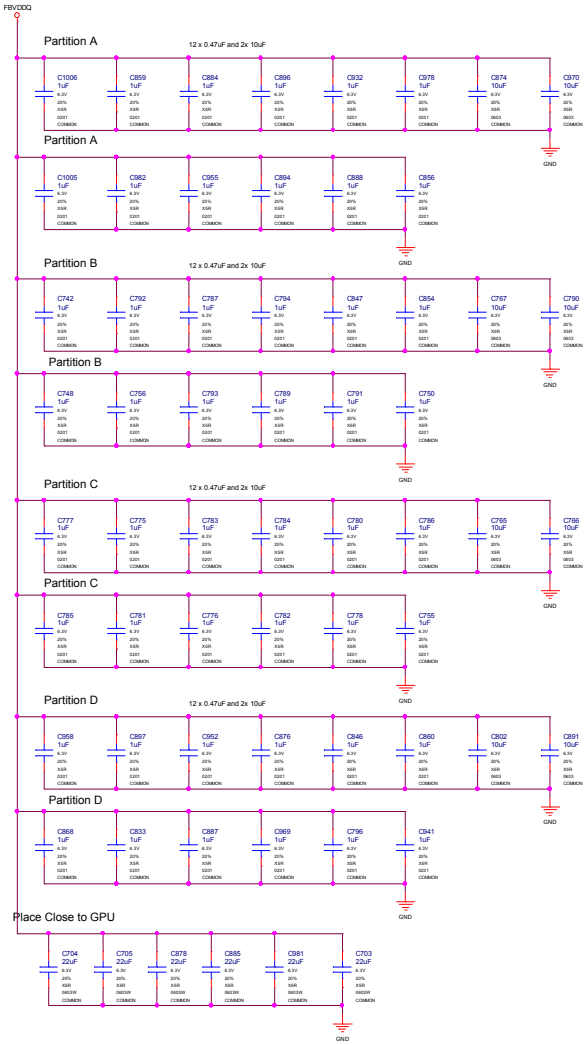
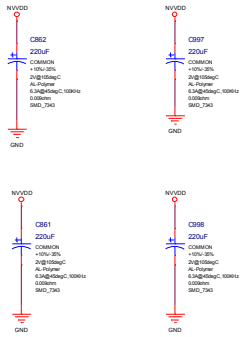
Page15: GPU Decoupling 1

FBVDDQ



NVVDD



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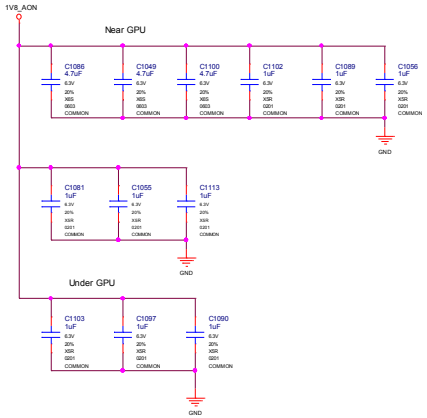

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PAGE DETAIL	GPU Decoupling

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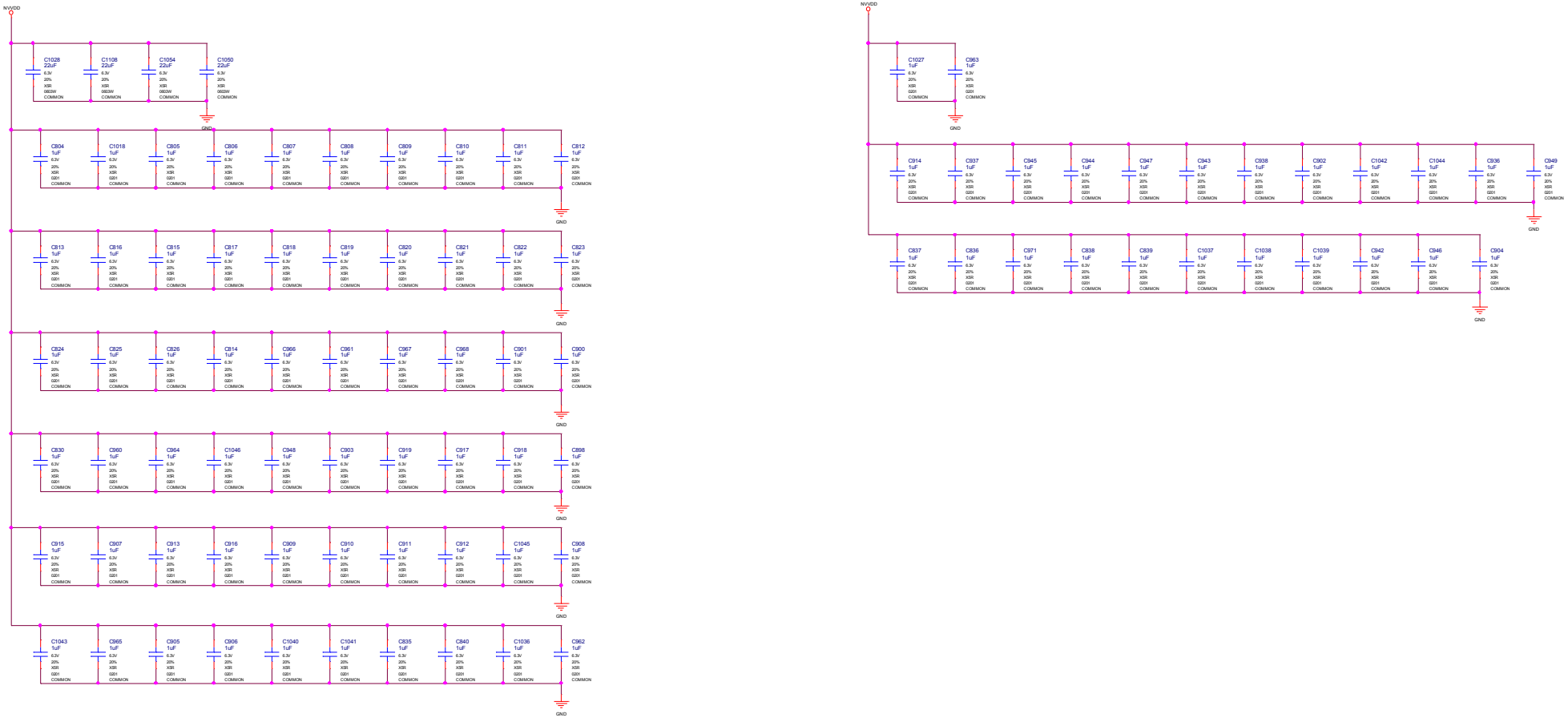
Page16: GPU Decoupling 2

NVVDD



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU Decoupling2

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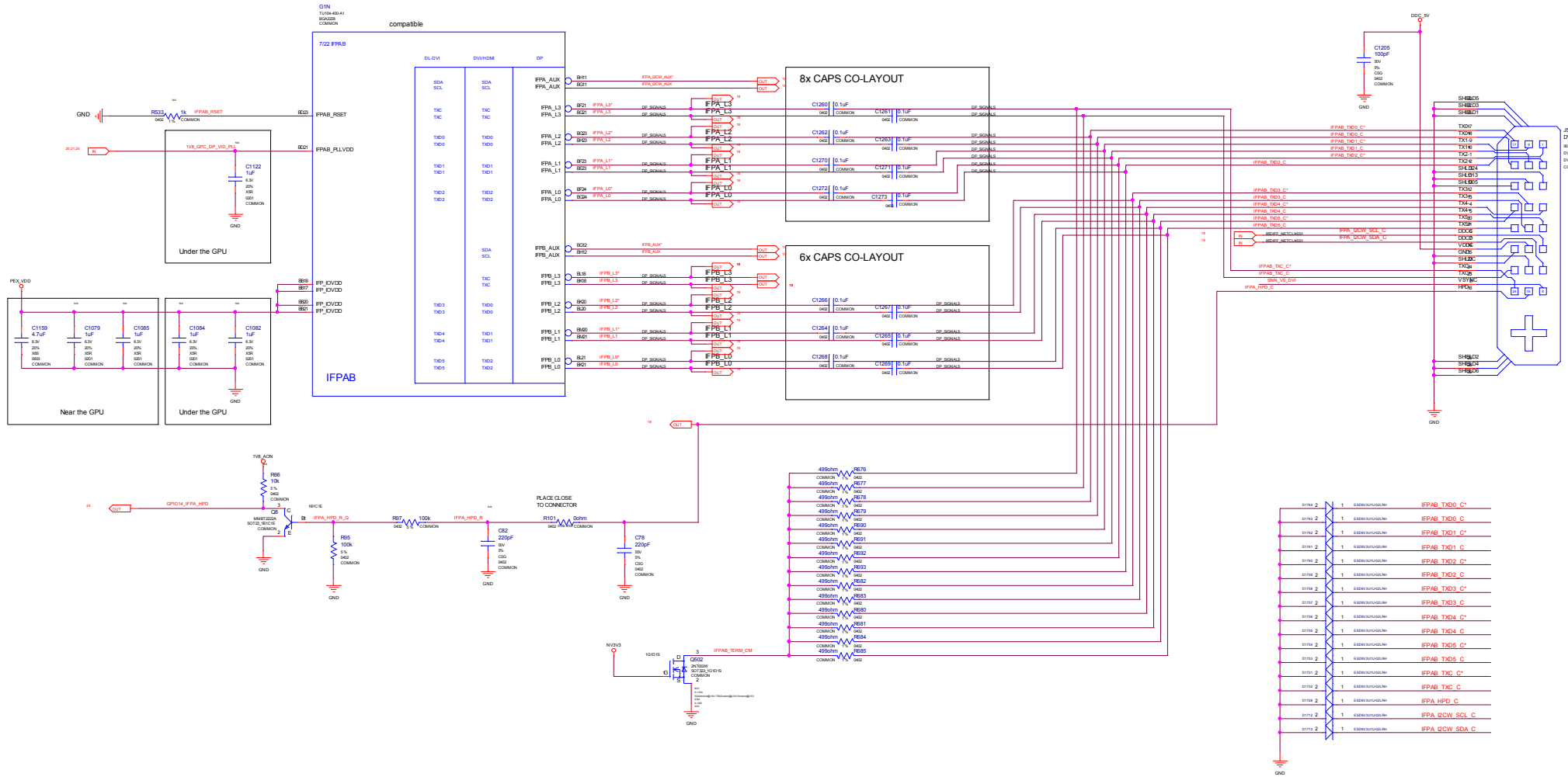
IFPAB DVI-D-DL CO-LAYOUT WITH 2x DP



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	ID: IFPAB DVI-D-DL

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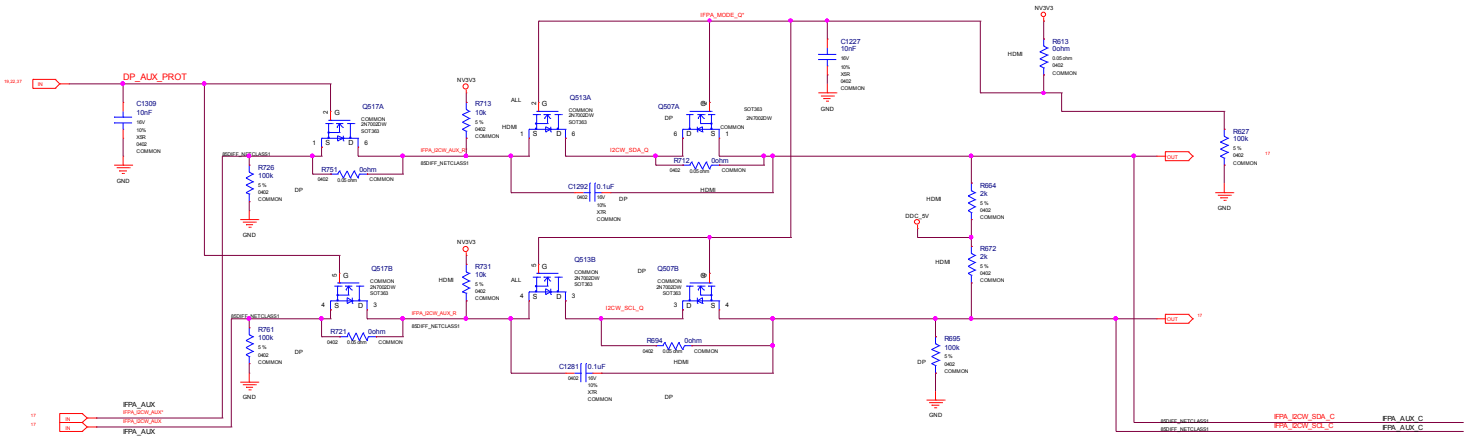

IFPA DP CO-LAYOUT WITH IFPAB DVI-D-DL

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	ID: IFPA DP

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IFPB DP CO-LAYOUT WITH IFPAB DVI-D-DL

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	ID: IFPB DP

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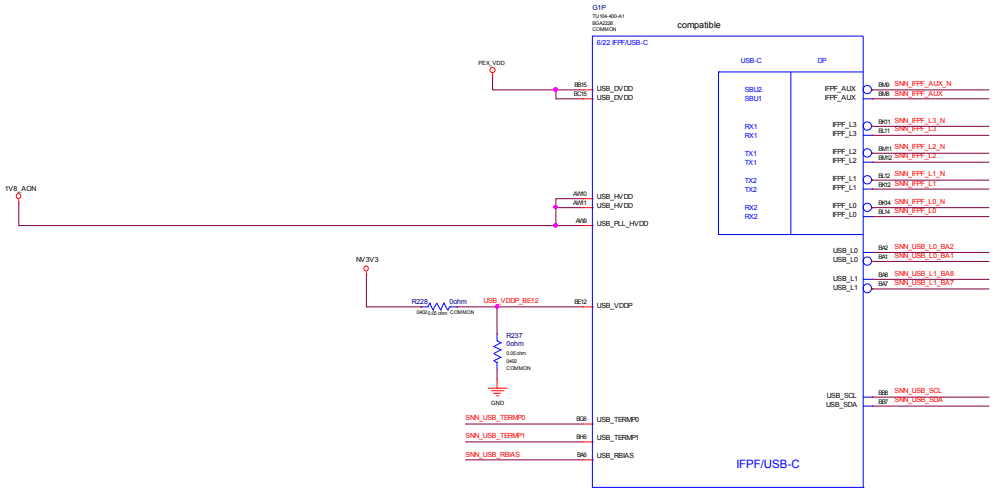
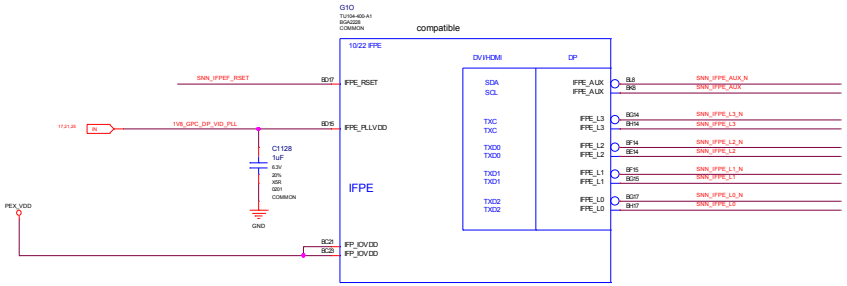
Page20: IFPE & IFPF USB-C NC



IFPF NC



IFPE NC

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	

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IC: IFPE & IFPF USBC NC

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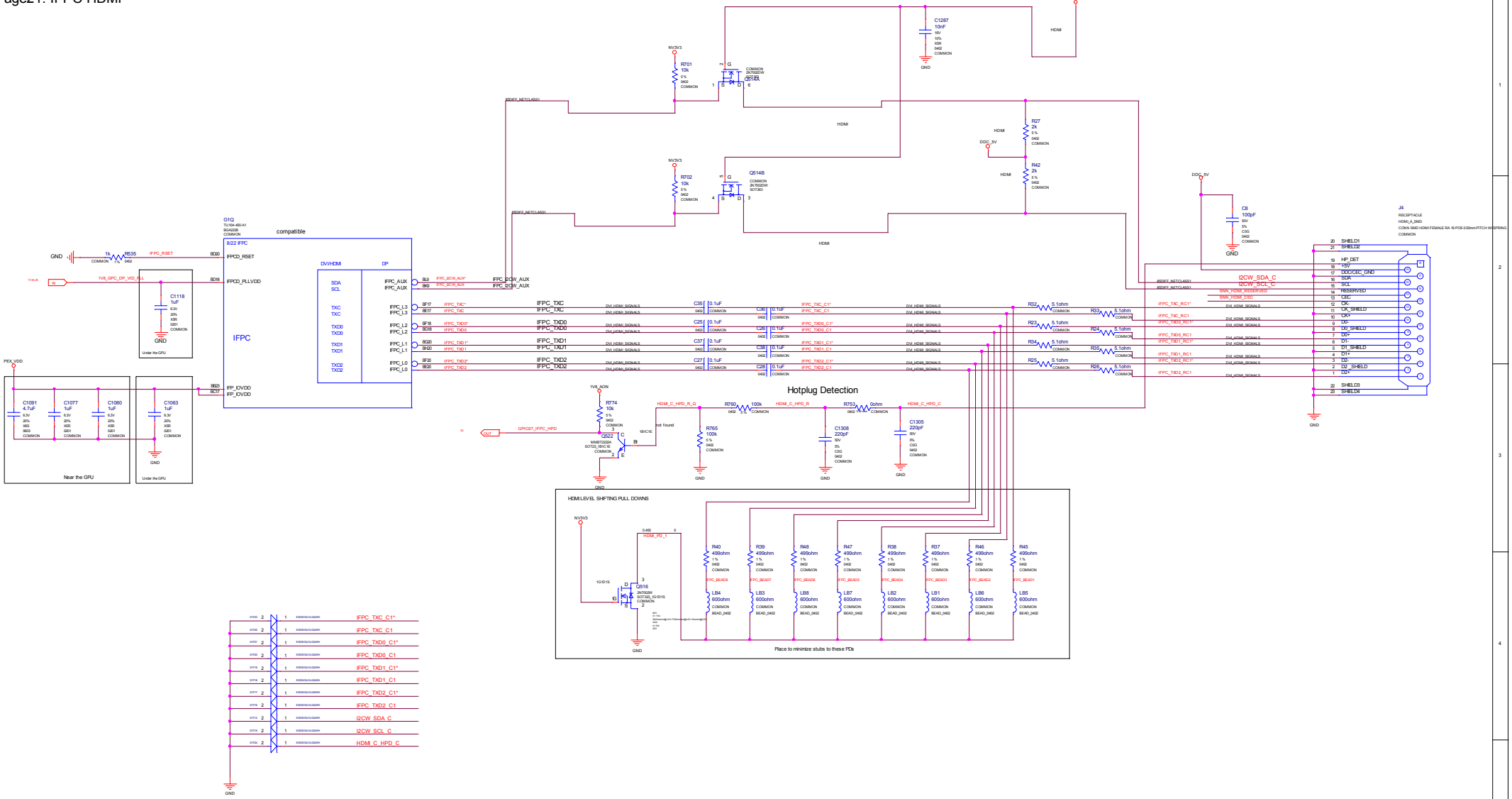
Page21: IFPC HDMI



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFPC HDMI

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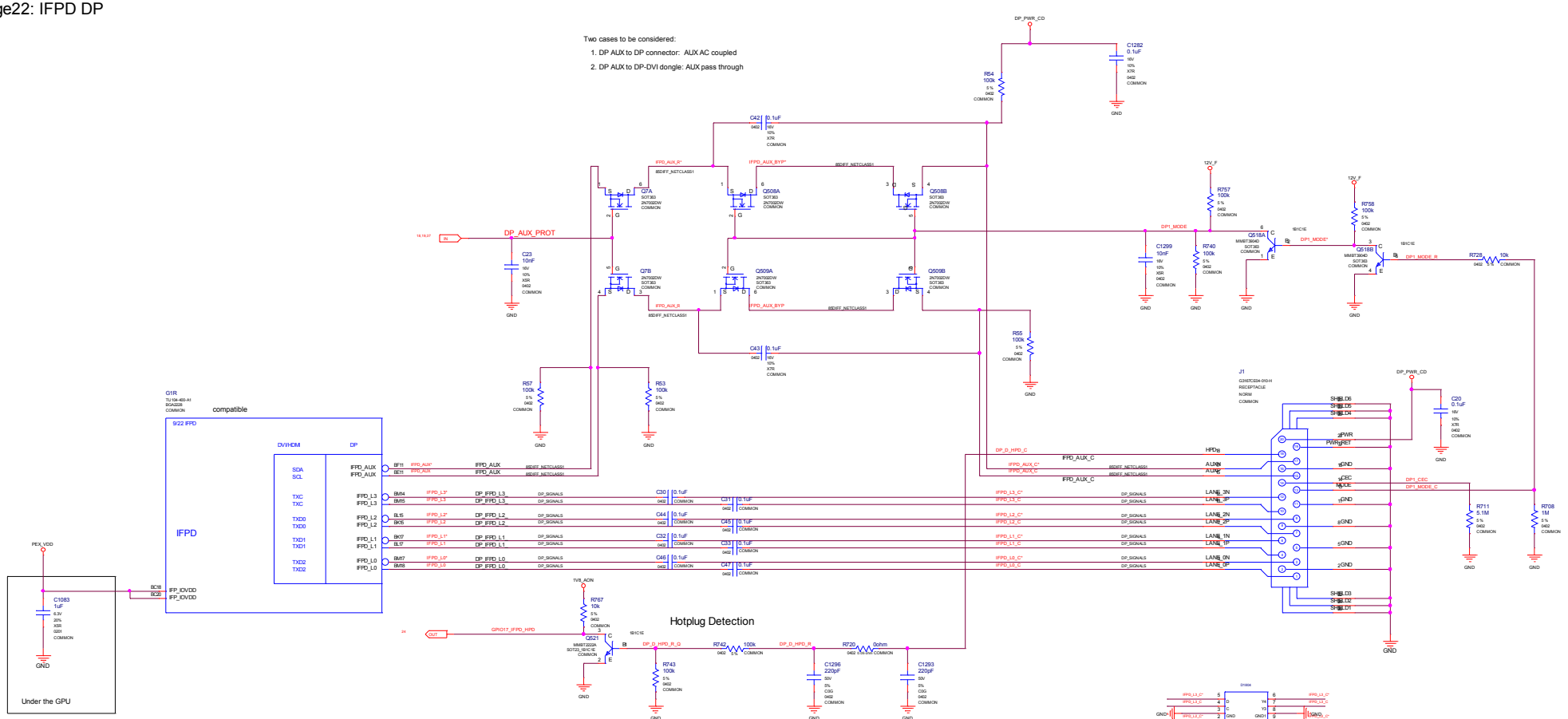
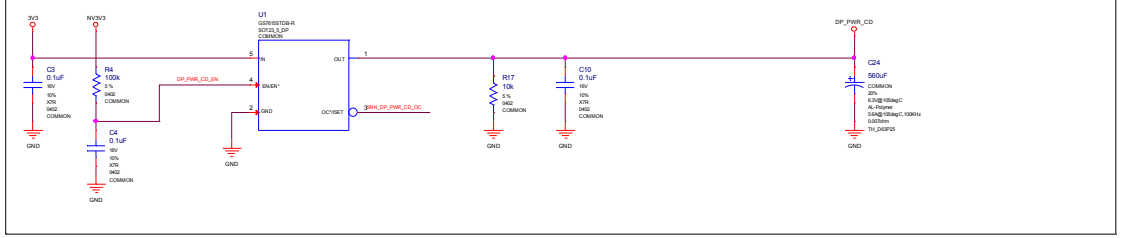
Page22: IFPD DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



Fused DP_PWR



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFPD DP

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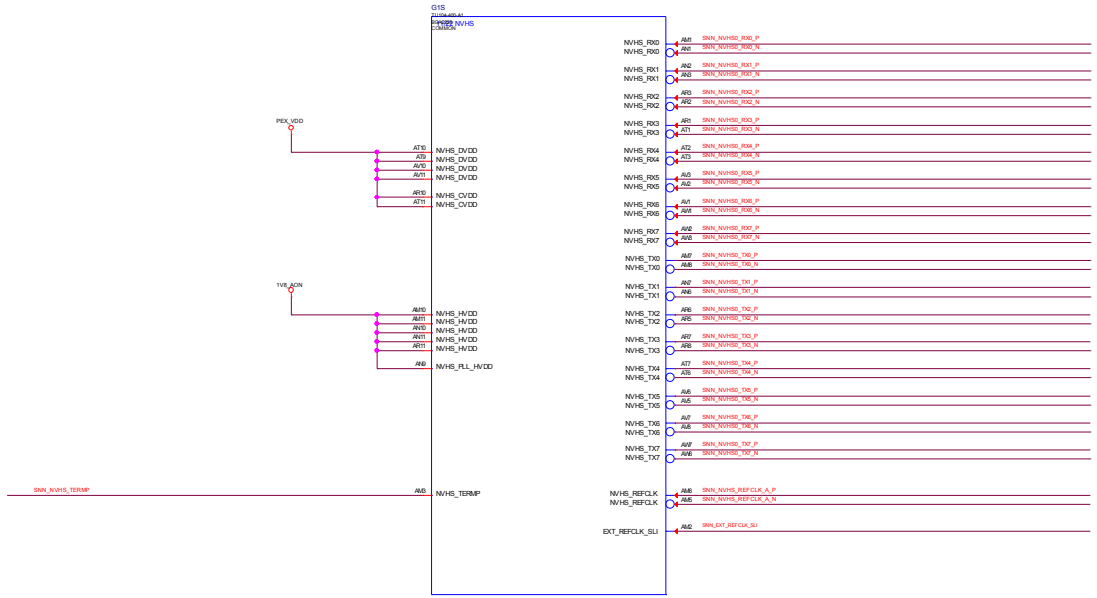
Page23: NVHS Interface and Frame Lock



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	ID: NVHS Interface and Frame Lock

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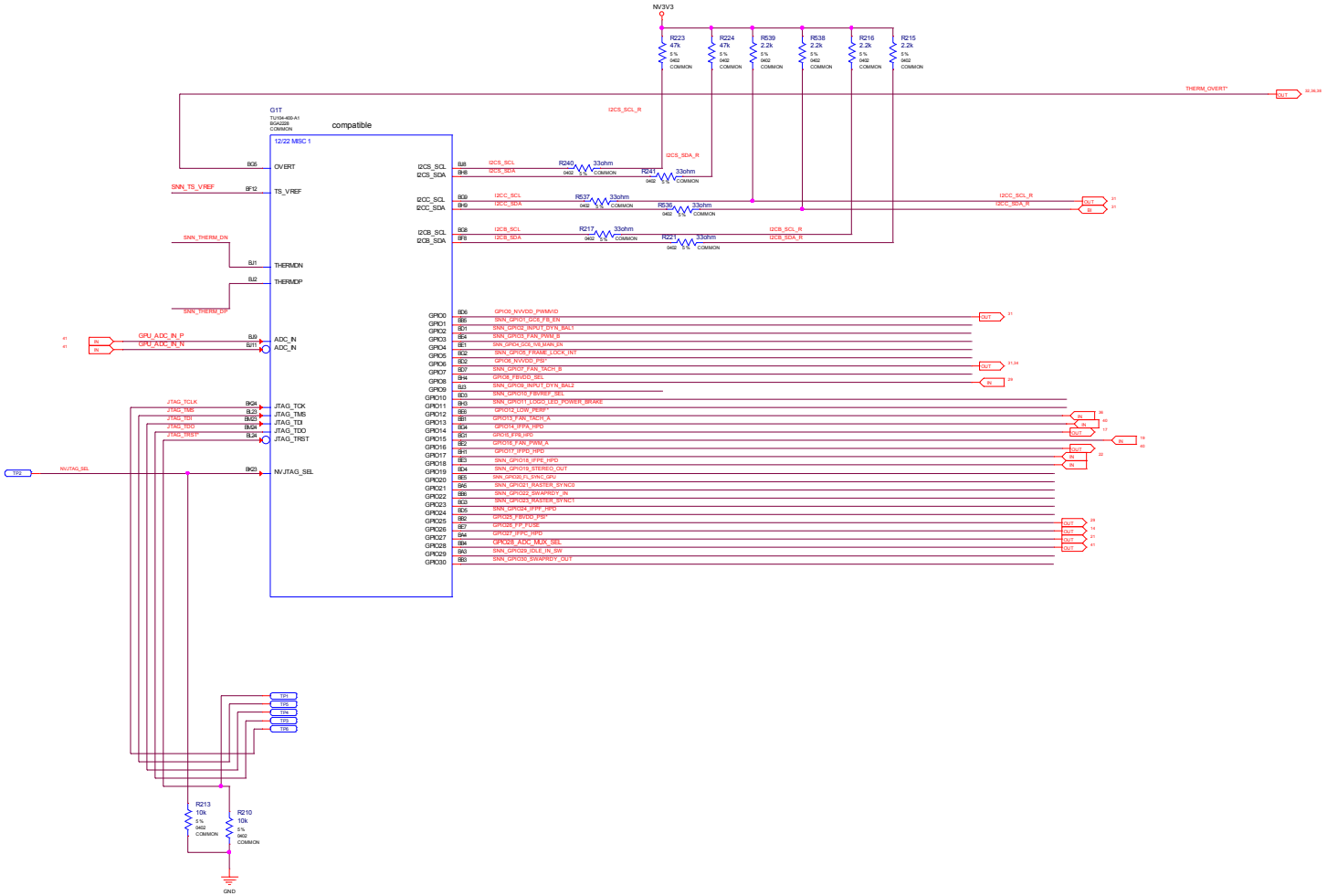
Page24: MISC1: Fan, Thermal, JTAG, GPIO



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC1: Thermal, JTAG, GPIO,STEREO

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Page25: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

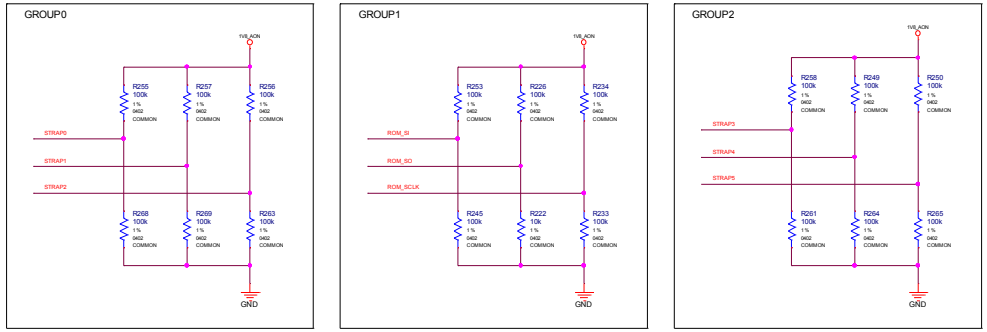
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

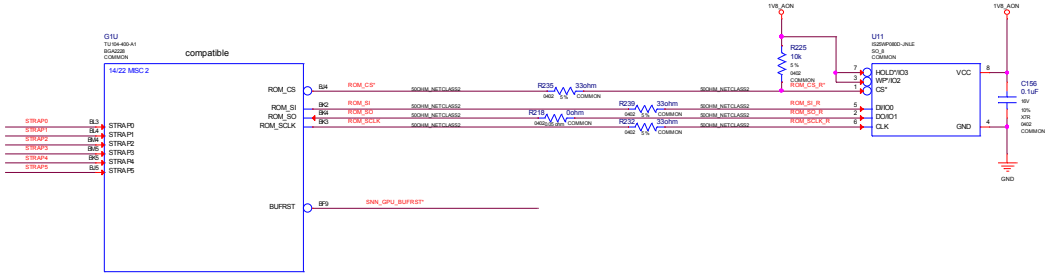
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

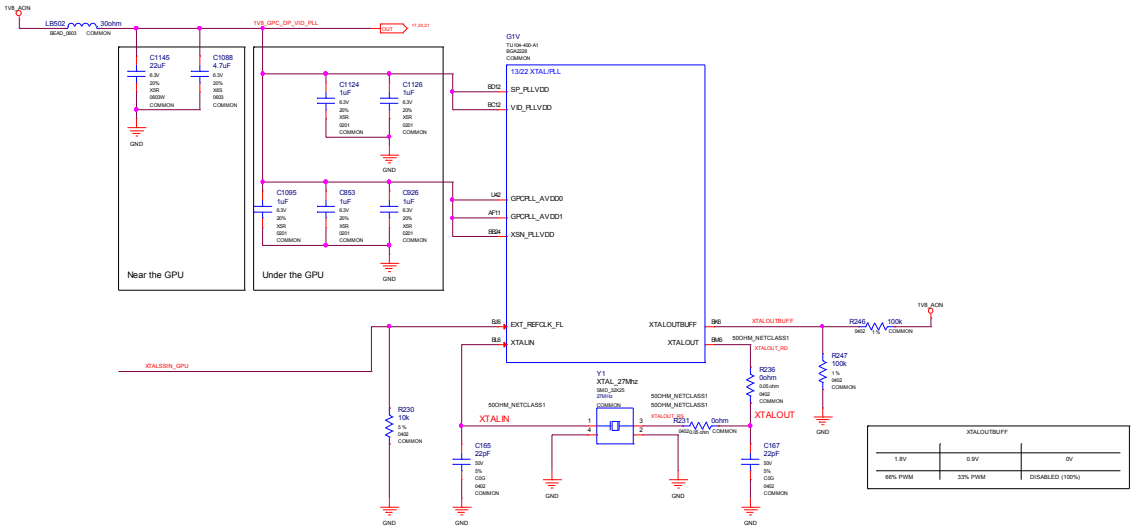
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE







XTALOUTBUFF		
1.8V	0.9V	0V
66% PWM	33% PWM	DISABLED (100%)

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC2: ROM, XTAL,STRAPS

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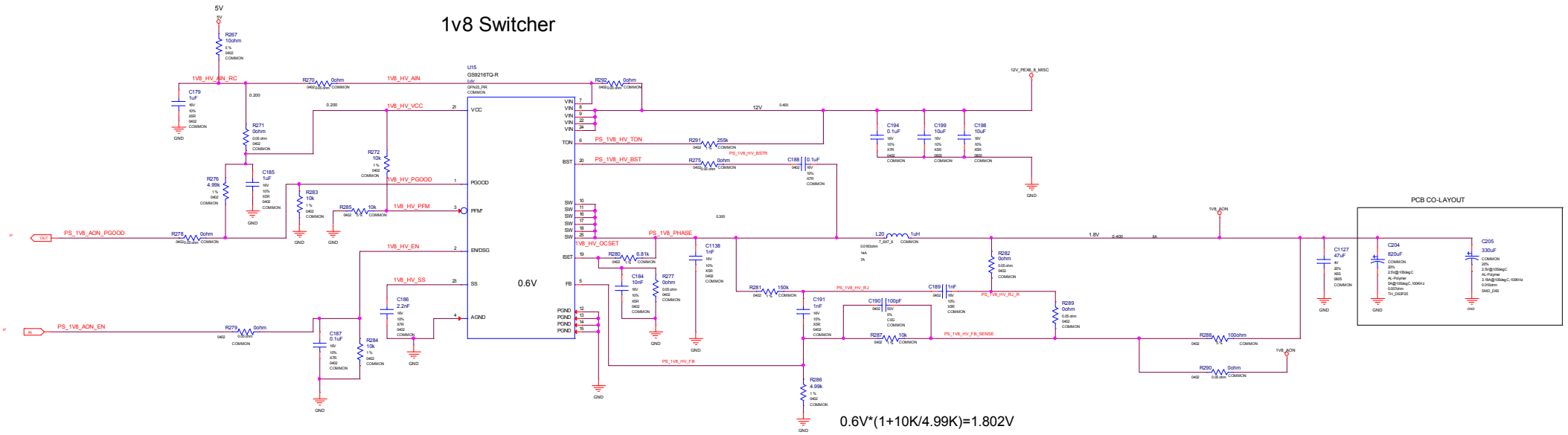
Page26: PS: 1V8_AON



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: 1V8_AON

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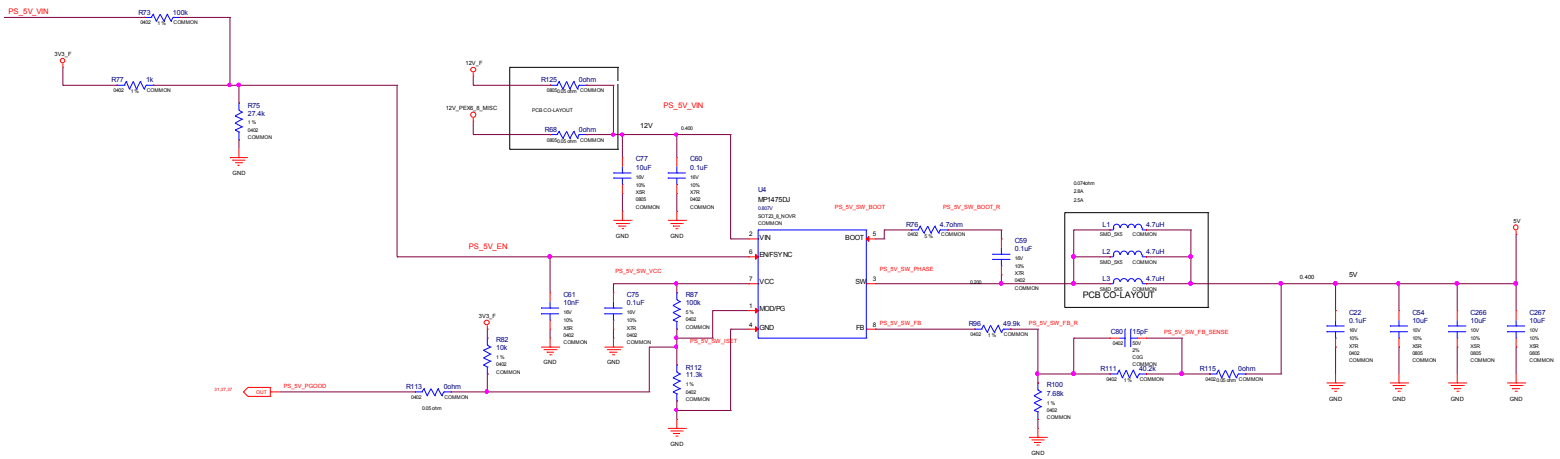
Page27: PS: 5V



0.8V*(1+40.2K/7.68K)=4.9875V

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: 5V

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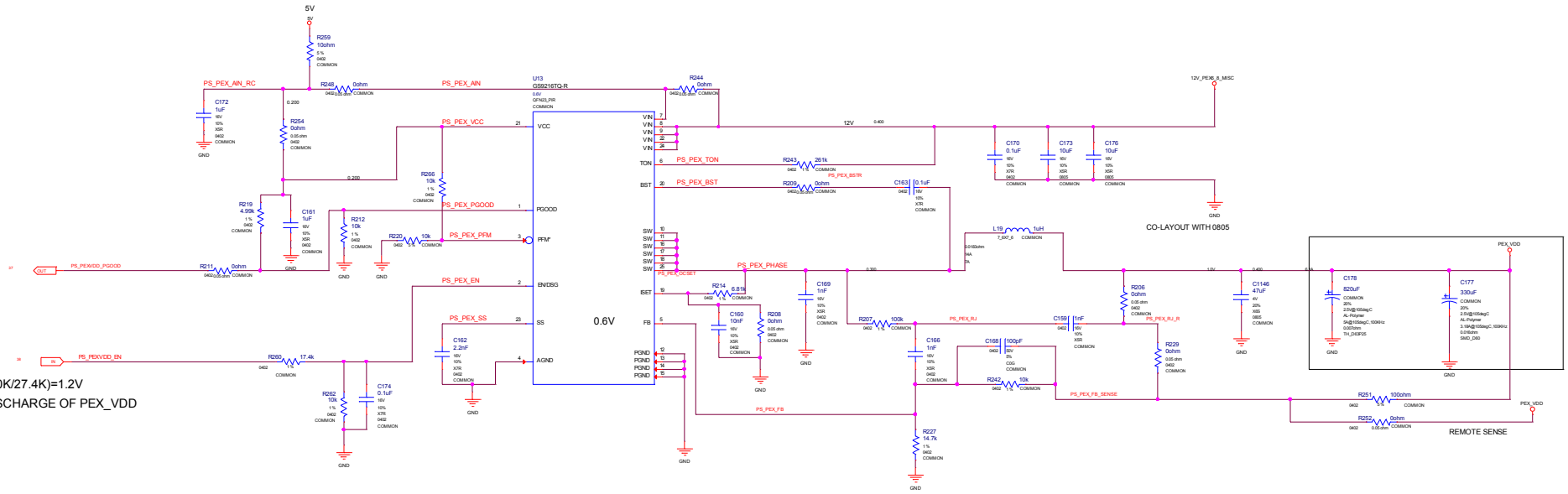
PEX Switcher



EN: 3.3V*(10K/27.4K)=1.2V

ENABLE DISCHARGE OF PEX_VDD

0.6V*(1+10K/14.7K)=1.008V

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: PEXVDD

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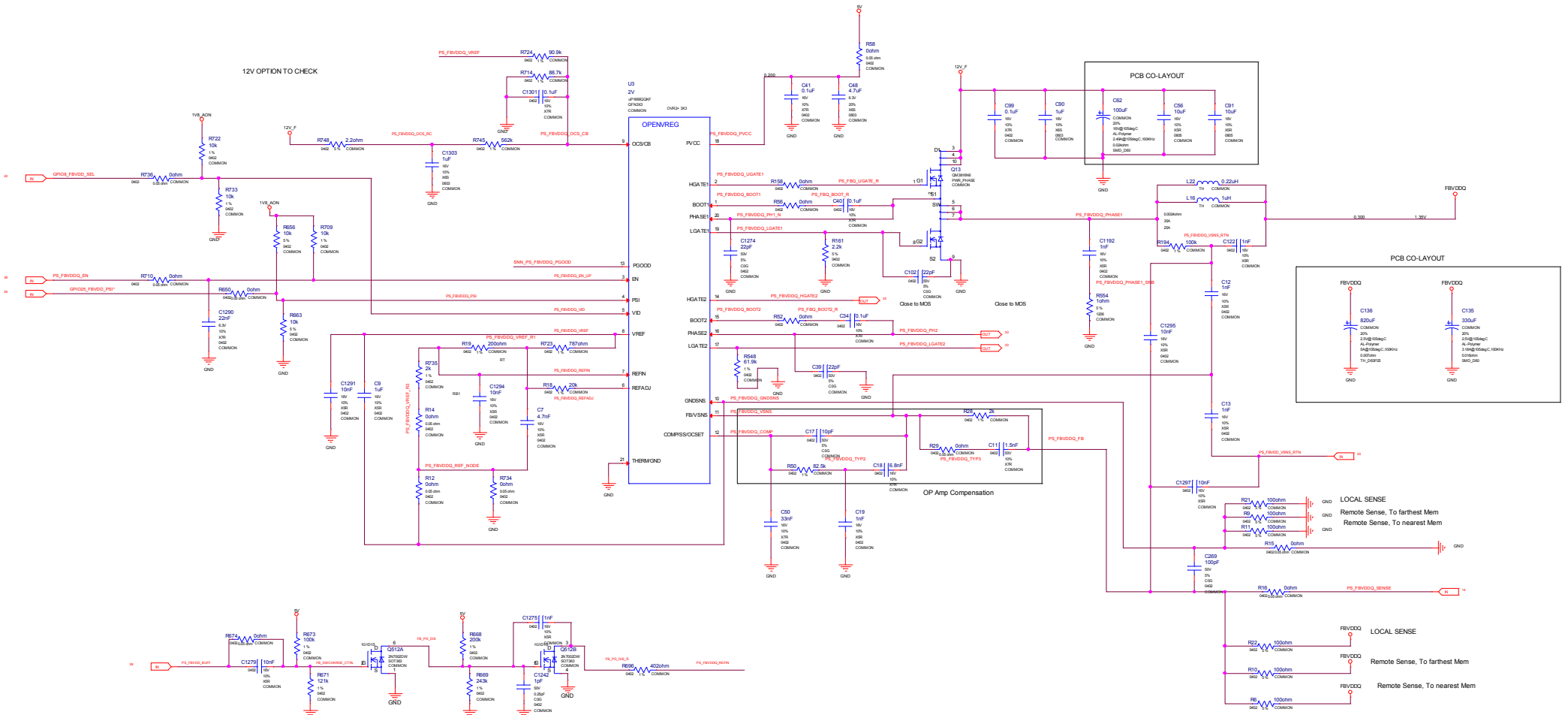
Page29: PS: FBVDDQ



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: FBVDDQ

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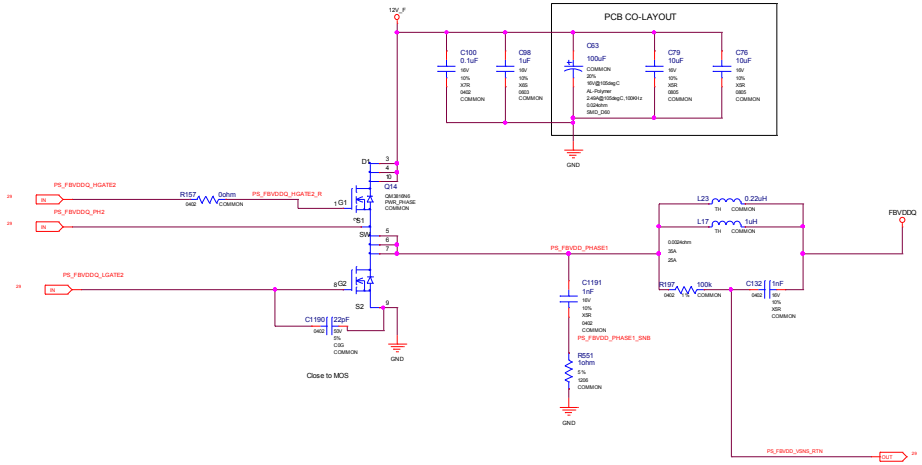
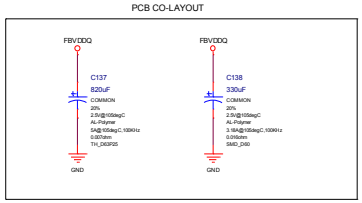
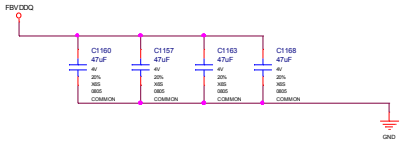
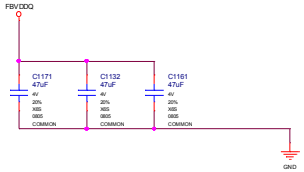
Page30: PS: FBVDDQ PH2









ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: FBVDDQ PH2

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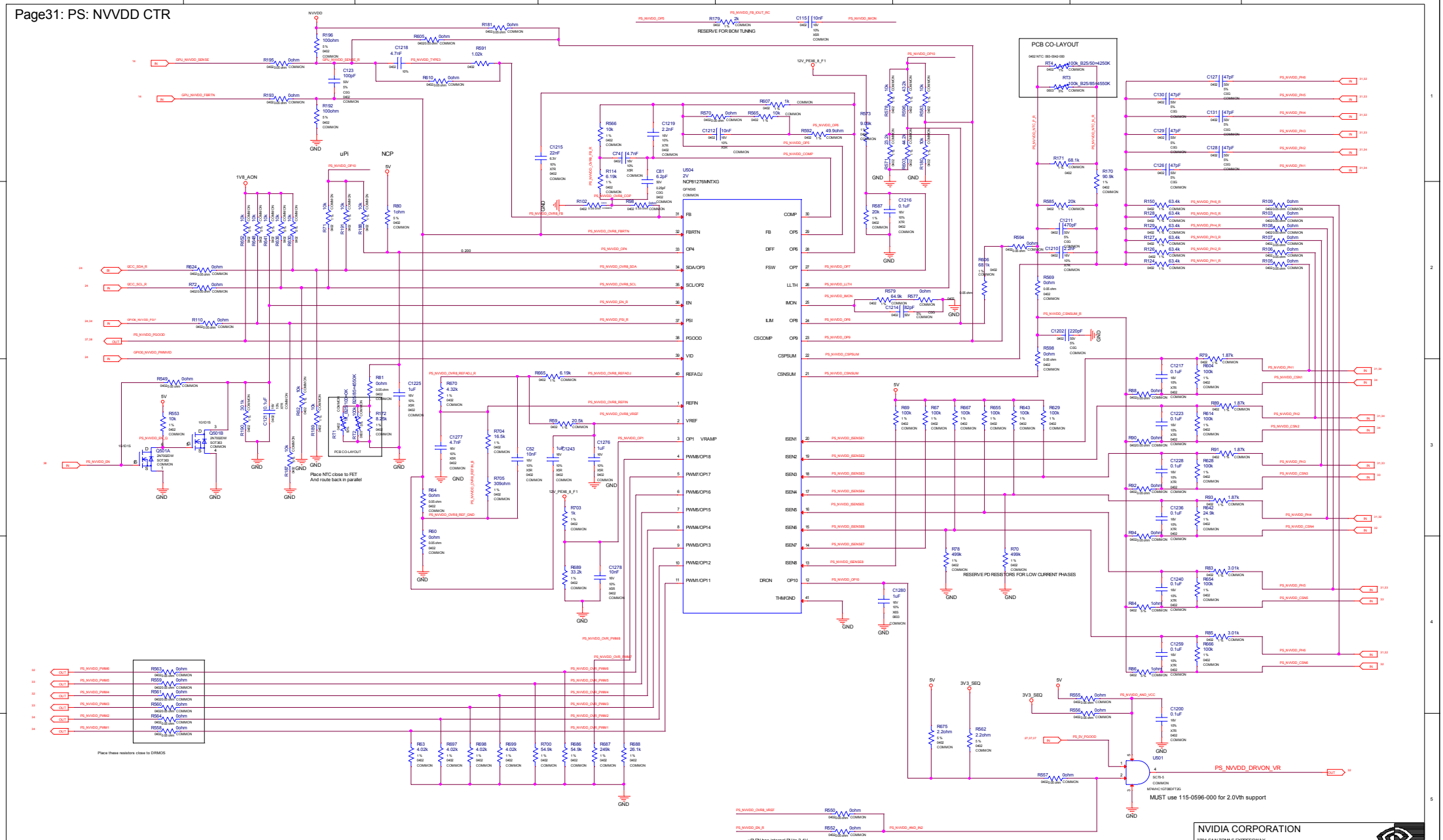
Page31: PS: NVVDD CTR



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD Controller

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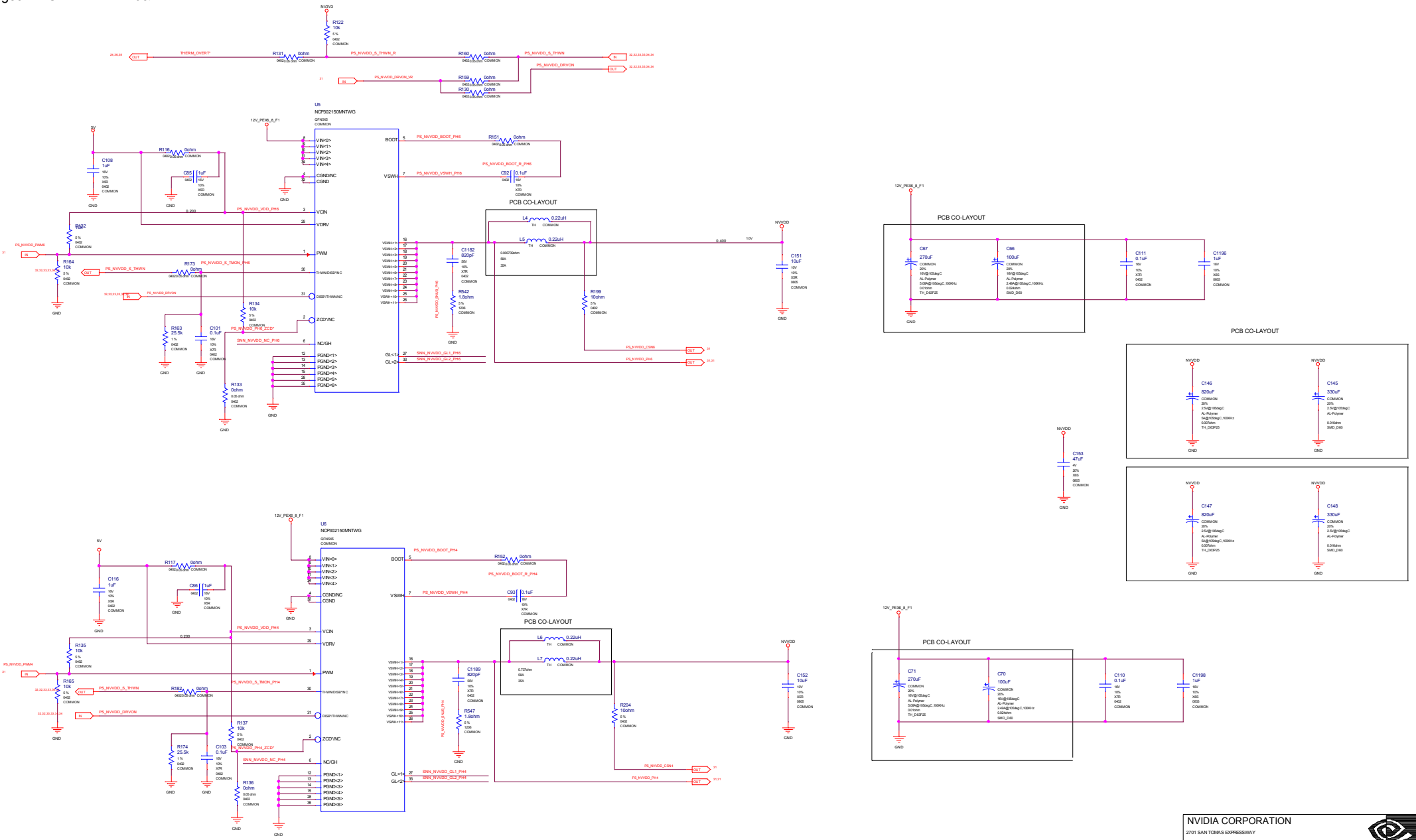
Page32: PS: NVVDD PH6&4



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PAGE DETAIL	PS: NVVDD Phase 6,4

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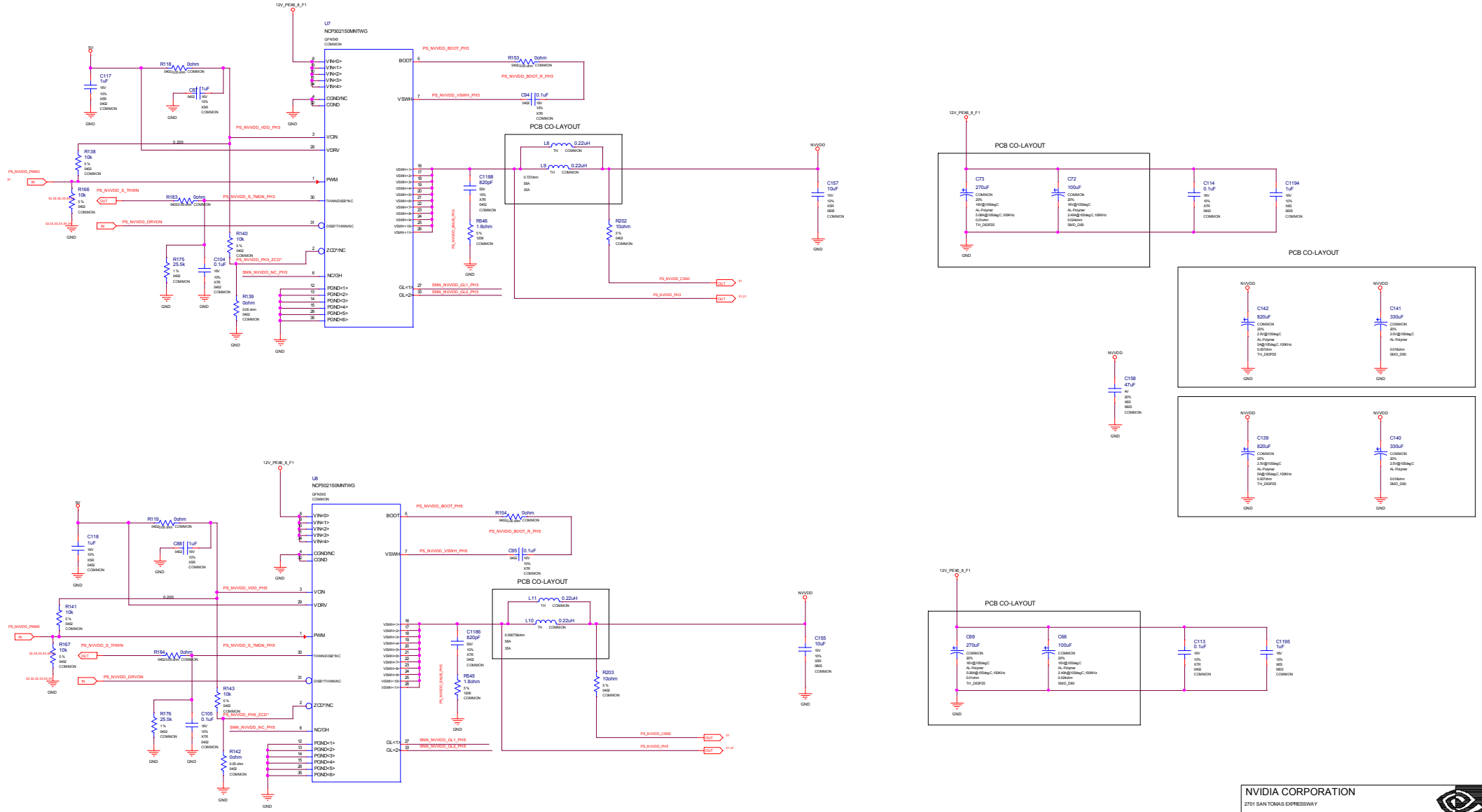
Page33: PS: NVVDD PH3&5



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD Phase 3,5

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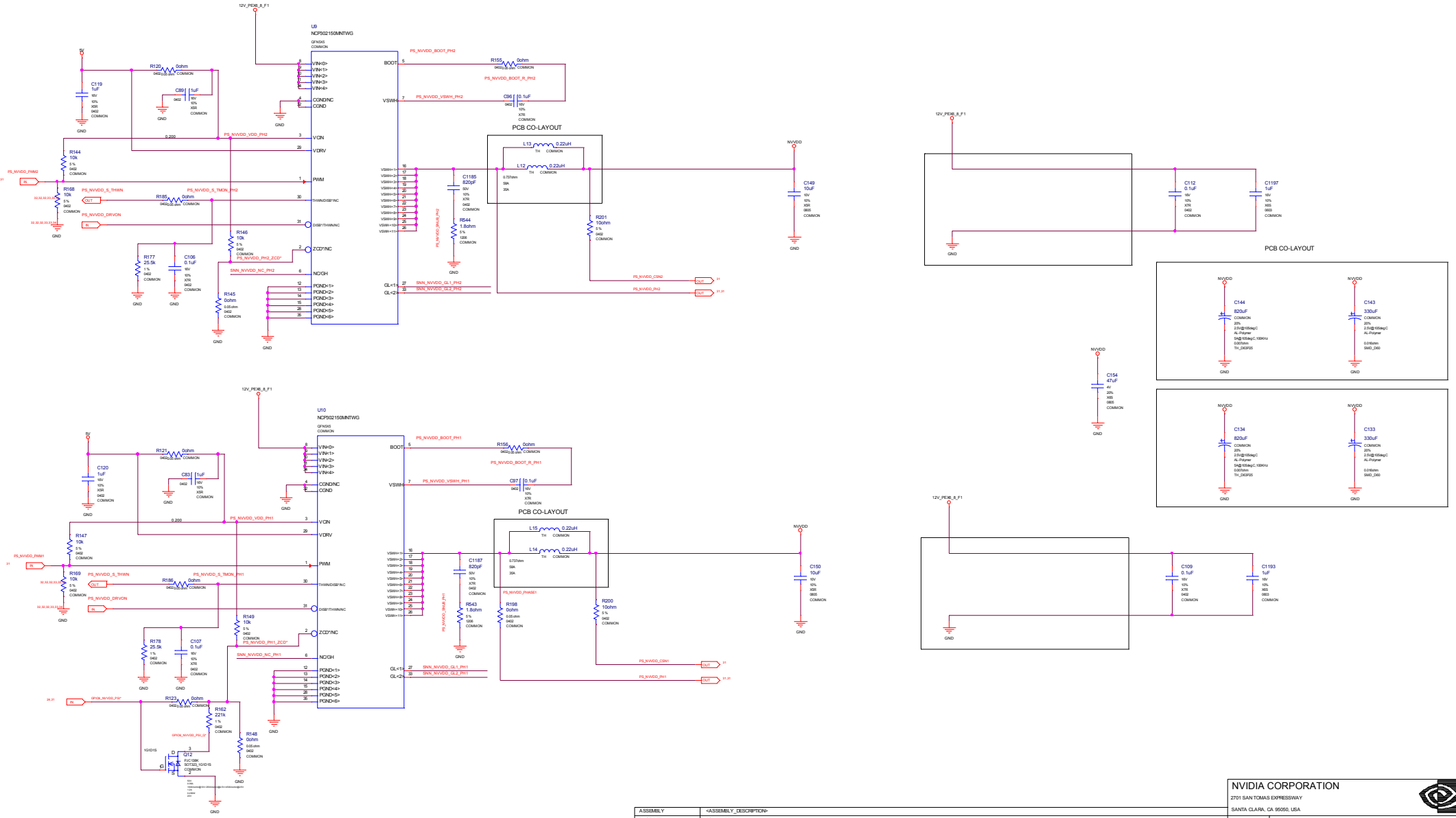
Page34: PS: NVVDD PH2&1



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD Phase 2,1

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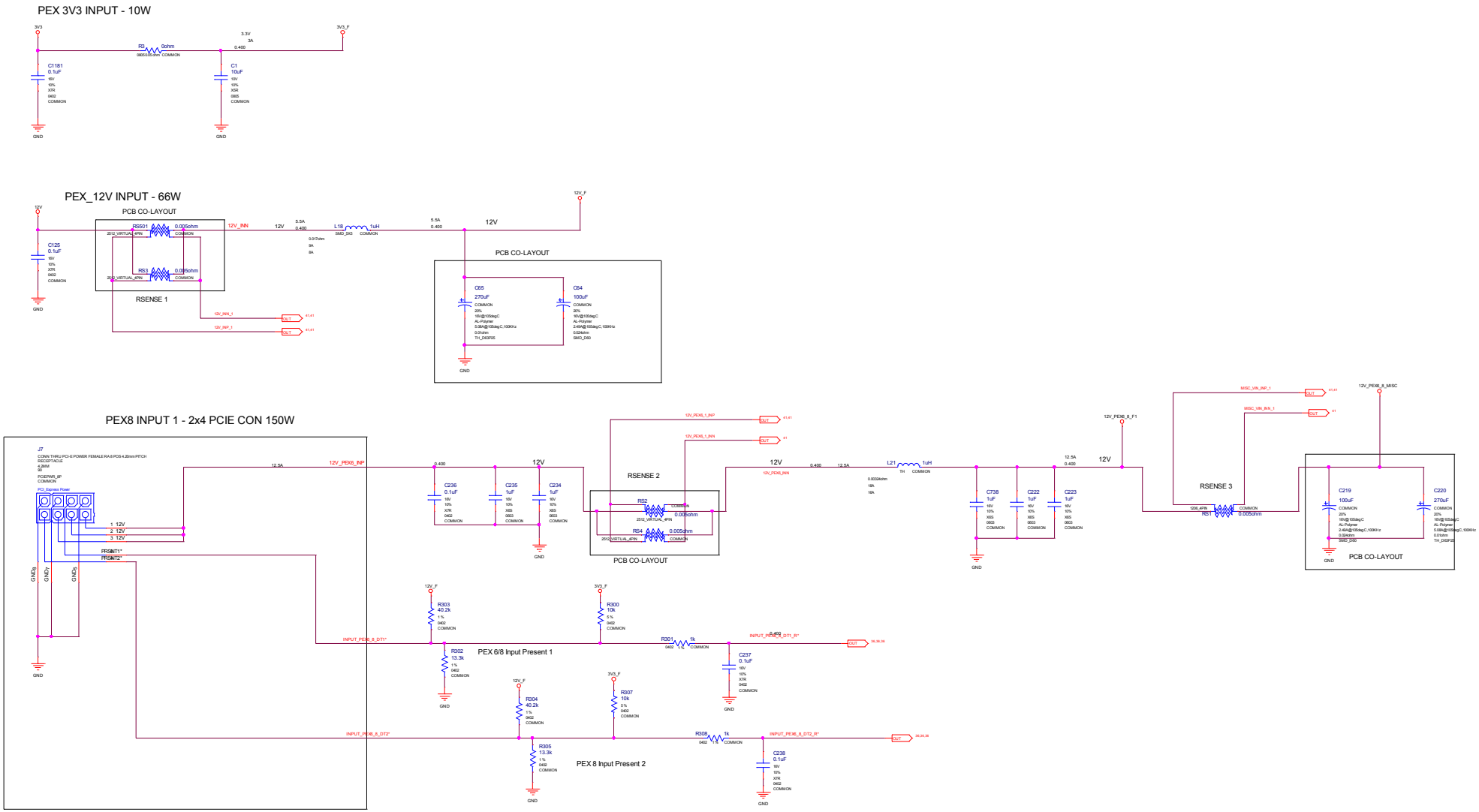
Page35: PS: Inputs, Filtering, and Monitoring



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Input, Filtering, and Monitoring

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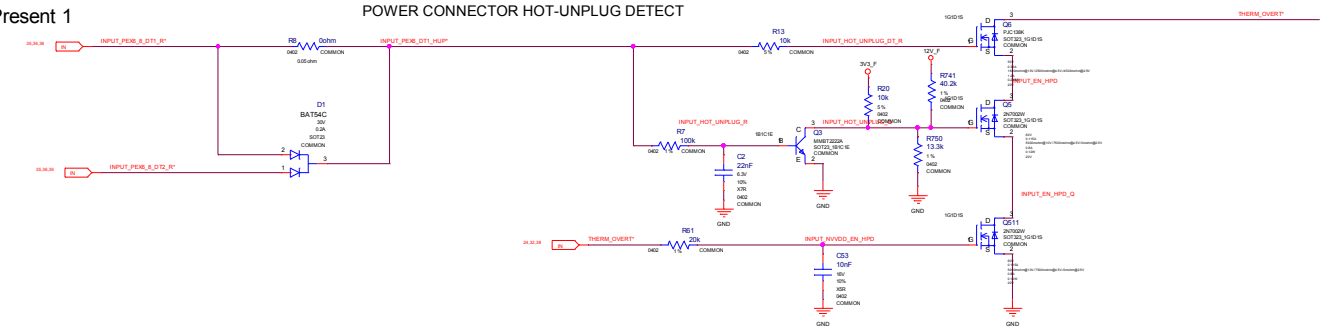
Page36: PS: HOT-UNPLUG, UNDER POWER BOOT, CURRENT STEERING

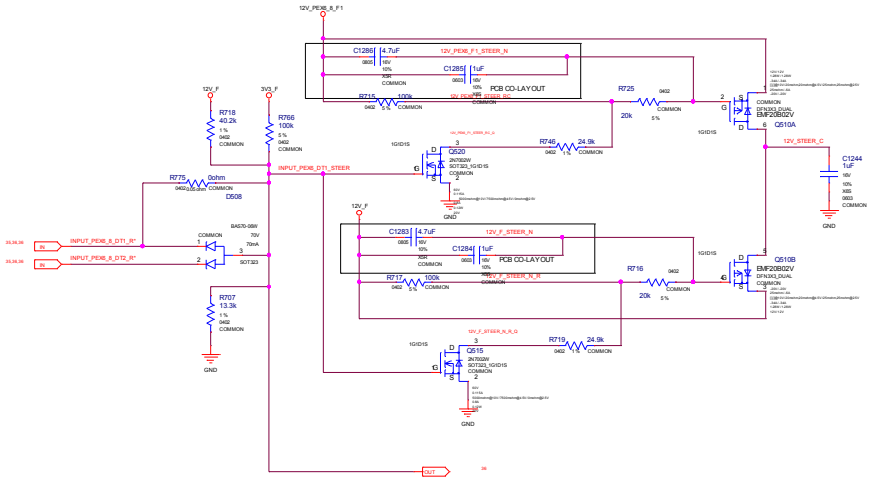
PEX Input Present 1

POWER CONNECTOR HOT-UNPLUG DETECT

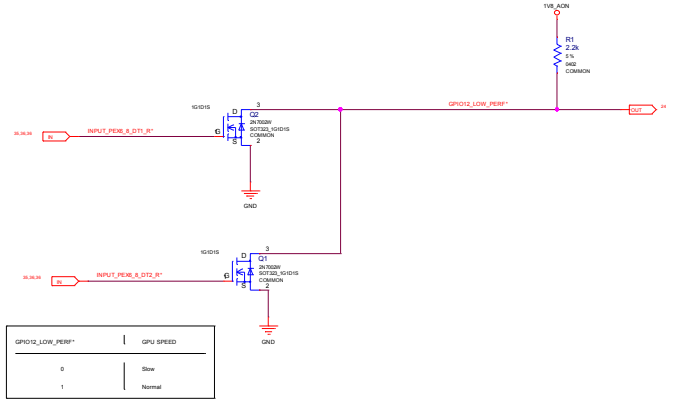


12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA



PEX Input - Power Level/PSI* Control



GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: STEERING, UPB & HOT-UNPLUG

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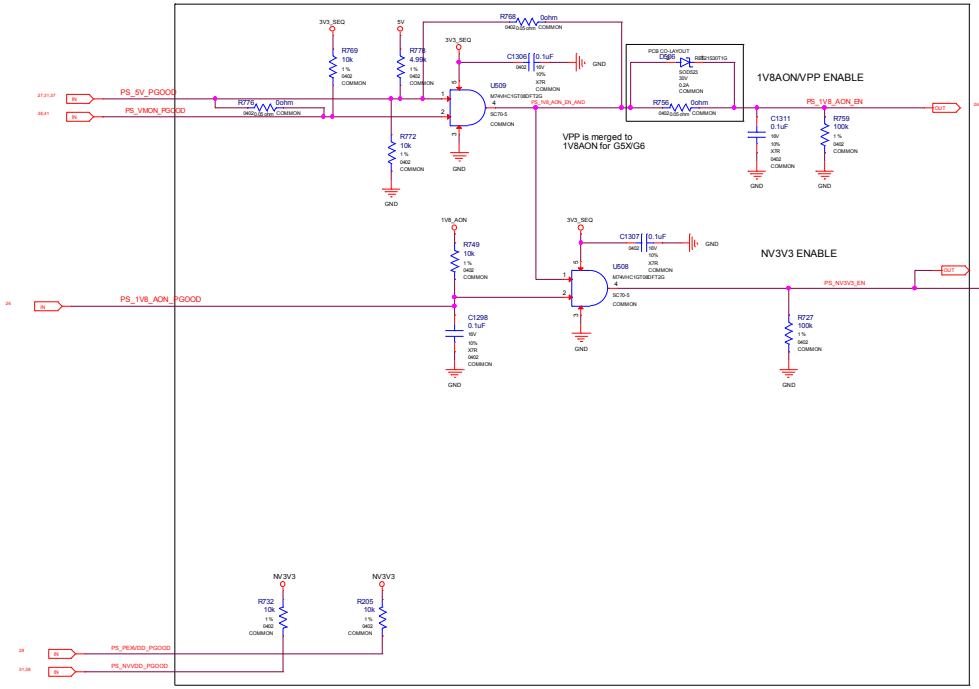
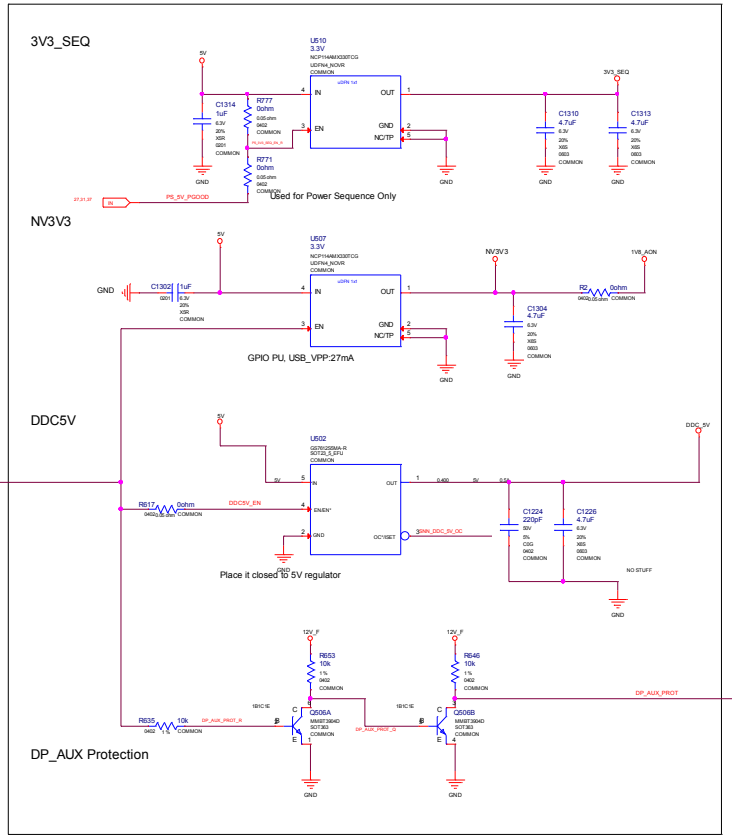
Page37: SEQ:5V,1V8,NV3V3 ENABLE





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PAGE DETAIL	SEQ: 5V, 1V8, NV3V3 ENABLE

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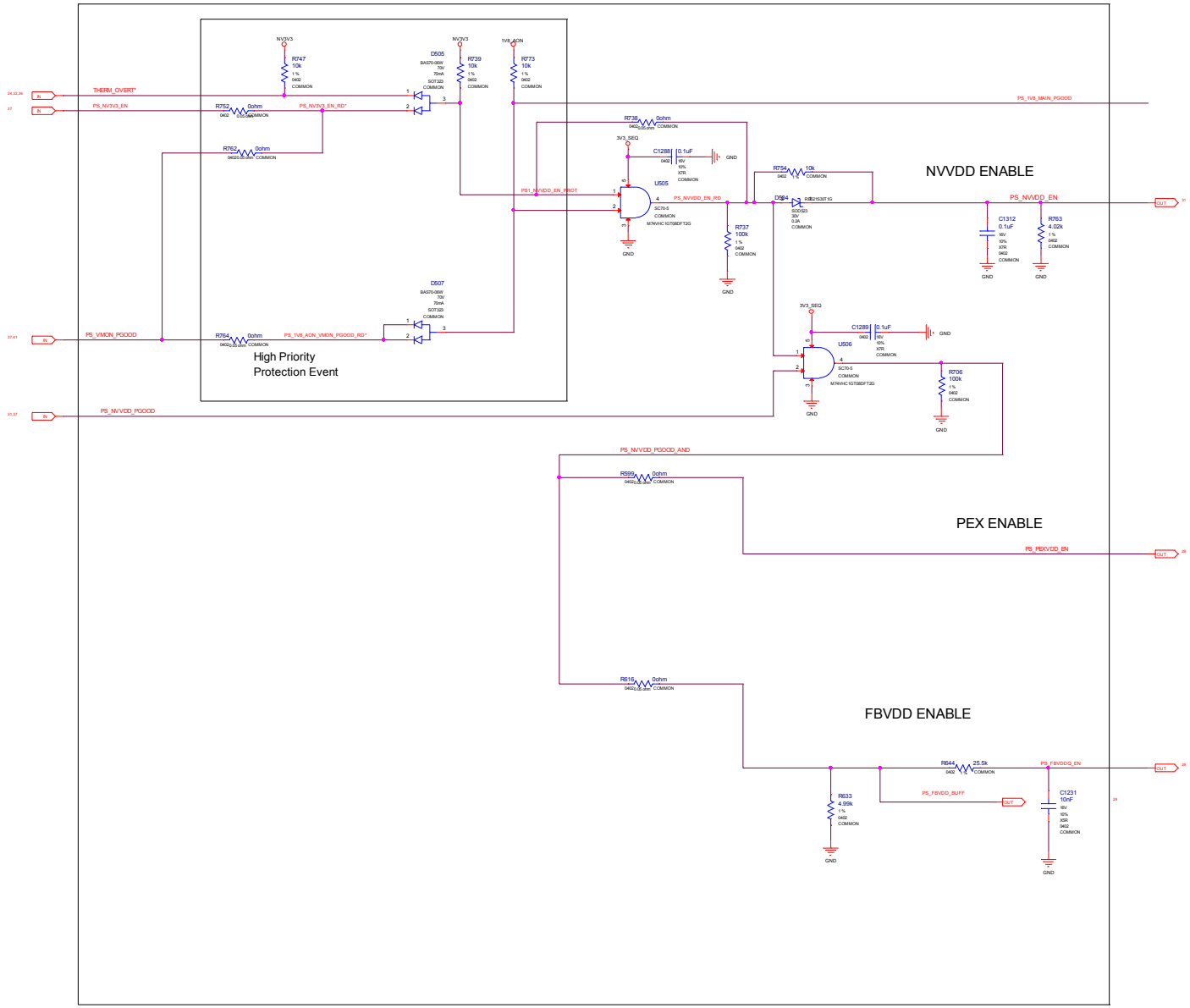
Page38: SEQ:NV,PEX,FB ENABLE



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQ: NV, PEX, FB ENABLE

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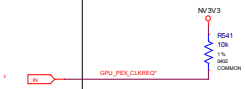
Page39: SEQUENCE:MISC

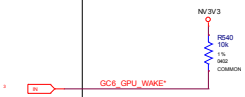
PEX_CLKREQ*



PU ON GPU SIDE

NC ON GOLD FINGER SIDE

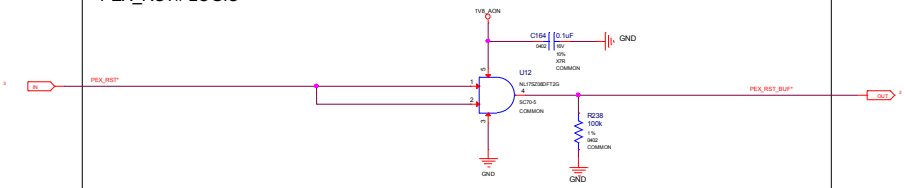
GPU_WAKE*



PU ON GPU SIDE

NC ON GOLD FINGER SIDE

PEX_RST# LOGIC



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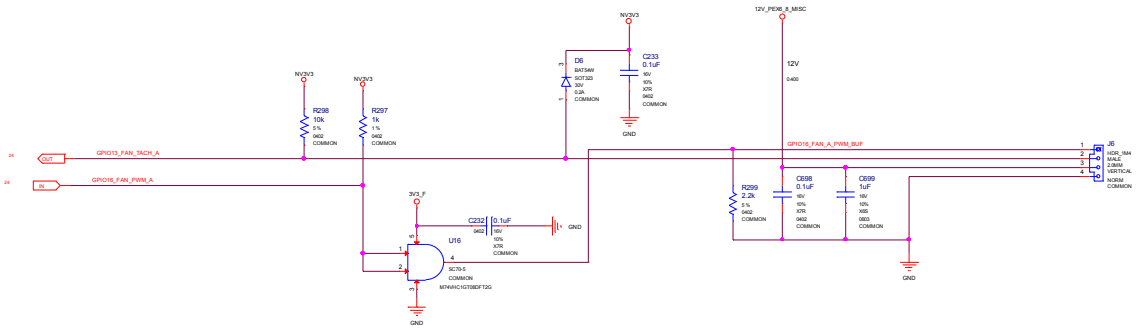
Page40: FAN



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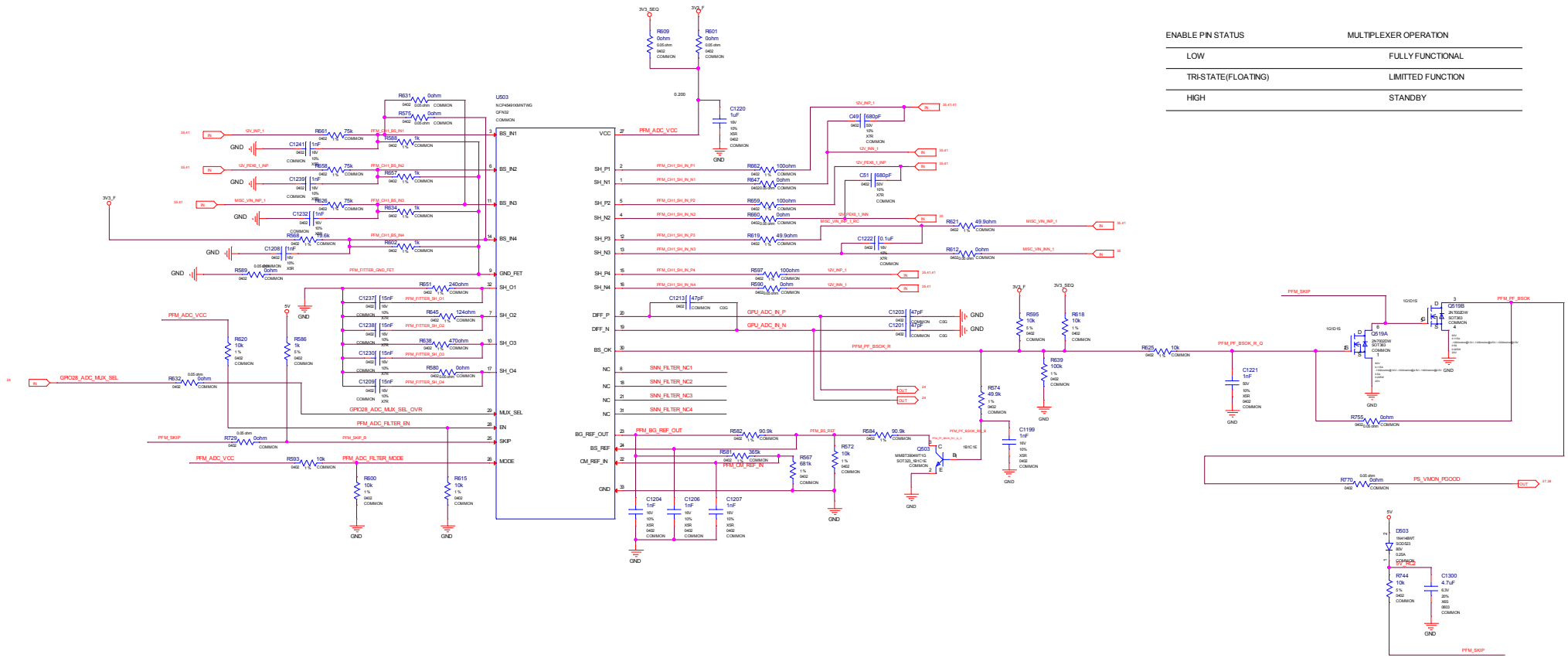
Page41: PWR SENSE

MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITTED FUNCTION
HIGH	STANDBY



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PAGE DETAIL	PS: Pre-filter

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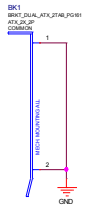
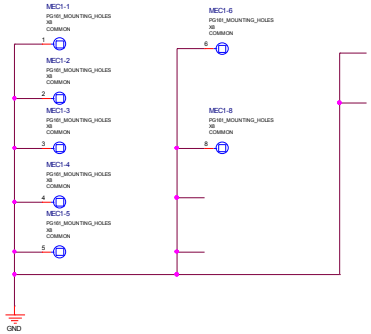
Page42: MECH

Bracket:



MOUNTING HOLES FOR HS:



BACK STIFFENER:

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MECH

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